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SCTWA35N65G2V

Silicon carbide Power MOSFET 650 V, 45 A, 75 mΩ (typ., T_J = 175 °C) in an HiP247™ long leads package

Datasheet - preliminary data

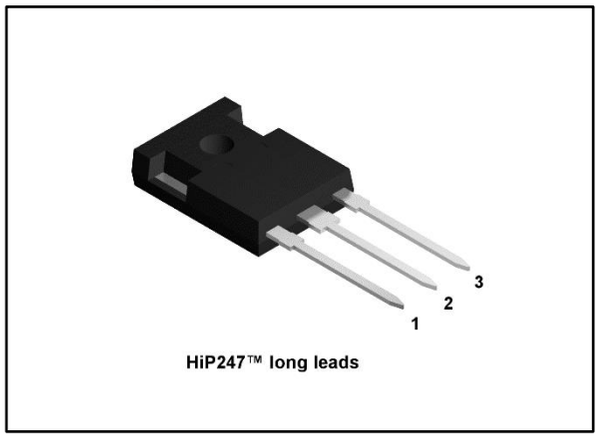
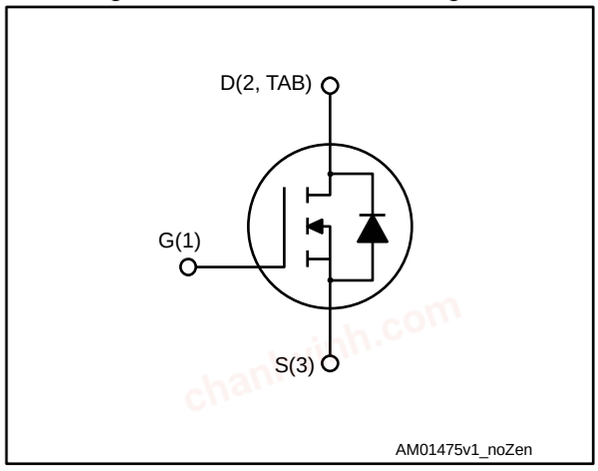


Figure 1: Internal schematic diagram



Features

- Very tight variation of on-resistance vs. temperature
- Very fast and robust intrinsic body diode
- Low capacitance

Applications

- Switching mode power supply
- EV chargers
- DC-DC converters

Description

This silicon carbide Power MOSFET has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of both on-resistance and switching losses is almost independent of junction temperature.

Table 1: Device summary

Order code	Marking	Package	Packing
SCTWA35N65G2V	SCT35N65G2V	HiP247™ long leads	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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Contents

1 Electrical ratings 3
2 Electrical characteristics 4
2.1 Electrical characteristics (curves) 6
3 Package information 9
3.1 HiP247 long leads package information 9
4 Revision history 11

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating range)	-5 to 20	
I_D	Drain current (continuous) at T_C = 25 °C	45	A
	Drain current (continuous) at T_C = 100 °C	35	
I_{DM}(1)	Drain current (pulsed)	90	A
P_{TOT}	Total dissipation at T_C = 25 °C	208	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		°C

Notes:

(1)Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.72	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	40	°C/W

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2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4: On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			50	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_J = 175 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±250	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	1.8	3.2		V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 20 V, I_D = 20 A		55	72	mΩ
		V_{GS} = 18 V, I_D = 20 A		63		
		V_{GS} = 20 V, I_D = 20 A, T_J = 175 °C		75		

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 400 V, f = 1 MHz	-	1370	-	pF
C_{oss}	Output capacitance		-	125	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 20 A, V_{GS} = 0 to 20 V	-	73	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	27	-	nC

Table 6: Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	V_{DD} = 400 V, I_D = 20 A, R_G= 4.7 Ω, V_{GS} = -5 to 20 V	-	100	-	µJ
E_{off}	Turn-off switching energy		-	35	-	µJ

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Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 20 A, R_G= 4.7 Ω, V_{GS} = -5 to 20 V	-	16	-	ns
t_f	Fall time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	35	-	ns
t_r	Rise time		-	9	-	ns

Table 8: Reverse diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	V_{GS} = 0 V, I_F = 20 A,	-	4.5	-	V
t_{rr}	Reverse recovery time	V_{DD} = 400 V, I_F = 20 A, di/dt = 1000 A/µs	-	18	-	ns
Q_{rr}	Reverse recovery charge		-	85	-	nC
I_{RRM}	Reverse recovery current		-	7	-	A

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2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

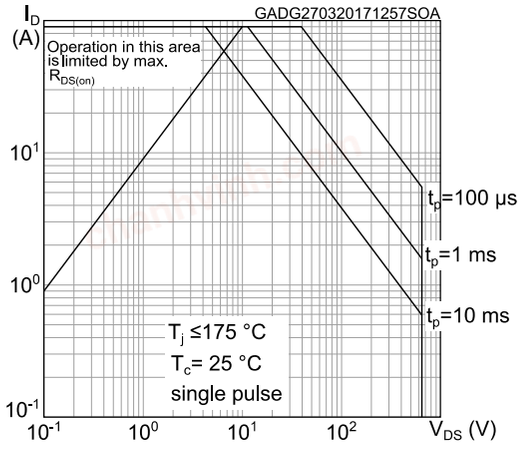


Figure 3: Thermal impedance

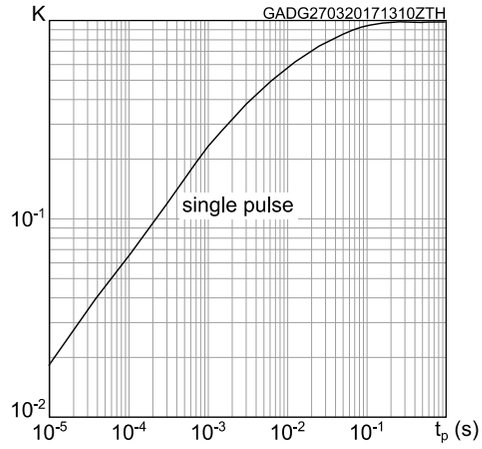


Figure 4: Output characteristics (T_J = 25 °C)

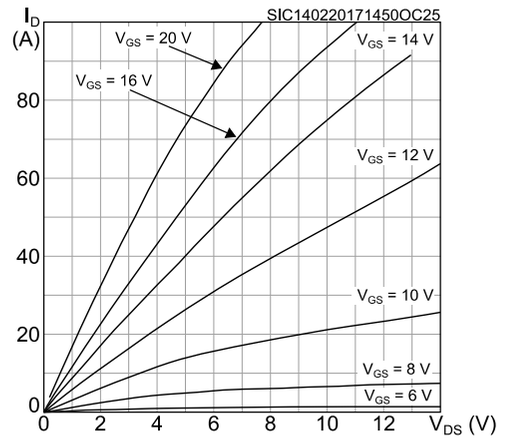


Figure 5: Output characteristics (T_J = 175 °C)

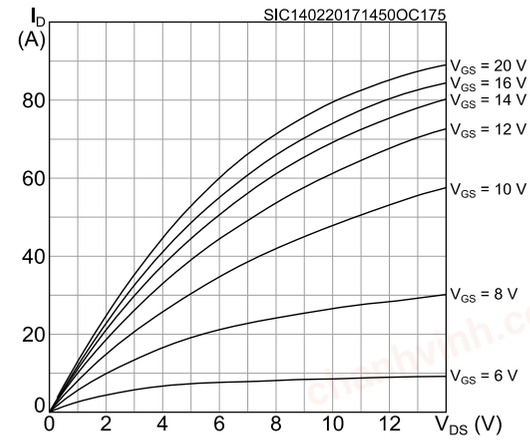


Figure 6: Transfer characteristics

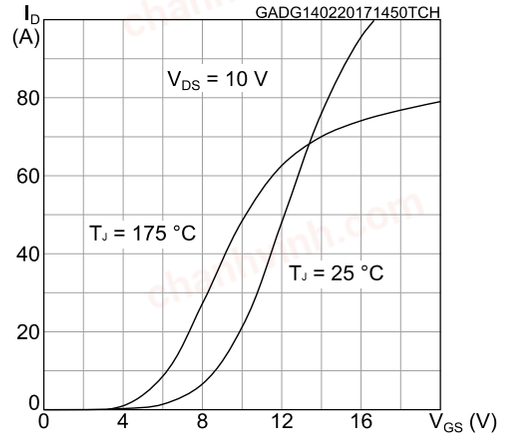
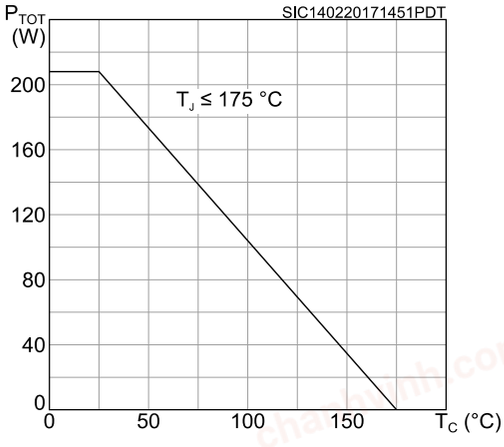


Figure 7: Power dissipation



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Figure 8: Gate charge vs. gate-source voltage

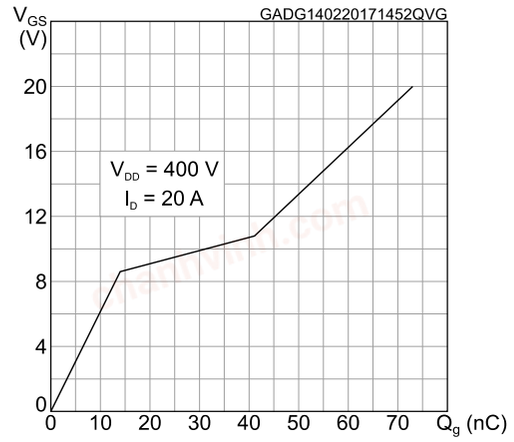


Figure 9: Capacitance variations

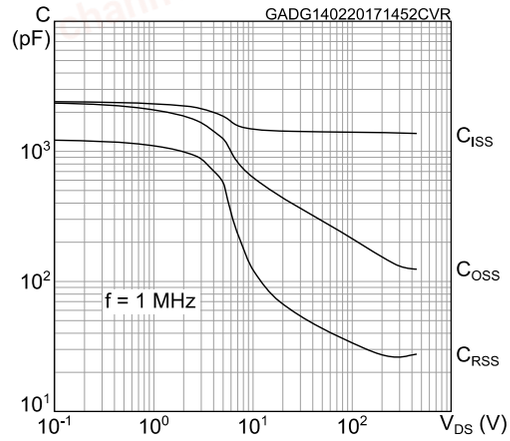


Figure 10: Switching energy vs. drain current

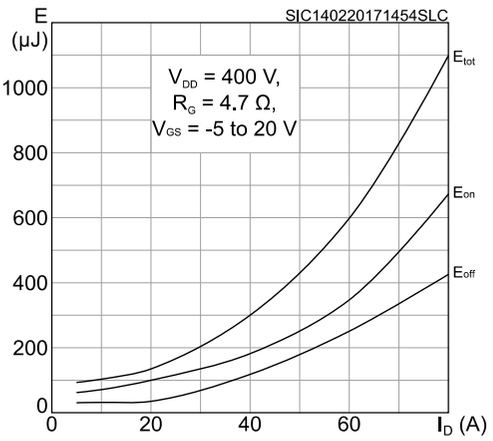


Figure 11: Switching energy vs. junction temperature

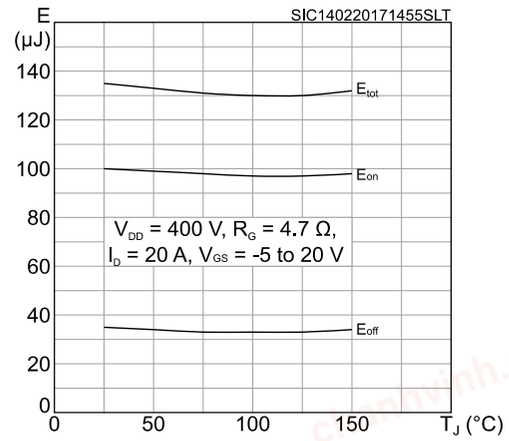


Figure 12: Normalized $V_{(BR)DSS}$ vs. temperature

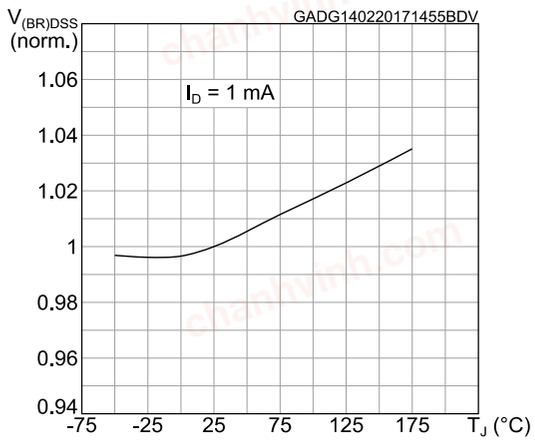
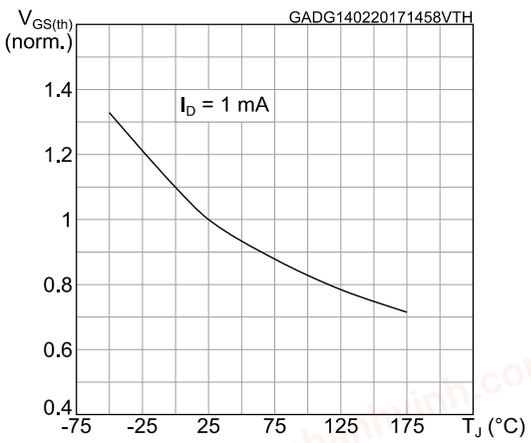


Figure 13: Normalized gate threshold voltage vs. temperature



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Figure 14: Normalized on-resistance vs. temperature

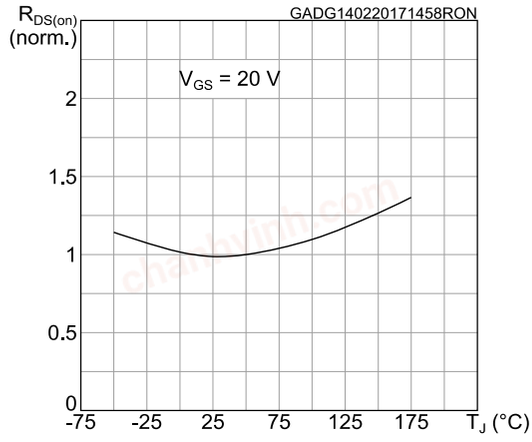


Figure 15: Reverse conduction characteristics (T_J = 25 °C)

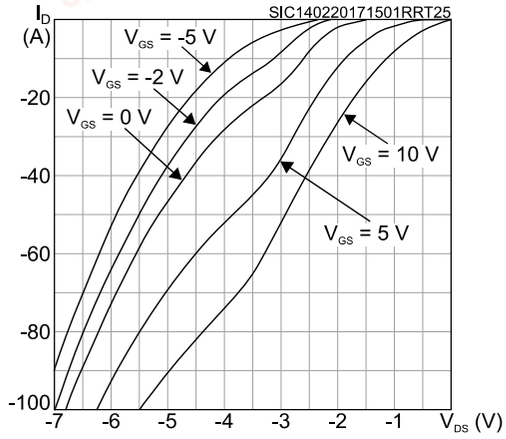
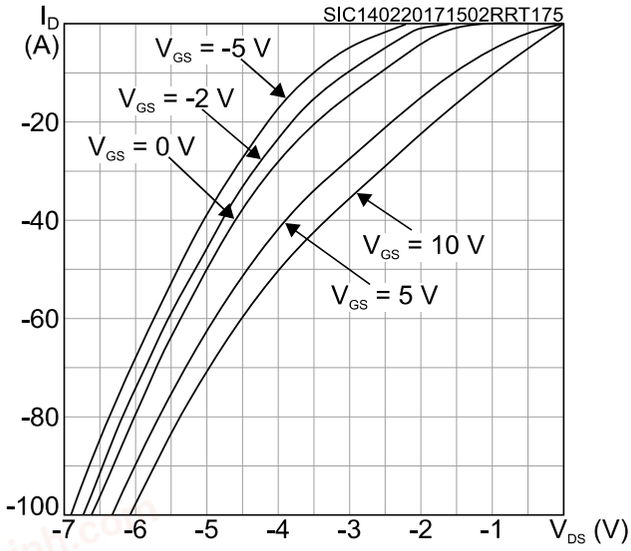


Figure 16: Reverse conduction characteristics (T_J = 175 °C)



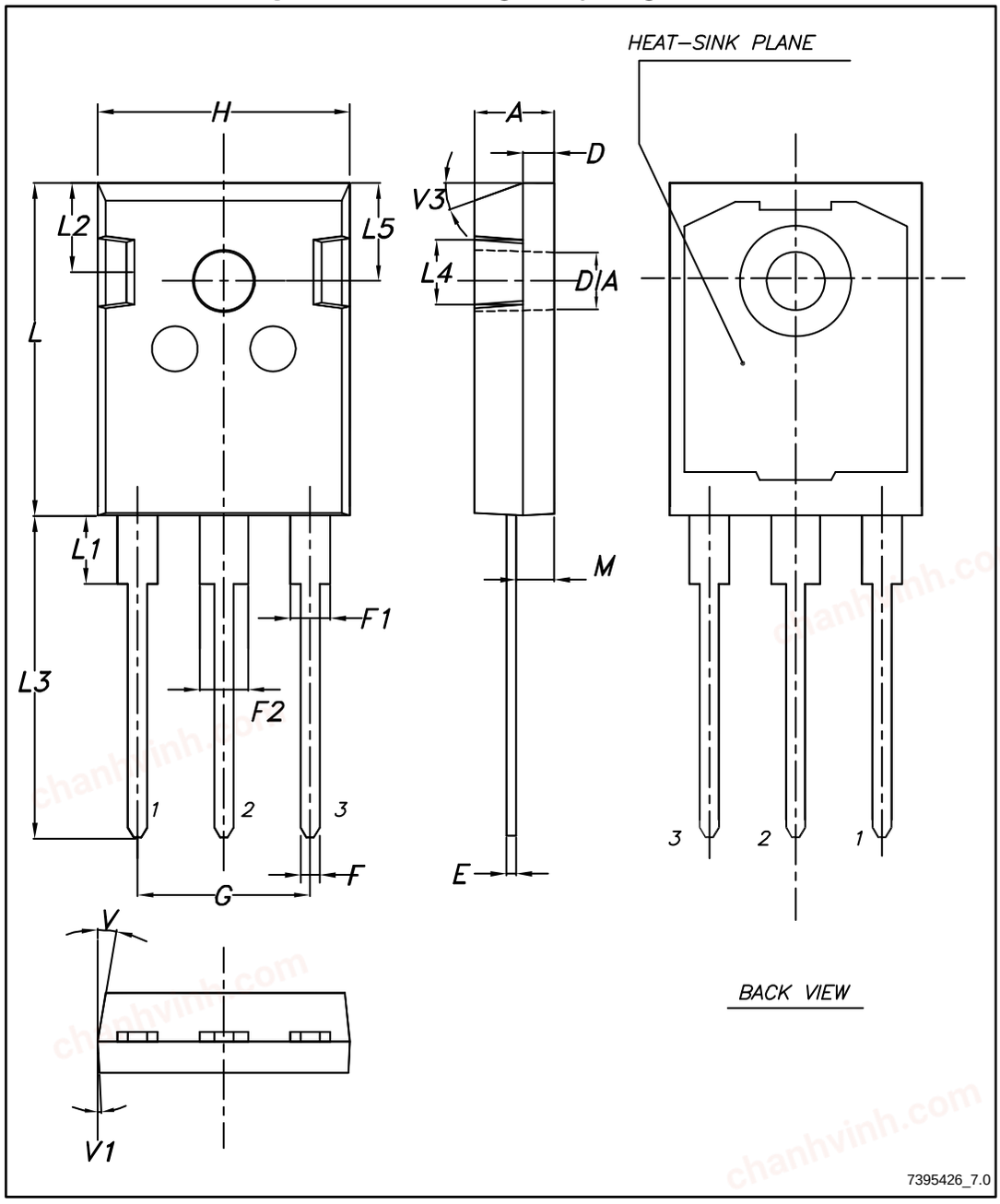
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3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

3.1 HiP247 long leads package information

Figure 17: HiP247™ long leads package outline



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Table 9: HiP247™ long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90		5.15
D	1.85		2.10
E	0.55		0.67
F	1.07		1.32
F1	1.90		2.38
F2	2.87		3.38
G	10.90 BSC		
H	15.77		16.02
L	20.82		21.07
L1	4.16		4.47
L2	5.49		5.74
L3	20.05		20.30
L4	3.68		3.93
L5	6.04		6.29
M	2.25		2.55
V		10°	
V1		3°	
V3		20°	
DIA	3.55		3.66

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4 Revision history

Table 10: Document revision history

Date	Revision	Changes
04-Apr-2017	1	First release

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