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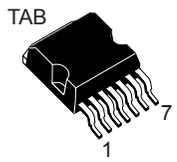
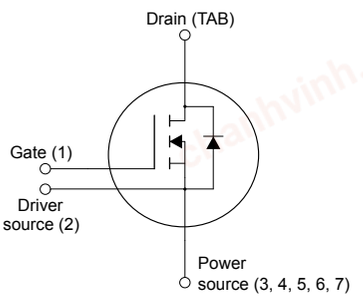
SCTH100N65G2-7AG

Datasheet

Automotive-grade silicon carbide Power MOSFET 650 V, 20 mΩ typ., 95 A in an H²PAK-7 package



H²PAK-7



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SCTH100N65G2-7AG	650 V	26 mΩ	95 A

- AEC-Q101 qualified
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitance
- Source sensing pin for increased efficiency

Applications

- Main inverter (electric traction)
- DC/DC converter for EV/HEV
- On board charger (OBC)

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

Product status link
SCTH100N65G2-7AG

Product summary	
Order code	SCTH100N65G2-7AG
Marking	100N65AG
Package	H²PAK-7
Packing	Tape and reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operational values)	-5 to 18	
I_D	Drain current (continuous) at T_C = 25 °C	95	A
	Drain current (continuous) at T_C = 100 °C	65	
I_{DM}(1)	Drain current (pulsed)	260	A
P_{TOT}	Total power dissipation at T_C = 25 °C	360	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.42	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

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2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	1.9	3.1	5.0	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 18 V, I_D = 50 A		20	26	mΩ
		V_{GS} = 18 V, I_D = 50 A, T_J = 175 °C		32		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 520 V, f = 1 MHz, V_{GS} = 0 V	-	3315	-	pF
C_{oss}	Output capacitance		-	267	-	pF
C_{rss}	Reverse transfer capacitance		-	46	-	pF
Q_g	Total gate charge	V_{DS} = 520 V, V_{GS} = -5 to 18 V, I_D = 50 A	-	162	-	nC
Q_{gs}	Gate-source charge		-	45	-	nC
Q_{gd}	Gate-drain charge		-	49	-	nC
R_G	Gate input resistance	f = 1 MHz, I_D = 0 A	-	1	-	Ω

Table 5. Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	V_{DD} = 520 V, I_D = 50 A,	-	486	-	µJ
E_{off}	Turn-off switching energy	R_G = 10 Ω, V_{GS} = -5 to 18 V	-	506	-	µJ

Table 6. Reverse SiC diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Diode forward voltage	I_F = 50 A, V_{GS} = 0 V	-	2.8	-	V
t_{rr}	Reverse recovery time	I_F = 50 A, di/dt = 2140 A/µs, V_{DD} = 520 V, R_G = 10 Ω, V_{GS} = -5 to 18 V	-	26		ns
Q_{rr}	Reverse recovery charge		-	370	-	nC
I_{RRM}	Reverse recovery current		-	24	-	A

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

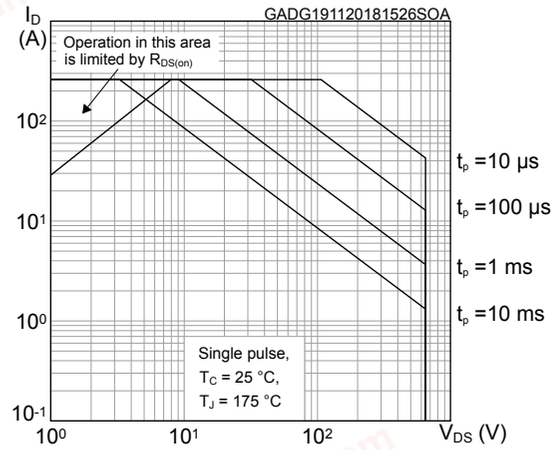

Figure 2. Thermal impedance

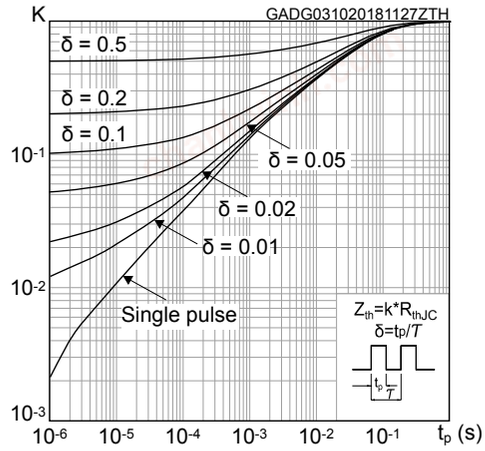

Figure 3. Output characteristics (T_J = 25 °C)

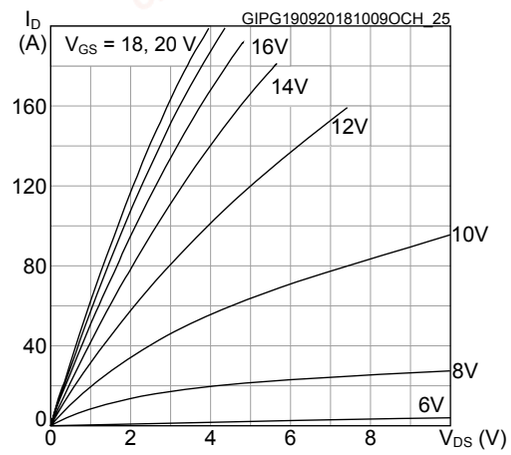

Figure 4. Output characteristics (T_J = 175 °C)

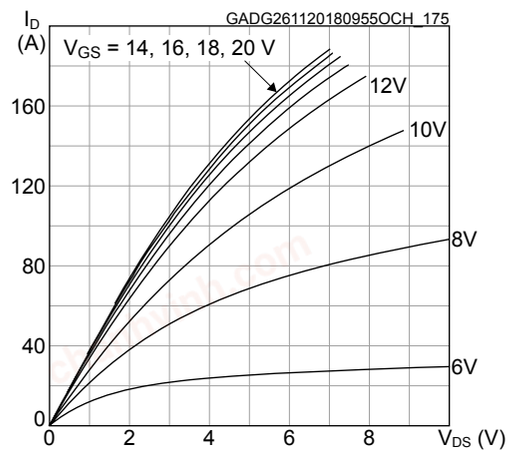

Figure 5. Transfer characteristics

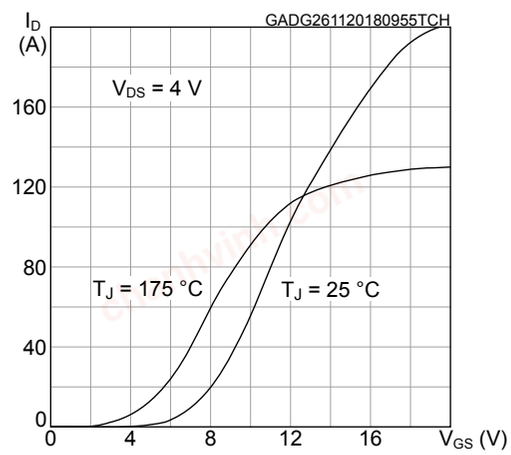

Figure 6. Total power dissipation

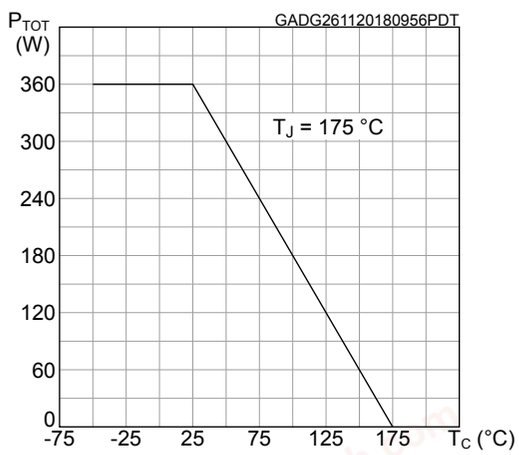

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Figure 7. Gate charge vs gate-source voltage

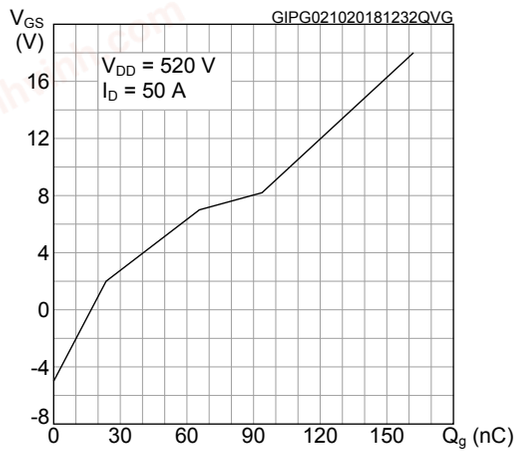

Figure 8. Capacitance variations

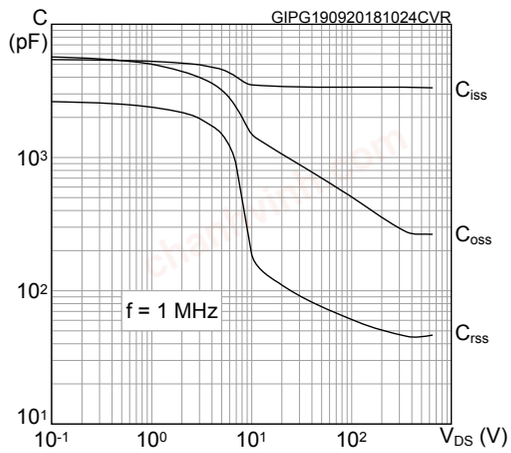

Figure 9. Switching energy vs drain current

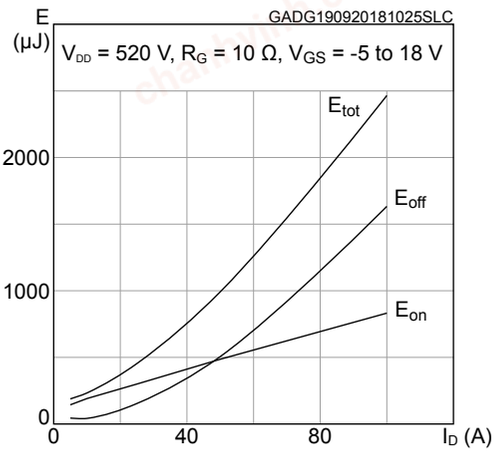

Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

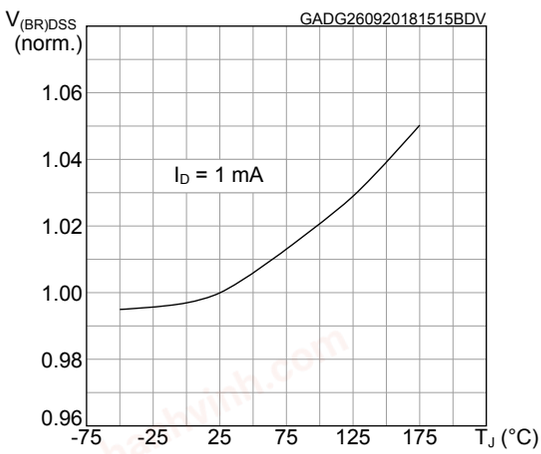

Figure 11. Normalized gate threshold voltage

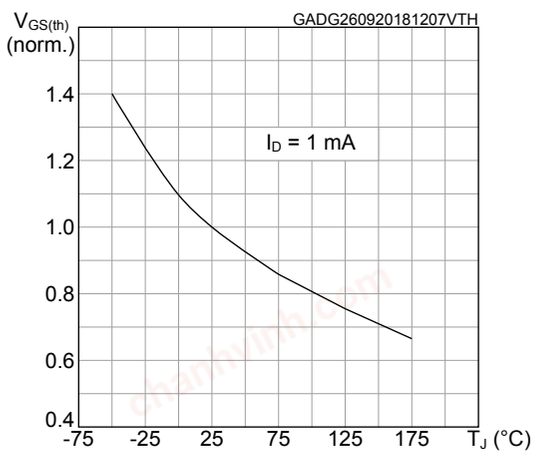

Figure 12. Switching energy vs junction temperature

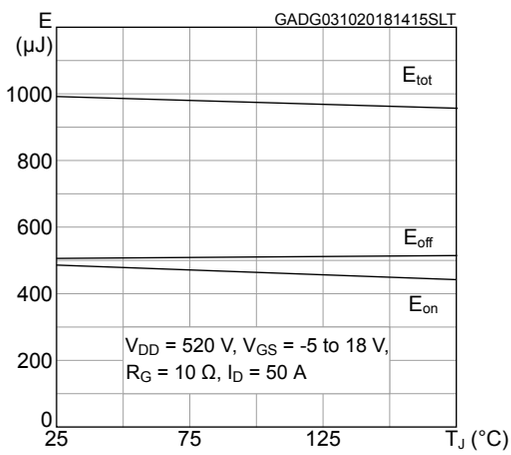

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Figure 13. Switching energy vs gate resistance

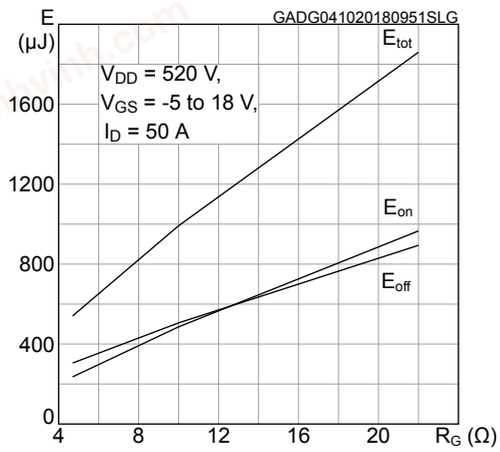


Figure 14. Normalized on-resistance vs temperature

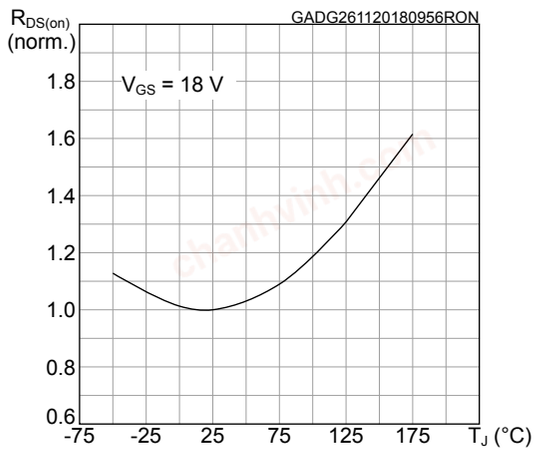


Figure 15. Body diode characteristics (T_J = 25 °C)

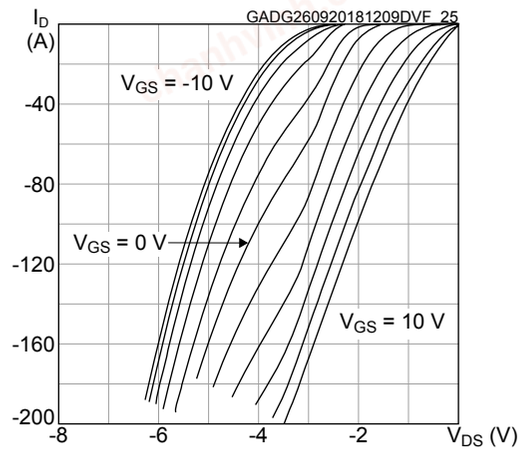
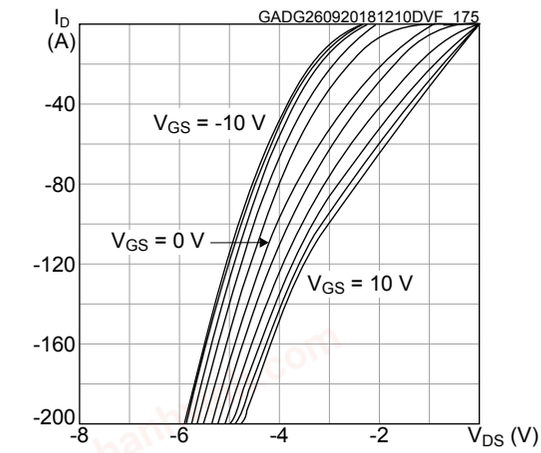


Figure 16. Body diode characteristics (T_J = 175 °C)



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3 Test circuits

Figure 17. Test circuit for resistive load switching times

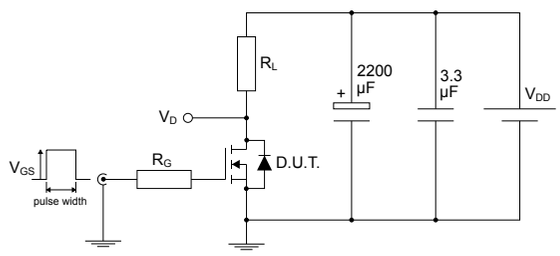

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Figure 18. Test circuit for gate charge behavior

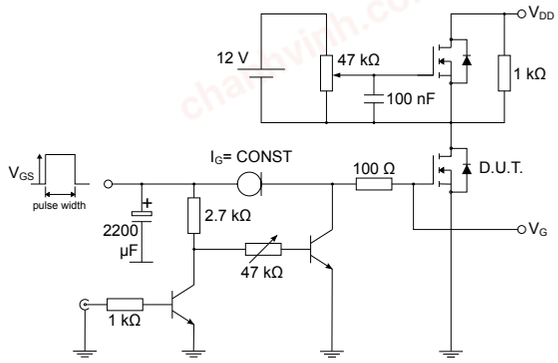

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Figure 19. Test circuit for inductive load switching and diode recovery times

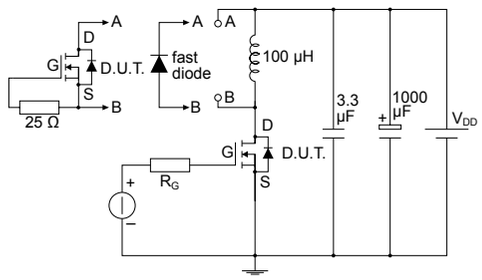

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Figure 20. Unclamped inductive load test circuit

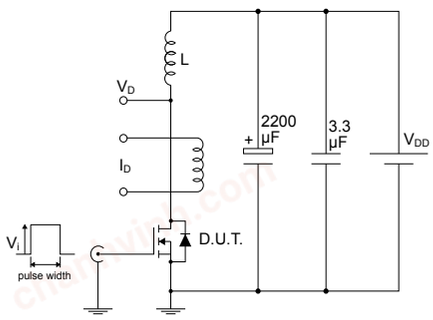

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Figure 21. Unclamped inductive waveform

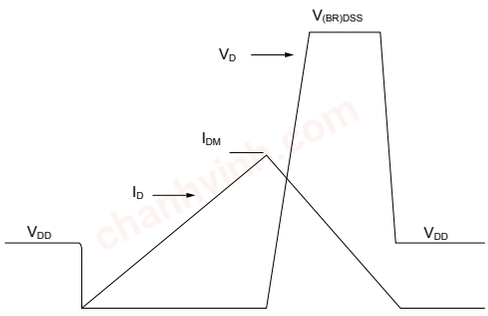

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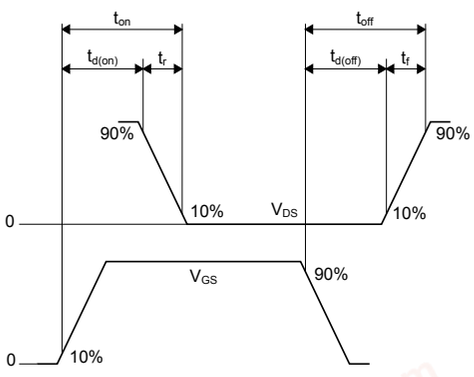
Figure 22. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-7 package information

Figure 23. **H²PAK-7 package outline**

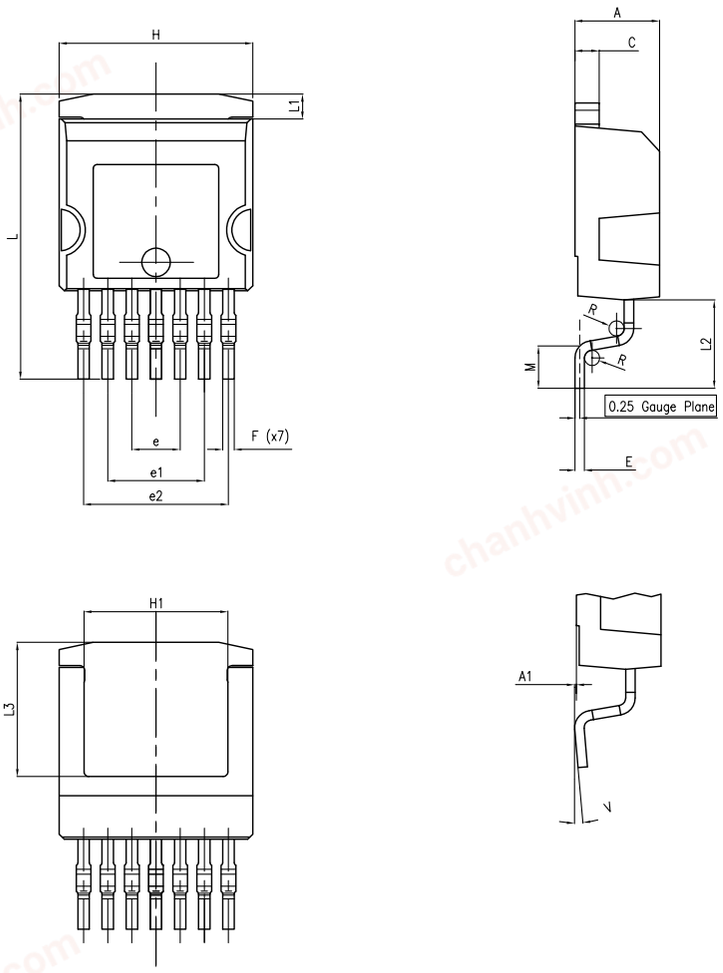

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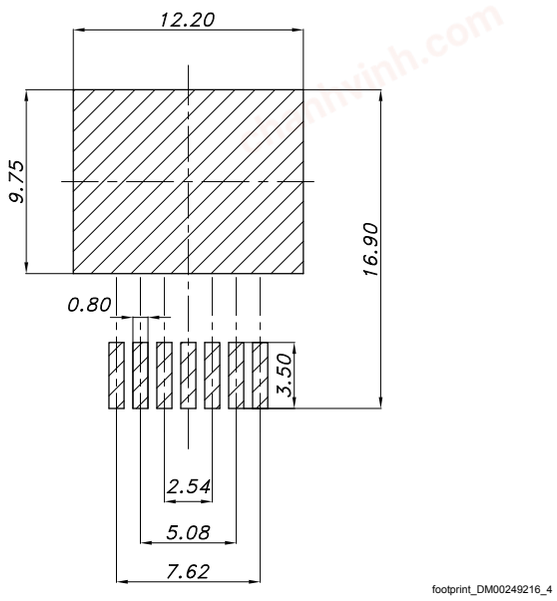
Table 7. **H²PAK-7 package mechanical data**

Dim.	mm	
	Min.	Max.
A	4.30	4.80
A1	0.03	0.20
C	1.17	1.37
e	2.34	2.74
e1	4.88	5.28
e2	7.42	7.82
E	0.45	0.60
F	0.50	0.70
H	10.00	10.40
H1	7.40	7.60
L	14.75	15.25
L1	1.27	1.40
L2	4.35	4.95
L3	6.85	7.25
M	1.90	2.50
R	0.20	0.60
V	0°	8°

Figure 24. **H²PAK-7 recommended footprint**



Note: Dimensions are in mm.

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4.2 Packing information

Figure 25. **Tape outline**

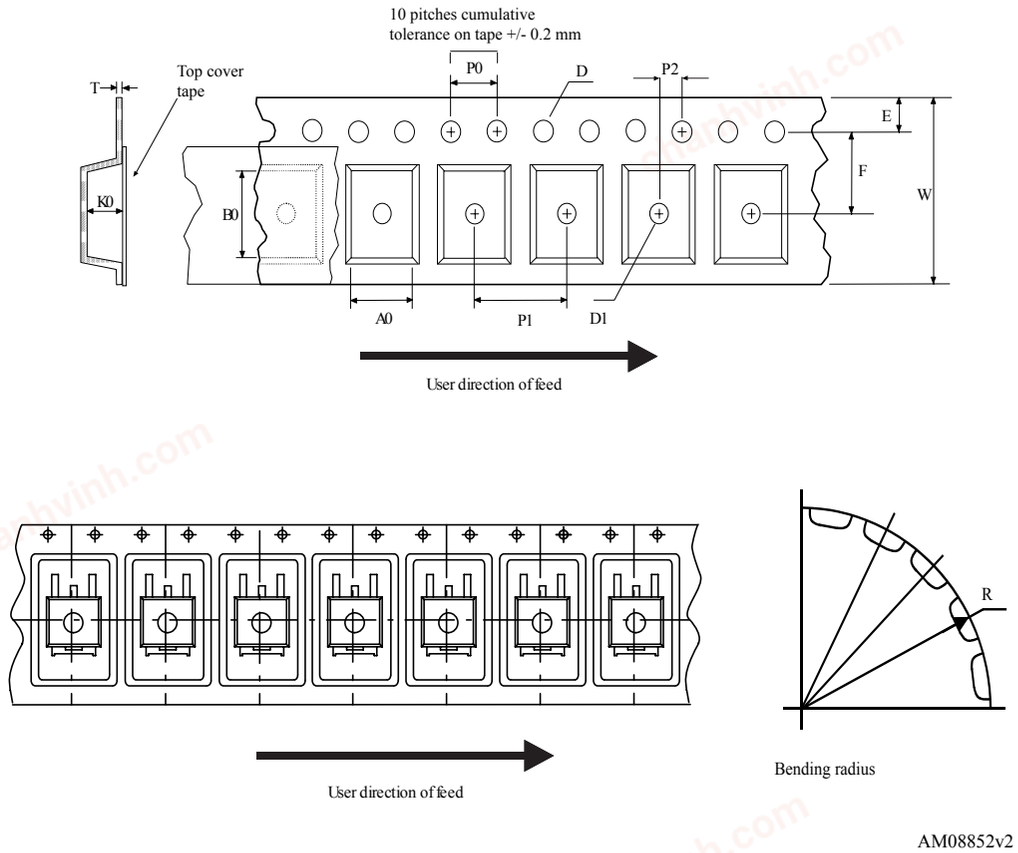

Figure 26. **Reel outline**

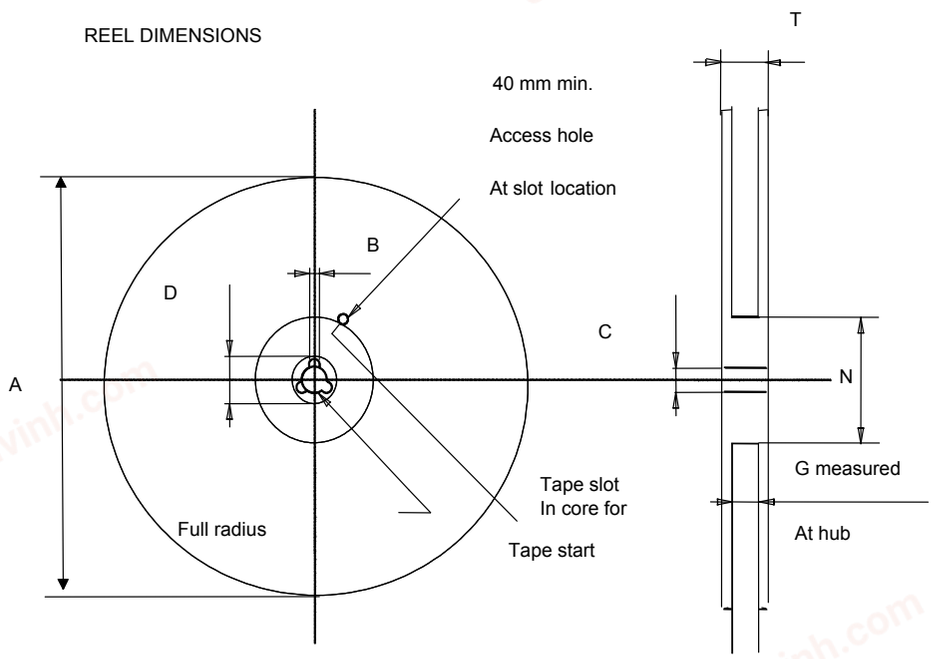

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Table 8. **Tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

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Revision history

Table 9. **Document revision history**

Date	Revision	Changes
27-Nov-2018	1	First release.
18-Aug-2021	2	Updated Features, Applications and Description. Updated Table 3. On/off states and Table 6. Reverse SiC diode characteristics. Minor text changes.

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