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MASTERGAN2

Data brief

High power density 600 V half-bridge driver with two enhancement mode GaN Power HEMT



Features

- 600 V system-in-package integrating half-bridge gate driver and high-voltage GaN power transistors in asymmetrical configuration:
  - QFN 9 x 9 x 1 mm package
  - $R_{DS(ON)}$ = 150 mΩ (LS) + 225 mΩ (HS)
  - $I_{DS(MAX)}$ = 10 A (LS) + 6.5 A (HS)
- Reverse current capability
- Zero reverse recovery loss
- UVLO protection on low-side and high-side
- Internal bootstrap diode
- Interlocking function
- Dedicated pin for shutdown functionality
- Accurate internal timing match
- 3.3 V to 15 V compatible inputs with hysteresis and pull-down
- Overtemperature protection
- Bill of material reduction
- Very compact and simplified layout
- Flexible, easy and fast design.

Application

- Switch-mode power supplies
- Chargers and adapters
- DC-DC converters

Product status link

MASTERGAN2

Product label

SUSTAINABLE TECHNOLOGY

Description

The MASTERGAN2 is an advanced power system-in-package integrating a gate driver and two enhancement mode GaN power transistors in asymmetrical half-bridge configuration.

The integrated GaN power transistors have 650 V drain-source breakdown voltage and RDS(ON) of 150 mΩ and 225 mΩ for low-side and high-side respectively, while the high-side of the embedded gate driver can be easily supplied by the integrated bootstrap diode

The MASTERGAN2 features UVLO protection on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions, and the interlocking function avoids cross-conduction conditions.

The input pins' extended range allows easy interfacing with microcontrollers, DSP units or Hall effect sensors.

The MASTERGAN2 operates in the industrial temperature range, -40°C to 125°C.

The device is available in a compact 9x9 mm QFN package.

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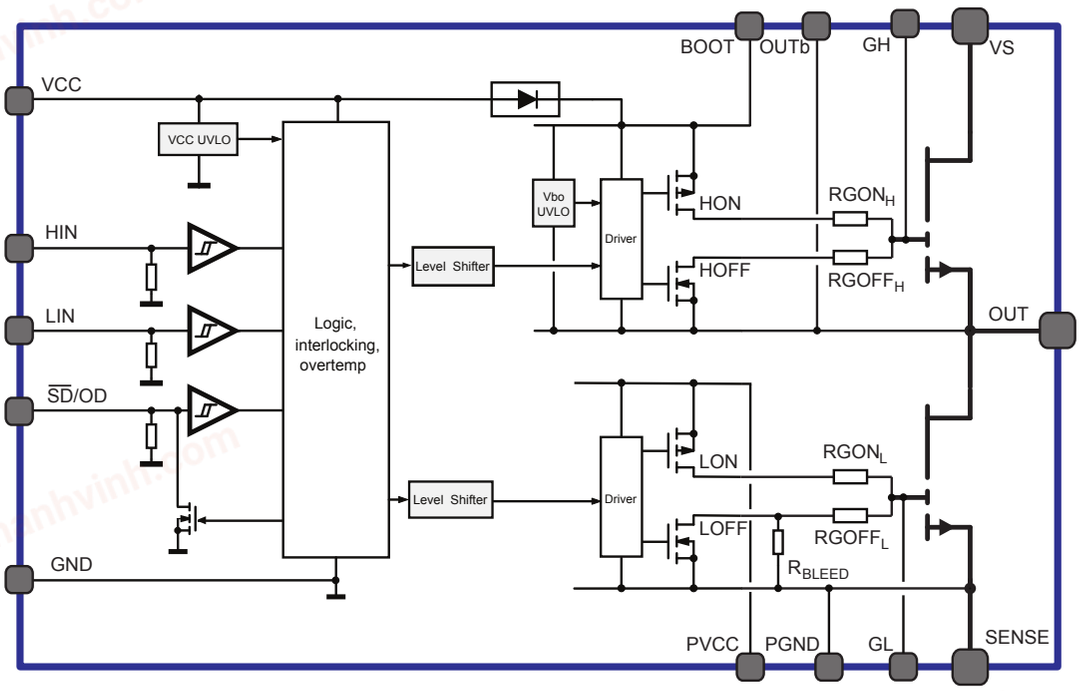
1 Block diagram

Figure 1. **Block diagram**



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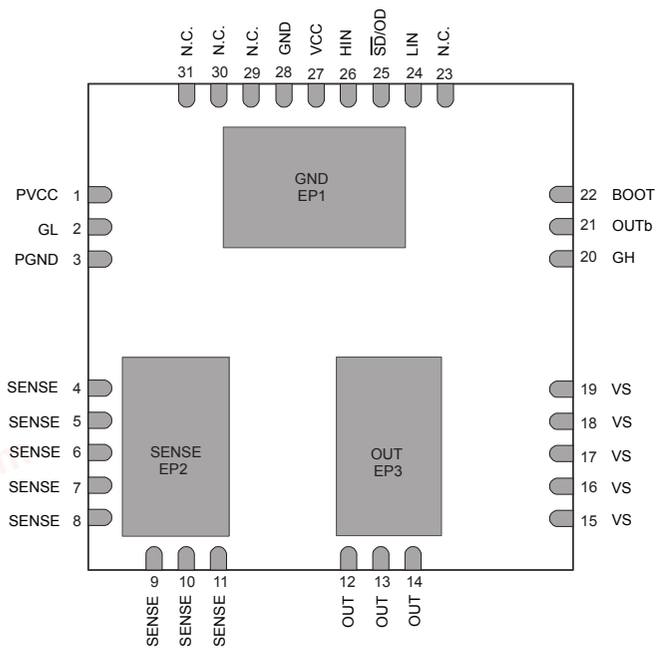
2 Pin description and connection diagram

Figure 2. Pin connection (top view)



2.1 Pin list

Table 1. Pin description

Pin Number	Pin Name	Type	Function
15, 16, 17, 18, 19	VS	Power supply	High voltage supply (high-side GaN Drain)
12, 13, 14, EP3	OUT	Power output	Half-bridge output
4, 5, 6, 7, 8, 9, 10, 11, EP2	SENSE	Power supply	Half-bridge sense (low-side GaN Source)
22	BOOT	Power supply	Gate driver high-side supply voltage
21	OUTb	Power supply	Gate driver high-side supply voltage, used only for Bootstrap capacitor connection. Internally connected to OUT.
27	VCC	Power supply	Logic supply voltage
1	PVCC	Power supply	Gate driver low-side supply voltage
28, EP1	GND	Power supply	Gate driver ground
3	PGND	Power supply	Gate driver low-side buffer ground. Internally connected to SENSE.
26	HIN	Logic input	High-side driver logic input
24	LIN	Logic input	Low-side driver logic input
25	$\overline{SD}$/OD	Logic input-output	Driver shutdown input and fault open-drain
2	GL	Output	Low-side GaN gate.
20	GH	Output	High-side GaN gate.
23, 29, 30, 31	N.C.	Not connected	Leave floating

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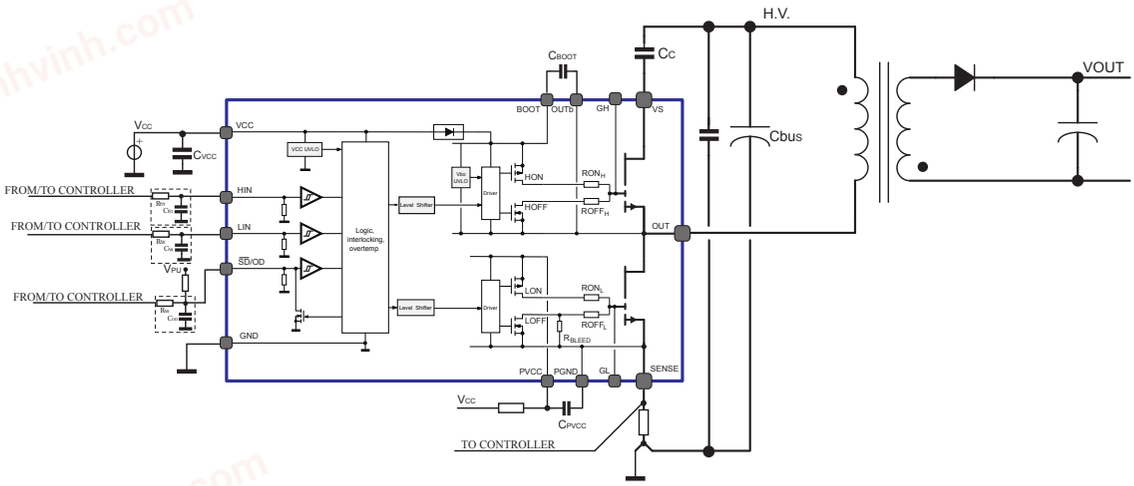
3 Typical application diagrams

Figure 3. **Typical application diagram – Asymmetrical Active clamp flyback**



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 QFN 9 x 9 x 1 mm, 31 leads, pitch 0.6 mm package information

Table 2. QFN 9 x 9 x 1 mm package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A3		0.10	
b	0.25	0.30	0.35
D	8.96	9.00	9.04
E	8.96	9.00	9.04
D1	3.30	3.40	3.50
E1	2.06	2.16	2.26
D2	1.76	1.86	1.96
E2	3.10	3.20	3.30
D3	1.70	1.80	1.90
E3	3.10	3.20	3.30
e		0.60	
K		0.24	
L	0.35	0.45	0.55
N	31		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. *Dimensioning and tolerances conform to ASME Y14.5-2009.*
2. *All dimensions are in millimeters.*
3. *N total number of terminals.*
4. *Dimensions do not include mold protrusion, not to exceed 0.15 mm.*
5. *Package outline exclusive of metal burr dimensions.*

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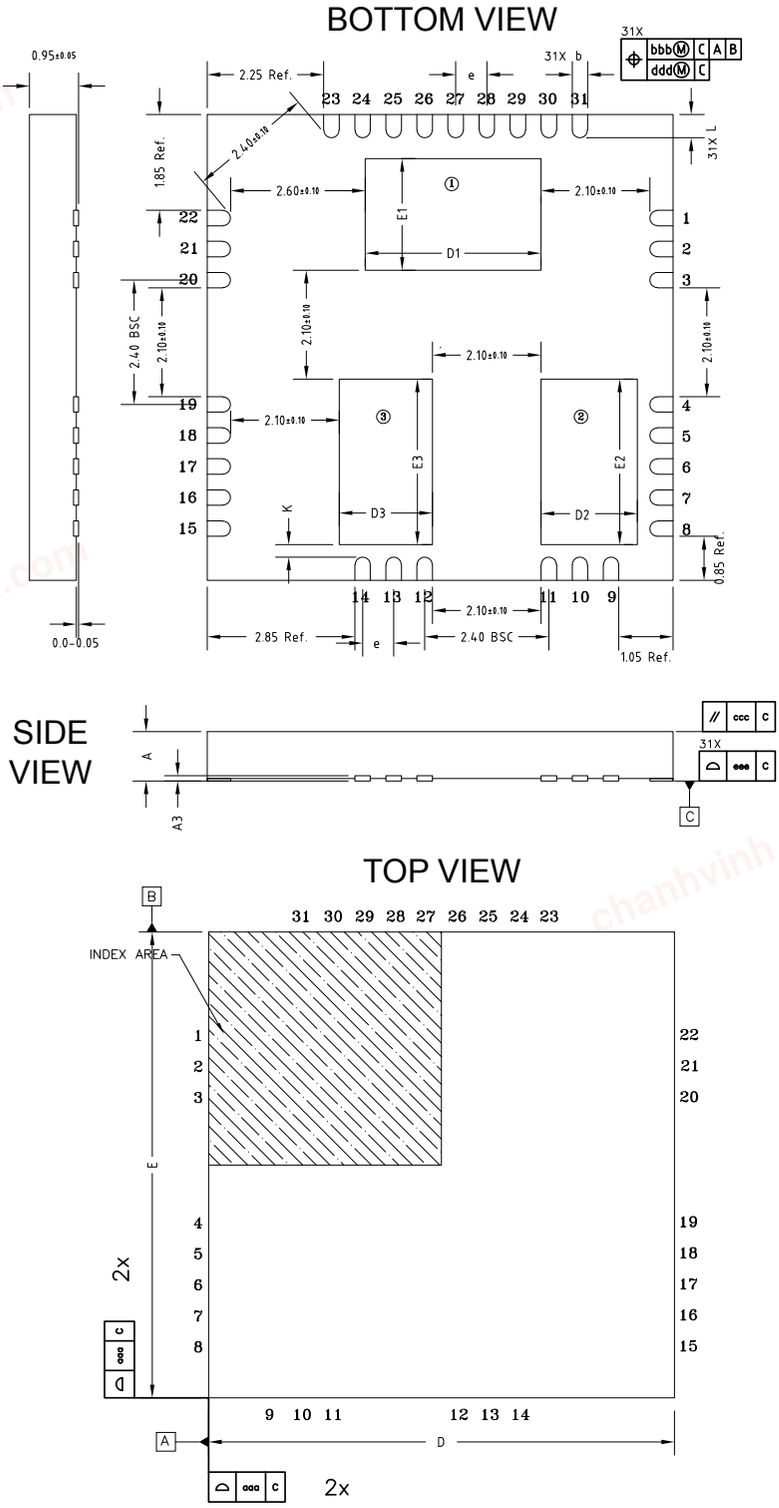
Figure 4. **QFN 9 x 9 x 1 mm package dimensions**



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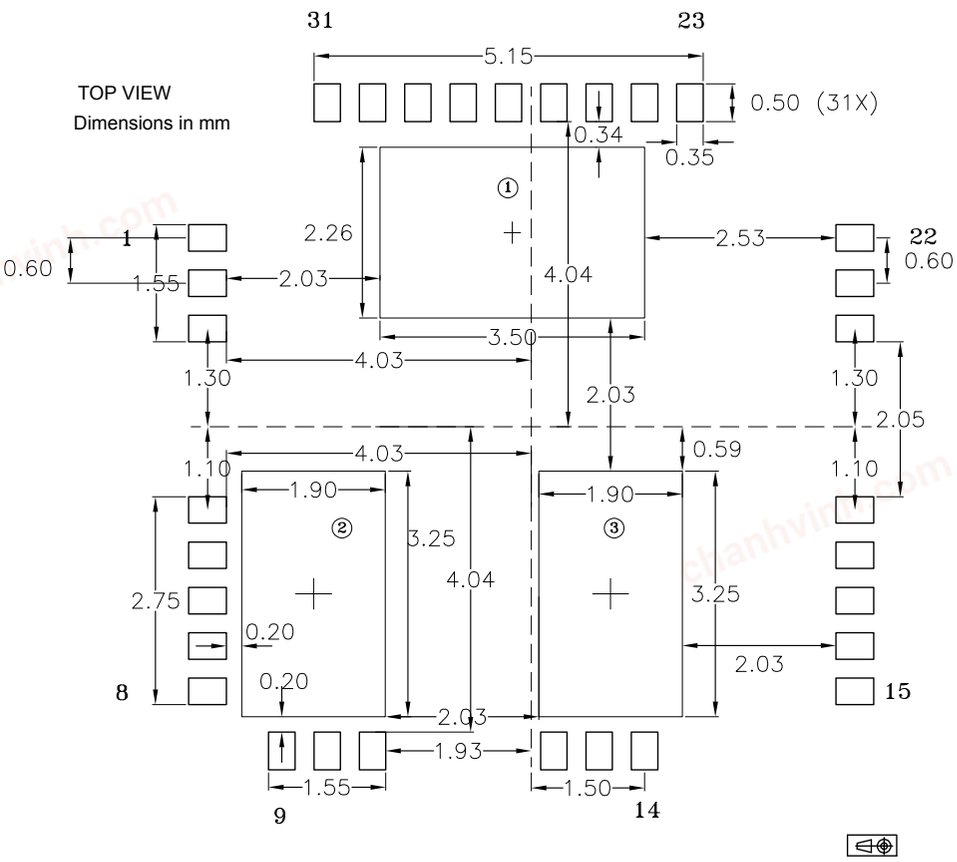
5 Suggested footprint

The MASTERGAN2 footprint for the PCB layout is usually defined based on several design factors such as assembly plant technology capabilities and board component density. For easy device usage and evaluation, ST provides the following footprint design, which is suitable for the largest variety of PCBs.

The following footprint indicates the copper area which should be free from the solder mask, while the copper area extends beyond the indicated areas especially for EP2 and EP3. To aid thermal dissipation, it is recommended to add thermal vias under these EPADs to transfer and dissipate device heat to the other PCB copper layers. A PCB layout example is available with the MASTERGAN2 evaluation board.

Figure 5. Suggested footprint (top view drawing)



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6 Ordering information

Table 3. **Order codes**

Order code	Package	Package marking	Packaging
MASTERGAN2	QFN 9 x 9 x 1 mm	MASTERGAN2	Tray
MASTERGAN2TR	QFN 9 x 9 x 1 mm	MASTERGAN2	Tape and Reel

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Revision history

Table 4. **Document revision history**

Date	Version	Changes
12-Nov-2020	1	Initial release.

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Contents

1 Block diagram 2
2 Pin description and connection diagram 3
2.1 Pin list 3
3 Typical application diagrams 4
4 Package information 5
4.1 QFN 9 x 9 x 1 mm, 31 leads, pitch 0.6 mm package information 5
5 Suggested footprint 7
6 Ordering information 8
Revision history 9
Contents 10
List of tables 11
List of figures 12

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List of tables

Table 1. Pin description . . . 3
Table 2. QFN 9 x 9 x 1 mm package dimensions . . . 5
Table 3. Order codes . . . 8
Table 4. Document revision history . . . 9

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List of figures

Figure 1. Block diagram 2
Figure 2. Pin connection (top view) 3
Figure 3. Typical application diagram – Asymmetrical Active clamp flyback 4
Figure 4. QFN 9 x 9 x 1 mm package dimensions 6
Figure 5. Suggested footprint (top view drawing) 7

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