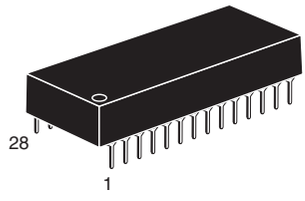
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M48T08
M48T08Y, M48T18

5 V, 64 Kbit (8 Kb x 8) TIMEKEEPER® SRAM

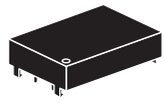
Features

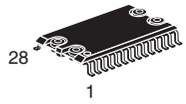
- Integrated ultra low power SRAM, real-time clock, power-fail control circuit, and battery
- BYTEWIDE™ RAM-like clock access
- BCD coded year, month, day, date, hours, minutes, and seconds
- Typical clock accuracy of ±1 minute a month, at 25 °C
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect
  (V_{PFD} = power-fail deselect voltage):
  - M48T08: V_{CC} = 4.75 to 5.5 V;
    4.5 V ≤ V_{PFD} ≤ 4.75 V
  - M48T18/T08Y: V_{CC} = 4.5 to 5.5 V;
    4.2 V ≤ V_{PFD} ≤ 4.5 V
- Software controlled clock calibration for high accuracy applications
- Self-contained battery and crystal in the CAPHAT™ DIP package
- Packaging includes a 28-lead SOIC and SNAPHAT® top (to be ordered separately)
- SOIC package provides direct connection for a snaphat top which contains the battery and crystal
- Pin and function compatible with DS1643 and JEDEC standard 8 K x 8 SRAMs
- RoHS compliant
  - Lead-free second level interconnect



PCDIP28
battery/crystal
CAPHAT™

SNAPHAT®
battery/crystal





SOH28

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1 Description

The M48T08/18/08Y TIMEKEEPER® RAM is an 8 K x 8 non-volatile static RAM and real-time clock which is pin and function compatible with the DS1643. The monolithic chip is available in two special packages to provide a highly integrated battery-backed memory and real-time clock solution.

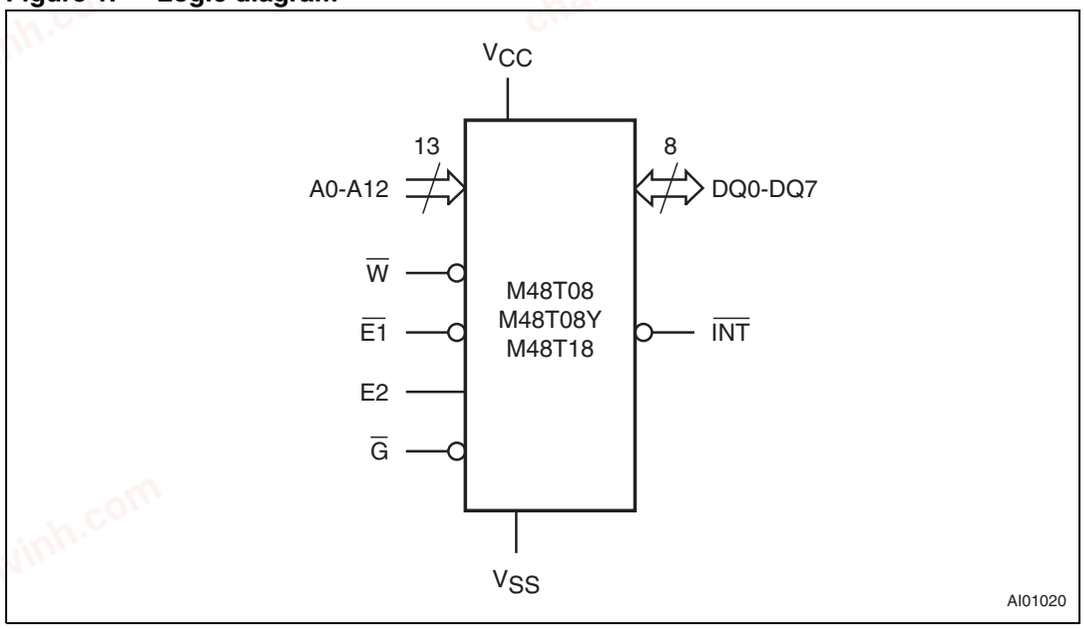
The M48T08/18/08Y is a non-volatile pin and function equivalent to any JEDEC standard 8 K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

The 28-pin, 600 mil DIP CAPHAT™ houses the M48T08/18/08Y silicon with a quartz crystal and a long-life lithium button cell in a single package.

The 28-pin, 330 mil SOIC provides sockets with gold-plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery and crystal. The unique design allows the SNAPHAT® battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT® housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT® housing is keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in tape & reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT®) part number is “M4T28-BR12SH” or “M4T32-BR12SH”.

Figure 1. Logic diagram



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Table 1. Signal names

A0-A12	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{INT}$	Power fail interrupt (open drain)
$\overline{E1}$	Chip enable 1
E2	Chip enable 2
$\overline{G}$	Output enable
$\overline{W}$	WRITE enable
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. DIP connections

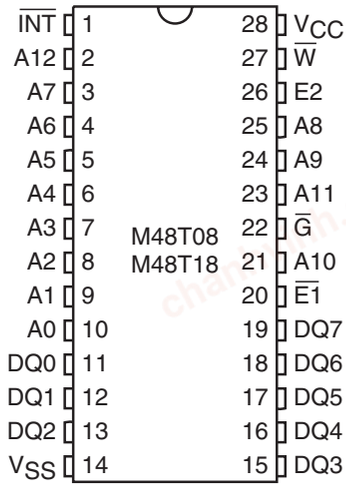
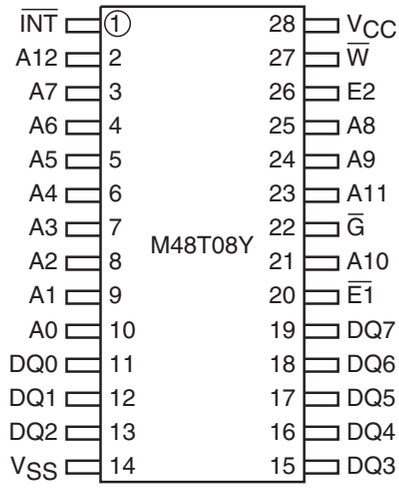
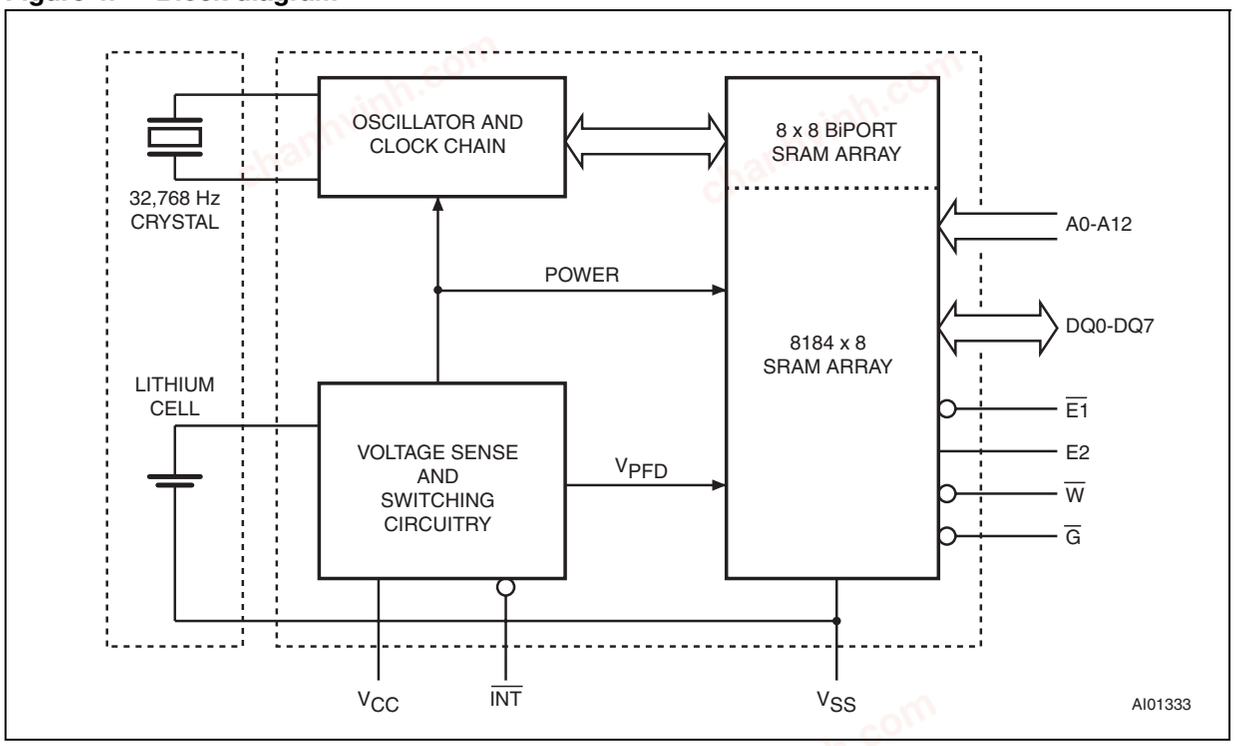


Figure 3. SOIC connections



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Figure 4. Block diagram



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2 Operation modes

As *Figure 4 on page 7* shows, the static memory array and the quartz-controlled clock oscillator of the M48T08/18/08Y are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh.

The clock locations contain the year, month, date, day, hour, minute, and second in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until 2100), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ READ/WRITE memory cells. The M48T08/18/08Y includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T08/18/08Y also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5 V supply for an out-of-tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below the battery backup switchover voltage (V_{SO}), the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Table 2. Operating modes

Mode	V_{CC}	$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75 to 5.5 V or 4.5 to 5.5 V	V_{IH}	X	X	X	High Z	Standby
Deselect		X	V_{IL}	X	X	High Z	Standby
WRITE		V_{IL}	V_{IH}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD}(min)(1)	X	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	X	High Z	Battery backup mode

1. See *Table 11 on page 22* for details.

Note: X = V_{IH} or V_{IL} ; V_{SO} = Battery backup switchover voltage.

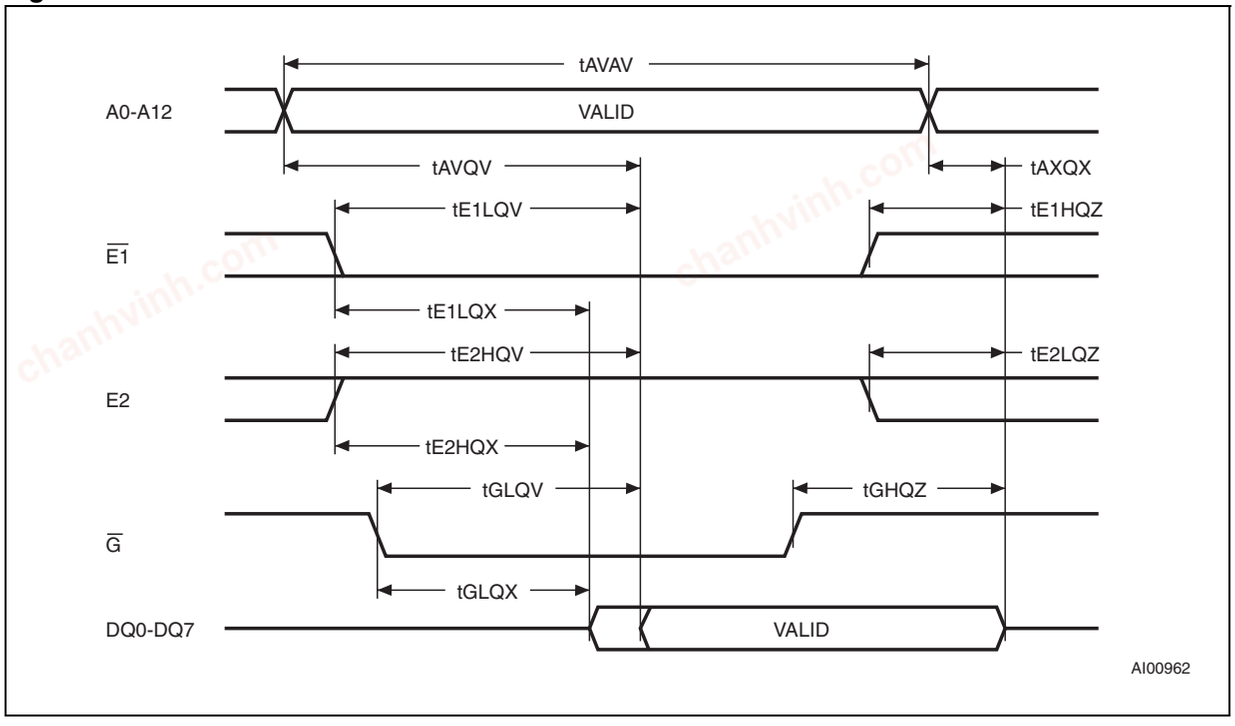
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2.1 READ mode

The M48T08/18/08Y is in the READ mode whenever $\overline{W}$ (WRITE enable) is high, $\overline{E1}$ (chip enable 1) is low, and E2 (chip enable 2) is high. The device architecture allows ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 address inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E1}$, E2, and $\overline{G}$ access times are also satisfied. If the $\overline{E1}$, E2 and $\overline{G}$ access times are not met, valid data will be available after the latter of the chip enable access times (t_{E1LQV} or t_{E2HQV}) or output enable access time (t_{GLQV}).

The state of the eight three-state data I/O signals is controlled by $\overline{E1}$, E2 and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E1}$, E2 and $\overline{G}$ remain active, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 5. READ mode AC waveforms



Note: WRITE enable ($\overline{W}$) = high.

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Table 3. READ mode AC characteristics

Symbol	Parameter[1]	M48T08/M48T18/T08Y				Unit
		–100/–10 (T08Y)		–150/–15 (T08Y)		
		Min	Max	Min	Max	
t_{AVAV}	READ cycle time	100		150		ns
t_{AVQV}	Address valid to output valid		100		150	ns
t_{E1LQV}	Chip enable 1 low to output valid		100		150	ns
t_{E2HQV}	Chip enable 2 high to output valid		100		150	ns
t_{GLQV}	Output enable low to output valid		50		75	ns
t_{E1LQX}	Chip enable 1 low to output transition	10		10		ns
t_{E2HQX}	Chip enable 2 high to output transition	10		10		ns
t_{GLQX}	Output enable low to output transition	5		5		ns
t_{E1HQZ}	Chip enable 1 high to output Hi-Z		50		75	ns
t_{E2LQZ}	Chip enable 2 low to output Hi-Z		50		75	ns
t_{GHQZ}	Output enable high to output Hi-Z		40		60	ns
t_{AXQX}	Address transition to output transition	5		5		ns

Note: Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

2.2 WRITE mode

The M48T08/18/08Y is in the WRITE mode whenever $\overline{W}$, $\overline{E1}$, and E2 are active. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E1}$, or the rising edge of E2. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E1}$, or the falling edge of E2. The addresses must be held valid throughout the cycle. $\overline{E1}$ or $\overline{W}$ must return high or E2 low for a minimum of t_{E1HAX} or t_{E2LAX} from chip enable or t_{WHAX} from WRITE enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; however, if the output bus has been activated by a low on $\overline{E1}$ and $\overline{G}$ and a high on E2, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

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Figure 6. WRITE enable controlled, WRITE AC waveform

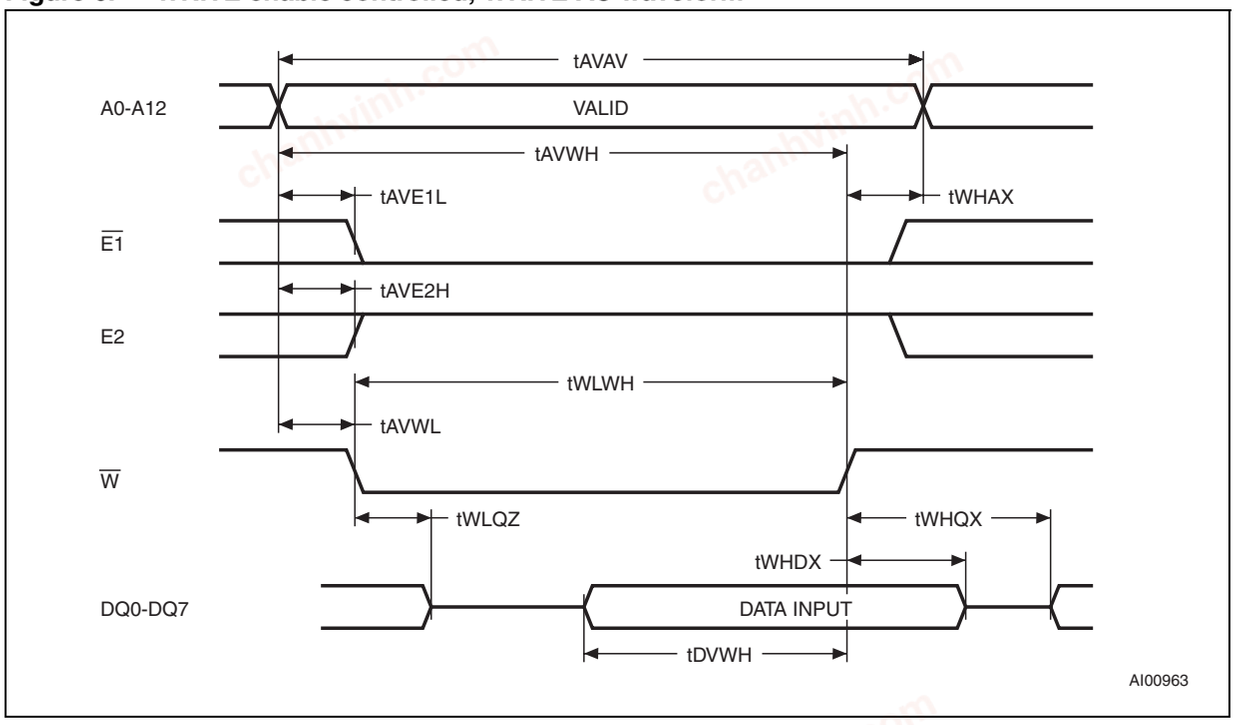
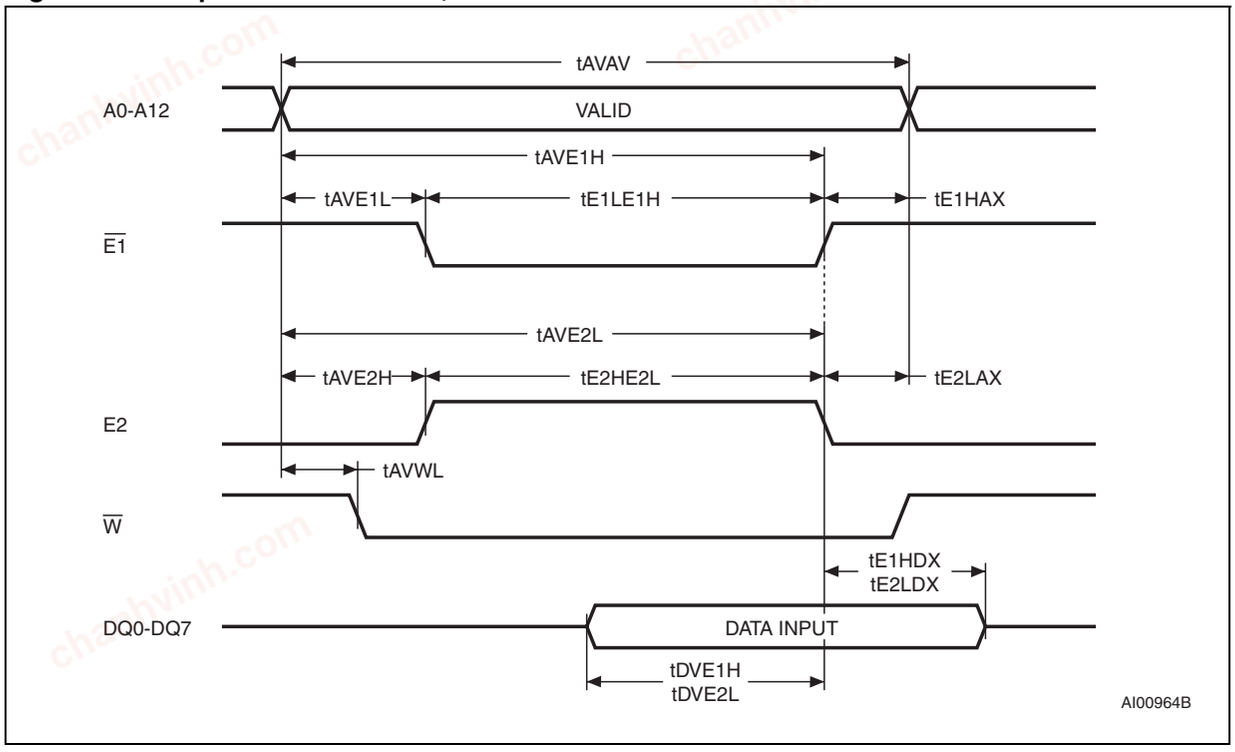


Figure 7. Chip enable controlled, WRITE AC waveforms



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Table 4. WRITE mode AC characteristics

Symbol	Parameter[1]	M48T08/M48T18/T08Y				Unit
		–100/–10 (T08Y)		–150/–15 (T08Y)		
		Min	Max	Min	Max	
t_{AVAV}	WRITE cycle time	100		150		ns
t_{AVWL}	Address valid to WRITE enable low	0		0		ns
t_{AVE1L}	Address valid to chip enable 1 low	0		0		ns
t_{AVE2H}	Address valid to chip enable 2 high	0		0		ns
t_{WLWH}	WRITE enable pulse width	80		100		ns
t_{E1LE1H}	Chip enable 1 low to chip enable 1 high	80		130		ns
t_{E2HE2L}	Chip enable 2 high to chip enable 2 low	80		130		ns
t_{WHAX}	WRITE enable high to address transition	10		10		ns
t_{E1HAX}	Chip enable 1 high to address transition	10		10		ns
t_{E2LAX}	Chip enable 2 low to address transition	10		10		ns
t_{DVWH}	Input valid to WRITE enable high	50		70		ns
t_{DVE1H}	Input valid to chip enable 1 high	50		70		ns
t_{DVE2L}	Input valid to chip enable 2 low	50		70		ns
t_{WHDX}	WRITE enable high to input transition	5		5		ns
t_{E1HDX}	Chip enable 1 high to input transition	5		5		ns
t_{E2LDX}	Chip enable 2 low to input transition	5		5		ns
t_{WLQZ}	WRITE enable low to output Hi-Z		50		70	ns
t_{AVWH}	Address valid to WRITE enable high	80		130		ns
t_{AVE1H}	Address valid to chip enable 1 high	80		130		ns
t_{AVE2L}	Address valid to chip enable 2 low	80		130		ns
t_{WHQX}	WRITE enable high to output transition	10		10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

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2.3 Data retention mode

With valid V_{CC} applied, the M48T08/18/08Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “Don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T08/18/08Y may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T08/18/08Y for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}.

Note: Requires use of M4T32-BR12SH SNAPHAT® top when using the SOH28 package.

As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected and the power supply is switched to external V_{CC}.

Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{rec} (min). $\overline{E1}$ should be kept high or E2 low as V_{CC} rises past V_{PFD} (min) to prevent inadvertent WRITE cycles prior to system stabilization. Normal RAM operation can resume t_{rec} after V_{CC} exceeds V_{PFD} (max).

For more information on battery storage life refer to the application note AN1012.

2.4 Power-fail interrupt pin

The M48T08/18/08Y continuously monitors V_{CC}. When V_{CC} falls to the power-fail detect trip point, an interrupt is immediately generated. An internal clock provides a delay of between 10 µs and 40 µs before automatically deselecting the M48T08/18/08Y. The $\overline{INT}$ pin is an open drain output and requires an external pull-up resistor, even if the interrupt output function is not being used.

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3 Clock operations

3.1 Reading the clock

Updates to the TIMEKEEPER® registers should be halted before clock data is read to prevent reading data in transition. The BiPORT™ TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0.'

3.2 Setting the clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1,' like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24-hour BCD format (on *Table 5*). Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in *Table 5* must be written to '0' to allow for normal TIMEKEEPER and RAM operation.

See the application note AN923, “TIMEKEEPER® rolling Into the 21st century” for information on century rollover.

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Table 5. Register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 years				Year				Year	00-99
1FFEh	0	0	0	10 M	Month				Month	01-12
1FFDh	0	0	10 date		Date				Date	01-31
1FFCh	0	FT	0	0	0	Day			Day	01-07
1FFBh	0	0	10 hours		Hours				Hours	00-23
1FFAh	0	10 minutes			Minutes				Minutes	00-59
1FF9h	ST	10 seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	

Keys:

S = SIGN bit

FT = FREQUENCY TEST bit (set to '0' for normal clock operation)

R = READ bit

W = WRITE bit

ST = STOP bit

0 = Must be set to '0'

3.3 Stopping and starting the oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit (ST) is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T08/18/08Y (in the PCDIP28 package) is shipped from STMicroelectronics with the STOP bit set to a '1.' When reset to a '0,' the M48T08/18/08Y oscillator starts within one second.

Note: To guarantee oscillator startup after initial power-up, first write the STOP bit (ST) to '1,' then reset to '0.'

3.4 Calibrating the clock

The M48T08/18/08Y is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. A typical M48T08/18/08Y is accurate within 1 minute per month at 25 °C without calibration. The devices are tested not to exceed ± 35 ppm (parts per million) oscillator frequency error at 25 °C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T08/18/08Y improves to better than +1/–2 ppm at 25 °C.

The oscillation rate of any crystal changes with temperature. *Figure 8 on page 17* shows the frequency error that can be expected at various temperatures. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome “trim” capacitors. The

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M48T08/18/08Y design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 9 on page 17*. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five-bit calibration byte found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration byte occupies the five lower order bits in the control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is the sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles; that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T08/18/08Y may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of standard test equipment. When the frequency test (FT) bit, the seventh-most significant bit in the day register, is set to a '1,' and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the seconds register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (WR001010) to be loaded into the calibration byte for correction.

Note: Setting or changing the calibration byte does not affect the frequency test output frequency. The device must be selected and addresses must be stable at address 1FF9h when reading the 512 Hz on DQ0.

The LSB of the seconds register is monitored by holding the M48T08/18/08Y in an extended READ of the seconds register, but without having the READ bit set. The FT bit MUST be reset to '0' for normal clock operations to resume.

For more information on calibration, see the application note AN934, “TIMEKEEPER® calibration.”

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Figure 8. Crystal accuracy across temperature

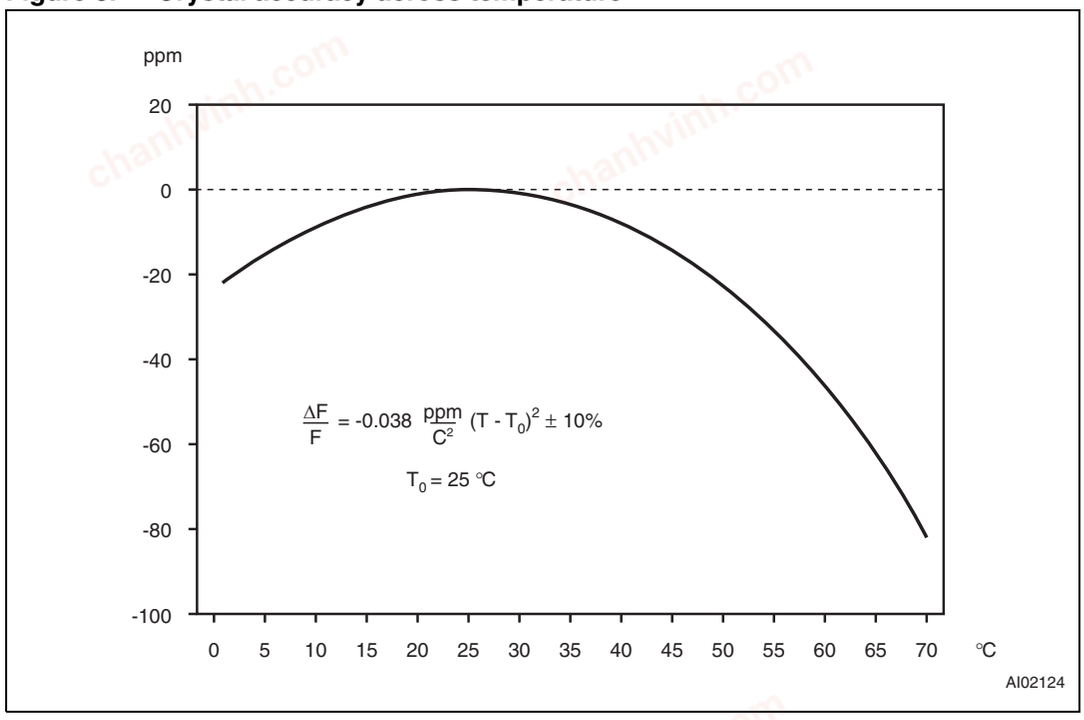
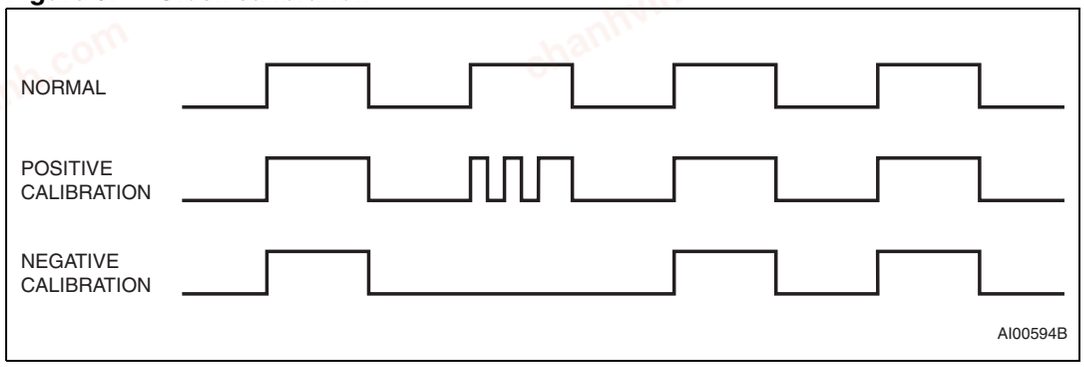


Figure 9. Clock calibration



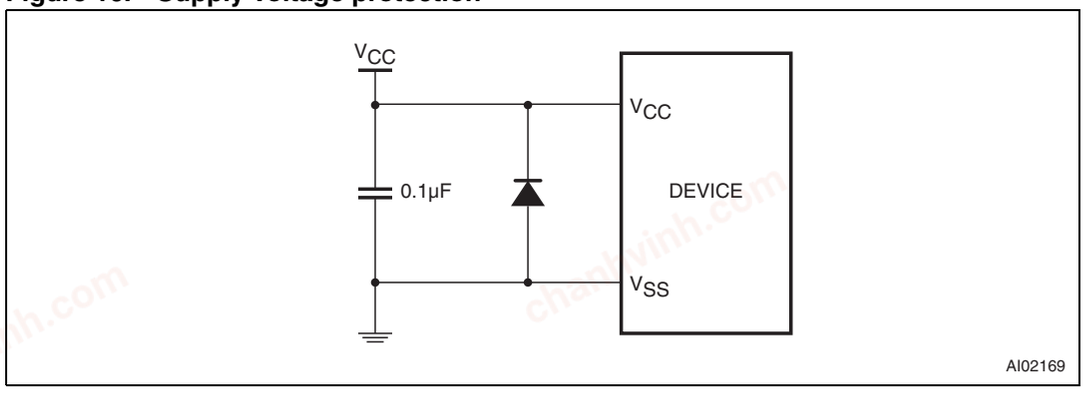
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3.5 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 µF (as shown in *Figure 10*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 10. Supply voltage protection



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4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature	0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–40 to 85	°C
T_{SLD} (1)(2)(3)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to 7	V
V_{CC}	Supply voltage	–0.3 to 7	V
I_O	Output current	20	mA
P_D	Power dissipation	1	W

1. For DIP package, soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. Furthermore, the devices shall not be exposed to IR reflow nor preheat cycles (as performed as part of wave soldering). ST recommends the devices be hand-soldered or placed in sockets to avoid heat damage to the batteries.
2. For DIP packaged devices, ultrasound vibrations should not be used for post-solder cleaning to avoid damaging the crystal.
3. For SO package, lead-free (Pb-free) lead finish: reflow at peak temperature of 260 °C (the time above 255 °C must not exceed 30 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

Caution: *Do NOT wave solder SOIC to avoid damaging SNAPHAT® sockets.*

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5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. Operating and AC measurement conditions

Parameter	M48T08	M48T18/T08Y	Unit
Supply voltage (V_{CC})	4.75 to 5.5	4.5 to 5.5	V
Ambient operating temperature (T_A)	0 to 70	0 to 70	°C
Load capacitance (C_L)	100	100	pF
Input rise and fall times	≤ 5	≤ 5	ns
Input pulse voltages	0 to 3	0 to 3	V
Input and output timing ref. voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 11. AC testing load circuit

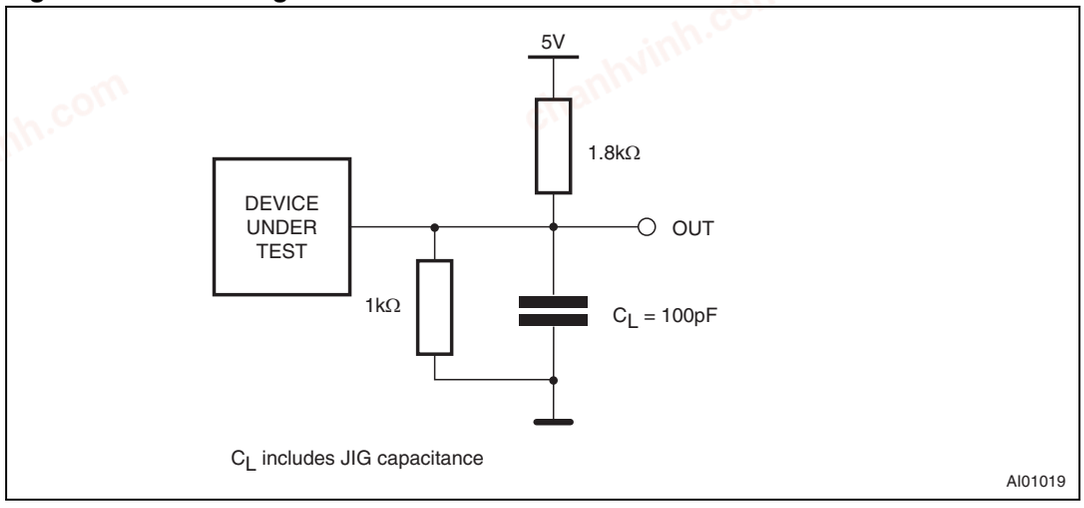


Table 8. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance	-	10	pF
C_{IO}[3]	Input / output capacitance	-	10	pF

1. Effective capacitance measured with power supply at 5 V; sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

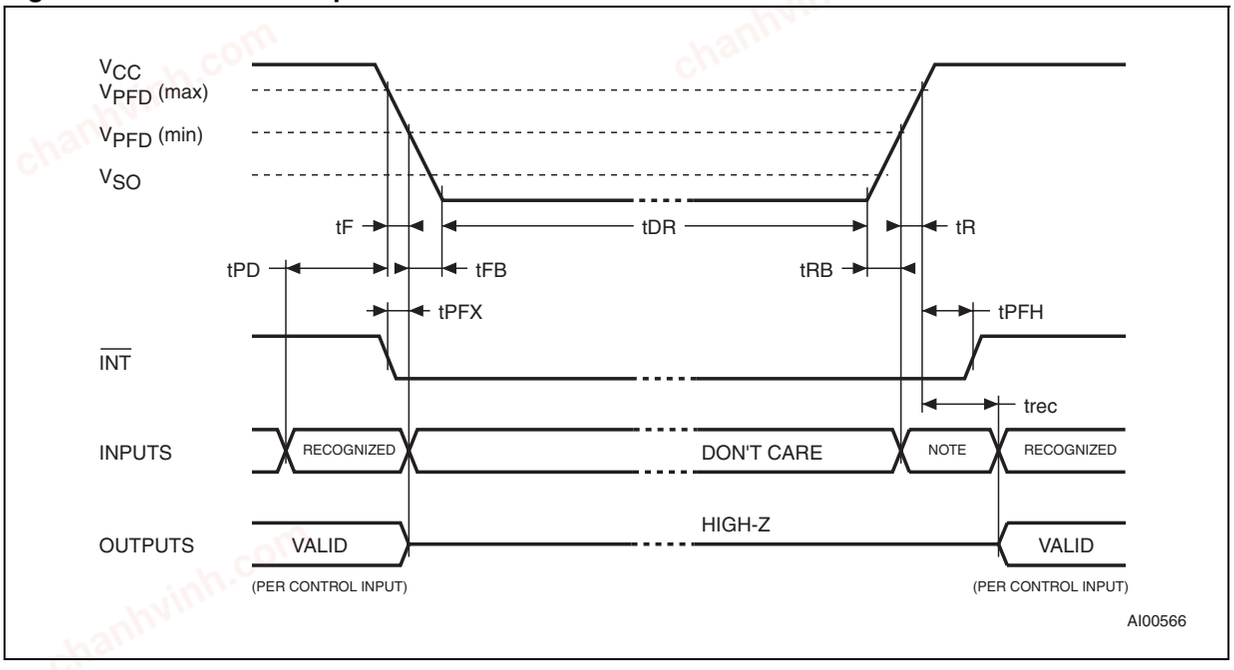
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Table 9. DC characteristics

Symbol	Parameter	Test condition(1)	M48T08/M48T18/T08Y		Unit
			Min	Max	
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}(2)	Output leakage current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply current	Outputs open		80	mA
I_{CC1}(3)	Supply current (standby) TTL	$\overline{E1} = V_{IH}$, $E2 = V_{IL}$		3	mA
I_{CC2}(3)	Supply current (standby) CMOS	$\overline{E1} = V_{CC} - 0.2V$, $E2 = V_{SS} + 0.2V$		3	mA
V_{IL}	Input low voltage		–0.3	0.8	V
V_{IH}	Input high voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		0.4	V
	Output low voltage ($\overline{INT}$)(4)	I_{OL} = 0.5 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –1 mA	2.4		V

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. Outputs deselected.
3. Measured with control bits set as follows: R = '1'; W, ST, FT = '0.'
4. The $\overline{INT}$ pin is open drain.

Figure 12. Power down/up mode AC waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E1}$ high or E2 low as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertent WRITE cycles after V_{CC} rises above V_{PFD} (min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system clock is running.

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Table 10. Power down/up AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before power-down	0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	0		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	1		µs
t_{rec}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before power-up	1		ms
t_{PFX}	$\overline{INT}$ low to auto deselect	10	40	µs
t_{PFH}	V_{PFD} (max) to $\overline{INT}$ high		120	µs

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 11. Power down/up trip points DC characteristics

Symbol	Parameter[1][2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	M48T08	4.5	4.6	4.75	V
		M48T18/T08Y	4.2	4.3	4.5	V
V_{SO}	Battery backup switchover voltage			3.0		V
t_{DR}	Expected data retention time		10[3]			Years

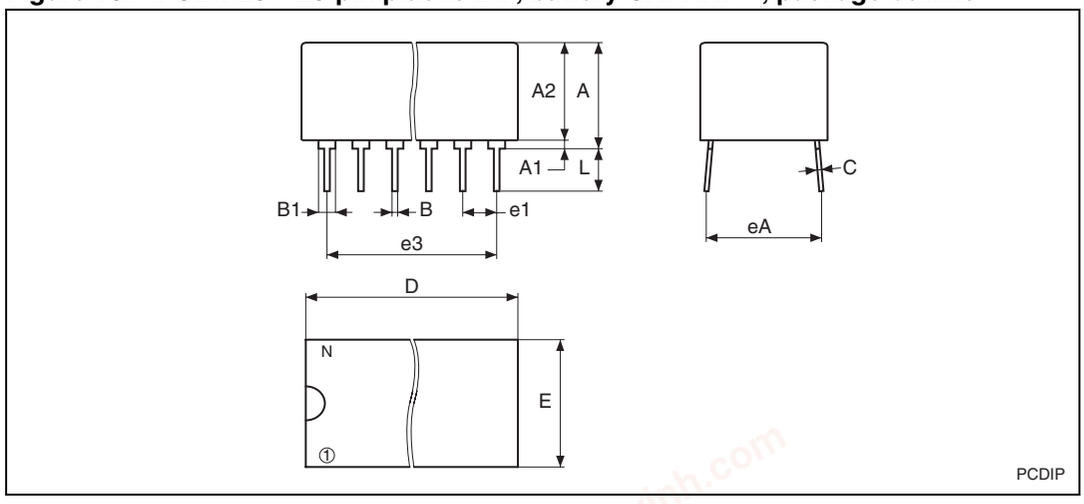
1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
3. At 55 °C, V_{CC} = 0 V; t_{DR} = 8.5 years (typ) at 70 °C. Requires use of M4T32-BR12SH SNAPHAT® top when using the SOH28 package.

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6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 13. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package outline



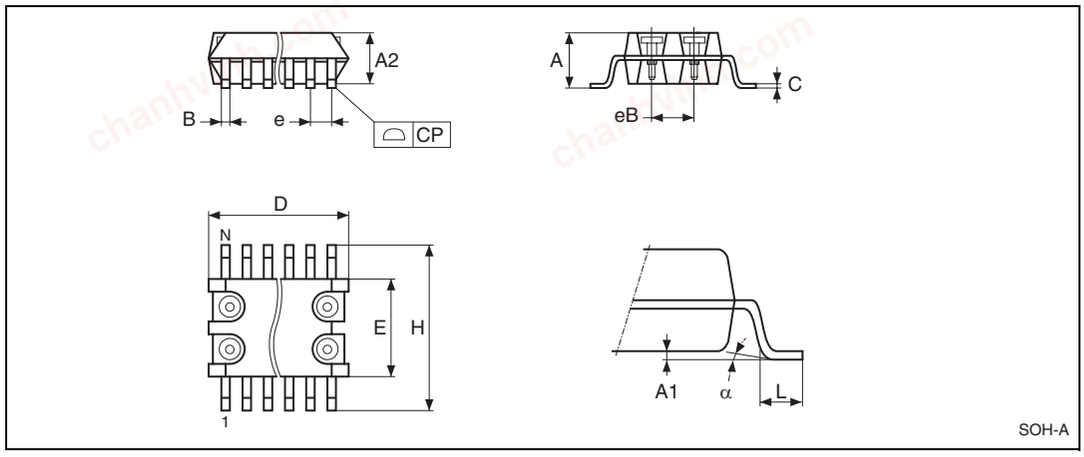
Note: Drawing is not to scale.

Table 12. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3	33.02			1.3		
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

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Figure 14. SOH28 – 28-lead plastic small outline, 4-socket battery SNAPHAT®, package outline



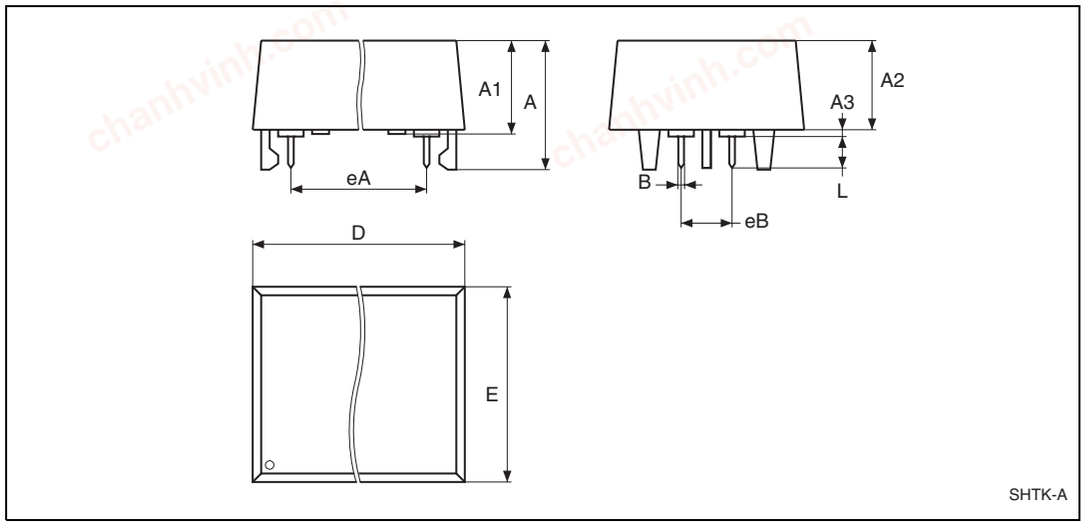
Note: Drawing is not to scale.

Table 13. SOH28 – 28-lead plastic SO, 4-socket battery SNAPHAT®, package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

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Figure 15. SH – 4-pin SNAPHAT® housing for 48 mAh battery & crystal, package outline



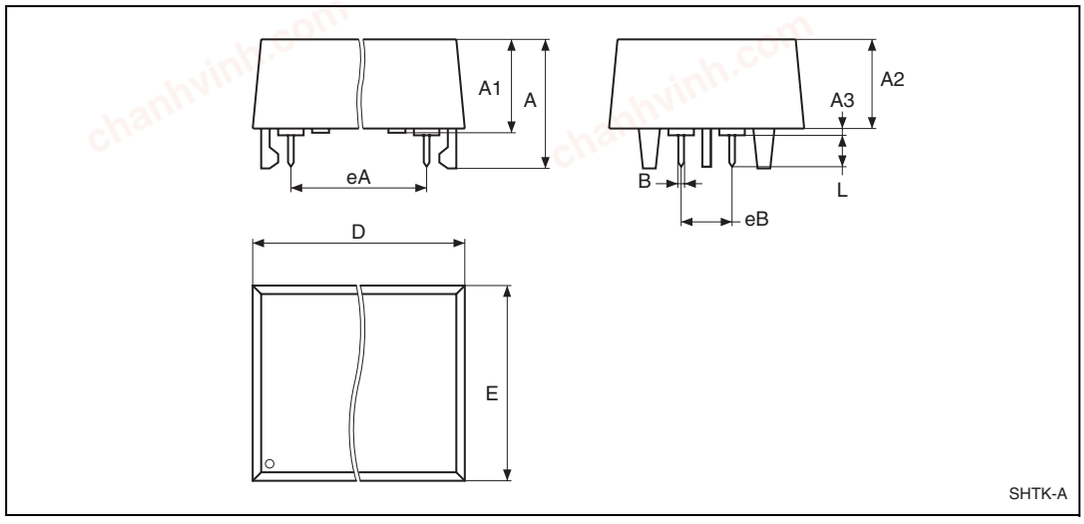
Note: Drawing is not to scale.

Table 14. SH – 4-pin SNAPHAT® housing for 48 mAh battery & crystal, package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

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Figure 16. SH – 4-pin SNAPHAT® housing for 120 mAh battery & crystal, package outline



Note: Drawing is not to scale.

Table 15. SH – 4-pin SNAPHAT® housing for 120 mAh battery & crystal, package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	.0335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	.0710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

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7 Part numbering

Table 16. Ordering information scheme

Example: M48T 18 –100 PC 1 E

Device type

M48T

Supply voltage and write protect voltage

08[1] = V_{CC} = 4.75 to 5.5 V; V_{PFD} = 4.5 to 4.75 V

18/08Y = V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V

Speed

–100 = 100 ns

–150 = 150 ns

–10 = 100 ns (M48T08Y)

Package

PC[1] = PCDIP28

MH[2] = SOH28

Temperature range

1 = 0 to 70 °C

Shipping method

For SOH28:

blank = Tubes (not for new design - use E)

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

TR = Tape & reel (not for new design - use F)

For PCDIP28:

blank = ECOPACK® package, tubes

1. The M48T08/18 part is offered with the PCDIP28 (e.g., CAPHAT™) package only.
2. The SOIC package (SOH28) requires the SNAPHAT® battery/crystal package which is ordered separately under the part number “M4TXX-BR12SH” in plastic tube or “M4TXX-BR12SHTR” in tape & reel form (see *Table 17*). The M48T08Y part is offered in the SOH28 (SNAPHAT) package only.

Caution: Do not place the SNAPHAT® battery package “M4TXX-BR12SH” in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

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Table 17. SNAPHAT® battery table

Part number	Description	Package
M4T28-BR12SH	Lithium battery (48 mAh) SNAPHAT®	SH
M4T32-BR12SH	Lithium battery (120 mAh) SNAPHAT®	SH

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8 Environmental information

Figure 17. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

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9 Revision history

Table 18. Document revision history

Date	Revision	Changes
Dec-1999	1	First Issue
07-Feb-2000	2	From Preliminary Data to Datasheet; Battery Low Flag paragraph changed; 100ns speed class identifier changed (*Table 3*, *4*)
11-Jul-2000	2.1	t_{FB} changed (*Table 10*); Watchdog Timer paragraph changed
16-Jul-2001	3	Reformatted; SNAPHAT battery table added (*Table 17*); added temp./voltage info. to tables (*Table 8*, *9*, *3*, *4*, *10*, *11*).
01-Aug-2001	3.1	Reference to App. Note corrected in “Calibrating the Clock” section
21-Dec-2001	3.2	Changes to text in document to reflect addition of M48T08Y option
06-Mar-2002	3.3	Fix Ordering Information table and add to footnote (*Table 16*)
20-May-2002	3.4	Modify reflow time and temperature footnotes (*Table 6*)
29-Aug-2002	3.5	t_{DR} specification temperature updated (*Table 11*)
28-Mar-2003	4	v2.2 template applied; updated test conditions (*Table 10*)
10-Dec-2003	5	Reformatted
30-Mar-2004	6	Reformatted; Lead-free (Pb-free) information package update (*Table 6*, *16*)
13-Dec-2005	7	Updated template, Lead-free information, removed footnote (*Table 9*, *16*)
04-Jul-2007	8	Reformatted; added lead-free second level interconnect information to cover page and *Section 6: Package mechanical data*.
10-Feb-2009	9	Updated *Table 6*, text in *Section 6: Package mechanical data*; added *Section 8: Environmental information*; minor formatting changes.
21-Jun-2010	10	Updated *Section 4*, *Table 12*; reformatted document.
07-Jun-2011	11	Updated footnote *1* of *Table 6: Absolute maximum ratings*; updated *Section 8: Environmental information*.

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