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M24256E-F

Datasheet

256-Kbit serial I²C bus EEPROM with configurable device address



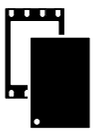
TSSOP8

169 mil width



SO8N

150 mil width



UFDFPN8 (MC)

DFN8 - 2x3 mm



UFDFPN5 (MH)

DFN5 - 1.7x1.4 mm

Product status link
M24256E-F

Features

- Compatible with following I²C bus modes:
  - 1 MHz (Fast-mode Plus)
  - 400 kHz (Fast-mode)
  - 100 kHz (Standard-mode)
- Memory array:
  - 256 Kbit (32 Kbytes) of EEPROM
  - Page size: 64 bytes
  - Additional identification page
- Single supply voltage:
  - 1.6 to 5.5 V
- Operating temperature range
  - From -40°C up to +85°C
- Write cycle time:
  - Byte write within 5 ms
  - Page write within 5 ms
- Random and sequential read modes
- Write protection of the whole memory array
- Configurable device address
- Enhanced ESD / latch-up protection
- More than 4 million write cycles
- More than 200-year data retention
- Package
  - SO8N ECOPACK2
  - TSSOP8 ECOPACK2
  - UFDFPN8 ECOPACK2
  - UFDFPN5 ECOPACK2
  - RoHS-compliant and halogen-free (ECOPACK2)

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1 Description

The M24256E-F is a 256-Kbit I^{2}C-compatible EEPROM (electrically erasable programmable read only memory) organized as 32 K × 8 bits.

The M24256E-F can operate with a supply voltage from 1.65 V to 5.5 V, with a clock frequency of 1 MHz (or less), over an ambient temperature range of -40 °C/+85 °C. It can also operate down to 1.6 V, under some restricting conditions.

The M24256E-F offers an additional page of 64 bytes, named identification page, which can be used to store sensitive application parameters which can be (later) permanently locked in read-only mode.

The M24256E-F offers also an additional 8-bit register, named the configurable device address (CDA) register authorizing the user, through software, to configure up to eight possibilities of chip enable address.

1.1 Device block diagram

Figure 1. Logic diagram

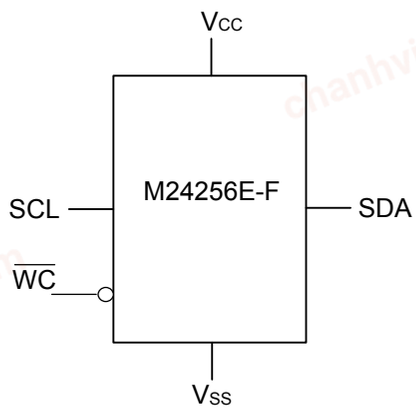


Table 1. Signal names

Signal name	Function	Direction
SDA	Serial data	I/O
SCL	Serial clock	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-
$\overline{WC}$	Write control	Input

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1.2 Device packaging

Figure 2. 5-pin package connection

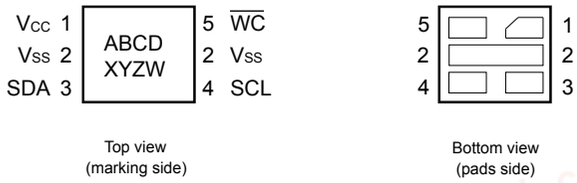
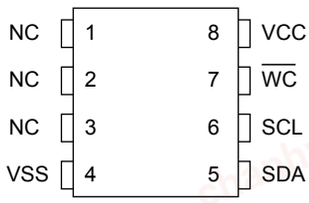


Figure 3. 8-pin package connections, top view



1. NC = Not connected

See Section 10 Package information for package dimensions, and how to identify pin 1.

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2 Signal description

2.1 Serial clock (SCL)

SCL is an input. The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-AND with other open drain or open collector signals on the bus. A pull-up resistor must be connected from serial data (SDA) to V_{CC} (Figure 17 and Figure 18 indicate how to calculate the value of the pull-up resistor).

2.3 Write control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory and the configurable device address register from inadvertent write operations. Write operations are disabled when write control ($\overline{WC}$) is driven high. Write operations are enabled when write control ($\overline{WC}$) is either driven low or left floating.

When write control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, data bytes are not acknowledged.

2.4 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.5 Supply voltage (V_{CC})

2.5.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in Section 9 DC and AC parameters). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (from 10 nF to 100 nF) close to the V_{CC} / V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.5.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Table 7 in Section 9 DC and AC parameters).

Once the V_{CC} is greater than, or equal to, the minimum V_{CC} level, the master must wait for at least T_{WU} before sending the first command to the device. See Table 13 for the value of the wake-up time parameter.

2.5.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in Section 9 DC and AC parameters). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in Section 9 DC and AC parameters).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

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2.5.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

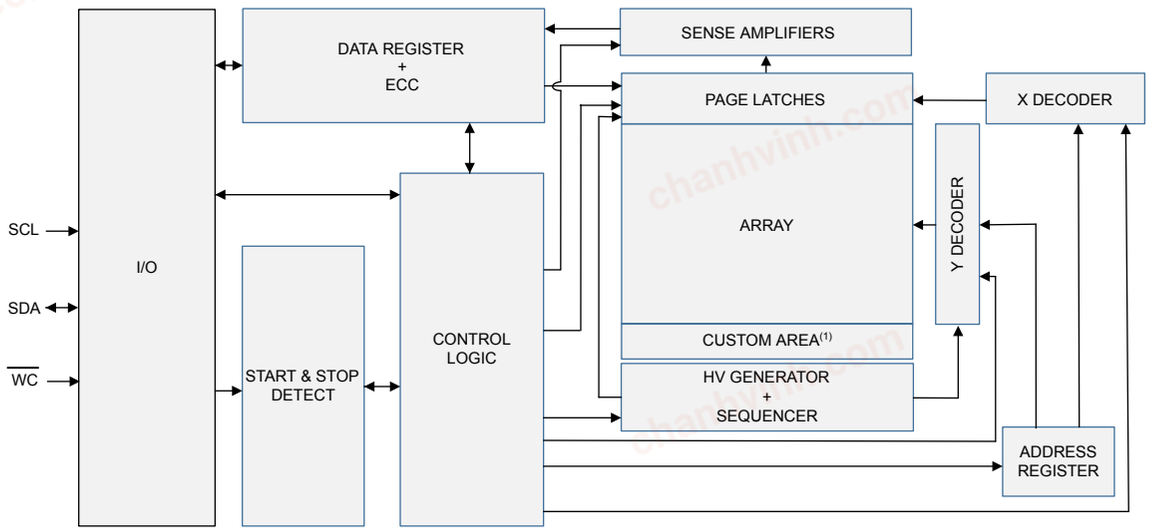
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3 Block diagram

The block diagram of the device is described below

Figure 4. Block diagram



1. ID page and CDA register area

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4 Features

4.1 Identification page

The identification page (64 bytes) is an additional page which can be read or written and (later) permanently locked in read-only mode. It is read or written by issuing the read or write identification page instruction. These instruction uses the same protocol and format as the random address read or page write (from/into memory array) except for the following differences (refer to Table 3, Table 4 and Table 5):

- Device type identifier = 1011b
- MSB address bits A15/A6 are don't care except for address bit A10 which must be ‘0’
- LSB address bits A5/A0 define the byte address inside the Identification page

If the identification page is locked, the data bytes transferred during the write identification page instruction are not acknowledged (NoACK).

Note: MSB address bits A15/A14/A13 with values '110' (A15=1;A14=1;A13=0) are only recognized and decoded for CDA management.

4.2 Configurable device address register (CDA)

As the M24256E-F is delivered without chip enable inputs, the device provides a non-volatile 8-bit register allowing the user to define a configurable device address (CDA) and a specific bit, named device address lock (DAL), to freeze the configurable device address register. This register can be read and written by issuing the read or write configurable device address instructions. These instructions use the same protocol and format as the random address read or page write (from/into memory array) except for the following differences (refer to Table 3, Table 4 and Table 5):

- Device type identifier = 1011b
- MSB address bits A15/A14/A13 must be equal to '110' (A15=1, A14=1 and A13=0)
- MSB address bits A12/A8 are don't care
- LSB address bits A7/A0 are don't care

The description of the configurable device address register is given in Table 2.

Table 2. configurable device address register format

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X (1)	X(1)	X(1)	X(1)	C2	C1	C0	DAL

1. *X = Don’t care bits. Read as 0.*

Note: Factory delivery of the register is 00000000b.

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Bit b7:b4	Reserved bits - Read as '0'. (b7,b6,b5,b4)=(0,0,0,0)
Bit b3:b1	**C2, C1, C0**: Configurable device address bits b3, b2, b1 are used to configure up to eight possibilities of chip enable address: • (b3, b2, b1) = (0, 0, 0): the chip enable address is 000 (factory delivery value) • (b3, b2, b1) = (0, 0, 1): the chip enable address is 001 • (b3, b2, b1) = (0, 1, 0): the chip enable address is 010 • (b3, b2, b1) = (0, 1, 1): the chip enable address is 011 • (b3, b2, b1) = (1, 0, 0): the chip enable address is 100 • (b3, b2, b1) = (1, 0, 1): the chip enable address is 101 • (b3, b2, b1) = (1, 1 0): the chip enable address is 110 • (b3, b2, b1) = (1, 1, 1): the chip enable address is 111
Bit b0	**DAL**: device address lock bit b0 locks the CDA regster in read-only mode: • b0 = 0: bits b3,b2,b1,b0 can be modified • b0 = 1: bits b3,b2,b1,b0 cannot be modified and therefore the CDA register is frozen Note: bits b3 to b0 can be updated (if b0 = 0) in the same write instruction. Setting b0 from 0 to 1 is an irreversible action.

C2, C1, C0 and DAL are defining the chip enable address in the device select code and the device address lock. These bits can be written and re-configured with a write command.

At power up or after reprogramming, the device load the last configuration of C2, C1, C0 and DAL values.

In order to prevent unwanted change of configurable device address bits, the M24256E proposes to protect the CDA register,freezing it in read-only mode. The update of the CDA register is disabled (read-only) when the DAL bit is set to '1' (DAL=1b).

In the same way, the update of the CDA register is enabled when the DAL bit is set to '0' (DAL= 0b).

Note:

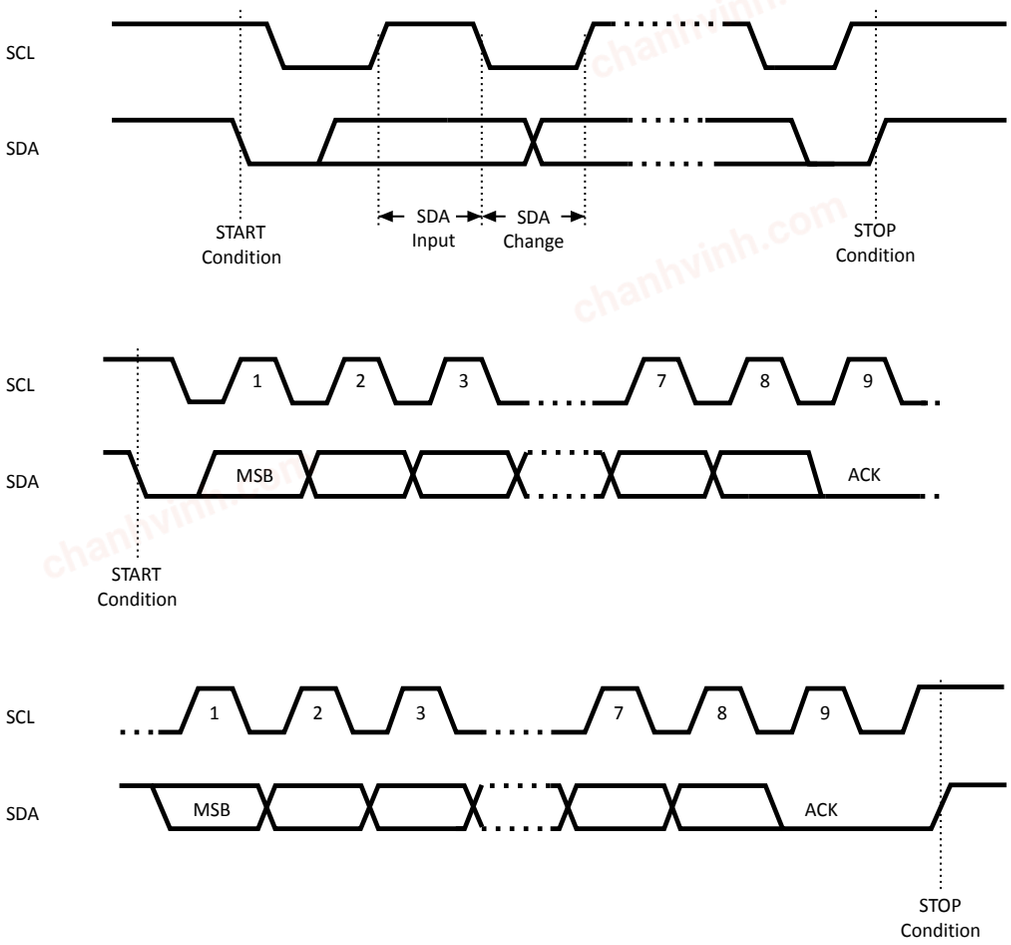
- *Updating the DAL bit from 0 to 1 is an irreversible action: the C2,C1,C0 and DAL bits cannot be updated any more.*
- *If the write control input ($\overline{WC}$) is driven high or if the DAL bit is set to 1, the write configurable device address command is not executed and the accompanying data byte is not acknowledged, as shown in Figure 7.*

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5 Device operation

The device supports the I²C protocol. This is summarized in Figure 5. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data is defined to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 5. I²C bus protocol



5.1 Start condition

Start is identified by a falling edge of serial data (SDA) while serial clock (SCL) is stable in the high state. A start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) serial data (SDA) and serial clock (SCL) for a start condition.

5.2 Stop condition

Stop is identified by a rising edge of serial data (SDA) while serial clock (SCL) is stable in the high state. A Stop condition terminates communication between the device and the bus master. A Read instruction is terminated by no ACK followed by a stop condition to force the device into the standby mode.

A stop condition at the end of a write instruction triggers the internal write cycle.

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5.3 Data input

During data input, the device samples serial data (SDA) on the rising edge of serial clock (SCL). For correct device operation,serial data (SDA) must be stable during the rising edge of serial clock (SCL), and the serial data (SDA) signal must change only when serial clock (SCL) is driven low.

5.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases serial data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls serial data (SDA) low to acknowledge the receipt of the eight data bits.

5.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a start condition. Following this, the bus master sends the device select code and byte address as specified in Table 3, Table 4 and Table 5.

Table 3. Device address

Features	Device type identifier				Chip enable address			Bit 0 (LSB)
	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	
Memory	1	0	1	0	C2	C1	C0	R/W
Identification page	1	0	1	1	C2	C1	C0	R/W
Identification page lock	1	0	1	1	C2	C1	C0	R/W
Configurable device address	1	0	1	1	C2	C1	C0	R/W

1. *The most significant bit, b7, is sent first.*

Table 4. First word address

Features	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	X(2)	A14	A13	A12	A11	A10	A9	A8
Identification page	X(3)	X(3)	X(3)	X	X	0	X	X
Identification page lock	X(3)	X(3)	X(3)	X	X	1	X	X
Configurable device address	1	1	0	X	X	X	X	X

1. *The most significant bit, b7, is sent first.*
2. *X = Don't care*
3. *For identification page do not use A15/A14/A13 equal to '110'*

Table 5. Second word address

Features	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	A7	A6	A5	A4	A3	A2	A1	A0
Identification page	X(2)	X	A5	A4	A3	A2	A1	A0
Identification page lock	X	X	X	X	X	X	X	X
Configurable device address	X	X	X	X	X	X	X	X

1. *The most significant bit, b7, is sent first.*
2. *X = Don't care*

When the device select code is received, the device responds only if the bit 3, bit 2 and bit 1 values match the values of the C2, C1 and C0 bits programmed in the configurable device address register.

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If a match occurs, the corresponding device gives an acknowledgement on serial data (SDA) during the 9th bit time.

If the device does not acknowledge the device select code, the device de-selects itself from the bus, and goes into standby mode (therefore it does not acknowledge the device select code).

The 8th bit is the Read/Write bit ($\overline{RW}$). This bit is set to 1 for read and 0 for write operations.

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6 Instructions

6.1 Write operations on memory array

Following a start condition the bus master sends a device select code with the R$\overline{W}$ bit (R$\overline{W}$) set to 0. The device acknowledges this, as shown in Figure 6, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Section 5.5 Device addressing (Table 3, Table 4 and Table 5) how to address the memory array.

When the bus master generates a stop condition immediately after a data byte ACK bit (in the "10^{th} bit" time slot), either at the end of a byte write or a page write, the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

After the stop condition and the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

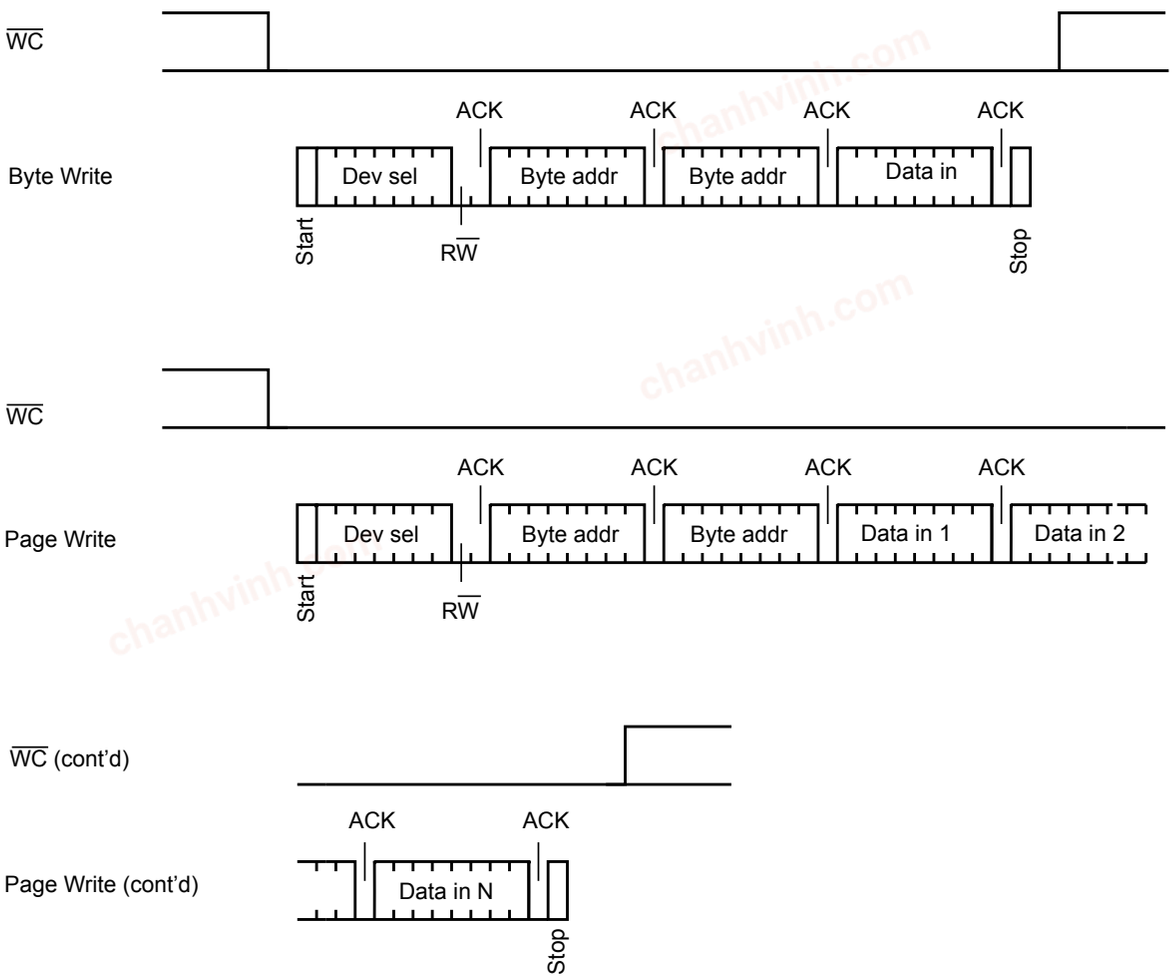
If the write control input ($\overline{WC}$) is driven high, the write instruction is not executed and the accompanying data bytes are not acknowledged, as shown in Figure 7.

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6.1.1 Byte write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is write-protected, by write control $\overline{WC}$ being driven high, the device replies with noACK, and the location is not modified, as shown in Figure 7. If, instead, the addressed location is not write-protected, the device replies with ACK. The bus master terminates the transfer by generating a stop condition, as shown in Figure 6.

Figure 6. Write mode sequence with $\overline{WC}$ = 0 (data write enabled)



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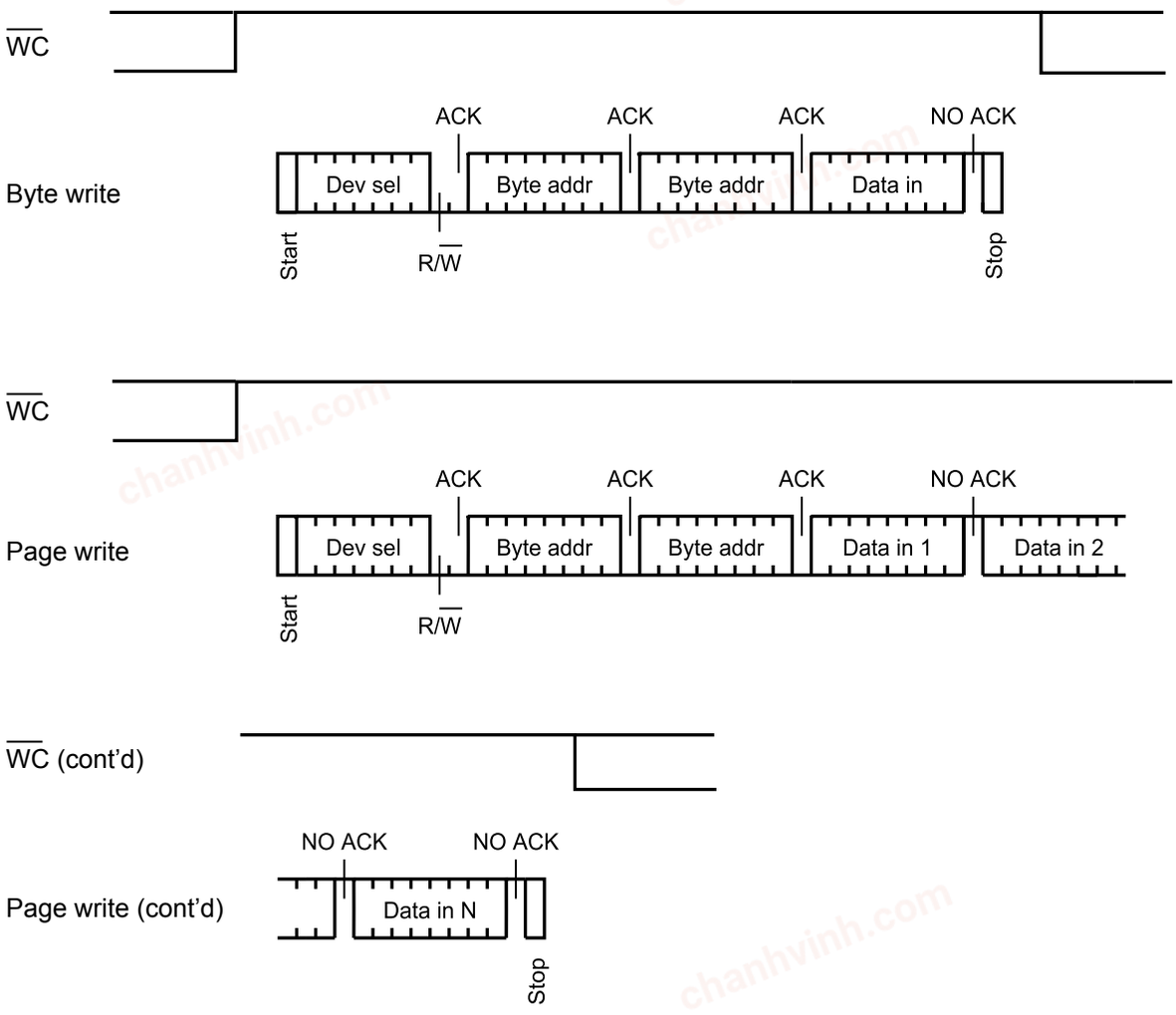
6.1.2 Page write

The page write mode allows up to 64 bytes to be written in a single write cycle, provided they are all located in the same page in the memory: that is, the most significant memory address bits, A14/A6 are the same. If more bytes than those that will fit up to the end of the page are sent, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 64 bytes of data, each one is acknowledged by the device if write control ($\overline{WC}$) is low. If write control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a no ACK, as shown in Figure 7. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a stop condition.

Figure 7. Write mode sequence $\overline{WC}$ = 1 (data write inhibited)



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6.1.3 ECC (error correction code) and write cycling

The error correction code (ECC) is an internal logic function which is transparent for the I2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes. Inside a group, if a single bit out of the four bytes happens to be erroneous during a read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group (a group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.)

As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte 0, byte 1, byte 2 and byte 3 of the same group must remain below the maximum value defined in Table 10.

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6.1.4 Minimizing write delays by polling on ACK

During the internal write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in AC characteristics tables in Section 9 DC and AC parameters, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

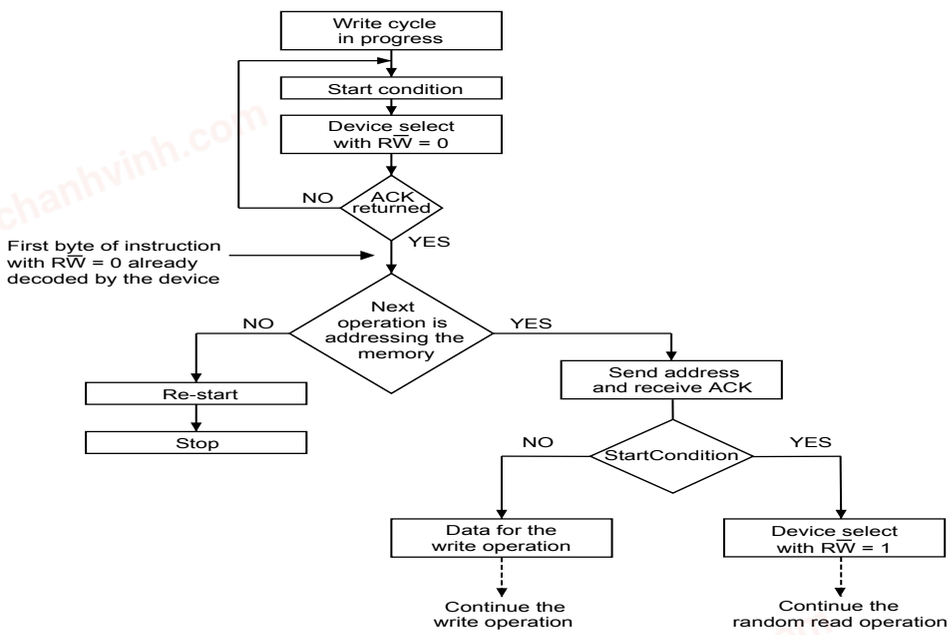
The polling sequence, as shown in Figure 8, is:

- Initial condition: a write cycle is in progress.
- Step 1: the bus master issues a start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal write cycle, no ACK will be returned and the bus master goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Note: In case of write command to the configurable device address register when C2, C1 and C0 are re-configured, the device returns ACK only if:

- *Chip enable address of the device select code is equal to the new C2, C1 and C0 values*
- *An internal write cycle is completed (new C2, C1 and C0 values have been programmed in the chip enable register).*

Figure 8. Write cycle polling flowchart using ACK



Note: The seven most significant bits of the device select code of a random read (bottom right box in the Figure 8) must be identical to the seven most significant bits of the device select code of the write (polling instruction in the Figure 8).

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6.2 Write identification page

The identification page (64 bytes) is an additional page which can be written and (later) permanently locked in read-only mode. It is written by issuing the write identification page instruction. This instruction uses the same protocol and format as page write (into memory array), except for the device select code and the address. See in Section 5.5 Device addressing (Table 3, Table 4 and Table 5) how to address the identification page.

If the identification page is locked, the data bytes transferred during the write identification page instruction are not acknowledged (noACK).

6.2.1 Lock identification page

The lock identification page instruction (lock ID) permanently locks the identification page in read-only mode. The lock ID instruction is similar to byte write (into memory array) except for the device select code and the address.

See in Section 5.5 Device addressing (Table 3, Table 4 and Table 5) how to address the identification page.

The sent data byte must have the b1 bit equal to '1' (b1=1) and the others value of the bits b7 to b2 and b0 are "Don't Care". The data byte have the following format: xxxx xx1x (where x = Don't Care)"

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6.3 Write operations on configurable device address register

Write operations on configurable device address register are performed according to the state of the device address lock bit (DAL) or the status of $\overline{WC}$ line. If the configurable device address register is write protected with DAL=1 or hard protected with $\overline{WC}$ line driven high, the write operation on this register is not executed and the accompanying data byte is not acknowledged as shown in Figure 10.

Following a start condition the bus master sends a device select code with the $\overline{RW}$ bit ($\overline{RW}$) set to 0. The device acknowledges this, as shown in Figure 9, and waits for the address bytes where the register is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Section 5.5 Device addressing (Table 3, Table 4 and Table 5) how to address the configurable device address register.

When the bus master generates a stop condition immediately after the data byte ACK bit (in the "10th bit" time slot), the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests (no ACK).

If the three bits C2, C1 and C0 have been re-configured with a correct write command, the device acknowledges if the chip enable address of the device select code is equal to the new values of C2, C1 and C0, otherwise noACK.

Sending more than one byte aborts the write cycle (configurable device address register content is not changed).

Bits (DAL + C2, C1, C0) can be updated (DAL = '0' to '1') in the same program instruction.

Figure 9. Write on configurable device address register

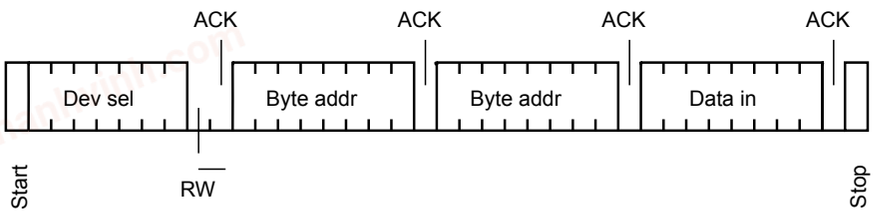
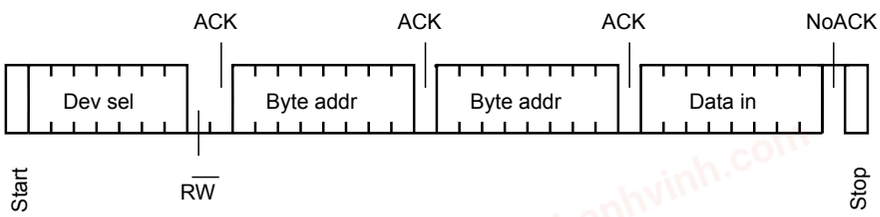


Figure 10. Write configurable device address register with DAL=1 or hard write protected with $\overline{WC}$ line driven high



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6.4 Read operations on memory array

Read operations are performed independently of the state of the write control ($\overline{WC}$) signal.

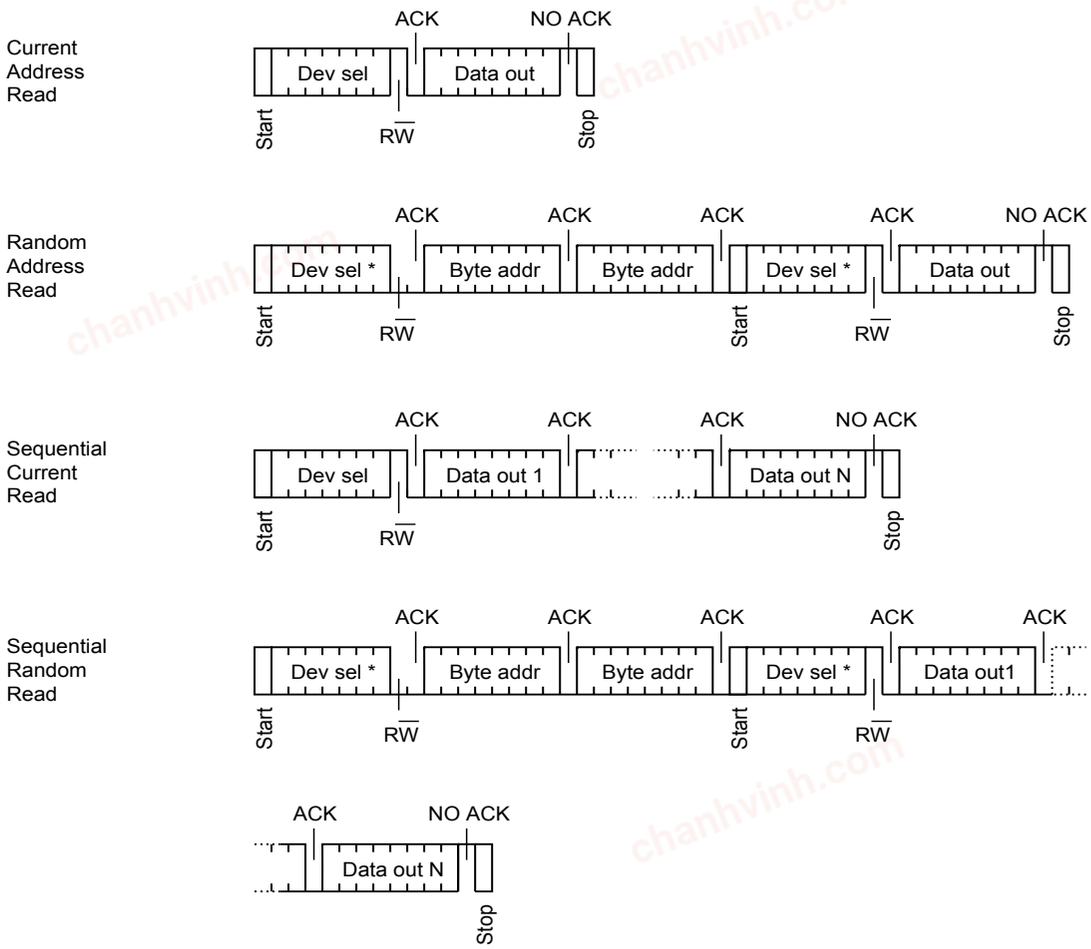
After the successful completion of a read operation, the device internal address counter is incremented by one, to point to the next byte address.

Following a start condition the bus master sends a device select code with the R/W bit (R/W) set to '0'. The device acknowledges this and waits for the two bytes address. The device responds to each address byte with an acknowledge bit. Then, the bus master sends another start condition, and repeats the device select code,with the RW bit set to '1'. The device acknowledges this, and outputs the contents of the data. See in Section 5.5 Device addressing (Table 3, Table 4 and Table 5) how to address the memory array.

After each byte read (data out), the device waits for an acknowledgement (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its standby mode after a stop condition.

After the successful completion of a read operation, the device internal address counter is incremented by one, to point to the next byte address.

Figure 11. Read mode sequences



Note: The seven most significant bits of the first device select code of a random read must be identical to the seven most significant bits of the device select code of the write.

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6.4.1 Random address read

A dummy write is first performed to load the address into this address counter (as shown in Figure 11) but without sending a stop condition. Then, the bus master sends another start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. To terminate the transfer master, master must not acknowledge the byte, and sends a stop condition.

6.4.2 Current address read

For the current address read operation, following a start condition, the bus master only sends a device select code with the RW bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a stop condition, as shown in Figure 11, without acknowledging the byte.

Note: The address counter value is defined by instructions accessing either the memory or the register or the identification page. When accessing the register or the identification page, the address counter value is loaded with the register or the identification page byte location, therefore the next current address read in the memory uses this new address counter value. When accessing the memory, it is safer to use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the current address read instruction.

6.4.3 Sequential read

This operation can be used after a current address read or a random address read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a stop condition, as shown in Figure 11.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

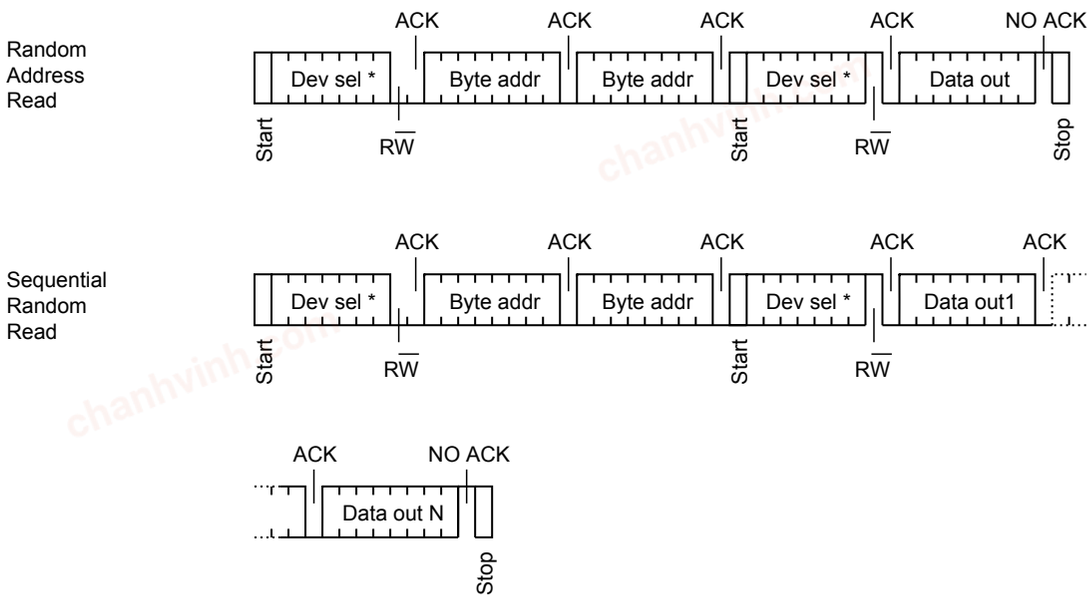
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6.5 Read identification page

Following a start condition the bus master sends a device select code with the RW bit (RW) set to '0'. The device acknowledges this and waits for the address bytes where the identification page is located. The device responds to each address byte with an acknowledge bit. The bits A6/A0 define the byte address inside the identification page. Then, the bus master sends another start condition, and repeats the same device select code but with the RW bit set to '1'. The device acknowledges this, and outputs the contents of the identification page. See in Section 5.5 Device addressing (Table 3, Table 4 and Table 5) how to address identification page.

The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the identification page from location 10d, the number of bytes should be less than or equal to 54, as the ID page boundary is 64 bytes). After the 64th byte of the identification page, there is no “roll-over” to the beginning of the page. To terminate the stream of data byte, the bus master must not acknowledge the byte, and must generate a stop condition, as shown in Figure 15.

Figure 12. Random read identification page



*: The seven most significant bits of the device select code of a random read must be identical.

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6.6 Read the lock status

The locked/unlocked status of the identification page can be checked by transmitting a specific truncated command.

Following a start condition the bus master sends a device select code with the R/W bit (RW) set to 0. The device acknowledges this and waits for the address bytes where the identification page is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Section 5.5 Device addressing (Table 3, Table 4 and Table 5) how to address the identification page.

The device returns an acknowledge bit after the data byte if the identification page is unlocked as shown in Figure 13, otherwise a NoAck bit as shown in Figure 14, if the identification page is locked.

Right after this, it is recommended to transmit to the device a start condition followed by a stop condition, so that:

- Start: the truncated command is not executed because the start condition resets the device internal logic
- Stop: the device is then set back into standby mode by the stop condition.

Figure 13. Read lock status with identification page unlocked

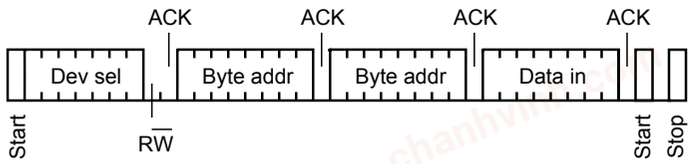
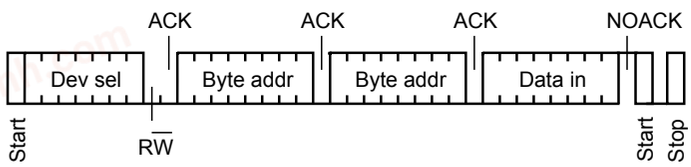


Figure 14. Read lock status with identification page locked



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6.7 Read operations on configurable device address register

Following a start condition the bus master sends a device select code with the $\overline{RW}$ bit ($\overline{RW}$) set to 0. The device acknowledges this and waits for the address bytes where the CDA register is located. The device responds to each address byte with an acknowledge bit. Then, the bus master sends another start condition, and repeats the device select code,with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the contents of the CDA register. See in Section 5.5 Device addressing (Table 3, Table 4 and Table 5) how to address the configurable device address register.

To terminate the stream of data byte, the bus master must not acknowledge the byte, and must generate a stop condition, as shown in Figure 15.

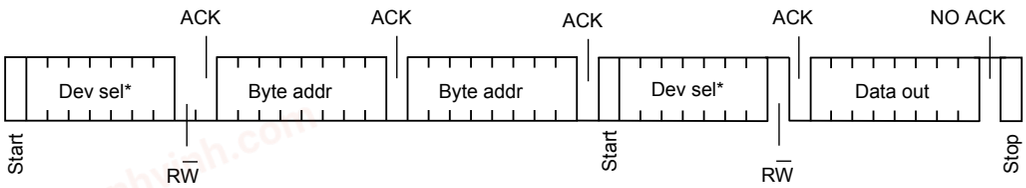
After the successful completion of a read configurable device address, the device internal address counter is not incremented by one, to point to the next byte address. Reading more than one byte loops on reading the configurable device address register value.

The configurable device address register cannot be read while a write cycle (t_W) is ongoing.

The configurable device address bits (C2, C1, C0) values can be checked by sending the device select code.

- If the chip enable address bit 3, bit 2, bit 1 sent in the device select code is matching with the C2, C1 and C0 values, the device sends an ACK
- Otherwise, device will answer no ACK

Figure 15. Random read on configuration device address register



* The seven most significant bits of the first device select code of a random read must be identical to the seven most significant bits of the second device select code

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7 Initial delivery state

At factory delivery, the device is delivered with:

- All the memory array and identification page bits set to 1 (each byte contains FFh)
- The CDA register sets to 00000000b (00h)

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8 Maximum ratings

Stressing the device outside the ratings listed in Table 6 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these conditions, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model) (2)	-	4000	V

1. *Compliant with JEDEC standard J-STD-020 (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001, C1=100 pF, R1=1500 Ω).*

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9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 7. Operating conditions

Symbol	Parameter	Min.		Max.	Unit
V_{CC}	Supply voltage	1.6	1.65	5.5	V
T_A	Ambient operating temperature: READ	-40	-40	85	°C
	Ambient operating temperature: WRITE	0	-40	85	
f_C	Operating clock frequency	-		1	MHz

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 16. AC measurement I/O waveform

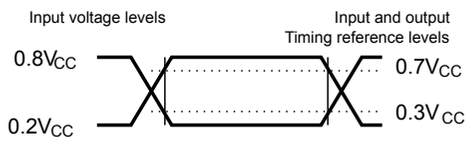


Table 9. Input parameters

Symbol	Parameter (1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF
Z_L	Input impedance ($\overline{WC}$)	V_{IN} < 0.3 V_{CC}	30	-	kΩ
Z_H		V_{IN} > 0.7 V_{CC}	500	-	kΩ

1. *Evaluated by characterization – Not tested in production.*

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Table 10. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition	Max.	Unit
Ncycle	Write cycle endurance(1)	$T_A \leq 25$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4 000 000	Write cycles(2)
		$T_A = 85$°C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1 200 000	

1. *The write cycle endurance is defined by characterization and qualification. For devices embedding the ECC functionality, the write cycle endurance is defined for group of four bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer.*
2. *A write cycle is executed when either a write CDA register, a page write, a byte write , a write identification page or a lock identification page instruction is decoded. When using the byte write, the page write or the write identification page, refer also to Section 6.1.3 ECC (error correction code) and write cycling.*

Table 11. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention (1)	$T_A = 55$ °C	200	Year

1. *The data retention behaviour is checked in production, while the data retention limit defined in this table is extracted from characterization and qualification results.*

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Table 12. DC characteristics

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	f_C = 400 kHz	-	0.5	mA
		f_C = 1 MHz	-	1	
I_{CC0}	Supply current (Write)	Value averaged over t_W	-	1 (1)	mA
I_{CC1}	Standby supply current	Device not selected, (2) $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} < 2.5 V	-	1	µA
		Device not selected, (2) $V_{IN} = V_{SS}$ or V_{CC}, $V_{CC} \geq$ 2.5 V	-	2	
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	1.6 ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 ≤ V_{CC} ≤ 5.5 V	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.6 ≤ V_{CC} < 2.5 V	0.75 V_{CC}	6	V
		2.5 ≤ V_{CC} ≤ 5.5 V	0.7 V_{CC}	6	V
	Input high voltage ($\overline{WC}$)	1.6 ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC} + 0.6	V
		2.5 ≤ V_{CC} ≤ 5.5 V	0.7 V_{CC}	V_{CC} + 0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.6 V	-	0.2	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. *Evaluated by characterization – Not tested in production.*
2. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*

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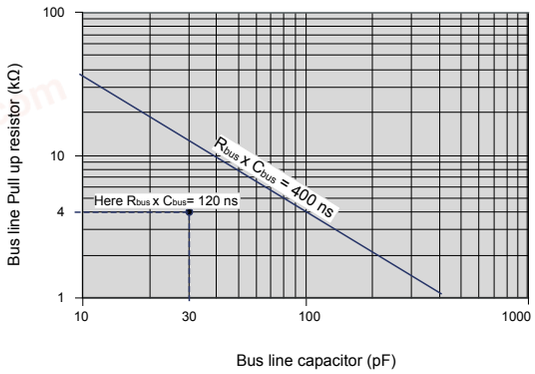
Table 13. AC characteristics

Symbol	Alt.	Parameter	Standard mode		Fast-mode		Fast-mode plus		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_C	f_{SCL}	Clock frequency	-	100	-	400	-	1000	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	4	-	600	-	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	4.7	-	1300	-	500	-	ns
t_{QL1QL2} (1)	t_F	SDA (out) fall time	-	300	20(2)	300	20(2)	120	ns
t_{XH1XH2}	t_R	Input signal rise time	-	1000	(3)	(3)	(4)	(4)	ns
t_{XL1XL2}	t_F	Input signal fall time	-	300	(3)	(3)	(4)	(4)	ns
t_{DVCH}	$t_{SU:DAT}$	Data in set up time	250	-	100	-	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	0	-	0	-	ns
t_{CLQX} (5)	t_{DH}	Data out hold time	100	-	100	-	100	-	ns
t_{CLQV} (6)	t_{AA}	Clock low to next data valid (access time)	-	4500	-	900	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	4700	-	600	-	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	4000	-	600	-	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	4000	-	600	-	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	4700	-	1300	-	500	-	ns
t_{WLDL} (1)(7)	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	0	-	0	-	µs
t_{DHWH} (1)(8)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	1	-	1	-	µs
t_W	t_{WR}	Write time	-	5	-	5	-	5	ms
t_{NS}	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	50	-	50	-	50	ns
t_{WU} (1)(9)	-	Wake up time	-	5	-	5	-	5	µs

1. *Evaluated by characterization – Not tested in production.*
2. *With CL = 10 pF.*
3. *There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when fC < 400 kHz*
4. *There are no minimum or maximum values for the input signal rise and fall times. However, it is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns when f_C < 1 MHz.*
5. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.*
6. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3V_{CC} or 0.7V_{CC}, assuming that R_{bus} × C_{bus} time constant is within the values specified in Figure 17 and Figure 18.*
7. *$\overline{WC}$=0 set up time condition to enable the execution of a write command.*
8. *$\overline{WC}$=0 hold time condition to enable the execution of a write command.*
9. *Wake up time: Delay between the V_{CCmin} stable and the first accepted commands.*

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Figure 17. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz



The R_{bus} x C_{bus} time constant must be below the 400 ns time constant line represented on the left

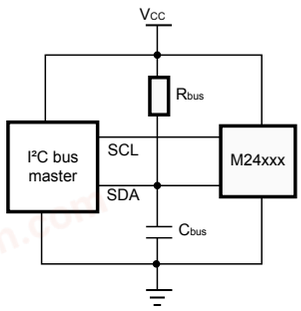
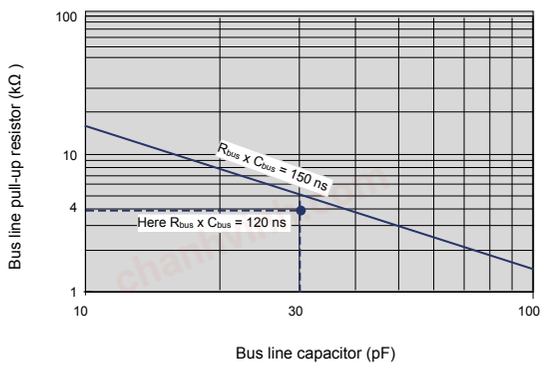
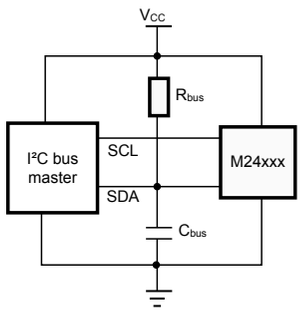


Figure 18. Maximum R_{bus} value vs. bus parasitic capacitance (C_{bus}) for an I^2C bus at f_C = 1MHz

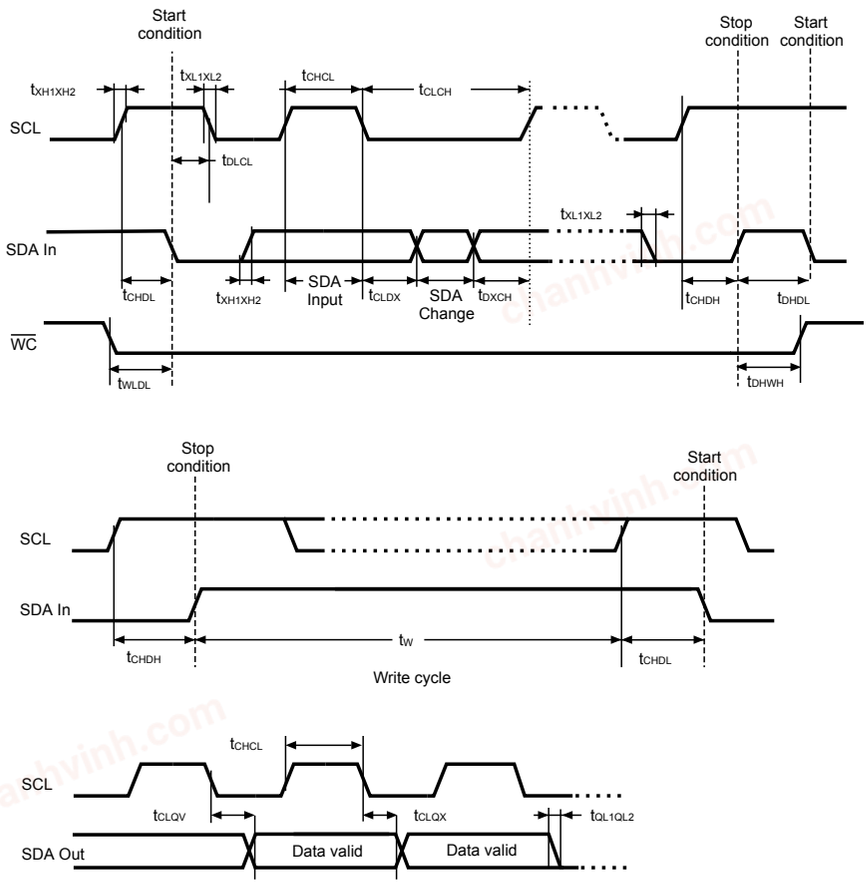


The R_{bus} x C_{bus} time constant must be below the 150 ns time constant line represented on the left



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Figure 19. **AC waveforms**



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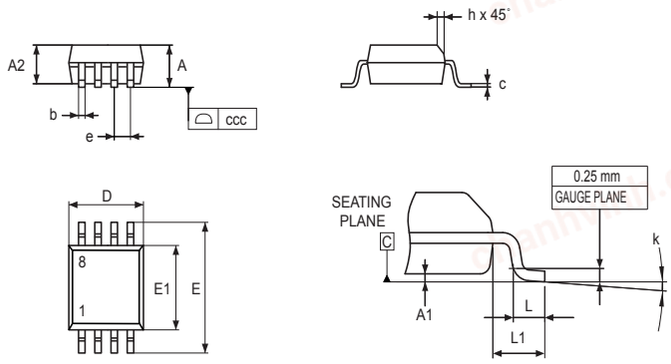
10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

Figure 20. SO8N – Outline



1. Drawing is not to scale.

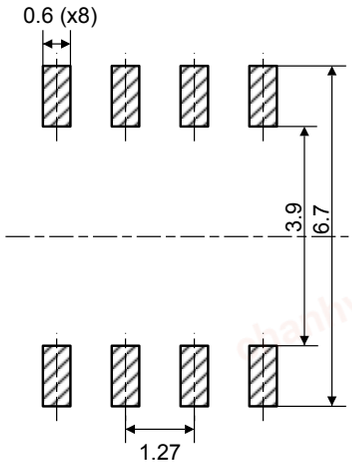
Table 14. SO8N – Mechanical data

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.100	-	0.230	0.0030	-	0.0091
D(2)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(3)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

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Figure 21. **SO8N - Recommended footprint**



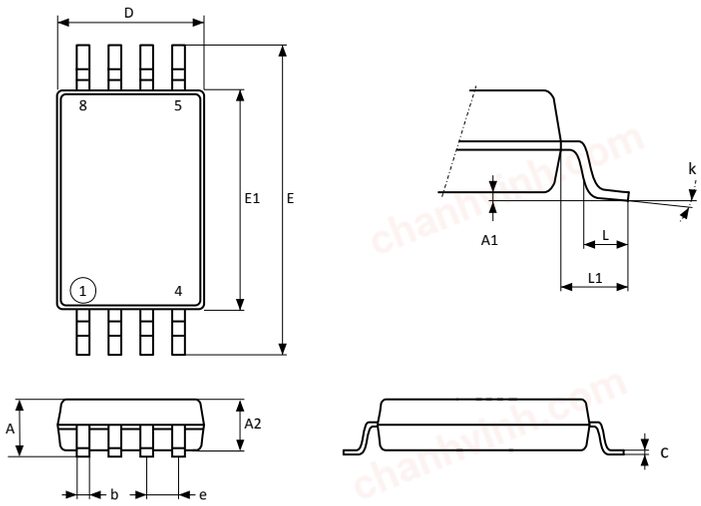
1. Dimensions are expressed in millimeters.

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10.2 TSSOP8 package information

This TSSOP is an 8-lead, 3 x 6.4 mm, 0.65 mm pitch, thin shrink small outline package.

Figure 22. TSSOP8 – Outline



1. Drawing is not to scale.

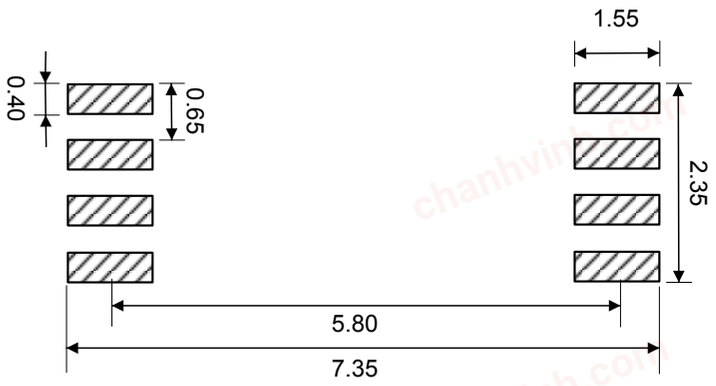
Table 15. TSSOP8 – Mechanical data

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

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Figure 23. **TSSOP8 – Recommended footprint**



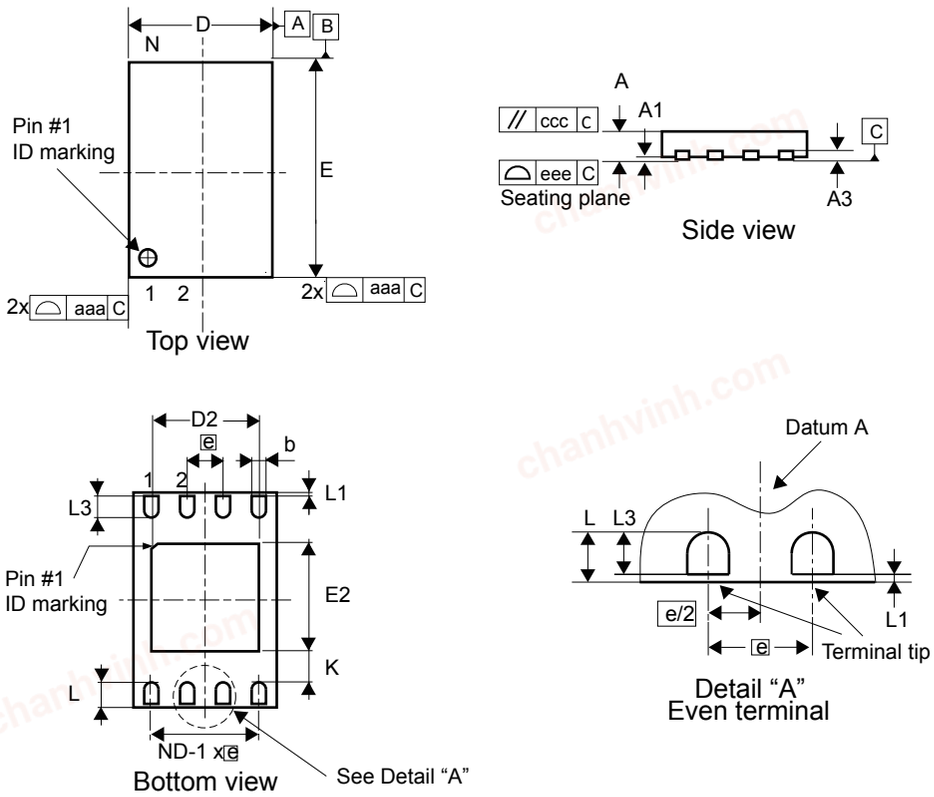
1. Dimensions are expressed in millimeters.

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10.3 UFDFPN8 (DFN8) package information

This UFDFPN is a 8-lead, 2 x 3 mm, 0.5 mm pitch ultra thin profile fine pitch dual flat package.

Figure 24. UFDFPN8 - Outline



1. Maximum package warpage is 0.05 mm.
2. Exposed copper is not systematic and can appear partially or totally according to the cross section.
3. Drawing is not to scale.
4. The central pad (the area E2 by D2 in the above illustration) must be either connected to V_{SS} or left floating (not connected) in the end application.

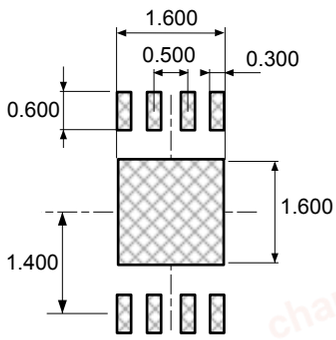
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Table 16. UFDFPN8 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.450	0.550	0.600	0.0177	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
b[2]	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
D2	1.200	-	1.600	0.0472	-	0.0630
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
E2	1.200	-	1.600	0.0472	-	0.0630
e	-	0.500	-	-	0.0197	-
K	0.300	-	-	0.0118	-	-
L	0.300	-	0.500	0.0118	-	0.0197
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
aaa	-	-	0.150	-	-	0.0059
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee[3]	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.*
3. *Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.*

Figure 25. UFDFPN8 - Recommended footprint



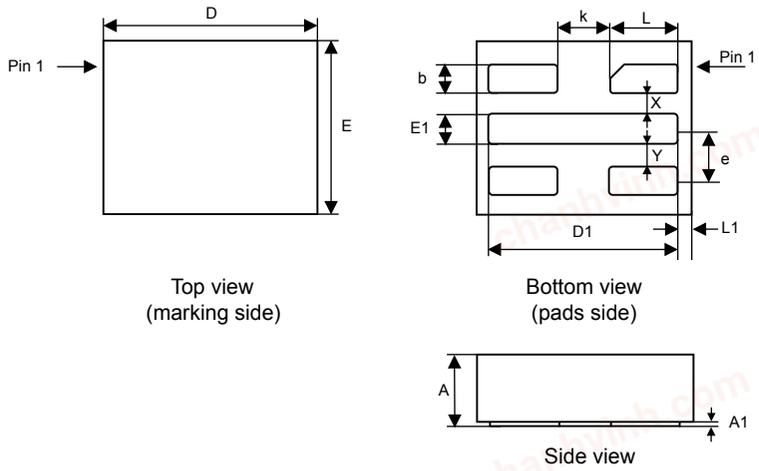
1. Dimensions are expressed in millimeters.

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10.4 UFDFPN5 (DFN5) package information

UFDFPN5 is a 5-lead, 1.7 × 1.4 mm, 0.55 mm thickness, ultra thin fine pitch dual flat package.

Figure 26. UFDFPN5 - Outline



1. Maximum package warpage is 0.05 mm.
2. Exposed copper is not systematic and can appear partially or totally according to the cross section.
3. Drawing is not to scale.
4. On the bottom side, pin 1 is identified by the specific pad shape and, on the top side, pin 1 is defined from the orientation of the marking. When reading the marking, pin 1 is below the upper left package corner.

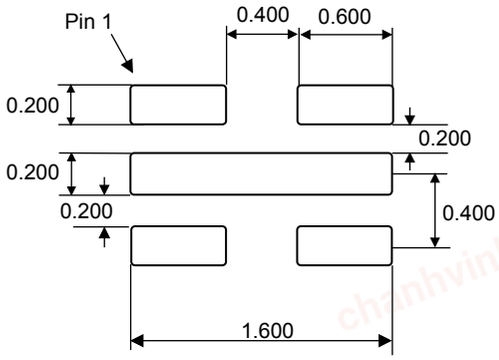
Table 17. UFDFPN5 - Mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	-	0.050	0.0000	-	0.0020
b(1)	0.175	0.200	0.225	0.0069	0.0079	0.0089
D	1.600	1.700	1.800	0.0630	0.0669	0.0709
D1	1.400	1.500	1.600	0.0551	0.0591	0.0630
E	1.300	1.400	1.500	0.0512	0.0551	0.0591
E1	0.175	0.200	0.225	0.0069	0.0079	0.0089
X	-	0.200	-	-	0.0079	-
Y	-	0.200	-	-	0.0079	-
e	-	0.400	-	-	0.0157	-
L	0.500	0.550	0.600	0.0197	0.0217	0.0236
L1	-	0.100	-	-	0.0039	-
k	-	0.400	-	-	0.0157	-

1. *Dimension b applies to plated terminal and is measured between 0.15 and 0.30mm from the terminal tip.*

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Figure 27. **UFDFPN5 - Recommended footprint**



1. Dimensions are expressed in millimeters.

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11 Ordering information

Table 18. Ordering information scheme

Example:	M24	256E -	F	MH	6	T	P

Device type

M24 = I^2C serial access EEPROM

Device function

256E = 256 Kbit (32 K x 8 bit)

Operating voltage

F = V_{CC} = 1.6 V to 5.5 V

Package (1)

MN = SO8 (150 mil width)

DW = TSSOP8 (169 mil width)

MC = UFDFPN8 (DFN8)

MH = UFDFPN5 (DFN5)

Device grade

6 = Industrial device tested with standard test flow over -40 to 85 °C

Option

T = Tape and reel packing

blank = tube packing

Plating technology

P or G = ECOPACK2

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).*

Note: Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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Revision history

Table 19. **Document revision history**

Date	Revision	Changes
01-Mar-2022	1	Initial release

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