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LM2904B

Datasheet

Low-power dual operational amplifiers



MiniSO8

Features

- Up to 36 V operating supply voltage
- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.2 MHz (temperature compensated)
- Very low supply current/amplifier, essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rail
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to Vcc -1.5 V

Applications

- Telecom equipment
- Power management
- Industrial application
- Automotive

Product status link
LM2904B

Description

The LM2904B consists of two independent, high gain operational amplifiers (op-amps) that have frequency compensation implemented internally. They are designed specifically for automotive and industrial control systems. This circuit operates from a single power supply over a wide range of voltages. The LM2904B is guaranteed up to 36 V supply voltage operation. The low power supply drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied from the standard 5 V which is used in logic systems and easily provides the required electronic interfaces without requiring any additional power supply. In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from a single power supply.

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1 Schematic diagram

Figure 1. **Schematic diagram**

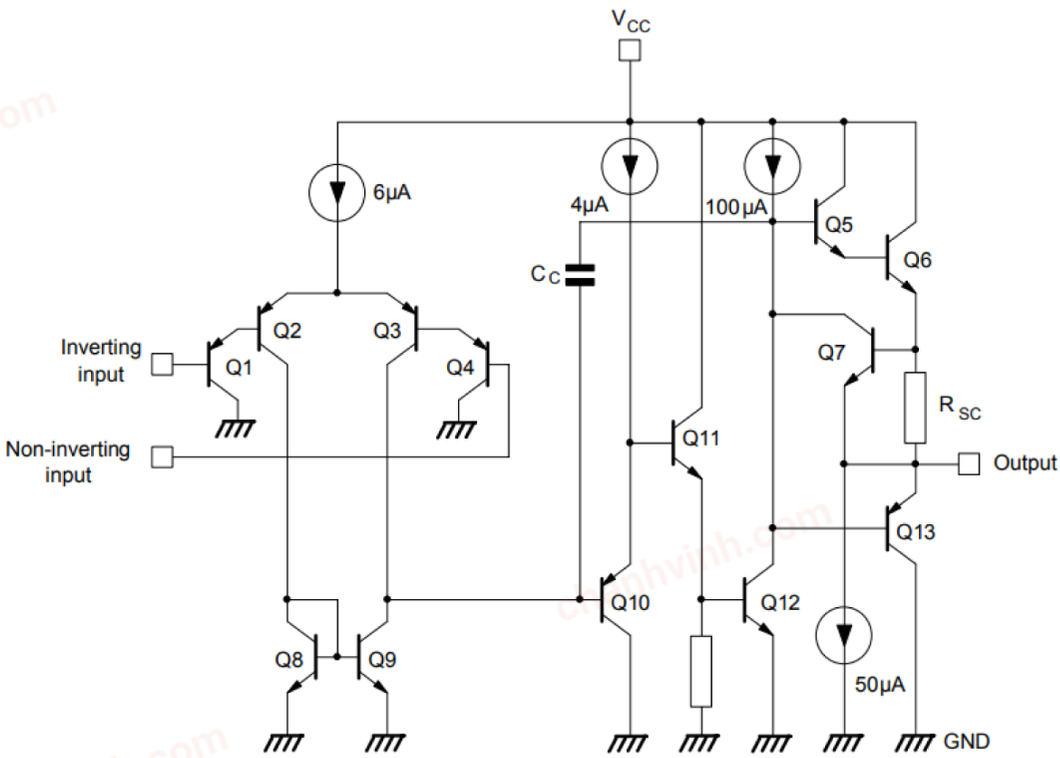
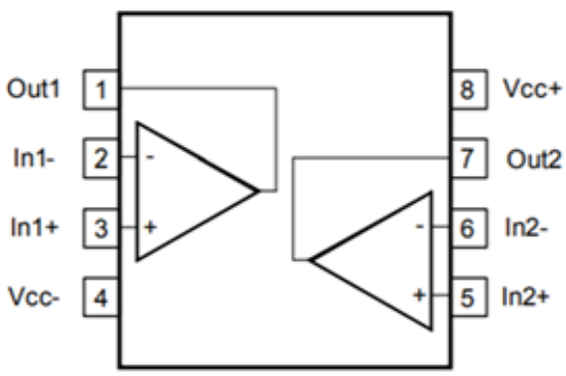


Figure 2. **Pin connections (top view)**



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2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	±20 or 40	V
V_{id}	Differential input voltage(2)	±40	
V_{in}	Input voltage	-0.3 to 40	
	Output short-circuit duration (3)	Infinite	s
I_{in}	Input current: V_{IN} driven negative(4)	5 mA in DC or 50 mA in AC, (duty cycle = 10 %, T = 1 s)	mA
	Input current: V_{in} driven positive above AMR value(5)	0.4	
T_{stg}	Storage temperature range	-65 to 150	°C
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction-to-ambient(6) MiniSO8	190	°C/W
R_{thjc}	Thermal resistance junction-to-case (6) MiniSO8	39	
ESD	HBM: human body model(7)	300	V
	MM: machine model (8)	200	
	CDM: charged device model (9)	1500	

1. *All voltage values, except differential voltage, are with respect to network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.*
3. *Short-circuits from the output to V_{CC} can cause an excessive heating if (V_{CC} +) > 15 V. The maximum output current is approximately 40 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.*
4. *This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as an input diode clamp. In addition to this diode action, there is an NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.*
5. *The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400 µA max. ($R = (V_{in} - 32\ V)/400\ µA$).*
6. *Short-circuits can cause an excessive heating and destructive dissipation. Values are typical.*
7. *Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.*
8. *Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.*
9. *Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.*

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Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	3 to 36	V
V_{icm}	Common mode input voltage range T_{amb} = 25 °C Common mode input voltage range Tmin ≤ Tamb ≤ Tmax	Vcc- to Vcc+ - 1.5 Vcc- to Vcc+ - 2	
T	Operating free-air temperature range	-40 to 125	°C

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3 Electrical characteristics

Table 3. Electrical characteristics, V_{cc}+=5 V and 36 V, V_{cc}-=0 V, V_o=1.4 V, R_L connected to ground, T=25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage(1)	T = 25 °C			4	mV
		Tmin < T < Tmax			5	
Δ_{Vio}/ ΔT	Input offset voltage drift	Tmin < T < Tmax		7	30	µV/°C
I_{io}	Input offset current	T = 25 °C			30	nA
		Tmin < T < Tmax			40	
Δ_{Iio}/ ΔT	Input offset current drift	Tmin < T < Tmax		10	300	pA/°C
I_{ib}	Input bias current(2)	T = 25 °C			150	nA
		Tmin < T < Tmax			200	
A_{vd}	Large signal voltage gain	V_{cc} = 15 V, R_L = 2 kΩ, V_o = 1.4 to 11.4 V, T = 25 °C	50	100		V/mV
		V_{cc}=15 V, R_L=2 kΩ, V_o=1.4 to 11.4 V, Tmin < T < Tmax	25			
		V_{cc} = 36 V, R_L = 2 kΩ, V_o = 1.4 to 11.4 V, T = 25 °C	50	100		
		V_{cc}=36 V, R_L=2 kΩ, V_o=1.4 to 11.4 V, Tmin < T < Tmax	25			
SVR	Supply voltage rejection ratio	V_{cc} = 5 to 36 V, V_{icm} = 0 V, T = 25 °C	65	100		dB
		V_{cc} = 5 to 36 V, V_{icm} = 0 V, Tmin < T < Tmax	65			
I_{cc}	Supply current	All amps, no load, V_{cc} = 5 V, T = 25 °C		0.45	0.6	mA
		All amps, no load, V_{cc} = 5 V, Tmin < T < Tmax			1	
		All amps, no load, V_{cc} = 36 V, T = 25 °C		0.7	1.2	
		All amps, no load, V_{cc} = 36 V, Tmin < T < Tmax			2.0	
CMR	Common-mode rejection ratio	V_{cc} = 36 V, V_{icm} = 0 to 34.5 V, T = 25 °C	70	85		dB
		V_{cc} = 36 V, Vicm = 0 to 34 V, Tmin < T < Tmax	60			
I_{source}	Output source current	V_{cc} = 36 V, V_o = 2 V, V_{id} = 1 V	25	32	40	mA
I_{sink}	Output sink current	V_{cc} = 36 V, V_o = 2 V	15	18		mA
		V_{cc} = 36 V, V_o = 0.2 V	70	94		µA
V_{oh}	High-level output voltage	V_{cc} = 36 V, R_L = 2 kΩ, T = 25 °C	32	33		V
		V_{cc} = 36 V, R_L = 2 kΩ, Tmin < T < Tmax	32			
		V_{cc} = 36 V, R_L = 10 kΩ, T = 25 °C	33	34		
		V_{cc} = 36 V, R_L = 10 kΩ, Tmin < T < Tmax	33			
V_{ol}	Low-level output voltage	V_{cc} = 5 V, R_L = 10 kΩ, T = 25 °C		5	20	mV
		V_{cc} = 5 V, R_L = 10 kΩ, Tmin < T < Tmax			20	
		V_{cc} = 36 V, R_L = 10 kΩ, T = 25 °C		5	20	
		V_{cc} = 36 V, R_L = 10 kΩ, Tmin < T < Tmax			20	

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate	V_{cc} = 15 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain, T=25 °C	0.3	0.6		V/µs
		V_{cc} = 15 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain, Tmin < T < Tmax	0.2			
		V_{cc} = 36 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_l = 100 pF, unity gain, T = 25 °C	0.5	0.75		
		V_{cc} = 36 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_l = 100 pF, unity gain, Tmin < T < Tmax	0.4			
GBP	Gain bandwidth product	V_{cc} = 36 V, f = 100 kHz, V_{in} = 10 mV, R_l = 2 kΩ, C_l = 100 pF	0.8	1.2		MHz
Vo1 / Vo2	Channel separation (3)	V_{cc} = 30 V, 1 kHz ≤ f ≤ 20 kHz		120		dB

1. *V_O = 1.4 V, 5 V ≤ V_{CC} ≤ 36 V, 0 ≤ V_{icm} ≤ V_{CC} - 1.5 V.*
2. *The direction of the input current is out of the IC. This current is essentially constant as long as the output is not saturated, so there is no change in the loading charge on the input lines.*
3. *Due to the proximity of external components, ensure that the stray capacitance does not cause coupling between these external parts. This can typically be detected at higher frequencies because this type of capacitance increases.*

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Figure 3. Supply current vs. supply voltage

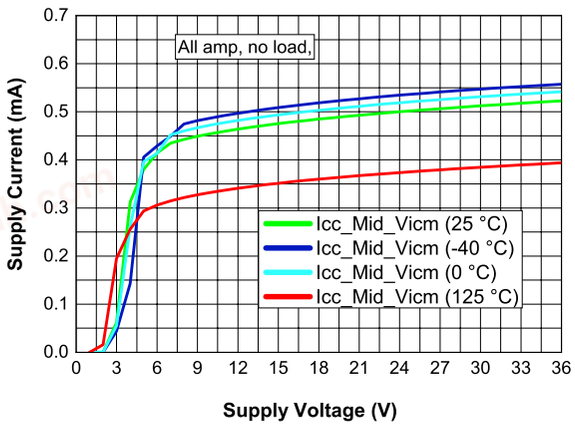


Figure 4. Offset voltage production distribution at V_{CC} = 36 V

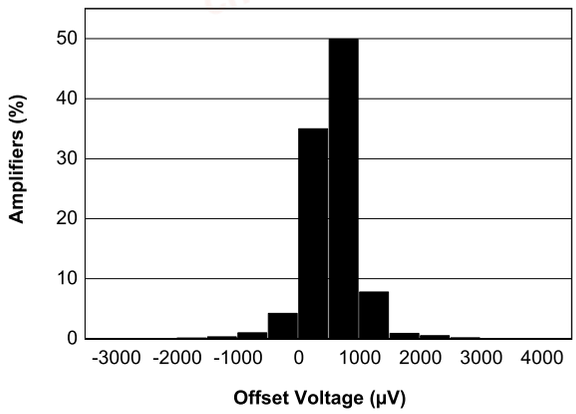


Figure 5. Input offset voltage vs. temperature at V_{CC} = 36 V

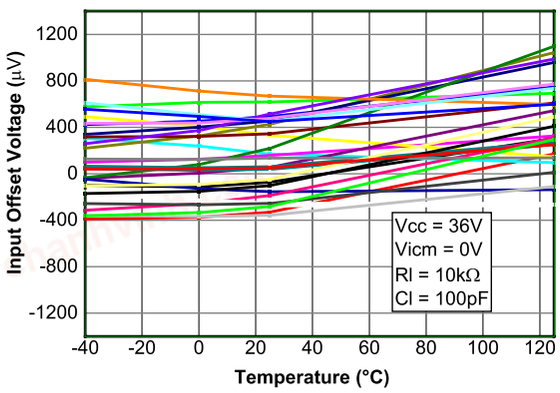


Figure 6. Input offset voltage vs. common-mode voltage at V_{CC} = 36 V

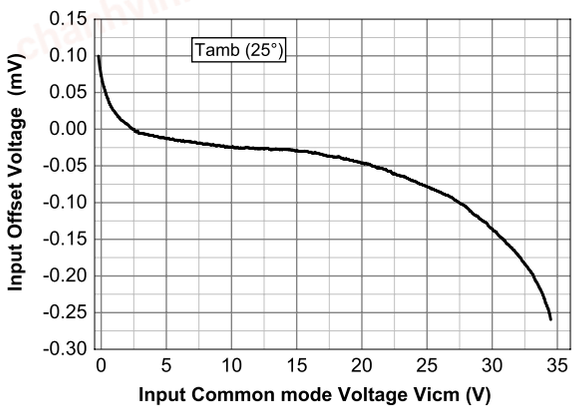


Figure 7. Input bias current vs. temperature

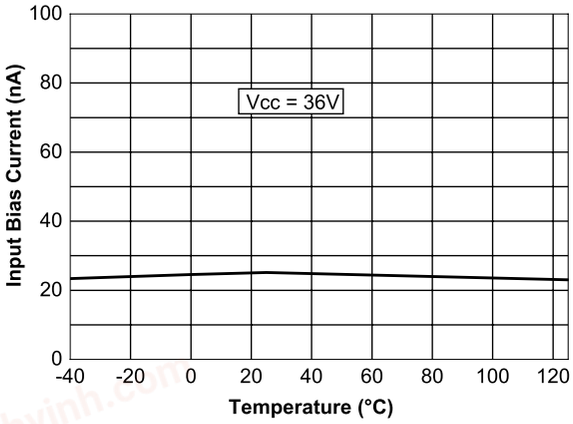
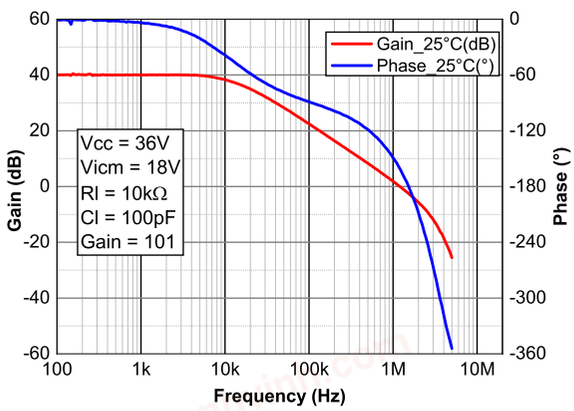


Figure 8. Gain and phase vs. freq. at V_{CC}=36 V



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Figure 9. Phase margin vs. capacitive load at V_{CC}=36 V

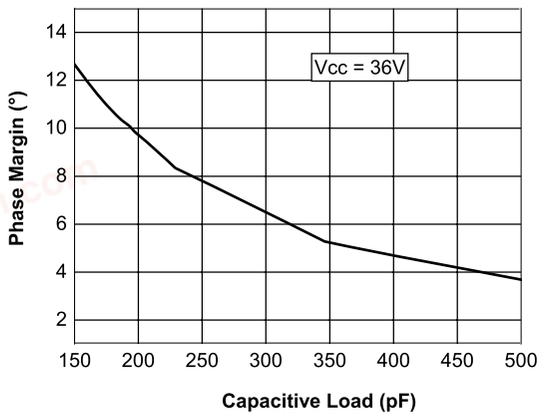


Figure 10. Overshoot vs. capacitive load at V_{CC}=36V

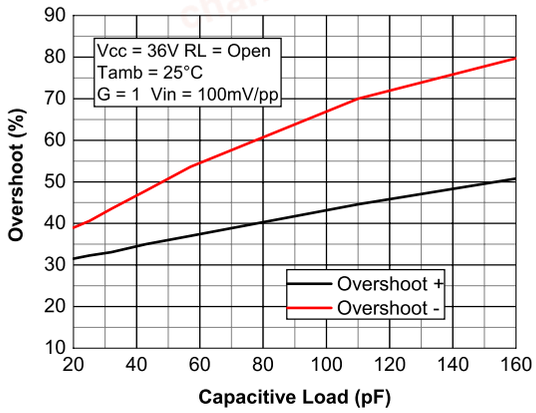


Figure 11. Output voltage vs. output current (sinking)

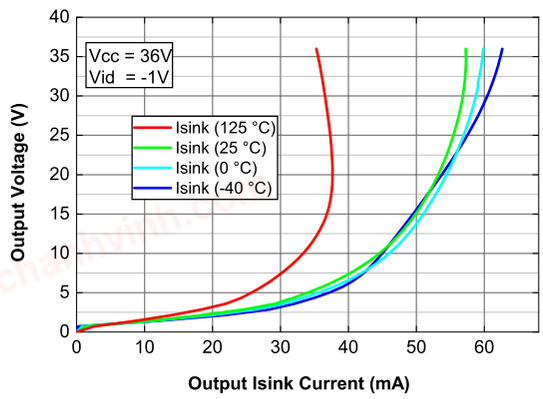


Figure 12. Output voltage vs. output current (sourcing)

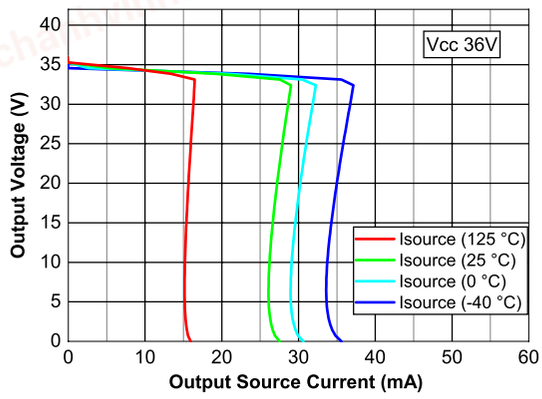


Figure 13. Current limiting vs. temperature

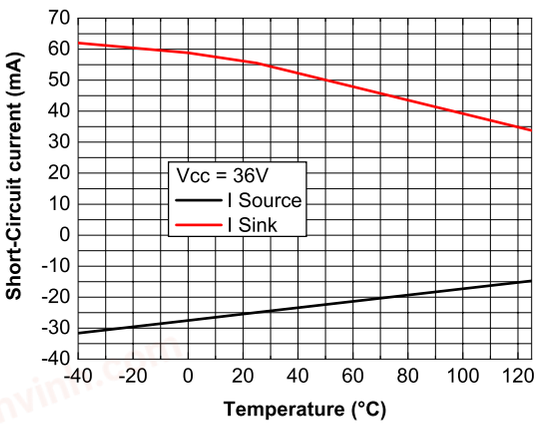
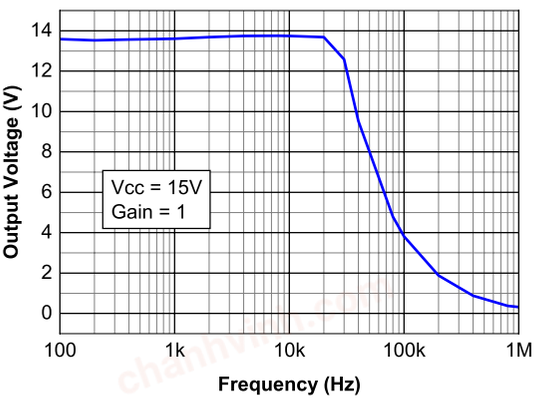


Figure 14. Maximum output voltage vs. frequency at V_{CC} = 15 V



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Figure 15. Slew rate behavior at V_{CC} = 36 V

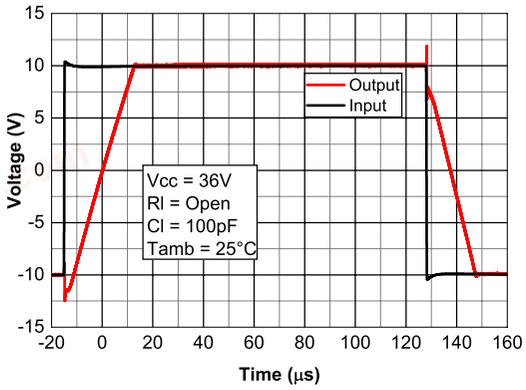


Figure 16. Slew rate behavior vs. temperature at V_{CC} = 36 V

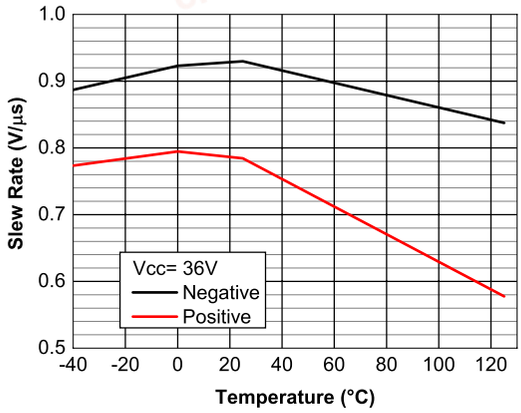


Figure 17. Common-mode rejection ratio and power supply rejection ratio at V_{CC} = 5 V

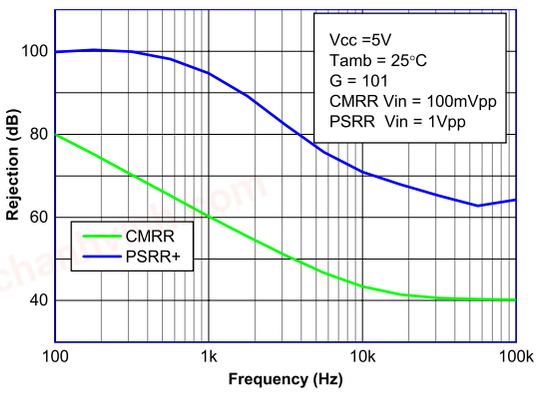


Figure 18. Noise vs. frequency at V_{CC} = 36 V

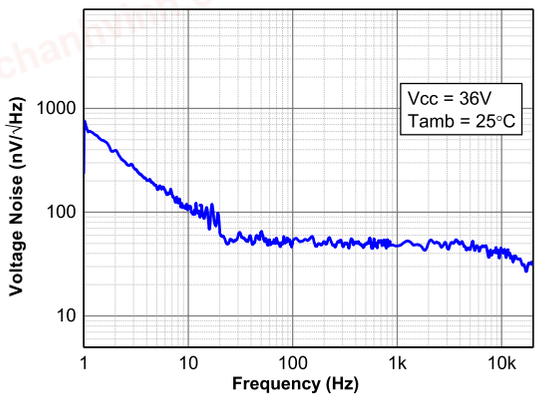


Figure 19. THD + N vs. voltage at V_{CC} = 36 V

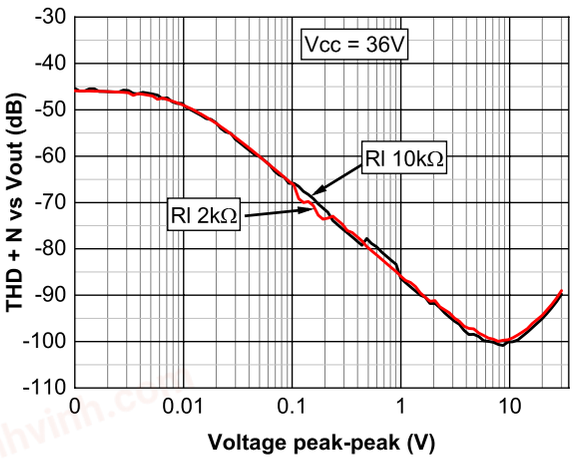
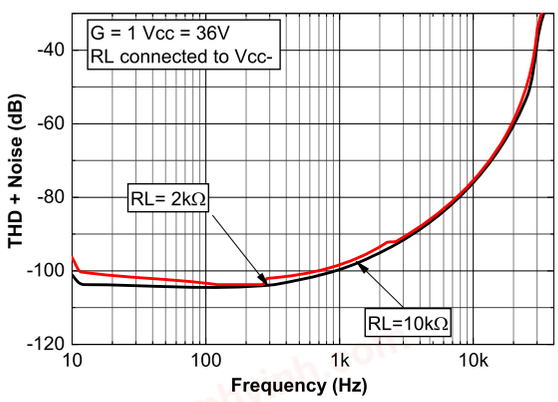
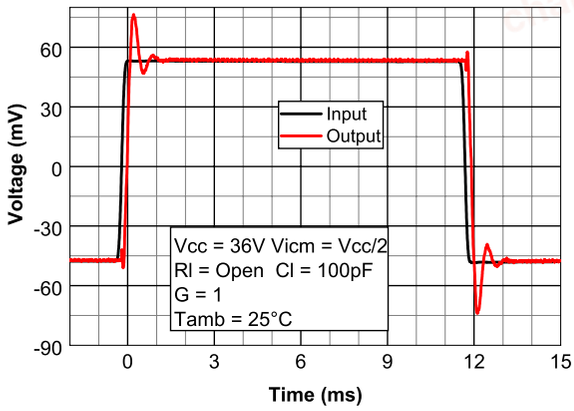


Figure 20. THD + N vs. frequency at V_{CC} = 36 V



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Figure 21. **Small-signal step response vs. time at V_{CC} = 36 V**



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 MiniSO8 package information

Figure 22. MiniSO8 package outline

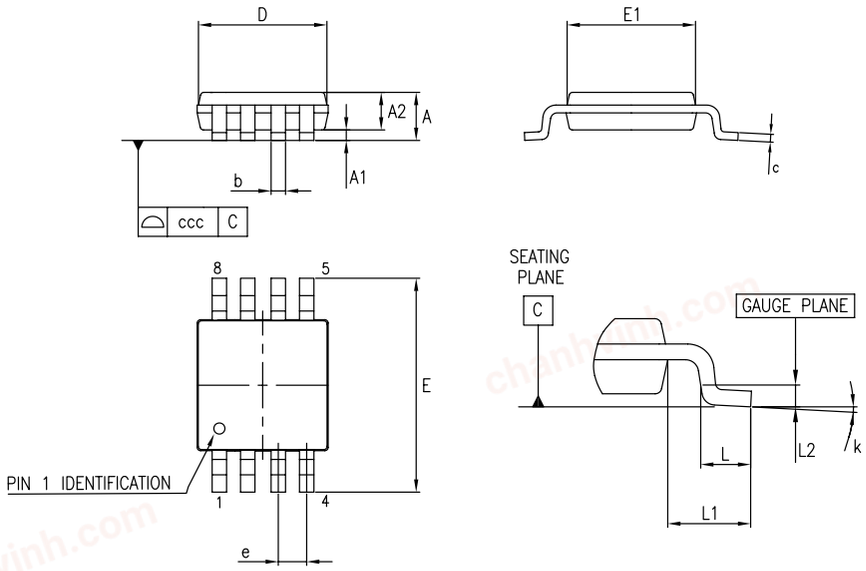


Table 4. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

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5 Ordering information

Table 5. Ordering information

Order code	Temperature range	Package	Packaging	Marking
LM2904BYST (1)	-40 to +125°C	MiniSO8	Tape and reel	K2F

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.*

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Revision history

Table 6. **Document revision history**

Date	Version	Changes
09-Dec-2020	1	Initial release.
15-Dec-2020	2	Updated Table 3. Electrical characteristics, V_{CC}+=5 V and 36 V, V_{CC}-=0 V, V_O=1.4 V, R_L connected to ground, T=25 °C (unless otherwise specified).

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