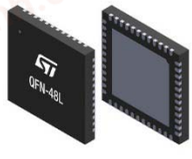
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L99LDLH32

32-channel LED driver with automotive CAN FD Light interface

Datasheet - production data



QFN48L 7x7

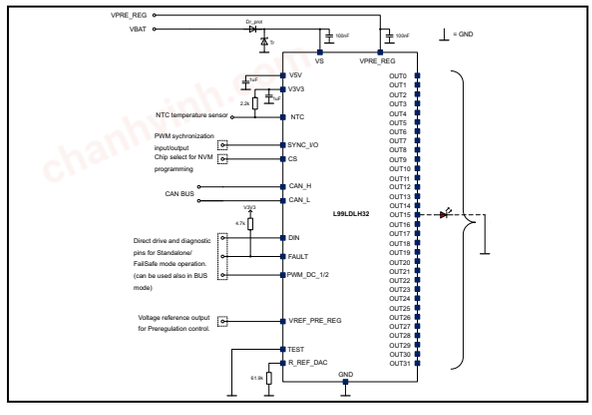
Features

- AEC-Q100 qualified
- General
  - CAN FD Light compatible Serial Interface, Protocol Handler, Draft Specification Proposal (DSP) available from CAN in Automation (CiA)
  - High precision oscillator integrated, no external quartz required
  - QFN48L 7x7 with exposed pad
  - Timeout watchdog with Limp Home
  - Low standby current
  - Stand Alone/Fail Safe and Bus mode operation
  - Direct drive (1 Direct Input), for 1 function group supporting ASIL requirements
  - Widest configurability by embedded non-volatile and volatile memories
  - Operating supply voltage range 5.5 V – 40 V
- Linear Regulators section
  - Operating temperature range - 40°C – 150°C
  - 32 constant current output channels, high side configuration
  - Output current from 1 mA to 15 mA, parallelable outputs
  - Output voltage up to 35 V
  - Feedback voltage to external pre-regulator, to optimize the regulation voltage minimizing overall power dissipation
  - Current setting per channel by 8-bit DAC
  - Analogue dimming, 8-bit PWM channel individual exponential brightness control and 8-bit global PWM dimming
  - Programmable PWM frequency
  - Slow turn on/off time, gradual outputs delay and dithered clock, for better EMC performances
- Protection and diagnostic
  - Integrated 8-bit ADC, for full and flexible diagnostic
  - 1 dedicated line for fault bus
  - Temperature warning (1 threshold)
  - Over-temperature shutdown
  - Short circuit and open load detection and protection
  - Automatic LED current derating, through external NTC measurement and device junction temperature (T_J)

Applications

- Automotive OLED Rear Lighting
- Automotive Ambient Lighting

Figure 1. Simplified application schematic



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1 Description

The L99LDLH32 is a monolithic 32-channel linear current regulator specifically designed for automotive exterior O/LED rear lighting applications. Thanks to the high side configuration of the output channels, the L99LDLH32 is suitable to drive OLED panel with common cathode. It guarantees up to 35 V output driving capability - to cover the OLED forward voltage wide spread - and features 32 regulated current sources able to provide from 1 mA up to 15 mA individually programmable current to drive each pixel of the OLED panel independently. As the other device in the family (L99LDLL16), the L99LDLH32 integrates a robust purely automotive CAN FD Light compatible communication interface which allows a high rate data transmission (up to 1 Mbit/s) and uses CAN FD structure for long frames. Besides the CAN FD Light compatible physical layer, the device also integrates the protocol handler, so no additional external devices are needed to facilitate communication with Commander ECU. The L99LDLH32 can operate in bus mode using CAN FD Light compatible interface or in stand-alone/fail-safe mode using internal Few Time Programmable (FTP) memory registers.

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2 Introduction

The L99LDLH32 is a monolithic 32-channel driver specifically designed for automotive O/LED lighting applications.

The device offers a high level of flexibility, thanks to its programmability through CAN FD Light compatible communication interface. This feature supports generic platform approaches, which require a software configurability of several parameters.

This differential robust interface offers a detailed diagnostic of the device itself - as well as of the controlled O/LED panel's pixel - and makes the device suitable for high data rate transmission, up to 1Mbit/s.

This device can operate in bus mode using CAN FD Light compatible interface or in stand-alone / fail-safe mode using internal few time programmable (FTP) memory registers.

As the device potentially controls safety critical functions such as tail light and turn indicators, built-in features are integrated in order to support a high level of functional safety on application level. The L99LDLH32 features a programmable timeout watchdog, a monitoring of the watchdog counter, a Limp Home (fail safe) function and 1 direct input.

Supplied directly from car battery, the L99LDLH32 guarantees up to 35 V output driving capability and features 32 regulated current sources able to provide from 1 mA up to 15 mA programmable current to drive each pixel of the O/LED panels. The current can be individually programmed using an integrated 8-bit DAC.

Each O/LED pixel can be supplied through one pre-regulator connected between battery and the integrated current source. The pre-regulated (as well as the battery) voltages are internally monitored by an 8-bit ADC, the results are stored in a dedicated result register.

The brightness can be adjusted separately for each channel through an 8-bit PWM exponential dimming control. An 8-bit linear global dimming can be superimposed to each channel individual PWM. A slow turn-on and turn-off time improves the system low noise generation performances.

The device supports control of up to 2 individual lighting functions. Each channel can be mapped or not mapped to the direct input as well as through the pre-regulated external supply voltages. This feature ensures the highest flexibility to control different lighting functions composed of different O/LED types, currents and string lengths.

Thanks to integrated high precision oscillators the device generates all relevant timing functions such as PWM frequency, duty cycle, trigger points for ADC conversion, phase shift, etc. autonomously. No external timers are required.

In the L99LDLH32, thanks to the integration of an 8-bit ADC, a complete diagnostic is also available: open load detection, short to ground detection.

Diagnostic thresholds are freely configurable for each function group. Moreover the user can configure the desired device reaction to detected faults, ensuring maximum flexibility for the application and sophisticated auto-recovery strategies.

The device features also the output gradual delay which avoids contemporary turning on of all the channels used for a specific light function, reducing the inrush current. To further improve EMI performances, the device implements an internal clock dithering to have a spread spectrum noise reduction.

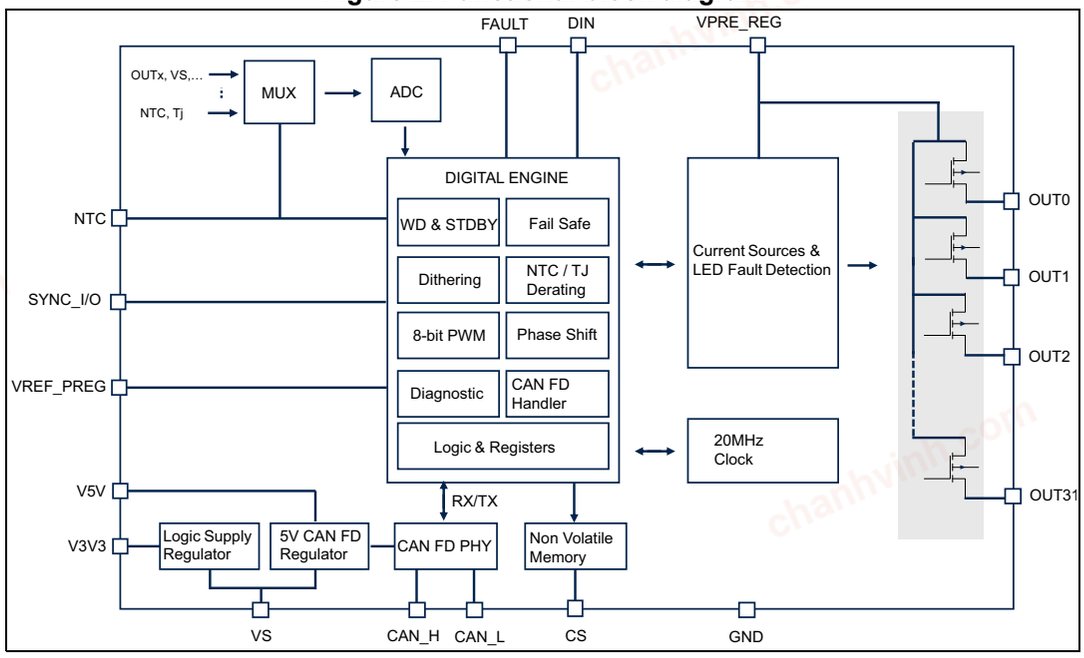
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Thermal management is equipped with thermal warning (TW) and outputs thermal shutdown (TSD). The device performs an automatic thermal derating based on external NTC measurement as well on device junction temperature (T_J).

The supply voltage range is between V_{S_MIN} and 40 V avoiding any additional load dump protection on power supply stage.

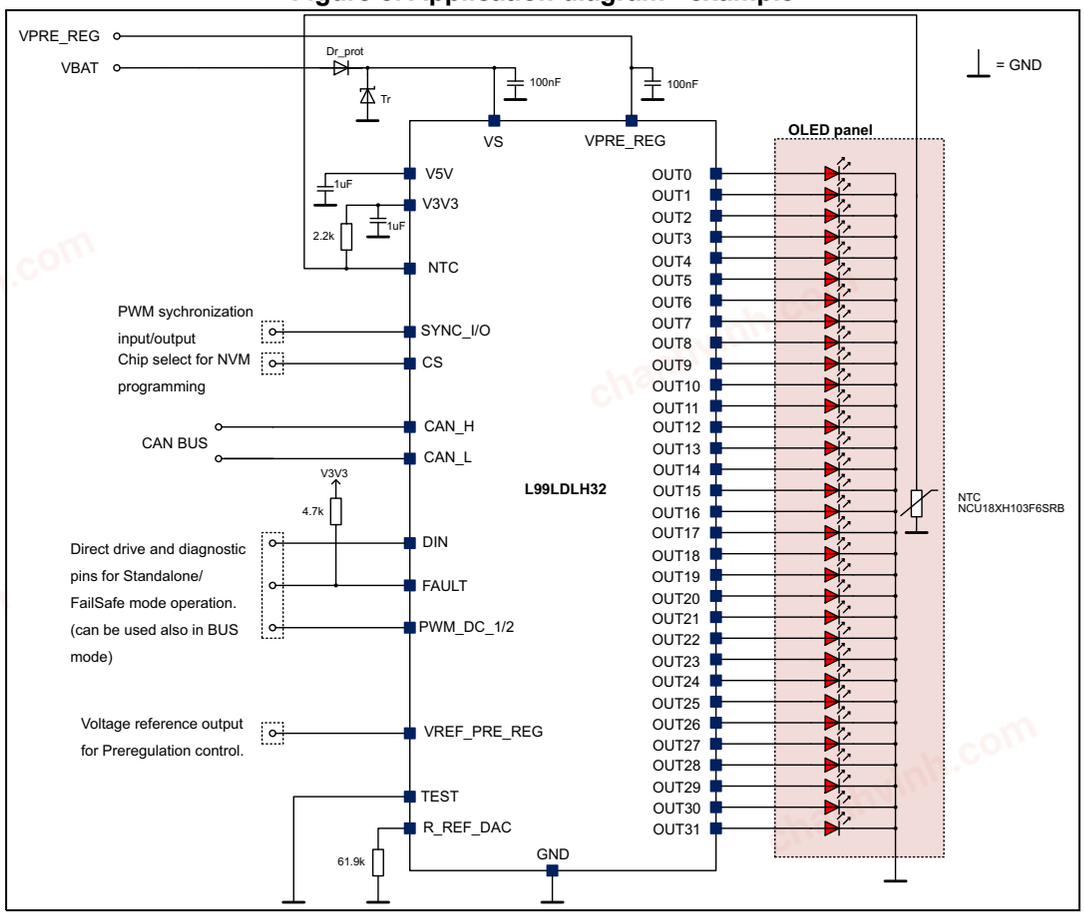
2.1 Device information

Figure 2. Functional block diagram



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Figure 3. Application diagram - example



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Figure 4. QFN48L 7x7 connection diagram

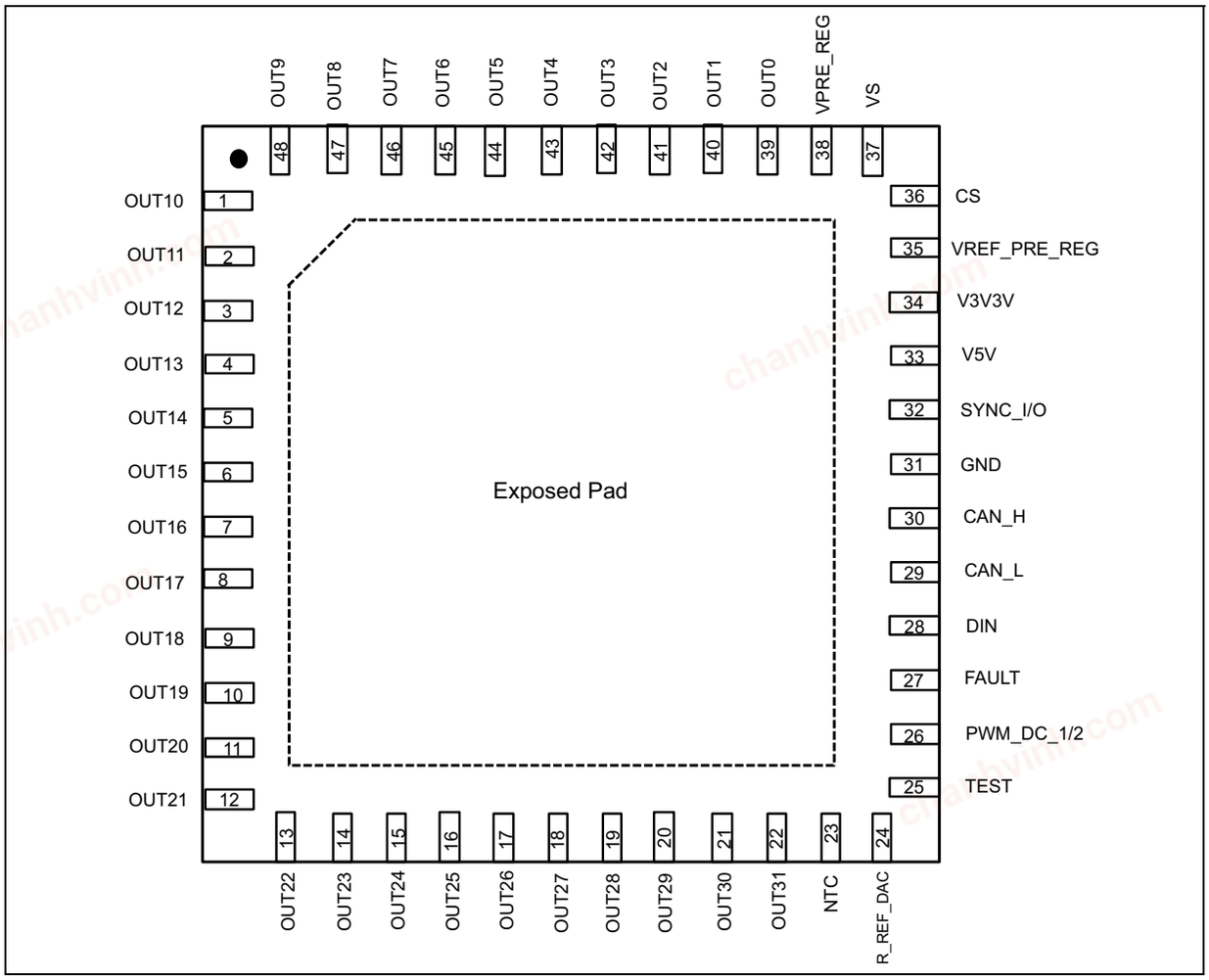


Table 1. Pin list description

Pin #	Name	Description
1÷22, 39÷48	OUTx	Output Pin for 32-channels – High Side configuration
38	VPRE_REG	1 pin for connection to external pre-regulator.
37	VS	Input supply pin of the IC. Connect VS to the car battery voltage. Must be reverse protected (external diode). Input supply for the 3.3 V and 5 V internal linear voltage regulators.
36	CS	Chip Select input (test and programming mode entering)
35	VREF_PRE_REG	1 analog feedback voltage output pin. (provided as reference for VPRE_REG external Pre-regulator)
34	V3V3	3.3 V Regulator Output Voltage (Logic and I/O). Connect a low ESR capacitor (1 µF) close to this pin.
33	V5V	5 V Regulator Output Voltage (Communication interface supply). Connect a low ESR capacitor (1 µF) close to this pin.

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Table 1. Pin list description (continued)

Pin #	Name	Description
32	SYNC_I/O	Synchronization input/output pin - floating when not used. (for PWM synchronization between several devices)
31	GND	Ground connection.
30	CAN_H	CAN bus high level voltage I/O
29	CAN_L	CAN bus low level voltage I/O
28	DIN	Direct Input pin
27	FAULT	I/O pin for diagnostic. (1 Fault pin used for diagnostic)
26	PWM_DC_1/2	PWM DC setting pin (To select between two different PWM duty cycle setting, when internal PWM dimming in standalone mode is enabled).
25	TEST	Internal use only. To be connected to GND.
24	R_REF_DAC	External resistor for DACs current reference It is suggested to use E96 series, 61.9 kΩ (1% tolerance standard thin film resistance, +/- 0.7%, 100 ppm/K, temperature spread in the range [-40÷100]°C)
23	NTC	NTC pin for LEDs thermal control Connect an external NTC resistor (see *Table 78*)
-	EP	Exposed Pad - suggested to connect to GND board plane, for better thermal dissipation

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3 Device supply concept

The L99LDLH32 IC is supplied through VS pin, connected to the car battery through an external diode for reverse polarity protection or to an external pre-regulator.

The supply voltage is in the range of [V_{S_MIN}÷40] V, avoiding any additional load dump protection on power supply stage. On top of that, no device reset will occur in the supply voltage range of [3÷V_{S_MIN}] V – to keep digital content during cold cranking pulse.

In that range – [3÷V_{S_MIN}] V - and till POR threshold ($V_{3V3_POR_H}$) is not reached, full device protection is granted and digital part (register content and state machine) is kept alive.

An under-voltage threshold (V_{S_UV}) is implemented to avoid wrong output current due to low battery and, till device leaves the voltage range between under-voltage V_{S_UV} and under-voltage reset $V_{S_UV_RST}$ some parameters may deviate versus specified value.

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4 Linear current sources

4.1 General description

The L99LDLH32 features 32 high side linear current generators to regulate from 1 mA up to 15 mA current on the output channels.

The output channels can be put in parallel to address higher current than the programmable one and, for each channel, the current can be individually programmed by using an integrated 8-bit DAC. The output channels paralleling is allowed, provided that all these channels are controlled simultaneously. Moreover, in case of fault on one of the paralleled channels, it is recommended to deactivate all the channels belonging to the same fault bus (by setting FAULT_REACT_MODE bit to "0", see *Table 8*).

Supplied directly from car battery, the L99LDLH32 IC guarantees up to 35 V output driving capability - suitable to cover the OLED forward voltage wide spread.

Each O/LED string can be supplied by battery or through one pre-regulator connected between battery and linear current regulators.

The pre-regulated (V_{PRE_REG}) and battery (V_S) voltages are internally monitored by an 8-bit ADC, the results are stored in a dedicated result register. The ADC is used also to monitor the device temperature (T_J) as well as all the output channels. These channels are refreshed once per PWM period in on-state.

The minimum PWM on-time (vs PWM frequency) - to ensure a correct channel ADC reading - is $t_{PWM_ON_OFF}$ time (see *Table 77*). In any case, ADC will not perform any reading operation before a configurable blanking time (t_{DIAG_BLANK}, see *Table 79*) has elapsed. This blanking time is applied on the first channel turn on as well as on each PWM rising edge.

The ADC monitoring of all these parameters allows a complete diagnostic: open load detection, hard short circuit (versus ground), O/LED current derating in case of device temperature increasing.

The L99LDLH32 features an 8-bit logarithmic PWM for dimming control to adjust separately the brightness for each channel. A linear 8-bit global dimming dedicated for each function group mapped with Direct Input pin can be superimposed with the channel individual dimming.

A slow turn-on and turn-off time (t_{SR_ON} and t_{SR_OFF}) of the channel improves the system low noise generation performances.

Moreover, this device features the output gradual delay (t_{GD}) which avoids contemporary turning on of all the channels used for a specific light function, reducing the inrush current.

To further improve EMI performances, the device implements an internal clock dithering: more precisely, a triangular waveform (see the *Figure 57*) is applied to the embedded 20 MHz oscillator to have a spread spectrum noise reduction. Frequency modulation and deviation, along with rejection, are showed in the *Table 39*, for each of the eight possible configurations the user can set by means of 3 dedicated bits (DITHERING [2÷0], see FTP/RAM memory map, *Chapter 7*).

The L99LDLH32 integrates a thermal sensor block used to sense the device junction temperature (T_J) as well as to detect thermal warning (TW) and thermal shutdown (TSD) thresholds, granting device protection in case of temperature increasing.

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The sensed junction temperature (T_J) is monitored by an 8-bit ADC with the aim of starting an automatic, downwards derating of the LED string current as soon as the T_{TW} - T_{TW_HYS} threshold is reached. The derating ends when the 50% of the nominal LED current is reached, which corresponds to T_J = 165°C.

The 8-bit ADC is also used to monitor the voltage on the NTC pin, where an external resistor can be connected. If the monitored voltage – whose value depends on the temperature detected by the NTC resistor itself - reaches the V_{NTC_TH} threshold (programmable by 3 bits, see *Table 78*), a downwards derating of the LED string current automatically starts, till 50% of the nominal LED current is reached. This corresponds to a NTC temperature 20°C higher than the one corresponding to V_{NTC_TH}.

The monitoring of both T_J and NTC voltage is contemporarily active.

The device can be controlled by a microcontroller via CAN FD Light compatible interface. Stand-alone operation (no microcontroller used) is also possible thanks to direct drive functionality and full configurability by FTP, which can be programmed (up to N_{FTP} cycles) in application via CAN FD Light compatible interface. To avoid unintentional writing, there is the possibility to lock any FTP area.

4.2 Channel current setting

The L99LDLH32 features 32 high side linear current generators to regulate from 1 mA up to 15 mA current on the output LED strings. The current can be individually programmed per channel through the 8-bit DAC (CURR_SET_CHx - see FTP/RAM memory map, *Chapter 7*)

The output channels can be put in parallel to address higher current than the programmable one.

Moreover, the value programmed in the 8-bit DAC per channel is stored in the RAM and can be reconfigured dynamically in Bus/Normal mode.

4.3 Channel driver drop-out voltage

To guarantee the regulation of the programmed channel current, a minimum output voltage (V_{OUTx_DROP}) across each current generator must be ensured.

The *Table 2* shows the minimum channel V_{OUTx_DROP} at the boundary of regulation region (output current is 3% less than the target value, output power MOS already in triode region). These measurements refer to only one output ON (if more channels are contemporary on, the drop voltage increases).

If on one hand a lower than minimum recommended V_{OUTx_DROP} leads to a regulated current lower than the expected one, a too high V_{OUTx_DROP} implies too high power dissipation.

To guarantee the current regulation and to optimize the power dissipation on each channel, in case of maximum current set on one channel and Tj at 125°C (worst case condition), the minimum output voltage drop (from device V_{PRE_REG} to device OUTx) is 1.05 V.

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Table 2. Minimum channel drop-out voltage at max current vs T_J

T_J [°C]	V_{OUTx_DROP} [V]
125	1.05
25	1
-40	0.95

The L99LDLH32 features one analog pin ($V_{REF_PRE_REG}$) providing a voltage proportional to the maximum output voltage of active channels plus the required drop voltage across the current regulator required for proper regulation (~1.4 V). This signal can be used in combination with an analogue discrete circuit to close directly the feedback loop with an external DC/DC converter.

For applications with a common DC/DC converter for several L99LDLH32 devices, the $V_{REF_PRE_REG}$ output signal is buffered, therefore, it can be combined in wired-OR with $V_{REF_PREG_REG}$ output signals from other devices to make sure only the highest reference voltage is fed back to the external DC/DC converter.

A dedicated Application Note is available for more information on this feature and how to use in application.

4.4 Channel output gradual delay

The L99LDLH32 features the output gradual delay, which consists in gradual turning on of the current generators. In case of driving several outputs simultaneously, the output gradual delay is applied in order to lower the current transients and improve device emissions. This feature can be activated – for all the channels - through one dedicated bit (OUT_DELAY, see FTP/RAM memory map, *Chapter 7*).

In case one or more channels are not enabled, gradual delay is increased according to the number of channels turned OFF.

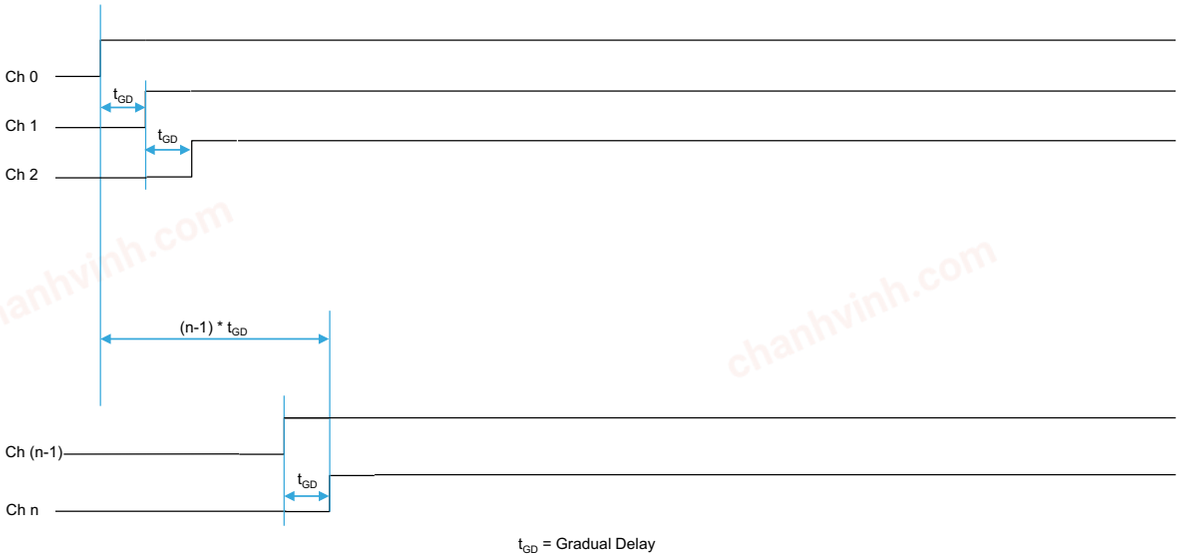
The Gradual Delay concept is valid in PWM mode as well: in this case, the PWM waveform is shifted and the gradual delay is applied also when channel is turned OFF.

The output gradual delay feature is valid both for Normal / Bus mode and Fail Safe / Stand Alone Mode. In this latter case, Direct Input (DIN) controls output channels as per FTP setting (DIN_MAP_CHx, 1bit - see FTP/RAM memory map, *Chapter 7*): it is suggested to apply the output gradual feature if minimum PWM on time is ≥ 20 µs. Otherwise, it is suggested to disable the feature by the dedicated bit.

The delay between each output is showed in *Figure 5*.

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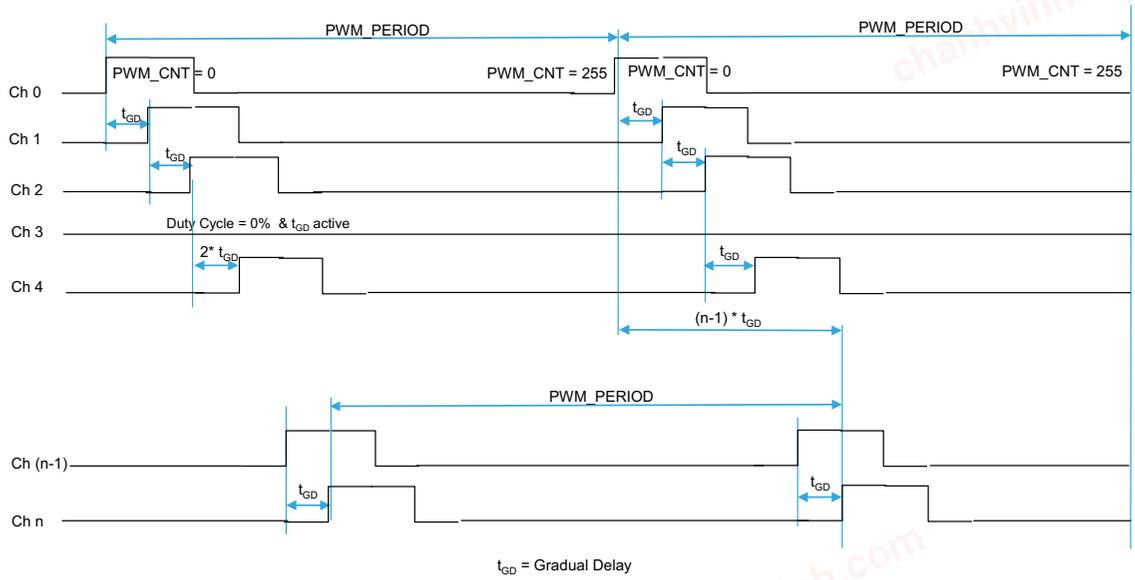
Figure 5. Gradual delay concept



t_{GD} = Gradual Delay

n = Channel number

Conditions: Duty_Cycle = 10% & t_{GD} active - behavior valid for any 0% < Duty Cycle < 100%)



t_{GD} = Gradual Delay

n = Channel number

PWM_CNT = PWM counter

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5 Functional description

5.1 Operating modes

The L99LDLH32 features different operating modes. The related device states are reported in *Figure 6* and well detailed in the following sub-chapters.

There are 2 bits for safe transition between different modes: BUSMODE and GOSTBY configuration bits (see RAM memory map, *Chapter 7*) are used to set, leave and check device Normal / Bus operating mode.

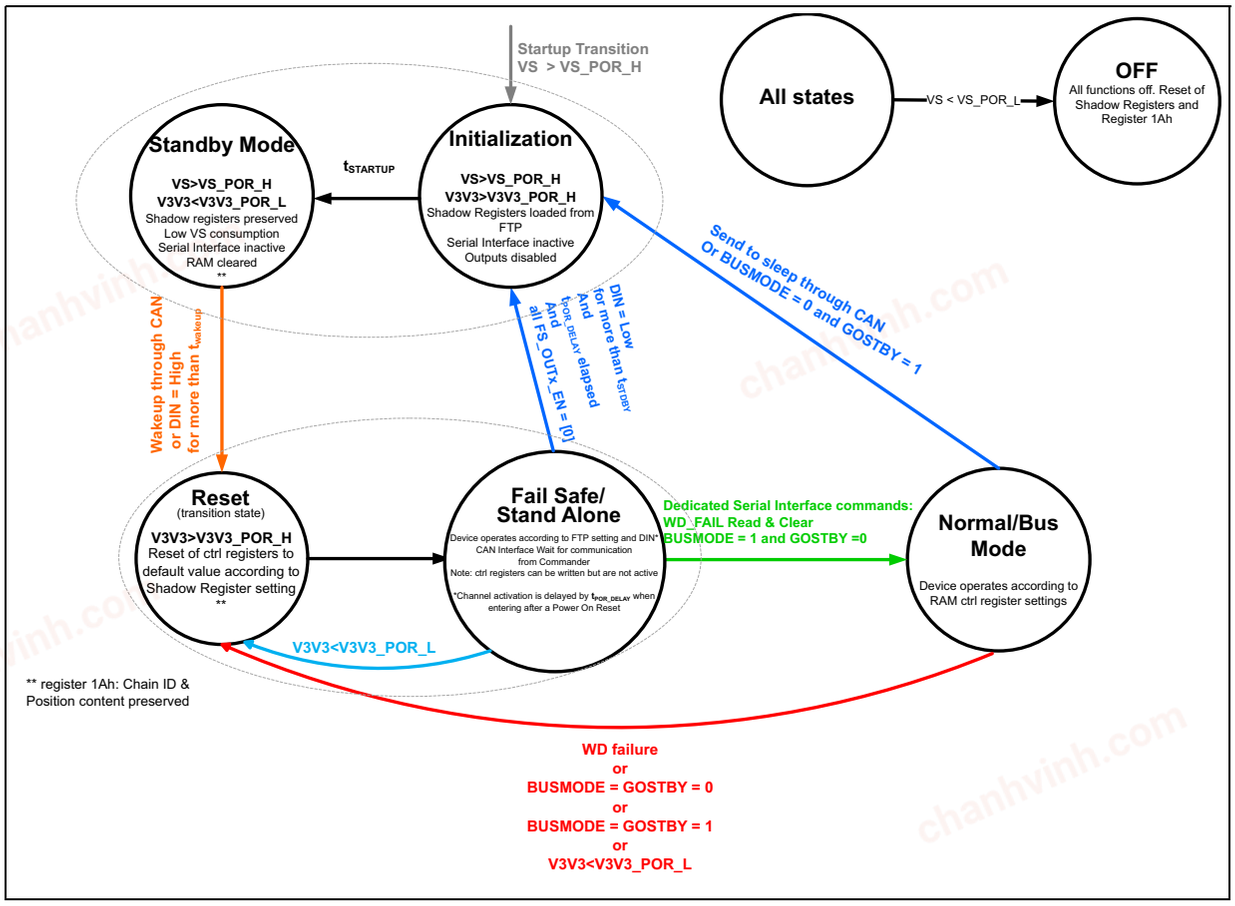
A dedicated pattern through CAN FD Light compatible interface is used to wake-up and to sleep the device. On top of that, device can be opportunely woken up or sent to sleep also through DIN pin as well as through BUSMODE / GOSTBY bits respectively.

As the device potentially controls safety critical functions such as tail light and turn indicators, built-in features are integrated to support a high level of functional safety on application level. The L99LDLH32 features a programmable timeout watchdog by WD_CONF (2 bits - see FTP/RAM memory map, *Chapter 7*), a monitoring of the watchdog counter by WD_STATUS (2 bits - see RAM memory map, *Chapter 7*), a Fail Safe and a Direct Input mode.

To keep the device in Normal / Bus mode, a watchdog trigger bit (WD_TRIG<0> - see RAM memory map, *Chapter 7*) is cyclically toggled within the programmable watchdog timeout period. In case of watchdog failure, the WD_FAIL bit (see RAM memory map, *Chapter 7*) is set and the device leaves Normal/Bus mode operation to enter Fail Safe mode.

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Figure 6. Device state diagram



Note: Partial networking feature is not supported by the device. Mixed state on the bus has to be avoided. In case devices are sent to initialization / stand by mode NOT through a broadcast "send to sleep" command, the first UNICAST response frame of the device after wakeup has to be ignored.

5.1.1 Stand-by mode

The pre-requisite for this mode is:

- Device in initialization phase

The device enters Standby mode under the following condition:

- By default, once the device is powered (V_S present) and leaves initialization phase ($V_S > V_{S_POR_H}$)

The Standby mode characteristics are:

- Shadow register [(a)] preserved
- RAM cleared
- $V_S > V_{S_POR_H}$
- $V_{3V3} < V_{3V3_POR_L}$
- V_S low consumption
- CAN FD Light compatible Interface inactive

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The device leaves this mode if:

- Wake-up pattern is sent through CAN FD Light compatible interface

Or

- DIN High for a time t > t_{WAKEUP}

5.1.2 Initialization

The device enters Initialization phase under the following conditions:

- Sleep pattern sent through CAN FD Light compatible interface

Or

- One frame setting bit (BUSMODE,GOSTBY) = (0,1)

Or

- DIN Low for a time t > t_{STDBY} AND power on reset delay time (t_{POR_DELAY}) elapsed AND channels NOT set permanently ON in Fail Safe (FS_OUT_ENx [0])

The Initialization mode characteristics are:

- $V_S > V_{S_POR_H}$
- $V_{3V3} > V_{3V3_POR_H}$
- Shadow register[a] loaded from FTP
- Outputs disabled
- CAN FD Light compatible Interface inactive

The device leaves automatically Initialization mode entering Standby mode after $t_{STARTUP}$.

5.1.3 Reset mode

The device enters Reset mode (transition state) under the following conditions:

- By default, once the device leaves Standby mode
- If device state is in Fail Safe / Stand Alone mode, when $V_{3V3} < V_{3V3_POR_L}$
- If device state is Normal / Bus mode, when one of the following events occur:
  - Watchdog failure
  - One frame setting bits (BUSMODE,GOSTBY) = (0,0)
  - One frame setting bits (BUSMODE,GOSTBY) = (1,1)
  - $V_{3V3} < V_{3V3_POR_L}$

The Reset mode characteristics are:

- $V_{3V3} > V_{3V3_POR_H}$
- Reset of control register to default values according to the shadow register setting
- CAN FD Light compatible Interface inactive

The device leaves automatically Reset mode and enters Limp Home after 400 ns (typically).

a. Shadow registers are RAM copy of FTP registers, added to speed-up transition between Standby to Fail Safe modes and Fail Safe to Normal modes.

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5.1.4 Fail Safe / Stand Alone mode

The device enters Fail Safe / Stand Alone mode automatically 400 ns (typically) after Reset mode.

Fail Safe / Stand Alone mode characteristics are:

- Device operates according to FTP setting and Direct Input
- CAN FD Light compatible Interface wait for communication from Commander

Note: Control registers can be written but are not active

When the device leaves this mode, it can enter Standby or Normal/Bus mode.

If the device receives the following two frames:

- The first frame reads and clears the WD_FAIL bit (bit <15>, *Device status register #3*)
- The second frame (not necessarily directly consecutive to the first frame) sets BUSMODE = 1 and GOSTBY = 0 (bit <0-1>, *Device configuration register #4*) the device enters Bus mode.

If WD_FAIL Read & Clear operation is not performed (and in case of WD_FAIL = 1) device state will remain in fail safe but control register will be reset to default value.

Upon the condition:

- DIN Low for a time t > t_{STDBY} AND power on reset delay time (t_{POR_DELAY}) elapsed AND all channels NOT set permanently ON in Fail Safe (all FS_OUT_ENx bits = [0])

the device enters Standby mode.

Upon the condition:

- $V_{3V3} < V_{3V3_POR_L}$

the device enters Reset transition mode:

- RAM content is reloaded with shadow register content
- device will remain in FAILSAFE state with GSB.RSTB = 1, to inform the user about any potential write operations already performed in Fail Safe hast to be repeated.

5.1.5 Normal / Bus mode

The device enters the Normal / Bus mode if the device receives the following frames:

- The first frame reads and clears the WD_FAIL bit (bit <15>, *Device status register #3*)
- The second frame sets BUSMODE =1 and GOSTBY = 0 (bit <0-1>, *Device configuration register #4*)

If WD_FAIL Read & Clear operation is not performed (and in case of WD_FAIL = 1) device state will remain in fail safe but control register will be reset to default value.

In this mode the device operates according to its RAM register settings. Direct Input access can be Enabled/Disabled by a dedicated bit on DIN pin (DIN_EN - see RAM memory map, *Chapter 7*). In order to maintain the device in Normal / Bus mode the watchdog toggle bit has to be refreshed within the watchdog timeout time-frame.

The device leaves Normal / Bus mode, entering initialization state (to refresh shadow register with FTP configuration), upon the following conditions:

- Send-To-Sleep pattern is sent through CAN FD Light compatible interface

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or

- BUSMODE =0 and GOSTBY =1

The device leaves Normal / Bus mode, entering reset transition state, upon the following conditions:

- Watchdog failure
- One frame setting bits (BUSMODE,GOSTBY) = (0,0)
- One frame setting bits (BUSMODE,GOSTBY) = (1,1)
- $V_{3V3} < V_{3V3_POR_L}$:
  - RAM content reloaded with shadow register content.
  - Device will reach FAILSAFE state with GSB.RSTB = 1 – to inform the application about the reason of this transition.

5.2 Programmable functions

5.2.1 Direct drive and functional configuration

Output channels assignment

The L99LDLH32 features 1 Direct Input pin (DIN).

Each output can be assigned to DIN or to none by 1 dedicated FTP bit (DIN_MAP_CHx - see FTP/RAM memory map, *Chapter 7*) per output channel, as showed in *Table 3*.

Table 3. Output channel assignment to DIN

DIN_MAP_CHx <0>	Output channel status
0	OUTx NOT mapped
1	OUTx mapped on DIN

In Fail Safe / Stand Alone mode, the outputs are always controlled by DIN - according to the assignment defined in *Table 3* - except the case when the channel is programmed permanently ON by dedicated FTP bits (FS_OUT_ENx<0>- see FTP/RAM memory map, *Chapter 7*). When this bit is set, the related output channel “x” is permanently active in Fail Safe / Stand Alone mode regardless of the DIN – see *Table 4*.

Table 4. Output channel in Fail Safe / Stand Alone mode

FS_OUT_ENx <0>	Output Channel Status
0	OUTx according to DIN_MAP_CHx <0>
1	OUTx permanently ON

In case the channel is configured ON in Fail Safe / Stand Alone mode, a configurable delay of the output activation after power on reset (t_{POR_DELAY}) prevents any undesired flashing while configuring the devices and entering Normal / Bus mode. In other words, after power on reset, all outputs are kept off till power on reset delay time elapses to prevent any flashing during the time needed to enter in Bus mode operation.

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In Normal / Bus mode, the direct input access to outputs can be enabled /disabled for each channel. If enabled (DIN_EN), bus control is applied when DIN = 0. If DIN is set (DC or PWM) the bus control is automatically disabled (after elapsing of t_{FILTER}) and overtaken by DIN (the direct input has priority versus Bus control). Bus control is re-established upon $t_{BUS_CONTROL}$ elapse after last falling edge on DIN.

For DIN, a read-back information is available. It is forecasted one status bit (DIN_STATUS<0> - see RAM memory map, *Chapter 7*) to support functional safety.

The L99LDLH32 features also 1 V_{PRE_REG} pin, to supply the current sources through an external pre-regulator.

5.2.2 PWM operation

In the L99LDLH32, the brightness of LED strings can be modified by PWM.

The PWM dimming could be performed in different ways:

- Through serial bus
- Through direct input
- Through power line

When PWM operation is managed through the serial bus, there are 3 bits (PWM_FREQ_DINx, see FTP/RAM memory map, *Chapter 7*) to configure the PWM frequency of the channels.

The PWM frequency range is reported in the below table.

Table 5. PWM frequency range

PWM_FREQ_DINx [2÷0]			PWM_FREQ [Hz]
bit 2	bit 1	bit 0	
0	0	0	200
0	0	1	300
0	1	0	400
0	1	1	500
1	0	0	700
1	0	1	1000
1	1	0	1200
1	1	1	1400

For all the non-mapped output channels (see *Table 3: Output channel assignment to DIN*), the PWM frequency and duty cycle will be the same as the DIN mapped channels (as reported in the *Dimming with direct input in Fail Safe/Stand Alone Mode* section).

Dimming with serial bus

In the L99LDLH32, each channel can be individually dimmed on an 8-bit exponential duty cycle to adequate LED brightness change to human eye light perception, giving in this way the impression of brightness linear variation. The exponential law used to calculate the dimming steps is the following:

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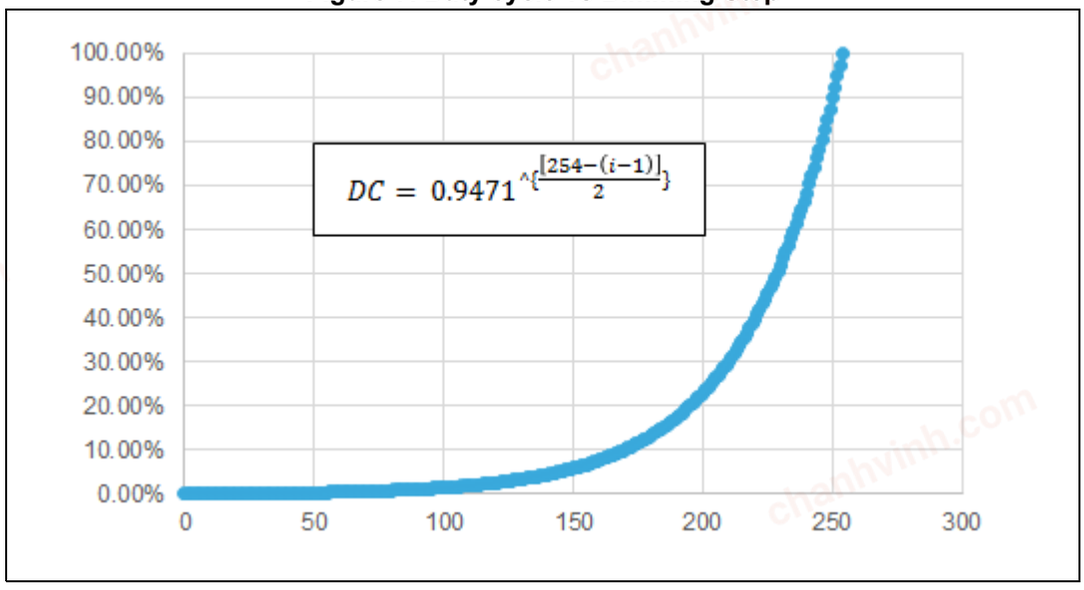
$$ton_i = PWM_{period} \cdot \alpha^{\left\{\frac{[N-(i-1)]}{2}\right\}}$$

Where ton_i is the LED ON-time during step number "i", $1 \le i \le 255$, $\alpha \approx 0.9471$, N=254.

For the step number "i" = 0, DC is set to "0".

The function of duty cycle vs 8-bit PWM_DUTY_CHx setting is shown in the following graph. The minimum duty cycle is clamped to 0.1% in any case.

Figure 7. Duty cycle vs Dimming Step

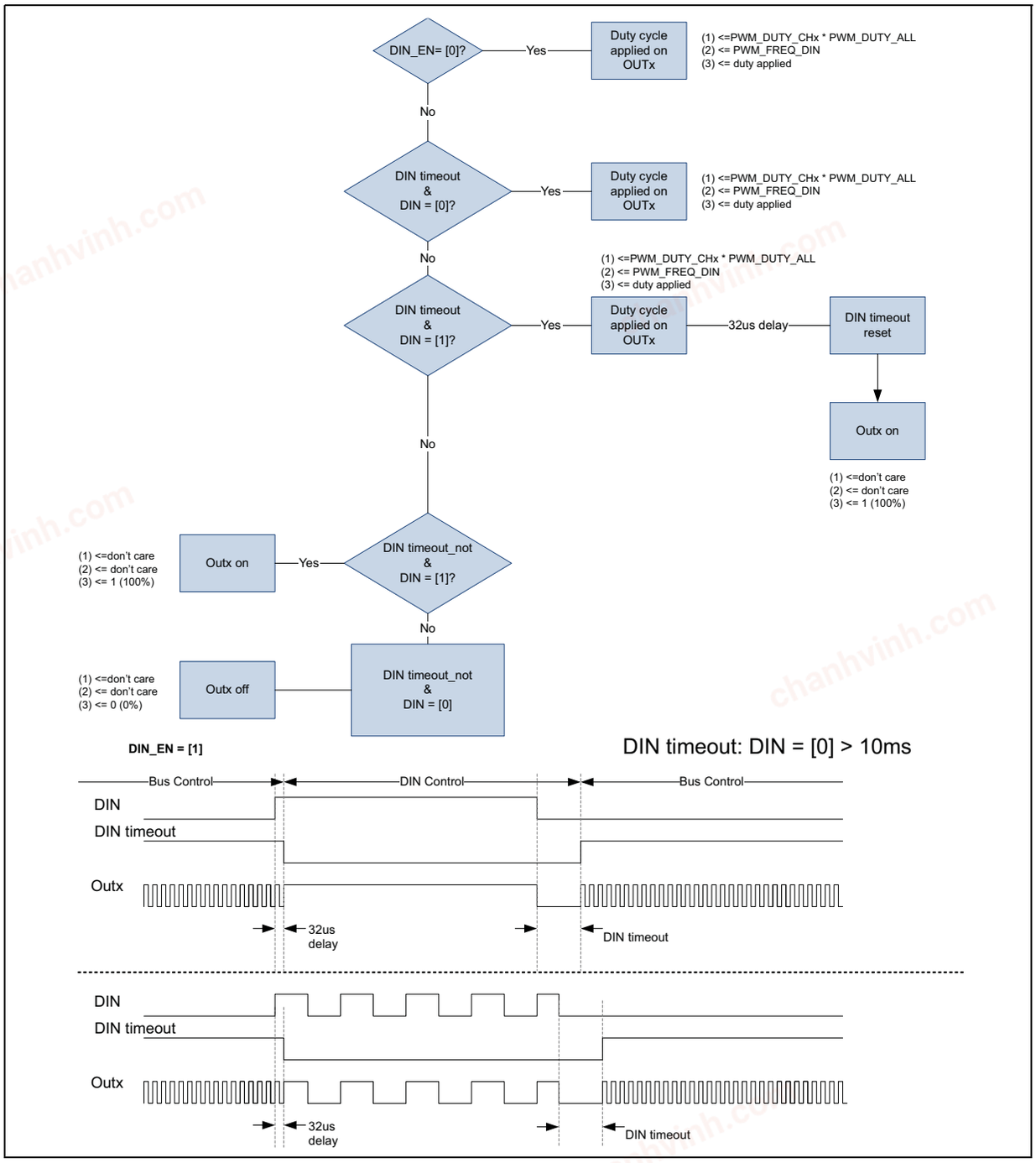


The duty cycle is configurable through serial bus (PWM_DUTY_CHx, 8 bits per channel – see RAM memory map, *Chapter 7*) and the programmed value is stored in the RAM. The individual duty cycle per channel can be superimposed by a linear 8-bit global dimming PWM_DUTY_ALL (applicable for outputs mapped to DIN). The resulting duty cycle is the product of PWM_DUTY_CHx*PWM_DUTY_ALL. Global dimming is not available for function group not mapped to DIN. If global dimming is not desired, the PWM_DUTY_ALL register has to be programmed with FFh.

Direct Input access to outputs can be enabled or disabled for each channel separately in Bus / Normal Mode. If Direct Input is enabled (by DIN_EN configuration bit – see RAM memory map, *Chapter 7*), bus control is applied when DIN = 0. In case of DIN <> 0, the bus control is automatically disabled (after t_{FILTER} time) and overtaken by DIN: the DIN input control has priority versus bus control. After a timeout higher than $t_{BUS_CONTROL}$ after the last falling edge on DIN, the bus control is reactivated. The characteristics of the function group is illustrated in the following flow chart.

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Figure 8. PWM concept for DIN function group



The PWM frequency and phase relation of several devices can be synchronized versus each other through the SYNC_I/O pin. There is one dedicated bit (SYNC I/O_M/S - see FTP/RAM memory map, *Chapter 7*) to configure the device in Provider [1] or Consumer [0] mode.

In Provider mode, the Clock frequency with scaler and phase signal is transferred to the SYNC_I/O line. In Consumer mode, clock frequency and phase signal on the SYNC_I/O line are used to synchronize its own clock. Consequently the phase relation among several

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devices can be configured (through FTP only) by PHASE_DEV bits (3-bits - see FTP/RAM memory map, *Chapter 7*).

Table 6. PWM phase shift (in Consumer mode)

PHASE_DEV [2÷0]			PWM_PHASE_SHIFT [µs]
bit 2	bit 1	bit 0	
0	0	0	0
0	0	1	15
0	1	0	30
0	1	1	45
1	0	0	60
1	0	1	75
1	1	0	90
1	1	1	105

The internal PWM clock oscillator can be reset by PWM_SYNC bit (see RAM memory map, *Chapter 7*) in order to start the PWM period at a known phase relation.

Dimming with direct input in Fail Safe/Stand Alone Mode

The L99LDLH32 features the channel output PWM dimming through direct input control.

The Direct Input controls the output channels as per FTP setting (see *Table 3: Output channel assignment to DIN*).

There is 1 configuration bit (PWM_FS_ALLx_EN - see FTP/RAM memory map, *Chapter 7*) for enabling internal PWM dimming in Stand Alone / Fail Safe mode.

The PWM signal is deactivated by related DIN: if DIN = 0, the outputs are off; otherwise the outputs follow internal PWM signal.

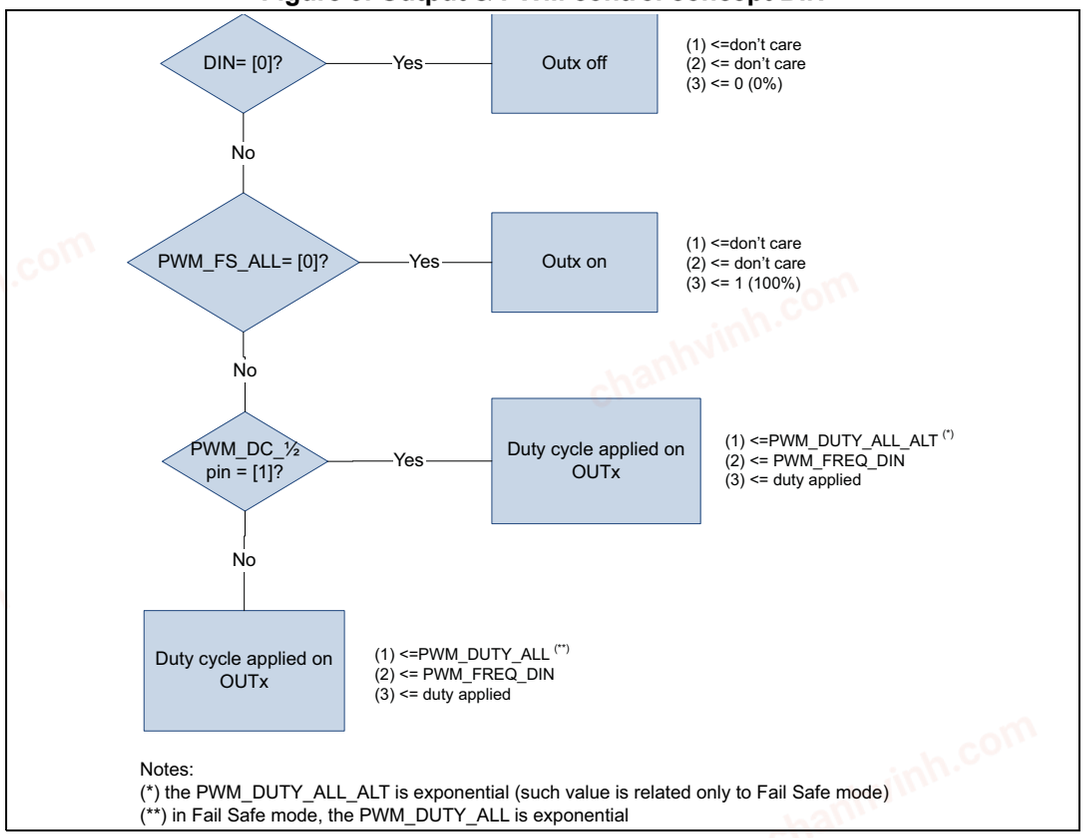
In Fail Safe / Stand Alone mode, an alternative duty cycle for DIN function group can be set by an additional 8-bit register (PWM_DUTY_ALLx_ALT - see FTP/RAM memory map, *Chapter 7*).This alternative duty cycle can be activated by dedicated pin PWM_DC_1/2.

If this pin is set at “1”, the alternative register values will be considered, otherwise, the default register PWM_DUTY_ALLx will be the reference.

The channel PWM control concept in Fail Safe / Stand Alone Mode is illustrated in the following flow chart.

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Figure 9. Output & PWM control concept DIN



Dimming with power line

In the L99LDLH32, PWM dimming through power line is possible by rectifying the V_S supply and connecting the Power Line to the Direct Inputs through resistor divider. A buffer capacitor on V_S supply pin has to be able to supply the device during PWM off state to keep it in operating mode without any reset.

When dimming through power line is performed, PWM frequency is expected in the range of [100÷200Hz] with 5% minimum duty cycle. The start-up time for light function availability is $t_{STARTUP_PWM_VS}$.

The $t_{STARTUP_PWM_VS}$ parameter is the time needed for device startup, from device power up (presence of V_S) to the channel activation.

5.3 Protections and diagnostic

5.3.1 Diagnostic availability and validation - strategy

The L99LDLH32 performs a configurable blanking time for the diagnosis, which is applied on the first channel turn on as well as on each PWM rising edge.

There are 2 configuration bits per function group (DIAG_BLANK_x - see FTP/RAM memory map, *Chapter 7*) to set the desired blanking time before validating any fault related to the channel.

The possible configuration is reported in the table below.

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Table 7. Diagnostic blanking time

DIAG_BLANK_x [1÷0]	$t_{DIAG_BLANK_x}$ [us]
00	50
01	100
10	150
11	200

After $t_{DIAG_BLANK_x}$ elapses, a failure counter starts and any channel fault is validated after N_Fails number of detected failures (also non-consecutive). The N_Fails readings are kept in memory up to N_Fails_reset (number of consecutive NOT failures detection), then the counter will be reset.

Diagnostic validation strategy is applied for any possible load fault: O/LED short to ground, open string, short to V_{PRE_REG}. If the on-time of any channel is shorter than the configured blanking time, the device automatically disables fault detection on that channel and sets the pre-regulator voltage feedback to maximum.

5.3.2 Fault bus capability

In the L99LDLH32, there is 1 fault pin with "Fault Bus" capability: 1 open drain fault pin (FAULT) is associated with 1 Direct Input (DIN), output channels are mapped according to DIN_MAP_CHx.

The fault pin is bidirectional, active low. Several fault pins of several devices can be connected together to have a common fault bus associated to a particular light function. This allows an automatic deactivation of complete light function in case of fault on single O/LED string only, according to the selected Fault reaction mode.

There is, in fact, 1-bit (FAULT_REACT_MODEx - see FTP/RAM memory map, *Chapter 7*) for fault reaction mode configuration:

Table 8. Fault reaction mode

FAULT_REACT_MODE <0>	Fault Reaction Mode
0	Fault on one string => all strings of same fault bus deactivated
1	Fault on one string => no action on other strings

5.3.3 Thermal warning

The L99LDLH32 integrates a temperature warning with one threshold.

If the junction temperature (T_J) of the device – read by internal ADC - rises above the warning temperature threshold (T_{TW}), the thermal warning status bit (TW – see RAM memory map, *Chapter 7*) is set.

Thermal warning is also reported in the Global Status Byte register, in particular Global Warning (GW) bit is set.

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As soon as the T_J drops below the thermal warning reset threshold (T_{TW}-T_{TW_HYS}), the corresponding thermal warning status bit is automatically cleared.

Even if a temperature warning is detected, device as well as output channels are kept functional.

5.3.4 Thermal shutdown

If the junction temperature of the L99LDLH32 rises above the shutdown temperature threshold (T_{TSD}), a thermal shutdown event is detected: all the output channels are switched off and the thermal shutdown status bit (TSD – see RAM memory map, *Chapter 7*) is set. The Fault pin is pulled low.

Thermal shutdown event is also reported in the Global Status Byte register, in particular Functional Error 1 (FE1) bit is set.

As soon as the T_J drops below the thermal shutdown reset threshold (T_{TSD}-T_{TSD_HYS}), the output channels are automatically re-activated. The corresponding thermal shutdown status bit (T_{TSD}) is automatically cleared as soon as T_J drops below the thermal shutdown reset threshold, contemporarily to channel re-activation.

In case of thermal shutdown, device logic and state machine remain active.

5.3.5 LED current derating

In case of temperature increasing, the device performs an automatic LED current derating based on the measurement of external NTC voltage as well as on the internal device temperature (T_J).

An integrated thermal sensor is used to sense the device junction temperature (T_J) as well as to detect thermal warning (TW) and thermal shutdown (TSD) thresholds, granting device protection in case of temperature increasing. The sensed junction temperature (T_J) is monitored by an 8-bit ADC with the aim of starting an automatic, downwards derating of the LED string current as soon as the T_{TW} - T_{TW_HYS} threshold is reached. The derating ends when the 50% of the nominal LED current is reached, which corresponds to T_J = 165°C.

The 8-bit ADC is also used to monitor the voltage on the NTC pin, where an external resistor can be connected. If the monitored voltage – whose value depends on the temperature detected by the NTC resistor itself - reaches the V_{NTC_TH} threshold (programmable by 3 bits, see *Table 78*), a downwards derating of the LED string current automatically starts, till 50% of the nominal LED current is reached. This corresponds to a NTC temperature 20°C higher than the one corresponding to V_{NTC_TH}.

The monitoring of both T_J and NTC voltage is contemporarily active. The actual derating is determined by the parameter which would require the most severe derating.

5.3.6 VS under voltage lockout

If the V_S supply falls below V_S under-voltage threshold (V_{S_UV}), the device will be deactivated - regardless of the operating mode – and the FAULT pin will be pulled low.

This feature is implemented, in order to avoid any operation outside the allowed V_S operating range.

If Supply under-voltage event is detected, the related flag (V_{S_UV} – see RAM memory map, *Chapter 7*) is set and reported also in the Global Status Byte register, where Device Error (DE) bit is set.

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As soon as the V_S supply crosses the under-voltage reset threshold ($V_{S_UV_RES}$) the device is automatically re-activated.

5.3.7 Channel output - LED short circuit detection

The L99LDLH32 performs the LED short circuit fault detection – both in Bus mode as well as Fail Safe / Stand Alone mode - based on voltage monitoring across the channel output voltage: the detection is done by comparing the absolute output voltage versus a configurable threshold.

The device features 2 groups of configurable short circuit threshold ($V_{SHT_CH_TH}$ and $V_{SHT_CH_DIN_TH}$, as showed in *Table 9*). This configurability allows short detection of one or more LEDs within the string connected to a given channel mapped according to DIN_MAP_CHx <0>.

Table 9. LED short circuit threshold - grouping

DIN_MAP_CHx <0>	Short circuit threshold group
0	$V_{SHT_CH_TH}$
1	$V_{SHT_CH_DIN_TH}$

The short circuit detection can be enabled /disabled through the SHT_DET_EN bit (see FTP/RAM memory map, *Chapter 7*): if this bit is equal to “0”, the short circuit detection is disabled, otherwise, the short circuit detection is enabled. In this latter case, two different scenarios are possible: to enable or disable the channel output deactivation in case of short circuit, by one dedicated bit (SHT_OFF_x – see FTP/RAM memory map, *Chapter 7*). If SHT_OFF_x bit is set to 0, the faulty channel output is kept active in case of short circuit, otherwise the faulty channel is latched off. The channel is recognized in short circuit as soon as its output voltage - read by ADC - is less than the specified short circuit threshold ($V_{SHT_CH_TH}$ or $V_{SHT_CH_DIN_TH}$, see *Table 9*).

In Bus mode, the faulty channel output is latched off and the dedicated fault bit (SHT_CHx – see RAM memory map, *Chapter 7*) is set. The channel output can be restarted and the fault bit will be cleared by sending a read & clear command to address 28. Selective bitwise read & clear is possible.

In case of fault in Fail Safe / Stand Alone mode:

- for the channels configured with FS_OUT_EN = 0, the output is latched off and it is cleared upon falling edge of DIN with t_{DIN_FALL} settling time. This means that fault is not cleared during PWM dimming with PWM off-time shorter than t_{DIN_FALL} time.
- for the channels configured with FS_OUT_EN = 1, after elapsing the $t_{AUTORESTART}$, the faulty channel is automatically re-activated and the SHT_CHx bit is cleared.

If outputs are permanently enabled by FS_OUT_ENx = [1], in case of short circuit, they will be latched and the latch can be cleared only through a power on reset condition.

For all (and only) those channels mapped on DIN (DIN_MAP_CHx = 01), the L99LDH32 features the indication of short circuit on FAULT pin. If the bit SHT_EN (see FTP/RAM memory map, *Chapter 7*) is equal to “0”, the short circuit fault detection is NOT propagated on FAULT bus; whilst if SHT_EN = 1, the short circuit of the faulty channel is indicated on associated FAULT bus (pulled low).

The channel short event is also reported in the Global Status Byte register, in particular Functional Error 2 (FE2) bit is set.

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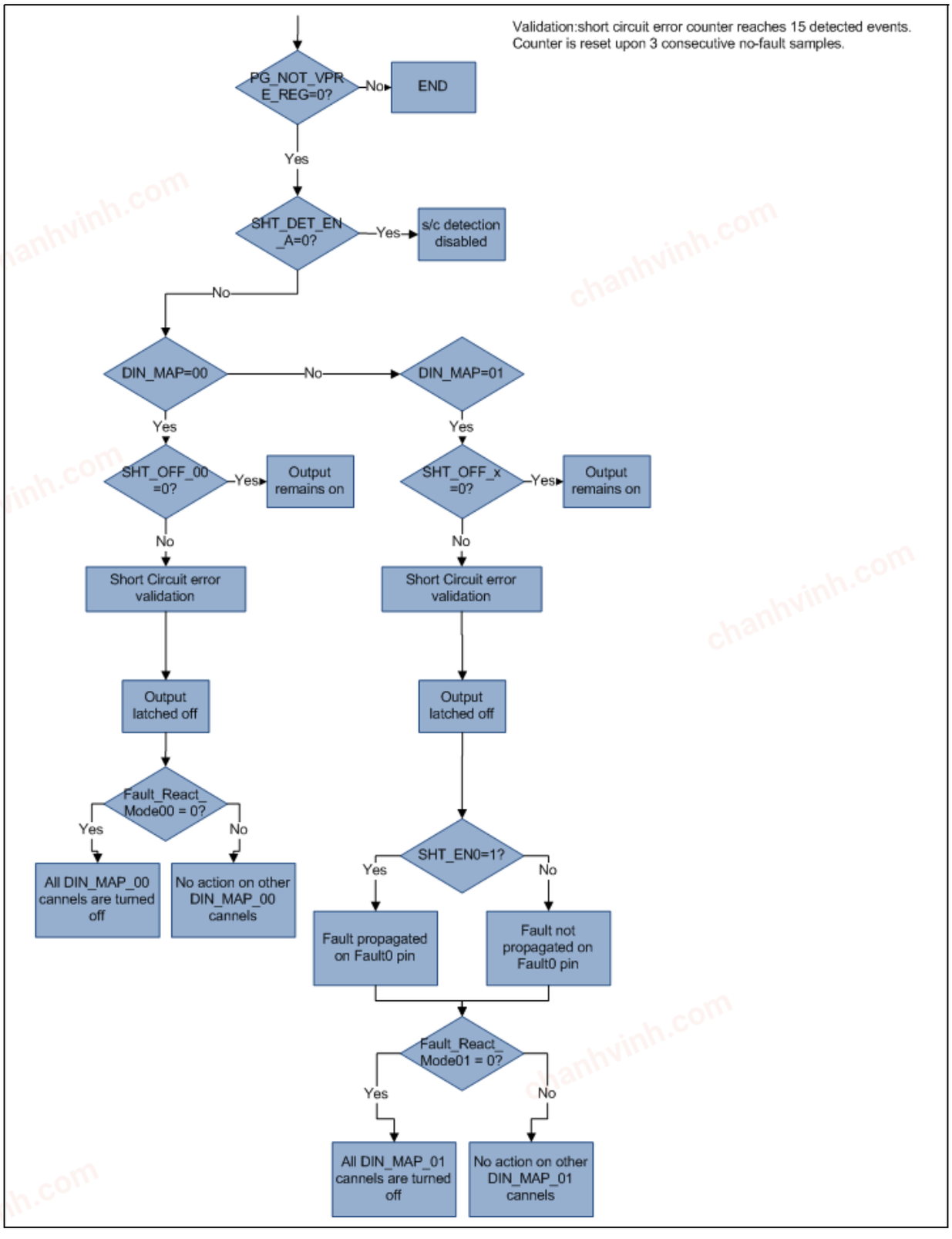
Then, for both mapped and non-mapped channels, according to the fault reaction mode configuration bit (see *Table 8*), an automatic deactivation of the complete light function respectively of the faulty channel only is performed.

The flow chart reported in *Figure 10* shows how the device manages the faulty channel and the channels corresponding to DIN_MAP as well as the fault pin handling.

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Figure 10. LED short circuit fault management



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5.3.8 Channel output - short circuit to GND

The L99LDLH32 features the output channel voltage shortage to GND - both in Bus mode as well as Fail Safe / Stand Alone mode - based on voltage monitoring across the channel output voltage: the detection is done by comparing the absolute output voltage versus a fixed threshold ($V_{OUT_SHT_GND_TH}$).

The short circuit to GND detection is masked when the O/LED supply voltage is below a power good threshold ($V_{PG_TH_VPRE_REG}$).

When the channel output voltage is lower than the $V_{OUT_SHT_GND_TH}$ threshold, a shortage between a channel output and GND is detected and the related channel bit (OUT_SHT_GND_CHx– see RAM memory map, *Chapter 7*) is set. In case the LED short detection threshold (either $V_{SHT_CH_TH}$ or $V_{SHT_CH_DIN_TH}$) is set lower than the channel short to ground threshold ($V_{OUT_SHT_GND_TH}$), this latter protection has the highest priority.

When this flag is set, the faulty channel is disabled regardless of the setting of its own short off (SHT_OFF_x) bit. This flag is a read & clear bit: channel “x” is latched off in case of fault, it will restart after bit clearing. If fault is still there, the channel will be latched off again.

In case of Fail Safe / Stand Alone mode, after elapsing the $t_{AUTORESTART}$, the faulty channel is automatically re-activated and the OUT_SHT_GND_CHx bit is cleared.

Channel output short to GND voltage event is also reported in the Global Status Byte register, in particular Functional Error 2 (FE2) bit is set.

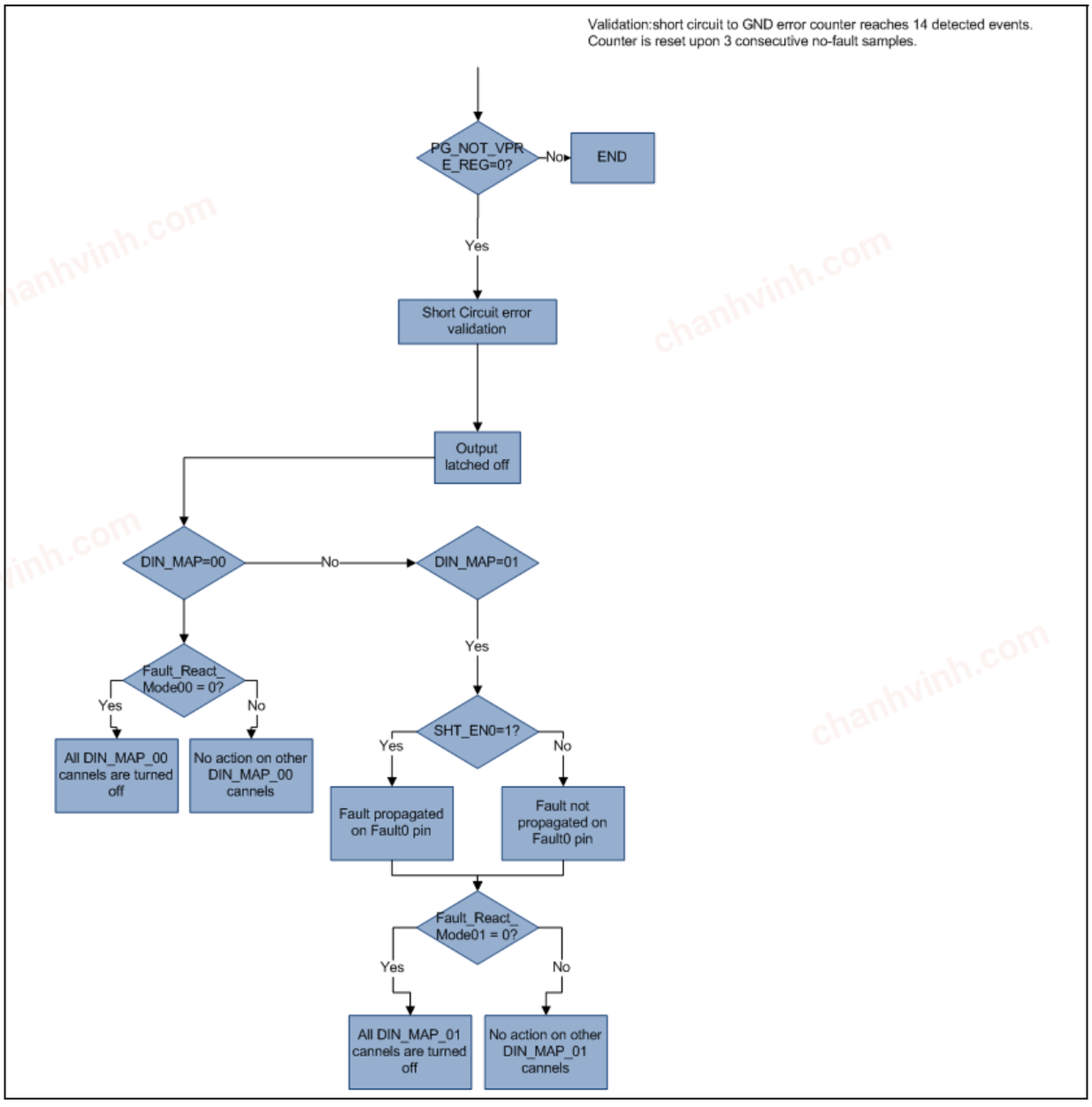
For all (and only) those channels mapped on DIN (DIN_MAP_CHx = 01), the L99LDH32 features the indication of short circuit to GND on FAULT pin. If the SHT_EN bit (see FTP/RAM memory map, *Chapter 7*) is equal to “0”, the short circuit fault detection is NOT propagated on FAULT bus; whilst if SHT_EN = 1, the short circuit of the faulty channel is indicated on associated FAULT bus (pulled low).

Then, for both mapped and non-mapped channels, according to the status of the fault reaction mode configuration bit (see *Table 8*), an automatic deactivation of the complete light function respectively of the faulty channel only is performed.

The flow chart reported in *Figure 11* shows how the device manages the faulty channel and the channels corresponding to DIN_MAP as well as the fault pin handling.

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Figure 11. Short to ground fault management



5.3.9 Channel output – Open load detection

The L99LDLH32 features the open load (no current regulation) detection, implemented both in Bus mode and Fail Safe / Stand Alone mode as well.

The open load detection is masked when the O/LED supply voltage is below a power good threshold ($V_{PG_TH_VPRE_REG}$), which is configurable in the range of [$V_{PG_TH_VPRE_REG_min}$ ÷ $V_{PG_TH_VPRE_REG_max}$] with a step equal to $V_{PG_TH_VPRE_REG_step}$.

There is one status bit (PG_NOT_VPRE_REG - see RAM memory map, *Chapter 7*) for the V_{PRE_REG} group to indicate the selected voltage threshold to enable open load diagnostic is reached. If this bit is equal to “0”, the desired voltage threshold is not reached and the open load diagnostic is disabled; otherwise, the threshold is reached and the diagnostic enabled.

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After power good threshold is reached, the open load detection starts and the channel is recognized in open load as soon as its voltage drop – read by ADC as a difference between V_{PRE_REG} and V_{OUTx} - is less than the specified open load threshold (V_{OL_TH}).

Whenever PG_NOT_VPRE_REG (bit 0, see *Chapter 7.1.18*) is set, the application shall temporarily deactivate the Pre-Regulator control algorithm, by two consecutive UNICAST WRITE frames to disable and enable VREF_PRE_REG bit (bit 22, see *Chapter 7.1.6*).

In Bus mode, the faulty channel output is latched off and the dedicated fault bit (OL_CHx – see RAM memory map, *Chapter 8*) is set. The channel output can be restarted and the fault bit will be cleared by sending a read & clear command to address 29. Selective bitwise read & clear is possible.

In case of fault in Fail Safe / Stand Alone mode:

- for the channels configured with FS_OUT_EN = 0, the output is latched off and it is cleared upon falling edge of DIN with t_{DIN_FALL} settling time. This means that fault is not cleared during PWM dimming with PWM off-time shorter than t_{DIN_FALL} time.
- for the channels configured with FS_OUT_EN = 1, after elapsing the $t_{AUTORESTART}$, the faulty channel is automatically re-activated and the OL_CHx bit is cleared.

For all (and only) those channels mapped on DIN (DIN_MAP_CHx = 01), the L99LDH32 features the indication of open load on FAULT pin. If the bit OL_EN (see FTP/RAM memory map, *Chapter 7*) is equal to “0”, the open load fault detection is NOT propagated on FAULT bus; whilst if OL_EN = 1, the open load of the faulty channel is indicated on associated FAULT bus (pulled low).

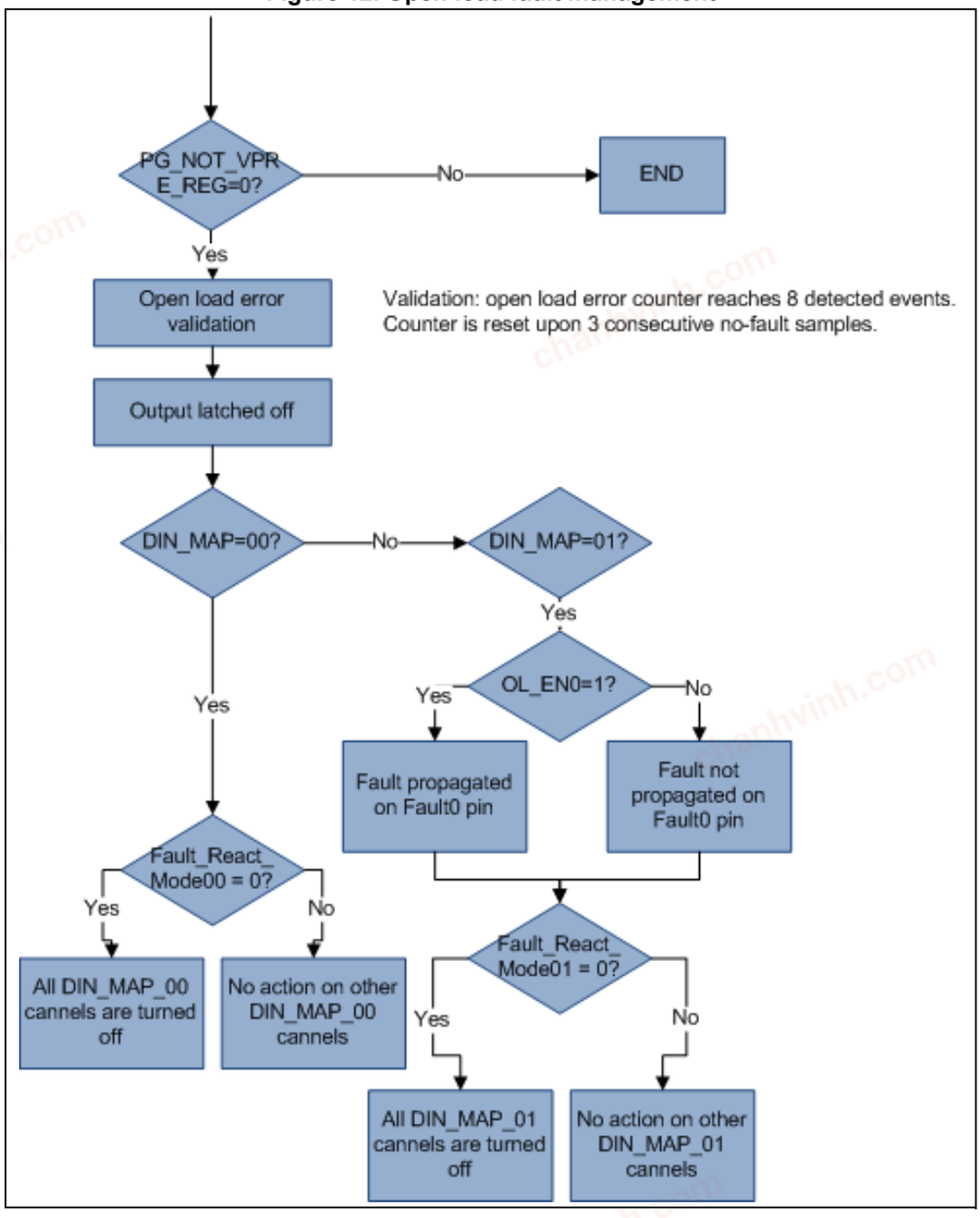
Channel open load event is also reported in the Global Status Byte register, in particular Functional Error 2 (FE2) bit is set.

Then, for both mapped and non-mapped channels, according to the fault reaction mode configuration bit (see *Table 8*), an automatic deactivation of the complete light function respectively of the faulty channel only is performed.

The flow chart reported in *Figure 12* shows how the device manages the faulty channel and the channels corresponding to DIN_MAP as well as the fault pin handling.

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Figure 12. Open load fault management



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6 Communication interface

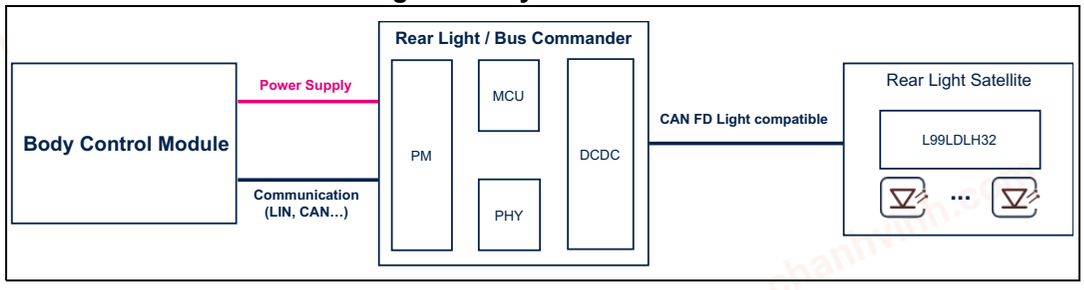
6.1 CAN FD Light compatible network protocol

The L99LDLH32 features a serial CAN FD Light compatible interface, a robust Commander-Responder communication bus, restricted to the lamp internal communication.

It uses the CAN FD physical interface - therefore differential bus wiring – and a protocol that can be implemented by a CAN FD protocol controller. It guarantees a defined edge density for synchronization and, for safety, CRC and error checking are provided.

The system overview is shown in *Figure 13*. The communication Commander is implemented in the Rear LED ECU using the protocol controller in the µC and a CAN FD transceiver. An additional transceiver (e.g. LIN, High-Speed CAN or other) may be used by the ECU to communicate with other ECUs in the car. The communication Responders are located in the LED satellites.

Figure 13. System overview



6.2 Protocol overview

6.2.1 Basic function

The CAN FD Light compatible network is a bus system on which all participants share the same differential wires. Messages being sent by one participant are received by all others. Its protocol uses a Commander-Responder scheme. The Commander is implemented in the host ECU while the Responders are built in the LED drivers.
The Responders only answer upon request by the Commander, therefore no collision resolving mechanisms are needed.
Two basic message types are used: broadcast messages and unicast messages.
A broadcast message is sent to the Responders and expects no answer from them. The Responders on the bus pick the data relevant for them from the message.
A unicast message is addressed to a specific Responder that answers by sending the requested data.
A specific unicast message can be sent in predefined intervals to serve a watchdog triggering. The unicast message can expect an answer from the addressed Responder within a given time frame. Both mechanisms can be used to implement an efficient supervision scheme, which allows the detection of a disconnected or failed network participant.

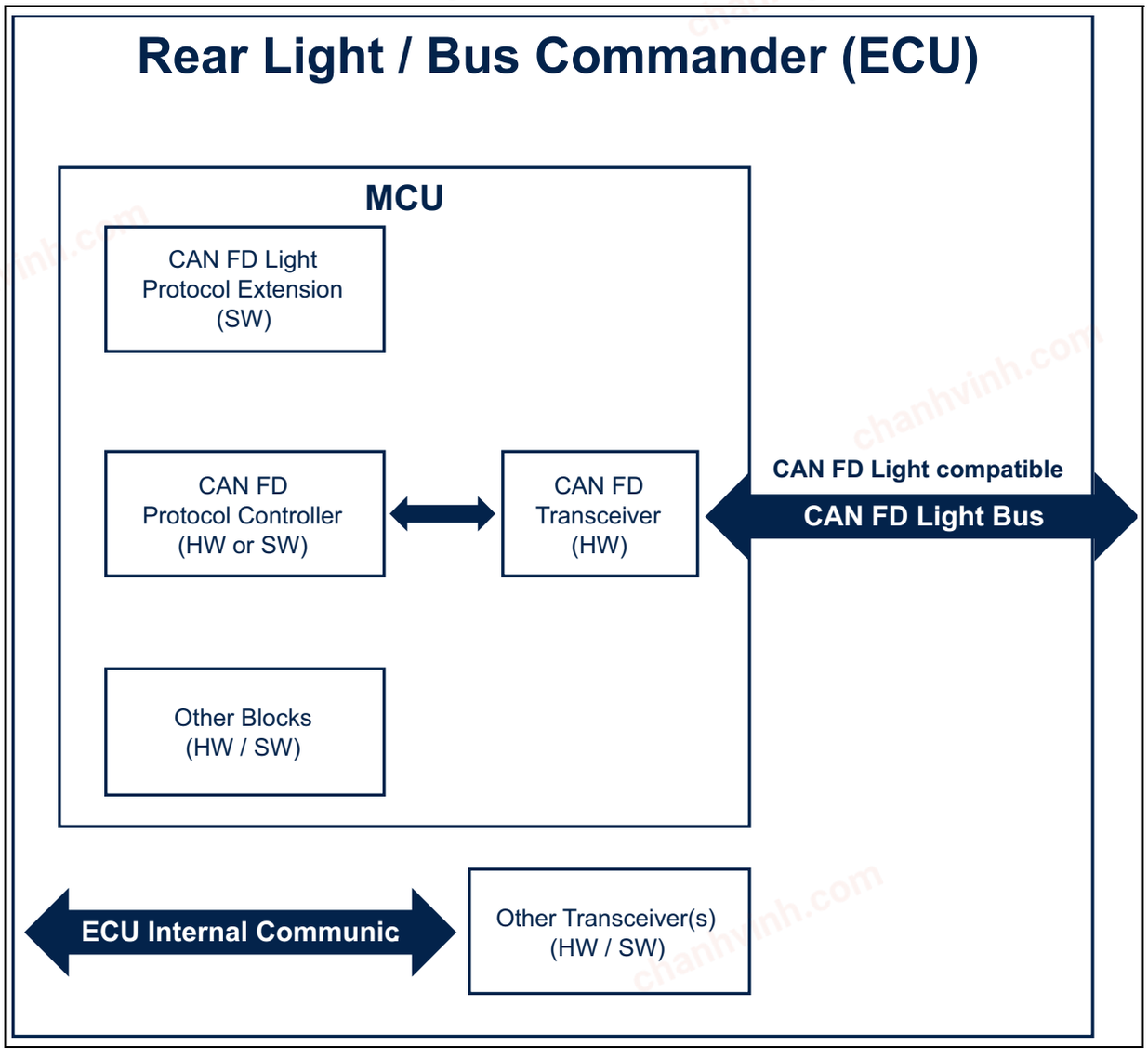
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6.2.2 Commander

Figure 14 shows the block diagram of the Commander as referred in *Figure 13*. The protocol Commander uses a standard CAN FD protocol controller that may be already implemented in the automotive microcontroller in hardware or software. An additional CAN FD protocol extension software controls this protocol controller to make it act as CAN FD Light compatible Commander and implements the Commander side of the CAN FD Light compatible protocol.

To access the physical interface of the CAN FD network a standard CAN FD transceiver is used.

Figure 14. Commander block diagram

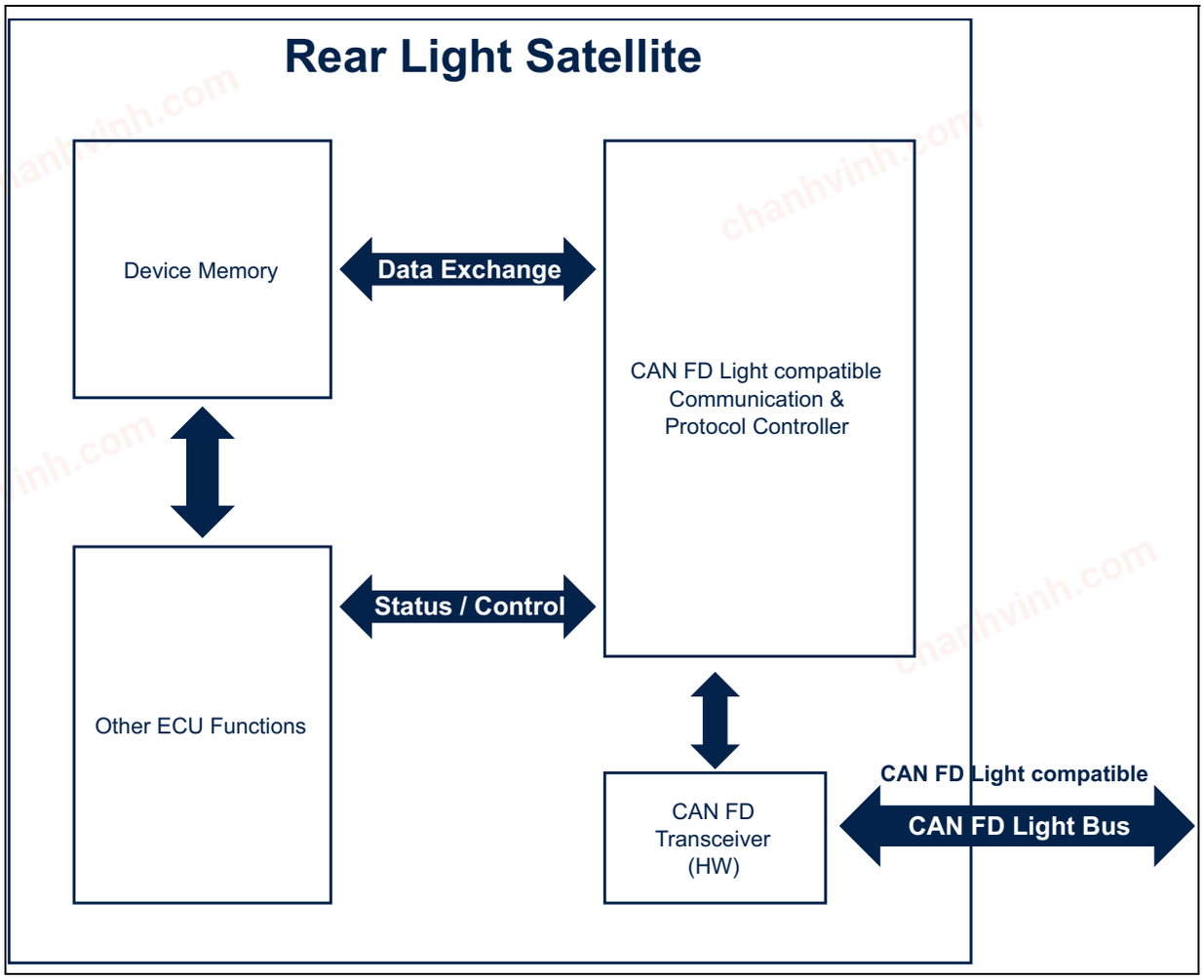


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6.2.3 Responder

The CAN FD Light compatible Responder is located in the LED satellites (see *Figure 13*) and there inside the LED controller device (see *Figure 15*).

Figure 15. Responder ECU Controller Device



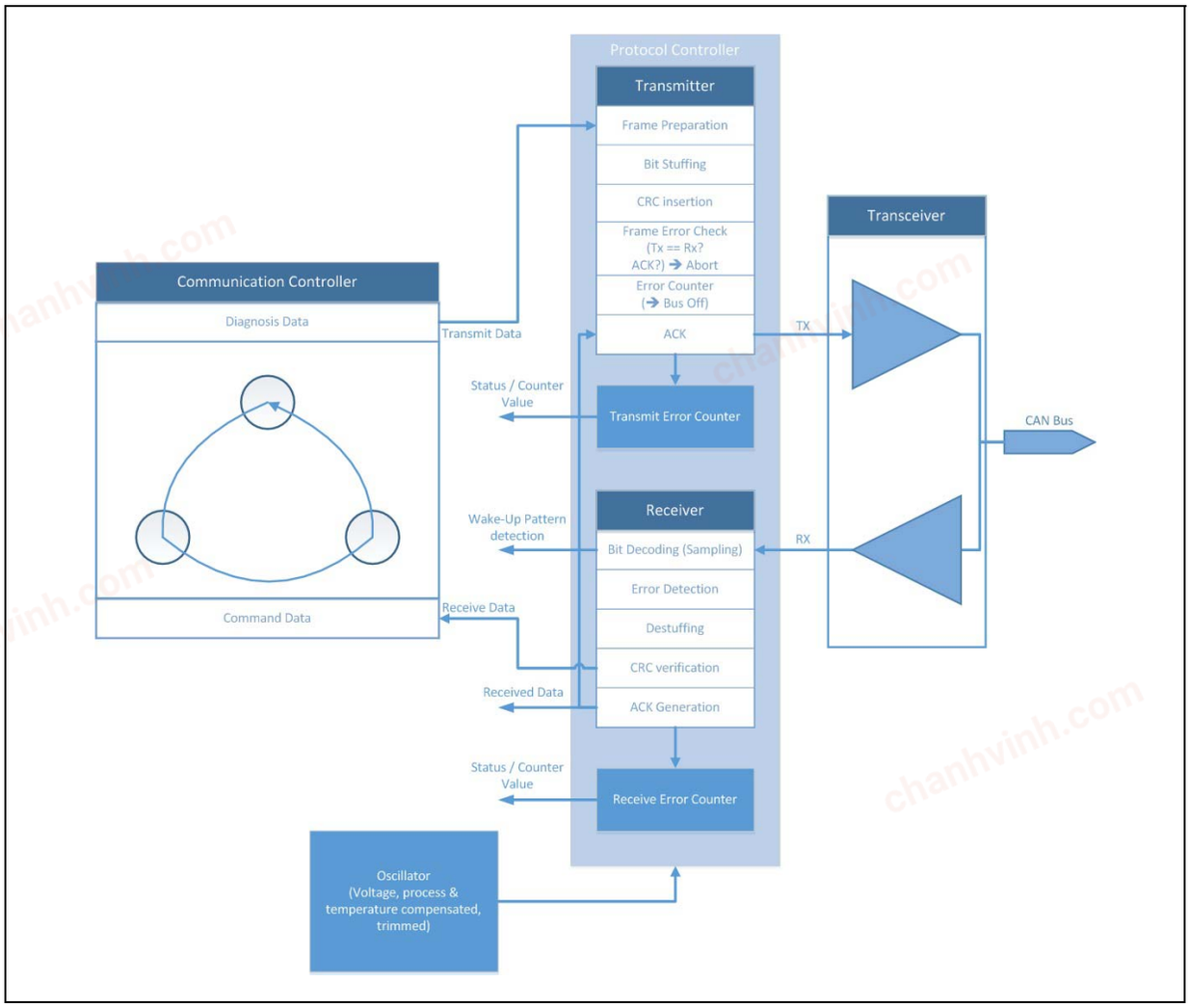
The implementation is done entirely in hardware It consists of three parts shown in *Figure 16*:

- A standard CAN FD transceiver, according to ISO-11898-2;
- A CAN FD Light compatible protocol controller with an accurate oscillator for generating and sampling the data bits.
- A communication protocol controller that sends and receives data to and from the protocol controller and controls the communication.

Each Responder has its own 9-bit wide ID.

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Figure 16. CAN FD Light compatible Communication and Protocol Controller



6.3 Data link layer

The L99LDLH32 supports data exchange at a bit rate of 1Mb/s.

The communication is checked for safety reasons: a CRC value is sent with each data frame, supporting ASIL B requirements.

After every frame all recipients send an acknowledge bit so at least one is received by the sender so it can detect if it is still connected to the network.

Since all participants of the network are connected to the same wire, a transmitter is able to detect if it is not correctly operating - consequently entering passive state not to disturb the bus communication.

The data sampling clock is generated in each receiver individually, therefore a minimum edge density of the data stream is guaranteed such that at least every 10th bit a recessive to dominant edge is present so a synchronization of the receiver to the data stream is possible.

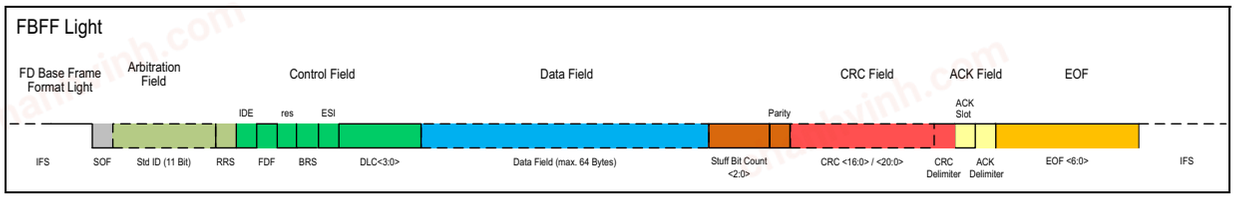
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Also a wake-up over the network is implemented.

6.3.1 CAN FD Light compatible frame format

The CAN FD base format is used for the CAN FD Light compatible protocol without extended ID implemented as shown in *Figure 17*.

Figure 17. CAN FD Base Frame Format (FBFF)



The bits in the control field are fixed: FD frame (FDF) is always recessive. Not supported are extended ID (EID, IDE bit always dominant), bit rate switch (BRS, always dominant) and error state indication (ESI, always dominant).

The data field can be up to 64 bytes long, the number of bytes is encoded in the data length code (DLC) field. Depending on the number of data bytes either CRC17 or CRC21 is calculated. Only one CRC delimiter bit is sent and accepted since the data bit rate is the same as the arbitration bit rate.

The arbitration and data bit rate are both 1 Mb/s. The bit rate is not switched.

6.3.2 Wake-Up

The Responders support a power down mode out of which they can be woken up by the wake-up frame shown in *Table 10*.

6.3.3 Error frames

No error frames are sent by the Responders. Error frames may be sent by the Commander, but are ignored by the Responders.

6.3.4 Collisions

Since the communication is always controlled and initiated by the Commander, the bus participants do not arbitrate. Collisions lead to data frame errors.

6.3.5 Error handling

Network participant disconnect

Since all participants share the same bus various mechanisms allow the detection of a disconnected device.

After each sent frame at least one acknowledge is expected from a receiver. If this acknowledge is not received it can be assumed that the sender is not connected to the network.

Broadcast frames can be transmitted within a given interval. Responders not receiving a broadcast frame after a defined time may have lost their connection to the Commander.

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The Commander may expect an answer from the addressed Responder after having sent a diagnosis request within a given time frame. If the answer is not received the communication with the addressed Responder may have been lost.

Sender bus block

The Responders check the bus for permanent recessive or dominant states. Both states indicate a bus block and the sender may not be able to transmit any messages

Frame errors

Each received frame is verified in regard to these features:

- CRC: the correctness of the received CRC for each frame is checked.
- CRC Delimiter: after the CRC, one recessive bit as CRC delimiter has to be received;
- Bit Stuffing: The correct position of the stuff bits is checked

If at least one of these conditions is not met, the frame is discarded.
Each transmitted frame is checked for:

- Permanent recessive errors: If transceiver transmitter changes to dominant state, but CAN bus does not follow for four times, the transceiver transmitter is disabled
- Permanent dominant errors: if the bus state is dominant for t > 700 µs a permanent dominant error is detected. The transceiver transmitter is disabled.

Invalid messages are not resent.
Error recovery: upon reception of a valid unicast frame, the transceiver transmitter is enabled again.

6.4 Data handling

6.4.1 Overview

As described in the *Section 6.2: Protocol overview*, two basic message types are used: broadcast messages, addressed to several Responders without any Responder answer; unicast messages, addressed to individual Responder followed by Responder answer.

A Responder corresponds to a 16 channels entity, therefore the L99LDLH32 is a two Responder device and has two Responder IDs, Responder ID0 and Responder ID1. Only Responder ID0 (corresponding to the 16 channels entity of CH0 - Ch15) is programmable, Responder ID1 (corresponding to the 16 channels entity of Ch16 - Ch31) is automatically forced to Responder ID0+1. The Responder ID is programmable with 9 bits while its 2 LSB are reserved to distinguish between different Responders within the device and shall be programmed to “00” (any different value is ignored). This means that physical devices on the bus are distinguished by Responder ID bits [8:2] – for example 0, 4, 8, 12, 16 …

In case of “Unicast communication” (see *Section 6.6*), a Commander can access all device registers either using CAN ID equal to Responder ID0 or Responder ID1, while the ID of response is always equal to (Responder ID0 | 0x200). A specific protocol is embedded into the data of the unicast frames in order to allow to specify register address and type of operation (read/write/clear).

In case of “Broadcast communication” (see *Section 6.5*), a Commander can send CAN FD frame with 64 data bytes to several Responders. Each broadcast data frame has a specific Chain ID (bits 0-5 of CAN ID field, see *Section 6.5.3*) which allows to distinguish between 64 different groups of Responders. Each Responder assigned to this Chain ID group can pick

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16 data bytes from this frame (data position is configurable) and update all duty cycle or current values registers accordingly. The selection between duty cycle or current value update is done by bit 6 of CAN ID field. The Chain ID and data position of each Responder is configurable using broadcast initialization frame. Responder ID0 and Responder ID1 of the same device have to be assigned to different Chain IDs. This means that it is not possible to update all 32 channels by single broadcast frame.

6.5 Broadcast frames

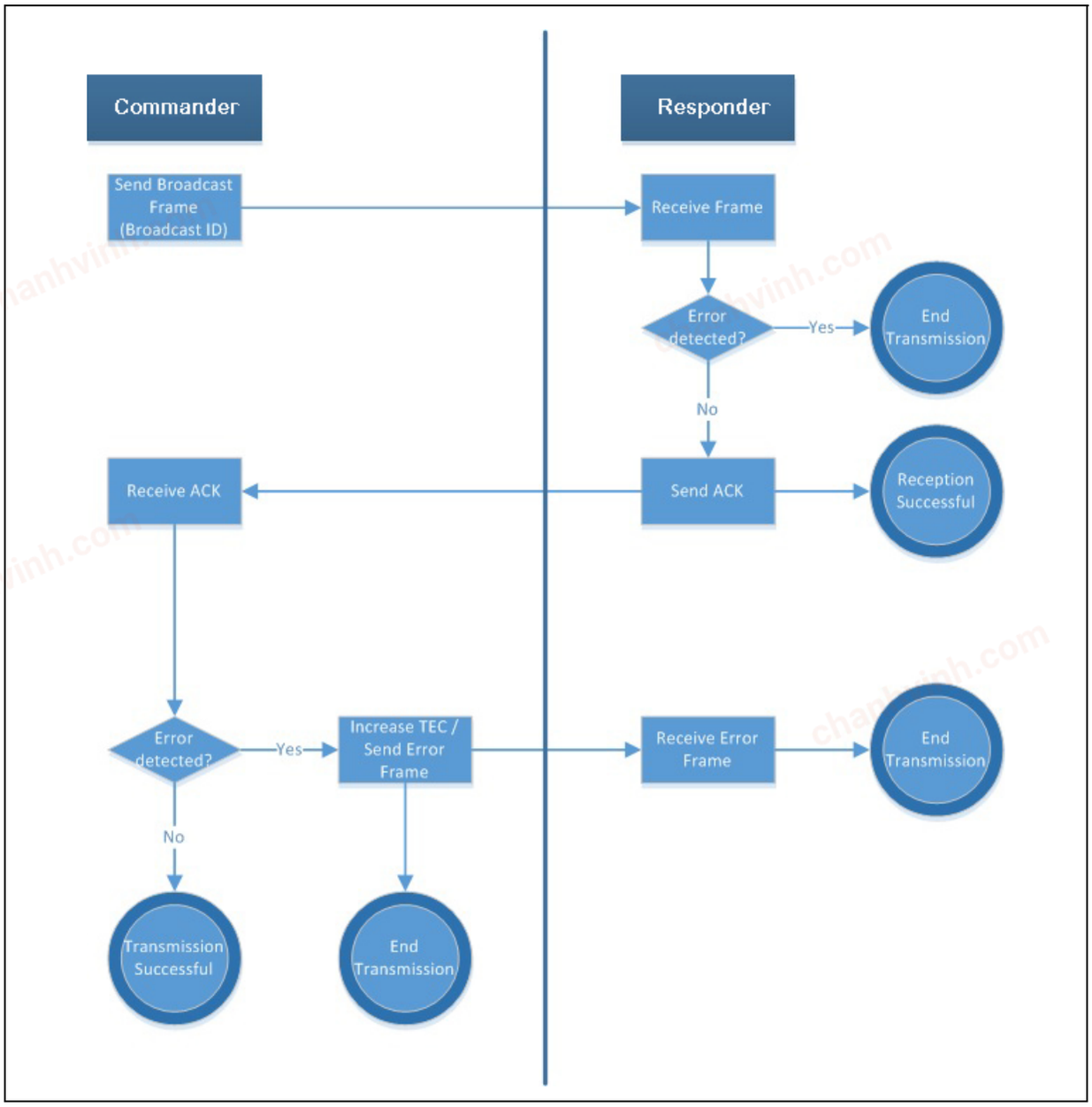
6.5.1 Frame format

Broadcast frames are transmitted to all Responders in the network. The broadcast frame contains in its ID the number of the chain that is addressed. Each Responder belonging to this chain picks its data from the maximum 64 bytes transferred by this frame. Each L99LDLH32 device can pick 16 bytes of data. The position from where it picks the data is defined during Chain Initialization.

Figure 18 shows the communication flow of a broadcast frame.

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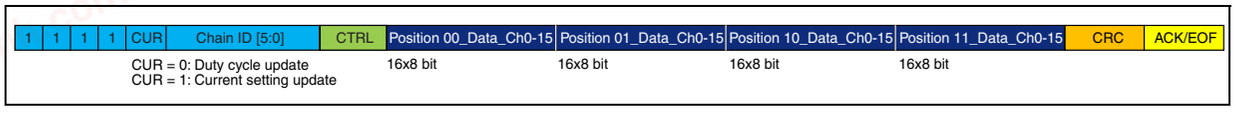
Figure 18. Broadcast message flow



6.5.2 Broadcast frame for current setting and PWM duty cycle setting

As shown in *Figure 19*, a broadcast frame uses the ID starting with '1' followed by three '1's and the chain number. Bit 6 "CUR" defines whether the data contains PWM duty cycle data (0) or current setting data (1). The six-bit chain number allows the assignment of 64 chains with up to four Responders consisting of 16-channel entities each.

Figure 19. Broadcast frame



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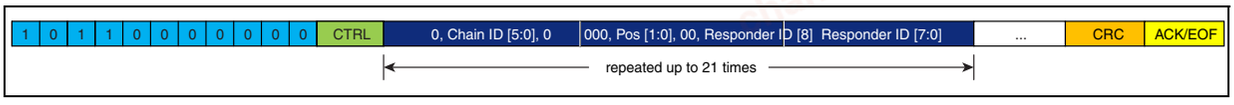
In each 16-byte data package data for Ch15, respectively the highest channel number, is the MSB, data for Ch0, respectively the lowest channel number, is the LSB.

This broadcast frame will be ignored by the Responder as long as its Reset Bit RSTB is not cleared.

6.5.3 Chain initialization

A specific broadcast frame is sent to all Responders to inform them about the chain they belong to and their position within this chain so each Responder is able to grab data intended for it.

Figure 20. Broadcast chain initialization



The ID for this chain initialization frame is “1_0110_0000000”. For every Responder three bytes are used to identify the chain it belongs to, its position and the addressed Responder with the following data structure for each Responder:

- MSB: 0, Chain ID [5:0], 0
- Next byte: 000,Pos[1,0], 00, Responder ID[8]
- LSB: Responder ID[7:0]
- Position 00: Responder picks data bytes 0-15
- Position 01: Responder picks data bytes 16-31
- Position 10: Responder picks data bytes 32-47
- Position 11: Responder picks data bytes 48-63

Note: If a device has several Responder IDs (i.e. a 32-channel device has two Responder IDs), those Responder IDs must be assigned to different Chain IDs

Responder IDs of the same device cannot be initialized in a single broadcast frame.

As reported in Figure 20, it is possible to initialize up to 21 Responders within one chain initialization broadcast frame.

Chain Initialization will be executed on the Responder, even if its Reset Bit RSTB is set. Chain Initialization will not clear Reset Bit RSTB.

6.5.4 Go to sleep/wake-up pattern

For sending the network to sleep and waking it up again a dedicated ID is defined. The reserved WUP ID is “1_000_011_1100”. A frame with this ID and without data (DLC=0) is the command to send all Responders into sleep/standby mode. This is shown in *Figure 21*.

Figure 21. Send-To-Sleep command



For waking up all the Responders, in the network the data in the payload satisfy the wake-up pattern requirements of ISO11898-2 with t_{CAN_FILTER} (short) at 1Mb/s.

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This wake-up pattern is repeated in the eight data bytes of the frame shown in *Table 10*. The Responders recognize the dominant-recessive-dominant pulse in which the three individual pulses are longer than the specified filter time. These pulses are contained in the data field.

If the frame does not contain any data, it serves as “Go-To-Sleep”-command for all Responders in the network. If it contains at least one data byte, it acts as a wake-up pattern for all Responders.

Table 10. Wake-up pattern (WUP) frame

ID	CTRL	DLC	DATA BYTE 1	DATA BYTE 2-8
“1_000_011_1100”	“001000”	1000	1111_1110	0000_1111

In conclusion:

ID = “1_000_011_1100” & DLC = 0 → send-to-sleep command

ID = “1_000_011_1100” & DLC ≠ 0 → wake-up pattern frame

6.5.5 Synchronization Frame

The synchronization frame must be sent by the commander after each responder reply, but only if the addressed devices change in the next commander frame. Due to the frequency offset between the replying Responder and the Commander some other Responders may not be able to receive frames sent by the Commander correctly after a Responder answer. Therefore, the frame in *Figure 22* has to be sent by the Commander to ensure correct synchronization of all Responders to the Commander. The Responders will synchronize on this frame but drop the content because it does not contain an ID that the Responders recognize.

Figure 22. Synchronization frame



Table 11. Synchronization frame

ID	CTRL	DLC
“1_010_101_0101”	“001000”	0000

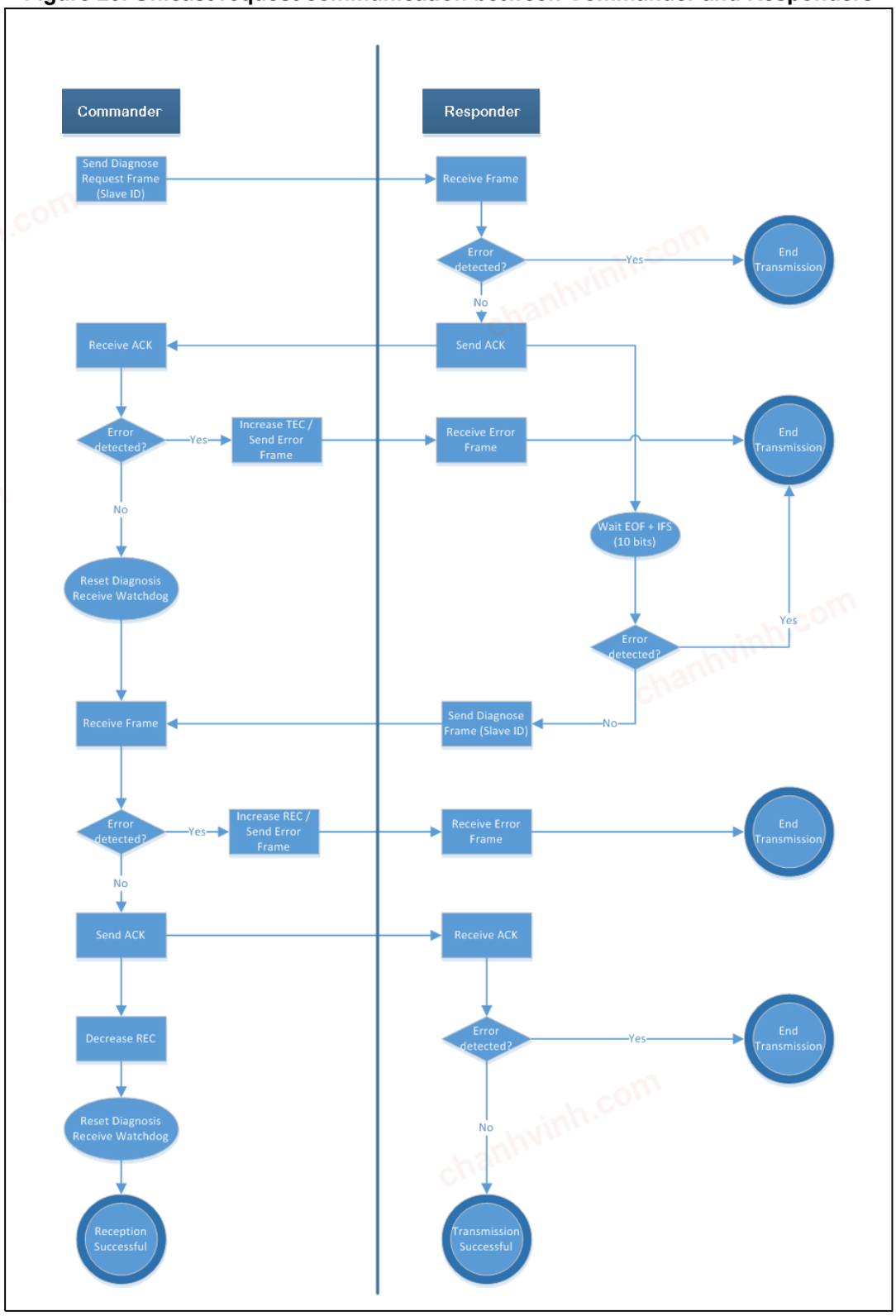
6.6 Unicast frames

6.6.1 Unicast request frame

The Commander may request action from a particular Responder by sending a unicast request frame, which uses the Responder ID in the CAN FD ID field preceded by “0” to distinguish the Commander request from the Responder answer. The MSB of all CAN FD IDs used for unicast frames in the network is “0” to distinguish between unicast and broadcast frames.

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Figure 23. Unicast request communication between Commander and Responders



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In case the unicast frame contains data, the first data byte contains OP code (bits 7-6) and register address (bits 5-0). The Operation Code represents the instruction to be performed; whilst the following 6 bits represent the address on which the operation will be performed.

The next 4 data bytes contain the optional data.

Table 12. Unicast frame data - Operating Code and Register Address

	Command Byte (8-bit)							
	Operating Code		Address					
Bit	7	6	5	4	3	2	1	0
Name	OC1	OC0	A5	A4	A3	A2	A1	A0

The operation code is used to distinguish among different accesses modes to the registers of the Responder device.

Table 13. Unicast frame data - Registers access mode

Bit 7	Bit 6	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Read and Clear Mode>
1	1	<Read Device Information>

A Write Operation will lead to a modification of the addressed data by the payload if a write access is allowed (e.g. Control Register, valid data).

A Read Operation will instruct the Responder to respond with a frame containing a Global Status Byte and the data present in the addressed register at Communication Start. Read operation instructions executed on specific addresses will initiate the Responder to respond with a frame containing data present in the addressed register and the three subsequent registers. This command is called Burst Read. In any case, the payload data of the Commander request will be ignored and internal data will not be modified.

A Read & Clear Operation will instruct the Responder to respond with a frame containing a Global Status Byte and the data present in the addressed register after the execution of Clear command. Furthermore a Read & Clear Operation will lead to a clearance of the addressed register status bits. The bits to be cleared are defined first by address and secondly by the payload bits set to ‘1’.

A read device information operation accesses the ROM device data (see ROM memory map).

Besides write, read, read&clear, there are two Advanced Operation Codes. Both of them can be used to clear all status registers, whilst one can be used to set all control registers to their default value.

Both ‘set all control registers to default’ and ‘clear all status registers’ commands are performed when an OpCode ‘11’ at address b’111111 is performed.

The Payload is the data transferred to the Responder device with every unicast communication. The Payload always follows the OpCode and the Address bits.

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For *Write* access the Payload represents the new data written to the address registers.

For *Read* Operation the Payload is not used. For functional safety reasons it is recommended to set unused Payload to ‘0’.

For *Read & Clear* operation the *Payload* indicate the clearance of specific bits in the Status Register. The bits to be cleared are defined first by address and secondly by the payload bits set to ‘1’.

Figure 24. Unicast diagnosis request frame



As shown in *Figure 24*, the Commander addresses a Responder by its “Responder ID” in CAN FD ID.

6.6.2 Unicast response frame

The Responders answer with a diagnosis response frame to the Commander’s diagnosis request frame (see *Figure 25*). The CAN FD frame ID is the Responder ID preceded by “01” to distinguish the Responder answer from the Commander request.

The Commander must send a synchronization frame - according to *Chapter 6.5.5* - after each responder replies (but only if the addressed devices change in the next commander frame), to ensure the responders are synchronized to the commander and the frames sent by the commander are correctly received by all responders.

Figure 25. Unicast diagnosis response frame



6.6.3 Global Status Byte (GSB)

Figure 26. Global Status Byte

Bit	7	6	5	4	3	2	1	0
Name	GSBN	RSTB	x	FE2	FE1	DE	GW	FS

The Global Status Byte is described here below.

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Table 14. Global status byte field description

Bit #	Name	Description
7	GSBN	Global Status Bit Not This bit is a NOR combination of the remaining bits of this register: RSTB nor FE2 nor FE1 nor DE nor GW nor FS
6	RSTB	Reset Bit The RSTB indicates a device reset. In case this bit is set, all internal RAM Control and Configuration Registers are set to default and kept in that state until the bit is cleared. Any valid unicast frame requiring GSB in the response frame clears the Reset Bit after Responder sent its response frame. No data can be written to RAM Configuration and Control Registers as long as Reset Bit is set. Chain Initialization command will be executed, but will not clear Reset Bit.
5	x	Not used 0
4	FE2	Functional Error 2 The FE2 indicates the logical OR combination of the following errors: Any Output Channel exceeding short circuit threshold (when enabled): SHT_CHx, or Any Output Channel in open load: OL_CHx, or Any Output Channel in short circuit with GND: OUT_SHT_GND_CHx
3	FE1	Functional Error 1 The FE1 reports the following error: Thermal Shutdown: TSD
2	DE	Device error The DE indicates the logical OR combination of the following errors: Short circuit on external NTC: NTC_FAULT, or Power Good Threshold not reached: PG_NOT_VPRE_REG, or Supply voltage undervoltage fault: VS_UV, or Open or Short Circuit Fault on DAC Reference Resistor: DAC_RES_FAULT
1	GW	Global warning The GW is a logical OR combination of warning flags: Thermal Warning: TW, or NTC derating active: NTC_DER_ACT
0	FS	Fail safe: The Fail Safe bit is set, when the device operates in Fail Safe / Stand Alone Mode

The subsequent data bytes are the data transferred from the Responder device with every communication to Commander.

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6.6.4 Unicast frame – no data

If the unicast frame does not contain any data the addressed Responder will transmit the Global Status Byte.

Figure 27. Unicast frame w/o data - Commander request and Responder answer

	ID field bits														
	10	9	8	7	6	5	4	3	2	1	0				
Commander request =>	0	0	Responder ID[8:0]									CTRL	CRC	ACK/EOF	
Responder answer =>	0	1	Responder ID[8:0]									CTRL	GSB	CRC	ACK/EOF

6.6.5 Unicast frame – single RAM read

The data frame comprises 5 bytes. The MSB of the Commander request data frame contains OP Code and Address of the register. The following 4 bytes are “don´t care” data. The Responder answer contains the GSB and the register content of the register addressed by the Commander at the time of Responder answer communication start. The L99LDLH32 registers are arranged with 4 data bytes per register (see *Chapter 7*).

Figure 28. Unicast frame with single RAM read - Commander request and Responder answer

	ID field bits																
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address						
Commander request =>	0	0	Responder ID[8:0]									CTRL	"01" + Address	Do not care 3	Do not care 2	Do not care 1	Do not care 0	CRC	ACK/EOF
Responder answer =>	0	1	Responder ID[8:0]									CTRL	GSB	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	CRC	ACK/EOF

6.6.6 Unicast frame – Single RAM read & clear

The data frame comprises 5 bytes. The MSB of the Commander request data frame contains OP Code and Address of the register. The following 4 bytes specify the bits of the addressed register to be cleared. Bits to be cleared have to be set at `1 ` in the Commander request. The Responder answer contains the GSB and the register content of the register addressed by the Commander at the time of Responder answer after the execution of Clear command.

Figure 29. Unicast frame with Single RAM read and clear - Commander request and Responder answer

	ID field bits																
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address						
Commander request =>	0	0	Responder ID[8:0]									CTRL	"10" + Address	Byte 3: bits to be cleared "1"	Byte 2: bits to be cleared "1"	Byte 1: bits to be cleared "1"	Byte 0: bits to be cleared "1"	CRC	ACK/EOF
Responder answer =>	0	1	Responder ID[8:0]									CTRL	GSB	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	CRC	ACK/EOF

6.6.7 Unicast frame – single ROM read

The OPCode for this instruction is 11 “Read Device Information”. It is used for internal traceability and testing purposes and is not needed for the application.

6.6.8 Unicast frame - burst read mode RAM register

A burst read mode is supported when a Single RAM Read request is executed on a specific RAM addresses. The RAM addresses eligible to Burst Read Mode are specified in *Chapter 7*. The Responder responds to a valid Burst Read Mode RAM register command with 16 bytes of data. The 4 most significant data bytes correspond to the data stored in the

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register addressed by the Commander request. The following 12 bytes correspond to the data stored on the next 3 consecutive addresses.

Therefore the Commander request frame contains 5 data bytes, while the Responder answer frame contains 12 data bytes.

Figure 30. Unicast frame with burst read mode RAM register - Commander request and Responder answer

	ID field bits																		
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address (Status Register Addresses eligible for burst read)						
Commander request =>	0	0	Responder ID[8:0]									CTRL	"01" + Address	Do not care 3	Do not care 2	Do not care 1	Do not care 0	CRC	ACK/EOF
Responder answer =>	0	1	Responder ID[8:0]									CTRL	Data Byte 0	Data Byte 1	Data Byte 2	Data Byte 3	=>		
												=>	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7	=>		
												=>	Data Byte 8	Data Byte 9	Data Byte 10	Data Byte 11	=>		
												=>	Data Byte 12	Data Byte 13	Data Byte 14	Data Byte 15	CRC	ACK/EOF	

6.6.9 Unicast frame – single RAM write

The MSB of the Commander request data frame contains OP Code and Address of the register. The Responder answer contains only the GSB.

Figure 31. Unicast frame with single RAM write - Commander request and Responder answer

	ID field bits																		
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address						
Commander request =>	0	0	Responder ID[8:0]									CTRL	"00" + Address	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	CRC	ACK/EOF
Responder answer =>	0	1	Responder ID[8:0]									CTRL	GSB	CRC	ACK/EOF				

Therefore the Commander request frame contains 5 data bytes, while the Responder answer frame contains only one data byte.

6.6.10 Unicast frame – 3x RAM write

This instruction allows to write to 3 different RAM addresses with one CAN FD frame. Only OP Code “00” is allowed in this mode. The Commander frame request contains 16 data bytes. The MSB of the Commander request data frame contains OP Code and Address of the register, followed by 4 data bytes to be written to the addressed register. Next 5 data bytes contain again OP Code, address and data to be written. Next 5 data bytes contain again OP Code, address and data to be written. LSB is “Don´t care”. This write mode allows therefore a fast programming of configuration registers lowering the bit overhead and bus-load.

The Responder answer contains only the GSB.

Figure 32. Unicast frame with 3x RAM write - Commander request and Responder answer

	ID field bits																		
	10	9	8	7	6	5	4	3	2	1	0		OP Code + Address						
Commander request =>	0	0	Responder ID[8:0]									CTRL	"00" + Address	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	=>	
												=>	"00" + Address	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	=>	
												=>	"00" + Address	Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0	Do not care	CRC	ACK/EOF
Responder answer =>	0	1	Responder ID[8:0]									CTRL	GSB	CRC	ACK/EOF				

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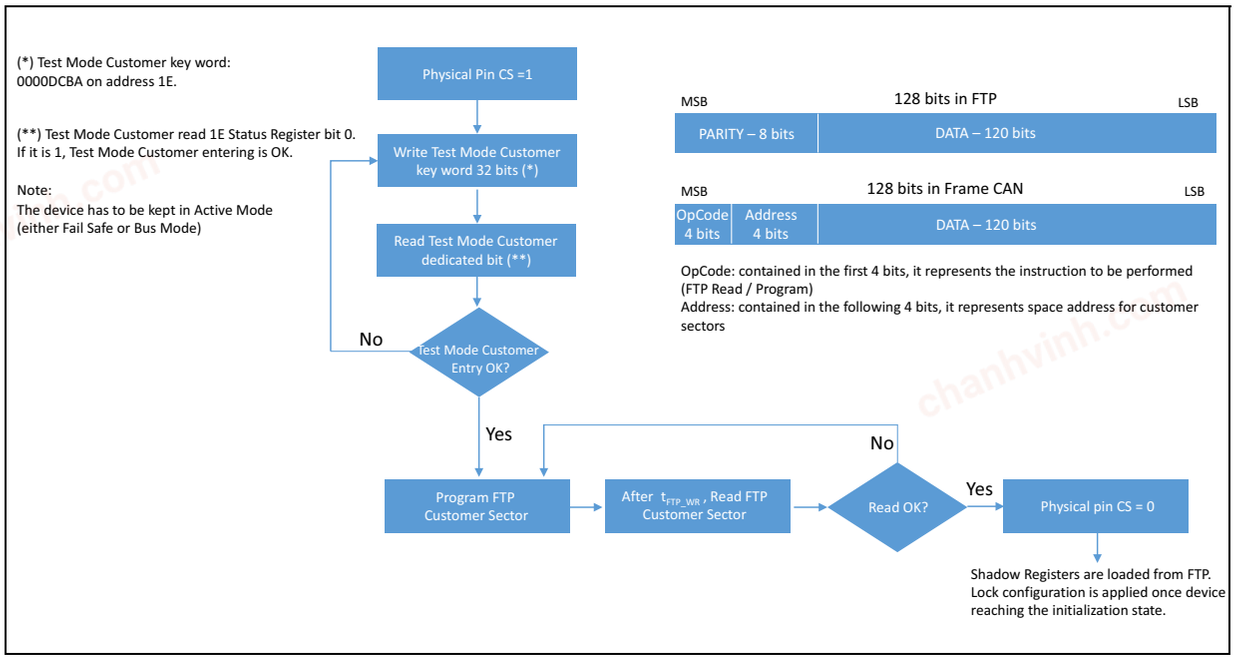
7 FTP and RAM memory mapping

The L99LDLH32 is equipped with a 2 kbits EEPROM, used also to store device configuration data. Part of this memory will be managed by the customer.

The device can operate in stand-alone mode (no microcontroller used) thanks to full configurability by FTPs. In application, the FTPs can be programmed (up to N_{FTP} cycles) via CAN FD Light compatible interface – even if the device does not integrate any counter to take note about the FTP writing cycles. By the way, for safety reason, any FTP sector can be locked to avoid unintentional writing.

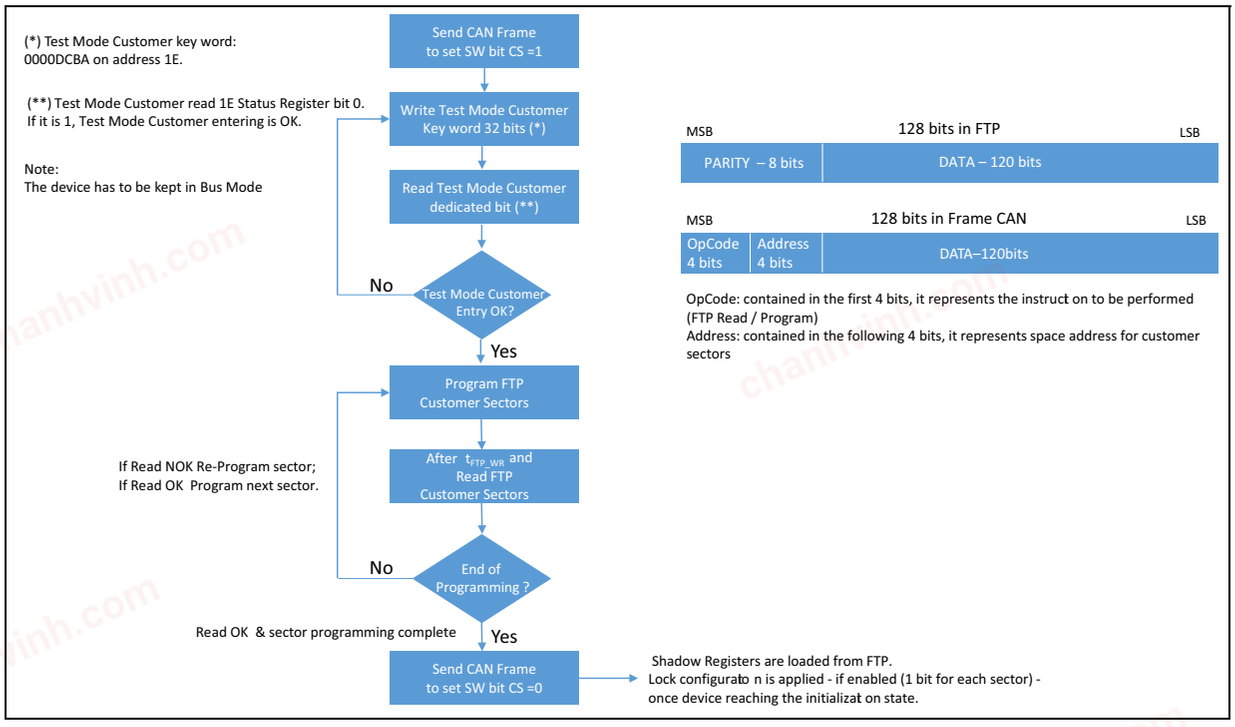
The user can program FTPs setting CS pin to “1” via HW or via SW.

Figure 33. FTP access through CAN bus - programming by physical pin CS



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Figure 34. FTP access through CAN bus - programming by setting SW bit CS



Besides FTP memory, the device is also equipped with a RAM memory type.

Here below both RAM and FTP memories mapping is reported.

Table 15. RAM memory map

Address	Name	Access	Content	Note
Configuration and Control				
00h			Not used	
01h	PWM_DUTY_ALL	Read/Write	Linear 8-bit Global PWM duty cycle	(1)
02h	PWM_DUTY_CH0_3	Read/Write/ Broadcast Write	Exponential 8-bit individual PWM duty cycle Channel 0-3	(2)
03h	PWM_DUTY_CH4_7	Read/Write/ Broadcast Write	Exponential 8-bit individual PWM duty cycle Channel 4-7	(2)
04h	PWM_DUTY_CH8_11	Read/Write/ Broadcast Write	Exponential 8-bit individual PWM duty cycle Channel 8-11	(2)
05h	PWM_DUTY_CH12_15	Read/Write/ Broadcast Write	Exponential 8-bit individual PWM duty cycle Channel 12-15	(2)
06h	PWM_DUTY_CH16_19	Read/Write/ Broadcast Write	Exponential 8-bit individual PWM duty cycle Channel 16-19	(2)
07h	PWM_DUTY_CH20_23	Read/Write/ Broadcast Write	Exponential 8-bit individual PWM duty cycle Channel 20-23	(2)
08h	PWM_DUTY_CH24-27	Read/Write/ Broadcast Write	Exponential 8-bit individual PWM duty cycle Channel 24-27	(2)

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Table 15. RAM memory map (continued)

Address	Name	Access	Content	Note
09h	PWM_DUTY_CH28-31	Read/Write/ Broadcast Write	Exponential 8-bit individual PWM duty cycle Channel 28-31	(2)
0Ah	CURR_SET_CH0_3	Read/Write/ Broadcast Write	8-bit analogue current setting Channel 0-3	(2)
0Bh	CURR_SET_CH4_7	Read/Write/ Broadcast Write	8-bit analogue current setting Channel 4-7	(2)
0Ch	CURR_SET_CH8_11	Read/Write/ Broadcast Write	8-bit analogue current setting Channel 8-11	(2)
0Dh	CURR_SET_CH12_15	Read/Write/ Broadcast Write	8-bit analogue current setting Channel 12-15	(2)
0Eh	CURR_SET_CH16_19	Read/Write/ Broadcast Write	8-bit analogue current setting Channel 16-19	(2)
0Fh	CURR_SET_CH20_23	Read/Write/ Broadcast Write	8-bit analogue current setting Channel 20-23	(2)
10h	CURR_SET_CH24_27	Read/Write/ Broadcast Write	8-bit analogue current setting Channel 24-27	(2)
11h	CURR_SET_CH28_31	Read/Write/ Broadcast Write	8-bit analogue current setting Channel 28-31	(2)
12h	DIN_MAP_CH0_15	Read/Write	Direct Input Mapping Channel 0-15	(2)
13h	DIN_MAP_CH16_31	Read/Write	Direct Input Mapping Channel 16_31	(2)
14h			not used	
15h	CONFIG_1	Read/Write	Device Configuration Register 1	(1)
16h	CONFIG_2	Read/Write	Device Configuration Register 2, Power Good thresholds VPRE_REG, Short Circuit detection thresholds	(1)
17h	CONFIG_3	Read/Write	Device Configuration Register 3	(1)
18h	CONFIG_4	Read/Write	Device Configuration Register 4, Chip Select Enable and mode transistion bits	(1)
19h	WD_TRIG	Read/Write	Watchdog trigger	(1)
Status				
1Ah	Chain_IDPOS	Read	ChainID and Position number Responder ID0 & Responder ID1	(1)
1Bh			Not used	
1Ch			Not used	
1Dh			Not used	
1Eh			Not used	

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Table 15. RAM memory map (continued)

Address	Name	Access		Content	Note
1Fh	VLED_ON_CH0_3	Burst Read from address 1Fh		8-bit Output on-state Voltage Channel 0-3	(2)
20h	VLED_ON_CH4_7		Read	8-bit Output on-state Voltage Channel 4-7	(2)
21h	VLED_ON_CH8_11		Read	8-bit Output on-state Voltage Channel 8-11	(2)
22h	VLED_ON_CH12_15		Read	8-bit Output on-state Voltage Channel 12-15	(2)
23h	VLED_ON_CH16_19	Burst Read from address 23h		8-bit Output on-state Voltage Channel 16-19	(2)
24h	VLED_ON_CH20_23		Read	8-bit Output on-state Voltage Channel 20-23	(2)
25h	VLED_ON_CH24_27		Read	8-bit Output on-state Voltage Channel 24-27	(2)
26h	VLED_ON_CH28_31		Read	8-bit Output on-state Voltage Channel 28-31	(2)
27h	OUT_STATUS_CH0_31	Burst Read from address 27h	-	Output Status Bit Channel 0-31	(2)
28h	SHT_CH0_31		Read/ Read&Clear	Short Circuit Detection Flag Channel 0-31	(2)
29h	OL_CH0_31		Read/ Read&Clear	Open Load Detection Flag Channel 0-31	(2)
2Ah	OUT_SHT_GND_CH0_31		Read/ Read&Clear	Output Shorted to Ground Detection Flag Channel 0-31	(2)
2Bh	VLEDON_RFR_CH0_31	Read		VLED_ON refresh information bit Channel 0-31	(2)
2Ch	STATUS_1	Burst Read from address 2Ch	—	Device Status Register 1, ADC voltage on Vs, VPRE_REG, Tj	(1)
2Dh	STATUS_2		Read	Device Status Register 2, Channel highest output voltage and ADC voltage on NTC	(1)
2Eh	STATUS_3		Read/ Read&Clear	Device Status Register 3, various status bits	(1)
2Fh	FTP_STATUS_1		Read	Device FTP Status 1, Read only status of various FTP configuration bits	(1)
30h	FTP_STATUS_2	Read		Device FTP Status 2, Read only status of FTP configuration Fail Safe Output Permanent Enable Channel 0-31	(2)
34h	FTP_PARITY_ERROR	Read		16 parity error bits - 1 bit per FTP Row (0=ok, 1=error)	

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Table 15. RAM memory map (continued)

Address	Name	Access		Content	Note
Reserved					
31h-3Fh (except 34h)				Reserved for ST testing and trimming	

1. Registers have to be accessed via UNICAST frames selecting Responder ID0 only. Any command to those registers with different Responder ID will be rejected.
2. Via UNICAST frames these registers can be accessed either selecting Responder ID0 or Responder ID1.

Table 16. FTP memory map

Address	Name	Access	Comment
0x0h	Row_0	Read/Write	See *Table 63*
0x1h	Row_1	Read/Write	See *Table 64*
0x2h	Row_2	Read/Write	See *Table 65*
0x3h	Row_3	Read/Write	See *Table 66*
0x4h	Row_4	Read/Write	See *Table 67*
0x5h	Row_5	Reserved	
0x6h	Row_6	Reserved	
0x7h	Row_7	Reserved	
0x8h	Row_8	Reserved	
0x9h	Row_9	Reserved	
0xAh	Row_10	Reserved	
0xBh	Row_11	Read	See *Table 68*
0xCh	Row_12	Read/Write	See *Table 69*
0xDh	Row_13	Reserved	
0xEh	Row_14	Reserved	
0xFh	Row_15	Reserved	

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7.1 RAM registers description

7.1.1 Channel PWM duty cycle

Figure 35. Channel PWM duty cycle 0x01h register

Address 01h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—								—								—								PWM_DUTY_ALL							

Table 17. Channel PWM duty cycle field description

Bit	Name	Default	Description
31-16		0000h	Not used
15-8		00h	Not used
7-1	PWM_DUTY_ALL	FTP	Linear Global PWM dimming for outputs mapped to DIN0 adjustable in 1/256 steps 00h: 0.0% 7Fh: 49.8% FFh: 100%

Figure 36. Channel PWM duty cycle 0x02h register

Address 02h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH3								PWM_DUTY_CH2								PWM_DUTY_CH1								PWM_DUTY_CH0							

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Table 18. Channel PWM duty cycle 0x02h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH3	00h	Exponential individual PWM dimming for Channel 3 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH2	00h	Exponential individual PWM dimming for Channel 2 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH1	00h	Exponential individual PWM dimming for Channel 1 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH0	00h	Exponential individual PWM dimming for Channel 0 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC

Figure 37. Channel PWM duty cycle 0x03h register

Address 03h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH7								PWM_DUTY_CH6								PWM_DUTY_CH5								PWM_DUTY_CH4							

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Table 19. Channel PWM duty cycle 0x03h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH7	00h	Exponential individual PWM dimming for Channel 7 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH6	00h	Exponential individual PWM dimming for Channel 6 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH5	00h	Exponential individual PWM dimming for Channel 5 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH4	00h	Exponential individual PWM dimming for Channel 4 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC

Figure 38. Channel PWM duty cycle 0x04h register

Address 04h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH11								PWM_DUTY_CH10								PWM_DUTY_CH9								PWM_DUTY_CH8							

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Table 20. Channel PWM duty cycle 0x04h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH11	00h	Exponential individual PWM dimming for Channel 11 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH10	00h	Exponential individual PWM dimming for Channel 10 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH9	00h	Exponential individual PWM dimming for Channel 9 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH8	00h	Exponential individual PWM dimming for Channel 8 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC

Figure 39. Channel PWM duty cycle 0x05h register

Address 05h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH15								PWM_DUTY_CH14								PWM_DUTY_CH13								PWM_DUTY_CH12							

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Table 21. Channel PWM duty cycle 0x05h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH15	00h	Exponential individual PWM dimming for Channel 15 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH14	00h	Exponential individual PWM dimming for Channel 14 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH13	00h	Exponential individual PWM dimming for Channel 13 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH12	00h	Exponential individual PWM dimming for Channel 12 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC

Figure 40. Channel PWM duty cycle 0x06h register

Address 06h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH19								PWM_DUTY_CH18								PWM_DUTY_CH17								PWM_DUTY_CH16							

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Table 22. Channel PWM duty cycle 0x06h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH19	00h	Exponential individual PWM dimming for Channel 19 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH18	00h	Exponential individual PWM dimming for Channel 18 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH17	00h	Exponential individual PWM dimming for Channel 17 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH16	00h	Exponential individual PWM dimming for Channel 16 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC

Figure 41. Channel PWM duty cycle 0x07h register

Address 07h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH23								PWM_DUTY_CH22								PWM_DUTY_CH21								PWM_DUTY_CH20							

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Table 23. Channel PWM duty cycle 0x07h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH23	00h	Exponential individual PWM dimming for Channel 23 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH22	00h	Exponential individual PWM dimming for Channel 22 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH21	00h	Exponential individual PWM dimming for Channel 21 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH20	00h	Exponential individual PWM dimming for Channel 20 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC

Figure 42. Channel PWM duty cycle 0x08h register

Address 08h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH27								PWM_DUTY_CH26								PWM_DUTY_CH25								PWM_DUTY_CH24							

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Table 24. Channel PWM duty cycle 0x08h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH27	00h	Exponential individual PWM dimming for Channel 27 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH26	00h	Exponential individual PWM dimming for Channel 26 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH25	00h	Exponential individual PWM dimming for Channel 25 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH24	00h	Exponential individual PWM dimming for Channel 24 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC

Figure 43. Channel PWM duty cycle 0x09h register

Address 09h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PWM_DUTY_CH31								PWM_DUTY_CH30								PWM_DUTY_CH29								PWM_DUTY_CH28							

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Table 25. Channel PWM duty cycle 0x09h field description

Bit	Name	Default	Description
31-24	PWM_DUTY_CH31	00h	Exponential individual PWM dimming for Channel 31 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
23-16	PWM_DUTY_CH30	00h	Exponential individual PWM dimming for Channel 30 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
15-8	PWM_DUTY_CH29	00h	Exponential individual PWM dimming for Channel 29 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC
7-0	PWM_DUTY_CH28	00h	Exponential individual PWM dimming for Channel 28 according to law embedded in *Figure 7* 00h: 0% - channel off 01h: 0,10% 7Fh: 3,09% FFh: 100% - channel on in DC

7.1.2 Channel current setting

Figure 44. Channel current setting 0x0Ah register

Address 0Ah

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CURR_SET_CH3								CURR_SET_CH2								CURR_SET_CH1								CURR_SET_CH0							

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Table 26. Channel current setting 0x0Ah field description

Bit	Name	Default	Description
31-24	CURR_SET_CH3	FTP	Linear individual analogue dimming for Channel 3 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
23-16	CURR_SET_CH2	FTP	Linear individual analogue dimming for Channel 2 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
15-8	CURR_SET_CH1	FTP	Linear individual analogue dimming for Channel 1 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
7-0	CURR_SET_CH0	FTP	Linear individual analogue dimming for Channel 0 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA

Figure 45. Channel current setting 0x0Bh register

Address 0Bh

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CURR_SET_CH7								CURR_SET_CH6								CURR_SET_CH5								CURR_SET_CH4							

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Table 27. Channel current setting 0x0Bh field description

Bit	Name	Default	Description
31-24	CURR_SET_CH7	FTP	Linear individual analogue dimming for Channel 7 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
23-16	CURR_SET_CH6	FTP	Linear individual analogue dimming for Channel 6 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
15-8	CURR_SET_CH5	FTP	Linear individual analogue dimming for Channel 5 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
7-0	CURR_SET_CH4	FTP	Linear individual analogue dimming for Channel 4 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA

Figure 46. Channel current setting 0x0Ch register

Address 0Ch

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CURR_SET_CH11								CURR_SET_CH10								CURR_SET_CH9								CURR_SET_CH8							

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Table 28. Channel current setting 0x0Ch field description

Bit	Name	Default	Description
31-24	CURR_SET_CH11	FTP	Linear individual analogue dimming for Channel 11 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
23-16	CURR_SET_CH10	FTP	Linear individual analogue dimming for Channel 10 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
15-8	CURR_SET_CH9	FTP	Linear individual analogue dimming for Channel 9 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
7-0	CURR_SET_CH8	FTP	Linear individual analogue dimming for Channel 8 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA

Figure 47. Channel current setting 0x0Dh register

Address 0Dh

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CURR_SET_CH15								CURR_SET_CH14								CURR_SET_CH13								CURR_SET_CH12							

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Table 29. Channel current setting 0x0Dh field description

Bit	Name	Default	Description
31-24	CURR_SET_CH15	FTP	Linear individual analogue dimming for Channel 15 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
23-16	CURR_SET_CH14	FTP	Linear individual analogue dimming for Channel 14 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
15-8	CURR_SET_CH13	FTP	Linear individual analogue dimming for Channel 13 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
7-0	CURR_SET_CH12	FTP	Linear individual analogue dimming for Channel 12 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA

Figure 48. Channel current setting 0x0Eh register

Address 0Eh

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CURR_SET_CH19								CURR_SET_CH18								CURR_SET_CH17								CURR_SET_CH16							

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Table 30. Channel current setting 0x0Eh field description

Bit	Name	Default	Description
31-24	CURR_SET_CH19	FTP	Linear individual analogue dimming for Channel 19 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
23-16	CURR_SET_CH18	FTP	Linear individual analogue dimming for Channel 18 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
15-8	CURR_SET_CH17	FTP	Linear individual analogue dimming for Channel 17 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
7-0	CURR_SET_CH16	FTP	Linear individual analogue dimming for Channel 16 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA

Figure 49. Channel current setting 0x0Fh register

Address 0Fh

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CURR_SET_CH23								CURR_SET_CH22								CURR_SET_CH21								CURR_SET_CH20							

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Table 31. Channel current setting 0x0Fh field description

Bit	Name	Default	Description
31-24	CURR_SET_CH23	FTP	Linear individual analogue dimming for Channel 23 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
23-16	CURR_SET_CH22	FTP	Linear individual analogue dimming for Channel 22 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
15-8	CURR_SET_CH21	FTP	Linear individual analogue dimming for Channel 21 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
7-0	CURR_SET_CH20	FTP	Linear individual analogue dimming for Channel 20 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA

Figure 50. Channel current setting 0x10h register

Address 10h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CURR_SET_CH27								CURR_SET_CH26								CURR_SET_CH25								CURR_SET_CH24							

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Table 32. Channel current setting 0x10h field description

Bit	Name	Default	Description
31-24	CURR_SET_CH27	FTP	Linear individual analogue dimming for Channel 27 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
23-16	CURR_SET_CH26	FTP	Linear individual analogue dimming for Channel 26 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
15-8	CURR_SET_CH25	FTP	Linear individual analogue dimming for Channel 25 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
7-0	CURR_SET_CH24	FTP	Linear individual analogue dimming for Channel 24 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA

Figure 51. Channel current setting 0x11h register

Address 11h

Access R/W/BW

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CURR_SET_CH31								CURR_SET_CH30								CURR_SET_CH29								CURR_SET_CH28							

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Table 33. Channel current setting 0x11h field description

Bit	Name	Default	Description
31-24	CURR_SET_CH31	FTP	Linear individual analogue dimming for Channel 31 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
23-16	CURR_SET_CH30	FTP	Linear individual analogue dimming for Channel 30 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
15-8	CURR_SET_CH29	FTP	Linear individual analogue dimming for Channel 29 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA
7-0	CURR_SET_CH28	FTP	Linear individual analogue dimming for Channel 28 in 1/256 steps 00h: 1,00 mA 01h: 1,05 mA 7Fh: 7,97 mA FFh: 15,0 mA

7.1.3 Channel mapping on DIN

Figure 52. Channel mapping on DIN 0x12h register

Address 12h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0									
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIN_MAP_CH15		DIN_MAP_CH14		DIN_MAP_CH13		DIN_MAP_CH12		DIN_MAP_CH11		DIN_MAP_CH10		DIN_MAP_CH9		DIN_MAP_CH8		DIN_MAP_CH7		DIN_MAP_CH6		DIN_MAP_CH5		DIN_MAP_CH4		DIN_MAP_CH3		DIN_MAP_CH2		DIN_MAP_CH1		DIN_MAP_CH0	

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Table 34. Channel mapping on DIN 0x12h field description

Bit	Name	Default	Description
31-30	DIN_MAP_CH15	FTP	Mapping of Channel to Direct Input 00: Channel not mapped to Direct Input 01: Channel mapped to Direct Input 10: Channel not mapped to Direct Input 11: Channel mapped to Direct Input
29-28	DIN_MAP_CH14	FTP	
27-26	DIN_MAP_CH13	FTP	
25-24	DIN_MAP_CH12	FTP	
23-22	DIN_MAP_CH11	FTP	
21-20	DIN_MAP_CH10	FTP	
19-18	DIN_MAP_CH9	FTP	
17-16	DIN_MAP_CH8	FTP	
15-14	DIN_MAP_CH7	FTP	
13-12	DIN_MAP_CH6	FTP	
11-10	DIN_MAP_CH5	FTP	
9-8	DIN_MAP_CH4	FTP	
7-6	DIN_MAP_CH3	FTP	
5-4	DIN_MAP_CH2	FTP	
3-2	DIN_MAP_CH1	FTP	
1-0	DIN_MAP_CH0	FTP	

Figure 53. Channel mapping on DIN 0x13h register

Address 13h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIN_MAP_CH31		DIN_MAP_CH30		DIN_MAP_CH29		DIN_MAP_CH28		DIN_MAP_CH27		DIN_MAP_CH26		DIN_MAP_CH25		DIN_MAP_CH24		DIN_MAP_CH23		DIN_MAP_CH22		DIN_MAP_CH21		DIN_MAP_CH20		DIN_MAP_CH19		DIN_MAP_CH18		DIN_MAP_CH17		DIN_MAP_CH16	

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Table 35. Channel mapping on DIN 0x13h field description

Bit	Name	Default	Description
31-30	DIN_MAP_CH31	FTP	Mapping of Channel to Direct Input 00: Channel not mapped to Direct Input 01: Channel mapped to Direct Input 10: Channel not mapped to Direct Input 11: Channel mapped to Direct Input
29-28	DIN_MAP_CH30	FTP	
27-26	DIN_MAP_CH29	FTP	
25-24	DIN_MAP_CH28	FTP	
23-22	DIN_MAP_CH27	FTP	
21-20	DIN_MAP_CH26	FTP	
19-18	DIN_MAP_CH25	FTP	
17-16	DIN_MAP_CH24	FTP	
15-14	DIN_MAP_CH23	FTP	
13-12	DIN_MAP_CH22	FTP	
11-10	DIN_MAP_CH21	FTP	
9-8	DIN_MAP_CH20	FTP	
7-6	DIN_MAP_CH19	FTP	
5-4	DIN_MAP_CH18	FTP	
3-2	DIN_MAP_CH17	FTP	
1-0	DIN_MAP_CH16	FTP	

7.1.4 Device configuration 1

Figure 54. Device configuration register #1

Address 15h

Access R/W

Data Byte 3								Data Byte 2				Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—					FAULT_REACT_MODE_00	—	FAULT_REACT_MODE_01	PHASE_DEV (Read Only in RAM)			OUT_DELAY	SYNC I/O_M/S	PWM_SYNC	—							PWM_FREQ_DIN			—				SHT_THR_Vpre_reg			

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Table 36. Device configuration 1 field description

Bit	Name	Default	Description
31-27		00000	Don’ t care
26	FAULT_REACT_MODE_00	FTP	Fault reaction mode Group 00: 0: Fault on one string, all strings of the same group are turned off 1: Fault on one string, no action on other strings of same Group
25		0	Don’ t care
24	FAULT_REACT_MODE_01	FTP	Fault reaction mode Group 01: 0: Fault on one string, all strings of the same group are turned off 1: Fault on one string, no action on other strings of same Group
23-21	PHASE_DEV (Read Only in RAM)	FTP	PWM phase shift in Responder mode: Phase Shift with regards to SYNC_I/O synchronized clock in 15 µs steps: 000: 0 µs 001: 15 µs 010: 30 µs ... 111: 105 µs
20	OUT_DELAY	FTP	Enable/Disable of gradual output delay: 0: gradual delay disabled 1: gradual delay enabled
19	SYNC I/O_P/C	FTP	Provider/Consumer SYNC_I/O: Synchronization of PWM frequency and phase between Provider and Consumer Devices 1: Provider Mode selected. SYNC_I/O is input. Clock frequency and phase signal on the SYNC_I/O line is used to synchronize own clock 0 (default): Provider Mode selected. SYNC_I/O is output. Device Clock frequency with scaler and phase signal is transfered to the SYNC_I/O line
18	PWM_SYNC	0	Reset bit for internal PWM counter: 0: PWM counter running 1: PWM counter reset to zero; bit is automatically cleared directly after reset
17-11		0h	Don’ t care

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Table 36. Device configuration 1 field description (continued)

Bit	Name	Default	Description
10-8	PWM_FREQ_DIN	FTP	PWM frequency for Group 01: 000: 200 Hz 001: 300 Hz 010: 400 Hz 011: 500 Hz 100: 700 Hz 101: 1000 Hz 110: 1200 Hz 111: 1400 Hz
7-4		0000	Don’ t care
3-0	SHT_THR_Vpre_reg	FTP	Short circuit detection threshold Group 00 channels mapped to VPRE_REG: Adjustable in 314 mV steps 0h: 0,31 V 1h: 0,62 V 2h: 0,94 V ... Fh: 5,02 V

7.1.5 Device configuration 2

Figure 55. Device configuration register #2

Address 16h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—												SHT_THR_VPRE_REG_DIN				—								PG_TH_VPRE_REG							

Table 37. Device configuration 2 field description

Bit	Name	Default	Description
31-20		0h	Don’ t care

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Table 37. Device configuration 2 field description (continued)

Bit	Name	Default	Description
19-16	SHT_VPRE_REG_DIN	FTP	Short circuit detection threshold Group 01 channels mapped to VPRE_REG: Adjustable in 314 mV steps 0h: 0,31 V 1h: 0,62 V 2h: 0,94 V ... Fh: 5,02 V
15-8		00h	Don’ t care
7-0	PG_TH_VPRE_REG	FTP	Power Good Threshold for VPRE_REG adjustable in 157 mV steps - from 00h to 1Ah codes the threshold value is clamped to 4 V: 1Dh: 4,55 V 32h: 7,84 V DFh: 34,88 V

7.1.6 Device configuration 3

Figure 56. Device configuration register #3

Address 17h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0									
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—		DITHERING			VNTC_TH			—	VREF_PRE_REG	—			DIN_EN	—	OL_EN	DIAG_BLANK_11		DIAG_BLANK_10		DIAG_BLANK_01		DIAG_BLANK_00		—	SHT_DET_EN	—	SHT_EN	—	SHT_OFF_00	—	SHT_OFF_01

Table 38. Device configuration 3 field description

Bit	Name	Default	Description
31-30			Not used
29-27	DITHERING	FTP	See *Table 39*
26-24	VNTC_TH	FTP	NTC voltage threshold related to the start of derating 000: 2,034 V (55°C) 001: 1,908 V (60°C) 010: 1,783 V (65°C) 011: 1,660 V (70°C) 100: 1,423 V (80°C) 101: 1,207 V (90°C) 110: 1,106 V (95°C) 111: 1,013 V (100°C)
23		0	Not used

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Table 38. Device configuration 3 field description (continued)

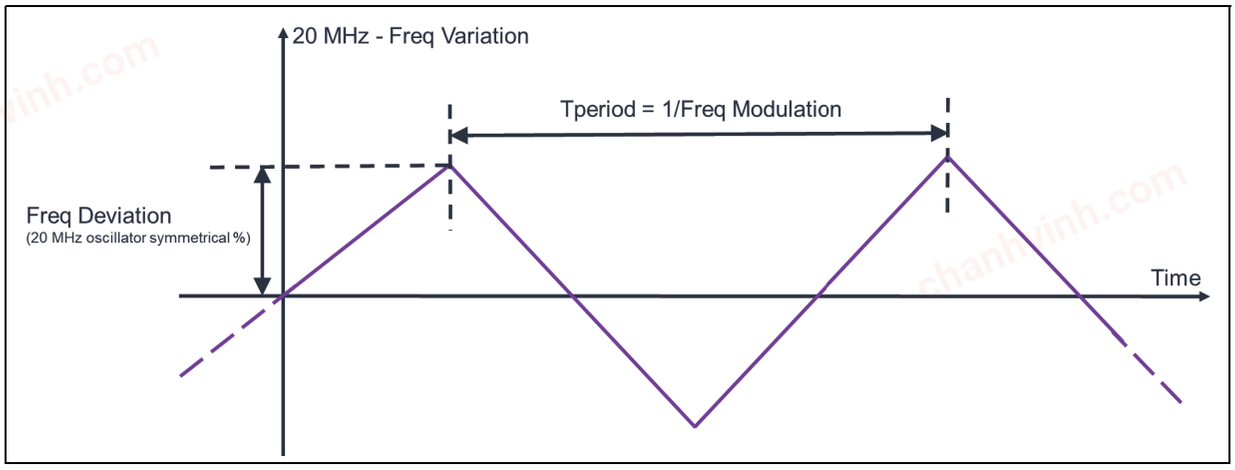
Bit	Name	Default	Description
22	VREF_PRE_REG	FTP	VREF_PRE_REG enable 0 (default): VREF_PRE_REG feedback reference voltage generation is enabled 1: VREF_PRE_REG feedback reference voltage generation is disabled
21-19		000	Don’ t care
18	DIN_EN	0	DIN enable in Bus Mode 0: DIN disabled 1: DIN enabled
17		0	Don’ t care
16	OL_EN	FTP	Enable Open load fault propagation of Group 01 on Fault pin 0: open load propagation to Fault pin disabled 1: open load propagation to Fault pin enabled
15-12		0000	Don’ t care
11-10	DIAG_BLANK_01	FTP	Diagnostic blanking time after rising edge (incl PWM) for Group 01 00: 50 µs 01: 100 µs 10: 150 µs 11: 200 µs
9-8	DIAG_BLANK_00	FTP	Diagnostic blanking time after rising edge (incl PWM) for Group 00 00: 50 µs 01: 100 µs 10: 150 µs 11: 200 µs
7		0	Don’ t care
6	SHT_DET_EN	FTP	Short circuit detection for channels mapped to VPRE_REG 0: short circuit detection disabled 1: short circuit detection enabled
5		0	Don’ t care
4	SHT_EN	FTP	Enable Short circuit fault propagation of Group 01 on Fault pin 0: Short circuit propagation to Fault pin disabled 1: short circuit propagation to Fault pin enabled
3		0	Don’ t care
2	SHT_OFF_00	FTP	Output deactivation in case of Short Circuit detection for Group 00 0: Output deactivation disabled 1: Output deactivation enabled
1		0	Don’ t care
0	SHT_OFF_01	FTP	Output deactivation in case of Short Circuit detection for Group 01 0: Output deactivation disabled 1: Output deactivation enabled

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Table 39. 20 MHz Oscillator, Dithering - Modulation Parameters

Configuration [#]	DITHERING Bit [2÷0]	Freq Modulation [kHz]	Freq Deviation [%]	Rejection [dB]
1	000	0	0	0
2	001	78	1.5	-7
3	010	39	3.2	-11.5
4	011	26	5	-14
5	100	19.5	6.5	-17
6	101	15.6	7.8	-18
7	110	13	9.7	-20
8	111	11	11.5	-21

Figure 57. 20 MHz Oscillator, Dithering - Modulation Curve



7.1.7 Device configuration 4

Figure 58. Device configuration register #4

Address 18h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0									
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Not used																													CS_EN	GOSTBY	BUSMODE

Table 40. Device configuration 4 field description

Bit	Name	Default	Description
31-3		0	Not used

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Table 40. Device configuration 4 field description (continued)

Bit	Name	Default	Description
2	CS_EN	0	Chip Select Enable to enter FTP programming mode 0: Chip Select disabled 1: Chip Select enabled
1	GOSTBY	0	See *Table 41*
0	BUSMODE	0	

Table 41. State transition bits

GOSTBY	BUSMODE	State
0	0	Reset --> Fail Safe / Stand Alone
0	1	Normal Mode / Bus Mode
1	0	Initialization --> Standby Mode
1	1	Reset --> Fail Safe / Stand Alone

7.1.8 Watchdog

Figure 59. Watchdog register

Address 19h

Access R/W

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Not used																															WD_TRIG

Table 42. Watchdog field description

Bit	Name	Default	Description
31-1		0h	Not used
0	WD_TRIG	0	Watchdog Trigger In order to keep device in Normal Mode / Bus Mode, this bit must be cyclically toggled within a period configured by WD_CONF bits to refresh the watchdog.

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7.1.9 Position and chain identifier for Responder IDx

Figure 60. Position and chain identifier for Responder IDx register

Address 1Ah

Access R

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Not used								Not used								ChainID_Responder ID1						POS_Responder ID1		ChainID_Responder ID0						POS_Responder ID0	

Table 43. Position and chain identifier for Responder IDx field description

Bit	Name	Default	Description
31-24			Not used
23-16			Not used
15-10	ChainID_Responder ID1	000000	6-bit Chain Identifier for Responder ID1
9-8	POS_Responder ID1	0	2-bit Position Identifier in Chain for Responder ID1
7-2	ChainID_Responder ID0	000000	6-bit Chain Identifier for Responder ID0
1-0	POS_Responder ID0	0	2-bit Position Identifier in Chain for Responder ID0

7.1.10 Channel output on-state voltage

Figure 61. Channel output on-state voltage 0x1Fh register

Address 1Fh

Access Burst Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH3								VLED_ON_CH2								VLED_ON_CH1								VLED_ON_CH0							

Table 44. Channel output on-state voltage 0x1Fh field description

Bit	Name	Default	Description
31-24	VLED_ON_CH3	00h	8-bit Output on-state Voltage Channel 3 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

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Table 44. Channel output on-state voltage 0x1Fh field description (continued)

Bit	Name	Default	Description
23-16	VLED_ON_CH2	00h	8-bit Output on-state Voltage Channel 2 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-8	VLED_ON_CH1	00h	8-bit Output on-state Voltage Channel 1 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
7-0	VLED_ON_CH0	00h	8-bit Output on-state Voltage Channel 0 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

Figure 62. Channel output on-state voltage 0x20h register

Address 20h

Access Burst Read from 1Fh

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH7								VLED_ON_CH6								VLED_ON_CH5								VLED_ON_CH4							

Table 45. Channel output on-state voltage 0x20h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH7	00h	8-bit Output on-state Voltage Channel 7 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
23-16	VLED_ON_CH6	00h	8-bit Output on-state Voltage Channel 6 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-8	VLED_ON_CH5	00h	8-bit Output on-state Voltage Channel 5 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

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Table 45. Channel output on-state voltage 0x20h field description (continued)

Bit	Name	Default	Description
7-0	VLED_ON_CH4	00h	8-bit Output on-state Voltage Channel 4 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

Figure 63. Channel output on-state voltage 0x21h register

Address 21h

Access Burst Read from 1Fh

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH11								VLED_ON_CH10								VLED_ON_CH9								VLED_ON_CH8							

Table 46. Channel output on-state voltage 0x21h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH11	00h	8-bit Output on-state Voltage Channel 11 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
23-16	VLED_ON_CH10	00h	8-bit Output on-state Voltage Channel 10 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-8	VLED_ON_CH9	00h	8-bit Output on-state Voltage Channel 9 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
7-0	VLED_ON_CH8	00h	8-bit Output on-state Voltage Channel 8 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

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Figure 64. Channel output on-state voltage 0x22h register

Address 22h

Access Burst Read from 1Fh

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH15								VLED_ON_CH14								VLED_ON_CH13								VLED_ON_CH12							

Table 47. Channel output on-state voltage 0x22h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH15	00h	8-bit Output on-state Voltage Channel 15 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
23-16	VLED_ON_CH14	00h	8-bit Output on-state Voltage Channel 14 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-8	VLED_ON_CH13	00h	8-bit Output on-state Voltage Channel 13 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
7-0	VLED_ON_CH12	00h	8-bit Output on-state Voltage Channel 12 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

Figure 65. Channel output on-state voltage 0x23h register

Address 23h

Access Burst Read from 23h

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH19								VLED_ON_CH18								VLED_ON_CH17								VLED_ON_CH16							

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Table 48. Channel output on-state voltage 0x23h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH19	00h	8-bit Output on-state Voltage Channel 19 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
23-16	VLED_ON_CH18	00h	8-bit Output on-state Voltage Channel 18 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-8	VLED_ON_CH17	00h	8-bit Output on-state Voltage Channel 17 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
7-0	VLED_ON_CH16	00h	8-bit Output on-state Voltage Channel 16 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

Figure 66. Channel output on-state voltage 0x24h register

Address 24h

Access Burst Read from 23h

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH23								VLED_ON_CH22								VLED_ON_CH21								VLED_ON_CH20							

Table 49. Channel output on-state voltage 0x24h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH23	00h	8-bit Output on-state Voltage Channel 23 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

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Table 49. Channel output on-state voltage 0x24h field description (continued)

Bit	Name	Default	Description
23-16	VLED_ON_CH22	00h	8-bit Output on-state Voltage Channel 22 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-8	VLED_ON_CH21	00h	8-bit Output on-state Voltage Channel 21 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
7-0	VLED_ON_CH20	00h	8-bit Output on-state Voltage Channel 20 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

Figure 67. Channel output on-state voltage 0x25h register

Address 25h

Access Burst Read from 23h

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH27								VLED_ON_CH26								VLED_ON_CH25								VLED_ON_CH24							

Table 50. Channel output on-state voltage 0x25h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH27	00h	8-bit Output on-state Voltage Channel 27 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
23-16	VLED_ON_CH26	00h	8-bit Output on-state Voltage Channel 26 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-8	VLED_ON_CH25	00h	8-bit Output on-state Voltage Channel 25 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

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Table 50. Channel output on-state voltage 0x25h field description (continued)

Bit	Name	Default	Description
7-0	VLED_ON_CH24	00h	8-bit Output on-state Voltage Channel 24 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

Figure 68. Channel output on-state voltage 0x26h register

Address 26h

Access Burst Read from 23h

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLED_ON_CH31								VLED_ON_CH30								VLED_ON_CH29								VLED_ON_CH28							

Table 51. Channel output on-state voltage 0x26h field description

Bit	Name	Default	Description
31-24	VLED_ON_CH31	00h	8-bit Output on-state Voltage Channel 31 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
23-16	VLED_ON_CH30	00h	8-bit Output on-state Voltage Channel 30 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-8	VLED_ON_CH29	00h	8-bit Output on-stateon-state Voltage Channel 29 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
7-0	VLED_ON_CH28	00h	8-bit Output on-state Voltage Channel 28 in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

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7.1.11 Channel output status

Figure 69. Channel output status register

Address 27h

Access Burst read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OUT_STATUS_CH24-31								OUT_STATUS_CH16-23								OUT_STATUS_CH8-15								OUT_STATUS_CH0-7							

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Table 52. Channel output status field description

Bit	Name	Default	Description
31	OUT_STATUS_CH31	0	Output Status bit 0: channel gate off 1: channel gate on (regardless of the PWM OFF phase)
30	OUT_STATUS_CH30	0	
29	OUT_STATUS_CH29	0	
28	OUT_STATUS_CH28	0	
27	OUT_STATUS_CH27	0	
26	OUT_STATUS_CH26	0	
25	OUT_STATUS_CH25	0	
24	OUT_STATUS_CH24	0	
23	OUT_STATUS_CH23	0	
22	OUT_STATUS_CH22	0	
21	OUT_STATUS_CH21	0	
20	OUT_STATUS_CH20	0	
19	OUT_STATUS_CH19	0	
18	OUT_STATUS_CH18	0	
17	OUT_STATUS_CH17	0	
16	OUT_STATUS_CH16	0	
15	OUT_STATUS_CH15	0	
14	OUT_STATUS_CH14	0	
13	OUT_STATUS_CH13	0	
12	OUT_STATUS_CH12	0	
11	OUT_STATUS_CH11	0	
10	OUT_STATUS_CH10	0	
9	OUT_STATUS_CH9	0	
8	OUT_STATUS_CH8	0	
7	OUT_STATUS_CH7	0	
6	OUT_STATUS_CH6	0	
5	OUT_STATUS_CH5	0	
4	OUT_STATUS_CH4	0	
3	OUT_STATUS_CH3	0	
2	OUT_STATUS_CH2	0	
1	OUT_STATUS_CH1	0	
0	OUT_STATUS_CH0	0	

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7.1.12 Channel short circuit status

Figure 70. Channel short circuit status register

Address 28h

Access Burst Read from 27h / Read / Read & Clear

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SHT_CH24-31								SHT_CH16-23								SHT_CH8-15								SHT_CH0-7							

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Table 53. Channel short circuit status field description

Bit	Name	Default	Description
31	SHT_CH31	0	Short Circuit Status bit 0: no fault on channel 1: fault validated on channel All the SHT_CHx bits are Read & Clear bits - after their latch, a Clear command needs to be unlatched.
30	SHT_CH30	0	
29	SHT_CH29	0	
28	SHT_CH28	0	
27	SHT_CH27	0	
26	SHT_CH26	0	
25	SHT_CH25	0	
24	SHT_CH24	0	
23	SHT_CH23	0	
22	SHT_CH22	0	
21	SHT_CH21	0	
20	SHT_CH20	0	
19	SHT_CH19	0	
18	SHT_CH18	0	
17	SHT_CH17	0	
15	SHT_CH15	0	
14	SHT_CH14	0	
13	SHT_CH13	0	
12	SHT_CH12	0	
11	SHT_CH11	0	
10	SHT_CH10	0	
9	SHT_CH9	0	
8	SHT_CH8	0	
7	SHT_CH7	0	
6	SHT_CH6	0	
5	SHT_CH5	0	
4	SHT_CH4	0	
3	SHT_CH3	0	
2	SHT_CH2	0	
1	SHT_CH1	0	
0	SHT_CH0	0	

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7.1.13 Channel open load status

Figure 71. Channel open load status register

Address 29h

Access Burst Read from 27h / Read / Read & Clear

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OL_CH24-31								OL_CH16-23								OL_CH8-15								OL_CH0-7							

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Table 54. Channel open load status field description

Bit	Name	Default	Description
31	OL_CH31	0	Open Load Status bit 0: no fault on channel 1: fault validated on channel All the OL_CHx bits are Read & Clear bits - after their latch, a Clear command needs to be unlatched.
30	OL_CH30	0	
29	OL_CH29	0	
28	OL_CH28	0	
27	OL_CH27	0	
26	OL_CH26	0	
25	OL_CH25	0	
24	OL_CH24	0	
23	OL_CH23	0	
22	OL_CH22	0	
21	OL_CH21	0	
20	OL_CH20	0	
19	OL_CH19	0	
18	OL_CH18	0	
17	OL_CH17	0	
16	OL_CH16	0	
15	OL_CH15	0	
14	OL_CH14	0	
13	OL_CH13	0	
12	OL_CH12	0	
11	OL_CH11	0	
10	OL_CH10	0	
9	OL_CH9	0	
8	OL_CH8	0	
7	OL_CH7	0	
6	OL_CH6	0	
5	OL_CH5	0	
4	OL_CH4	0	
3	OL_CH3	0	
2	OL_CH2	0	
1	OL_CH1	0	
0	OL_CH0	0	

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7.1.14 Channel short to GND

Figure 72. Channel short to GND register

Address 2Ah

Access Read/Read and Clear

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OUT_SHT_GND_CH24-31								OUT_SHT_GND_CH16-23								OUT_SHT_GND_CH8-15								OUT_SHT_GND_CH0-7							

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Table 55. Channel short to GND field description

Bit	Name	Default	Description
31	OUT_SHT_GND_CH31	0	Output Short to GND bit 0: no fault on channel 1: fault validated on channel All the OUT_SHT_GND_CHx bits are Read & Clear bits - after their latch, a Clear command needs to be unlatched.
30	OUT_SHT_GND_CH30	0	
29	OUT_SHT_GND_CH29	0	
28	OUT_SHT_GND_CH28	0	
27	OUT_SHT_GND_CH27	0	
26	OUT_SHT_GND_CH26	0	
25	OUT_SHT_GND_CH25	0	
24	OUT_SHT_GND_CH24	0	
23	OUT_SHT_GND_CH23	0	
22	OUT_SHT_GND_CH22	0	
21	OUT_SHT_GND_CH21	0	
20	OUT_SHT_GND_CH20	0	
19	OUT_SHT_GND_CH19	0	
18	OUT_SHT_GND_CH18	0	
17	OUT_SHT_GND_CH17	0	
16	OUT_SHT_GND_CH16	0	
15	OUT_SHT_GND_CH15	0	
14	OUT_SHT_GND_CH14	0	
13	OUT_SHT_GND_CH13	0	
12	OUT_SHT_GND_CH12	0	
11	OUT_SHT_GND_CH11	0	
10	OUT_SHT_GND_CH10	0	
9	OUT_SHT_GND_CH9	0	
8	OUT_SHT_GND_CH8	0	
7	OUT_SHT_GND_CH7	0	
6	OUT_SHT_GND_CH6	0	
5	OUT_SHT_GND_CH5	0	
4	OUT_SHT_GND_CH4	0	
3	OUT_SHT_GND_CH3	0	
2	OUT_SHT_GND_CH2	0	
1	OUT_SHT_GND_CH1	0	
0	OUT_SHT_GND_CH0	0	

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7.1.15 Channel VLEDON ADC status refresh

Figure 73. Channel VLEDON ADC status refresh register

Address 2Bh

Access Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VLEDON_RFR_CH24-31								VLEDON_RFR_CH16-23								VLEDON_RFR_CH8-15								VLEDON_RFR_CH0-7							

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Table 56. Channel VLEDON ADC status refresh field description

Bit	Name	Default	Description
31	VLEDON_RFR_CH31	0	VLEDON ADC Status Refresh bit 0: VLEDON ADC result not updated since last reading 1: VLEDON ADC result updated since last reading
30	VLEDON_RFR_CH30	0	
29	VLEDON_RFR_CH29	0	
28	VLEDON_RFR_CH28	0	
27	VLEDON_RFR_CH27	0	
26	VLEDON_RFR_CH26	0	
25	VLEDON_RFR_CH25	0	
24	VLEDON_RFR_CH24	0	
23	VLEDON_RFR_CH23	0	
22	VLEDON_RFR_CH22	0	
21	VLEDON_RFR_CH21	0	
20	VLEDON_RFR_CH20	0	
19	VLEDON_RFR_CH19	0	
18	VLEDON_RFR_CH18	0	
17	VLEDON_RFR_CH17	0	
16	VLEDON_RFR_CH16	0	
15	VLEDON_RFR_CH15	0	
14	VLEDON_RFR_CH14	0	
13	VLEDON_RFR_CH13	0	
12	VLEDON_RFR_CH12	0	
11	VLEDON_RFR_CH11	0	
10	VLEDON_RFR_CH10	0	
9	VLEDON_RFR_CH9	0	
8	VLEDON_RFR_CH8	0	
7	VLEDON_RFR_CH7	0	
6	VLEDON_RFR_CH6	0	
5	VLEDON_RFR_CH5	0	
4	VLEDON_RFR_CH4	0	
3	VLEDON_RFR_CH3	0	
2	VLEDON_RFR_CH2	0	
1	VLEDON_RFR_CH1	0	
0	VLEDON_RFR_CH0	0	

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7.1.16 Device status 1

Figure 74. Device status register #1

Address 2Ch

Access Burst Read from 2Ch

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Tj								—								VPRE_REG								VS							

Table 57. Device status 1 field description

Bit	Name	Default	Description
31-24	Tj	00h	8-bit Value of junction temperature in 1/256 steps 6Bh: 175°C 82h: 140°C A6h: 85°C CCh: 25°C F7h: -40°C
23-16		00h	Don’ t care
15-8	VPRE_REG	00h	8-bit Voltage of VPRE_REG in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
7-0	VS	00h	8-bit Voltage of VS in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V

7.1.17 Device status 2

Figure 75. Device status register #2

Address 2Dh

Access Burst Read from 2Ch

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
NTC_ADC								VLEDON_LOW								—															

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Table 58. Device status 2 field description

Bit	Name	Default	Description
31-24	NTC_ADC	00h	8-bit Voltage of NTC in 1/256 steps 00h: 0 mV 01h: 10 mV 7Fh: 1,25 V FFh: 2,50 V
23-16	VLEDON_LOW	00h	8-bit value of highest Output on-state Voltage of an active channel in 1/256 steps 00h: 0 mV 01h: 157 mV 7Fh: 19,9 V FFh: 40 V
15-0		00h	Not used

7.1.18 Device status 3

Figure 76. Device status register #3

Address 2Eh

Access Burst Read from 2Ch/Read/Read and Clear

Data Byte 3								Data Byte 2							Data Byte 1							Data Byte 0									
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—														VREF_PRE_REG_MAX	DAC_RES_FAULT	WD_FAIL	VS_UV	WD_STATUS		—	DIN_STATUS	NTC_FAULT	NTC_DER_ACT	OR_OL	OR_SHT	OR_OUT_STATUS	OR_OUT_SHT_GND	TW	TDS	—	PG_NOT_VPRE_REG

Table 59. Device status 3 field description

Bit	Name	Default	Description
31-18		0h	Not used
17	VREF_PRE_REG_MAX	0	Reference Voltage feedback Preregulator: 0: reference voltage is not set to maximum level 1: reference voltage is set to maximum level
16	DAC_RES_FAULT	0	External DAC Reference Resistor Fault: 0: No fault on external DAC Reference Resistor 1: Open or Short Circuit fault on external DAC Reference Resistor (FAULT pin is pulled low)

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Table 59. Device status 3 field description (continued)

Bit	Name	Default	Description
15	WD_FAIL	0	Watchdog fail: 0: Watchdog Trigger bit toggled within WD_CONF timeout period - watchdog fail 1: Watchdog Trigger bit not toggled within WD_CONF timeout period - devices enters Fail Safe / Stand Alone Mode WD_FAIL bit is Read & Clear bit - after its latch, a Clear command needs to be unlatched.
14	VS_UV	0	VS undervoltage Fault bit: 0: VS>VS_UV 1: VS<VS_UV
13-12	WD_STATUS	00	Watchdog Status bits: 00: 0% < Timer status < 24% 01: 24% < Timer status < 50% 01: 50% < Timer status < 74% 11: Timer Status > 74%
11		0	Not used
10	DIN_STATUS	0	Direct Input Status bit: 0: low logical level at DIN 1: high logical level at DIN
9	NTC_FAULT	0	NTC Fault Status bit: 0: no short circuit fault detected on NTC: $V_{NTC} > V_{NTC_SHT}$ 1: short circuit fault detected on NTC: $V_{NTC} < V_{NTC_SHT}$
8	NTC_DER_ACT	0	NTC Derating Active bit Status bit: 0: $V_{NTC} > V_{NTC_TH}$, no derating active 1: $V_{NTC} < V_{NTC_TH}$, NTC derating active
7	OR_OL	0	OR combination of all channels´ Open Load Status Flags: 0: no open load is present on any active channel 1: open load present on an active channel
6	OR_SHT	0	OR combination of all channels´ Short Circuit Status Flags: 0: no short circuit is present on any active channel 1: short circuit present on an active channel
5	OR_OUT_STATUS	0	OR combination of all channels´ Output Status Flags: 0: all output gate drivers are inactive 1: at least one output gate driver is active
4	OR_OUT_SHT_GND	0	OR combination of all channels´ Output Short to GND Status Flags: 0: no short circuit to GND is present on any active channel 1: short circuit to GND is present on any active channel
3	TW	0	Thermal Warning Status bit: 0: $T_J < T_{TW} - T_{TW_HYS}$, thermal warning not active 1: $T_J > T_{TW}$, thermal warning active

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Table 59. Device status 3 field description (continued)

Bit	Name	Default	Description
2	TSD	0	Thermal Shutdown Status bit: 0: T_J < T_TSD - T_TSD_HYS, thermal shutdown not active, device not in autorestart thermal cycling 1: T_J > T_TSD - T_TSD_HYS, thermal shutdown active, device in autorestart thermal cycling
1		0	Not used
0	PG_NOT_VPRE_REG(1)	1	Power Good Threshold Status bit VPRE_REG: 0: VPRE_REG < PG_TH_VPRE_REG, Power good threshold reached on VPRE_REG 1: VPRE_REG > PG_TH_VPRE_REG, Power good threshold not reached on VPRE_REG

1. Whenever PG_NOT_VPRE_REG is set, the application shall temporarily deactivate the Pre-regulator control algorithm, by two consecutive UNICAST WRITE frames to disable and enable VREF_PRE_REG bit (bit 22 of *Chapter 7.1.6*).

7.1.19 FTP status 1

Figure 77. FTP status register #1

Address 2Fh

Access Burst Read from 2Ch

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—										POR_DELAY		WD_CONF		—	PWM_FS_ALL_EN	—								PWM_DUTY_ALL_ALT							

Table 60. FTP status 1 field description

Bit	Name	Default	Description
31-22			Not used
21-20	POR_DELAY	00	Power on Reset Delay Time t_POR_DELAY; delay time before activating outputs in Fail Safe / Stand alone mode after POR 00: 0 ms 01: 25 ms 10: 50 ms 11: 100 ms
19-18	WD_CONF	00	Watchdog timeout period tWD 00: 50 ms 01: 100 ms 10: 200 ms 11: 25 ms

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Table 60. FTP status 1 field description (continued)

Bit	Name	Default	Description
17		0	Not used
16	PWM_FS_ALL_EN	0	Enable bit of internal PWM dimming in Fail Safe / Stand Alone Mode for Group 01: 0: internal PWM dimming disabled 1: internal PWM dimming enabled (PWM_DUTY_ALL FTP value with PWM_FREQ_DIN FTP Value)
15-8		00h	Not used
7-0	PWM_DUTY_ALL_ALT	00h	Linear alternative Global PWM duty cycle for outputs mapped to DIN adjustable in 1/256 steps 00h: 0.4% 7Fh: 50.0% FFh: 100%

7.1.20 FTP status 2

Figure 78. FTP status register #2

Address 30h

Access Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FS_OUT_EN31-24								FS_OUT_EN23-16								FS_OUT_EN15-8								FS_OUT_EN7-0							

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Table 61. FTP status 2 field description

Bit	Name	Default	Description
31	FS_OUT_EN_CH31	0	Output permanent on enable bit in Fail Safe / Stand Alone Mode 0: Output permanent on disabled 1: Output permanent on enabled
30	FS_OUT_EN_CH30	0	
29	FS_OUT_EN_CH29	0	
28	FS_OUT_EN_CH28	0	
27	FS_OUT_EN_CH27	0	
26	FS_OUT_EN_CH26	0	
25	FS_OUT_EN_CH25	0	
24	FS_OUT_EN_CH24	0	
23	FS_OUT_EN_CH23	0	
22	FS_OUT_EN_CH22	0	
21	FS_OUT_EN_CH21	0	
20	FS_OUT_EN_CH20	0	
19	FS_OUT_EN_CH19	0	
18	FS_OUT_EN_CH18	0	
117	FS_OUT_EN_CH17	0	
16	FS_OUT_EN_CH16	0	
15	FS_OUT_EN_CH15	0	
14	FS_OUT_EN_CH14	0	
13	FS_OUT_EN_CH13	0	
12	FS_OUT_EN_CH12	0	
11	FS_OUT_EN_CH11	0	
10	FS_OUT_EN_CH10	0	
9	FS_OUT_EN_CH9	0	
8	FS_OUT_EN_CH8	0	
7	FS_OUT_EN_CH7	0	
6	FS_OUT_EN_CH6	0	
5	FS_OUT_EN_CH5	0	
4	FS_OUT_EN_CH4	0	
3	FS_OUT_EN_CH3	0	
2	FS_OUT_EN_CH2	0	
1	FS_OUT_EN_CH1	0	
0	FS_OUT_EN_CH0	0	

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7.1.21 FTP parity error status register

Figure 79. FTP parity error status register

Address 34h

Access Read

Data Byte 3								Data Byte 2								Data Byte 1								Data Byte 0							
bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved		Row 15	Row 14	Row 13	Row 12	Row 11	Row 10	Row 9	Row 8	Row 7	Row 6	Row 5	Row 4	Row 3	Row 2	Row 1	Row 0	Reserved													

Table 62. FTP parity error status field description

Bit	Name	Default	Description
31-30	Reserved		
29	Row 29	0	Parity Error bits - 1 bit per FTP Row 0: NO Error 1: Error Parity Error bits should be read back after POR during application initialization together with a read-back of all Current Setting registers and Configuration #2 register. If Current Setting and Configuration registers content is unequal x00000000h and parity error map from register 34h is x00h, the NVM content was downloaded correctly to the RAM registers. This check is recommended for ASIL applications.
28	Row 28	0	
27	Row 27	0	
26	Row 26	0	
25	Row 25	0	
24	Row 24	0	
23	Row 23	0	
22	Row 22	0	
21	Row 21	0	
20	Row 20	0	
19	Row 19	0	
18	Row 18	0	
17	Row 17	0	
16	Row 16	0	
15	Row 15	0	
14	Row 14	0	
13-0	Reserved		

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7.2 FTP Rows description

7.2.1 Device FTP Configuration - Row_0

Figure 80. Device FTP Configuration - Row_0

Address 0x0h

Access R/W

Data Byte 15								.....	Data Byte 0							
bit 127	bit 126	bit 125	bit 124	bit 123	bit 122	bit 121	bit 120		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved									Responder ID0							

Table 63. Row_0

Bit	Name(1)	Default	Description
127-29	Reserved		
28	Lock_Row_12	0	0: Row_12 unlocked (R/W access) 1: Row_12 locked (R only access)
27-21	Reserved		
20-16	Lock_Row_x	0	0: Row_x unlocked (R/W access) 1: Row_x locked (R only access)
15-10	Reserved		
9	Lock_Responder ID	0	0: Responder ID unlocked (R/W access) 1: Responder ID locked (R only access)
8-0	Responder ID0	0	

1. All lock bits are one time programmable only - once programmed to 1, they cannot be reverted back to 0.

7.2.2 Device FTP Configuration - Row_1

Figure 81. Device FTP Configuration - Row_1

Address 0x1h

Access R/W

Data Byte 15								.....	Data Byte 0							
bit 127	bit 126	bit 125	bit 124	bit 123	bit 122	bit 121	bit 120		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved									CURR_SET_CH <0-7> (first 8 bits out of 64 bits in total)							

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Table 64. Row_1

Bit	Name	Default	Description
127-108	Reserved		
107-104	STH_THR_Vpre_reg_DIN	0	Short circuit detection threshold Group 1 channels mapped to VPRE_REG: Adjustable in 314 mV steps 0h: 0.31 V 1h: 0.62 V 2h: 0.94 V ... Fh: 5.02V
103-100	Reserved		
99-96	STH_THR_Vpre_reg	0	Short circuit detection threshold Group 0 channels mapped to VPRE_REG: Adjustable in 314 mV steps 0h: 0.31 V 1h: 0.62 V 2h: 0.94 V ... Fh: 5.02V
95-80	DIN_MAP_CH <0-7>	0	0: OUTx NOT mapped 1: OUTx mapped on DIN
79-72	FS_OUT_EN7_0	0	0: OUTx according to DIN_MAP_CHx 1: OUTx permanently ON
71-64	Reserved		
63-0	CURR_SET_CH <0-7>	0	Linear individual analogue dimming for Channels 0-7 in 1/256 steps 00h: 1.00 mA 01h: 1.05 mA 7Fh: 7.97 mA FFh: 15.00 mA

7.2.3 Device FTP Configuration - Row_2

Figure 82. Device FTP Configuration - Row_2

Address 0x2h

Access R/W

Data Byte 15								.....	Data Byte 0							
bit 127	bit 126	bit 125	bit 124	bit 123	bit 122	bit 121	bit 120		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved									CURR_SET_CH <8-15> (first 8 bits out of 64 bits in total)							

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Table 65. Row_2

Bit	Name	Default	Description
127-96	Reserved		
95-80	DIN_MAP_CH <8-15>	0	0: OUTx NOT mapped 1: OUTx mapped on DIN
79-72	FS_OUT_EN15_8	0	0: OUTx according to DIN_MAP_CHx 1: OUTx permanently ON
71-64	Reserved		
63-0	CURR_SET_CH <8-15>	0	Linear individual analogue dimming for Channels 8-15 in 1/256 steps 00h: 1.00 mA 01h: 1.05 mA 7Fh: 7.97 mA FFh: 15.00 mA

7.2.4 Device FTP Configuration - Row_3

Figure 83. Device FTP Configuration - Row_3

Address 0x3h

Access R/W

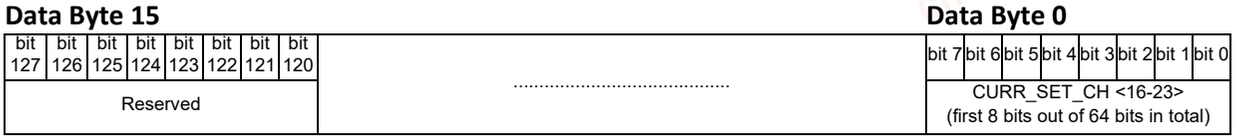


Table 66. Row_3

Bit	Name	Default	Description
127-96	Reserved		
95-80	DIN_MAP_CH <16-23>	0	0: OUTx NOT mapped 1: OUTx mapped on DIN
79-72	FS_OUT_EN23_16	0	0: OUTx according to DIN_MAP_CHx 1: OUTx permanently ON
71-64	Reserved		
63-0	CURR_SET_CH <16-23>	0	Linear individual analogue dimming for Channels 16-23 in 1/256 steps 00h: 1.00 mA 01h: 1.05 mA 7Fh: 7.97 mA FFh: 15.00 mA

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7.2.5 Device FTP Configuration - Row_4

Figure 84. Device FTP Configuration - Row_4

Address 0x4h

Access R/W

Data Byte 15								.....	Data Byte 0							
bit 127	bit 126	bit 125	bit 124	bit 123	bit 122	bit 121	bit 120		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved									CURR_SET_CH <24-31> (first 8 bits out of 64 bits in total)							

Table 67. Row_4

Bit	Name	Default	Description
127-96	Reserved		
95-80	DIN_MAP_CH <24-31>	0	0: OUTx NOT mapped 1: OUTx mapped on DIN
79-72	FS_OUT_EN31_24	0	0: OUTx according to DIN_MAP_CHx 1: OUTx permanently ON
71-64	Reserved		
63-0	CURR_SET_CH <24-31>	0	Linear individual analogue dimming for Channels 24-31 in 1/256 steps 00h: 1.00 mA 01h: 1.05 mA 7Fh: 7.97 mA FFh: 15.00 mA

7.2.6 Device FTP Configuration - Row_11

Figure 85. Device FTP Configuration - Row_11

Address 0xBh

Access R

Data Byte 15								.....	Data Byte 0							
bit 127	bit 126	bit 125	bit 124	bit 123	bit 122	bit 121	bit 120		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved									Encrypted Traceability Code (first 8 bits out of 120 bits in total)							

Table 68. Row_11

Bit	Name	Default	Description
127-120	Reserved		
119-0	ENCRYPTED TRACEABILITY CODE - 120 bits	0	Traceability Code - Read Only

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7.2.7 Device FTP Configuration - Row_12

Figure 86. Device FTP Configuration - Row_12

Address 0xCh

Access R/W

Data Byte 15										Data Byte 0								
bit 127	bit 126	bit 125	bit 124	bit 123	bit 122	bit 121	bit 120	.....		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved										PWM_DUTY_ALL								

Table 69. Row_12

Bit	Name	Default	Description
127-120	Reserved		
119-117	DITHERING	0	See *Table 39*
116-112	CAN SAMPLING POINT	0	See *Table 70*
111-104	Reserved		
103-96	PG_TH_VPRE_REG	0	Power Good Threshold for VPRE_REG adjustable in 157 mV steps (as in the RAM, see *Table 37*)
95-93	Reserved		
92	SYNC_I/O_M/S	0	Commander/Responder SYNC_I/O: Synchronization of PWM frequency and phase between Commander and Responder Devices 1: Responder Mode selected. SYNC_I/O is input. Clock frequency and phase signal on the SYNC_I/O line is used to synchronize own clock 0 (default): Commander Mode selected. SYNC_I/O is output. Device Clock frequency with scaler and phase signal is transfered to the SYNC_I/O line
91-90	POR_DELAY	0	Power on Reset Delay Time t_POR_DELAY; delay time before activating outputs in Fail Safe / Stand alone mode after POR 00: 0 ms 01: 25 ms 10: 50 ms 11: 100 ms
89	Reserved		
88	STH_DET_EN	0	Short circuit detection for channels mapped to VPRE_REG 0: short circuit detection disabled 1: short circuit detection enabled

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Table 69. Row_12 (continued)

Bit	Name	Default	Description
87-86	WD_CONF	0	Watchdog timeout period t_WD 00: 50 ms 01: 100 ms 10: 200 ms 11: 25 ms
85	VREF_PRE_REG	0	VREF_PRE_REG enable 0 (default): VREF_PRE_REG feedback reference voltage generation is enabled 1: VREF_PRE_REG feedback reference voltage generation is disabled
84-83	Reserved		
82-80	VNTC_TH	0	NTC voltage threshold related to the start of derating 000: 2,034 V (55 °C) 001: 1,908 V (60 °C) 010: 1,783 V (65 °C) 011: 1,660 V (70 °C) 100: 1,423 V (80 °C) 101: 1,207 V (90 °C) 110: 1,106 V (95 °C) 111: 1,013 V (100 °C)
79-72	Reserved		
71-69	PWM_FREQ_DIN	0	PWM frequency: 000: 200 Hz 001: 300 Hz 010: 400 Hz 011: 500 Hz 100: 700 Hz 101: 1000 Hz 110: 1200 Hz 111: 1400 Hz
68	OL_EN	0	Enable Open load fault propagation of Group 1 on Fault pin 0: open load propagation to Fault pin disabled 1: open load propagation to Fault pin enabled
67-66	Reserved		
65	FAULT_REACT_MODE_01	0	Fault reaction mode Group 01: 0: Fault on one string, all strings of the same group are turned off 1: Fault on one string, no action on other strings of same Group

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Table 69. Row_12 (continued)

Bit	Name	Default	Description
64	FAULT_REACT_MODE_00	0	Fault reaction mode Group 00: 0: Fault on one string, all strings of the same group are turned off 1: Fault on one string, no action on other strings of same Group
63-56	Reserved		
55	SHT_EN	0	Enable Short circuit fault propagation of Group 1 on Fault pin 0: Short circuit propagation to Fault pin disabled 1: short circuit propagation to Fault pin enabled
54	SHT_OFF_01	0	Output deactivation in case of Short Circuit detection for Group 01: 0: Output deactivation disabled 1: Output deactivation enabled
53	SHT_OFF_00	0	Output deactivation in case of Short Circuit detection for Group 00 0: Output deactivation disabled 1: Output deactivation enabled
52-44	Reserved		
43-42	DIAG_BLANK_01	0	Diagnostic blanking time after rising edge (included PWM) for Group 01: 00: 50 µs 01: 100 µs 10: 150 µs 11: 200 µs
41-40	DIAG_BLANK_00	0	Diagnostic blanking time after rising edge (included PWM) for Group 00 00: 50 µs 01: 100 µs 10: 150 µs 11: 200 µs
39-37	PHASE_DEV	0	PWM phase shift in Responder mode: Phase Shift with regards to SYNC_I/O synchronized clock in 15 µs steps: 000: 0 µs 001: 15 µs 010: 30 µs ... 111: 105 µs
36	OUT_DELAY	0	Enable/Disable of gradual output delay: 0: gradual delay disabled 1: gradual delay enabled
35-33	Reserved		

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Table 69. Row_12 (continued)

Bit	Name	Default	Description
32	PWM_FS_ALL_EN	0	Enable bit of internal PWM dimming in Fail Safe / Stand Alone Mode for Group 01: 0: internal PWM dimming disabled 1: internal PWM dimming enabled (PWM_DUTY_ALL FTP value with PWM_FREQ_DIN FTP Value)
31-16	Reserved		
15-8	PWM_DUTY_ALL_ALT	0	Alternative Exponential global PWM dimming for outputs mapped to DIN (only applicable in Fail Safe mode, see formula at page 27)
7-0	PWM_DUTY_ALL	0	Exponential global PWM dimming for outputs mapped to DIN in Fail Safe mode (see formula at pag. 27). Default values of Linear global PWM dimming for outputs mapped to DIN in Normal/Bus mode adjustable in 1/256 steps 00h: 0.0% 7Fh: 49.8% FFh: 100%

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Table 70. CAN bit sampling point

CAN sampling point FTP value [hex]	CAN sampling point [%]
00	53.1
01	50.0
02	46.9
03	43.8
04	40.6
05	37.5
06	34.4
07	31.3
08	28.1
09	25.0
0A	21.9
0B	18.8
0C	15.6
0D	12.5
0E	9.4
0F	Not supported
10	Not supported
11	Not supported
12	Not supported
13	93.8
14	90.6
15	87.5
16	84.4
17	81.3
18	78.1
19	75.0
1A	71.9
1B	68.8
1C	65.6
1D	62.5
1E	59.4
1F	56.3

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8 Electrical characteristics

Unless otherwise specified, the operating battery voltage and junction temperature ranges are 5.5 V < VS < 28 V, -40 °C < Tj < 150 °C.

The device is still operative and functional at higher temperatures (up to 175°C). Voltages are referred to ground and currents are assumed positive when the current flows into the pin.

The device is operated in the specified operating range, unless otherwise specified.

Note: Parameter limits at temperatures higher than 150 °C may change with respect to what is specified as per the standard temperature range. Device functionality at high temperature is guaranteed by characterization.

8.1 Absolute maximum ratings

Stressing the device above the "Absolute maximum ratings" may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Table 71. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Input supply pin of the IC	-0.3 ÷ 40	V
V_{OUT_X}	Output Pin for CHx (x=0÷31)	-0.3 ÷ V_{PRE_REG}	
V_{PRE_REG}	Pre-Regulator (external) Voltage	0 ÷ 35	
V_{5V}	5V Regulator (internal) output voltage	-0.3 ÷ 7	
V_{3V3}	3V3 Regulator (internal) output voltage	-0.3 ÷ 4.6	
V_{NTC}	NTC analog input voltage	-0.3 ÷ V_{3V3}+0.3	
V_{DIN}	Direct input pin voltage	-0.3 ÷ V_{5V}+0.3	
V_{FAULT}	Diagnostic I/O pin voltage	-0.3 ÷ V_{3V3}+0.3	
$V_{SYNC_I/O}$	Synchronization I/O pin voltage	-0.3 ÷ V_{3V3}+0.3	
V_{CAN_H}, V_{CAN_L}	Can bus terminal voltage	-27 ÷ 40	
V_{CANH} - V_{CANL}	Differential CAN-Bus voltage	-5 to +10	
V_{CS}	Chip select input pin voltage	-0.3 ÷ 7	
V_{TEST}	Test pin voltage	-0.3 ÷ V_{3V3}+0.3	
$V_{REF_PRE_REG}$	Reference pin (for external Pre-regulators) voltage	-0.3 ÷ V_{3V3}+0.3	
$V_{R_REF_DAC}$	External resistor (for DACs ref) pin voltage	-0.3 ÷ V_{3V3}+0.3	
$V_{PWM_DC_1/2}$	PWM DC setting pin voltage	-0.3 ÷ V_{5V}+0.3	
N_{FTP}	Number of FTP writing cycles (No integrated counter taking note about the FTP writing cycles).	1000	

8.2 ESD protection

Table 72. ESD protection

Parameter	Value	Unit
Electrostatic Discharge Test (AECQ100-002-E) - all pins(1)	+/-2	kV
Electrostatic Discharge Test (AECQ100-002-E) - all output pins(2)	+/-4	kV
Charge Device Model (CDM-AEC-Q100-011) - all pins	+/-500	V
Charge Device Model (CDM-AEC-Q100-011) - corner pins	+/-750	V
Machine Model (3) – all pins	+/-150	V

1. Included CAN_H and CAN_L.
2. VS, GND.
3. According to Machine Model: C = 200 pF; R = 0 Ω.

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8.3 Thermal characteristics

Table 73. QFN48L 7x7 package thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction to ambient (JEDEC JESD 51-2)	—	16	—	°C/W
$R_{thj\text{-}top}$	Junction - to - top thermal resistance (JEDEC JESD 51-2)	—	5.2	—	°C/W

1. Device soldered on 2s2p PCB thermally enhanced (slug included).

Table 74. Thermal data, warning and shutdown

Symbol	Parameter	Min	Typ	Max	Unit
T_{STG}	Storage temperature	-55		150	°C
T_J	Operating junction temperature	-40		150	°C
T_{TW}	Junction temperature thermal warning - threshold	130	140	150	°C
T_{TW_HYS}	Junction temperature thermal warning - hysteresis		10		°C
T_{TSD}	Junction temperature thermal shutdown - threshold	160	175	190	°C
T_{TSD_HYS}	Junction temperature thermal shutdown - hysteresis		15		°C

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8.4 Main electrical characteristics

Table 75. Supply

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_S	Operating battery voltage		5.5		28	V
V_{S_UV}	V_S under voltage shutdown	V_S = 13.5 V Force a ramp (on VS pin) from 4.5 V down to 3 V	3.75	4	4.25	V
$V_{S_UV_RES}$	V_S under voltage shutdown – reset threshold			4.5	4.75	V
I_{VS_STBY}	V_S stand-by current consumption (1)	Device in standby mode through: DIN = Low No CAN communication		40 (T_J=T_{room} °C)	65 (T_J=125°C)	uA
$I_{OP_OUT_OFF}$	Operating current consumption – all outputs off	From V_S – valid in Bus and SA mode		24		mA
		From V_{PRE_REG} – valid in Bus and SA mode		3.5		
$I_{OP_OUT_ON}$	Operating current consumption – all outputs on, 15mA per output	From V_S – valid in Bus and SA mode, DC and PWM mode		24		mA
		From V_{PRE_REG} – valid in Bus and SA mode, DC and PWM mode		27.5		
V_{5V}	5 V Output Regulator	V_S = 13.5 V Sink 100 mA on V5V pin	4.85	5	5.15	V
I_{V5V}	5 V Regulator Output Current	V_S = 13.5 V Sink 100 mA on V5V and check the output voltage regulator		100		mA
I_{V5V_SHT}	5 V Regulator short circuit current	V_S = 13.5 V Force 0 V on V5V pin	280	340	390	mA
V_{3V3}	3.3 V Output Regulator	V_S = 13.5 V Sink 5 mA on V3V3 pin	3.15	3.3	3.45	V

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Table 75. Supply (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{V3V3}	3V3 Regulator Output Current	V_S = 13.5 V Sink 5 mA on V3V3 pin and check the output voltage regulator		5		mA
I_{V3V3_SHT}	3.3 V Regulator short circuit current	V_S = 13.5 V Force 0 V on V3V3 pin	130	167	190	mA
$V_{3V3_POR_H}$	3.3 V Regulator power on reset – high threshold voltage	V_S = 13.5 V Force a ramp (on V3V3 pin) from 2.3 V to 3 V	2.7	2.8	2.9	V
$V_{3V3_POR_L}$	3.3 V Regulator power on reset – low threshold voltage	V_S = 13.5 V Force a ramp (on V3V3 pin) from 3 V down to 2.3 V	2.4	2.5	2.6	V
$V_{3V3_POR_HYST}$	3.3 V Regulator power on reset – hysteresis			300		mV
$V_{S_POR_H}$	Internal pre-regulator power on reset - high threshold voltage		2.4	2.5	2.6	V
$V_{S_POR_L}$	Internal pre-regulator power on reset - low threshold voltage		2.2	2.3	2.4	V
$V_{S_POR_HYST}$	Internal pre-regulator power on reset - hysteresis			200		mV

1. (CAN_H – CAN_L) < 0.4 V or (CAN_H – CAN_L) > 1.2 V.

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8.5 Linear current sources

The L99LDLH32 features 32 channels in High Side configuration. Output current regulation is demanded to 32 integrated linear current sources. Their relevant electrical characteristics are reported in the below table.

Table 76. Output characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{OUTx}	Channel output current - setting range (absolute value)		1		15	mA
I_{OUTx_STEP}	Channel output current - step			0.055		mA
I_{OUTx_ACC}	Channel output current – accuracy (1)	Over the whole current and temperature ranges	-11		+11	%
ΔI_{OUTx}	Channel To Channel output current – deviation within the same device	Over the whole current range			+14(2)	%
I_{OUTx_LEAK}	Channel output current - leakage	T_J=125°C, V_{OUTx}= 35 V; OUTx channel off			1	µA
RON_{PD_OUTx}	Channel output pull down (active when channel is off, not active in PWM operation) - RDSon resistance	T_J=125°C V_{OUTx}= 1 V			225	Ω
V_{OUTx_DROP}	Channel output voltage – drop (3)	I_{OUTx}= 15 mA T_J=125°C			1.05	V
t_{GD}	Gradual delay for each output	All channels enabled Guaranteed by scan		1.8		µs
t_{SR_ON}	Slew rate - turn on time for each channel			1		µs
t_{SR_OFF}	Slew rate - turn off time for each channel			1		µs
$V_{SHT_CH_TH_min}$ $V_{SHT_CH_DIN_TH_min}$	LED short circuit threshold – minimum voltage			0.31		V
$V_{SHT_CH_TH_max}$ $V_{SHT_CH_DIN_TH_max}$	LED Short circuit threshold - maximum voltage			5.02		V
$V_{SHT_CH_TH_step}$ $V_{SHT_CH_DIN_TH_step}$	LED short circuit threshold - step voltage			0.314		V

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Table 76. Output characteristics (continued)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
$V_{OUT_SHT_GND_TH}$	Output Channel Short To Ground - voltage threshold				850		mV
$V_{PG_TH_VPRE_REG_min}$	Minimum V_{PRE_REG} power good threshold - for channel diagnostic detection enabling				4(4)		V
$V_{PG_TH_VPRE_REG_max}$	Maximum V_{PRE_REG} power good threshold - for channel diagnostic detection enabling				35		V
$V_{PG_TH_VPRE_REG_step}$	V_{PRE_REG} power good threshold step				157		mV
V_{OL_TH}	Open Load – voltage threshold		Guaranteed by ADC (V_{OUTx} reading) and Scan tes		470		mV
V_{NTC_TH}	NTC threshold voltage – derating start				See *Table 78*		
V_{NTC_SHT}	NTC threshold voltage - short detection			185	245	315	mV
$V_{REF_PRE_REG}$	External Pre-Regulator Reference Voltage		V_S = 13.5 V V_{OUTmax} = 12.5 V $V_{REF_PRE_REG}$ = k*(V_{OUTmax}+1.4) k = 0.05 (2/40)	560	695	800	mV
N_Fails	Number of detected failures (also non-consecutive)– counter cycles	Short Circuit	Guaranteed by Scan		14		
		Open Load			8		
N_Fails_reset	Number of NOT detected failures (consecutive) - counter reset		Guaranteed by Scan		3		
N_{FTP}	Number of FTP writing cycles. (No integrated counter to take note about the FTP writing cycles)		Guaranteed by Scan			1000	

1. Upon the usage of the suggested resistance on R_REF_DAC pin.
2. New parameter, Max spread Channel to Channel: ($Curent_{Max}$ – $Current_{Min}$) / $Current_{Max}$.
3. Minimum voltage drop from device V_{PRE_REG} to device OUTx (to guarantee programmed current regulation).
4. Any V_{PRE_REG} value from 00h to 1Ah codes is clamped to 4 V.

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Table 77. PWM characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$PWM_{_FREQ_MIN}$	PWM minimum frequency			200		Hz
$PWM_{_FREQ_MAX}$	PWM maximum frequency			1400		Hz
$PWM_{_FREQ_ACC}$	PWM frequency accuracy	Guaranteed by Scan	-5		5	%
$PWM_{_PHASE_SHIFT_MIN}$	PWM minimum phase shift – Responder mode	Guaranteed by Scan		0		µs
$PWM_{_PHASE_SHIFT_MAX}$	PWM maximum phase shift – Responder mode	Guaranteed by Scan		105		µs
$PWM_{_PHASE_SHIFT_STEP}$	PWM phase shift step – Responder mode			15		µs
$t_{PWM_ON_OFF}$	Minimum PWM on-time and off-time vs frequency	PWM_FREQ = 200 Hz	5			µs
		PWM_FREQ = 300 Hz	3.3			µs
		PWM_FREQ ≥ 400 Hz	2.5			µs
$t_{STARTUP_PWM_VS}$	Time needed for device startup, from device power up (presence of V_S) to the channel activation – PWM dimming through power line	DIN_MAP_CHx = 01 (all outputs mapped to Direct Input) DIN connected to Power Supply = 12.5 V through resistor divider CURR_SET_CHx = FFh (all outputs current set to 15 mA) Power Supply Dimming Frequency = 200 Hz Power Supply Dimming Duty Cycle = 50%			750	µs

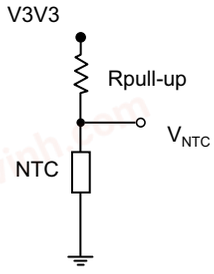
Table 78. NTC derating start configuration – Voltage vs Temperature

Bit 2	Bit 1	Bit 0	Derating Start Temp. [°C]	V_{NTC_TH} [V]
0	0	0	55	2.034
0	0	1	60	1.908
0	1	0	65	1.783
0	1	1	70	1.66
1	0	0	80	1.423
1	0	1	90	1.207
1	1	0	95	1.106

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Table 78. NTC derating start configuration – Voltage vs Temperature

Bit 2	Bit 1	Bit 0	Derating Start Temp. [°C]	V_{NTC_TH} [V]
1	1	1	100	1.013



V_{NTC_TH} is the NTC voltage corresponding to the derating start temperature
Rpull-up=2.2 kΩ; NTC= 10 kΩ ± 1%, @ 25°C.
NTC part number: NCU18XH103F6SRB
NTC chip type temperature characteristics: B-constant = 3380K ± 0.7%

8.6 Digital timings and ADC characteristics

Table 79. Digital timings

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
t_{WD}	Watchdog timeout period	Guaranteed by scan	00 (default)	45	50	55	ms
			01	95	100	105	
			10	195	200	205	
			11	20	25	30	
$t_{AUTORESTART}$	Auto-restart time in Fail Safe / Stand-alone mode	Guaranteed by Scan		45	50	55	ms
t_{FILTER}	Filtering time – Time needed for DIN overtaking control on bus mode (after DIN rising edge when DIN_EN set in bus mode)	Guaranteed by scan			32		µs
$t_{BUS_CONTROL}$	Timeout for bus control re-activation after last falling edge on DIN	Guaranteed by Scan			10		ms
t_{WAKE_UP}	Time for a complete wake up (V_{3V3} > $V_{3V3_POR_H}$)	DIN high for t > t_{WAKEUP} Cap on V3V3 = 1 µF V_{3V3} > $V_{3V3_POR_H}$			30		us
t_{STDBY}	Time needed for a transition to standby mode (V_{3V3} < $V_{3V3_POR_L}$)	DIN low Cap on V3V3 = 1 µF V_{3V3} < $V_{3V3_POR_L}$			15		ms
$t_{STARTUP}$	Time needed for initialization phase (transition state)				650		µs

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Table 79. Digital timings (continued)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
t_{POR_DELAY}	Time needed after POR, before configuring the device (all outputs kept off during this time)	Guaranteed by scan	00		0		ms
			01		25		
			10		50		
			11		100		
$t_{DIAG_BLANK_x}$	Blanking time - for diagnostic validation	Guaranteed by scan	00		50		µs
			01		100		
			10		150		
			11		200		
t_{FTP_WR}	FTP memory writing time	Guaranteed by scan			12		mS
t_{DIN_FALL}	DIN falling edge setting time - for fault clearing	Guaranteed by scan			10		mS

Table 80. ADC characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ADC_{RES}	ADC resolution			8		bit
ADC_{CONV_TIME}	ADC conversion time			1.6		µs
ADC_{FS_VOUTx}	ADC full scale for V_{OUTx}			40		V
ADC_{STEP_VOUTx}	ADC step for V_{OUTx}			157		mV
$ADC_{FS_VPRE_REG}$	ADC full scale for V_{PRE_REG}			40		V
$ADC_{STEP_VPRE_REG}$	ADC step for V_{PRE_REG}			157		mV
ADC_{FS_VS}	ADC full scale for V_S			40		V
ADC_{STEP_VS}	ADC step for V_S			157		mV
ADC_{FS_VNTC}	ADC full scale for V_{NTC}			2.5		V
ADC_{STEP_VNTC}	ADC step for V_{NTC}			10		mV
ADC_{FS_TJ}	ADC full scale for T_J			2.5		V
ADC_{STEP_TJ}	ADC step for T_J			10		mV
$ADC_{INTRINSIC_ACCURACY}$	ADC reading accuracy for NTC, T_J - including offset, INL, DNL		-3		3	LSB
$ADC_{VOLTAGE_ACCURACY}$	ADC reading accuracy for V_{OUTx}, V_{PRE_REG}, V_S - including offset, INL, DNL		-6		6	LSB

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Table 81. Digital I/O characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DIN_L} V_{FAULT_L} V_{SYNC_I/O_L} V_{CS_L} $V_{PWM_DC_1/2_L}$	Low Logic Level				0.3 * V3V3	V
V_{DIN_H} V_{FAULT_H} V_{SYNC_I/O_H} V_{CS_H} $V_{PWM_DC_1/2_H}$	High Logic Level		0.7 * V3V3		V3V3	V
R_{PullUp_FAULT}	FAULT pin - integrated pull up resistor			500		kΩ
I_{FAULT}	FAULT pin - sinking current (Fault active low)				10	mA
R_{ON_FAULT}	FAULT pin - open drain NMOS RDS_{ON} (Fault active low)				150	Ω
I_{LEAK_FAULT}	FAULT pin - open drain NMOS leakage (no FAULT active)				1	µA

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8.7 CAN FD Light compatible transceiver characteristics

Table 82. CAN FD Light compatible transceiver

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{CAN_H, CAN_L, CM}$	Common mode bus voltage (V_{CAN_H} + V_{CAN_L}) / 2	Measured with respect to the ground	-12		12	V
$I_{TR_CC_SC}$	Transceiver current consumption during output short	R_L=50 Ω … 65 Ω; V_{CAN_H}=-3 V or V_{CAN_L}=40 V			120	mA
CAN_{BR}	Transceiver bit-rates	Supported bit-rates at which all requirements are fulfilled	1			Mbit/s
$V_{CAN_H_DOM}$	Single ended CAN_H voltage level in dominant state	R_L=50 Ω … 65 Ω	2.75	3.5	4.5	V
$V_{CAN_L_DOM}$	Single ended CAN_L voltage level in dominant state	R_L=50 Ω … 65 Ω	0.5	1.5	2.25	V
V_{DIFF_DOM}	Differential output voltage in dominant state: $V_{CAN_H_DOM}$ - $V_{CAN_L_DOM}$		1.5	2.0	3	V
V_{CAN_SYM}	Driver symmetry: V_{CAN_SYM} = ($V_{CAN_H_DOM}$ + $V_{CAN_L_DOM}$) / 5V(1)	R_L=60 Ω ±1% f_{TXD} = 1 MHz (square wave, 50% duty cycle)(2); C_{SPLIT} = 4.7 nF (±5%);	0.9	1	1.1	V
$I_{CAN_H_DOM}$	CAN_H output current in dominant state	V_{CAN_H}=-3 V … 18 V;	-115		115	mA
$I_{CAN_L_DOM}$	CAN_L output current in dominant state	V_{CAN_L}=-3 V …18 V;	-115		115	mA
$V_{CAN_H_REC}$	CAN_H voltage level in recessive state	No Load	2	2.5	3	V
$V_{CAN_L_REC}$	CAN_L voltage level in recessive state	No Load	2	2.5	3	V
V_{DIFF_REC}	Differential output voltage in recessive state: $V_{CAN_H_REC}$ - $V_{CAN_L_REC}$	No Load	-50		50	mV
$V_{CAN_H_REC_LP}$	CAN_H voltage level in recessive state – standby mode	No Load	-0.1	0	0.1	V
$V_{CAN_L_REC_LP}$	CAN_L voltage level in recessive state - standby mode	No Load	-0.1	0	0.1	V
$V_{DIFF_REC_OUT_LP}$	Differential output voltage in recessive state – $V_{CAN_H_REC}$ -$V_{CAN_L_REC}$, standby mode	No Load	-50		50	mV
V_{TH_DOM}	Differential receiver switching threshold voltage - recessive to dominant state	-12 V ≤ V_{CAN_H} ≤ 12 V; -12 V ≤ V_{CAN_L} ≤ 12 V	0.5		0.9	V

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Table 82. CAN FD Light compatible transceiver (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DOM_RANGE}	Static differential dominant input level voltage range	-12 V ≤ V_{CAN_H} ≤ 12 V; -12 V ≤ V_{CAN_L} ≤ 12 V	0.9		8	V
V_{TH_REC}	Differential receiver switching threshold voltage - dominant to recessive state	-12 V ≤ V_{CAN_H} ≤ 12 V; -12 V ≤ V_{CAN_L} ≤ 12 V	0.5		0.9	V
V_{REC_RANGE}	Static differential recessive input level voltage range	-12 V ≤ V_{CAN_H} ≤ 12 V; -12 V ≤ V_{CAN_L} ≤ 12 V	-5		0.5	V
$V_{TH_DOM_LP}$	Differential receiver switching threshold voltage recessive to dominant state – standby mode	-12 V ≤ V_{CAN_H} ≤ 12 V; -12 V ≤ V_{CAN_L} ≤ 12 V	0.4		1.15	V
$V_{DOM_RANGE_LP}$	Static differential dominant input level voltage range – standby mode	-12 V ≤ V_{CAN_H} ≤ 12 V; -12 V ≤ V_{CAN_L} ≤ 12 V	0.9		8	V
$V_{TH_REC_LP}$	Differential receiver switching threshold voltage dominant to recessive state – standby mode	-12 V ≤ V_{CAN_H} ≤ 12 V; -12 V ≤ V_{CAN_L} ≤ 12 V	0.4		1.15	V
$V_{REC_RANGE_LP}$	Static differential recessive input level voltage range – standby mode	-12 V ≤ V_{CAN_H} ≤ 12 V; -12 V ≤ V_{CAN_L} ≤ 12 V	-3		0.5	V
R_{DIFF}	Differential internal resistance	No Load R_{DIFF} = R_{CAN_H} + R_{CAN_L} -2 V ≤ V_{CAN_H} ≤ +5,0 V; -2 V ≤ V_{CAN_L} ≤ +5,0 V	12		100	kΩ
$R_{CAN_H,\ CAN_L}$	Single Ended Internal resistance	No Load -2 V ≤ V_{CAN_H} ≤ +5,0 V; -2 V ≤ V_{CAN_L} ≤ +5,0 V	6		50	kΩ
m_R	Internal Resistance matching R_{CAN_H,CAN_L}	Biasing active; No Load m_R = 2 x (R_{CAN_H} - R_{CAN_L}) / (R_{CAN_H} + R_{CAN_L}); V_{CAN_H} = +5,0 V; V_{CAN_L} = +5,0 V	-0.03		0.03	
$t_{LOOP_HighToLow}$	Loop delay TXD to RXD - High to Low	5.5 V ≤ V_S ≤ 18 V; R_L=60 Ω ±1%; C_L = 100 pF; 30% V_{TXD} – 30% V_{RXD}; TXD fall time = 10 ns (90% - 10%); (3)			255	ns
$t_{LOOP_LowToHigh}$	Loop delay TXD to RXD - Low to High	5.5 V ≤ V_S ≤ 18 V; R_L=60 Ω ±1%; C_L = 100 pF; 70% V_{TXD} – 70% V_{RXD}; TXD rise time = 10 ns (10% - 90%);(3)			255	ns

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Table 82. CAN FD Light compatible transceiver (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{LEAK_CAN_H}$	Input leakage current CAN_H	Unpowered device (VS not present); V_{CAN_H}=5 V; V_{CAN_L}=5 V V_S connected via 0 Ω to GND V_S connected via 47 kΩ to GND	-10		10	µA
$I_{LEAK_CAN_L}$	Input leakage current CAN_L	Unpowered device (VS not present); V_{CAN_H}=5 V; V_{CAN_L}=5 V V_S connected via 0 Ω to GND V_S connected via 47 kΩ to GND	-10		10	µA
t_{WUP}	Time between WUP(4) on the CAN bus until V3V3 LDO is active	Wake-Up-Pattern Wake-Up V3V3 in regulation	0		1	ms
t_{CAN_FILTER}	CAN activity filter time	Guaranteed by scan	0.5		1.8	µs
t_{CAN_WUP}	Wake-up time out	Guaranteed by scan	0.8	1	5	ms
t_{BIAS}	Bias Reaction Time	5.5 V ≤ V_S ≤ 18 V; R_L=50 … 65 Ω; 1.15V_{DIFF} ➔ V_{SYM} = 0.1(5); Transition bias inactive to bias active			250	µs

1. 5 V is the CAN supply.
2. TXD is the internal CAN transmitter input accessible in test mode only. Measurement equipment input load <20 pF, >1 MΩ.
3. TXD and RXD are the internal CAN transmitter input and output that are accessible in test mode only.
4. Measured from the start of the WUP frame.
5. Measured from the start of the WUP frame until $V_{SYM} \geq 0.1$, $V_{SYM} = V_{CAN_H} + V_{CAN_L} / 5V$.

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9 Package and PCB thermal data

9.1 QFN-48L 7x7 thermal data

Figure 87. QFN-48L 7x7 on four-layer PCB

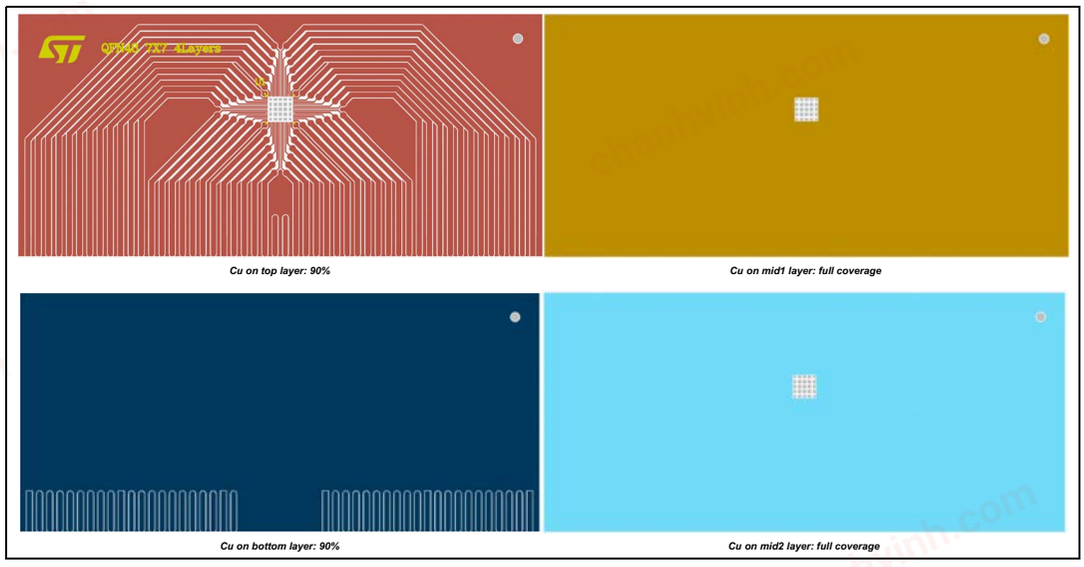


Table 83. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	129 mm x 60 mm
Board Material	FR4
Copper thickness (outer layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm

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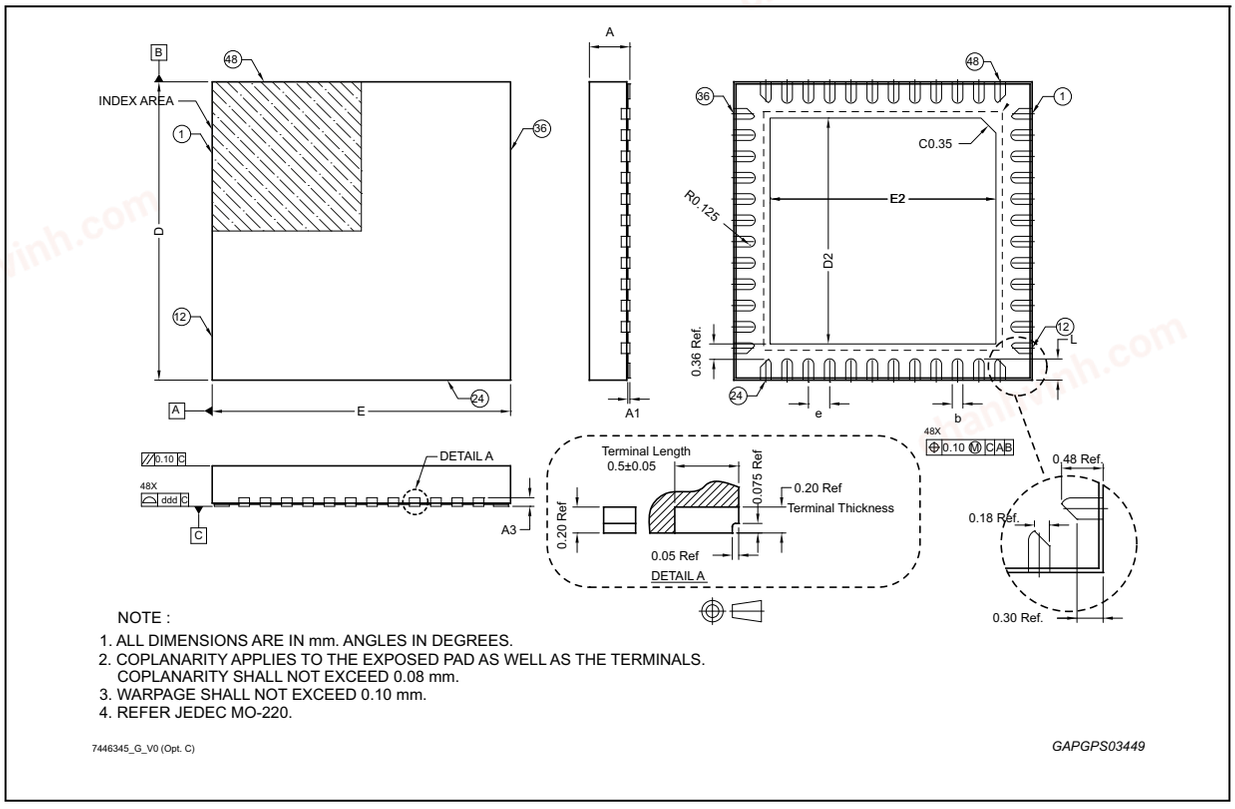
10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK is an ST trademark.

10.1 QFN48L 7x7 package outline

Figure 88. Package outline



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10.2 QFN48L 7x7 mechanical data

Table 84. Package mechanical data

	997G Dimensions					
	Databook (mm)			Drawing (mm)		
Ref.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A	0.85	0.95	1.05	0.90	0.95	1.00
A1		0.0	0.05		0.0	0.05
A2		0.75			0.75	
A3		0.2			0.2	
b	0.15	0.25	0.35	0.20	0.25	0.30
D	6.85	7.00	7.15	6.90	7.00	7.10
D2	5.15	5.30	5.45	SEE EXPOSED PAD VARIATION		
E	6.85	7.00	7.15	6.90	7.00	7.10
E2	5.15	5.30	5.45	SEE EXPOSED PAD VARIATION		
e	0.45	0.50	7.15	0.45	0.50	0.55
L	0.45	0.50	0.55	0.45	0.50	0.55
ddd			0.08			0.08
	EXPOSED PAD VARIATION					
	D2			**E2**		
VARIATION	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A	5.15	5.30	5.45	5.20	5.30	5.40

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11 Order codes

Table 85. Device summary

Package	Order code
	Tape and Reel
QFN48L 7x7	L99LDLH32TR

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12 Revision history

Table 86. Document revision history

Date	Revision	Changes
15-Apr-2019	1	Initial release.
10-Oct-2019	2	Added: – *Chapter 6.5.5: Synchronization Frame*; – *Chapter 9: Package and PCB thermal data*. Updated: – *Table 36: Device configuration 1 field description*; – *Table 37: Device configuration 2 field description*; – *Table 38: Device configuration 3 field description*; – *Table 71: Absolute maximum ratings*; – *Table 73: QFN48L 7x7 package thermal data*; – *Table 75: Supply*; – *Table 76: Output characteristics*; – *Table 77: PWM characteristics*; – *Table 79: Digital timings*; – *Table 82: CAN FD Light compatible transceiver*. Minor text changes.

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Table 86. Document revision history (continued)

Date	Revision	Changes
25-Feb-2021	3	Added: – *Table 16: FTP memory map*; – *Chapter 7.1.21: FTP parity error status register*; – *Chapter 7.2: FTP Rows description*. Updated: – *Figure 4: QFN48L 7x7 connection diagram*; – *Figure 6: Device state diagram*; – *Figure 10: LED short circuit fault management*; – *Figure 11: Short to ground fault management*; – *Figure 12: Open load fault management*; – *Chapter 5.1.3: Reset mode*; – *Chapter 5.1.4: Fail Safe / Stand Alone mode*; – *Chapter 5.1.5: Normal / Bus mode*; – *Chapter 5.3.4: Thermal shutdown*; – *Table 2: Minimum channel drop-out voltage at max current vs T_J*; – *Table 71: Absolute maximum ratings*; – *Table 76: Output characteristics*; – *Table 77: PWM characteristics*; – *Table 82: CAN FD Light compatible transceiver*; – *Table 85: Device summary*. Minor text changes in: – *Chapter 5.3.7: Channel output - LED short circuit detection*; – *Chapter 5.3.8: Channel output - short circuit to GND*; – *Chapter 5.3.9: Channel output – Open load detection*; – *Chapter 6.5.3: Chain initialization*; – *Table 14: Global status byte field description*; – *Table 15: RAM memory map*; – *Table 36: Device configuration 1 field description*; – *Table 37: Device configuration 2 field description*; – *Table 38: Device configuration 3 field description*; – *Table 39: 20 MHz Oscillator, Dithering - Modulation Parameters*; – *Table 53: Channel short circuit status field description*; – *Table 54: Channel open load status field description*; – *Table 55: Channel short to GND field description*; – *Table 59: Device status 3 field description*; – *Table 60: FTP status 1 field description*; – *Table 74: Thermal data, warning and shutdown*; – *Table 75: Supply*; – *Table 78: NTC derating start configuration – Voltage vs Temperature*; – *Table 79: Digital timings*; – *Table 81: Digital I/O characteristics*.
09-Mar-2021	4	Added watermark “Confidential”.

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Table 86. Document revision history (continued)

Date	Revision	Changes
16-Dec-2021	5	Added: – *Figure 1: Simplified application schematic*; – *Figure 3: Application diagram - example*; – *Figure 57: 20 MHz Oscillator, Dithering - Modulation Curve*. Updated: – *Figure 2: Functional block diagram*; – *Figure 6: Device state diagram*; – *Figure 9: Output & PWM control concept DIN*; – *Figure 14: Commander block diagram*; – *Figure 15: Responder ECU Controller Device*; – *Figure 27: Unicast frame w/o data - Commander request and Responder answer*; – *Figure 28: Unicast frame with single RAM read - Commander request and Responder answer*; – *Figure 29: Unicast frame with Single RAM read and clear - Commander request and Responder answer*; – *Figure 30: Unicast frame with burst read mode RAM register - Commander request and Responder answer*; – *Figure 31: Unicast frame with single RAM write - Commander request and Responder answer*; – *Figure 32: Unicast frame with 3x RAM write - Commander request and Responder answer*; – *Table 39: 20 MHz Oscillator, Dithering - Modulation Parameters*; – *Table 69: Row_12*; – *Table 70: CAN bit sampling point*; – *Table 75: Supply*; – *Table 76: Output characteristics*; – *Table 79: Digital timings*; – *Section 4.3: Channel driver drop-out voltage*; – *Section 6.1: CAN FD Light compatible network protocol*.

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Table 86. Document revision history (continued)

Date	Revision	Changes
16-Dec-2021	5	Minor text changes in: – *Figure 54: Device configuration register #1*; – *Figure 76: Device status register #3*; – *Table 36: Device configuration 1 field description*; – *Table 52: Channel output status field description*; – *Table 59: Device status 3 field description*; – *Table 71: Absolute maximum ratings*; – *Table 77: PWM characteristics*; – *Table 78: NTC derating start configuration – Voltage vs Temperature*; – *Section : Features*; – *Section 1: Description*; – *Section 4.1: General description*; – *Section 6.5.5: Synchronization Frame*; – *Section 6.6.2: Unicast response frame*. Typo corrections. Removed watermark “Confidential”.

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