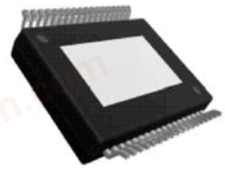
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L99H02

H-bridge gate driver for automotive applications

Datasheet - production data



PowerSSO-36



LQFP32
7x7mm

Features

- AEC-Q100 qualified
- Operating supply voltage 6 V to 28 V
- Central 2-stage charge pump
- 100% duty cycle
- Full R_{DSon} down to 6 V (standard level threshold MOSFETs)
- Charge pump output available for driving an external reverse battery NMOSFET protection
- Charge pump current limited
- PWM operation up to 30 kHz
- SPI interface
- Current sense amplifier / free configurable
- Zero adjust for end of line trimming
- Power management: programmable free wheeling
- Sensing circuitry of external MOSFETs with embedded thermal sensors

Applications

- Wiper
- Power door
- Seat belt tensioner
- Seat positioning
- Valve tronic
- Park break
- 2H motors

Description

The L99H02 is designed to drive 4 external N-channel MOS transistors in H-bridge configuration for DC-motor driving in automotive applications. A free configurable current sense amplifier is integrated. The integrated standard serial peripheral interface (SPI) controls the device and provides diagnostic information. An interface pin for the thermal sensors of the external MOSFETs is implemented.

Table 1. Device summary

Package	Order codes		
	Part number (tube)	Part number (tape and reel)	Part number (tray)
PowerSSO-36	L99H02XP	L99H02XPTR	-
LQFP32	-	L99H02QFTR	L99H02QF

This is information on a product in full production. www.st.com

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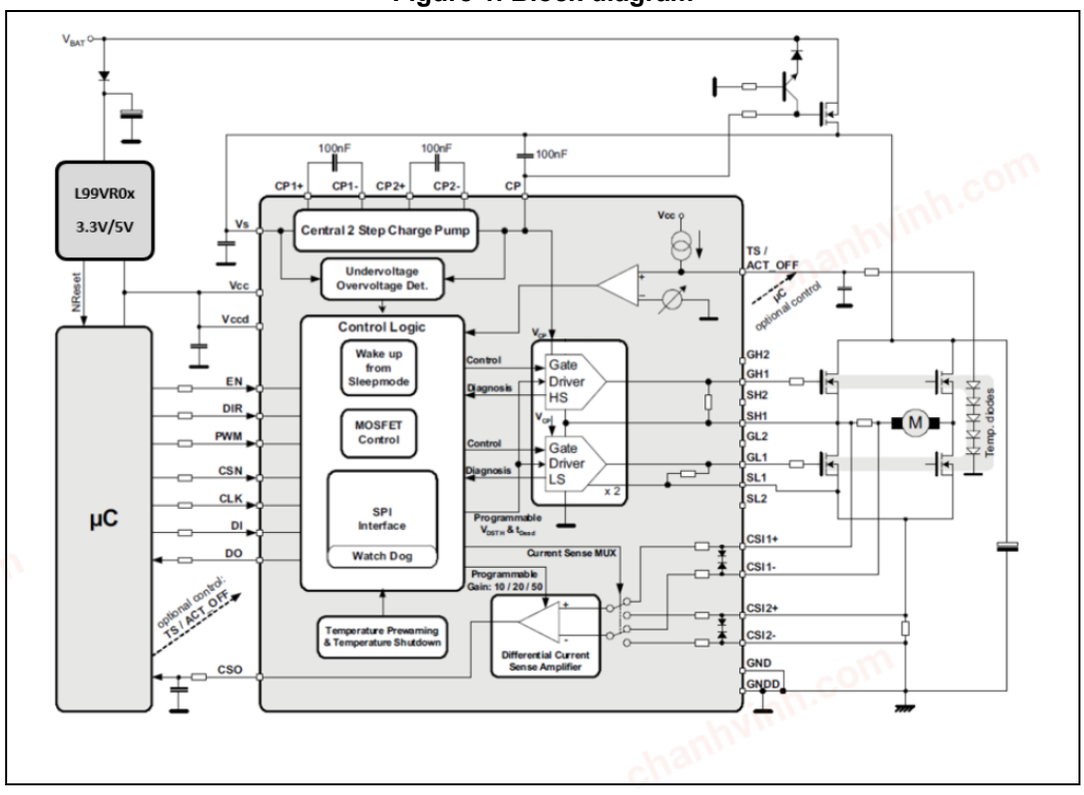
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1 Block diagram and pin description

Figure 1. Block diagram



1.1 Pin description

Table 2. Pin definitions and functions

Pin	Symbol	Function
1	GND	Ground. Reference potential, connected to slug.
2	GNDD	Digital ground. Reference potential.
3	V_{CCD}	Logic voltage supply 3.3 V/5 V: for this input a ceramic capacitor as close as possible to GND is recommended.
4	V_{CC}	Analog voltage supply 3.3 V/5 V: for this input a ceramic capacitor as close as possible to GND is recommended.
5	EN	Enable input. The enable input has a pull-down resistor.
6	DIR	Direction select input for H-bridge control. This input has a pull-down current.
7	PWM	PWM input for H-bridge control. This input has a pull-down current.
8	CSN	Chip select not input: this input is low active and requires CMOS logic levels. The serial data transfer between L99H02 and microcontroller is enabled by pulling the input CSN to low-level. This input has a pull-up current.

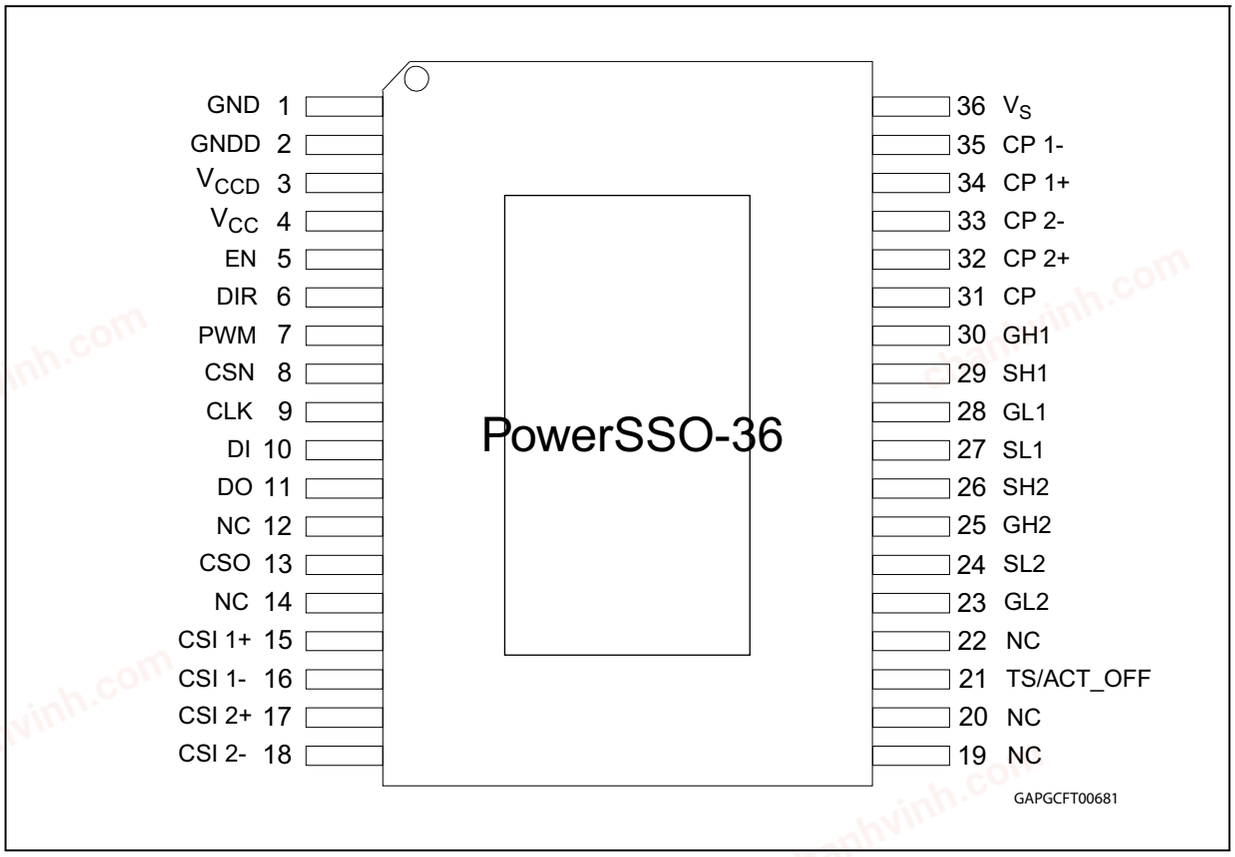
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Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
9	CLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels.This input has a pull-down current.
10	DI	Serial data in: the input requires CMOS logic levels and receives serial data from the microcontroller. The data is an 8-bit control word and the most significant bit (MSB, bit 7) is transferred first. This input has a pull-down current.
11	DO	Serial data out: the diagnosis data is available via the SPI and this tristate-output. The output remains in tristate, if the chip is not selected by the input CSN (CSN = high).
12, 14, 19, 20, 22	NC	Not connected.
13	CSO	Current sense amplifier output: V_{CC} compatible.
15	CSI1+	Current sense amplifier input: positive input 1, multiplexible.
16	CSI1-	Current sense amplifier input: negative input 1, multiplexible.
17	CSI2+	Current sense amplifier input: positive input 2, multiplexible.
18	CSI2-	Current sense amplifier input: negative input 2, multiplexible.
21	TS/ ACT_OFF	Thermal sensor interface or input to switch all driver in sink condition.
23	GL2	Gate driver for PowerMOS low-side switch in half bridge 2.
24	SL2	Source of low-side switch in half bridge 2.
25	GH2	Gate driver for PowerMOS high-side switch in half bridge 2.
26	SH2	Source/drain of half bridge 2.
27	SL1	Source of low-side switch in half bridge 1.
28	GL1	Gate driver for PowerMOS low-side switch in half bridge 1.
29	SH1	Source/drain of half bridge 1.
30	GH1	Gate driver for PowerMOS high-side switch in half bridge 1.
31	CP	Charge pump output.
32	CP2+	Charge pump pin for capacitor 2, positive side.
33	CP2-	Charge pump pin for capacitor 2, negative side.
34	CP1+	Charge pump pin for capacitor 1, positive side.
35	CP1-	Charge pump pin for capacitor 1, negative side.
36	V_S	Power supply voltage (external reverse protection required). For EMI reason a ceramic capacitor as close as possible to GND is recommended.

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Figure 2. Pinning of device in PowerSSO-36 package



1.2 Pinout LQFP32

Table 3. Pin definitions and functions

Pin	Symbol	Function
1	CP2-	Charge pump pin for capacitor 2, negative side.
2	CP1+	Charge pump pin for capacitor 1, positive side.
3	CP1-	Charge pump pin for capacitor 1, negative side.
4	V_S	Power supply voltage (external reverse protection required). For EMI reason a ceramic capacitor as close as possible to GND is recommended.
5	GND	Ground. Reference potential.
6	GNDD	Digital ground. Reference potential.
7	V_{CCD}	Logic voltage supply 3.3 V/5 V: for this input a ceramic capacitor as close as possible to GND is recommended.
8	V_{CC}	Analog voltage supply 3.3 V/5 V: for this input a ceramic capacitor as close as possible to GND is recommended.
9	EN	Enable input. The enable input has a pull-down resistor.

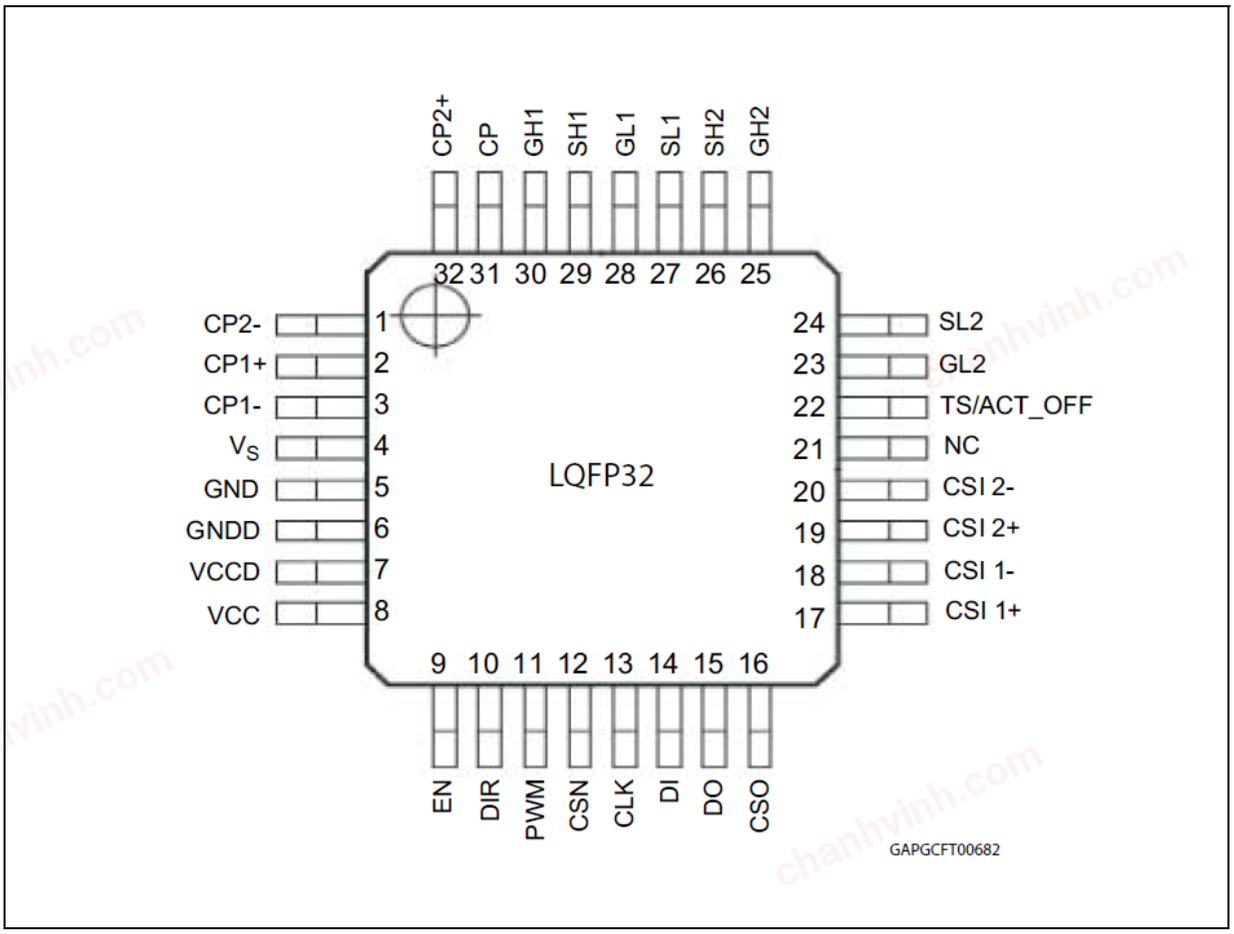
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Table 3. Pin definitions and functions (continued)

Pin	Symbol	Function
10	DIR	Direction select input for H-bridge control. This input has a pull-down current.
11	PWM	PWM input for H-bridge control. This input has a pull-down current.
12	CSN	Chip select not input: this input is low active and requires CMOS logic levels. The serial data transfer between L99H01 and microcontroller is enabled by pulling the input CSN to low-level. This input has a pull-up current.
13	CLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels.This input has a pull-down current.
14	DI	Serial data in: the input requires CMOS logic levels and receives serial data from the microcontroller. The data is an 8-bit control word and the most significant bit (MSB, bit 7) is transferred first. This input has a pull-down current.
15	DO	Serial data out: the diagnosis data is available via the SPI and this tristate-output. The output remains in tristate, if the chip is not selected by the input CSN (CSN = high).
16	CSO	Current sense amplifier output: V_{CC} compatible.
17	CSI1+	Current sense amplifier input: positive input 1, multiplexible.
18	CSI1-	Current sense amplifier input: negative input 1, multiplexible.
19	CSI2+	Current sense amplifier input: positive input 2, multiplexible.
20	CSI2-	Current sense amplifier input: negative input 2, multiplexible.
21	NC	Not connected.
22	TS/ ACT_OFF	Thermal sensor interface or external off for all gate drivers.
23	GL2	Gate driver for PowerMOS low-side switch in halfbridge 2.
24	SL2	Source of low-side switch in halfbridge 2.
25	GH2	Gate driver for PowerMOS high-side switch in halfbridge 2.
26	SH2	Source/drain of halfbridge 2.
27	SL1	Source of low-side switch in halfbridge 1.
28	GL1	Gate driver for PowerMOS low-side switch in halfbridge 1.
29	SH1	Source/drain of halfbridge 1.
30	GH1	Gate driver for PowerMOS high-side switch in halfbridge 1.
31	CP	Charge pump output.
32	CP2+	Charge pump pin for capacitor 2, positive side.

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Figure 3. Pinning of device in LQFP-32 package



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2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Item	Symbol	Parameter	Value	Unit
4.1.1	V_S	Power supply voltage	-0,3 to 35	V
4.1.2		Single pulse t_{max} < 400 ms	40	V
4.2	V_{CC}	Stabilished supply voltage	-0.3 to 5.5	V
4.3	DI, DO, CLK, CSN, EN, DIR, PWM	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
4.4	CSO, TS	Analog input / output voltage	-0.3 to V_{CC} + 0.3	V
4.5	CSI1+, CSI1-, CSI2+, CSI2-	HV signal pins	-4 to V_S + 8 V	V
4.6	GL2, GH2, GL1, GH1 (Gxy)	HV signal pins	Sxy - 1 to Sxy + 10; V_{CP} + 0.3	V
4.7	SL2, SH2, SL1, SH1	HV signal pins	-6 to 40	V
4.8	CP2- CP1-	HV signal pins	-0.3 to V_S + 0.3	V
4.9	CP1+	HV signal pins	V_S - 0.3 to V_S + 14	V
4.10	CP2+	HV signal pins	V_S - 0.6 to V_S + 14	V
4.11	CP	Power pin	V_S - 0.3 to V_S + 14	V

2.2 ESD protection

Table 5. ESD protection

Item	Parameter	Value	Unit
5.1	All pins	± 2 (1)	kV
5.2	V_S versus GND	± 4 (1)	kV

1. - HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.
   - HBM with all unzapped pins grounded.

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2.3 Thermal data

Table 6. Operating junction temperature

Item	Symbol	Parameter	Value	Unit
6.1	T_j	Operating junction temperature	-40 to 150	°C

Table 7. Temperature warning and thermal shutdown

Item	Symbol	Parameter		Min.	Typ.	Max.	Unit
7.1	$T_{jTW\ ON}$	Temperature warning threshold junction temperature	T_j	135	—	165	°C
7.2	$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	T_j increasing	155	—	185	°C
7.3	$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	T_j decreasing	150	—	180	°C

Table 8. Packages thermal resistance

Item	Symbol	Parameter	Value		Unit
			PowerSSO-36	LQFP32	
8.1	$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (max.)	58(1)	80(1)	°C/W

1. Minimum footprint.

2.4 Electrical characteristics

V_S = 6 V to 28 V, V_{CC} = 3 V to 5.3 V, T_j = -40°C to 150°C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 9. Supply

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
9.1	V_S	Operating supply voltage range		6		28	V
9.2	V_{VS_OV1}	Overvoltage disable high threshold 1	SPI: OVT = 1	28	30.5	32	V
9.3	V_{VS_OV1H}	Overvoltage threshold 1 hysteresis		0.57	0.77	1.07	V
9.4	V_{VS_OV2}	Overvoltage disable high threshold 2	SPI: OVT = 0	18	20	22	V
9.5	V_{VS_OV2H}	Overvoltage threshold 2 hysteresis		0.42	0.62	0.82	V

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Table 9. Supply (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
9.6	V_{VS_UV}	Undervoltage disable low threshold		4.7	4.9	5.1	V
9.7	V_{VS_UVH}	Undervoltage threshold hysteresis		0.2	0.3	0.4	V
9.8.1	I_S	V_S DC supply current	V_S = 13 V; V_{CC} = 5 V; Active mode; Outputs floating	4.5	5.5	6.5	mA
9.8.2			V_S = 6 V to 28 V; V_{CC} = 5.0 V; Active mode; Outputs floating	2.5		18	mA
9.9	I_{SL}	V_S quiescent supply current	V_S = 13 V; V_{CC} = 0 V; Standby mode; T_{Test} = -40°C, 25°C; Outputs floating			5	µA
9.10	I_{CC}	V_{CC} DC supply current	V_S = 13 V; V_{CC} = 5 V; active mode	1.5	1.8	2.5	mA
9.11	I_{CC}	V_{CC} quiescent supply current	V_{CC} = 5 V; standby mode	30	70	150	µA
9.12	I_{CCd}	V_{CCd} supply current	V_S = 13 V; V_{CC} = V_{CCd} = 5 V; active mode	250	500	750	µA

Table 10. Undervoltage detection

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
10.1	$V_{POR\ OFF}$	Power-on reset threshold	V_{CC} increasing	2.2	2.55	2.8	V
10.2	$V_{POR\ ON}$	Power-on reset threshold	V_{CC} decreasing	2.0	2.25	2.6	V
10.3	$V_{POR\ hyst}$	Power-on reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$	0.2	0.3	0.4	V

Table 11. Watchdog

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.1	T_{WDTO}	Watchdog time out	—	50	60	100	ms

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Table 12. Inputs: CSN, CLK, PWM, DIR, EN and DI

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
12.1	$V_{in\ L}$	Low-level input voltage		0.3 * V_{CC}	0.4 * V_{CC}		V
12.2	$V_{in\ H}$	High-level input voltage			0.6 * V_{CC}	0.7 * V_{CC}	V
12.3	$V_{in\ Hyst}$	Input voltage hysteresis		0.1 * V_{CC}			V
12.4	$I_{CSN\ in}$	Pull-up current at input CSN	V_{CSN} = V_{CC} - 1.5 V	-50	-25	-10	µA
12.5	$I_{CLK\ in}$	Pull-down current at input CLK	V_{CLK} = 1.5 V	10	35	50	µA
12.6	$I_{DI\ in}$	Pull-down current at input DI	V_{DI} = 1.5 V	10	35	50	µA
12.7	$I_{DIR\ in}$	Pull-down current at input DIR	V_{DIR} = 1.5 V	10	35	50	µA
12.8	$I_{PWM\ in}$	Pull-down current at input PWM	V_{PWM} = 1.5 V	10	35	50	µA
12.9	$R_{EN\ in}$	Pull-down resistance at input EN	V_{EN} = V_{CC}	100	210	480	kΩ
12.10	C_{in} (1)	Input capacitance at input CSN, CLK, DI, DIR and PWM	0 V < V_{CC} < 5.3 V		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 13. Charge pump output

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
13.1.1	V_{CP}	Charge pump output voltage	V_S = 6 V; I_{CP} = 15 mA	V_S + 6	V_S + 7	V_S + 7.5	V
13.1.2			V_S = 10 V; I_{CP} = 15 mA	V_S + 11	V_S + 12	V_S + 13.5	V
13.1.3			V_S > 12 V; I_{CP} = 15 mA	V_S + 11	V_S + 12	V_S + 13.5	V
13.2	I_{CP}	Charge pump output current	f_{CP} = f_{SYS_CLK} / 32; V_S = 14 V; V_{CP} = V_S + 10 V	26	38	48	mA
13.3	V_{CP_LOW}	Charge pump low threshold voltage		V_S + 4.5	V_S + 5	V_S + 5.5	V
13.4.1	f_{SYS_CLK}	Clock frequency (internal oscillator)	V_{CC} = 5 V	3	4	4.5	MHz
13.4.2			V_{CC} = 3 V	2.4	3.3	3.5	MHz
13.5	T_{CP}	Charge pump low filter time			64		µs

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Table 14. Gate drivers for external PowerMOS

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Drivers for external high-side PowerMOS							
14.1	$I_{GHx(on)}$	Turn on current (SOURCE stage)	T_j = 25 °C (1)	0.3	0.5(2)	0.8	A
14.2.1	R_{GHx}	On-resistance of SINK stage	V_{SHx} = 0 V; I_{GHx} = 50 mA; T_j = 25°C	3	4	5	Ω
14.2.2			V_{SHx} = 0 V; I_{GHx} = 50 mA; T_j = 125°C	4.5	5.3	7	Ω
14.3	V_{GHxH}	Gate on voltage	Outputs floating	V_{SHx} + 8 V	V_{SHx} + 10 V	V_{SHx} + 12 V	V
14.4	R_{GSHx}	Passive Gate clamp resistance		11	13	15	kΩ
Drivers for external low-side PowerMOS							
14.5	$I_{GLx(on)}$	Turn on current (SOURCE stage)	T_j = 25°C (1)	0.3	0.5(2)	0.8	A
14.6.1	R_{GLx}	On-resistance of SINK stage	V_{SLx} = 0 V; I_{GLx} = 50 mA; T_j = 25°C	3	4	5	Ω
14.6.2			V_{SLx} = 0 V; I_{GLx} = 50 mA; T_j = 125°C	4.5	5.3	7	Ω
14.7	V_{GLxH}	Gate on voltage		V_{SLx} + 8 V	V_{SLx} + 10 V	V_{SLx} + 12 V	V
14.8	R_{GSLx}	Passive gate clamp resistance		11	13	15	kΩ
Timing of the drivers							
14.9	t_{GHxHL}	Propagation delay time high to low	V_S = 13.5 V; V_{SHx} = 0; R_G = 30 Ω; C_G = 4.7 nF	0.8	1.4	1.9	µs
14.10	t_{GLxHL}	Propagation delay time low to high	V_S = 13.5 V; V_{SLx} = 0; R_G = 30 Ω,; C_G = 4.7 nF	0.6	1.2	1.8	µs
14.11	t_{GHxr2}	Rise time	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 4.7 nF	45		170	ns
14.12	t_{GHxf2}	Fall time	V_S = 13.5 V; V_{SHx} = 0; R_G = 0 Ω; C_G = 4.7 nF	60		210	ns
14.13	t_{GLxr2}	Rise time	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 4.7 nF	45		170	ns
14.14	t_{GLxf2}	Fall time	V_S = 13.5 V; V_{SLx} = 0; R_G = 0 Ω; C_G = 4.7 nF	60		210	ns

1. Indirect measurement, parameter measured dynamically using 100 nF load capacitor and evaluating the slew rate.
2. Average value.

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Table 15. Cross current protection time

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
15.1	t_{CCP0}	Cross current protection time	V_{CC} = 5 V, V_S = 13.5 V	—	250(1)	—	ns
15.2	t_{CCP1}	Cross current protection time	V_{CC} = 5 V, V_S = 13.5 V	250	500	750	
15.3	t_{CCP2}	Cross current protection time	V_{CC} = 5 V, V_S = 13.5 V	500	750	1000	
15.4	t_{CCP3}	Cross current protection time	V_{CC} = 5 V, V_S = 13.5 V	700	1000	1300	
15.5	t_{CCP4}	Cross current protection time	V_{CC} = 5 V, V_S = 13.5 V	950	1250	1570	
15.6	t_{CCP5}	Cross current protection time	V_{CC} = 5 V, V_S = 13.5 V	1160	1500	1880	
15.7	t_{CCP6}	Cross current protection time	V_{CC} = 5 V, V_S = 13.5 V	1360	1750	2180	
15.8	t_{CCP7}	Cross current protection time	V_{CC} = 5 V, V_S = 13.5 V	1560	2000	2480	

1. Not tested.

Table 16. Drain source monitoring

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
16.1	V_{SCd1}	Drain - source threshold voltage	—	0.15	0.5	0.7	V
16.2	V_{SCd2}	Drain - source threshold voltage	—	0.45	1	1.25	V
16.3	V_{SCd3}	Drain - source threshold voltage	—	0.9	1.5	1.8	V
16.4	V_{SCd4}	Drain - source threshold voltage	—	1.4	2	2.35	V
16.5	t_{SCd}	Drain - source filter-time	—		6		µs

Table 17. Thermal sense interface (4.5 V < V_{CC} < 5.3 V)

Item	Symbol	Parameter		Min.	Typ.	Max.	Unit
17.1	I_{TS_bias}	Output bias current		200	250	300	µA
17.2	V_{th_TS}	TS threshold voltage	V_{TS} < V_{CC} - 1 V n = number of diodes m = programmed level (0 to 7)		n * (0.31 + m * 0.03)		V

Table 18. Current sense amplifier

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC parameters							
18.1	V_{ICM}	Input voltage range – common mode	V_{CC} = 5 V, V_S = 13 V	-4		V_{CP} - 8 V	V
18.2	V_{IOFF50}	Input offset voltage	V_{CC} = 5 V, V_S = 13 V Gain = 50	-11	-4	3	mV
18.3	V_{IOFF20}	Input offset voltage	V_{CC} = 5 V, V_S = 13 V Gain = 20	-23	-8	7	mV
18.4	V_{IOFF10}	Input offset voltage	V_{CC} = 5 V, V_S = 13 V Gain = 10	-30	-10	10	mV

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Table 18. Current sense amplifier (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
18.5	$V_{IOFF-T50}/\Delta T$	Input offset voltage drift vs. temperature	V_{CC} = 5 V, V_S = 13 V Gain = 50		10(1)		µV/°K
18.6	$V_{IOFF-T20}/\Delta T$	Input offset voltage drift vs. temperature	V_{CC} = 5 V, V_S = 13 V Gain = 20		18(1)		µV/°K
18.7	$V_{IOFF-T10}/\Delta T$	Input offset voltage drift vs. temperature	V_{CC} = 5 V, V_S = 13 V Gain = 10		27(1)		µV/°K
18.8	V_{IOFF-O_50}	Input offset voltage with offset compensation	V_{CC} = 5 V, V_S = 13 V Gain = 50	-3.5	-1	1.5	mV
18.9	V_{IOFF-O_20}	Input offset voltage with offset compensation	V_{CC} = 5 V, V_S = 13 V Gain = 20	-6	-2	4	mV
18.10	V_{IOFF-O_10}	Input offset voltage with offset compensation	V_{CC} = 5 V, V_S = 13 V Gain = 10	-10	-3	6	mV
18.11	P_{SRR_50}	Power supply rejection ratio	V_{CC} = 5 V, V_S = 13 V Gain = 50	39			dB
18.12	P_{SRR_20}	Power supply rejection ratio	V_{CC} = 5 V, V_S = 13 V Gain = 20	31			dB
18.13	P_{SRR_10}	Power supply rejection ratio	V_{CC} = 5 V, V_S = 13 V Gain = 10	25			dB
18.14	CMRR	Input common mode rejection	V_{CC} = 5 V, V_S = 13 V T_j = 25°C, DC	60			dB
18.15	$Gain_{50}$	Gain	V_{CC} = 5 V, V_S = 13 V	46.75	50	53.25	
18.16	$Gain_{20}$	Gain	V_{CC} = 5 V, V_S = 13 V	19	20	21	
18.17	$Gain_{10}$	Gain	V_{CC} = 5 V, V_S = 13 V	9.5	10	10.5	
18.18.1	V_{CSOh}	High-level output voltage	V_{CC} = 5 V, V_S = 13 V I_{OUT} = 2 mA	V_{CC} - 250 mV			V
18.18.2			V_{CC} = 5 V, V_S = 13 V I_{OUT} = 200 µA	V_{CC} - 50 mV	V_{CC} - 20 mV		V
18.19.1	V_{CSOl}	Low-level output voltage	V_{CC} = 5 V, V_S = 13 V I_{OUT} = -2 mA		100	250	mV
18.19.2			V_{CC} = 5 V, V_S = 13 V I_{OUT} = -200 µA		15	50	mV
Dynamic parameters							
18.20	SRcso_10	CSO slew rate	V_{CC} = 5 V, V_S = 13 V Gain = 10; RL = 1 kΩ,; CL = 22 pF		2.8	4	V/µs
18.21	SRcso_20	CSO slew rate	V_{CC} = 5 V, V_S = 13 V Gain = 20; RL = 1 kΩ,; CL = 22 pF		3	4.5	V/µs

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Table 18. Current sense amplifier (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
18.22	SRcso_50	CSO slew rate	V_{CC} = 5 V, V_S = 13 V Gain = 50; RL = 1 kΩ,; CL = 22 pF		4.4	6	V/µs
18.23	I_{CSI_10}	CSI input current	V_{CC} = 5 V, V_S = 13 V Gain = 10	-114	-102	-90	µA
18.24	I_{CSI_20}	CSI input current	V_{CC} = 5 V, V_S = 13 V Gain = 20	-80	-72	-64	µA
18.25	I_{CSI_50}	CSI input current	V_{CC} = 5 V, V_S = 13 V Gain = 50	-39	-33	-27	µA

1. Not tested, guaranteed by design.

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Figure 4. Output timing diagram (active free wheeling)

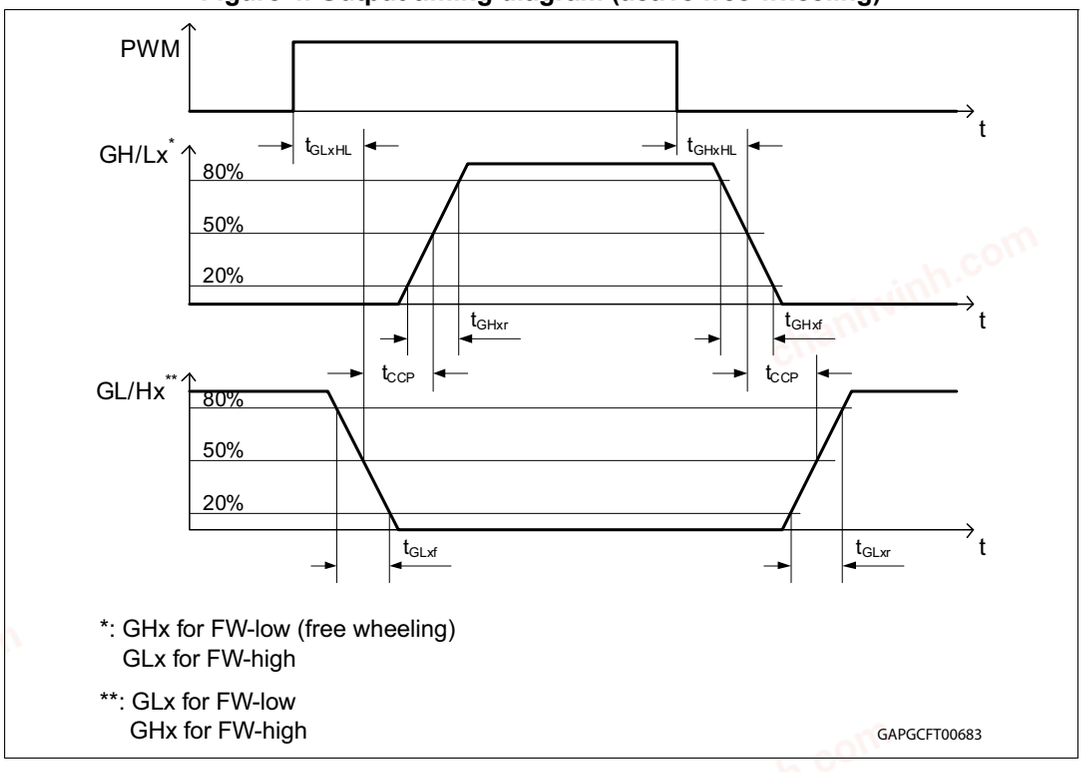
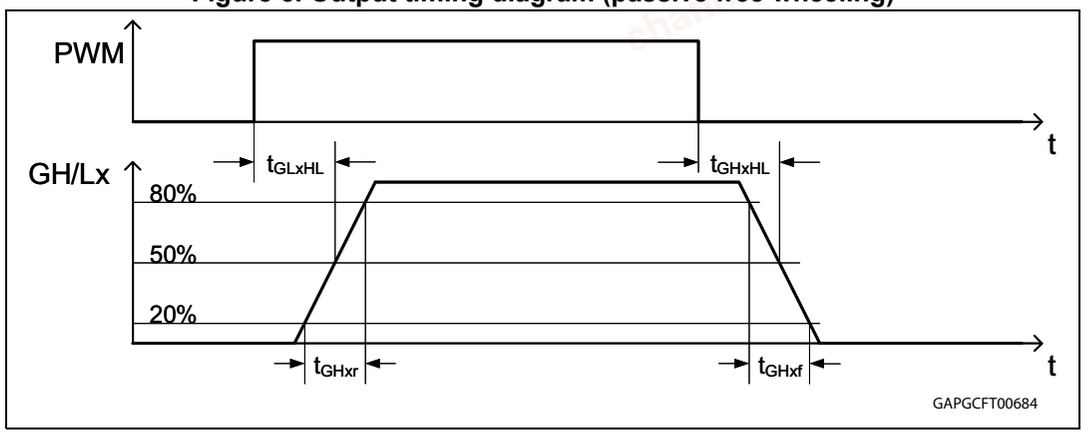


Figure 5. Output timing diagram (passive free wheeling)



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2.5 SPI - electrical characteristics

V_S = 6 V to 28 V, V_{CC} = 3 V to 5.3 V, T_j = -40°C to 150°C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

DI timing parameters tested in production by a passed/failed test:

- Tj = -40°C / +25°C: SPI communication @ 2 MHz.
- Tj = +125°C: SPI communication @ 1.25 MHz.

Table 19. DI timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
19.1	t_{CLK}	Clock period	—	1000	—		ns
19.2	t_{CLKH}	Clock high time	—	400	—		ns
19.3	t_{CLKL}	Clock low time	—	400	—		ns
19.4	$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	—	400	—		ns
19.5	$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	—	400	—		ns
19.6	$t_{set\ DI}$	DI setup time	—	200	—		ns
19.7	$t_{hold\ DI}$	DI hold time	—	200	—		ns
19.8	$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	—		—	100	ns
19.9	$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	—		—	100	ns

Table 20. DO

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
20.1	V_{DOL}	Low-level output voltage	I_D = -4 mA		0.2	0.4	V
20.2	V_{DOH}	High-level output voltage	I_D = 4 mA	V_{CC} - 0.4	V_{CC} - 0.2		V
20.3	I_{DOLK}	Tristate leakage current	$V_{CSN} = V_{CC}$; 0 V < V_{DO} < V_{CC}	-10		10	µA
20.4	C_{DO}(1)	Tristate input capacitance	$V_{CSN} = V_{CC}$; 0 V < V_{CC} < 5.3 V		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

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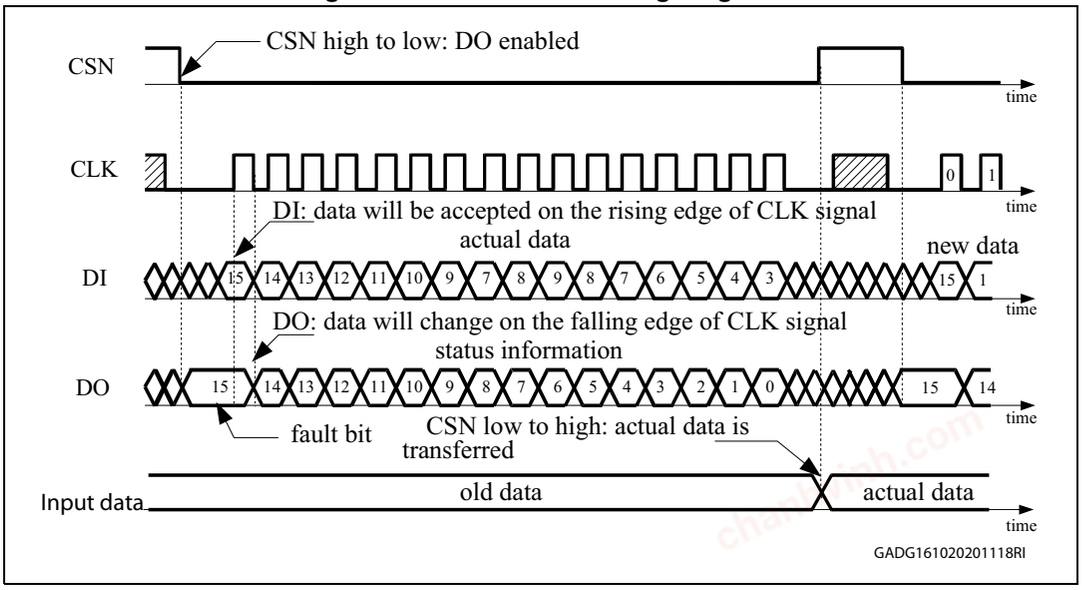
Table 21. DO timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
21.1	$t_{r\ DO}$	DO rise time	C_L = 100 pF; I_{load} = -1 mA	—	80	140	ns
21.2	$t_{f\ DO}$	DO fall time	C_L = 100 pF; I_{load} = 1 mA	—	50	100	ns
21.3	$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low-level	C_L = 100 pF; I_{load} = 1 mA; pull-up load to V_{CC}	—	100	250	ns
21.4	$t_{dis\ DO\ L\ tri}$	DO disable time from low-level to tristate	C_L = 100 pF; I_{load} = 4 mA; pull-up load to V_{CC}	—	380	450	ns
21.5	$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high-level	C_L = 100 pF; I_{load} = -1 mA; pull-down load to GND	—	100	250	ns
21.6	$t_{dis\ DO\ H\ tri}$	DO disable time from high-level to tristate	C_L = 100 pF; I_{load} = -4 mA; pull-down load to GND	—	380	450	ns
21.7	$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V_{CC}; V_{DO} > 0.7 V_{CC}; C_L = 100 pF	—	50	250	ns

Table 22. EN, CSN timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
22.3	$t_{CSN_HI,min}$	CSN HI time, active mode: the min high time between two independent SPI commands.	Transfer of SPI-command to input register	2			µs

Figure 6. SPI - transfer timing diagram



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Figure 7. SPI - input timing

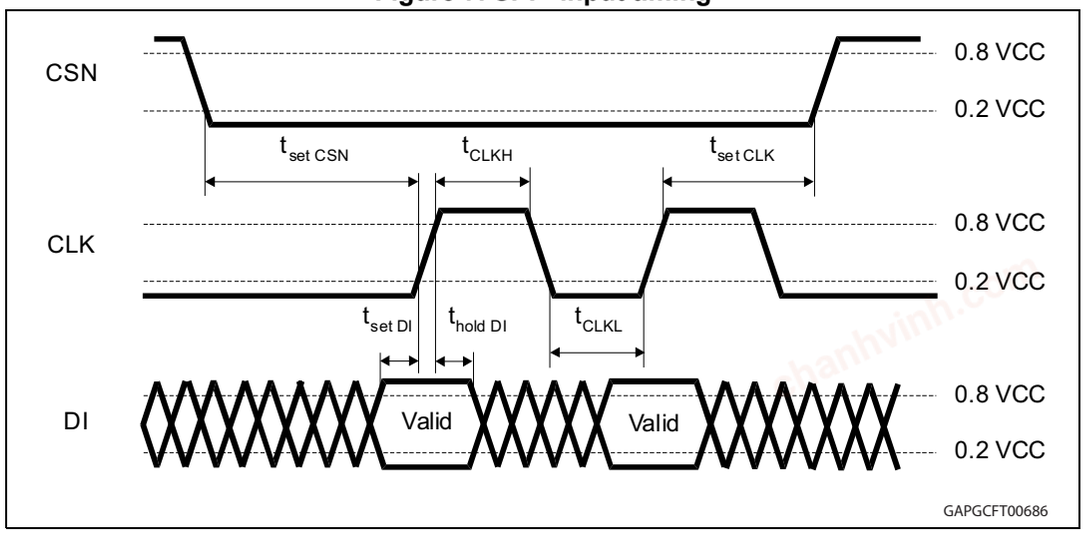
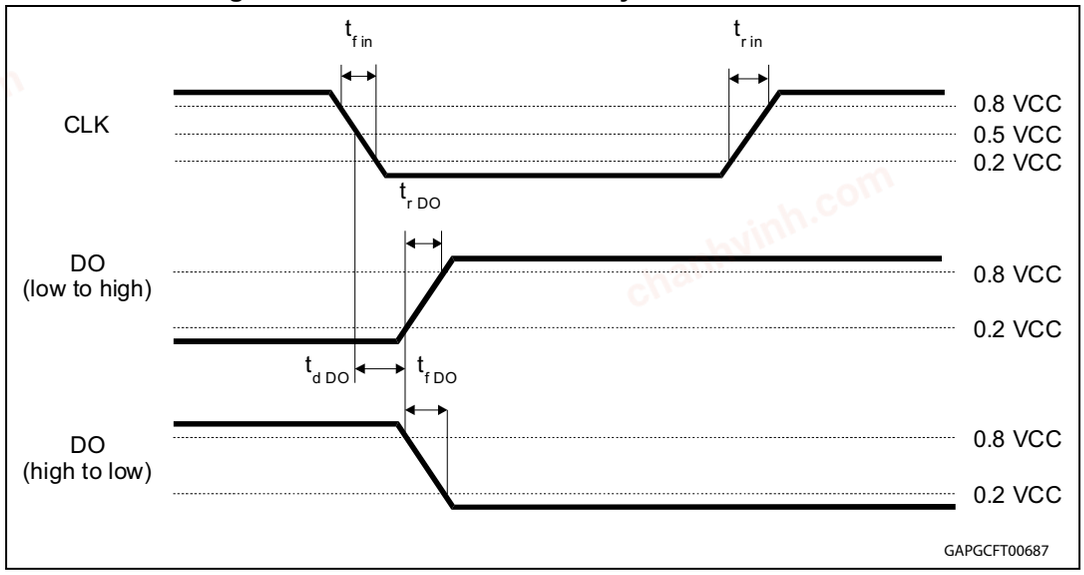


Figure 8. SPI - DO valid data delay time and valid time



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Figure 9. SPI - DO enable and disable time

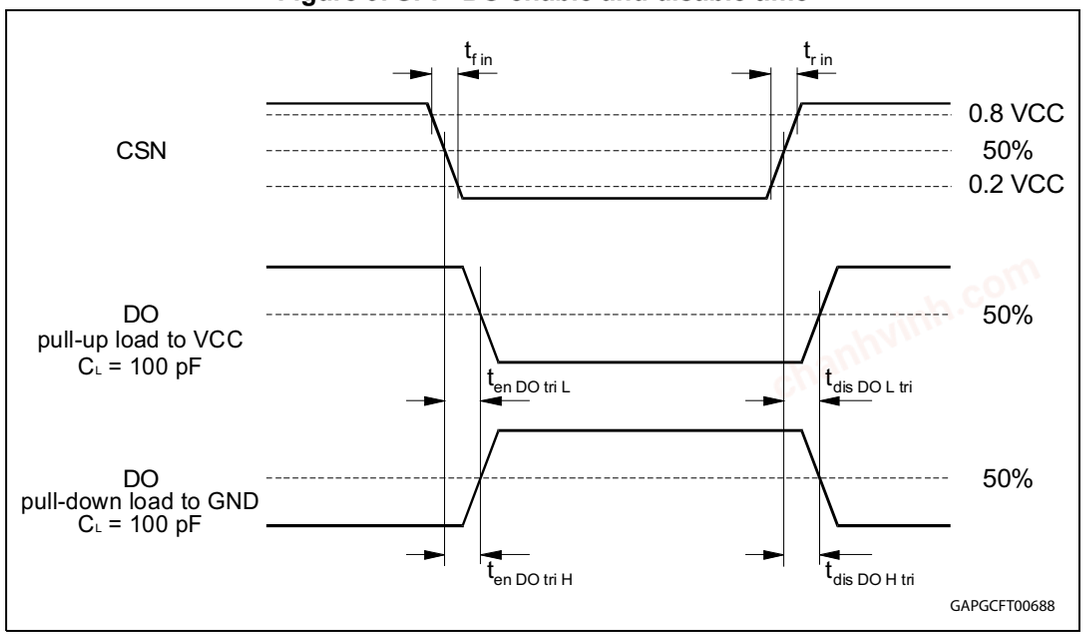
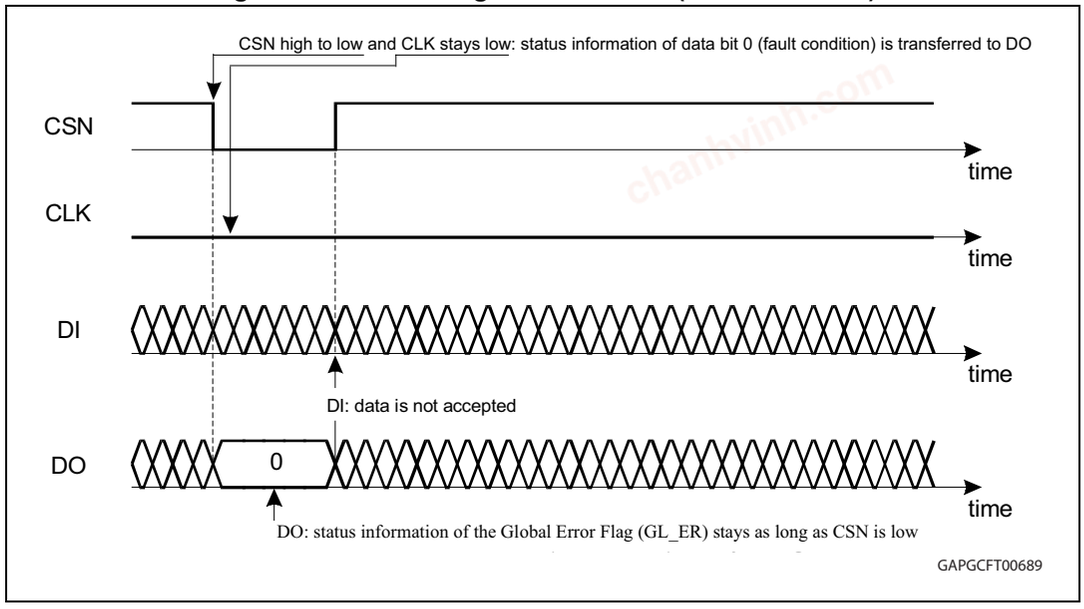


Figure 10. SPI - timing of status bit 0 (fault condition)



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3 Device description

3.1 Dual power supply: V_S and V_{CC}

The power supply Vs supplies the charge pump and the gate drivers. An internal charge-pump is used to drive the high-side switches and the low-side switches. The supply voltage V_{CC} (3.3 V / 5 V) is used for the logic part, the SPI of the device and for the output stage of the current sense amplifier. Due to the independent logic supply voltage the control and the status information is not lost, even if the supply voltage V_S is switched-off. In case of power-on (V_{CC} increases from undervoltage to $V_{POR\ OFF}$ = 2.5 V, typical) the circuit is initialized by an internally generated power-on reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON}$ = 2.2 V, typical), the outputs are switched-off and the status and the control registers are reset to default values.

3.2 Standby mode (EN)

The L99H02 is activated with enable input high. For enable input floating (not connected) or V_{EN} = 0 V the device is in standby mode. In standby mode all latched data are cleared and inputs and outputs are switched-off. In standby mode the current at V_S is less than 5 µA (1 µA) for CSN = high (DO in tristate). If $V_{CC} > V_{POR\ OFF}$ and EN = high the device enters the active mode.
In active mode the diagnostic functions are active. In fact gate drivers and charge pump status will depend on the fault flags. For example if the device enters in active mode with VS>VSOV the charge pump will be disabled.

3.3 H-bridge control (DIR, PWM, bit FW)

The DIR and PWM inputs control the drivers of the external H-bridge transistors. The motor direction can be chosen with the DIR input, the duty cycle and frequency with the PWM input. With the SPI bits FW and FW-PAS 4 different free wheeling modes (2 active and 2 passive) can be selected by using the high-side transistors or the low-side transistors. Unconnected inputs are defined by internal pull-down current.

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Table 23. Truth table

N°	Control pins				Control bits		Failure bits						Output pins				SPI DO	Comment
	EN	DIR	PWM	TS/ACT_OFF	FW	FW_PAS	CP_LOW	OV	UV	DS_MON	TSD	WDTO	GH1	GL1	GH2	GL2	GL_ER	
1	0	X	X	X	X	X	X	X	X	X	X	X	RL	RL	RL	RL	T	Standby mode
2	1	X	X	X	X	X	X	X	X	X	X	X	RL	RL	RL	RL	1	Power-on reset
3	1	X	X	0	X	X	0	0	0	0	0	0	L	L	L	L	0	EXT_TS = 1 (external thermal shutdown)
4	1	X	X	0	X	X	0	0	0	0	0	0	L	L	L	L	0	EXT_TS = 0 (active Off)
5	1	X	X	1	X	X	1	0	0	0	0	0	RL	RL	RL	RL	0	Charge pump voltage too low
6	1	X	X	1	X	X	0	0	0	0	1	0	RL	RL	RL	RL	1	Internal thermal shutdown
7	1	X	X	1	X	X	0	1	0	0	0	0	L	L	L	L	1	V_S overvoltage
8	1	X	X	1	X	X	0	0	1	0	0	0	L	L	L	L	1	V_S undervoltage
9	1	X	X	1	X	X	0	0	0	1	0	0	L(1)	L(1)	L(1)	L(1)	0	Short-circuit(1)
10	1	X	X	1	X	X	0	0	0	0	0	1	L	L	L	L	1	Watchdog time out
11	1	0	1	1	X	X	0	0	0	0	0	0	L	H	H	L	0	-
12	1	X	0	1	0	0	0	0	0	0	0	0	L	H	L	H	0	Act. free wheeling mode LS
13	1	0	0	1	0	1	0	0	0	0	0	0	L	H	L	L	0	Pass. free wheeling mode LS
14	1	1	0	1	0	1	0	0	0	0	0	0	L	L	L	H	0	Pass. free wheeling mode LS
15	1	1	1	1	X	X	0	0	0	0	0	0	H	L	L	H	0	-
16	1	X	0	1	1	0	0	0	0	0	0	0	H	L	H	L	0	Act. free wheeling mode HS
17	1	0	0	1	1	1	0	0	0	0	0	0	L	L	H	L	0	Pass. free wheeling mode HS
18	1	1	0	1	1	1	0	0	0	0	0	0	H	L	L	L	0	Pass. free wheeling mode HS

1. Only the half bridge (low-side and high-side) where one MOSFET is in short-circuit condition is switched-off. Both MOSFETs of the other half bridge remain active and driven by DIR and PWM.

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Symbols:

- **x**: Don't care
- **1**: Logic high or active
- **0**: Logic low or not active
- **H**: Output in source condition
- **L**: Output in sink condition
- **RL**: Resistive low (see *Section 3.4: Resistive low*)
- **T**: Tristate
- **FW**: Free wheeling
- **FW_PAS**: Free wheeling passive
- **CP_LOW**: Charge pump low
- **OV**: Overvoltage
- **UV**: Undervoltage
- **DS_MON**: Short-circuit
- **TSD**: Thermal shutdown
- **GL_ER**: Global error flag

3.4 Resistive low

The resistive low output mode protects the L99H02 and the H-bridge in standby mode and in some failure modes (internal thermal shutdown (TSD), charge pump low (CP_LOW), stucked reset (STK_RESET_Q) and power-on reset (POR). When a gate driver changes into the resistive low output mode due to a failure a sequence is started. In this sequence the concerning driver is switched in sink condition for 32 µs to 64 µs to ensure a fast switch-off of the H-bridge transistor. Afterwards the driver is switched in the resistive output mode (resistive path to source).

3.5 Diagnostic functions

The diagnostic functions (over load, power supply over- and undervoltage, charge pump low, watchdog, temperature warning and internal/external thermal shutdown) are internally filtered and the condition has to be valid for at least 64 µs (6 µs for a short-circuit) before the corresponding status bit in the status registers is set. The filters are used to improve the noise immunity of the device. The internal temperature warning function is intended for information purpose and does not change the state of the output drivers. On the contrary, the over load condition switches the corresponding half bridge in sink condition. The internal thermal shutdown condition and charge pump low disable all drivers (resistive low). The external thermal shutdown, watchdog, over- and undervoltage condition switch all drivers in sink condition. The microcontroller needs to clear the status bits to reactivate the drivers.

3.6 Overvoltage and undervoltage detection

If the power supply voltage V_S rises above the overvoltage threshold V_{VS_OV} (typical 20 V / 30 V), all gate driver stages are switched in sink condition to protect the H-bridge and the load, setting the OV flag. Two values for the overvoltage threshold can be selected with the SPI. When the voltage V_S drops below the undervoltage threshold

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V_{VS_UV}, all gate driver stages are switched in the sink condition to avoid driving the power devices without sufficient gate driving voltage (increased power dissipation), setting the UV bit. In both cases, overvoltage and undervoltage detection, the charge pump is disabled. If the supply voltage V_S recovers from UV/OV to normal operating voltage range and if the OV_UV_RD is set to 0, then the charge pump is automatically enabled. In any case, regardless of the OV_UV_RD bit value, the microcontroller needs to clear the status register to reactivate the gate drivers.

Note: In particular when the OV_UV_RD control bit is set to one, two status register clear operations are needed to reactivate the gate drivers, one to clear the OV/UV flag and turn on the charge pump and one to clear the CP_LOW flag.

3.7 Charge pump

The charge pump uses 2 external capacitors. The output of the charge pump has a current limitation. In standby mode and after overvoltage, undervoltage or a thermal shutdown has been triggered the charge pump is disabled. If the charge pump output voltage drops below the charge pump low voltage threshold for longer than T_{CP}, the CP_LOW flag is set and all gate drivers are switched-off (resistive output, see *Section 3.4: Resistive low*). The CP_LOW flag has to be cleared through a software reset to reactivate the gate drivers.

3.8 Temperature warning and thermal shutdown

If junction temperature rises above T_{jTWON} the temperature warning flag TW is set and detectabled via the SPI. If junction temperature rises above the second threshold T_{jSDON}, the thermal shutdown flag (TSD) is set and the gate drivers and the charge pump are switched-off to protect the device. The gates of the H-bridge are discharged by the resistive low mode (see *Section 3.4: Resistive low*). In order to reactivate the output stages the junction temperature must decrease below $T_{j\ SD\ OFF}$ and the thermal shutdown flag has to be cleared by the microcontroller.

3.9 Short-circuit detection / drain source monitoring

The drain - source voltage of each activated external MOSFET of the H-bridge is monitored by comparators to detect shorts to ground or battery. If the voltage drop over the external MOSFET exceeds the threshold voltage V_{SCd} for longer than the short current detection time t_{SCd} the corresponding gate driver switches the external MOSFET off and the corresponding drain source monitoring flag (DS_MON_[3:0]) is set. Until this failure flag is reset the corresponding half bridge is in sink condition. The DS_MON flags have to be cleared through a software reset to reactivate the gate drivers. The drain source monitoring has a nominal filter time of 6 µs. This monitoring is only active when the corresponding gate driver is in source condition. The threshold voltage V_{SCd} can be programmed in 4 steps between 0.5 V and 2 V with the SPI.

3.10 Programmable cross current protection

The external Power MOSFET's transistors in H-bridge (two half bridges) configuration are switched-on with an additional delay time t_{CCP} to prevent cross current in the half bridge. The cross current protection time t_{CCP} can be programmed with the SPI.

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3.11 Current sense amplifier (CSA)

The current sense amplifier (CSA) is specially designed for current sensing in automotive applications. It is a bidirectional, single-supply amplifier for amplifying small differential voltages in a wide common mode voltage range (-4 V to (V_{CP} - 8) V). It supports the current measurement at two shunts. The result of the respective shunt can be multiplexed to the microcontroller compatible output voltage by a SPI command.

A gain of 50, 20 or 10 is SPI programmable. The inputs (CSI1+ / CSI1- and CSI2+ / CSI2-) are built as a transconductance stage. Therefore a series resistor (for filtering etc.) should not exceed 50 Ω to keep the additional gain error below 1%.

The output works at half scale: V_{CSO0} = (0,5 * V_{CC}) V for V_{IDIFF} = 0 V. An internal offset measurement is in normal mode available with the "OFF_CAL" SPI-bit. If this bit is set to logic "1" the input pins are disconnected from the amplifier and a virtual zero input differential voltage is selected.

3.12 Thermal sensor interface / H-bridge switch-off input

The TS/ACT_OFF input pin is configurable by SPI with the EXT_TS bit. This pin could be used as temperature sensor interface for the power stage temperature sensors or as external switch off input for the power stage (all the external MOSFETs). The output bias current for the power stage temperature sensors ITS_bias is on for EN = high.

3.12.1 EXT_TS-bit = low (active off)

The TS/ACT_OFF input is used as a logic driver control input, without filter delay and without latching the information.

Pulling the TS/ACT_OFF pin below the programmed threshold shuts off all the MOSFETs and sets the OT_EXT bit.

Increasing the voltage at TS/ACT_OFF pin above the programmed threshold brings back the MOSFETs to the status set by DIR and PWM-pins and resets the OT_EXT bit.

The threshold is programmable by SPI with the bits EXTTH_5:0.

3.12.2 EXT_TS-bit = high (thermal sensor interface)

The thermal sensor interface together with the thermal sensor diodes, can be used to control the temperature of the external H-bridge. When the drop over the diodes chain decreases below the reference voltage for longer than the internal filter time (64 µs) the OT_EXT bit is set and the drivers switch in sink condition.

In this mode the OT_EXT-status-bit has to be cleared through a software reset to reactivate the gate drivers.

The threshold is programmable by SPI with the bits EXTTH_5:0.

3.13 Watchdog

The task of the watchdog is to monitor the microcontroller during normal operation within a nominal trigger cycle of 60 ms. The microcontroller has to restart the watchdog timer by setting the watchdog restart bit via SPI repeatedly within the watchdog time T_{WDTO}. If no

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correct watchdog trigger is sent from the microcontroller, all gate drivers switch in sink condition and the watchdog time out flag (WDTO) is set. Once a watchdog time out is detected, the gate drivers can only be reactivated by sending a software reset.

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4 Functional description of the SPI

4.1 Signal description

4.1.1 Serial clock (CLK)

This input signal provides the timing of the serial interface. Data present at serial data input (DI) is latched on the rising edge of serial clock (CLK). Data on Serial Data Out (DO) is shifted out at the falling edge of serial clock (CLK).

The serial clock CLK must be active only during a frame (CSN low phase). Any other switching of CLK close to any CSN edge could generate setup/hold violations in the SPI logic of the device.

4.1.2 Serial data input (DI)

This input is used to transfer data serially into the device. Values are latched on the rising edge of serial clock (CLK).

4.1.3 Serial data output (DO)

This output is used to transfer data serially out of the device. Data is shifted out on the falling edge of serial clock (CLK).

DO also reflects the status of the <*Global Error Flag*> (<*Global Status Byte*>*[7]*) while CSN is low and no clock signal is present.

4.1.4 Chip select not (CSN)

When this input signal is high, the communication interface of the device is deselected and serial data output (DO) is high impedance. Driving this input low enables the communication. The communication must start and stop on a low-level of serial clock (CLK).

The SPI can be driven by a microcontroller with its SPI peripheral running in the following mode: CPOL = 0 and CPHA = 0.

For timing details and figures refer to *Section 2.5: SPI - electrical characteristics*

4.2 General data description

The SPI communication is based on a SPI interface structure using CSN (chip select not), DI (serial data in), DO (serial data out/error) and CLK (serial clock) signal lines.

Each DI communication frame consists of a <*Command Byte*> which is followed by 1 <*Data Byte*>.

The data returned on DO within the same frame always starts with the <*Global Status Byte*>, which provides general status information about the device. This byte is followed by 1 <*Data Byte*> (*'In-frame-response'*).

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Table 24. DI

Command byte								DI - data byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC1	OC0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 25. DO

Global Status byte								DO - data byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GL_ER	FE	STK_RESET_Q	TSD	TW	UV	OV	WDTO	D7	D6	D5	D4	D3	D2	D1	D0

4.2.1 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (*<Read>, <Write>, <Clear status>, <Read Device Information>*) and a 6-bit address.

Table 26. Command byte

Command byte							
MSB							LSB
Op code		Address					
OC1	OC0	A5	A4	A3	A2	A1	A0

Comments:

- **OCx**: Operating code
- **Ax**: Address

4.2.2 OpCode definition

Table 27. Operating code definition

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Clear Status>
1	1	<Read Device Information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device. The *<Clear Status>* operation is used to read a status register and subsequently clear its content. *<Read Device Information>* allows access to the ROM area which contains device related information such as <ID-Header>, <Product Code>, <Silicon Version and Category> and *<SPI-frame-ID>.*

More detailed descriptions of the *device information* are available in *Section 4.7*.

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4.3 Device memory map

4.3.1 Control and status (RAM) address map

Table 28. Control and status (RAM) address map

Name	Access	Address						Content							
		A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Start Reg0	Read/ Clear	0	0	0	0	0	0	DS_MON_3	DS_MON_2	DS_MON_1	DS_MON_0	0	0	OT_EXT	CP_LOW
Start Reg1	Read/ Write	0	0	0	0	0	1	RWD	FW_PAS	OFF_CAL	CLK_SPCTR	OVT	OV_UV_RD	DIAG_1	DIAG_0
Start Reg2	Read/ Write	0	0	0	0	1	0	RWD	COPT_2	COPT_1	COPT_0	FW	MCSA	GCSA_1	GCSA_0
Start Reg3	Read/ Write	0	0	0	0	1	1	RWD	EXT_TS	EXTTH_5	EXTTH_4	EXTTH_3	EXTTH_2	EXTTH_1	EXTTH_0

4.3.2 Device (ROM) address map (access with OC0 and OC1 set to ‘1’)

Table 29. Device (ROM) address map (access with OC0 and OC1 set to ‘1’)

Name	Access	Address						Content							
		A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
ID-Header	Read device	0	0	0	0	0	0	FAM_1	FAM_0	NR_PI_5	NR_PI_4	NR_PI_3	NR_PI_2	NR_PI_1	NR_PI_0
Product code 1	Read device	0	0	0	0	0	1	PR_ID_7	PR_ID_6	PR_ID_5	PR_ID_4	PR_ID_3	PR_ID_2	PR_ID_1	PR_ID_0
Product code 2	Read device	0	0	0	0	1	0	PR_ID_15	PR_ID_14	PR_ID_13	PR_ID_12	PR_ID_11	PR_ID_10	PR_ID_9	PR_ID_8
SPI-frame-ID	Read device	0	0	0	0	1	1	BR	AR5	AR4	AR3	32 bits	24 bits	16 bits	8 bits
Reserved	Read device	1	1	1	1	1	1	Reserved, accessing this address is recognized as a failure, the device enters a fail-safe state (see *Table 30*).							

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4.4 Global Status Byte

The Global Status Byte is the first byte shifted out at every SPI access.

The GL_ER bit is present at DO with the falling edge of CSN.

This byte can be reset with the command <clear status>.

The <clear status> command represents a software reset.

Table 30. Global Status Byte

Bit	15	14	13	12	11	10	9	8
Name	GL_ER	FE	STK_RESET_Q	TSD	TW	UV	OV	WDTO
<default>	0	0	1	0	0	0	0	0

Comments:

- **GL_ER**: Global Error Flag. This signal is a logical OR among all the errors of the Global Status Byte (<Global Status Register>[8:14]).
- **FE**: Frame Error. If the number of clock pulses within the previous frame is not 16 the frame is ignored and this bit is set.
- **STK_RESET_Q**: if a stuck at ‘1’ on SPI_DI during any SPI frame occurs, or if a power-on reset occurs, the STK_RESET_Q is set '0'.
  STK_RESET_Q is reset (‘1’) with any SPI command.
  When STK_RESET_Q is active (‘0’), the gate drivers are switched-off (see *Section 3.4: Resistive low*).
  After a startup of the circuit the STK_RESET_Q is active because of the POR pulse and the gate drivers are switched-off. The Gate drivers can only be activated after the STK_RESET_Q has been reset with a SPI command.
- **TSD**: Thermal Shutdown due to internal sensor. All the gate drivers and the charge pump are switched-off (see *Section 3.4: Resistive low*). The gate drivers can only be activated after the TSD has been reset with a SPI command.
- **TW**: Thermal Warning
- **UV**: V_S Undervoltage
- **OV**: V_S Overvoltage
- **WDTO**: Watchdog time out.

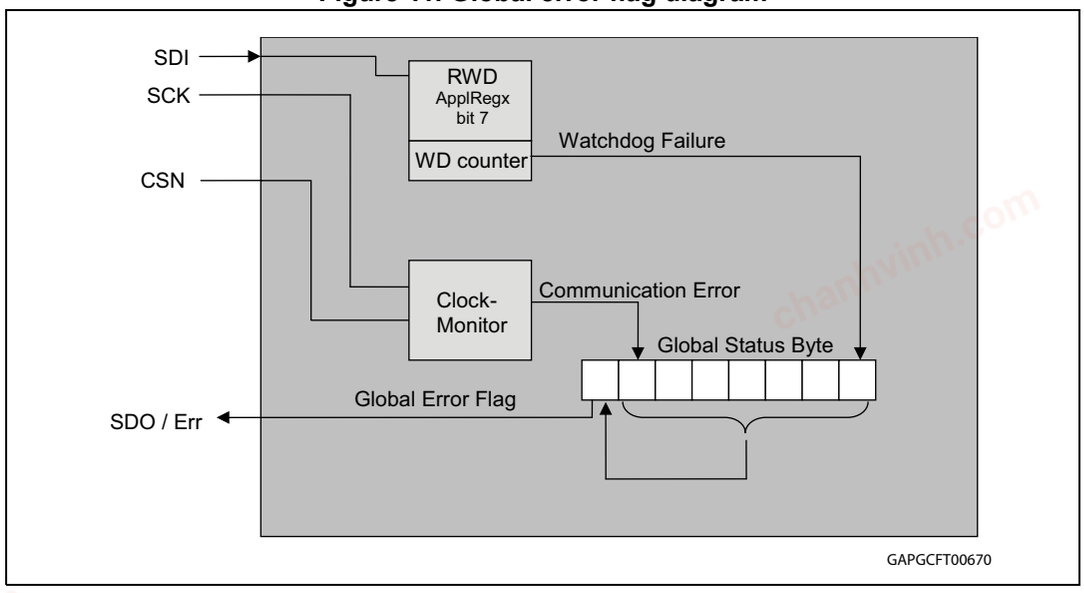
Failures of <*Global Status Byte*>[8:14] are always linked to the <*Global Error Flag*>.

The Global Error Flag is reflected via the DO pin while CSN is held low and no clock signal is available. The flag remains as long as CSN is low. This operation does not cause the <communication error> bit (FE) in the <Global Status Byte> to be set.

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4.4.1 SPI clock monitor and watchdog

Figure 11. Global error flag diagram



Note: Writing a "1" to RWD - bit in ApplRegx restarts the internal watchdog counter.

The clock monitor counts the number of clock pulses during a communication frame (while CSN is low). If the number of SCK pulses does not correspond with the frame width indicated in the <SPI-frame-ID> (ROM address 03hex) the frame is ignored and the bit *<frame error>* in the *<Global Status Byte>* is set.

Note: Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

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4.5 Detailed byte description of status register (StatReg0)

The read operation starts always with the command byte followed by 1 data byte. The content of the send data byte has to be ‘0’. The content of the addressed register is shifted out at DO within the same frame (‘in-frame response’).

The device uses 1 status register to monitor the status of the device. *Table 31* shows the address and the content of the register.

Note: The errors of the status register are not linked to the <Global Error Flag>.

Table 31. Address 0<00(hex)>:StatReg 0 - read clear

Bit	7	6	5	4	3	2	1	0
Name	DS_MON_3	DS_MON_2	DS_MON_1	DS_MON_0	X	X	OT_EXT	CP_LOW
<default>	0	0	0	0	0	0	0	0

Comments:

- **DS_MON[3:0]**: if max drain source voltage exceeds the defined thresholds, the DS_MON are set and the corresponding drivers go to sink mode. In particular both gate drivers of the faulty leg will be in sink mode until the DS_MON flag of one of its switch is reset. The DS_MON bits have to be cleared through a software reset to reactivate the drivers.

Table 32. DS_MON - drivers relations

Register	Deactivated driver
DS_MON_3	High-side 2
DS_MON_2	High-side 1
DS_MON_1	Low-side 2
DS_MON_0	Low-side 1

- **OT_EXT**: Depending on EXT_TS bit, the following two meanings exist:
  - EXT_TS = low (active off):
    TS/ACT_OFF pin is used as input to switch the H-bridge in tristate and back.
    Details are described in *Section 3.12.1*.
  - EXT_TS = high (thermal sensor interface):
    TS/ACT_OFF pin is used as thermal sensor interface for external temperature diodes. Details are described in *Section 3.12.1*.
- **CP_LOW**: if a charge pump output low voltage event occurs, all gate drivers are switched-off (resistive low). The CP_LOW bit has to be cleared through a software reset to reactivate the gate driver.

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4.6 Detailed byte description of application registers (ApplRegX)

The write/read operation starts always with a command byte followed by 1 data byte.

4.6.1 Description of the data byte

The device uses 3 application registers to configure the device. The default values represent the bits values after a POR event.

Table 33. Address 1 <01(hex)>:ApplReg1-read/write

Bit	7	6	5	4	3	2	1	0
Name	RWD	FW_PAS	OFF_CAL	CLK_SPCTR	OVT	OV_UV_ RD	DIAG1	DIAG0
<default>	0	0	0	0	0	0	0	0

Comments:

- **RWD**: restarts the watchdog counter by setting the bit to one
- **FW_PAS**: enables passive free wheeling according to *Table 23*
- **OFF_CAL**: offset calibration mode for CSA
- **OVT:** overvoltage threshold selection
- **CLK_SPCTR**: switch the clock to the charge pump
  - **0**: 125 Khz (50% duty cycle)
  - **1**: pulses train (max = 8 µs, min = 2 µs) to optimize power spectrum

Table 34. Overvoltage threshold of the Vs monitoring

OVT	Threshold
0	20 V
1	29 V

- **OV_UV_RD**: over/undervoltage recovery disabled.
  - 0: if V_S recovers from OV/UV condition to normal operating voltage range, the charge pump is automatically enabled;
  - 1: if V_S recovers from OV/UV condition to normal operating voltage range, the charge pump remains disabled;

  In both cases the microcontroller has to clear the status register to enable the gate drivers
- **DIAG[1:0]**: drain source monitoring threshold voltage selection

Table 35. DIAG monitoring of source voltages

DIAG[1]	DIAG[0]	Monitoring threshold voltage
0	0	V_{SCd1}= 0.5 V
0	1	V_{SCd2} = 1 V
1	0	V_{SCd3} = 1.5 V
1	1	V_{SCd4} = 2 V

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Table 36. Address 2 <02(hex)>: ApplReg2 – read/write

Bit	7	6	5	4	3	2	1	0
Name	RWD	COPT_2	COPT_1	COPT_0	FW	MCSA	GCSA_1	GCSA_0
<default>	0	0	0	0	0	0	0	0

Comments:

- **RWD**: restarts the watchdog counter by setting the bit to one
- **COPT[2:0]**: filter time to protect the two external half bridges against cross current

Table 37. Cross current protection time (t_{CCP})

COPT_2	COPT_1	COPT_0	Protection time
0	0	0	250 ns
0	0	1	500 ns
0	1	0	750 ns
0	1	1	1000 ns
1	0	0	1250 ns
1	0	1	1500 ns
1	1	0	1750 ns
1	1	1	2000 ns

- **FW**: selects high-side or low-side free wheeling
- **MCSA**: multiplexer for current sense amplifier.

Table 38. Multiplexer for current sense amplifier

MCSA	Selected amplifier
0	CSA2 (CSI2+ / CSI2-)
1	CSA1 (CSI1+ / CSI1-)

- **GCSA[1:0]**: gain of the current sense amplifier.

Table 39. Gain of current sense amplifier

GCSA_1	GCSA_0	Gain
0	0	10
0	1	20
1	0	50
1	1	Not applicable

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Table 40. Address 3 <03(hex)>: ApplReg3 – read/write

Bit	7	6	5	4	3	2	1	0
Name	RWD	EXT_TS	EXTTH_5	EXTTH_4	EXTTH_3	EXTTH_2	EXTTH_1	EXTTH_0
<default>	0	0	0	0	0	0	0	0

Comments:

- **RWD**: restarts the watchdog counter by setting the bit to one
- **EXT_TS**: the bit selects the mode of the input pin TS/ACT_OFF:
  - EXT_TS = low (active off):
    TS/ACT_OFF pin is used as input to switch the H-bridge in tristate and back.
    Details are described in *Section 3.12.1*.
  - EXT_TS = high (thermal sensor interface):
    TS/ACT_OFF pin is used as thermal sensor interface for external temperature diodes. Details are described in *Section 3.12.2*.
- **EXTTH[5:0]**: determines the threshold of the external thermal shutdown

Table 41. External threshold voltage, factor n

EXTTH_5	EXTTH_4	EXTTH_3	n
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

Table 42. External threshold voltage, factor m

EXTTH_2	EXTTH_1	EXTTH_0	m
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

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Equation 1

$V_{th} = n * (0.31 + m * 0.03)$ V

The purpose of factor n is to determine the number of external temperature sense diodes (in series). With factor m the level of the threshold voltage can be fine tuned.

4.7 Read device information (ROM)

The device information is stored at the ROM addresses defined below and it is read using the corresponding operating code.

Table 43. Read device information (ROM)

Op code		Address	Device information
OC1	OC0	Ax	
1	1	00H	<ID-Header>
1	1	01H	<Product Code 1>
1	1	02H	<Product Code 2>
1	1	03H	<SPI-frame-ID>
1	1	3FH	Reserved, accessing this address is recognized as a failure, the device enters a fail-safe state (see *Table 30: Global Status Byte*).

The <ID-Header> indicates the product family and specifies how many bytes of device information are available.

In *Table 44* the register is addressable only through a read device information command.

Table 44. Address 0 <00(hex)>: ID-header - read only

Bit	7	6	5	4	3	2	1	0
Name	FAM_1	FAM_0	NR_PI_5	NR_PI_4	NR_PI_3	NR_PI_2	NR_PI_1	NR_PI_0
<default>	0	1	0	0	0	0	1	0

- **FAM[1:0]**: family identifier, FAM[1:0] = [0:1] stands for ASSPs.
- **NR_PI[5:0]**: number of product information bytes.

The <*Product Code 1 and 2*> represents a unique identifier of the device and version.

In *Table 45* the register is addressable only through a read device information command.

Table 45. Address 1 <01(hex)>: product ID (LSB) - read only

Bit	7	6	5	4	3	2	1	0
Name	PR_ID_7	PR_ID_6	PR_ID_5	PR_ID_4	PR_ID_3	PR_ID_2	PR_ID_1	PR_ID_0
<default>	0	0	0	0	0	0	0	1

In *Table 46* the register is addressable only through a read device information command.

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Table 46. Address 2 <02(hex)>: product ID (MSB) - read only

Bit	7	6	5	4	3	2	1	0
Name	PR_ID_15	PR_ID_14	PR_ID_13	PR_ID_12	PR_ID_11	PR_ID_10	PR_ID_9	PR_ID_8
<default>	0	0	1	0	1	X	X	X

The <*SPI-frame-ID*> (ROM address 03H) provides information about the register width (1, 2, 3 bytes) and the availability of ‘burst mode read’ option.

In *Table 47* the register is addressable only through a read device information command.

Table 47. Address 3 <03(hex)>: SPI frame ID - read only

Bit	7	6	5	4	3	2	1	0
Name	BR	AR5	AR4	AR3	32 bits	24 bits	16 bits	8 bits
<default>	0	0	0	0	0	0	1	0

Comments:

- **BR**: Burst mode read. Not supported
- **AR5**: Address width reduction. Not supported
- **AR4**: Address width reduction. Not supported
- **AR3**: Address width reduction. Not supported
- **32 bits**: 32 bits frame width. Not supported
- **24 bits**: 24 bits frame width. Not supported
- **16 bits**: 16 bits frame width, 8 bits command and 8 bits data
- **8 bits**: 8 bits frame width. Not supported

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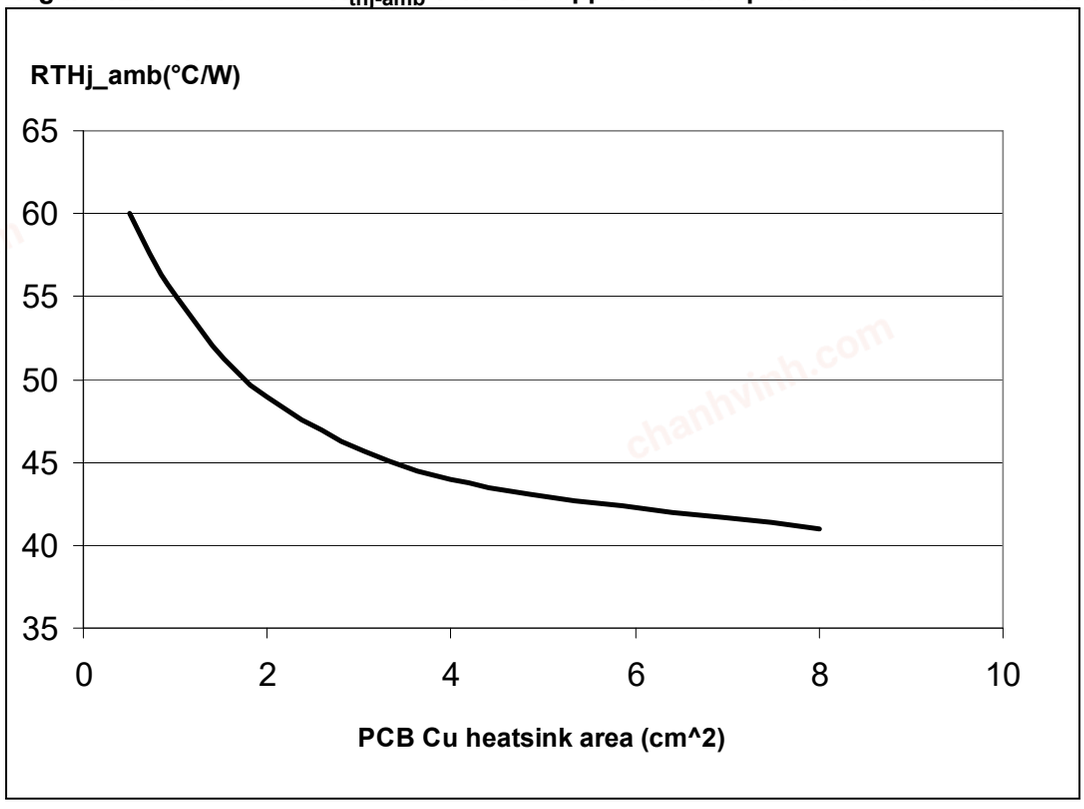
5 Package and packing information

5.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.2 Package thermal data

Figure 12. PowerSSO-36 $R_{thj\text{-}amb}$ vs. PCB copper area in open box free air condition

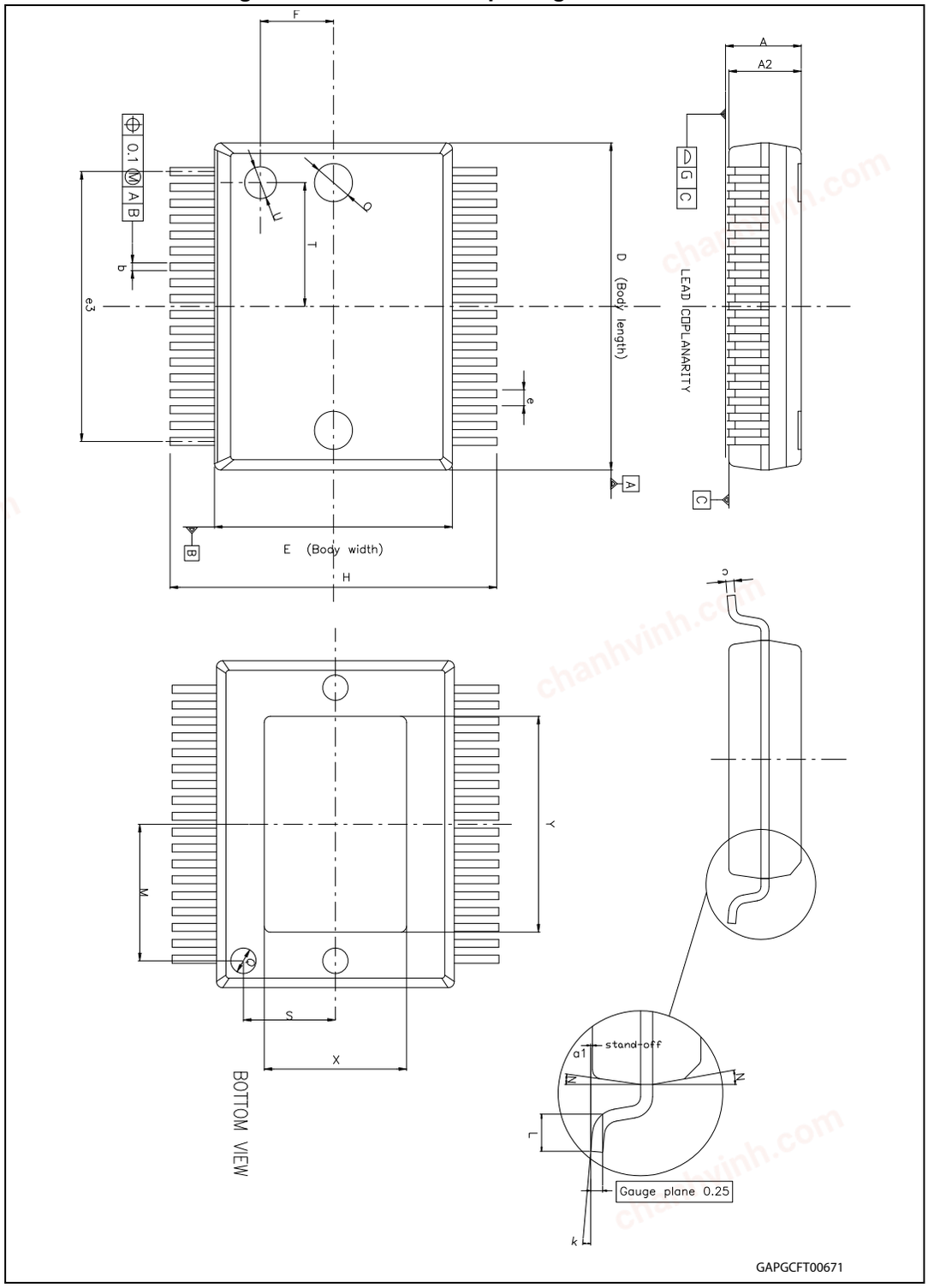


Note: In Figure 12 the Layout condition of Rth and Zth measurements (PCB: double layer, thermal vias FR4 area = 129 mm x 60 mm, PCB thickness =1.6 mm, Cu thickness =70 µm (front and back side). Copper areas: from minimum pad layout to 8 cm2).

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5.3 PowerSSO-36 package information

Figure 13. PowerSSO-36 package dimensions



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Table 48. PowerSSO-36 mechanical data

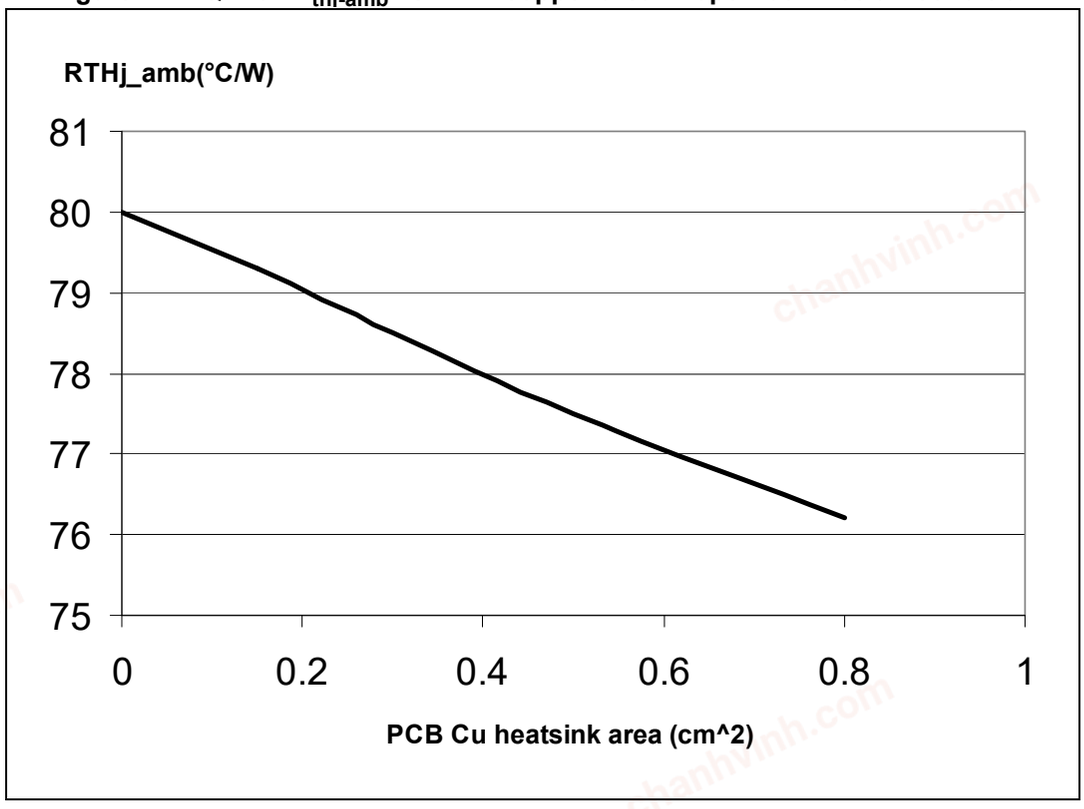
Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D(1)	10.10	-	10.50
E(1)	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	-
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1	-
X	4.1	-	4.7
Y	6.5	-	7.1

1. “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side (0.006”).

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5.4 Packages thermal data

Figure 14. LQFP32 $R_{thi\text{-}amb}$ vs. PCB copper area in open box free air condition

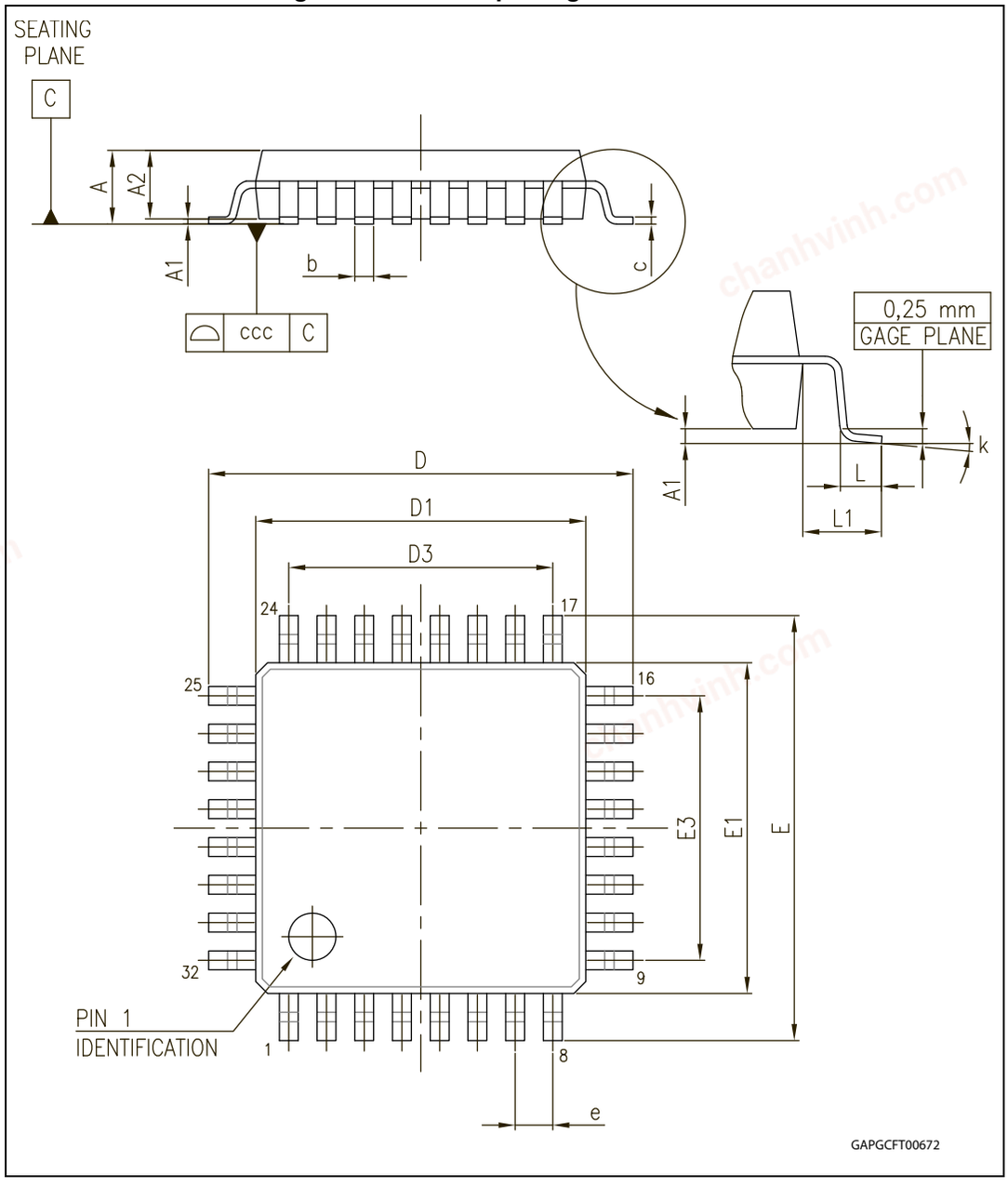


1. Layout condition of Rth and Zth measurements (PCB: double layer, thermal vias, FR4 area = 78 mm x 86 mm, PCB thickness =1.6 mm, Cu thickness =70 µm (front and back side), copper areas: from minimum pad layout to 8 cm^2).

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5.5 LQFP32 package information

Figure 15. LQFP32 package dimensions



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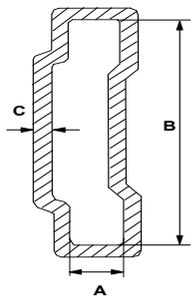
Table 49. LQFP32 mechanical data

Dim.	Millimeter		
	Min.	Typ.	Max.
A			1.60
A1	0.05		0.15
A2(1)	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
D3		5.60	
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
E3		5.60	
e		0.80	
L	0.45	0.60	0.75
L1		1.00	
K	0°	3.5°	7°
ccc			0.10

1. LQFP stands for low profile quad flat pachage.
Low profile: Body thickness (A2 = 1.40 mm)

5.6 PowerSSO-36 packing information

Figure 16. PowerSSO-36 tube shipment (no suffix)

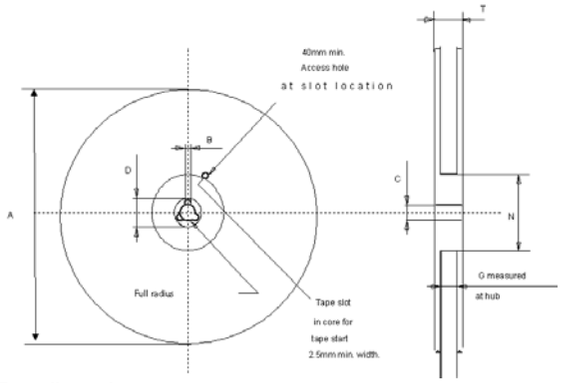


All dimensions are in mm.

Base qty	49
Bulk qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

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Figure 17. PowerSSO-36 tape and reel shipment (suffix “TR”)



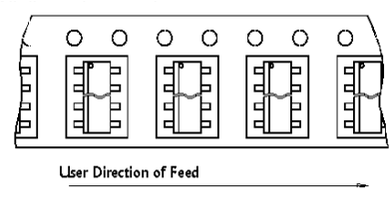
Reel dimensions

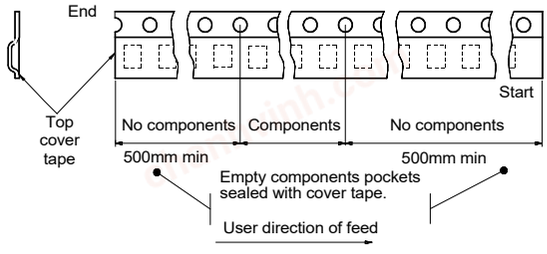
Base qty	1000
Bulk qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape hole spacing	**P0 (±0.1)**	4
Component spacing	**P**	12
Hole diameter	**D (±0.05)**	1.55
Hole diameter	**D1 (min)**	1.5
Hole position	**F (±0.1)**	11.5
Compartment depth	**K (max)**	2.85
Hole spacing	**P1 (±0.1)**	2

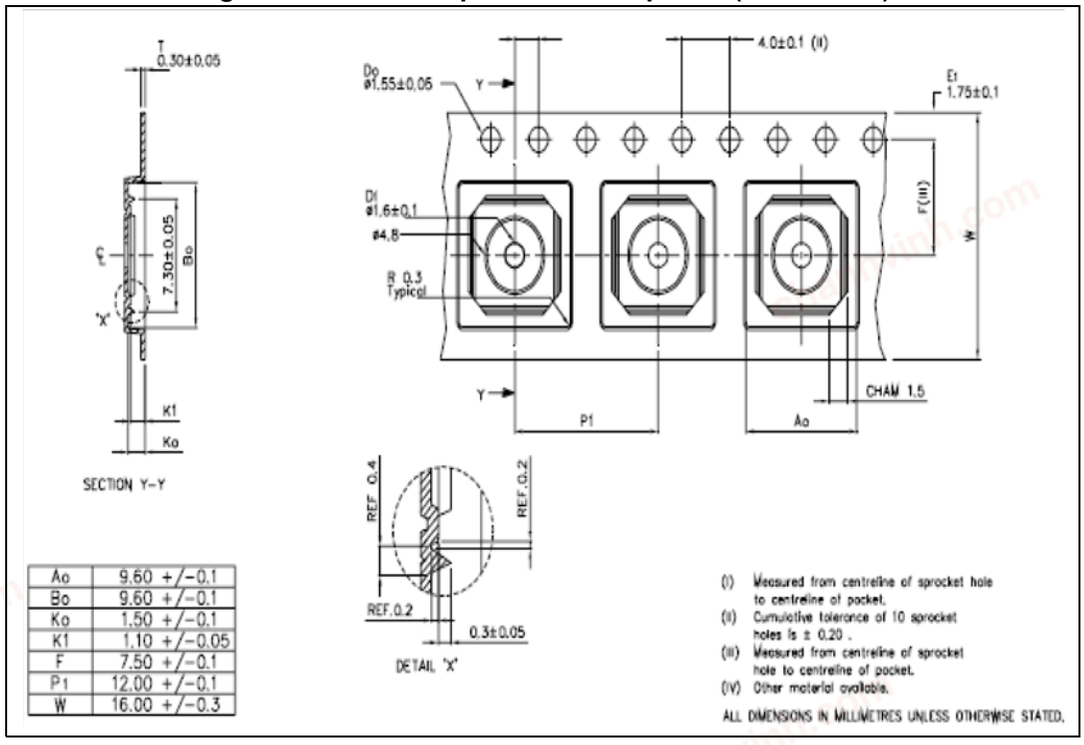




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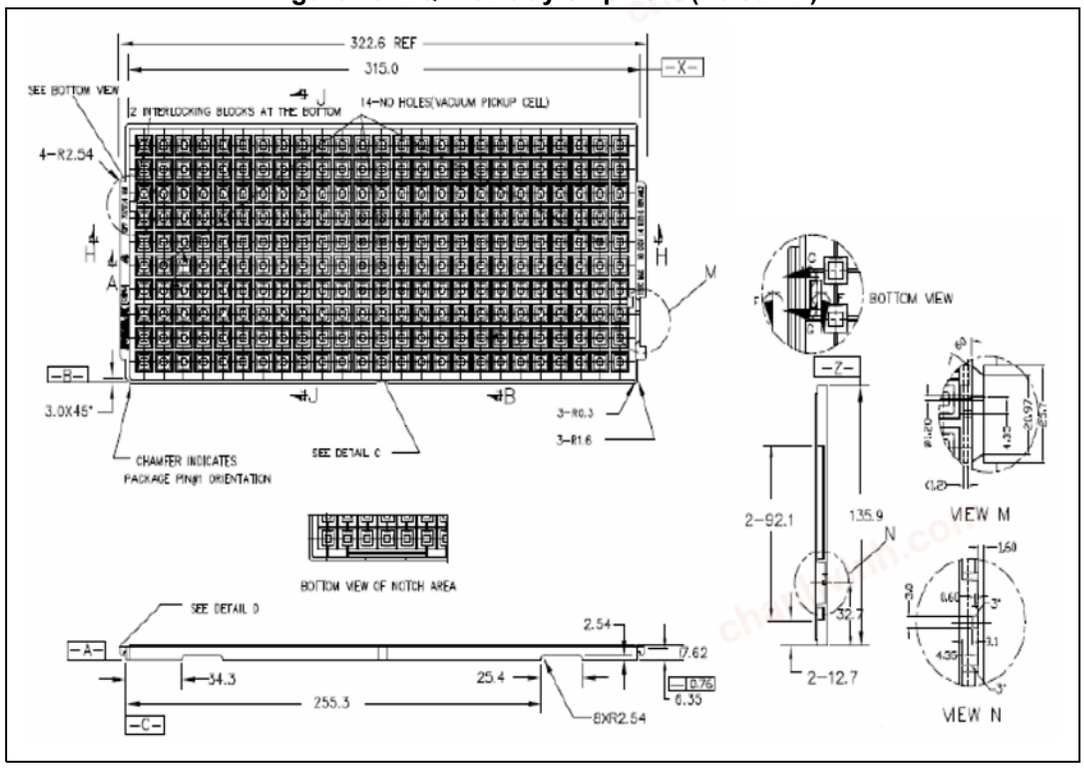
5.7 LQFP32 packing information

Figure 18. LQFP32 tape and reel shipment (suffix “TR”)



Ao	9.60 +/-0.1
Bo	9.60 +/-0.1
Ko	1.50 +/-0.1
K1	1.10 +/-0.05
F	7.50 +/-0.1
P1	12.00 +/-0.1
W	16.00 +/-0.3

Figure 19. LQFP32 tray shipment (no suffix)



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6 Revision history

Table 50. Document revision history

Date	Revision	Changes
15-Nov-2018	1	Initial release.
11-Mar-2019	2	Removed watermarks “Restricted”. Updated Table 8.
08-Apr-2019	3	Updated Table 2: Pin definitions and functions.
05-Nov-2020	4	Added package LQFP32. Updated Table 1: Device summary. Updated Figure 1: Block diagram, Update Table 2: Pin definitions and functions, Table 4: Absolute maximum ratings, Table 14: Gate drivers for external PowerMOS, Table 22: EN, CSN timing, Figure 6: SPI - transfer timing diagram, Section 3: Device description, Section 4: Functional description of the SPI.
26-Nov-2020	5	Updated Table 2: Pin definitions and functions.Table 2: Pin definitions and functionsTable 8: Packages thermal resistance Added Section 1.2: Pinout LQFP32, Section 5.2: Package thermal data, Section 5.5: LQFP32 package information, Section 5.7: LQFP32 packing information.
24-Feb-2021	6	Updated *Table 18: Current sense amplifier*.

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