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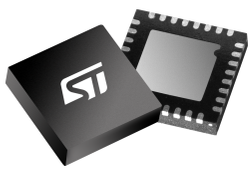
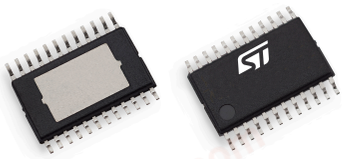
L9026

Datasheet

Configurable multi channel relay driver 2HS + 6HS/LS



VFQFPN32 exposed pad down
(5x5x1 mm)



HTSSOP24 exposed pad down
(7.8x6.4x1 mm)

Product status link
L9026

Product summary	
Order code	**L9026-B03N-TR**
Package	VFQFPN32
Packing	Tape & Reel
Order code	**L9026-YO-TR**
Package	HTSSOP24
Packing	Tape & Reel

Features

- AEC-Q100 qualified
- Six Configurable LS/HS drivers
- Two High Side drivers
- 2 parallel input pins with Input Mapping functionality
- Cranking capability down to VBATT = 3 V
- Digital supply voltage compatible with 3.3 V and 5 V microcontroller
- Reverse battery protection on VBATT and on drain pins without external components
- LED mode
- Bulb Inrush Mode (BIM) to drive lamps and electronic loads
- 2 Internal PWM Generator for microcontroller offload
- Very low quiescent current (with usage of IDLE pin)
- Limp Home mode (with usage of IDLE and IN pins)
- Green Product (RoHS compliant)
- Safety features
  - Temperature Sensor and Monitoring
  - Serial communications using address feedback, 1 parity bit, frame counter & short frame detection
- 16-bit serial peripheral interface for control and diagnosis
- Daisy Chain capability SPI, also compatible with 8-bit SPI devices
- Package options: HTSSOP24, VFQFPN32
- Full ISO26262 compliant, ASIL-B systems ready

Description

The L9026 is an eight-channel IC, with 2 fixed HS drivers and 6 configurable HS/LS drivers designed for Automotive applications (LEDs and Relays) and compatible with resistive, inductive and capacitive loads. The device offers advanced diagnostic and protection functionalities such as: short to GND, open load, overcurrent, over-temperature detections. The 8 output channels can be either driven by SPI or by 2 dedicated parallel inputs. Limp home functionality is also featured, which allows using 2 selected drivers in particular faulty conditions, such as SPI fault, micro fault or supply UV. Daisy chain compatible even with 8bit SPI is available. The device is able to guarantee operations under cranking scenario down to VBATT = 3 V and guarantees very low quiescent current under RESET condition.

A serial peripheral interface (SPI) is used for control and configuration of the loads as well as of the device; besides, status feedback of all diagnostic functions is provided. For direct control and PWM there are two input pins available: these are connected to two defined outputs by default, but additional or different output mapping can be controlled by SPI.

As reported above the device is available in two package versions HTSSOP24 and VFQFPN32. Only for the QFN package 2 additional pins are available for safety reasons. In details, the NRES pin is used to reset internal registers to their default values and the DIS pin is used to disable all channels.

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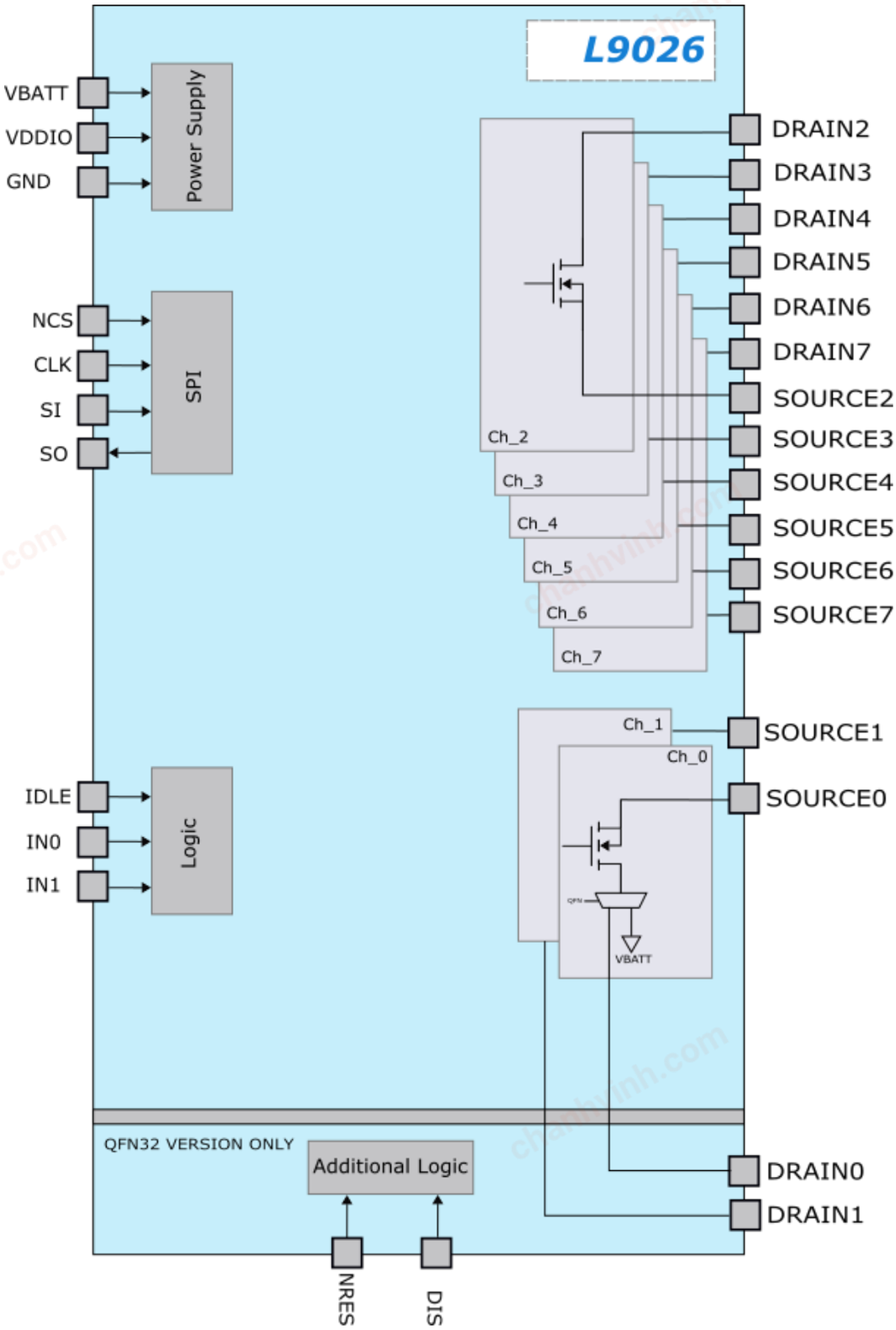
1 Block diagram

Figure 1. **Block diagram**



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2 Application circuit

Here below two general application circuits:

- Figure 2 reports L9026 with the HTSSOP24 version package
- Figure 3 shows the application of L9026 with the VFQFPN32 version package

In the list of external components, the different parts are marked following the items reported below:

1. mandatory components for L9026 functionality
2. recommended components for EMC robustness
3. recommended components for ESD trials
4. recommended System component

Note: recommended components may depend on the requirements at system levels and shall be confirmed by specific tests on the final application.

Figure 2. HTSSOP24 Application schematic

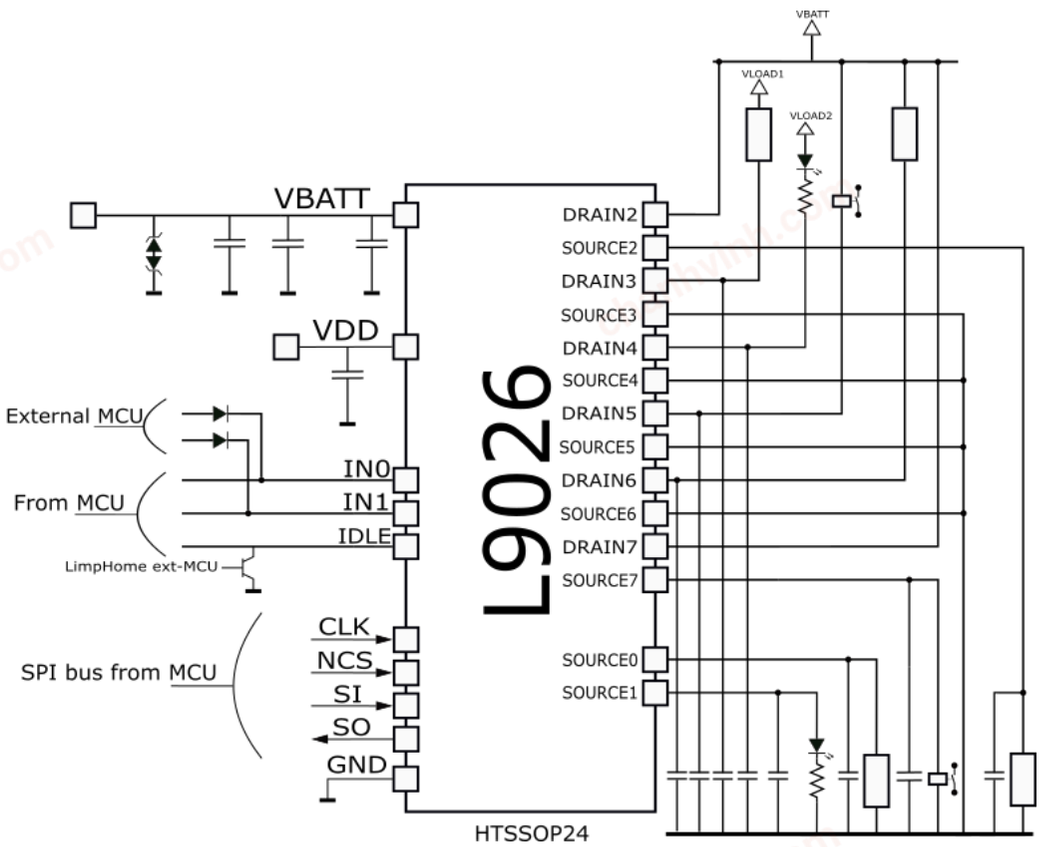

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Figure 3. **VFQFPN32 Application schematic**

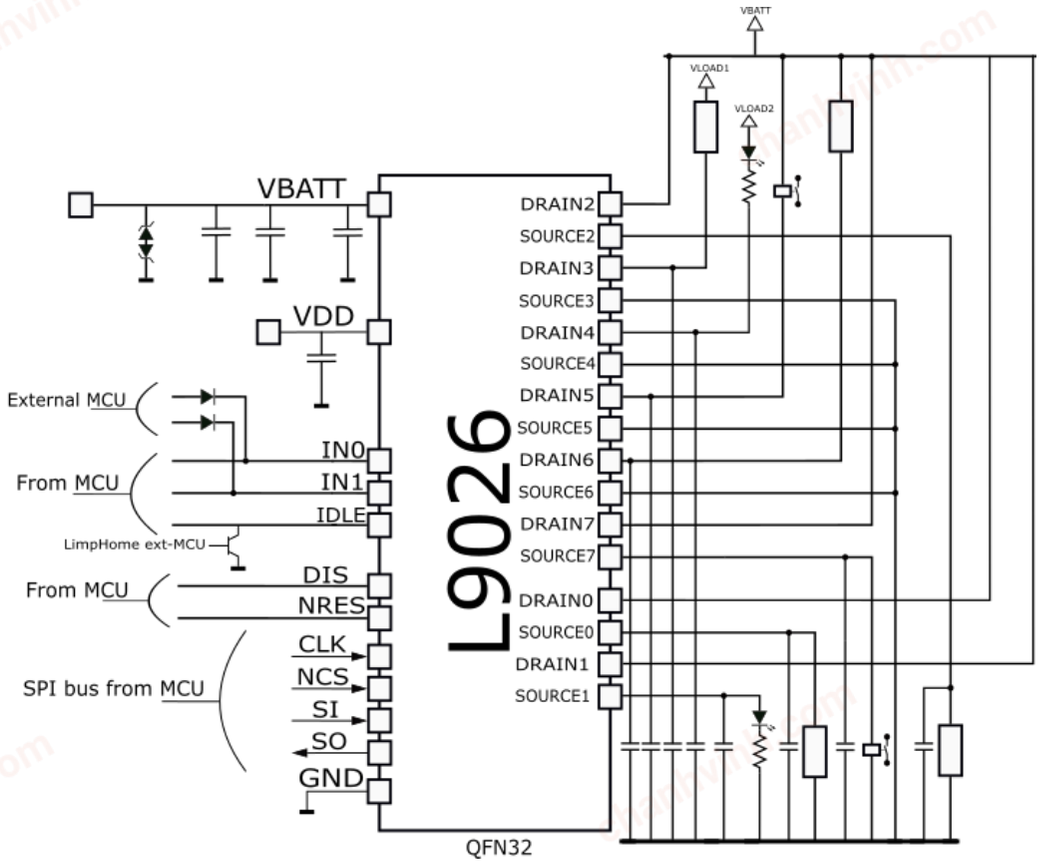

Table 1. **External components list for L9026 application circuit**

Pin	External components					Requirement	Comment
	Type	Min	Typ	Max	Unit		
VBATT	Capacitor	-	120	-	nF	(2), (3)	Tolerance ±20% 50 V
	Capacitor	-	100	-	µF	(2)	50 V, Transient and load dump protection
	TVS	- 15	-	38	V	(4)	Transient voltage suppressor
	Capacitor	-	10	-	µF	(2), (3)	Tolerance ±20% 50 V, Transient and load dump protection
VDDIO	Capacitor	-	100	-	nF	(2)	Tolerance ±10% 50 V
DRAIN2 DRAIN7	Capacitor	-	-	12	nF	(3)	Maximum total capacitance value at output load (channel configured as low side)
DRAIN0 DRAIN7		47	-	-		(4)	Minimum capacitance value at load supply (channel configured as high side, DRAIN0 and DRAIN1 if available)
SOURCE0 SOURCE7	Capacitor	-	-	12	nF	(3)	Maximum total capacitance value as output load (channel configured as high side)

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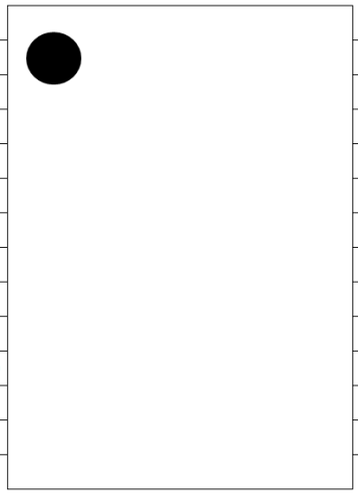
3 Pins description

Figure 4. **HTSSOP-24 pinout diagram**



positive	negative	pin name			pin name	negative	positive
42V	-0.3 V	**VBATT**	1	24	**SOURCE1**	-0.3 V	VOUT_D + 0.3V
VOUT_D + 0.3V	-0.3 V	**SOURCE0**	2	23	**SOURCE2**	-0.3 V	VOUT_D + 0.3V
42V	-0.3 V	**DRAIN7**	3	22	**DRAIN2**	-0.3 V	42V
VOUT_D + 0.3V	-0.3 V	**SOURCE7**	4	21	**SOURCE3**	-0.3 V	VOUT_D + 0.3V
42V	-0.3 V	**DRAIN6**	5	20	**DRAIN3**	-0.3 V	42V
VOUT_D + 0.3V	-0.3 V	**SOURCE6**	6	19	**SOURCE4**	-0.3 V	VOUT_D + 0.3V
42V	-0.3 V	**DRAIN5**	7	18	**DRAIN4**	-0.3 V	42V
VOUT_D + 0.3V	-0.3 V	**SOURCE5**	8	17	**SI**	-0.3 V	20V
VDDIO + 0.3	-0.3 V	**IN1**	9	16	**NCS**	-0.3 V	20V
20V	-0.3 V	**IN0**	10	15	**CLK**	-0.3 V	20V
0.3 V	-0.3 V	**GND**	11	14	**SO**	-0.3 V	VDDIO + 0.3
20V	-0.3 V	**IDLE**	12	13	**VDDIO**	-0.3 V	20V

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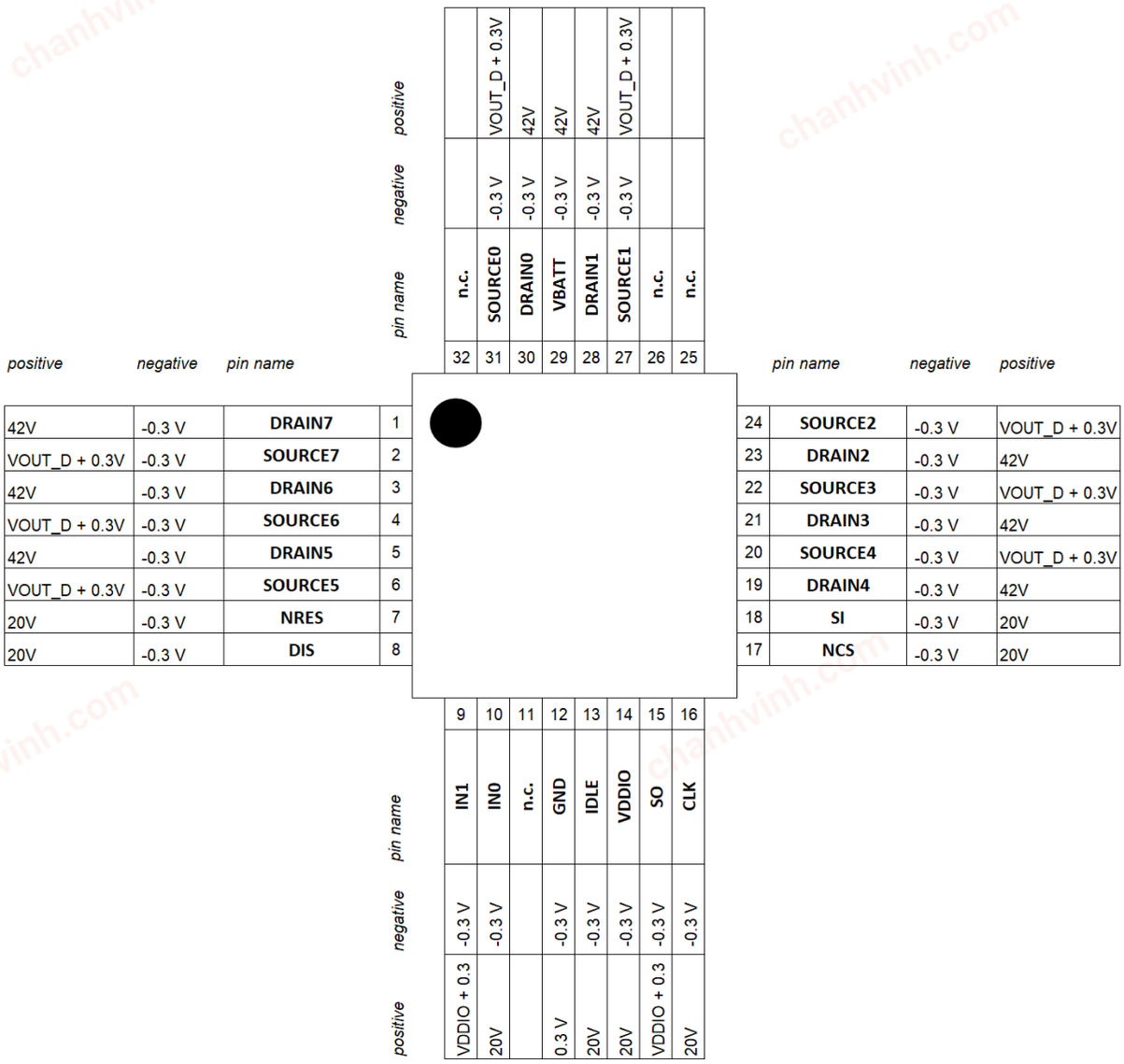
Figure 5. **VFQFPN32 pinout diagram**



pin	pin name	negative	positive
1	DRAIN7	-0.3 V	42V
2	SOURCE7	-0.3 V	VOUT_D + 0.3V
3	DRAIN6	-0.3 V	42V
4	SOURCE6	-0.3 V	VOUT_D + 0.3V
5	DRAIN5	-0.3 V	42V
6	SOURCE5	-0.3 V	VOUT_D + 0.3V
7	NRES	-0.3 V	20V
8	DIS	-0.3 V	20V
9	IN1	-0.3 V	VDDIO + 0.3
10	IN0	-0.3 V	20V
11	n.c.		
12	GND	-0.3 V	0.3 V
13	IDLE	-0.3 V	20V
14	VDDIO	-0.3 V	20V
15	SO	-0.3 V	VDDIO + 0.3
16	CLK	-0.3 V	20V
17	NCS	-0.3 V	20V
18	SI	-0.3 V	20V
19	DRAIN4	-0.3 V	42V
20	SOURCE4	-0.3 V	VOUT_D + 0.3V
21	DRAIN3	-0.3 V	42V
22	SOURCE3	-0.3 V	VOUT_D + 0.3V
23	DRAIN2	-0.3 V	42V
24	SOURCE2	-0.3 V	VOUT_D + 0.3V
25	n.c.		
26	n.c.		
27	SOURCE1	-0.3 V	VOUT_D + 0.3V
28	DRAIN1	-0.3 V	42V
29	VBATT	-0.3 V	42V
30	DRAIN0	-0.3 V	42V
31	SOURCE0	-0.3 V	VOUT_D + 0.3V
32	n.c.		

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Table 2. **HTSSOP-24 pins list**

Pin number	Symbol	Function
1	VBATT	Battery voltage
2	SOURCE0	HS Source 0
3	DRAIN7	LS/HS Drain 7
4	SOURCE7	LS/HS Source 7
5	DRAIN6	LS/HS Drain 6
6	SOURCE6	LS/HS Source 6
7	DRAIN5	LS/HS Drain 5
8	SOURCE5	LS/HS Source 5
9	IN1	Parallel command input 1
10	IN0	Parallel command input 0
11	GND	Ground pin
12	IDLE	Idle function
13	VDDIO	IO supply
14	SO	SPI output stream
15	CLK	SPI clock
16	NCS	SPI Chip Select
17	SI	SPI input stream
18	DRAIN4	LS/HS Drain 4
19	SOURCE4	LS/HS Source 4
20	DRAIN3	LS/HS Drain 3
21	SOURCE3	LS/HS Source 3
22	DRAIN2	LS/HS Drain 2
23	SOURCE2	LS/HS Source 2
24	SOURCE1	HS Source 1

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Table 3. **VFQFPN32 pins list**

Pin number QFN32	Symbol	Function
1	DRAIN7	LS/HS Drain 7
2	SOURCE7	LS/HS Source 7
3	DRAIN6	LS/HS Drain 6
4	SOURCE6	LS/HS Source 6
5	DRAIN5	LS/HS Drain 5
6	SOURCE5	LS/HS Source 5
7	NRES	NRES function – available only in VFQFPN32 package
8	DIS	Channel disable – available only in VFQFPN32 package
9	IN1	Parallel command input 1
10	IN0	Parallel command input 0
11	N.C.	-
12	GND	Ground pin
13	IDLE	Idle function
14	VDDIO	IO supply
15	SO	SPI output stream
16	CLK	SPI clock
17	NCS	SPI Chip Select
18	SI	SPI input stream
19	DRAIN4	LS/HS Drain 4
20	SOURCE4	LS/HS Source 4
21	DRAIN3	LS/HS Drain 3
22	SOURCE3	LS/HS Source 3
23	DRAIN2	LS/HS Drain 2
24	SOURCE2	LS/HS Source 2
25	N.C.	-
26	N.C.	-
27	SOURCE1	HS Source 1
28	DRAIN1	HS Drain 1
29	VBATT	Battery voltage
30	DRAIN0	HS Drain 0
31	SOURCE0	HS Source 0
32	N.C.	-

Note:
- *In case of VFQFPN32 package, CFG_0.DIS_EN and bit CFG_0.NRES_N needs to set through SPI.*
- *In case of HTSSOP24 package, NRES and DIS pins are not available; CFG_0.DIS_EN and bit CFG_0.NRES_N must be considered as reserved, kept at '0'.*
- *For both package options the exposed pad must be left floating to guarantee the reverse battery protection feature.*

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4 Product characteristics

4.1 Absolute maximum ratings

This part may be irreparably damaged if taken outside the specified Absolute Maximum Ratings. Operation above the Absolute Maximum Ratings may also cause a decrease in reliability.

The operating junction temperature range is -40 °C to +150 °C. The maximum junction temperature must not be exceeded. All voltages are referred to analog ground pin GND.

Table 4. Absolute maximum rating capability

Symbol	Type	Test condition	Min	Typ	Max	Unit	Pin type
VBATT	Global	ton = 400 ms; ton/toff = 10 %; limited to 100 pulses	-0.3	-	42	V	S
VDDIO	Local	-	-0.3	-	20	V	S
$-VBATT_{(REV)}$	Global	Reverse polarity voltageT = 25 °C, t < 2min, RL=70 Ω on all channels, with exposed pad floating	-	-	16	V	S
V_{OUT_S}	Global	Power transistor source voltage	-16	-	Min[VOUT_D + 0.3, 42]	V	O
V_{OUT_D}	Global	Power transistor drain voltage (VOUT_S ≥ 0 V)	VOUT_S - 0.3	-	42	V	O
V_{IDLE}	Local	-	-0.3	-	20	V	I
V_{IN0}	Local	-	-0.3	-	20	V	I
V_{IN1}	Local	-	-0.3	-	Min[VDDIO + 0.3, 20]	V	I
V_{NCS}	Local	-	-0.3	-	20	V	I
V_{CLK}	Local	-	-0.3	-	20	V	I
V_{SI}	Local	-	-0.3	-	20	V	I
V_{SO}	Local	-	-0.3	-	Min[VDDIO + 0.3, 20]	V	O
V_{IN}	Local	Applies to : V_{NRES} V_{DIS}	-0.3	-	20	V	I

4.2 Latchup trials

Latch-up tests performed according to JEDEC 78 class 2 Level A

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4.3 Temperature range

Table 5. **Temperature range**

Symbol	Description	Test condition	Min	Typ	Max	Unit
Ta	Operating ambient temperature	-	-40	-	125	°C
Tj	Junction temperature	-	-40	-	150	°C
Tstg	Storage temperature	-	-55	-	150	°C
RTHj-a	Thermal resistance junction to ambient	- Package: HTSSOP - 2s2p (4L) board(1) - Natural convection	-	38	-	°C/W
RTHj-c	Thermalr esistance junction to case		-	1	-	
RTHj-b	Thermal resistance junction to board		-	20	-	
RTHj-a	Thermal resistance junction to ambient	- Package: VFQFPN - 2s2p (4L) board(1) - Natural convection	-	36	-	°C/W
RTHj-c	Thermal resistance junction to case		-	4	-	
RTHj-b	Thermal resistance junction to board		-	18	-	

1. *JESD51-7*

All parameters are guaranteed, and tested, in the temperature range Tj -40 ÷ 150 °C (unless otherwise specified).

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5 Input / Output

5.1 Parallel inputs (IN0, IN1)

Device has two input pins available. Each input pin is connected by default to one channel (IN0 to channel 2, IN1 to channel 3). Input Mapping Registers MAP_IN0 and MAP_IN1 can be programmed to connect different channels to each input pin. The signals driving the channels are an OR combination between PWM_SPI register status, PWM Generators (according to PWM Generator Output Mapping status), IN0 and IN1 (according to Input Mapping registers status). See Section 11 SPI for further details.

The logic level of the input pins can be monitored via the status register STA_0. The Input Status Monitor is operative also when device is in Limp Home mode. If one of the Input pins is set to “high” and the IDLE pin is set to “low”, the device switches into Limp Home mode and activates the channel mapped by default to the input pins.

5.2 Idle pin (IDLE)

The IDLE pin is used to bring the device into Sleep mode operation when is set to “low” together with IN0, IN1 input pins being at “low” state. When IDLE pin is set to “low” while one of the input pins is set to “high” the device enters Limp Home mode.

To ensure a proper mode transition, IDLE pin must be set for at least $t_{IDLEFLT_max}$ (transition from “high” to “low” or from “low” to “high”).

Setting the IDLE pin to “low”, with both IN0 and IN1 also at “low” value, has the following consequences:

- Device goes in SLEEP MODE
- All registers in the SPI are reset to default values
- VDDIO and VBATT Under voltage detection circuits are disabled to decrease current consumption
- No SPI communication is allowed: SO pin remains in high impedance state also when NCS pin is active.

5.3 Reset pin (NRES, only in VFQFPN32 package option)

The NRES pin, available only for VFQFPN32 version, is the reset input for the device. The function uses the inverse logic, if the NRES pin is low, the device is held in an internal reset state, all outputs channels are disabled, and all registers are reset to their default values. An internal pull down will hold the NRES pin asserted in case of pin open. As default, the state of NRES pin is masked by the logic. The user must send a specific SPI frame to force the logic to take into account the state of NRES pin.

5.4 Enable (DIS, only in VFQFPN32 package option)

The DIS pin, available only for VFQFPN32 version, is used to enable / disable the output stages. When DIS pin is high, all channels are disabled if the pin is not masked. An internal pull up will hold the DIS pin asserted in case of pin open.

When DIS pin is set low, all channels are enabled based on their configuration settings. As default, the DIS pin is masked by the logic. The user needs to send a specific SPI frame to force the logic to take into account the state of DIS pin. The status of DIS pin can be monitored reading the STA_0 register.

The DIS pin can be connected to a general purpose output pin of the microcontroller or to an alternative safety circuit.

5.5 SPI communications (NCS, CLK, SI & SO)

The NCS, CLK, SI & SO pins provide serial communications between the device and the microcontroller. See Section 11 SPI for details on SPI features, device register functions and electrical characteristics.

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5.6 Input / output electrical specifications

3 V ≤ VDDIO ≤ 5.5 V; 6 V ≤ VBATT ≤ 18 V; -40 °C ≤ Tj ≤ 150 °C unless otherwise specified. All voltages are referred to GND pin.

Table 6. Digital input/output electrical performance

Parameter	Description	Test condition	Min	Typ	Max	Unit	Pin
$V_{IDLE(L)}$	L-input level	-	-	-	0.8	V	IDLE
$V_{IDLE(H)}$	H-input level	-	2	-		V	IDLE
R_{IDLE}	Input pull-down resistor at IDLE pin	VDDIO = 5 V; V_{DIS} = 2 V	60		125	kΩ	IDLE
$V_{IN(L)}$	L-input level	-	-	-	0.8	V	IN0-IN1
$V_{IN(H)}$	H-input level	-	2			V	IN0-IN1
R_{IN}	Input pull-down resistor at IN0 and IN1 pin	VDDIO = 5 V; V_{DIS} = 2 V	60	-	125	kΩ	IN0-IN1
$V_{NRES(L)}$	L-input level	-	-	-	0.8	V	NRES
$V_{NRES(H)}$	H-input level	-	2	-		V	NRES
R_{NRES}	Input pull-down resistor at NRES pin	VDDIO = 5 V; V_{DIS} = 2 V	70	-	140	kΩ	NRES
$V_{DIS(L)}$	L-input level	-	-	-	0.8	V	DIS
$V_{DIS(H)}$	H-input level	-	2	-		V	DIS
R_{DIS}	Input pull-up resistor at DIS pin	VDDIO = 5 V; V_{DIS} = 0.8 V	40	-	95	kΩ	DIS

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6 Power supply

6.1 Overview

The L9026 is fed by two supply voltages:

- VBATT (general supply for analog and digital part)
- VDDIO (supply for digital and output buffers)

The supply lines are monitored against under voltage: in case under voltage condition is detected the IC reacts as per the following:

- An under voltage on VBATT supply voltage prevents the activation of the power stages.
- An under voltage on VDDIO supply prevents any SPI communication and SPI read/write registers are reset to default values.

The combination of the different under voltage conditions are reported in Table 7.

Table 7. Supply ranges

	VDDIO ≤ $VDDIO_{(UV)}$	VDDIO > $VDDIO_{(UV)}$
VBATT ≤ VBATT_uv	channels cannot be controlled	channels cannot be controlled
	SPI registers reset	SPI registers available
	SPI communication not available	SPI communication possible
	Limp Home mode not available	Limp Home mode available(channels are OFF)
VBATT > VBATT_uv	channels cannot be controlled by SPI (INn functionality still available)	channels can be switched ON and OFF
	SPI registers reset	SPI registers available
	SPI communication not available	SPI communication possible

6.2 Battery supply (VBATT)

This pin is the general supply for analog and digital part unless an undervoltage condition is detected on VBATT. In this case, provided VDDIO is still in range, the logic is supplied by the VDDIO itself. The Table 8 summarizes the functional ranges dependent on battery supply voltage.

Table 8. VBATT electrical performance

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
VBATT	Supply Voltage Range for normal operations	3 V ≤ VDD ≤ 5.5 V	6	-	18	V
VBATT	Upper Supply Voltage Range for extended operations	3 V ≤ VDD ≤ 5.5 V	18	-	28	V
VBATT Low Voltage	Low Voltage Range Cranking(1)	3 V ≤ VDD ≤ 5.5 V	3	-	6	V

1. *Possible degradation of electrical parameters linked to battery line. Full functional operation will resume without operator intervention when battery voltage returns to Normal Operating Voltage Range.*

The device operates on 12 V system. Transient operation for these systems can reach 40 V maximum. Particular care has to be taken in PCB manufacturing to keep thermal dissipation to a reasonable level.

- For VBATT < $VBATT_{(UV)}$ the device is in a safety state (internal circuitries are on but all the outputs are off).
- For VBATT up to 40 V all the functions are granted with increased power dissipation and no reset is asserted during transient.

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6.3 Operating modes

The L9026 has 4 operative modes as per below:

- Sleep mode
- Idle mode
- Active mode
- Limp Home mode

The transition between operation modes is determined according to the following levels and states:

- logic level at IDLE pin
- logic level at INn pins
- PWM_SPI.OUTn bits state
- CFG_1.ACT bit state
- MAP_PWM.OUTn and PWM_SEL.OUTn bits state

The Figure 6 represents the possible transitions in the state diagram. The description is valid if the digital POR signal is de-asserted (indicated as POR_N in the register map). In case of POR = 0 transitions from Active to idle and from Limp Home to Sleep do not guarantee switch off behavior with functional timings. A POR condition is traced in a clear on read register in the STA_1.POR bit. The behavior of the device as well as some parameters may change depending on the operating mode of the device. Furthermore, due to the under voltage detection circuitry which monitors VBATT and VDDIO supply voltages, some changes within the same operation mode can be seen accordingly.

In case of VBATT < VBATT(UV_L) and IDLE = IN0 = IN1 = high device doesn't go from IDLE state to ACTIVE state.

Starting from Active state in the condition IDLE = ’0’ and INn = ’0’ (that corresponds to the transition Active to Sleep) to guarantee drivers turn OFF it is necessary also a SW reset.

There are different options to observe the operation mode of the device:

- status of output channels
- status of SPI registers
- current consumption at VBATT pin (IVBATT)

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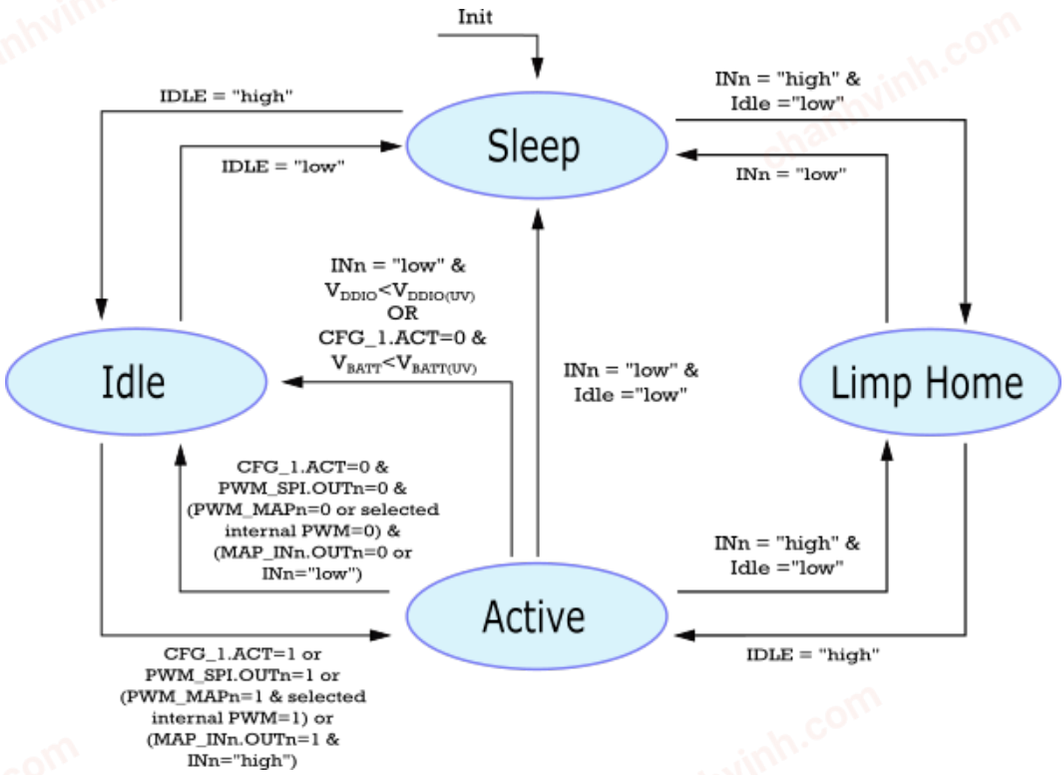
Figure 6. **State ddiagram**



The default operation mode to switch ON the loads is Active mode. If the device is not in Active mode and a request to switch ON one or more outputs occurs (via SPI or via Input pins), it will switch into Active or Limp Home mode, according to IDLE pin status. Due to the time needed for such transitions, output turn-on time tON will be extended due to the mode transition latency.

Table 9 shows the correlation between device operation modes, VBATT and VDDIO supply voltages, and state of device functions (channels operability, SPI communication and SPI registers).

Table 9. **Functions availability in different supply conditions**

Operating mode	Function	Under voltage condition on VBATT		VBATT not in under voltage	
		VDDIO ≤ $VDDIO_{UV}$	VDDIO > $VDDIO_{UV}$	VDDIO ≤ $VDDIO_{UV}$	VDDIO > $VDDIO_{UV}$
Sleep	Channels	not available	not available	not available	not available
	SPI comm.	not available	not available	not available	not available
	SPI registers	reset	reset	reset	reset
Idle	Channels	not available	not available	not available	not available
	SPI comm.	not available	available	not available	available
	SPI registers	reset	available	reset	available
Active	Channels	not available	not available	available (IN pins only)	available
	SPI comm.	not available	available	not available	available
	SPI registers	reset	available	reset	available
Limp Home	Channels	not available	not available	available (IN pins only)	available (IN pins only)
	SPI comm.	not available	available (read-only)	not available	available (read-only)
	SPI registers	reset	available (read-only)	reset	available (read-only)

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6.4 Analog & Digital supply (VBATT)

The VBATT is used to supply the internal logic, analog and digital, in normal condition (no under voltage on VBATT) and the output loads.

In case the voltage drops below $VBATT_{(UV_L)}$ the under voltage mechanism is triggered and the bit STA_1.VS_UV is reported via SPI. Once the faulty condition disappears (VBATT > $VBATT_{(UV_H)}$), the bit remains latched until its status is acknowledged by the microcontroller via SPI.

Under voltage condition on VBATT influences the status of the channels as described in Table 7.

6.5 I/O Supply (VDDIO)

VDDIO is the supply for all pins that interface with the external microcontroller and also works as feed for the internal logic if VBATT is in under voltage condition.

In case the voltage drops below $VDDIO_{(UV)}$ the under voltage mechanism is triggered and the bit STA_1. VDD_UV is reported via SPI. This is valid if digital POR_N is ‘1’. For all conditions that generate a POR_N=0, a dedicated clear on read STA_1.POR_N bit is set. Once the faulty condition disappears, the bit remains latched until its status is acknowledged by the microcontroller via SPI.

6.6 Power up

The IC performs Power-up procedure when one of the supply voltages (VBATT or VDDIO) is applied to the device and the INn or IDLE pins are set to “high”.

6.7 Sleep mode

When device is in Sleep mode, all outputs are OFF and the SPI registers are reset, independently of the supply voltages. The current consumption is reduced to the IVDDIO(SLEEP) and IVBATT(SLEEP).

6.8 Idle mode

In Idle mode, the current consumption of the device reaches the parameters IVDDIO(IDLE) and IVBATT(IDLE). The internal voltage regulator is still working. ON diagnosis functions are not available. The output channels are switched OFF, independently of the supply voltages. When VDDIO is available, the SPI registers are working and SPI communication is possible. In Idle mode the DIAG_OVC_OVT bits are not cleared.

6.9 Active mode

Active mode is the normal operation mode when no Limp Home condition is set and it is necessary to drive some or all loads. Voltage levels of VDDIO and VBATT influence the behavior as described in detail in Section 6.1 Overview. Device current consumption is specified with IVDDIO(ACTIVE) and IVBATT(ACTIVE).

In case CFG_1.ACT is set to “1”, the device enters in Active mode and remains in this state independently on the status of input pins, of internal PWM generators and PWM_SPI.OUTn bits.

Otherwise, in case the bit CFG_1.ACT is not set, in order to move the device in Active mode all conditions below are needed:

- the IDLE pin set to “high”
- the outputs configured as driven either by external pins (through MAPIN0, MAPIN1 registers) or by SPI (at least one PWM_SPI.OUTn bit is set to “1”) or by the internal PWM generators (through MAP_PWM)
- at least one channel enabled

In this scenario, the device returns to Idle mode as soon as IDLE pin set to “low”, all inputs pins are set to “low”, all PWM_SPI.OUTn bits are set to “0” and all the internal pwm generators are OFF.

Being the IDLE pin asserted high, an under voltage condition on VDDIO supply brings the device into Idle mode once all INn input pins are set to “low”, on top of the setting of the bit CFG_1.ACT.

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6.10 Limp Home mode

Device enters Limp Home mode when IDLE pin is “low” and one of the input pins is set to “high”, switching ON the channel connected to it. SPI communication is possible but in read-only mode (SPI registers can be read but cannot be written).

More in detail, Limp Home mode has the following effects:

- IN0 is mapped as channel 2 input command, IN1is mapped as channel 3 input command
- MODE bits are set to “01B” (Limp Home mode)
- Overload and Over temperature diagnostics on channel 2 and 3 are available and the related DIAG_OVC_OVT bits can be read.

Entering Limp Home mode from sleep means that all other registers are set to their default value and cannot be programmed as long as the device is in Limp Home mode (SPI in in read only mode) so far a special feature for Channel 2 and 3 is implemented and channels are able of auto-configuring as LS or HS depending on the configuration of the external load.

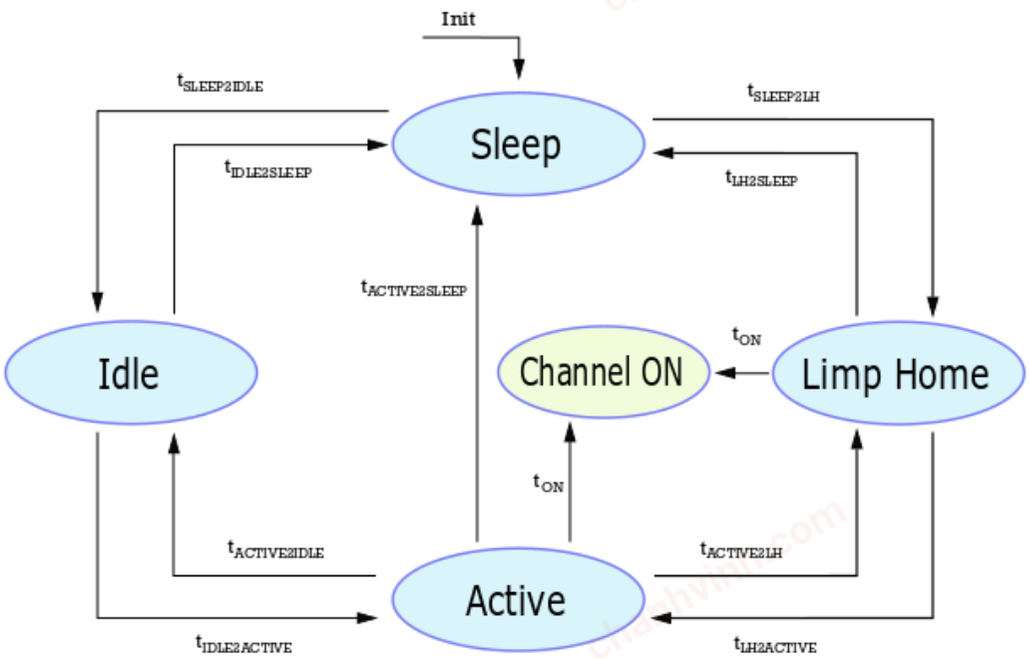
Open in ON diagnosis is not performed in Limp Home mode. This is true also if Limp Home mode has been entered from Active mode and DIAG_OPL_ON_EN.OUTn bits are set to '1'. In this case, the diagnostic cycles will be performed only when back in ACTIVE mode.

See Table 9 for a detailed overview of supply voltage conditions required to switch ON channels 2 and 3 during Limp Home. All other channels are kept OFF.

6.11 Power supply transition

The channel turn-ON time is defined by parameter *t*ON when device is in Active mode or in Limp Home mode. In all other cases, it is necessary to add the transition time required to reach one of the two above mentioned Power Supply modes, as reported in Figure 7.

Figure 7. Transition times block diagram



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6.12 Reset

One of the following 4 conditions reset the SPI read/write registers to the default value:

- VDDIO not present or below the undervoltage threshold VDDIO(UV)
- IDLE pin is set to “low” with both INn “low"
- A software reset (CFG_1.RST set to “1”) is commanded
- NRES pin is asserted (only available in VFQFPN32 package option and configured to sense the pin status)

When the SPI registers are reset, all channels (except 2,3) are switched OFF and the Input Mapping configuration is also reset. This means channels 2, 3 are still commanded by IN0, IN1 respectively.

For functional safety register DIAG_OVC_OVT and STA_1. VDDIO_UV, STA_1.VBATT_UV bits are not cleared by a reset command.

One of the following conditions resets the whole internal logic;

- General internal supply failure (internal supply 3.3 V in UV or bandgap reference not correct)
- VDDIO < VDDIO(UV) and IN1 = 0 and IN0 = 0

6.13 Power supply electrical specifications

3V ≤ VDDIO ≤ 5.5 V; 6 V ≤ VBATT ≤ 18 V; -40 °C ≤ Tj ≤ 150 °C unless otherwise specified. All voltages are referred to GND pin.

Table 10. Power supply electrical parameters

Parameter	Description	Test condition	Min	Typ	Max	Unit
VBATT pin						
$VBATT_{(UV_L)}$	Analog supply undervoltage low threshold	-	2.65	2.8	2.95	V
$VBATT_{(UV_H)}$	Analog supply undervoltage high threshold	-	2.7	2.85	3	V
$I_{VBATT(SLEEP)}$	Analog supply current consumption in Sleep mode	V_{IDLE} = 0: V_{INn} = 0; VDDIO = 5 V; TJ ≤ 85 °C	-	-	12	µA
$I_{VBATT(SLEEP)}$	Analog supply current consumption in Sleep mode	V_{IDLE} = 0; V_{INn} = 0; VDDIO = 5 V; TJ ≤ 175 °C	-	-	14	µA
$I_{VBATT(IDLE)}$	Analog supply current consumption in Idle mode	V_{IDLE} = 5 V; V_{INn} = 0; VDDIO = 5 V; f_{SCLK} = 0 MHz; CFG_1.ACT = 0_B; PWM_SPI.OUTn = 0_B; DIAG_OFF_EN.OUTn = 0_B	-	-	20	mA
$I_{VBATT(IDLE_COR)}$	Analog supply current consumption in Idle Mode with VBATT lower than VDDIO (device supplied by VDDIO)	V_{IDLE} = 5 V; V_{INn} = 0; VDDIO = 5 V; f_{SCLK} = 0 MHz; CFG_1.ACT = 0_B; PWM_SPI.OUTn = 0_B; DIAG_OFF_EN.OUTn = 0_B; VBATT = VDDIO - 1 V	–0.1	-	0.1	mA
$I_{VBATT(ACTIVE)}$	Analog supply current consumption in Active mode - channels OFF	V_{IDLE} = 5 V; V_{INn} = 0; VDDIO = 5 V; f_{SCLK} = 0 MHz; CFG_1.ACT = 1_B; PWM_SPI.OUTn = 0_B; DIAG_OFF_EN.OUTn = 0_B	-	14	20	mA
$I_{VBATT(ACTIVE_COR)}$	Analog supply current consumption in Active mode - channels OFF with VBATT lower than VDDIO (device supplied by VDDIO)	V_{IDLE} = 5 V; V_{INn} = 0; VDDIO = 5 V; f_{SCLK} = 0 MHz; CFG_1.ACT = 1_B; PWM_SPI.OUTn = 0_B; DIAG_OFF_EN.OUTn = 0_B; VBATT = VDDIO - 1 V	–0.1	-	0.1	mA

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Parameter	Description	Test condition	Min	Typ	Max	Unit
$t_{VBATTUVFLT}$	VBATT undervoltage filter	Covered bySCAN	9	14	19	µs
VDDIO pin						
$VDDIO_{(OP)}$	Logic Supply Operating range voltage	f_{SCLK} = 8 MHz	3	-	5.5	V
$VDDIO_{(UV_RECOVERY)}$	Analog supply threshold for recovery after battery undervoltage	MISO from “low” to high impedance	2.7	2.85	3	V
$VDDIO_{(UV)}$	Undervoltage shutdown	MISO from “low” to high impedance	2.65	2.8	2.95	V
$I_{VDDIO(SLEEP)}$	Logic supply current in Sleepmode	V_{IDLE} = 0; V_{INn} = 0; VDDIO = 5 VTJ ≤ 85 °C	-	-	1	µA
$I_{VDDIO(SLEEP)}$	Logic supply current in Sleep mode	V_{IDLE} = 0V; V_{INn} = 0 V; VDDIO = 5 VTJ ≤ 150 °C	-	-	2	µA
$I_{VDDIO(IDLE)}$	Logic supply current in Idle Mode	V_{IDLE} = 5 V; V_{INn} = 0 V; VDDIO = 5 V; f_{SCLK} = 0 MHz; CFG_1.ACT = 0_B; PWM_SPI.OUTn = 0_B; DIAG_OFF_EN.OUTn = 0_B	-	-	1.2	mA
$I_{VDDIO(IDLE)}$	Logic supply current in Idle mode (COR)	V_{IDLE} = 5 V; V_{INn} = 0 V; VDDIO = 5 V; f_{SCLK} = 0 MHz; CFG_1.ACT = 0_B; PWM_SPI.OUTn = 0_B; DIAG_OFF_EN.OUTn = 0_B; VBATT = VDDIO - 1 V	2	-	5	mA
$I_{VDDIO(ACTIVE)}$	Logic supply current in Active mode – channels OFF	V_{IDLE} = 5 V; V_{INn} = 0 V; VDDIO = 5 V; f_{SCLK} = 0 MHz; CFG_1.ACT = 1_B; PWM_SPI.OUTn = 0_B; DIAG_OFF_EN.OUTn = 0_B	-	0.95	1.5	mA
$I_{VDDIO(ACTIVE_COR)}$	Logic supply current in Active mode – channels OFF (COR)	V_{IDLE} = 5 V; V_{INn} = 0 V; VDDIO = 5 V; f_{SCLK} = 0 MHz; CFG_1.ACT = 1_B; PWM_SPI.OUTn = 0_B; DIAG_OFF_EN.OUTn = 0_B; VBATT = VDDIO - 1 V	12	-	20	mA
$t_{VDDIOUVFLT}$	VDDIO undervoltage filter	Covered bySCAN	9	14	19	µs
Timings						
$t_{IDLEFLT}$	Idle filter time	-	5	7	10	µs
$t_{SLEEP2IDLE}$	Sleep to Idle delay	-	-	-	10	µs
$t_{IDLE2SLEEP}$	Idle to Sleep delay	from IDLE pin to sleep External pull-down MISO to GND required	-	-	10	µs
$t_{IDLE2ACTIVE}$	Idle to Active delay	from INn or NCS pins to MODE = 11_B	-	-	1	µs
$t_{ACTIVE2IDLE}$	Active to Idle delay	from INn or NCS pins to MODE = 10_B	-	-	150	µs
$t_{SLEEP2LH}$	Sleep to Limp Home delay	from INn pins to VDS = 10 % VBATT	-	-	10+tON	µs
$t_{LH2SLEEP}$	Limp Home to Sleep delay	from INn pins to MODE = 00_B External pull-down MISO to GND required.	-	-	150	µs
$t_{LH2ACTIVE}$	Limp Home to Active delay	from IDLE pin to MODE = 11_B	-	-	10	µs
$t_{ACTIVE2LH}$	Active to Limp Home delay	from IDLE pin to MODE = 01_B	-	-	10	µs
$t_{ACTIVE2SLEEP}$	Active to Sleep delay	from IDLE pin to MODE = 00_B External pull-down MISO to GND required.	-	-	150	µs

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7 Power stages

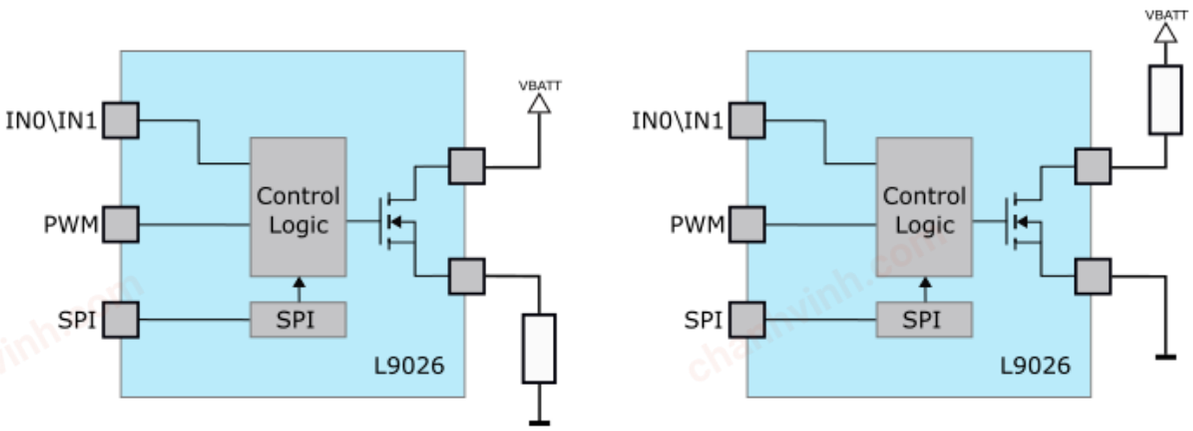
There are two fixed high-side channels and six channels which can be used either as low-side or as high-side switches. During the diagnosis in OFF State, the sequences of operations (pull-up or pull-down current source activation) are determined according to the SPI settings of CFG_0 register.

For the configurable channels, when in high-side configuration, the load is connected between ground and source of the power transistor (pins SOURCEn, n = 2...7) while the drains (pins DRAINn, n = 2...7) can be connected to any potential between ground and VBATT.

In low-side configuration, the source of the power transistors must be connected to GND pin potential (either directly or through a reverse current blocking diode).

The configuration can be chosen for each of these configurable channels individually via SPI.

Figure 8. HS driver (left) and LS driver (right) configuration



7.1 Operating modes

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J.

7.1.1 Switching resistive modes

When switching resistive loads, the following switching times and slew rates can be considered.

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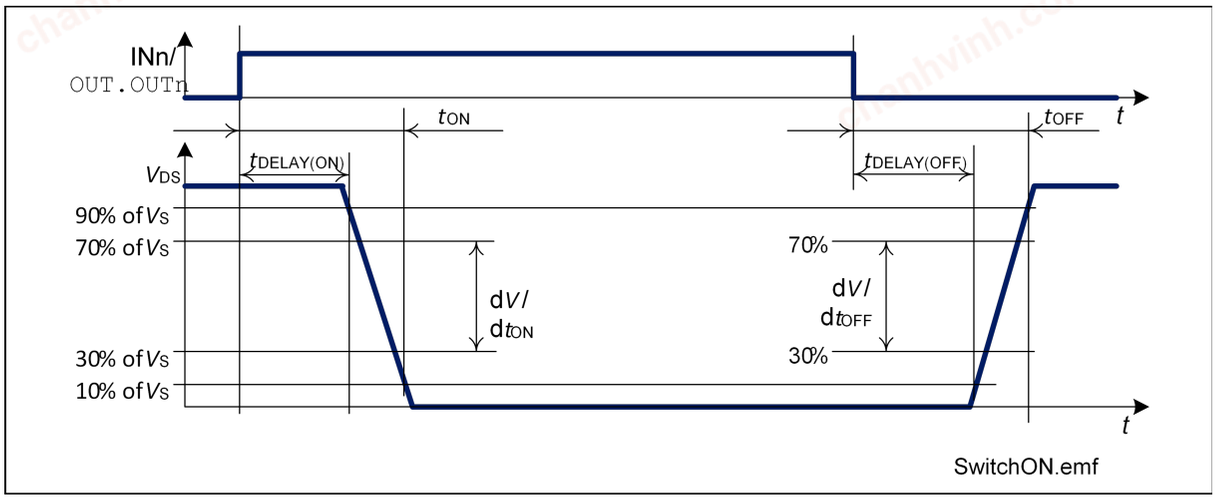
Figure 9. **Switching resistive loads**



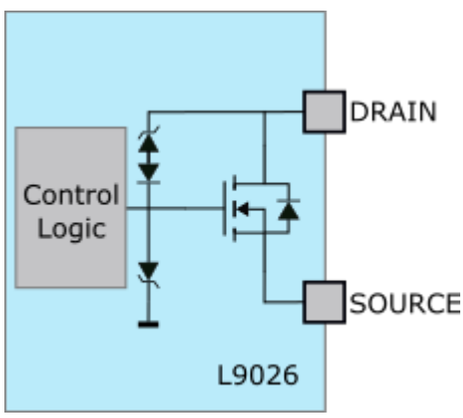
7.1.2 Inductive output clamp

When switching off inductive loads, the voltage across the power switch rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. In case of HS configuration, the potential at Output pin is not allowed to go below $V_{OUT_S(CL)}$. The voltage clamping is necessary to prevent device destruction.

To clarify this idea Figure 10 shows a concept drawing of the implementation.

Nevertheless, the maximum allowed load inductance is limited by the max energy. The clamping structure protects the device in all operative modes (Sleep, Idle, Active, Limp Home).

Figure 10. **Output clamp concept**



7.1.3 Maximum load inductance

During demagnetization of inductive loads, energy has to be dissipated device. Eq. (1)shows how to calculate the energy for low-side switches, while Eq. (2) can be used for high-side switches (auto-configurable switches can use all equations, depending on the load position):

$$E = V_{DS(CL)} \cdot \left[\frac{V_S - V_{DS(CL)}}{R_L} \cdot I_n \cdot \left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CL)}}\right) + I_L\right] \cdot \frac{L}{R_L} \quad (1)$$

$$E = \left(V_S - V_{DS(CL)}\right) \cdot \left[\frac{V_{OUTS(CL)}}{R_L} \cdot I_n \cdot \left(1 - \frac{R_L \cdot I_L}{V_{OUTS(CL)}}\right) + I_L\right] \cdot \frac{L}{R_L} \quad (2)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component. The E_{AR} value provided in Table 14 assumes that all channels can dissipate the same energy when the inductances connected to the outputs are demagnetized at the same time.

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7.2 Inverse current behavior

Inverse current ($V_{OUTn_S} > V_{OUTn_D}$) in high-side configuration may occur with channels in ON or in OFF state. A reverse current applied to a specific channel has no impact on the general functionality (switch ON and OFF, protection, diagnostic) of unaffected channels.

Parameter deviations are possible for the switching capability of the affected channel, while protection against Over Load and off state diagnostic are not available. Reliability in Limp Home condition for the unaffected channels remains unchanged.

7.3 Bulb inrush mode

Although device is optimized for relays and LED, it may be necessary to use one or more of the outputs as high-side switches to drive small lamps or electronic loads with a big input capacitor. In such a case the inrush current mat startup may trigger the overload diagnostic, switching the channel OFF.

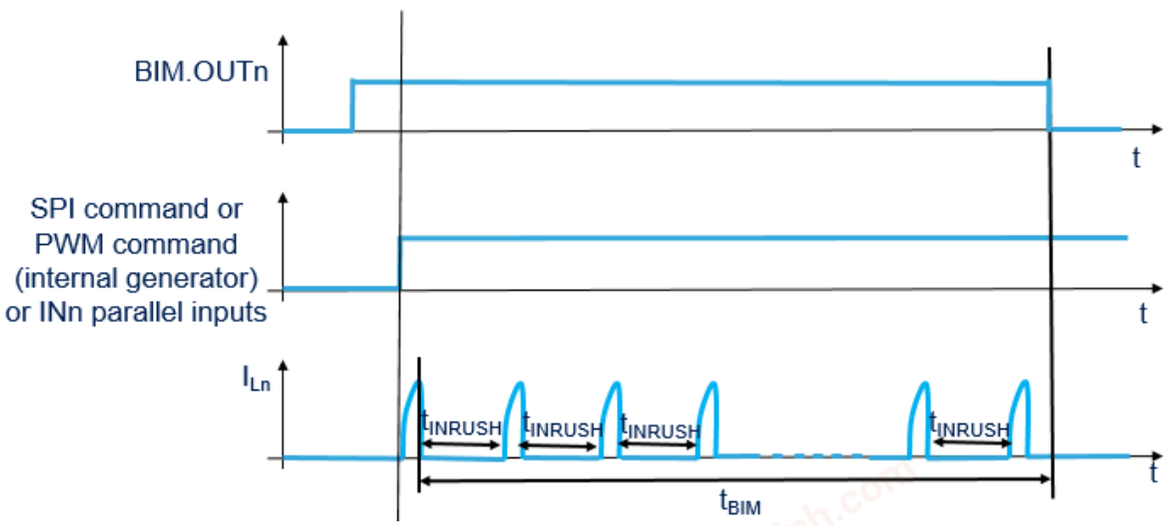
In normal operation in order to re-engage the channels from an overload condition, an SPI command to clear the latches (register DIAG_OVC_OVT) is needed, to allow the channel turning ON again; for some applications this re-engagement procedure takes too long to transfer enough energy to activate the load.

The IC provides means to overcome this issue by setting BIM.OUTn bit to “1”.

Once this feature is enabled, in case the channel reaches the overload current threshold and latches OFF, it restarts automatically after a time t_{INRUSH}, allowing the load to go out of the inrush phase. The automatic re-engagement of the faulty channels lasts for a BIM time (t_{BIM}). Once the t_{BIM} counter is started, it is reset only once the t_{BIM} is expired, unless a reset condition occurs (VDDIO_uv, hardware or software reset).

A time diagram is shown in Figure 11. The channel configured with BIM option can be either driven by an SPI command, PWM command (internal generator) or INn parallel input. Once programmed to “1” via SPI, the BIM.OUTn bit is set back to “0” at the end of BIM time (t_{BIM}), unless a reset condition occurs (VDDIO_uv, hardware or software reset): an eventual switch off of the channel commanded by the user has no impact on BIM.OUTn configuration.

Figure 11. Bulb inrush mode



When BIM.OUTn are set to “1”, eventual overcurrent/overtemperature conditions will flag DIAG_OVC_OVT.OUTn bit, but the affected channels will not be permanently switched OFF. Once asserted, eventual SPI attempt to clear DIAG_OVC_OVT.OUTn will be ignored, until the BIM counter is expired. In order to resume the normal behavior when the BIM counter is expired, the DIAG_OVC_OVT.OUTn shall be cleared in order to allow IC to perform open load ON diagnosis.

An internal timer set the bit BIM.OUTn back to “0” after 40 ms (parameter t_{BIM}) starting from the first overcurrent event latched to prevent an excessive thermal stress to the channel, especially in case of short circuit at the output.

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7.4 PWM generators

Device has two independent PWM generators, which are defined as “PWM GEN” and “PWM LED” here below. These can be assigned to one or more channels, and can be programmed with different duty cycles and frequencies. Both refer to the same base frequency f_{INT} (8 MHz typ) even if two separate pre-scalers can be defined.

7.4.1 PWM GEN

The first PWM generator is called PWM GEN. Its frequency pre-scaler can be adjusted using CFG_1.PWM_DIV_GEN bits to program target frequency and using CFG_2.FR_ADJ bits to modulate fine adjustments around the target. Configuration of fine adjustment is described in Table 11 while target frequency setting is reported in Table 12.

Table 11. Adjustment coefficients

CFG_2.FR_ADJ	Absolute delta to f_{INT} divider
00_B	0 %
01_B	-15 %
10_B	+15 %
11_B	0 %

The user can set the following parameters to configure the PWM generator:

- duty cycle (bits PWM_GEN_DC.DUTY_CYCLE)
  - 8 configuration bits are available, with 100/255 duty cycle resolution for each LSB
  - The maximum duty cycle achievable is 100% (PWM_GEN_DC.DUTY_CYCLE set to “11111111B”)
  - In case the duty cycle is changed, the next target is applied once the previous PWM period is over and the new one is started. Once a new target is programmed, the behavior above is valid also if the current duty is 100% while when the current duty is 0% the new target value is applied immediately.
- frequency (bits CFG_1.PWM_DIV_GEN)
  - 2 configuration bits are available to select the frequency among 4 target values

Table 12. PWM GEN generator available frequencies

CFG_1.PWM_DIV_GEN	PWM frequency
00_B	122.5 Hz
01_B	245.1 Hz
10_B	490.2 Hz
11_B	980.4 Hz

- Channels driven by PWM GEN (PWM_SEL and PWM_MAP registers)

The correct sequence to use the PWM generator is:

- define the frequency divider through CFG_1.PWM_DIV_GEN bit.
- define duty cycle control register through PWM_GEN_DC register.
- set up channel output control through PWM_SEL register (PWM GEN corresponds to 0)
- define channels driven by PWM selected in PWM_SEL through mapping register PWM_MAP

In order to clarify how to select the source that can drive the channels command, the driving tree with all possible sources (ie PWM generators, SPI and parallel inputs) is reported in Figure 12.

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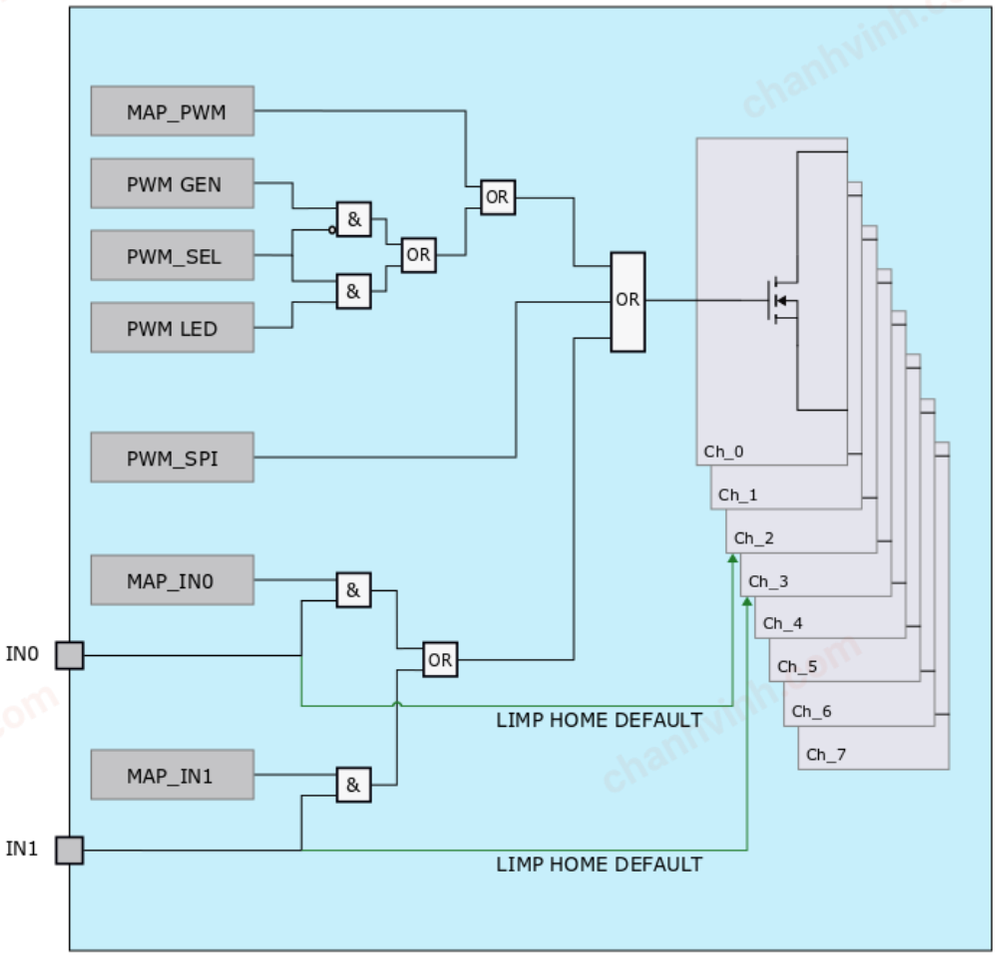
Figure 12. **Driving tree**



7.4.2 PWM LED

The second PWM generator is named PWM LED. Its frequency prescaler can be adjusted using CFG_2.PWM_DIV_LED bits (see Table 13) while the modulation around the defined target is actually shared with PWM GEN, using CFG_2.FR_ADJ bits described in Table 11.

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The user can set the following parameters to configure the PWM generator:

- duty cycle (bits PWM_LED_DC.DUTY_CYCLE)
  - 8 configuration bits are available, with 100/255 duty cycle resolution for each LSB
  - The maximum duty cycle achievable is 100% (PWM_LED_DC.DUTY_CYCLE set to “11111111B”)
  - In case the duty cycle is changed, the next target is applied once the previous PWM period is over and the new one is started. Once a new target is programmed, the behavior above is valid also if the current duty is 100% while when the current duty is 0% the new target value is applied immediately.
- frequency (bits CFG_1.PWM_DIV_LED)
  - 2 configuration bits are available to select the frequency among 4 target values

Table 13. PWM LED generator available frequencies

CFG_2.PWM_DIV_LED	PWM frequency
00_B	122.5 Hz
01_B	245.1 Hz
10_B	490.2 Hz
11_B	980.4 Hz

- Channels driven by PWM LED (PWM_SEL and PWM_MAP registers)

The correct sequence to use the PWM LED generator is:

- define the frequency divider through CFG_1.PWM_LED_GEN bit.
- define duty cycle control register through PWM_LED_DC register.
- set up channel output control through PWM_SEL register (PWM LED corresponds to 0)
- define channels driven by PWM selected in PWM_SEL through mapping register PWM_MAP

7.5 Power stages electrical specifications

3 V ≤ VDDIO ≤ 5.5 V; 6 ≤ VBATT ≤ 18 V; -40 °C ≤ Tj ≤ 150 °C unless otherwise noted. All voltages are referred to GND pin.

Table 14. Power stages electrical parameters

Parameter	Description	Test condition	Min	Typ	Max	Unit
$R_{DS(ON)}$	On-State Resistance	T_J = 25 °C	-	0.75	-	Ω
$R_{DS(ON)}$	On-State Resistance	T_J = 150 °C; I_L = 100 mA	-	-	1.5	Ω
$I_{L(NOM)}$	Nominal load current (all channels active)	T_J ≤ 150 °C; Design info	-	260	500	mA
E_{AS}	Maximum energy dissipation single pulse	T = 25 °C, IL = 2XIL(EAR)	-	-	50	mJ
E_{AS}	Maximum energy dissipation single pulse	T = 150 °C, IL = 400 mA	-	-	25	mJ
$I_{L(EAR)}$	Load current for maximum energy dissipation – repetitive (all channels active)	T_J ≤ 150 °C; Design info	-	220	-	mA
E_{AR}	Maximum energy dissipation repetitive pulses - 2*$I_{L(EAR)}$ (two channels in parallel)	$T_{J(0)}$ = 85 °C; $I_{L(0)}$ = 2*$I_{L(EAR)}$; 2*10^6 cycles	-	-	15	mJ
E_{AR}	Maximum energy dissipation repetitive pulses - $I_{L(EAR)}$	T = 85 °C, 2*10exp6 cycles	-	-	10	mJ
V_{DS}	Voltage at power transistor	-	-0.3	-	$V_{D(CL)}$	V
$V_{D(CL)}$	Drain to GND Output clamping voltage LS	I_L = 10 mA; Low-Side Configuration	45	47	49	V

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Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{S(CL)}$	Source to GND Output clamping voltage HS	I_L = 10 mA; V_{BATT} = V_{OUT_Dn} = 7 V; High-Side Configuration	-18	-17	-16	V
$I_{L(OFF)}$	Output leakage current (each channel) T_J = 150 °C	V_{BATT} = 0 V; V_{DDIO} = 0 V; V_{SOURCE} = 0 V; V_{DS} = 28 V; T_J up to 150 °C	-3	0	3	µA
$I_{L(OFF)_HS}$	Output leakage current (each channel) T_J = 150 °C	V_{BATT} = 28 V; V_{DDIO} = 0 V; V_{SOURCE} = 0 V; V_{DS} = 28 V; T_J up to 150°C – High side case	-3	-	3	µA
$I_{(OFF)_HS}$	Output current (each channel) in High side case	High side configuration, Power OFF, V_{SOURCE} = 0 V	-70	-	-30	µA
$I_{(OFF)_HS}$	Output current (each channel) in High side case	High side configuration, Power OFF, V_{SOURCE} = 2.5V	-10	-	10	µA
Timing						
$t_{DELAY(ON)}$	Turn-ON delay (from INn pin or bit to V_{OUT} = 90% VBATT) (Channels used as Low-Side)	RL = 50 Ω VBATT= 14 V Active or Limp Home mode	3	5	7	µs
$t_{DELAY(OFF)}$	Turn-OFF delay (from INn pin or bit to VOUT = 10% VBATT) (Channels used as Low-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	2.5	10	21	µs
t_{ON}	Turn-ON time (from INn pin or bit to VOUT = 10% VBATT) (Channels used as Low-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	7	15	35	µs
t_{OFF}	Turn-OFF time (from INn pin or bit to VOUT = 90% VBATT) (Channels used as Low-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	4	-	40	µs
dV/dt_{ON}	Turn-ON slew rate VDS = 70% to 30% VBATT (Channels used as Low-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	0.35	1	2.2	V/µs
$-dV/dt_{OFF}$	Turn-OFF slew rate VDS = 30% to 70% VBATT (Channels used as Low-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	0.15	1.3	3.4	V/µs
$-dV/dt_{OFF}$	Turn-OFF slew rate VDS = 30% to 70% VBATT Gate kill condition (Channels used as Low-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	12	-	35	V/µs
$t_{DELAY(ON)}$	Turn-ON delay (from INn pin or bit to VOUT = 10% VBATT) (Channels used as High-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	1.2	3.5	7.5	µs
$t_{DELAY(OFF)}$	Turn-OFF delay (from INn pin or bit to VOUT = 90% VBATT) (Channels used as High-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	2	10	21	µs
t_{ON}	Turn-ON time (from INn pin or bit to VOUT = 90% VBATT) (Channels used as High-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	7	16	25	µs
t_{OFF}	Turn-OFF time (from INn pin or bit to VOUT = 10% VBATT) (Channels used as High-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	5	19	35	µs
dV/dt_{ON}	Turn-ON slew rate VDS = 30% to 70% VBATT (Channels used as High-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	0.25	1	1.9	V/µs
$-dV/dt_{OFF}$	Turn-OFF slew rate VDS = 70% to 30% VBATT (Channels used as High-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	0.25	-	2.5	V/µs
$-dV/dt_{OFF}$	Turn-OFF slew rate VDS = 70% to 30% VBATT Gate kill condition (Channels used as High-Side)	RL = 50 Ω; VBATT= 14 V; Active or Limp Home mode	6	-	30	V/µs
t_{INRUSH}	Bulb Inrush Mode restart time	Active mode; Covered by SCAN	29	40	51	µs

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Parameter	Description	Test condition	Min	Typ	Max	Unit
t_{BIM}	Bulb Inrush Mode reset time	Active mode; Covered by SCAN	29	41	52	ms

Table 15. PWM electrical parameters

Parameter	Description	Test condition	Min	Typ	Max	Unit
f_{INT}	Internal reference frequency	Covered by SCAN	-	8	-	MHz
$f_{INT(VAR)}$	Internal reference frequency variation		-15	-	15	%
t_{SYNC}	Internal reference frequency synchronization time	Covered by SCAN	-	-	10.5	ms

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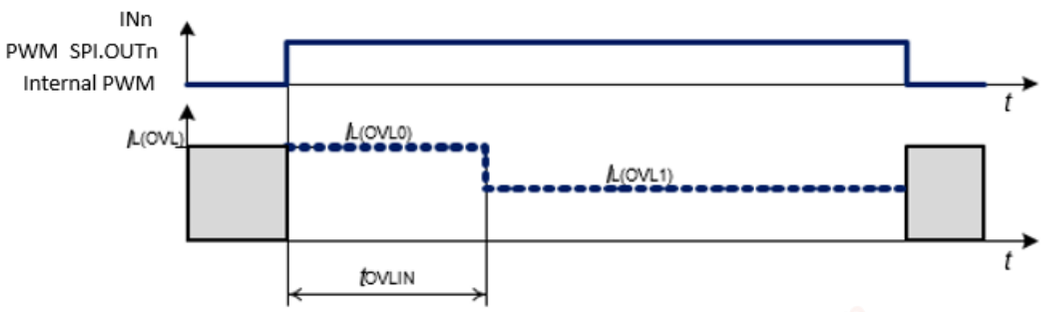
8 Protection functions

8.1 Overload protection

Device is protected in case of over load or short circuit of the load. This protection is present for each HS and LS driver. There are two over load current thresholds (see Figure 13):

- $I_{L(OVL0)}$ between channel switch ON and $t_{OVLINDS1}$
- $I_{L(OVL1)}$ after t_{OVLIN}

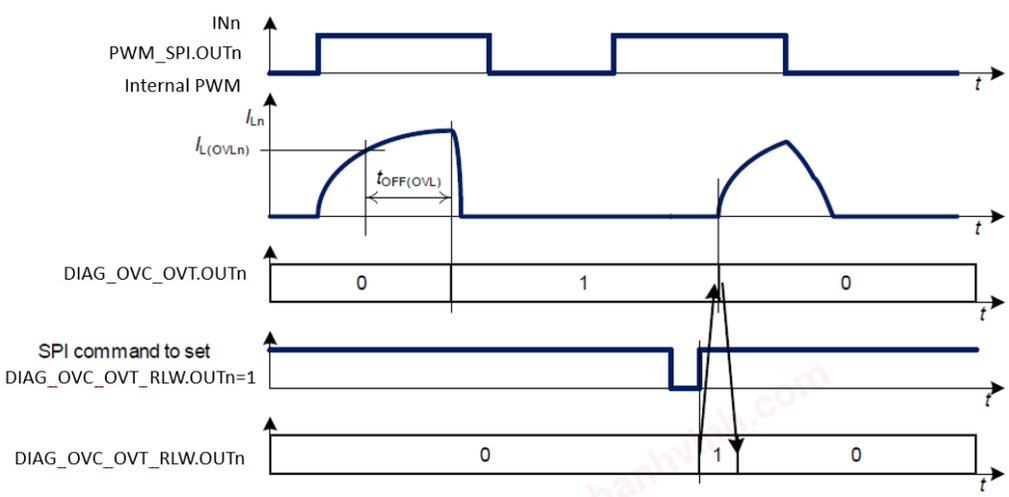
Figure 13. Overload thresholds



Every time the channel is switched OFF the over load current threshold is set back to $I_{L(OVL0)}$.

In case the load current is higher than $I_{L(OVL0)}$ or $I_{L(OVL1)}$, after time $t_{OFF(OVL)}$ the over loaded channel is switched OFF and the corresponding diagnosis bit DIAG_OVC_OVT.OUTn is set to “1”. The channel can be switched ON after clearing the protection latch by setting the corresponding DIAG_OVC_OVT_RLW.OUTn bit to “1”. This bit is set back to “0” internally after de-latching the channel. Please refer to Figure 14 for details.

Figure 14. Latch off in overload condition



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8.2 Over temperature protection

A temperature sensor is integrated for each channel. Totally 8 temperature sensors are present, which switch OFF the channel in over temperature in order to prevent destruction.

Once a channel over temperature is detected, the corresponding diagnosis bit DIAG_OVC_OVT is set (combined with Over Load protection). The channel can be switched ON after clearing the protection latch by setting the corresponding DIAG_OVC_OVT_RLW.OUTn bit to “1”. This bit is set back to “0” internally after de-latching the channel.

8.3 Over temperature and over load in Limp Home mode

In Limp Home mode, channels 2 and 3 can be switched ON using the input pins. In case of Over Load, Short Circuit or Over Temperature the channels are switched OFF. If the input pins remain “high”, meaning that the channel is still required to be on, in case of Over Load the channels restart at every t_{RETRY}.

8.4 Reverse polarity protection

In Reverse Polarity (also known as Reverse Battery) condition, power dissipation is caused by the intrinsic body diode of each DMOS. The reverse current through the channels has to be limited by the connected loads.

In order to sustain the Reverse polarity condition the exposed pad of device must be left electrically floating.

8.5 Electrical characteristics

3 V ≤ VDDIO ≤ 5.5 V; 6 V ≤ VBATT ≤ 18 V; -40 °C ≤ Tj ≤ 150 °C unless otherwise noticed. All voltages are referred to GND pin.

Table 16. Over temperature and over load electrical parameters

Symbol	Description	Test condition	Min	Typ	Max	Unit
$I_{L(OVL0_LS)}$	Over Load detection current (Channels used as Low-Side)	T_J = -40 °C	1	-	1.9	A
$I_{L(OVL0_LS)}$	Over Load detection current (Channels used as Low-Side)	T_J = 25 °C	1	-	1.7	A
$I_{L(OVL0_LS)}$	Over Load detection current (Channels used as Low-Side)	T_J = 150 °C	1	-	1.7	A
$I_{L(OVL1_LS)}$	Over Load detection current (Channels used as Low-Side)	T_J = -40 °C	0.6	-	1	A
$I_{L(OVL1_LS)}$	Over Load detection current (Channels used as Low-Side)	T_J = 25 °C	0.6	-	1	A
$I_{L(OVL1_LS)}$	Over Load detection current (Channels used as Low-Side)	T_J = 150 °C	0.6	-	1	A
$I_{L(OVL0_HS)}$	Over Load detection current (Channels used as High-Side)	T_J = -40 °C	1.2	-	2.1	A
$I_{L(OVL0_HS)}$	Over Load detection current (Channels used as High-Side)	T_J = 25 °C	1.2	-	1.9	A
$I_{L(OVL0_HS)}$	Over Load detection current (Channels used as High-Side)	T_J = 150 °C	1	-	1.7	A
$I_{L(OVL1_HS)}$	Over Load detection current (Channels used as High-Side)	T_J = -40 °C	0.7	-	1.4	A
$I_{L(OVL1_HS)}$	Over Load detection current	T_J = 25 °C	0.7	-	1.3	A

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Symbol	Description	Test condition	Min	Typ	Max	Unit
	(Channels used as High-Side)					
$I_{L(OVL1_HS)}$	Over Load detection current (Channels used as High-Side)	T_J = 150 °C	0.7	-	1.2	A
t_{OVLIN}	Over Load threshold switch delay time	Covered by SCAN	110	170	260	µs
$t_{OFF(OVL)}$	Over Load shut-down delay time	BIM.OUTn = 0_B	4	7	11	µs
$T_{J(SC)}$	Thermal shut-down temperature	-	182	192	202	°C
t_{RETRY}	Restart time in Limp Home mode	Covered by SCAN	29	41	52	ms
t_{OVC}	Restart time in Limp Home mode	Covered by SCAN	-	-	50	µs

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9 Diagnosis

The SPI interface provides diagnosis information about the device and the load status. Each channel diagnosis information is independent of other channels. A faulty condition on one channel has no influence on the diagnostic of other channels in the device.

9.1 Over load and Over temperature

When either an Over Load or an Over Temperature occurs on one channel, the diagnosis bit DIAG_OVC_OVT is set accordingly. The channel latches OFF and must be reactivated setting corresponding DIAG_OVC_OVT_RLWn bit to “1”. The writing operation is necessary to remove the fault as a consequence of the fact that DIAG_OVC_OVT register is clear on write.

9.2 OFF diagnosis

This diagnosis is available only in Active mode.

The device is able to detect two kind of faults in OFF, open load and short (to battery in HS configuration or to ground in LS configuration).

This diagnosis is available upon SPI request; Once the diagnosis has been started on one or more channels, a new eventual diagnosis request is ignored until the ongoing cycle is finished.

The diagnosis strategy is implemented over two different phases:

- First the IC distinguishes between faulty and no faulty condition.
- In case of trouble found in the previous step, a specific procedure is put in place to detect the nature of the fault.

The diagnosis is slightly different depending on a LS or HS configured output.

The strategy in LS configuration is reported below and referred to Figure 15; the HS case is quite similar, except for the order in which pull-up and pull-down current generators are activated and for the pin involved (SOURCEn for a HS configured channel, DRAINn for a LS).

- This first phase lasts for t_{OFF1LS}.

  The current generator marked with ‘pldw’ (driven by dw_on) is active while the current generator marked as ‘plup’ is off..

  In this condition, if the drain voltage remains above the threshold $V_{DS(OL)}$, the comparator output is low which means that a load is present.

  If the drain voltage decreases below the threshold, instead, the comparator flags the presence of a fault.
- This second phase lasts for t_{OFF2LS}.

  After the first diagnosis step the output of the comparator is set to ‘1’ if a faulty condition has been found.

  The current generator marked with ‘plup’ (driven by the signal up_on) is activated while ‘pldw’ is off.

  In case, after the pull-up activation, the drain voltage rises and overcomes the comparator threshold again, an Open Load fault is reported.

  If the voltage remains constant and equal to zero for the whole diagnosis time, instead, a Short to ground fault is recognized.

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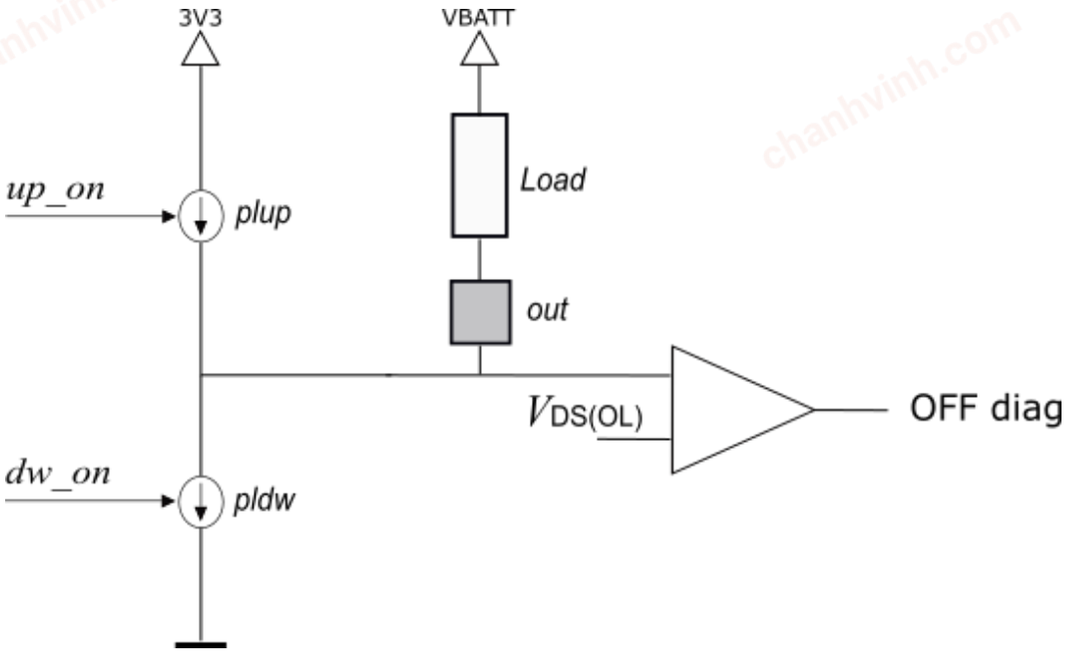
Figure 15. **OFF diagnosis circuit**



9.3 Open load at ON

On each channel it is possible to request the open load at on diagnosis.

This diagnosis is designed having in mind a specific case of high side channels driving LEDs kept fully ON.

Moreover, the device will ignore the request of an open load at on diagnosis in case the channel is configured as low side. This means that the request diagnosis register will not be updated in case it is requested the diagnosis on a low side configured channel.

Such a diagnosis is not recommended in case of loads driven in PWM mode (to avoid eventual interferences with the PWM driving signal) and inductive loads (to avoid unwanted power dissipations during switch OFF transients).

9.3.1 Open load at ON (diagnosis mechanism)

The diagnosis cannot be run on more channels simultaneously, but it can work only on one channel at a time.

This can be activated by setting the bit corresponding to the desired channel in the DIAG_OPL_ON_EN register.

During the diagnostic loop the channel is switched off every t_{OPLCYC} for a maximum time of t_{OPLEN}.

Such a time is designed to be short enough to result in a negligible variation of the luminescence of LED during the test.

During the short switch-off time required to perform the diagnosis a pull-up current generator $I_{L(OL)}$ is applied to the source of the channel, as can be seen from Figure 16.

If the load is present the source voltage drops suddenly, the output of the comparator is set and channel immediately restarts.

If an open load condition exists, instead, the pull-up current $I_{L(OL)}$ is capable of keeping the source voltage to battery and the Vds value remains stable for the whole diagnosis time interval.

In this case once t_{OPLEN}, is elapsed, the comparator output is still low and the flag related to the fault is set; the channel is anyway restarted.

The OPL ON diagnosis lasts just a t_{OPLEN} time in the worst case scenario, i.e. when the open load is detected.

Once an SPI frame commanding the diagnostic is received, the diagnosis will start a T_{oplcyc} time after the corresponding request has been accepted.

As long as the diagnosis request bit remains high the open load test will be performed every T_{oplcyc} and the results of the diagnosis will be reported in the register DIAG_OPL_ON: if an open load on channel ‘n’ is detected, the corresponding bit DIAG_OPL_ONn is set.

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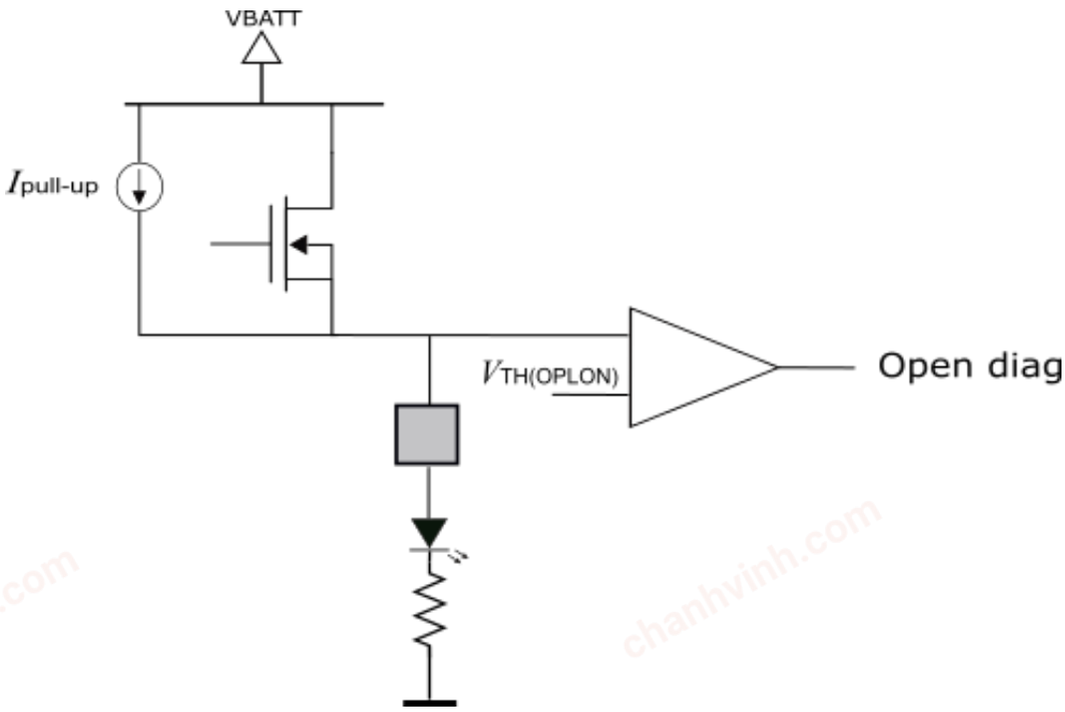
The OPL ON diagnosis can be performed only if the DIAG_OVC_OVT.OUTn flag is not asserted and can be run only on a single channel for each diagnostic cycle: an eventual diagnostic cycle performing OPL ON on multiple channels will not be executed and SPI command will have no effect.

Once the current diagnostic cycle is over, a new cycle can be started with OPL ON diagnosis requested for a different channel.

Figure 16. Open load at ON circuit



9.3.2 Open load at ON bit

In the DIAG_OPL_ON register there are 8 bits that can assume the following values:

- “0” = no Open Load at ON state detected, or the channel is OFF when the diagnosis is performed
- “1” = Open Load at ON state detected

This register is clear on read. An SPI read is necessary to clear the faulty information.

Once the DIAG_OPL_ON flag is set, it remains asserted until a new diagnostic cycle is completed when the fault is no longer present, and the diagnostic register is read through SPI.

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9.4 Electrical parameters

3 V ≤ VDDIO ≤5.5; 6 V ≤ VBATT ≤ 18 V; -40 °C ≤ Tj ≤ 150 °C unless otherwise noticed. All voltages are referred to GND pin.

Table 17. Output status and open load ON electrical parameters

Symbol	Description	Test condition	Min	Typ	Max	Unit
Output status monitor						
$V_{DS(OL)}$	Output Status Monitor threshold voltage	VBATT = 14 V; Active	1.7	1.95	2.2	V
I_{OLD_LS}	Output diagnosis pull down current (channels used as Low Side)	V_{DRAIN} = 14V (channels used as Low Side)	290	-	550	µA
I_{OLU_LS}	Output diagnosis pull up current (channels used as Low Side)	V_{DRAIN} = 0 V (channels used as Low Side)	-260	-	-140	µA
I_{OLD_HS}	Output diagnosis pull down current (channels used as High Side)	V_{SOURCE} = 14 V (channels used as High Side)	320	-	520	µA
I_{OLU_HS}	Output diagnosis pull up current (channels used as High Side)	V_{SOURCE} = 0 V (channels used as High Side)	-310	-	-160	µA
Open load at ON						
t_{OPLCYC}	Open Load at ON Diagnosis cycle time	Covered by SCAN	120	160	210	ms
t_{OPLEN}	Open Load at ON Diagnosis time	Covered by SCAN	30	45	55	µs
t_{OFF1LS}	Diag OFF LS first window	Covered by SCAN	0.96	1.03	1.28	ms
t_{OFF2LS}	Diag OFF LS second window	Covered by SCAN	210	250	290	µs
t_{OFF1HS}	Diag OFF HS first window	Covered by SCAN	210	250	290	µs
t_{OFF2HS}	Diag OFF HS second window	Covered by SCAN	0.96	1.03	1.28	ms
$V_{TH(OPLON)}$	Voltage threshold for HS OPL ON Diagnosis at VS pin	Active mode	VDrain-1.3	VDrain-1.2	VDrain-1.1	V
$I_{TH(OPLON)}$	Current provided by the source while forcing VBAT-3V on Source pin	VS = VBAT-3 V; Active mode	1.2	-	2	mA

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10 Limp Home mode

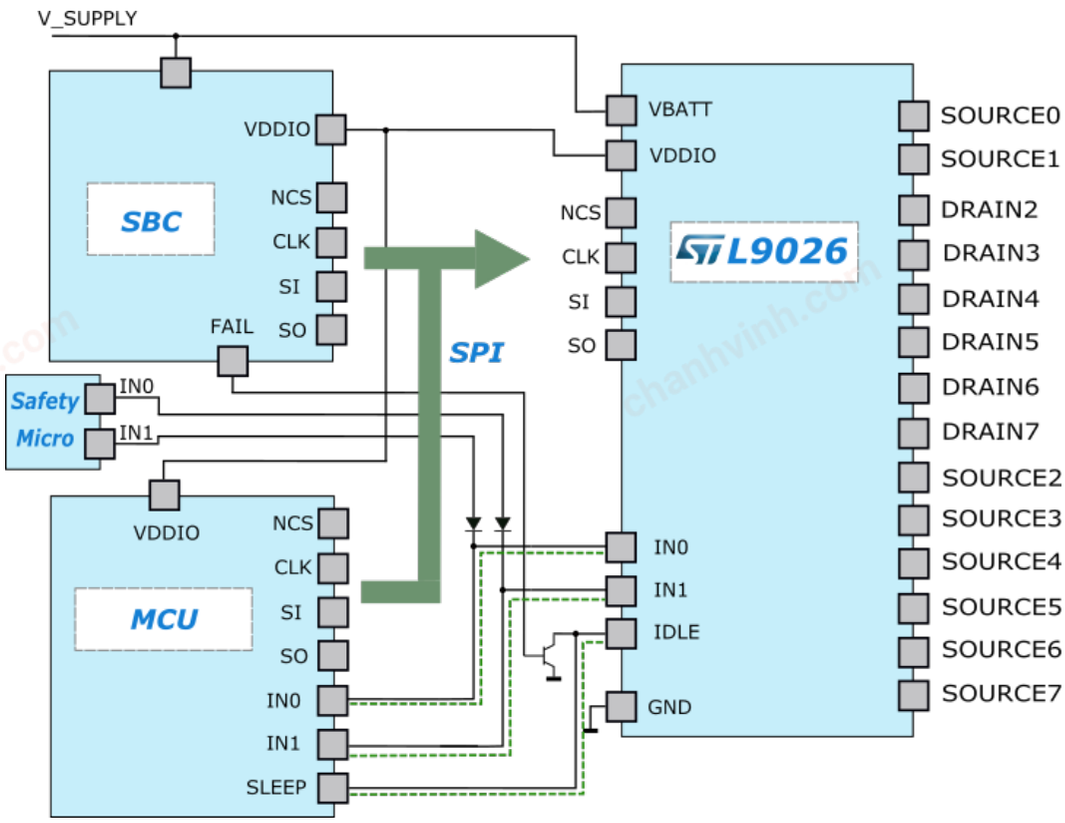
The Limp is intended to handle limited functionality of the device in critical faulty situations.

A typical application scenario is reported in Figure 17, with a system which is reconfigured during Limp Home as shown in Figure 18.

Shall the micro that controls the device fail, an external safety micro takes over controlling parallel inputs IN0 and IN1. The SBC will force the IDLE signal low which brings the device in Limp Home. Once the switching activity on IN0, IN1 is over, being the IDLE pin still de-asserted, the device will reach Sleep mode.

During this mode active, L9026 is only capable of driving two outputs i.e. OUT2 through IN0 and OUT3 through IN1; such a mapping is fixed and overcomes an eventual different mapping programmed via SPI once the Limp Home is reached.

Figure 17. Possible system configuration during normal operating conditions



In Figure 17 the dotted green lines mark the signals path when the device is operating in normal node, IDLE, IN0, IN1 are provided by the main MCU. Figure 18 shows a possible Limp Home configuration where the dotted blue lines mark the signals path.

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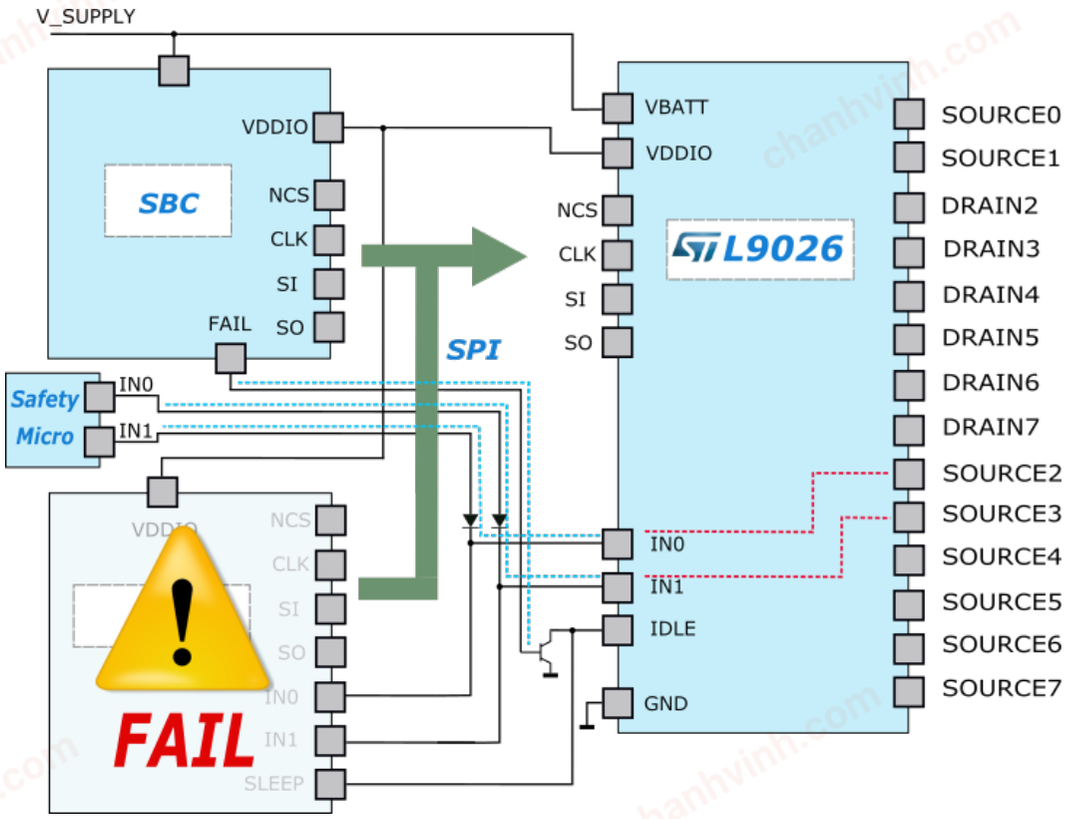
Figure 18. **Possible system configuration during Limp mode**



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11 SPI

The SPI interface is used to configure the device, control the outputs and read diagnostic and status registers.

11.1 SPI protocol

The serial peripheral interface (SPI) is a full duplex synchronous serial out-of-frame slave interface, with four lines: SO, SI, CLK and NCS. Data is transferred by the lines MOSI and MISO at the rate given by CLK.

Considering the out-of-frame protocol implemented, it is important to ignore the first MISO received at the start of communication because is meaningless.

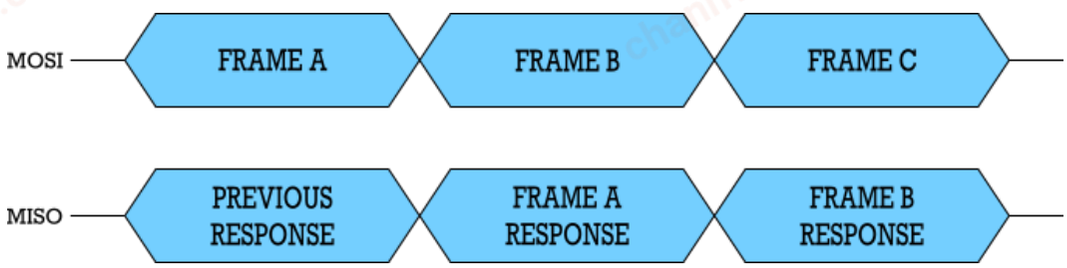
The falling edge of NCS defines the start of the SPI frames. L9026 samples the MOSI line (SI) at the rising edge of CLK while the output data is shifted out on line MISO (SO) at the falling edge of CLK. (CPOL='0', CPHA = '0'). End of SPI access is defined by a rising edge of NCS.

L9026 implements feature to guarantee that SPI frame is considered valid when at least 16 bits have been transferred: in case of transaction with less than 16 bit is received, the frame will be discarded and ERR bit is asserted in next SPI frame. An SPI access with frame longer than 16 bits will be not discarded in order to allow daisy chain operation.

As additional safety feature, the protocol is also equipped with 1 PARITY bit (odd parity) and a 1 bit frame counter; the frame counter value to be considered at the beginning of a new communication session after a reset action is "0". In case an incorrect frame counter value is detected, ERR bit is asserted in next SPI frame. The detailed structure of MOSI and MISO frames is shown in Section 11.5 SPI frame structure.

The relationship between MOSI and MISO content during SPI communication is shown in Figure 19: the protocol implements an out-of-frames strategy.

Figure 19. SPI out-of-frame protocol



During the Limp Home the SPI is in read only mode while no SPI access is possible during device Sleep Mode: eventual frames are ignored and MISO pin remains in high impedance.

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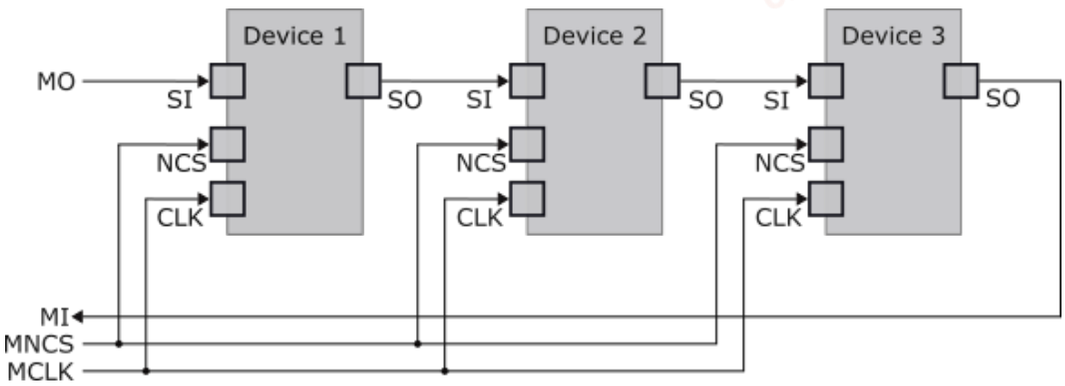
11.2 Daisy chain capability

L9026 implements SPI with daisy chain capability where a single master can address multiple slaves by driving a single NCS and MOSI lines, getting back data from a single MISO line as reported in the Figure 20.

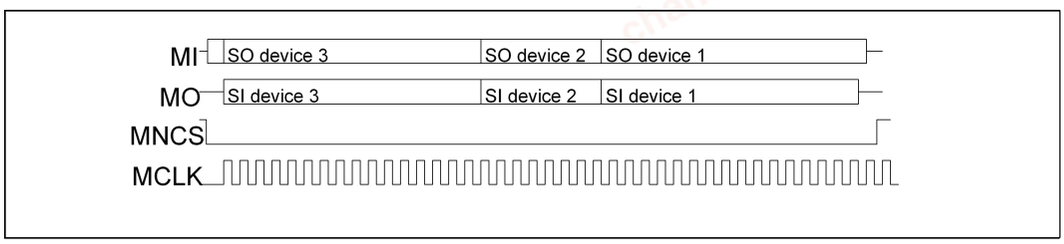
Figure 20. SPI Daisy chain configuration



In order to gain flexibility, the daisy chain approach can be used not only to address multiple L9026 but the IC allows addressing also mixed configurations, provided that all the elements of the chain work with CPOL = 0, CPHA = 0.

As reported in Figure 21, the only condition to be met is that the frame loaded inside each device of the chain is consistent and error free once the MNCS is de-asserted.

Figure 21. SPI message in daisy chain configuration



11.3 SPI electrical specifications

3 V ≤ VDDIO ≤ 5.5 V; 6 V ≤ VBATT ≤ 18 V; -40 °C ≤ Tj ≤ 150 °C unless otherwise noticed. All voltages are referred to GND pin.

Table 18. SPI electrical parameters

Parameter	Description	Test condition	Min	Typ	Max	Unit
Input SPI pins – low level						
$V_{NCS(L)}$	NCS	-	-	-	0.8	V
$V_{CLK(L)}$	CLK	-	-	-	0.8	V
$V_{SI(L)}$	SI	-	-	-	0.8	V
Input SPI pins – high level						
$V_{NCS(H)}$	NCS	-	2	-	-	V
$V_{CLK(H)}$	CLK	-	2	-	-	V
$V_{SI(H)}$	SI	-	2	-	-	V

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Parameter	Description	Test condition	Min	Typ	Max	Unit
Input pull up resistor at NCS pin						
R_{NCS}	L-input pull-up resistor at NCS pin	V_{NCS} = 0.8 V	40	58	95	KΩ
Input pull down resistor at pin						
R_{CLK}	Input pull-down resistor on CLK	V_{CLK} = 2 V	70	-	140	KΩ
R_{SI}	Input pull-down resistor on SI	V_{SI} = 2 V	70	-	140	KΩ
Output characteristics						
$V_{SO(L)}$	L level output voltage	I_{SO} = -1.5 mA	0	-	0.4	V
$V_{SO(H)}$	H level output voltage	I_{SO} = 1.5 mA	VDDIO -0.4	-	VDDIO	V
$I_{SO(OFF)}$	Output tristate leakage current	V_{NCS} = VDDIO VBATT = 0 V	-1	-	1	µA
$I_{SO(OFF)}$	Output tristate leakage current	V_{NCS} =VDDIO VBATT = VDDIO	-1	-	1	µA
Timings						
$t_{CSN(lead)}$	Enable lead time (falling NCS to rising CLK)	VDDIO = 4.5 V or VBATT > 7 V	200	-	-	ns
$t_{CSN(lag)}$	Enable lag time (falling CLK to rising NCS)	VDDIO = 4.5 V or VBATT > 7 V	200	-	-	ns
$t_{CSN(td)}$	Transfer delay time (rising NCS to falling NCS)	VDDIO = 4.5 V or VBATT > 7 V	650	-	-	ns
$t_{SO(en)}$	Output enable time (falling NCS to SO valid)	VDDIO = 4.5 V or VBATT > 7 V; C_L = 20 pF at MISO pin	-	-	200	ns
$t_{SO(dis)}$	Output disable time (rising NCS to SO tristate)	VDDIO = 4.5 V or VBATT > 7 V; C_L = 20 pF at MISO pin	-	-	200	ns
f_{SCLK}	Serial clock frequency	VDDIO = 4.5 V or VBATT > 7 V	-	-	8	MHz
$t_{SCLK(H)}$	Serial clock “high” time	VDDIO = 4.5 V or VBATT > 7 V	45	-	-	ns
$t_{SCLK(L)}$	Serial clock “low” time	VDDIO = 4.5 V or VBATT > 7 V	45	-	-	ns
$t_{SI(su)}$	Data setup time (required time MOSI to falling CLK)	VDDIO = 4.5 V or VBATT > 7 V	30	-	-	ns
$t_{SI(h)}$	Data hold time (falling CLK to SI)	VDDIO = 4.5 V or VBATT > 7 V	30	-	-	ns

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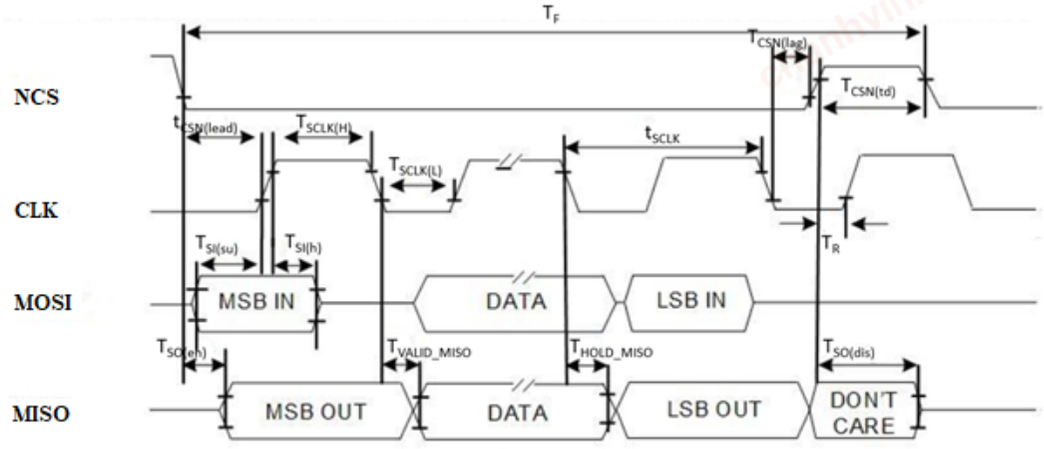
11.4 SPI timing diagram

Figure 22. **SPI timing diagrams**



11.5 SPI frame structure

11.5.1 MOSI frame structure

Each MOSI frame has 16 bits with the following structure:

- 1 command bit R/W, ‘1’ for write, ‘0’ for read
- 5 ADDRESS bits
- 8 DATA bits
- 1 PARITY bit, odd parity, calculated on bit [2:15]
- 1 FR_CNT frame counter bit

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	ADDRESS					DATA								PAR	FR_CNT

11.5.2 MISO frame structure

Each MISO frame has 16 bits with the following structure:

- 1 ERR error bit, ‘1’ if an error happened in the previous transmission, ‘0’ otherwise
- 5 ADDRESS bits
- 8 DATA bits
- 1 PARITY bit, odd parity, calculated on bit [2:15]
- 1 FR_CNT frame counter bit

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	ADDRESS					DATA								PAR	FR_CNT

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11.6 SPI register

11.6.1 Register structure

CHIP_ID

Register name:	CHIP_ID
Address:	Global Base Address + 0x00
Description:	Chip ID register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
CHIP_ID	RO	0	8	AA Bit 0->7 00100010 BA Bit 0->7 00101010 BB Bit 0->7 01010101	X	8 bit chip identifier

CFG_0

Register name:	CFG_0
Address:	Global Base Address + 0x01
Description:	Configuration 0

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	2	6	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:2], MSB refers to channel 7 0: (default) OUTn low side 1: OUTn high side
DIS_EN	RW	1	1	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	0: (default) DIS pin masked 1: DIS pin not masked
NRES_EN	RW	0	1	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	0: (default) NRES pin masked 1: NRES pin not masked

CFG_1

Register name:	CFG_1
Address:	Global Base Address + 0x02
Description:	Configuration 1

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
RST	WO	7	1	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Reset 0: (default) Normal operation 1: Execute Reset command (self clearing)
ACT	RW	6	1	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	active mode 0: (default) Normal operation or device leaves Active Mode 1: device enters and hold in Active Mode
NU	RO	2	4	0x00	X	-

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PWM_DIV_LED	RW	0	2	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	00: (default) PWM_FRQ=122.5Hz 01: PWM_FRQ=245.1Hz 10: PWM_FRQ=490.2Hz 11: PWM_FRQ=980.4Hz

CFG_2

Register name:	CFG_2
Address:	Global Base Address + 0x03
Description:	Configuration 2

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
NU	RO	4	4	0x00	X	-
FR_ADJ	RW	2	2	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	00: NO FREQ ADJUSTMENT 01: -15% ON SELECTED FREQUENCY 10: +15% ON SELECTED FREQUENCY 11: NO FREQ ADJUSTMENT
PWM_DIV_GEN	RW	0	2	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	00: (default) PWM_FRQ=122.5Hz 01: PWM_FRQ=245.1Hz 10: PWM_FRQ=490.2Hz 11: PWM_FRQ=980.4Hz

BIM

Register name:	BIM
Address:	Global Base Address + 0x04
Description:	Bulb Inrush Mode register configuration

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: (default) no BIM active 1: BIM active

RESERVED_1

Register name:	RESERVED_1
Address:	Global Base Address + 0x05
Description:	Reserved

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
UNUSED	RO	0	8	0x00	X	-

PWM_SPI

Register name:	PWM_SPI
Address:	Global Base Address + 0x06

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Description:	Power output control register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: (default) Output OFF 1: Output ON

MAP_IN0

Register name:	MAP_IN0
Address:	Global Base Address + 0x07
Description:	IN0 input mapping register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	0	8	0x04 OUT2 mapped on IN0	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: OUTn not driven by IN0 1: OUTn driven by IN0

MAP_IN1

Register name:	MAP_IN1
Address:	Global Base Address + 0x08
Description:	IN1 input mapping register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	0	8	0x08 OUT3 mapped on IN1	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: OUTn not driven by IN1 1: OUTn driven by IN1

MAP_PWM

Register name:	MAP_PWM
Address:	Global Base Address + 0x09
Description:	Internal PWM generator mapping register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: OUTn not driven by internal PWM generator 1: OUTn driven by internal PWM generator

PWM_SEL

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Register name:	PWM_SEL
Address:	Global Base Address + 0x0A
Description:	Internal PWM generator selection register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: (default) PWM_GEN selected for OUTn 1: PWM_LED selected for OUTn

PWM_GEN_DC

Register name:	PWM_GEN_DC
Address:	Global Base Address + 0x0B
Description:	PWM GEN duty cicle setting

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
DUTY_CYCLE	RW	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	b00000000, PWM GEN OFF b11111111, PWM GEN fully ON duty = 100/255*LSB

PWM_LED_DC

Register name:	PWM_LED_DC
Address:	Global Base Address + 0x0C
Description:	PWM LED duty cicle setting

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
DUTY_CYCLE	RW	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	b00000000, PWM GEN OFF b11111111, PWM GEN fully ON duty = 100/255*LSB

DIAG_OFF_EN

Register name:	DIAG_OFF_EN
Address:	Global Base Address + 0x0D
Description:	OFF Diagnostic enable register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: (default) OFF diagnosis not active 1: OFF diagnosis active

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DIAG_OPL_ON_EN

Register name:	DIAG_OPL_ON_EN
Address:	Global Base Address + 0x0E
Description:	Open Load in ON Diagnostic enable register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RW	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: (default) OL diagnosis not active 1: OL diagnosis active

DIAG_OVC_OVT_RLW

Register name:	DIAG_OVC_OVT_RLW
Address:	Global Base Address + 0x0F
Description:	Overcurrent/overtemperature error Clear on write

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	WO	0	8	0x00	POR_N, NRES pin, CFG_1.RST bit, VDD_UV	Channel [7:0], MSB refers to channel 7 0: (default) clear on write not active 1: clear on write active

STA_0

Register name:	STA_0
Address:	Global Base Address + 0x10
Description:	Status Register 0

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
NU	RO	7	1	0x00	X	-
DIS	RO	6	1	0x00	POR_N	Echo status of DIS input (if properly configured)
X	-	5	1	X	X	-
IDLE	RO	4	1	0x00	POR_N	Echo status of IDLE input
IN1	RO	3	1	0x00	POR_N	Echo status of IN1 input
IN0	RO	2	1	0x00	POR_N	Echo status of IN0 input
OUT_ON_ERR	RLR	1	1	0x00	POR_N	0: normal 1: overcurr/overtemp detected on a whatever channel
OUT_OFF_ERR	RLR	0	1	0x00	POR_N	0: normal 1: OFF state diag fail on whatever channel

STA_1

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Register name:	STA_1
Address:	Global Base Address + 0x11
Description:	Status Register 1

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
NU	RO	5	3	0x00	X	-
POR	RLR	4	1	0x00	POR_N	0: POR condition not detected 1: POR condition detected
VDDIO_UV	RLR	3	1	0x00	POR_N	0: no VDDIO undervoltage 1: VDDIO undevoltage detected
VBATT_UV	RLR	2	1	0x00	POR_N	0: no VBATT undervoltage 1: VBATT undevoltage detected
MODE	RO	0	2	0x00	POR_N	IC operating mode 00: Sleep Mode 01: Limp Home Mode 10: Idle Mode 11: Active Mode

DIAG_OVC_OVT

Register name:	DIAG_OVC_OVT
Address:	Global Base Address + 0x12
Description:	Overcurrent/overtemperature detection Register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RLW	0	8	0x00	POR_N	Channel [7:0], MSB refers to channel 7 0: (default) no fail 1: overcurr/overtemp detected

DIAG_OPL_OFF

Register name:	DIAG_OPL_OFF
Address:	Global Base Address + 0x13
Description:	Driver Open load detection in off state Register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RLR	0	8	0x00	POR_N	Channel [7:0], MSB refers to channel 7 0: (default) no fail 1: open load detected

DIAG_OPL_ON

Register name:	DIAG_OPL_ON

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Address:	Global Base Address + 0x14
Description:	Driver Open load detection in on state Register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RLR	0	8	0x00	POR_N	Channel [7:0], MSB refers to channel 7 0: (default) no fail 1: open load detected

DIAG_SHG

Register name:	DIAG_SHG
Address:	Global Base Address + 0x15
Description:	Driver shorted load detection in OFF state Register

Field name	Type	Bit Offset	Bit Width	Reset Value	Reset Sources	Description
OUTn	RLR	0	8	0x00	POR_N	Channel [7:0], MSB refers to channel 7 0: (default) no fail 1: STG/STB detected

Note: Global Base Address to be considered as 0x00

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12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

12.1 VFQFPN32 (5x5x1 mm exp. pad down 3.5x3.5) package information

Figure 23. **VFQFPN32 (5x5x1 mm exp. pad down 3.5x3.5) package outline**

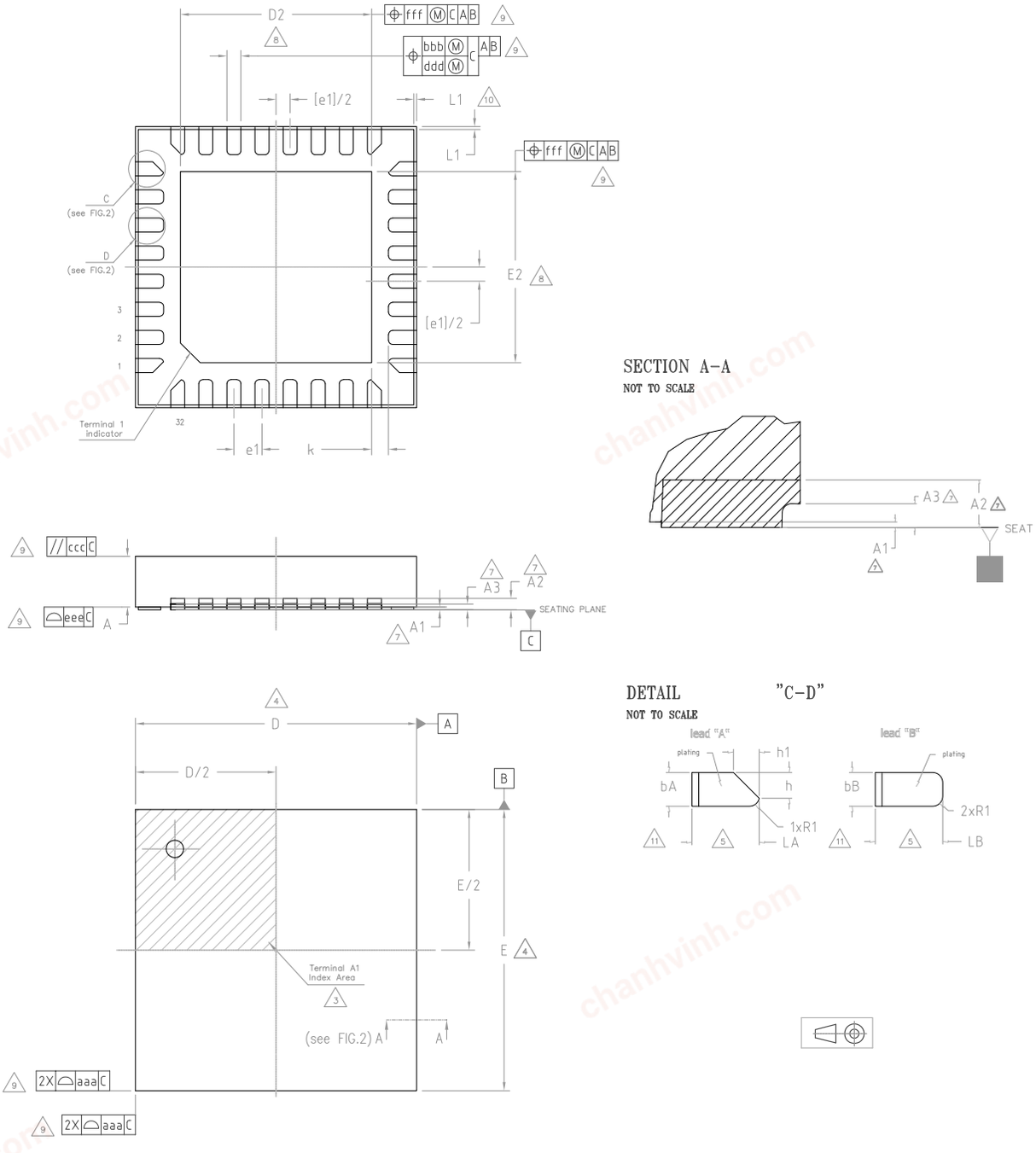

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Table 19. **VFQFPN32 (5x5x1 mm exp. pad down 3.5x3.5) mechanical data**

Symbol	Dimensions			Note
	Min	Typ	Max	
A	0.80	0.90	1.00	
A1	0.00	-	0.05	
A2		0.2 REF		
A3	0.1	-	-	
D		5.00 BSC		4
D2	3.40	3.50	3.60	8
E		5.00 BSC		4
E2	3.40	3.50	3.60	8
e1		0.5 BSC		
k	0.20	-	-	
L1	-	-	0.05	10
La	0.40	0.50	0.60	11
bA	0.20	0.25	0.30	11
h		0.19 REF		11
h1		0.19 REF		11
LB	0.45	0.50	0.55	11
bB	0.20	0.25	0.30	11
N		32		6
R1	-	-	0.1	
Tolerance of form and position				
aaa		0.15		1, 2
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
fff		0.10		

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Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. All Dimensions are in millimeters.
3. Terminal A1 identifier and terminal numbering convention shall conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded, or metalized feature. Optional indicator on bottom surface may be a molded, marked or metallized feature.
4. Outlines with “D” and “E” increments less than 0.5 mm should be registered as “stand alone” outlines. These outlines should use as many of the algorithms and dimensions states in the design standard as possible to insure predictability in manufacturing.
5. Inner edge of corner terminals may be chamfered or rounded in order to achieve minimum gap “k”. This feature should not affect the terminal width “b”, which is measured L/2 from the edge of the package body.
6. “N” is the maximum number of terminal positions for the specified body size. Depopulation is allowed, but only under the following conditions.
   – Depopulation scheme must be consistent in each quadrant of the package.
   – Non-symmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics.
7. A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).
8. Dimension D2 and E2 refer to exposed pad.
9. For Tolerance of Form and Position see Table 19.
10. Critical dimensions: 10.1 L1
11. Dimensions “b” and “L” are measured at terminal plating surface.
12. For Symbols, Recommended Values and Tolerances see Table below: (ACCORDING TO PACKAGE OR JEDEC SPEC IF REGISTERED)

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12.2 HTSSOP24 (7.8x6.4x1 mm exp. pad down 5.0x3.2) package information

Figure 24. **HTSSOP24 (7.8x6.4x1 mm exp. pad down 5.0x3.2) package outline**

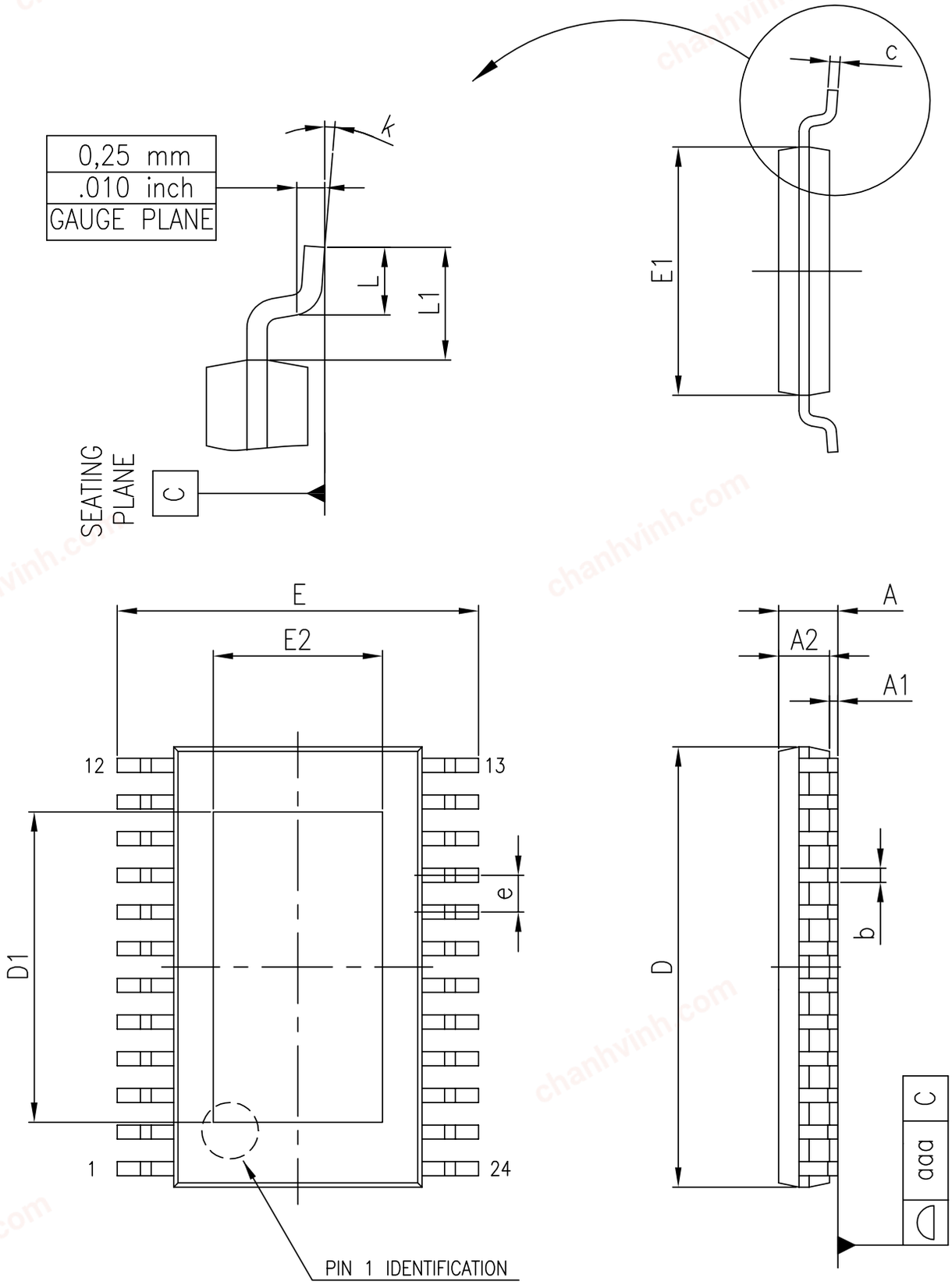

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Table 20. **HTSSOP24 (7.8x4.4x1.1 mm exp. pad down 5.0x3.2) mechanical data**

Symbol	Dimensions			Note
	Min	Typ	Max	
A	1.05	1.10	1.20	1
A1	0.05	-	0.15	
A2	0.80	1.00	1.2	
b	0.19	-	0.30	
D	7.70	7.80	7.90	
D1	4.80	5.00	5.20	
E	6.20	6.40	6.60	
E1	4.30	4.40	4.50	2
E2	3.00	3.20	3.40	
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	-	1.00	-	
K	0	-	8	Degrees
aaa	-	-	0.15	

Notes:

1. Very thin: 0.80 < A ≤ 1.00 mm / Fine pitch: e < 1.00mm
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

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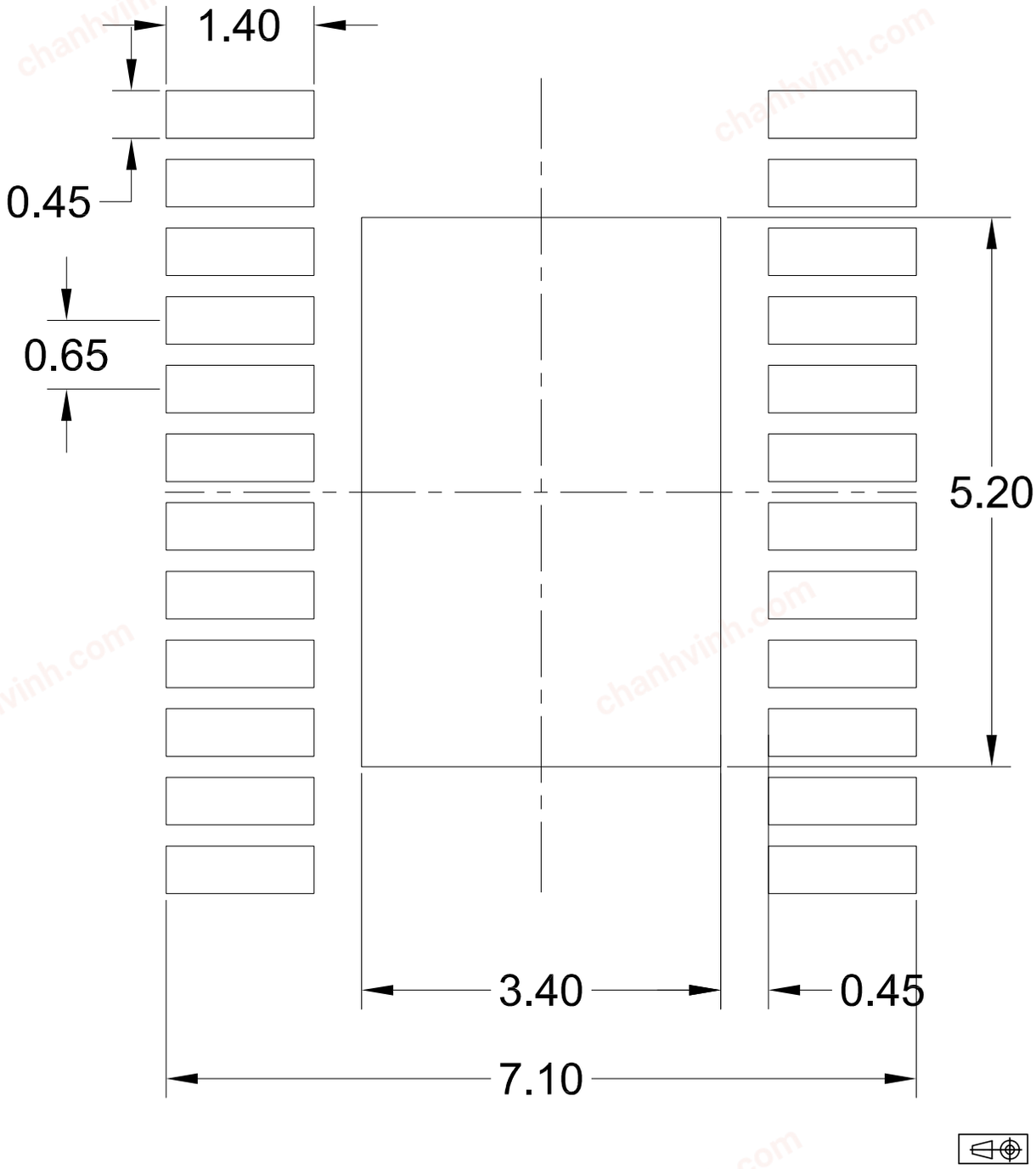
Figure 25. HTSSOP24 (7.8x4.4x1.1 mm exp. pad down 5.0x3.2) recommended footprint



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13 Errata

This chapter is intended to integrate the information provided in the L9026 product datasheet, in order to facilitate the correct usage of the product.

Table 21. Errata

#	Silicon	Function	Issue description
1	L9026BB	OFF state diagnostic	OFF state diagnostic for HS configured channels shall be invoked only after t_{OFF1HS} is elapsed since last channel switch ON command. A violation of this constraint may lead to a spurious overcurrent detection and then to a shut-OFF of channels previously enabled.

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Revision history

Table 22. **Document revision history**

Date	Version	Changes
06-Aug-2020	1	Initial release.
30-Sep-2020	2	Updated: • Order Code in Product summary; • Table 4. Absolute maximum rating capability; • Table 5. Temperature range; • Table 8. VBATT electrical performance; • Table 9. Functions availability in different supply conditions; • Table 16. Over temperature and over load electrical parameters; • Table 17. Output status and open load ON electrical parameters; • Table 18. SPI electrical parameters. Minor text changes.
09-Oct-2020	3	Added Section 13 Errata.
10-Nov-2020	4	Removed watermark "Restricted".

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