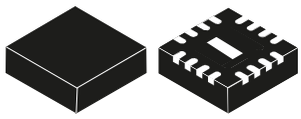
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L6983

Datasheet

38 V, 3 A synchronous step-down converter with 17 µA quiescent current



QFN16 (3 x 3 mm)

Maturity status link
L6983

Features

- 3.5 V to 38 V operating input voltage
- Output voltage from 0.85 V to V_{IN}
- 3.3 V and 5 V fixed output voltage versions
- 3 A DC output current
- 17 µA operating quiescent current
- Internal compensation network
- Two different versions: LCM for high efficiency at light loads and LNM for noise sensitive applications
- 2 µA shutdown current
- Internal soft-start
- Enable
- Overvoltage protection
- Output voltage sequencing
- Thermal protection
- 200 kHz to 2.2 MHz programmable switching frequency. Stable with low ESR capacitor
- Optional spread spectrum for improved EMC
- Power Good
- Synchronization to external clock for LNM devices
- QFN16 package

Applications

- Designed for 24 V buses industrial power systems
- 24 V battery powered equipment
- Decentralized intelligent nodes
- Sensors and always-on applications
- Low noise applications

Description

The L6983 is an easy to use synchronous monolithic step-down regulator capable of delivering up to 3 A DC to the load. The wide input voltage range makes the device suitable for a broad range of applications. The L6983 is based on a peak current mode architecture and is packaged in a QFN16 3x3 with internal compensation thus minimizing design complexity and size.

The L6983 is available both in low consumption mode (LCM) and low noise mode (LNM) versions. LCM maximizes the efficiency at light-load with controlled output voltage ripple so the device is suitable for battery-powered applications. LNM makes the switching frequency constant and minimizes the output voltage ripple for light load operations, meeting the specification for low noise sensitive applications. The L6983 allows the switching frequency to be selected in the 200 Hz - 2.2 MHz range with optional spread spectrum for improved EMC.

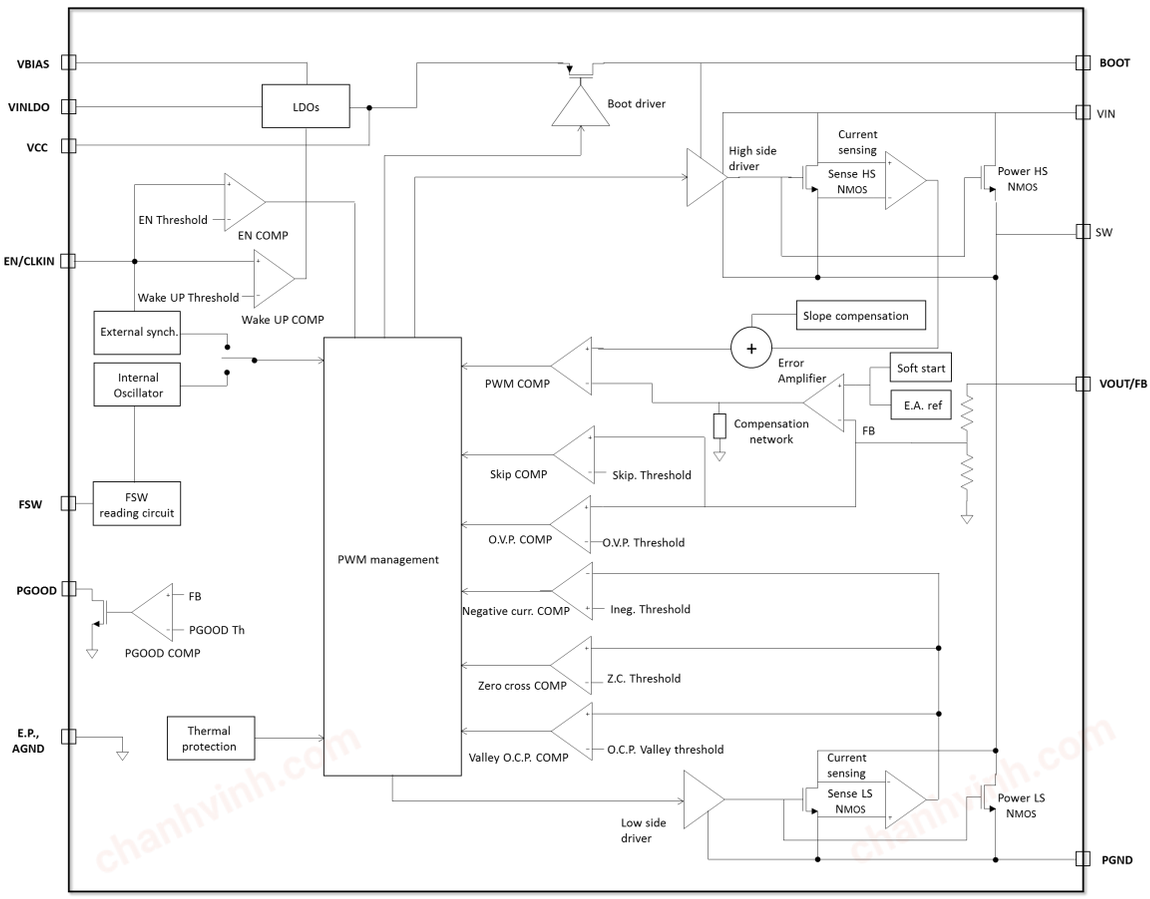
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The EN pin provides enable/disable function. The typical shutdown current is 2 µA when disabled. As soon as the EN pin is pulled up, the device is enabled and the internal 1.3 ms soft-start takes place. The L6983 features Power Good open collector that monitors the FB voltage. Pulse-by-pulse current sensing on both power elements implements an effective constant current protection and thermal shutdown prevents thermal run-away.

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1 Diagram

Figure 1. **Block diagram**



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2 Pin configuration

Figure 2. **Pin connection (top through view)**

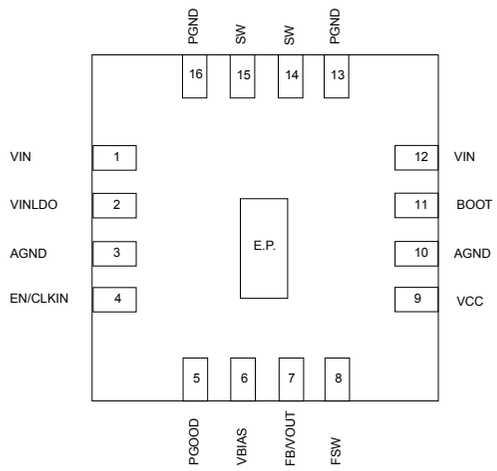


Table 1. **Pin description**

Pin	Symbol	Function
1	VIN	DC input voltage.
2	VINLDO	DC input voltage connected to the supply rail with a simple RC filter.
3	AGND	Analog ground.
4	EN / CLKIN	Enable pin with internal voltage divider. Pull-down/up to disable/ enable the device. In LNM versions, this pin is also used to provide an external clock signal, which synchronizes the device.
5	PGOOD	The PGOOD open collector output is driven to low impedance when the output voltage is out of regulation and released once the output voltage becomes valid.
6	VBIAS	Typically connected to the regulated output voltage, an external voltage source can be used to supply part of the analog circuitry to reduce current consumptions at light load. Connect it to AGND if not used.
7	FB/VOUT	This pin operates as VOUT or FB according to the selected part number. In fixed output voltage versions, VOUT is the output voltage sensing with selected internal voltage divider. In adjustable versions, FB is output voltage sensing with eternal voltage divider.
8	FSW	Connect an external resistor to program the oscillator frequency and enable the optional dithering.
9	VCC	This pin supplies the embedded analog circuitry. Connect a ceramic capacitor (≥ 1 µF) to filter internal voltage reference.
10	AGND	Analog ground.
11	BOOT	Connect an external capacitor (100 nF typ.) between BOOT and SW pins. The gate charge required to drive the internal NMOS is refreshed during the low-side switch conduction time.

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Pin	Symbol	Function
12	VIN	DC input voltage.
13	PGND	Power ground.
14	SW	Switching node.
15	SW	Switching node.
16	PGND	Power ground.
-	Exposed PAD	Exposed pad must be connected to AGND and PGND.

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3 Typical application circuit

Figure 3. Basic application (adjustable version)

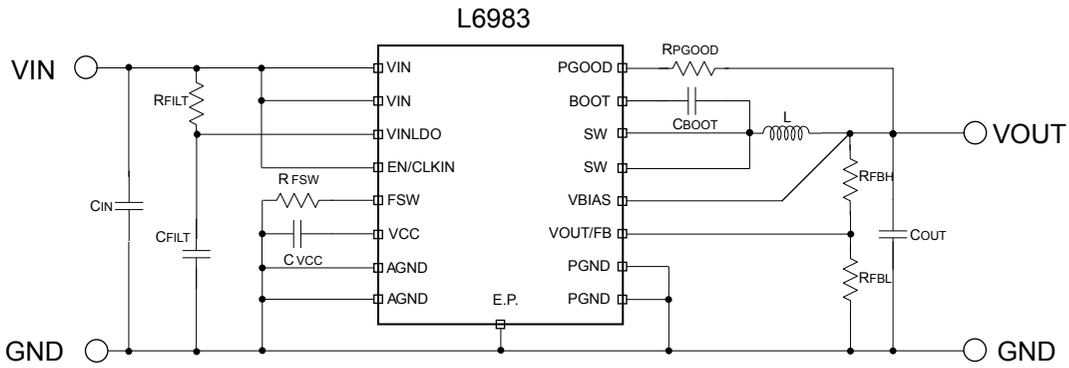


Table 2. Typical application component

Symbol	Value	Description
C_{IN}	10 µF	Input capacitor
R_{FILT}	0.1 kΩ	VINLDO filter resistor
C_{FILT}	1 µF	VINLDO filter capacitor
C_{VCC}	1 µF	VCC bypass capacitor
C_{BOOT}	100 nF	Bootstrap capacitor
C_{OUT}	40 µF	Output capacitor
R_{FBH}	400 kΩ	VOUT divider upper resistor
R_{FBL}	82 kΩ	VOUT divider lower resistor
L	4.7 µH (F_{SW} = 1 MHz)	Output inductor
R_{PGOOD}	1 MΩ	PGOOD resistor
R_{FSW}	10 kΩ	FSW setting resistor

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4 Absolute maximum ratings

Stressing the device above the rating listed in Section 4 Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VIN	Maximum pin voltage	- 0.3	42	V
AGND	Maximum pin voltage	0	0	V
PGND	Maximum pin voltage	- 0.3	0.3	V
BOOT	Maximum pin voltage	SW - 0.3	SW + 4	V
VCC	Maximum pin voltage	- 0.3	Min. (VIN + 0.3 V; 4 V)	V
VOUT/FB	Maximum pin voltage	- 0.3	8	V
FSW	Maximum pin voltage	- 0.3	VCC + 0.3	V
VBIAS	Maximum pin voltage	- 0.3	VIN + 0.3	V
EN	Maximum pin voltage	- 0.3	VIN + 0.3	V
PGOOD	Maximum pin voltage	- 0.3	VIN + 0.3	V
SW	Maximum pin voltage	- 0.85	VIN + 0.3	V
		- 3.8 for 0.5 ns (1)		V
IHS, ILS	High-side / Low-side RMS switch current		3	A
T_J	Operating temperature range	- 40	150	°C
TSTG	Storage temperature range	- 65	150	°C
TLEAD	Lead temperature (soldering 10 sec.)		260	°C

1. *Negative peak voltage during switching activities caused by parasitic layout elements.*

4.1 ESD protection

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM non-corner pins	500	V

4.2 Thermal characteristics

Table 5. Thermal data

Symbol	Parameter	Package	Value	Unit
R_{th_JA}	Thermal resistance junction ambient (device soldered on the STMicroelectronics demonstration board, please refer to Section 9 Application board)	QFN16	30	°C/W

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5 Electrical characteristics

T_J = 25 °C, V_{IN} = 24 V unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		3.5		38	V
V_{IN_H}	V_{CC} rising threshold		2.3		3.3	V
V_{IN_L}	V_{CC} UVLO falling threshold		2.15		3.15	V
I_{PK} (1)	Peak current limit	No slope contribution	4.1	4.6		A
		Full slope contribution	3.1	3.6		A
I_{VY}	Valley current limit		3.3	3.9	4.5	A
I_{SKIP} (1) (2)	Skip current limit			0.6		A
I_{VY_SINK} (1)	Reverse current limit	LNM or VOUT overvoltage	1.25	1.5	1.75	A
R_{DSON_HS}	High-side RDSON			0.130		Ω
R_{DSON_LS}	Low-side RDSON			0.85		Ω
T_{OFF_MIN}	Minimum off-time			200		ns
T_{ON_MIN}	Minimum on-time			75		ns
Enable						
V_{WAKE_UP}	Wake-up threshold	Rising			0.7	V
		Falling	0.2			V
V_{EN}	Enable threshold	Rising	1.08	1.2	1.32	V
		Hysteresis		0.2		V
VCC regulator						
V_{CC}	LDO output voltage		3.0	3.3	3.6	V
Power consumption						
I_{SHTDWN}	Shutdown current from V_{IN}	VEN = GND		2	3	µA
LCM device						
I_{Q_VIN}	Quiescent current from V_{IN}	VBIAS = GND	20	35	60	µA
		VBIAS = 5 V	1	3.5	6	µA
I_{Q_VBIAS}	Quiescent current from V_{BIAS}	VBIAS = 5 V	20	35	60	µA
LNM device						
I_{Q_VIN}	Quiescent current from V_{IN}	VBIAS = GND	1.6	2.3	3	mA
		VBIAS = 5 V	300	550	800	µA
I_{Q_VBIAS}	Quiescent current from V_{BIAS}	VBIAS = 5 V	1.3	1.8	2.3	mA
Soft-start						

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{SS}	Internal soft-start		1	1.3	1.6	ms
Error amplifier						
V_{FB}	Voltage feedback	Adjustable version T_J = 25 °C	0.845	0.85	0.855	V
		Adjustable version T_J = - 40 °C ≤ T_J ≤ 125 ° (4)	0.842	0.85	0.858	V
		Fixed 3.3 V version T_J = 25 °C	3.27	3.3	3.33	V
		Fixed 3.3 V version T_J = -40 °C ≤ T_J ≤ 125 °C (4)	3.284	3.3	3.346	V
		Fixed 5.0 V version T_J = 25 °C	4.955	5.0	5.045	V
		Fixed 5.0 V version T_J = -40 °C ≤ T_J ≤ 125 °C (4)	4.93	5	5.07	V
Overvoltage protection						
V_{OVP}	Overvoltage trip (VOVP/ VREF)		115	120	125	%
V_{OVP_HYST}	Overvoltage hysteresis		1	2	6	%
Synchronization (LNM versions only)						
f_{CLKIN} (3)	Synchronization range		200		2200	kHz
V_{CLKIN_TH} (3)	Amplitude of synchronization clock		2.3			V
V_{CLKIN_T} (3)	Synchronization pulse ON and OFF time 2.3 V ≤ V_{CLKIN_TH} ≤ 2.5 V	V_{CLKIN_TH} = 2.3 V	60			ns
	Synchronization pulse ON and OFF time V_{CLKIN_TH} > 2.5 V		20			ns
Power Good						
V_{THR}	PGOOD threshold	Adjustable output version T_J = -40 °C ≤ T_J ≤ 125 °C (4)	87	90	93	%
		Fixed 3.3 output version T_J = -40 °C ≤ T_J ≤ 125 °C (4)	87	90	93	%
		Fixed 5.0 output version T_J = -40 °C ≤ T_J ≤ 125 °C (4)	87	90	93	%
V_{THR_HYST} (4)	PGOOD hysteresis			3		
V_{PGOOD}	PGOOD open collector output	VIN > VIN_H AND VFB < VTH 4 mA sinking load			0.4	V
		2 < VIN < VIN_H 4 mA sinking load			0.8	V

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{SHDWN} (5)	Thermal shutdown temperature			165		°C
T_{HYS} (5)	Thermal shutdown hysteresis			30		°C

1. *Parameter tested in the static condition during testing phase. The parameter value may change over a dynamic application condition.*
2. *LCM version.*
3. *LNM version.*
4. *Specifications in the - 40 to 125 °C temperature range are assured by characterization and statistical correlation.*
5. *Not tested in production.*

5.1 Frequency selection table

Specification referred to - 40 ≤ T_J ≤ 125 °C and V_{IN} = 24 V, assured by testing at T_J = 25 °C, design, characterization and statistical correlation.

Table 7. FSW selection

Symbol	Option	RVCC (kΩ)	RGND (kΩ)	Min.	Typ.	Max.	Unit
FSW	Dithering (5 % F_{SW} typ.)	1.8	N.C.		200		kHz
		0	N.C.		400		kHz
		3.3	N.C.		500		kHz
		5.6	N.C.		700		kHz
		10	N.C.		1000		kHz
		18	N.C.		1500		kHz
		33	N.C.		2000		kHz
		56	N.C.		2300		kHz
	No dithering	N.C.	1.8		200		kHz
		N.C.	0	360	400	440	kHz
		N.C.	3.3		500		kHz
		N.C.	5.6	630	700	770	kHz
		N.C.	10	900	1000	1100	kHz
		N.C.	18		1500		kHz
		N.C.	33		2000		kHz
		N.C.	56	2000	2300	2600	kHz

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6 Functional description

The L6983 device is based on a “peak current mode" architecture with constant frequency control. Therefore, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

The device features LNM (low noise mode) that is forced PWM control, or LCM (low consumption mode) to increase the efficiency at light-load on the selected part number.

The main internal blocks shown in the block diagram in Figure 1. Block diagram and Figure 2. Pin connection (top through view) are:

- Embedded power elements
- A fully integrated adjustable oscillator which is able to set eight different switching frequencies from 200 to 2200 kHz
- The ramp for the slope compensation avoiding subharmonic instability
- A transconductance error amplifier with integrated compensation network
- The high-side current sense amplifier to sense the inductor current
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start block ramps up the reference voltage on error amplifier thus decreasing the inrush current at power-up. The EN pin inhibits the device when driven low
- The EN/CLK pin section, which, for LNM versions, allows synchronizing the device to an external clock generator
- The pulse-by-pulse high-side / low-side switch current sensing to implement the constant current protection
- A circuit to implement the thermal protection function
- The OVP circuitry to discharge the output capacitor in case of overvoltage event
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the VBIAS pin is connected to an external output voltage
- Enable/ disable dithering operation

6.1 Enable

The EN pin is a digital input that turns the device on or off.

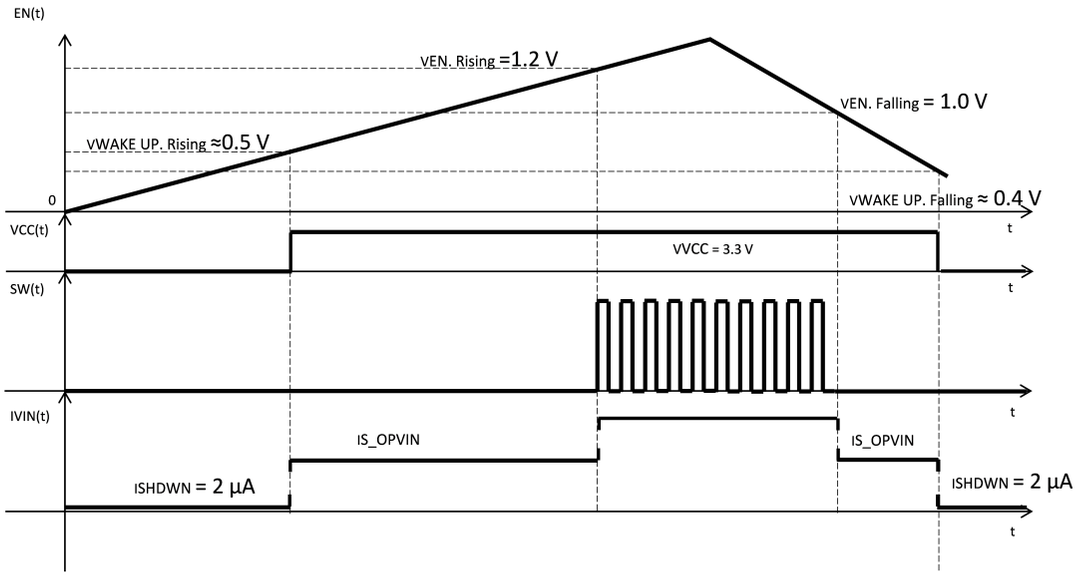
In order to maximize both the EN threshold accuracy and the current consumption, the device implements two different thresholds:

1. The wake-up threshold, V_{WAKE_UP} = 0.5 V (see Table 6. Electrical characteristics)
2. The start-up threshold, V_{EN} = 1.2 V (see Table 6. Electrical characteristics)

The following picture shows the device behavior.

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Figure 4. **Power-up/down behavior**



When the voltage applied on the EN pin rises over $V_{WAKEUP, RISING}$, the device powers up the internal circuit thus increasing the current consumption.

As soon as the voltage rises over the $V_{EN, RISING}$, the device starts the switching activities as described on Section 6.2 Soft-start.

Once the voltage becomes lower than $V_{EN, FALLING}$, the device interrupts the switching activities.

As soon as the voltage becomes lower than $V_{WAKEUP.FALLING}$, the device powers down the internal circuit reducing the current consumption.

The pin is VIN compatible.

Please refer to Table 6. Electrical characteristics for the reported thresholds.

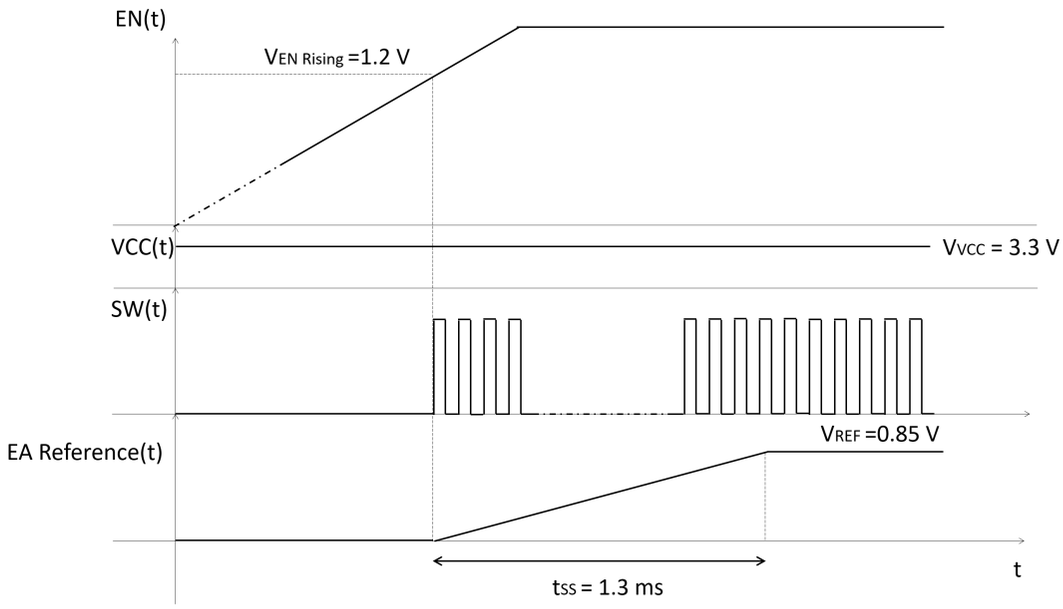
6.2 Soft-start

The soft-start (SS) limits the inrush current surge and makes the output voltage increase monotonically.

The device implements the soft-start phase ramping the internal reference with very small steps. Once the SS ends the error amplifier reference is switched to the internal value of 0.85 V coming directly from the band gap cell.

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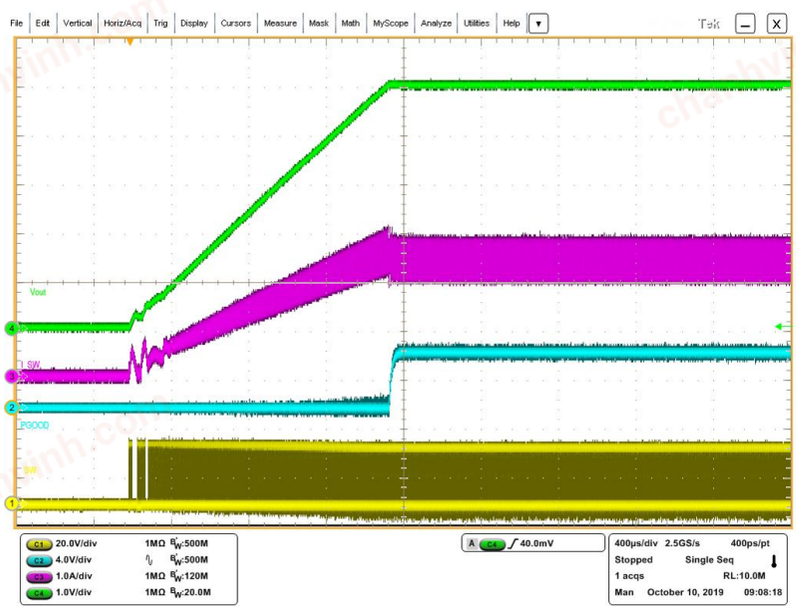
Figure 5. **Soft-start procedure**



During the normal operation, a new soft-start cycle takes place in case of:

1. Thermal shutdown event
2. UVLO event
3. EN pin rising over VEN threshold. Please refer to Table 6. Electrical characteristics

Figure 6. **Soft-start phase with I_{OUT} = 2.5 A**



6.3 Undervoltage lockout

The device implements the undervoltage lockout (UVLO) continuously sensing the voltage on the VCC pin, if the UVLO lasts more than 10 µs, the internal logic resets the device by turning off both LS and HS.

After the reset, if the EN pin is still high, the device repeats the soft-start procedure.

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6.4 Light-load operation

The L6983 implements two different light load strategies:

1. Low consumption mode (LCM)
2. Low noise mode (LNM)

Please refer to Table 12. Order codes to select the part number with the preferred light load strategy.

6.4.1 Low consumption mode (LCM)

The LCM maximizes the efficiency at light load.

When the switch peak current request is lower than the I_{SKIP} threshold (see Table 6. Electrical characteristics), the device regulates V_{OUT} by the skip threshold. The minimum voltage is given by:

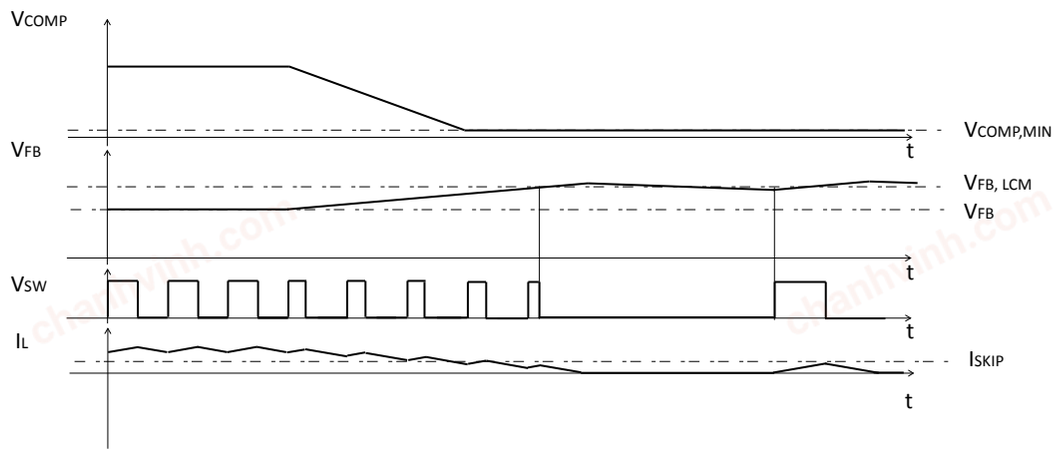
$$V_{OUT,\ LCM} = V_{FB,\ LCM} \cdot \frac{R_{PH} + R_{PL}}{R_{PL}} \quad (1)$$

Where $V_{FB,\ LCM}$ is 1.8% (typ.) higher than V_{FB}.

The device interrupts the switching activities when two conditions happen together:

1. The peak inductor current required is lower than I_{SKIP}
2. The voltage on the FB pin is higher than VFB, LCM

Figure 7. Light load operation



A new switching cycle takes place once the voltage on the FB pin becomes lower than $V_{FB,LCM}$.

The HS switch is kept on until the inductor current reaches I_{SKIP}.

Once the current on the HS reaches the defined value, the device turns the HS off and turns the LS on. The LS is kept enabled until one of the following conditions occurs:

1) The inductor current sensed by the LS becomes equal to zero

2) The switching period ends up

If, at the end of the switching cycle, the voltage on the FB pin rises over the $V_{FB,LCM}$ threshold, the LS is kept enabled until the inductor current becomes equal to zero. Otherwise, the device turns on again the HS and starts a new switching pulse.

During the burst pulse, if the energy transferred to COUT increases the VFB level over the threshold defined on Eq. (1), the device interrupts the switching activities. The new cycle takes place only when VFB becomes lower than the defined threshold. Otherwise, as soon as the LS is turned off the HS is turned on.

Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

$$V_{OUT\ RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^{T_{BURST}} I_L(t)\,dt}{C_{OUT}} \quad (2)$$

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Figure 8. LCM operation with I_{SKIP} = 600 mA typ. at zero load. L = 15 µH; C_{OUT} = 40 µF

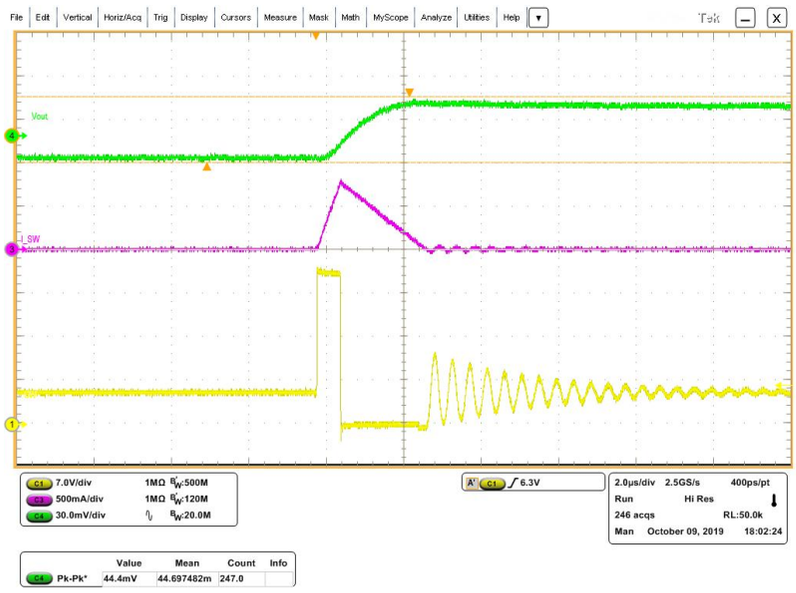
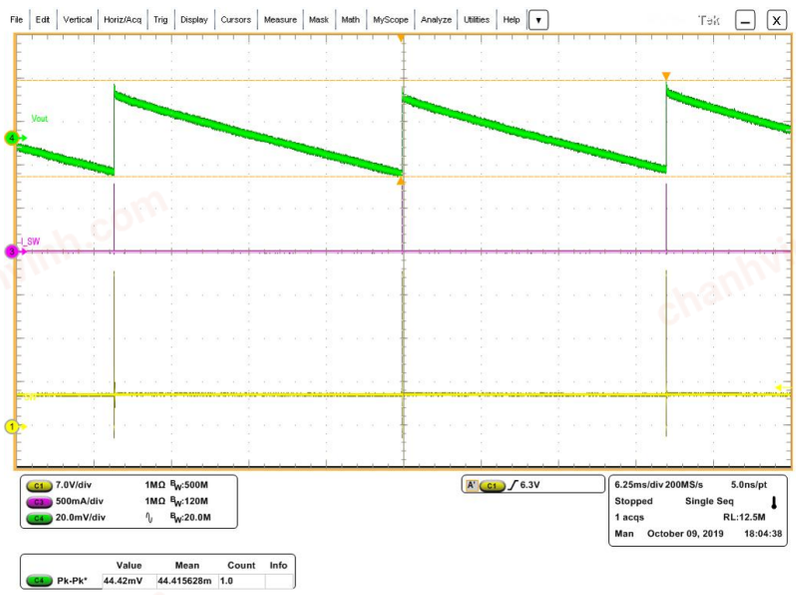


Figure 9. LCM operation over loading condition (part 1-pulse skipping)



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Figure 10. **LCM operation over loading condition (part 2-pulse skipping)**

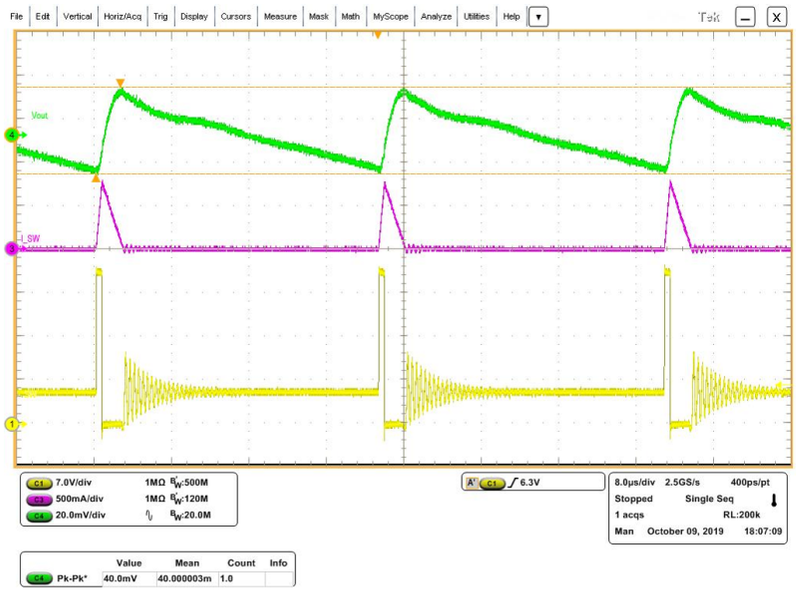
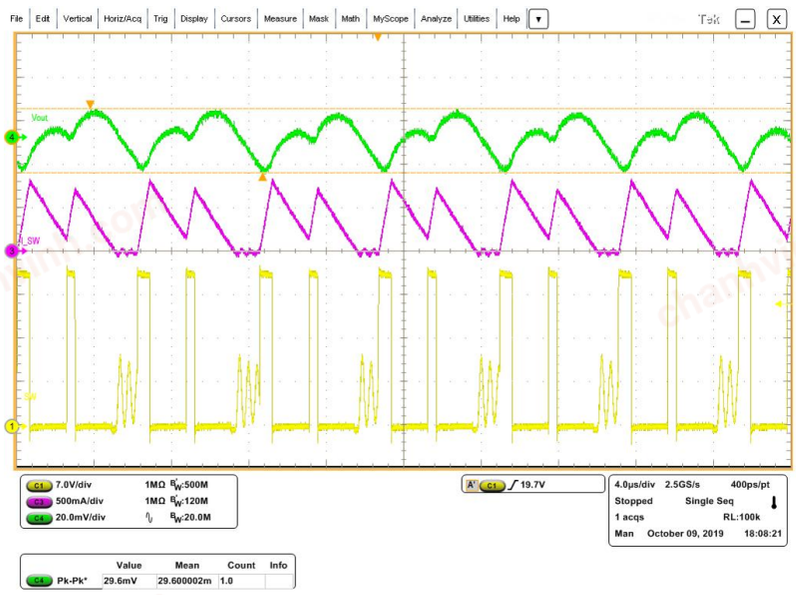
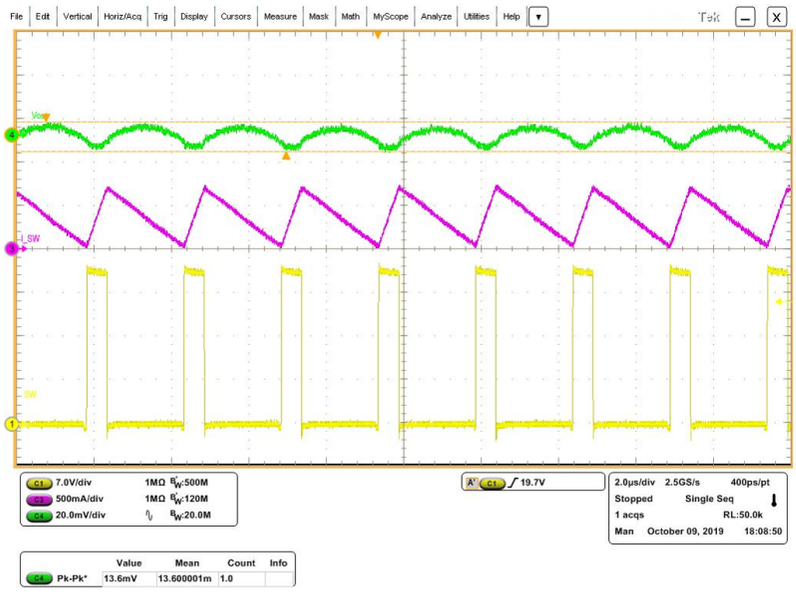


Figure 11. **LCM operation over loading condition (part 3-pulse skipping)**



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Figure 12. **LCM operation over loading condition (part 4-CCM)**



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6.4.2 Low noise mode (LNM)

The low noise mode implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed VIN.

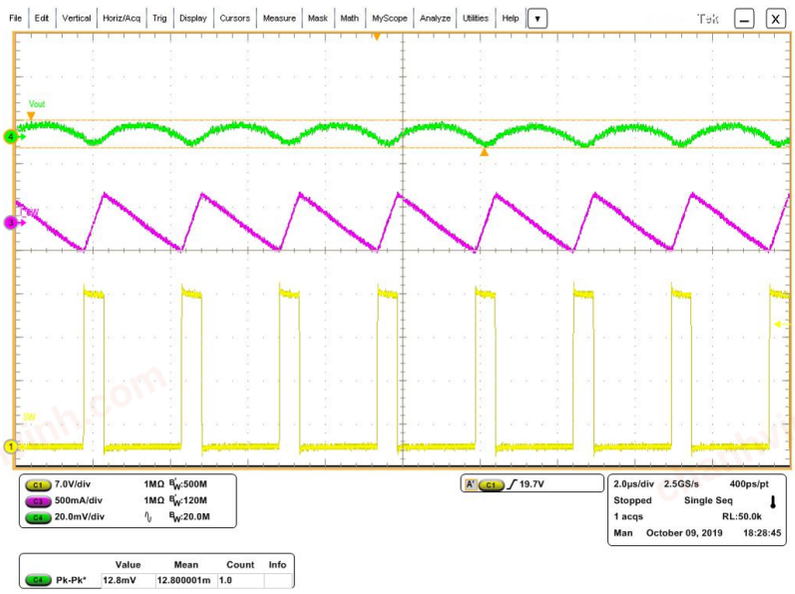
The regulator in steady loading condition operates in continuous conduction mode (CCM) over the different loading conditions.

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). Consequently, the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

$$V_{OUT\ RIPPLE} = ESR \cdot \Delta I_{LMAX} + \frac{\Delta I_{LMAX}}{8 \cdot C_{OUT} \cdot f_{SW}} \quad (3)$$

Usually the resistive component of the ripple can be neglected if the selected output capacitor is a multi-layer ceramic capacitor (MLCC).

Figure 13. Low noise mode operation at zero load



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6.4.3 Efficiency for low consumption mode and low noise mode part number

Figure 14. Light-load efficiency for low consumption mode and low noise mode - linear scale, and Figure 15. Light-load efficiency for low consumption mode and low noise mode - log scale report the efficiency measurements to highlight the gap at the light-load between LNM and LCM part numbers. The graph reports also exactly the same efficiency at the medium / high load.

Figure 14. Light-load efficiency for low consumption mode and low noise mode - linear scale

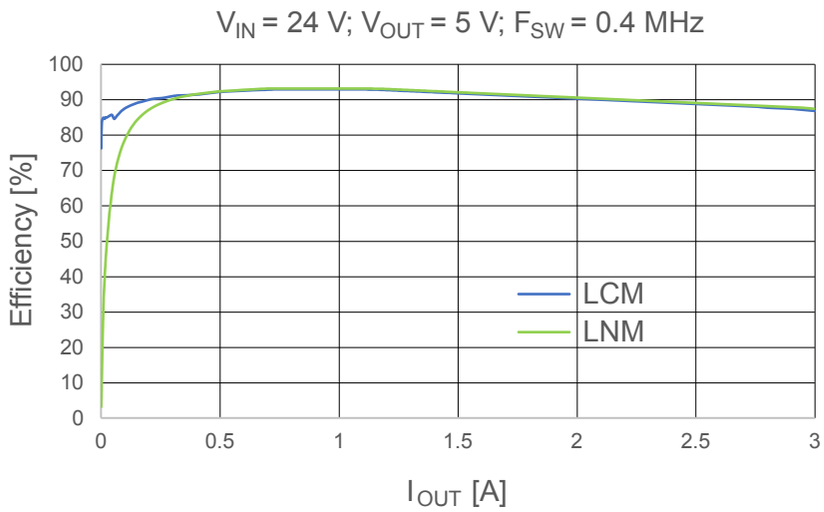
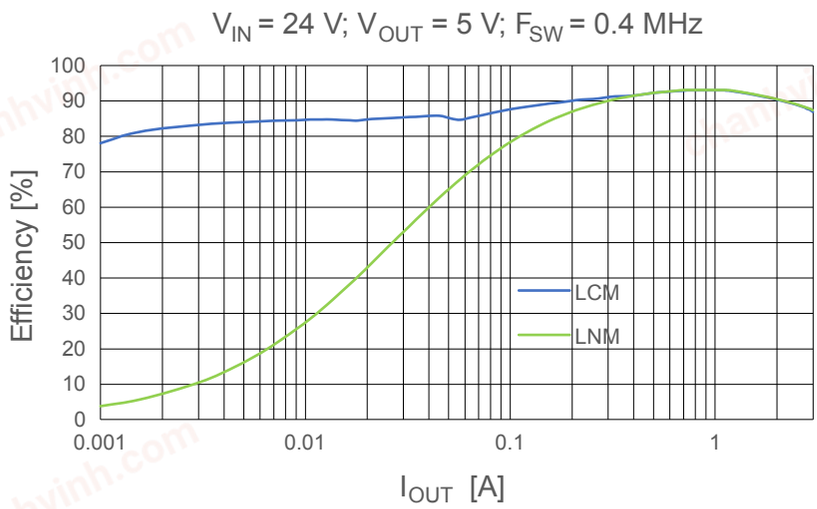


Figure 15. Light-load efficiency for low consumption mode and low noise mode - log scale



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6.4.4 Load regulation for low consumption mode and Low noise mode part number

Figure 16. Load regulation for LCM and LNM. V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 400 kHz - linear scale and Figure 17. Load regulation for low noise mode. V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 400 kHz - log scale report the load regulation to highlight the gap, given by the different regulation strategy, at the light-load between LNM and LCM part numbers. When the required I_{OUT} is higher than the threshold defined on the Section 6.4.1 Low consumption mode (LCM) the behavior of the different part number is exactly the same.

Figure 16. Load regulation for LCM and LNM. V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 400 kHz - linear scale

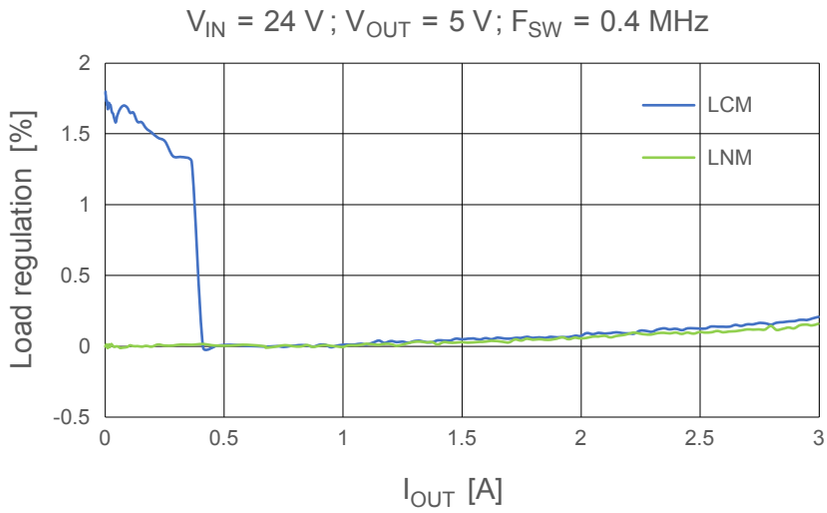
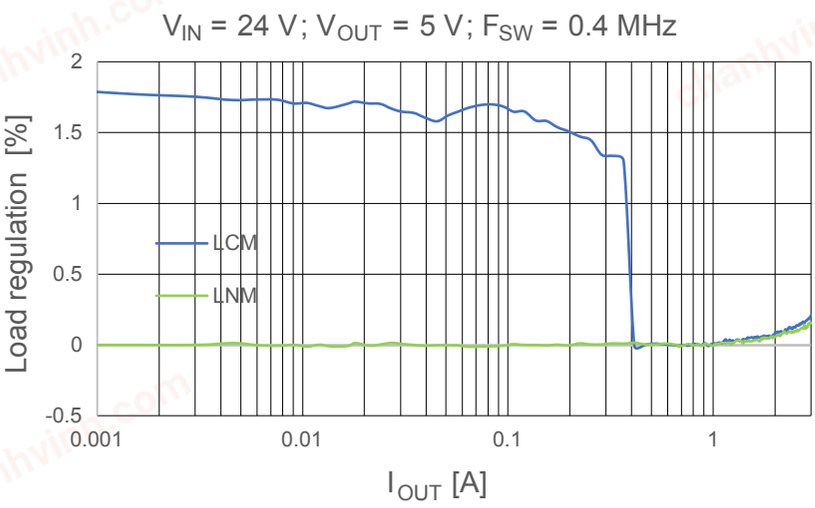


Figure 17. Load regulation for low noise mode. V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 400 kHz - log scale

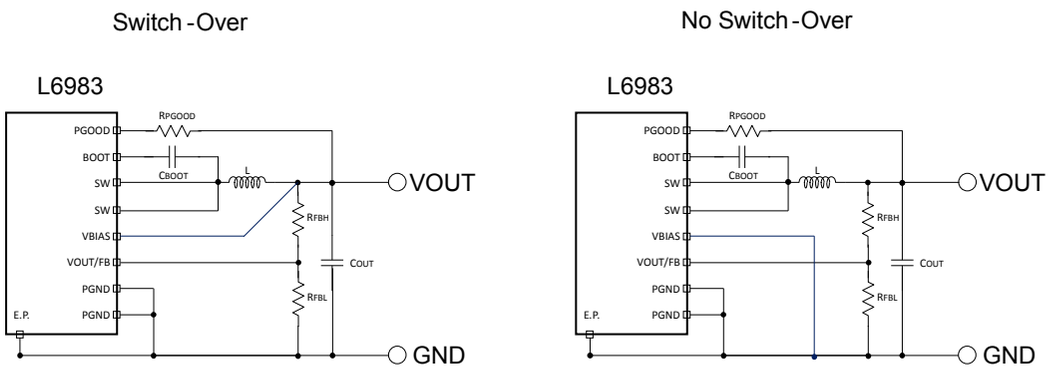


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6.5 Switch-over feature

The switch-over maximizes the efficiency at light load that is crucial for low consumption application.

Figure 18. Switch-over



In order to minimize the regulator quiescent current sink from the input voltage, the VBIAS pin can be connected to an external voltage source in the range of 3 V < VBIAS < VIN.

In case the VBIAS pin is connected to the regulated output voltage (VOUT), the total current drawn from the input voltage is given by the following equation:

$$I_{QVIN} = I_{QOPVIN} + \frac{1}{\eta_{L6983}} \cdot \frac{V_{BIAS}}{V_{IN}} \cdot I_{QOPVBIAS} \quad (4)$$

6.6 Spread spectrum

The spread spectrum is selectable by connecting the RFSW resistor to VCC (please refer to Table 7. FSW selection). The internal dithering circuit changes the switching frequency in a range of ± 5%.

$$\Delta F_{SW} = 5\% \cdot F_{sw} \quad (5)$$

The device updates the frequency every clock period by fixed steps:

- Ramps up in 63 steps from minimum to maximum FSW
- Ramps down in 63 steps from maximum to minimum FSW

The modulation shape is almost triangular with a frequency of:

$$F_{Dithering} = \frac{F_{sw}}{126} \quad (6)$$

6.7 Overvoltage protection

The overvoltage protection monitors the FB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% (typ.) over the nominal value.

This is a second level protection and it should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should guarantee an output voltage regulation within the overvoltage threshold even during the worst-case scenario in term of load transitions.

The protection is reliable and able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. Consequently, the output voltage regulation would be affected.

The L6983 device implements a 1.5 A (I_{VY_SINK} refer to Table 6. Electrical characteristics) negative current limitation to limit the maximum reversed switch current during the overvoltage operation.

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6.8 Overcurrent protection

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (please refer to Table 6. Electrical characteristics) in overcurrent condition.

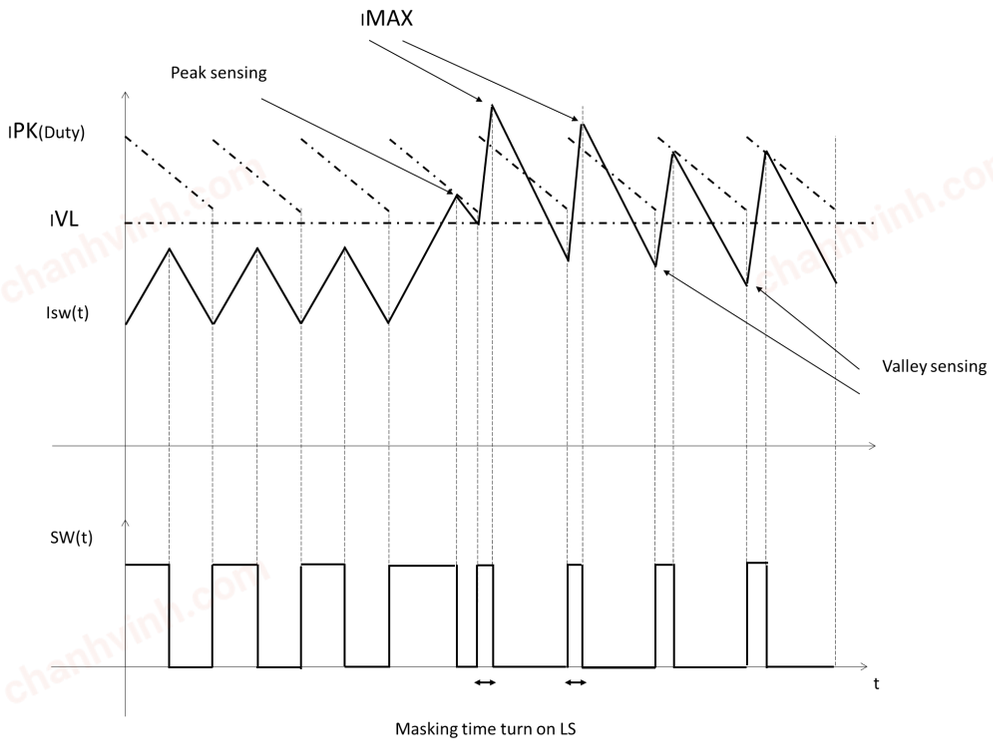
The L6983 device implements a pulse-by-pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak” the low-side sensing “valley”.

The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. Therefore, the peak current protection is disabled for a masking time after the high-side switch is turned on. The masking time for the valley sensing is activated after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, the valley current protection at extremely high duty cycles.

The L6983 device assures an effective overcurrent protection sensing the current flowing in both power elements. In case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits assure the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. The low-side operation is able to prevent the high-side turn on, so the device can skip pulses decreasing the switching frequency.

Figure 19. Over current protection behavior



In worst case scenario, reported in Figure 19. Over current protection behavior of the overcurrent protection the switch current is limited to:

$$I_{MAX} = I_{VY} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{MASKHS} \quad (7)$$

Where IVY is the current threshold of the valley sensing circuitry (please refer to Table 6. Electrical characteristics) and T_{MASKHS} is the masking time of the high-side switch (75 ns typ.).

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In most of the overcurrent conditions, the conduction time of the high-side switch is higher than the masking time and so the peak current protection limits the switch current.

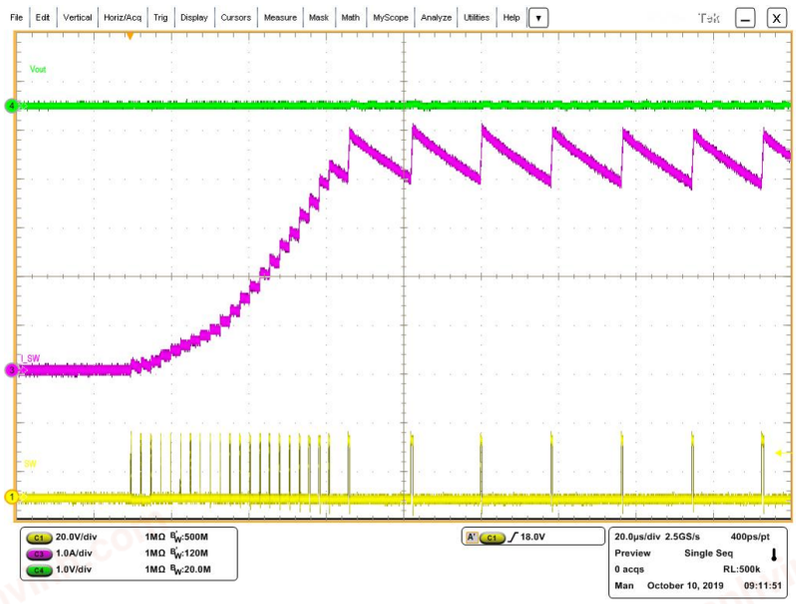
$$I_{MAX} = I_{PK} \tag{8}$$

The DC current flowing in the load in overcurrent condition is:

$$I_{DCOUT} = I_{MAX} - \frac{I_{RIPPLE}(V_{OUT})}{2} = I_{MAX} - \left(\frac{V_{IN} - V_{OUT}}{2 \cdot L} \cdot T_{ON}\right) \tag{9}$$

The Figure 20. Soft-start procedure with V_{OUT} shorted to GND shows the L6983 soft-start procedure with V_{OUT} shorted to GND.

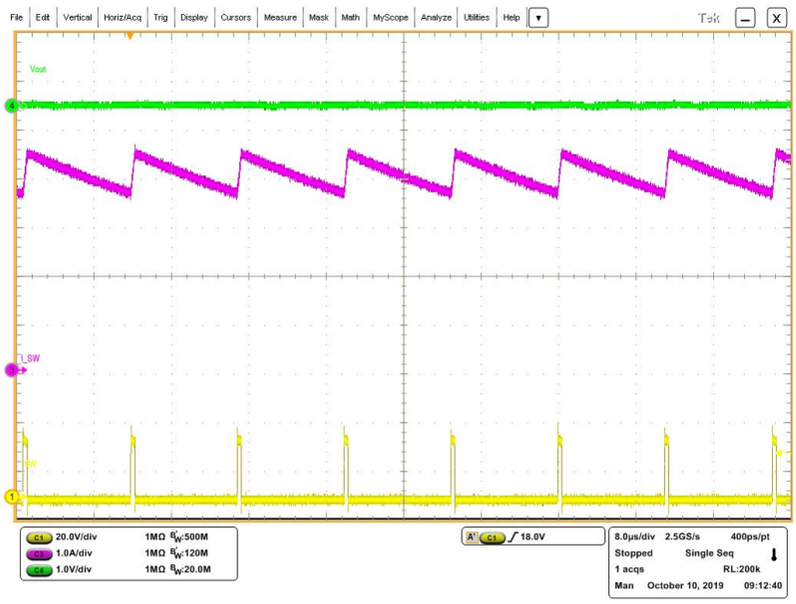
Figure 20. Soft-start procedure with V_{OUT} shorted to GND



The Figure 21. Over current procedure with persistent short circuit between V_{OUT} and GND shows the L6983 over current protection with a persistent short circuit between V_{OUT} and GND.

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Figure 21. **Over current procedure with persistent short circuit between V_{OUT} and GND**



6.9 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (T_{SHDWN} refer to Table 6. Electrical characteristics). The thermal sensing element is close to the power elements, assuring fast and accurate temperature detection. A hysteresis of approximately 30 °C prevents the device from turning ON and OFF too fast. After a thermal protection event is expired, the L6983 restarts with a new soft-start.

6.10 Power Good

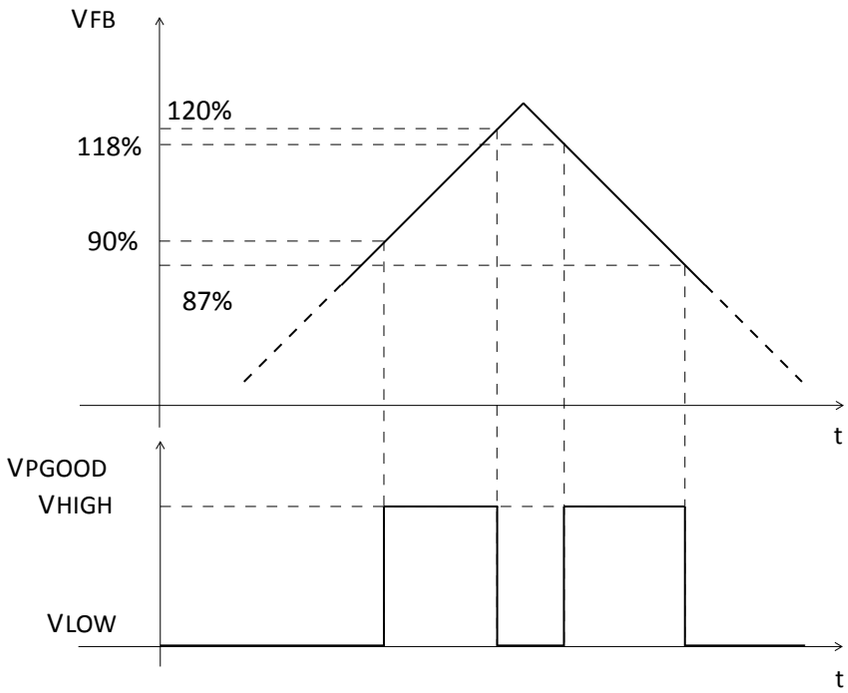
The PGOOD pin indicates whether the output voltage is within its regulation level. The pin output is an open drain MOSFET. The PG is pulled low when:

1. The FB pin voltage is lower than 90% (typ.) of the nominal internal reference for more than 10 µs
2. The FB pin voltage is higher than 120% (typ.) of the nominal internal reference for more than 10 µs (see Section 6.7 Overvoltage protection)
3. During the soft-start procedure also with pre-charged VOUT
4. If a thermal shutdown event occurs
5. If a UVLO event occurs

The PG pin is VIN compatible.

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Figure 22. **PGOOD thresholds**

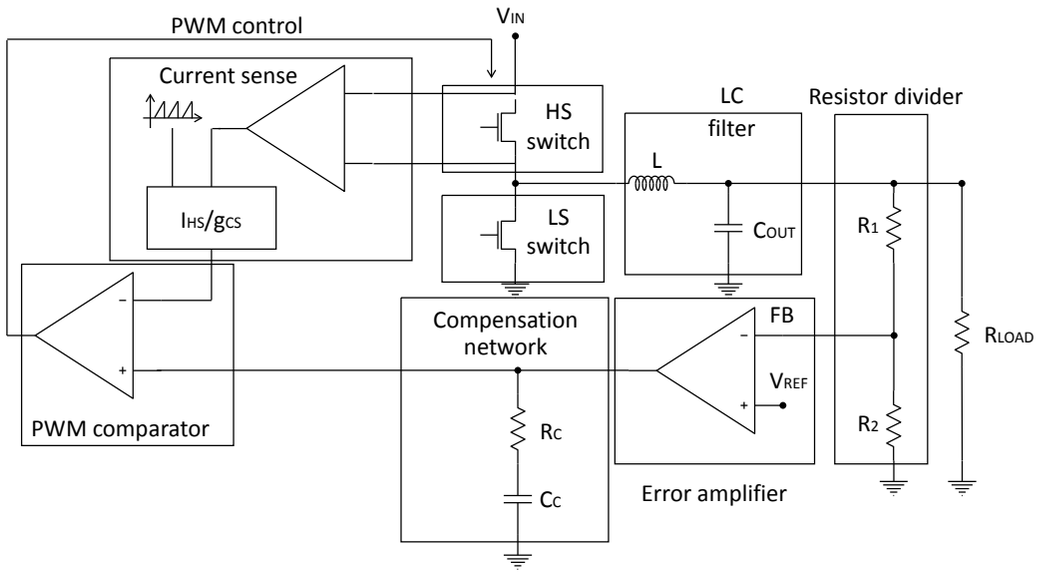


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7 Closing the loop

The following picture shows the typical compensation network required to stabilize the system.

Figure 23. Block diagram of the loop



7.1 GCO(s) control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as follows:

$$G_{CO}(s) = R_{LOAD} \cdot g_{CS} \cdot \frac{1}{1 + \frac{R_{LOAD} \cdot T_{SW}}{L} \cdot [m_C \cdot (1-D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \cdot F_H\left(s\right) \quad (10)$$

Where R_{LOAD} represents the load resistance, the g_{CS} equivalent sensing trans-conductance of the current sense circuitry, ω_P the single pole introduced by the power stage and the ω_Z zero given by the ESR of the output capacitor. $F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}} \quad (11)$$

$$\omega_P = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1-D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}} \quad (12)$$

where:

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = I_{SLOPE} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases} \quad (13)$$

Where I_{SLOPE} is equal to 1 A.

S_n represents the on-time slope of the sensed inductor current, S_e the on-time slope of the external ramp that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution F_H (s) is:

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$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = I_{SLOPE} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases} \quad (14)$$

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}} \quad (15)$$

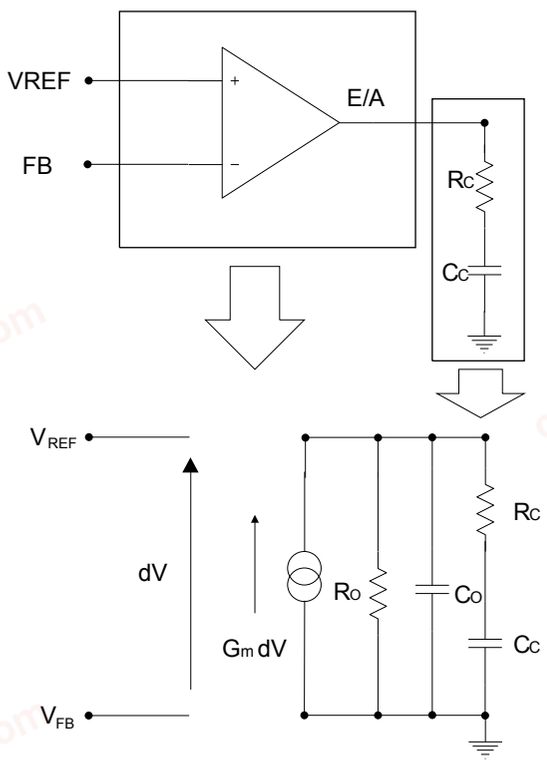
where:

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]} \quad (16)$$

7.2 Error amplifier compensation network

The following figure shows the typical compensation network required to stabilize the system.

Figure 24. Trans-conductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. The transfer function of the error amplifier and its compensation network is:

$$A_O(s) = \frac{A_{VO} \cdot (1 + s \cdot R_C \cdot C_C)}{s^2 \cdot R_O \cdot C_O \cdot R_C \cdot C_C + s \cdot (R_O \cdot C_C + R_O \cdot C_O + R_C \cdot C_C) + 1} \quad (17)$$

where:

$$A_{VO} = G_m \cdot R_O \quad (18)$$

The poles of this transfer function are (if $C_C >> C_O$):

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$$f_{PLF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_C} \quad (19)$$

$$f_{PHF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_O} \quad (20)$$

Whereas the zero is defined as:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C} \quad (21)$$

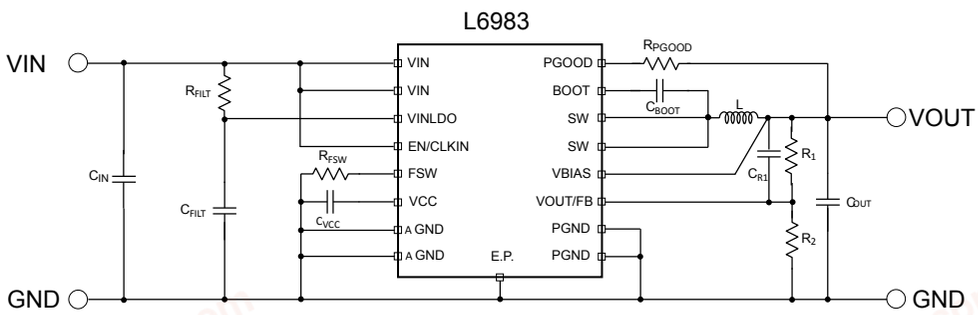
7.3 Voltage divider

The contribution of a simple voltage divider is:

$$G_{DIV}\left(s\right) = \frac{R_2}{R_1 + R_2} \quad (22)$$

A small signal capacitor in parallel to the upper resistor (only for the adjustable part number) of the voltage divider implements a leading network ($f_{ZERO} < f_{POLE}$), sometimes necessary to improve the system phase margin:

Figure 25. Leading network example



Laplace transformer of the leading network:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{(1 + s \cdot R_1 \cdot C_{R1})}{\left(1 + s \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}\right)} \quad (23)$$

where:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{R1}} \quad (24)$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}} \quad (25)$$

$$f_Z < f_P \quad (26)$$

So closing the loop, the loop gain is:

$$G(s) = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_O(s) \quad (27)$$

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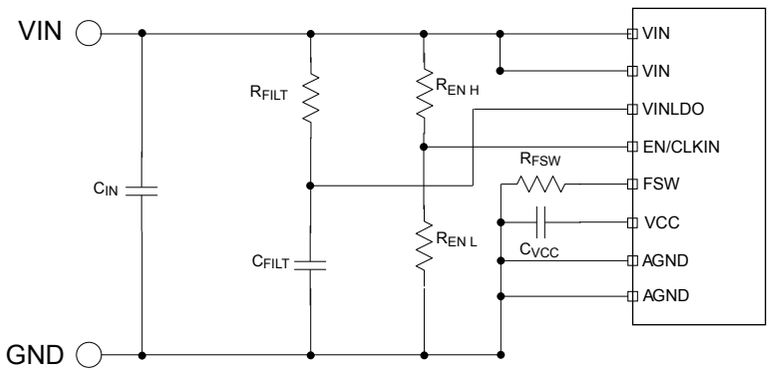
8 Application notes

8.1 Programmable power up threshold

The enable rising threshold is equal to 1.2 V typical (refer to Table 6. Electrical characteristics). The power-up threshold is adjusted according to the following equation:

$$V_{Power\ Up} = 1.2V \cdot \left(1 + \frac{R_{EN\ H}}{R_{EN\ L}}\right) \quad (28)$$

Figure 26. Leading network example



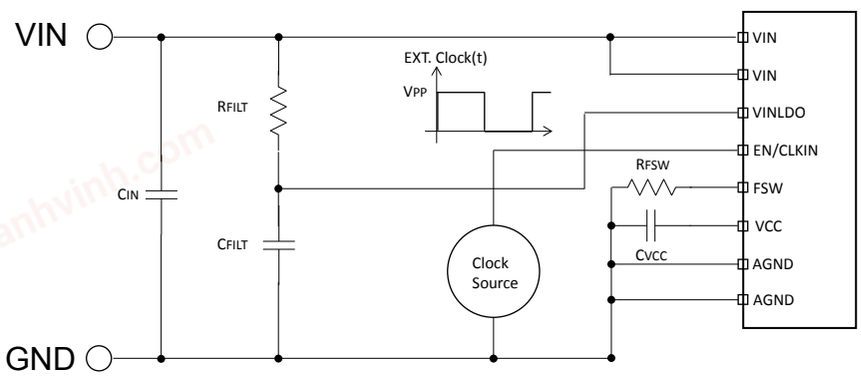
The enable falling threshold is equal to 1.0 V typical (refer to Table 6. Electrical characteristics). The turn threshold is obtained according to the following equation:

$$V_{Power\ Up} = 1.0V \cdot \left(1 + \frac{R_{EN\ H}}{R_{EN\ L}}\right) \quad (29)$$

8.2 External synchronization (available for low noise mode only)

The device allows a direct connection between a clock source and the EN/CLKIN pin.

Figure 27. External synchronization. Direct connection.



The device internally implements a low-pass filter connected to EN/CLKIN pin that is able to acquire the average value of the applied signal.

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The device turns on when the average of the signal applied is higher than V_{EN} rising (refer to Table 6. Electrical characteristics). The device turns off when the average of the signal should be lower than V_{EN} falling (refer to Table 6. Electrical characteristics).

Considering, for example, a clock source with V_{PP} = 5.0 V, the minimum duty cycle to guarantee the power-up is given by:

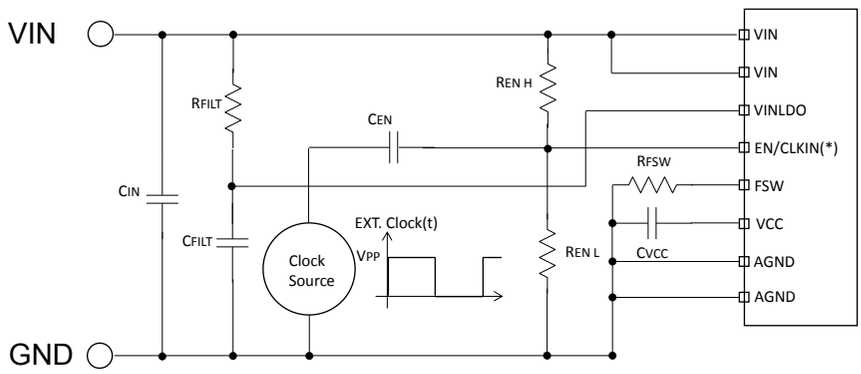
$$Duty_{min} = \frac{V_{EN,\ Rising}}{V_{PP}} = 0.24 \quad (30)$$

The maximum duty cycle to guarantee the turn-off is given by:

$$Duty_{MAX,} = \frac{V_{EN,\ Falling}}{V_{PP}} = 0.2 \quad (31)$$

The device allows also the AC coupling.

Figure 28. External synchronization. AC coupling



The AC-coupling allows the device to keep the power-up and down thresholds defined by the partition connected to EN/CLKIN pin and described on Section 8.1 Programmable power up threshold.

The following table resumes the minimum pulse duration for the external signal and maximum duty cycle that allows the synchronization by keeping the selected power-up and down thresholds.

Table 8. External synchronization AC coupling suggested operation range

V_{PP} [V]	TON, MIN, EXT_{Clock} [ns]	DMAX, EXT_{Clock} [%]
2.3	70	45
3.3	20	30
5	20	20

The minimum amplitude for the external clock signal is, for both the configurations, equal to 2.3 V.

The network given by C_{EN} and R_{ENL} sets a high-pass filter. Considering a resistor in the order of 220 kΩ, a capacitor equal to 1 nF is a correct choice.

8.3 Output voltage adjustment

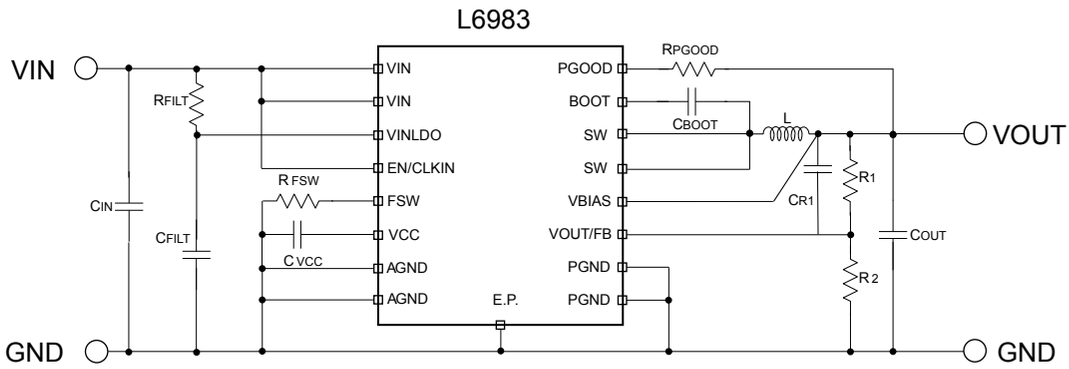
The error amplifier reference voltage is 0.85 V typical (refer to Table 6. Electrical characteristics). The output voltage is adjustable as per the following equation:

$$V_{OUT} = 0.85V \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (32)$$

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CR1 capacitor is sometimes useful to increase the small signal phase margin (please refer to the Section 7 Closing the loop).

Figure 29. Application circuit



8.4 Switching frequency

A resistor connected to the FSW pin features the selection of the switching frequency (refer to the Table 7. FSW selection).

Connecting the resistor between the pins R_{FSW} and VCC, the internal dithering circuit is turned on. (refer to the Section 6.6 Spread spectrum).

8.5 Design of the power components

8.5.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so, its RMS current capability must be selected according to the application conditions. Internal losses of the input filter depends on the ESR value so usually low ESR capacitors (such as multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current, flowing through the capacitor, can be calculated as follows:

$$I_{RMS} = I_{OUT} \cdot \sqrt{\left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta}} \quad (33)$$

Where I_{OUT} is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to $I_{OUT}/2$. In a specific application, the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INmin} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}} \quad (34)$$

$$D_{min} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMAX} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}} \quad (35)$$

Where $\Delta V_{HIGHSIDE}$ and $\Delta V_{LOWSIDE}$ are the voltage drops across the embedded switches. The peak-to-peak voltage across the input filter can be calculated as the equation below:

$$V_{PP} = \frac{I_{OUT}}{C_{IN} \cdot F_{SW}} \cdot \left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta} + ESR \cdot (I_{OUT} + \Delta I_L) \quad (36)$$

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In case of negligible ESR (MLCC capacitor), the equation of CIN as a function of the target VPP can be written as follows:

$$C_{IN} = \frac{I_{OUT}}{V_{PP} \cdot F_{SW}} \cdot \left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta} \quad (37)$$

Considering η = 1 this function has its maximum in D = 0.5:

$$C_{INmin} = \frac{I_{OUT}}{4 \cdot V_{PPMAX} \cdot F_{SW}} \quad (38)$$

Typically, CIN is dimensioned to keep the maximum peak-peak voltage across the input filter in the order of 5% V_{INMAX}.

In the following table, some suitable capacitor part numbers are listed.

Table 9. Capacitor part numbers

Manufacturer	Series	Size	Cap value (µF)	Rated voltage (V)
TDK	CGA5L3X5R1H106K160AB	1206	10	50
	C3216X5R1H106K160AB	1206	10	50
Murata	GRT31CR61H106KE01	1206	10	50

8.5.2 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple. Usually the inductor value is selected in order to keep the current ripple lower than 20% - 40% of the output current over the input voltage range. The inductance value can be calculated by the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF} \quad (39)$$

Where T_{ON} and T_{OFF} are the on and off time of the internal power switch. The maximum current ripple, at fixed V_{OUT}, is obtained at maximum T_{OFF} that is at minimum duty cycle. So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

$$L_{min} = \frac{V_{OUT}}{\Delta IL_{MAX}} \cdot \frac{1 - D_{min}}{F_{SW}} \quad (40)$$

In order to prevent the sub-harmonic instability in the peak current control loop, a slope compensation mechanism is internally implemented. This implies two limits on the inductor selection. In order to avoid poor slope compensation or over slopping with a pole coming back into the BW degrading phase margin, the inductor should be designed so that:

$$0.4 \leq Q_P \leq 1.33 \quad (41)$$

Where QP has been defined in Section 7.1 GCO(s) control to output transfer function.

Given the QP defined range the inductor should be selected with a value between

$$L_{SLOPE,min} = \frac{V_{IN,MAX} - V_{OUT}}{S_e} \cdot \left(\frac{\frac{1}{\pi \cdot Q_{P,MAX}} + \frac{1}{2}}{1 - \frac{V_{OUT}}{V_{IN,MAX}}} - 1 \right) \quad (42)$$

and:

$$L_{SLOPE,MAX} = \frac{V_{IN,min} - V_{OUT}}{S_e} \cdot \left(\frac{\frac{1}{\pi \cdot Q_{P,min}} + \frac{1}{2}}{1 - \frac{V_{OUT}}{V_{IN,min}}} - 1 \right) \quad (43)$$

In order to have the correct ripple, avoid sub-harmonic instability or over slopping, the selected inductor should satisfy every reported conditions.

The peak current through the inductor is given by:

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$$I_{L,PK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (44)$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

8.5.3 Output capacitor selection

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). Therefore, the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as:

$$\Delta V_{OUT} = ESR \cdot \Delta I_{L,MAX} + \frac{\Delta I_{L,MAX}}{8 \cdot C_{OUT} \cdot F_{SW}} \quad (45)$$

For a ceramic (MLCC) capacitor, the capacitive component of the ripple dominates the resistive one. While for an electrolytic capacitor the opposite is true. Neglecting the ESR contribution the minimum value of the output capacitor is given by:

$$C_{OUT,min,RIPPLE} = \frac{\Delta I_{L,MAX}}{8 \cdot \Delta V_{OUT} \cdot F_{SW}} \quad (46)$$

As the compensation network is internal, the output capacitor should be selected in order to have a proper phase margin and then a stable control loop. A good rule to obtain a proper dimensioning for the minimum amount of the output capacitor is set the target system bandwidth equal to $F_{SW}/8$. The following equation keep into account the precedent consideration:

$$C_{OUT,BW,min} = \frac{8.04}{\frac{Fsw}{8} \cdot V_{OUT}} \quad (47)$$

The maximum amount of the output capacitor is given by:

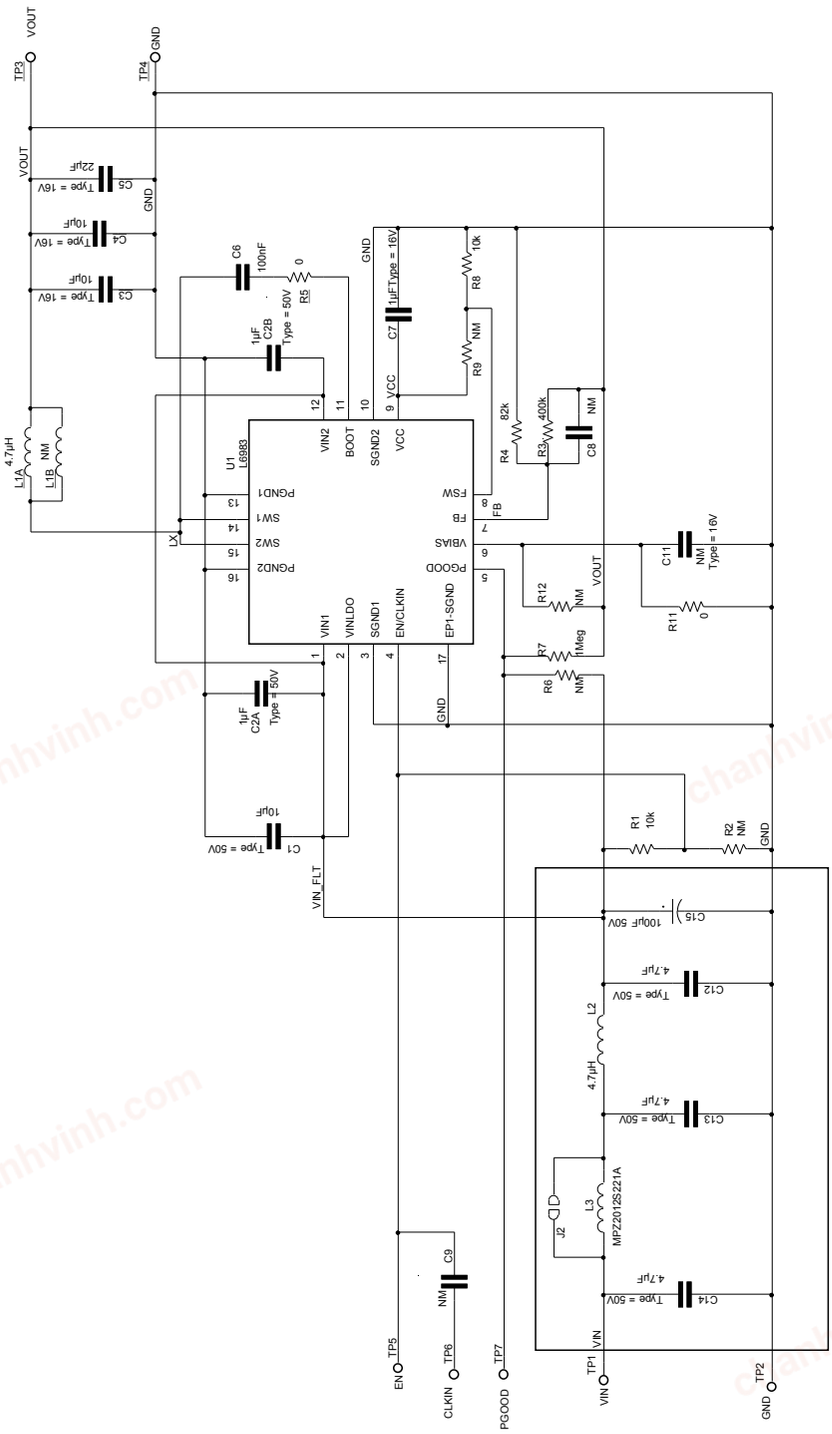
$$C_{OUT,BW,MAX} = \frac{0.960 \cdot 10^{-3}}{V_{OUT}} \quad (48)$$

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9 Application board

The figure below shows the reference evaluation board schematic:

Figure 30. Evaluation board schematic



The additional input filter (C14, L3, C13, L2, C12, and C15) limits the conducted emission on the power supply.

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Table 10. **Bill of material**

Reference	Part number	Description	Manufacturer
C1	CGA5L3X5R1H106K160AB	10 µF 50 V	TDK
C2A	CGA4J3X7R1H105K125AB	1 µF 50 V	TDK
C2B	CGA4J3X7R1H105K125AB	1 µF 50 V	TDK
C3-C4	GCM31CR71C106KA64L	10 µF 16 V	MURATA
C5	CGA6P1X7R1C226M250AC	22 µF 16 V	TDK
C6	CGA3E2X7R1H104K080AA	100 nF 50 V	TDK
C7	C2012X8R1C105K125AB	1 µF 16V	TDK
C8		NOT MOUNTED	
C9		NOT MOUNTED	
C11		NOT MOUNTED	
C12-C13-C14	GRM31CR71H475KA12L	4.7 µF 50 V	Murata
C15	EEHZA1H101P	100 µF, 50 V	Panasonic
L1B		NOT MOUNTED	
L1A	XAL6060-472ME	4.7 µH	Coilcraft
L2	XAL4030-472ME	4.7 µH	Coilcraft
L3	MPZ2012S221A	220 Ω 100 MHz	TDK
R1		10 k 1%	any
R2		NOT MOUNTED	
R3		400 k 1%	any
R4		82 k 1%	any
R5		0	any
R6		NOT MOUNTED	
R7		1 M 1%	any
R8		10 k 1%	any
R9		NOT MOUNTED	
R11		0	any
R12		NOT MOUNTED	any
J2			
U1	L6983CQTR		ST Microelectronics

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Figure 31. **Top layer**

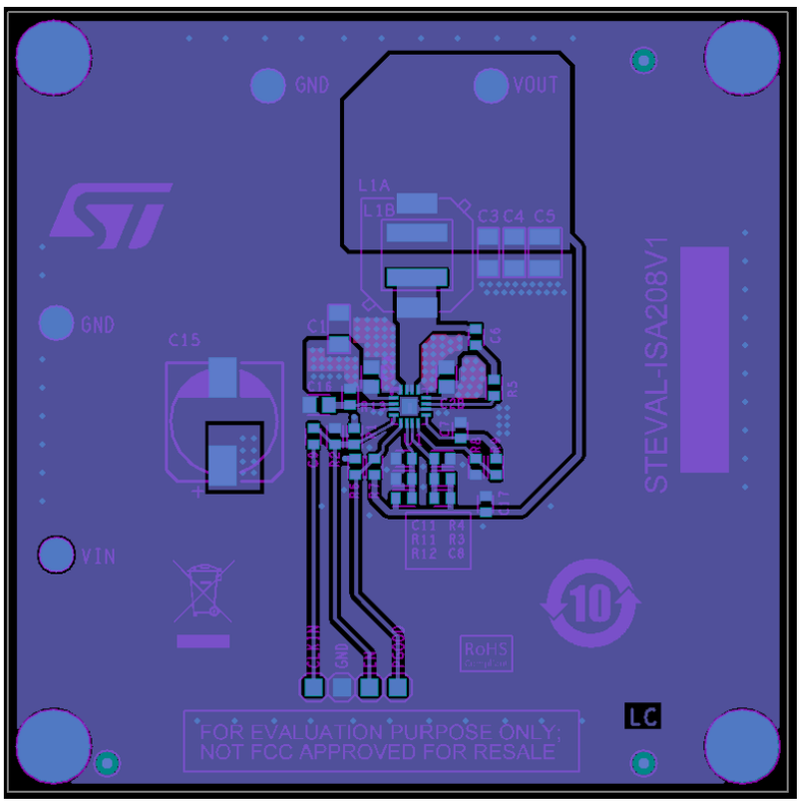
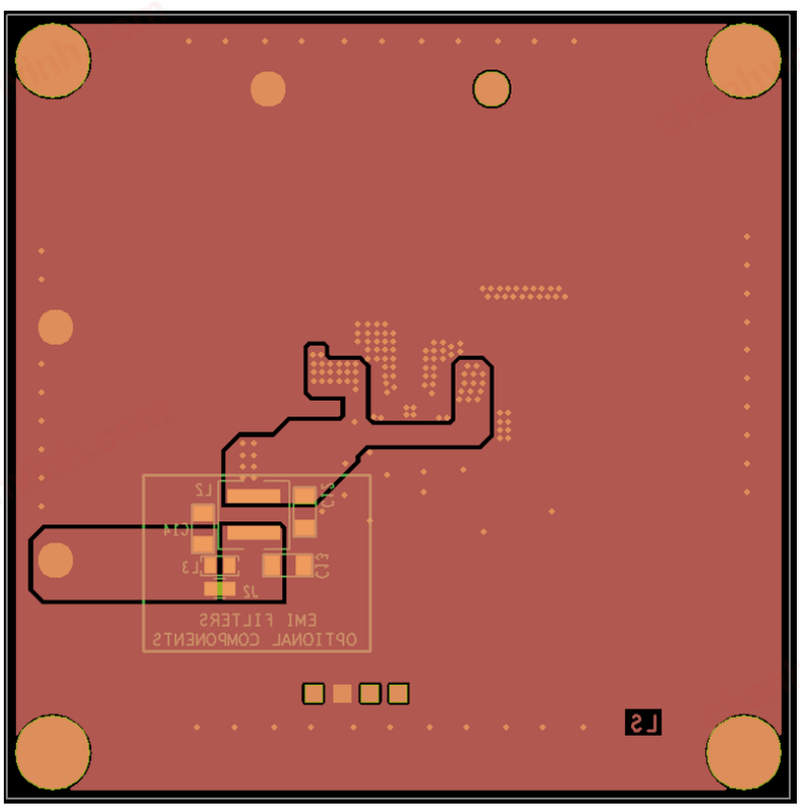


Figure 32. **Bottom layer**



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10 Efficiency curves

The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, STEVAL-ISA208V1, selecting the following output filter:

- C_{OUT}:
  - 1 x CGA6P1X7R1C226M250AC 22 µF 16 V (TDK);
  - 2 x CGA5L3X5R1H106K160AB 10 µF 50 V (TDK).
- Inductor:
  - XAL6060-153ME (Coilcraft)

Figure 33. Efficiency V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ

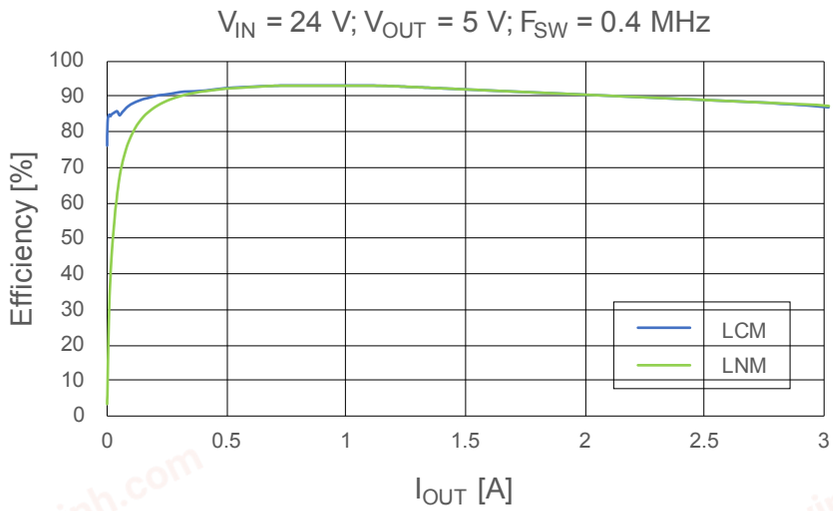
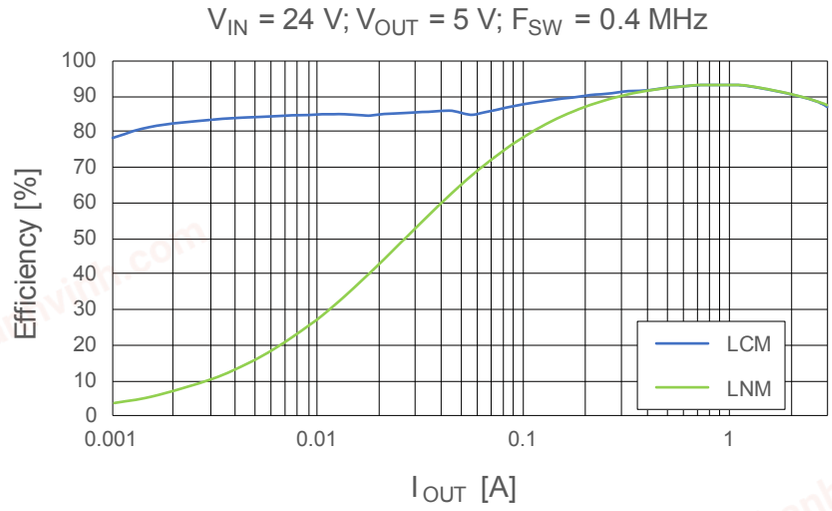
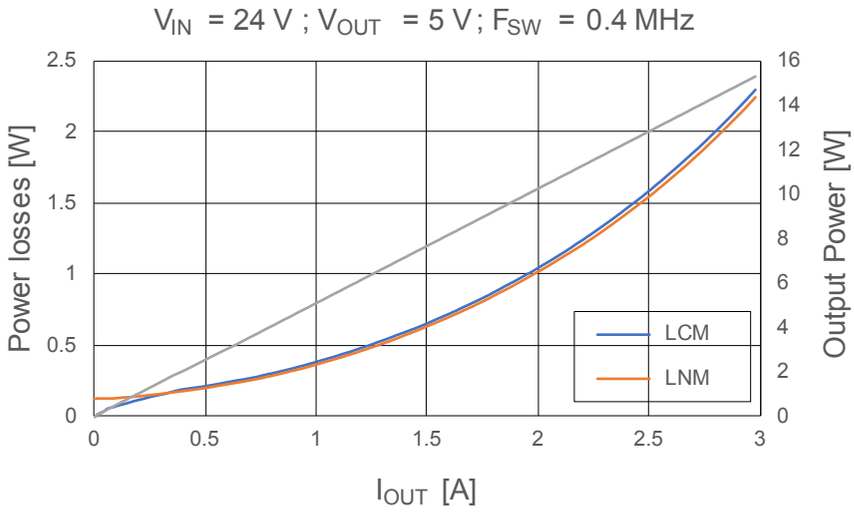


Figure 34. Efficiency V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ (log scale)



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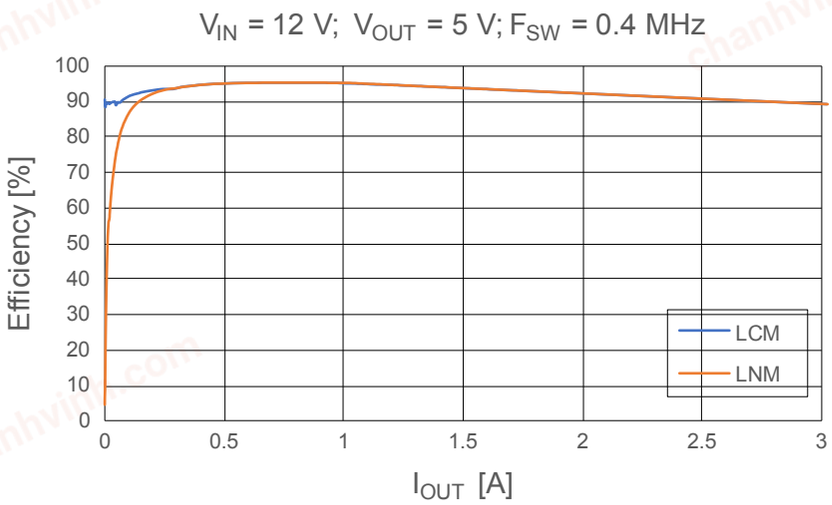
Figure 35. **Power losses V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, STEVAL-ISA208V1, selecting the following output filter:

- C_{OUT}:
  - 1 x CGA6P1X7R1C226M250AC 22 µF 16 V (TDK);
  - 2 x CGA5L3X5R1H106K160AB 10 µF 50 V (TDK).
- Inductor:
  - XAL6060-153ME (Coilcraft).

Figure 36. **Efficiency V_{IN} = 12 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ**



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Figure 37. **Efficiency V_{IN} = 12 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ (log scale)**

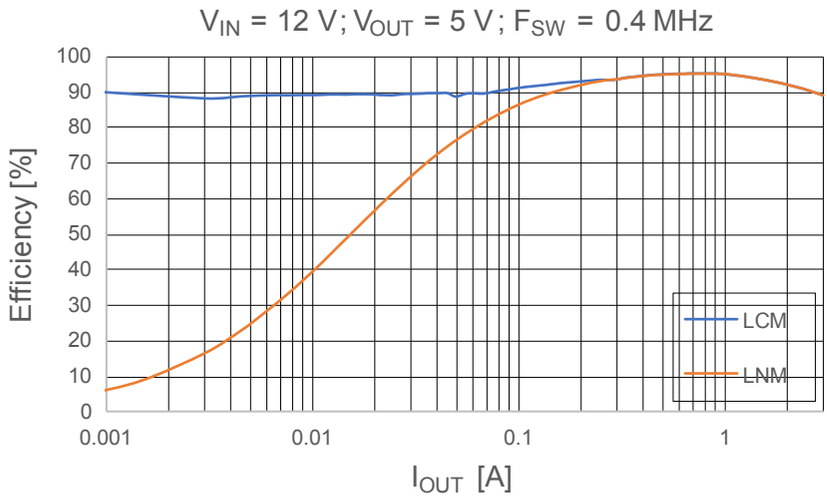
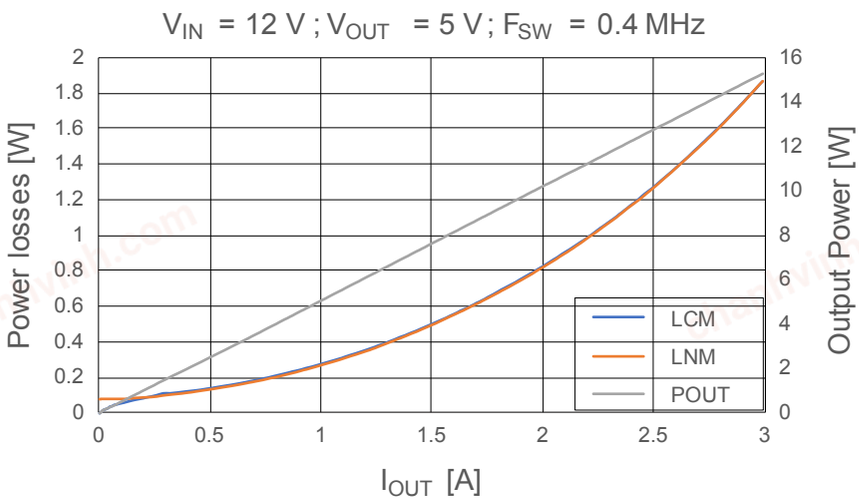


Figure 38. **Power losses V_{IN} = 12 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, STEVAL-ISA208V1, selecting the following output filter:

- C_{OUT}:
  - 2 x CGA6P1X7R1C226M250AC 22 µF 16 V (TDK);
  - 2 x CGA5L3X5R1H106K160AB 10 µF 50 V (TDK).
- Inductor:
  - XAL6060-822ME (Coilcraft).

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Figure 39. **Efficiency V_{IN} = 24 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ**

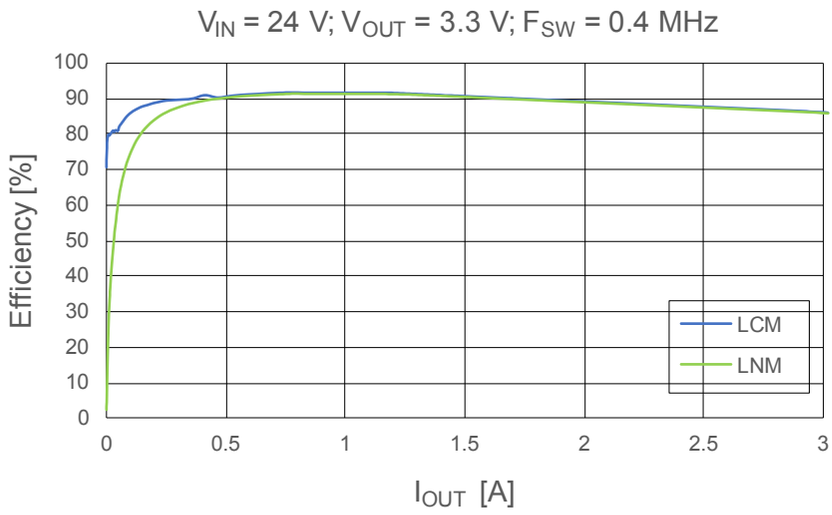
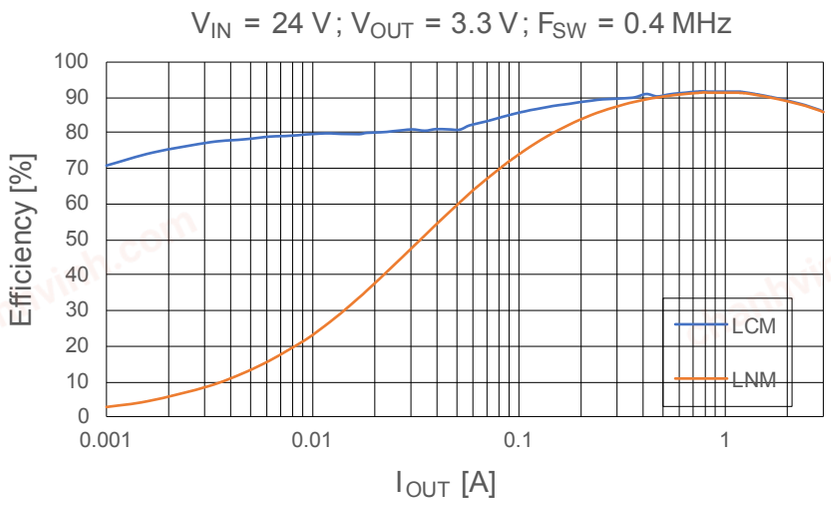
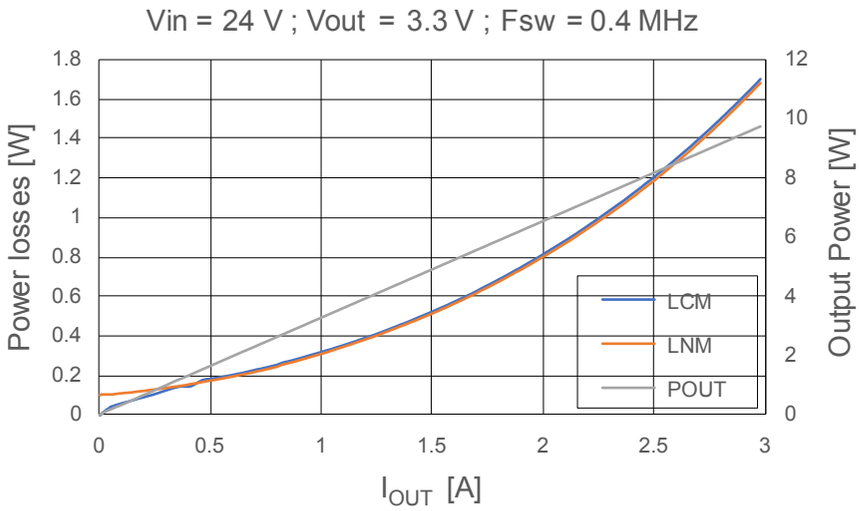


Figure 40. **Efficiency V_{IN} = 24 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ (log scale)**



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Figure 41. **Power losses V_{IN} = 24 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, STEVAL-ISA208V1, selecting the following output filter:

- C_{OUT}:
  - 2 x CGA6P1X7R1C226M250AC 22 µF 16 V (TDK);
  - 2 x CGA5L3X5R1H106K160AB 10 µF 50 V (TDK).
- Inductor:
  -

  XAL6060-822ME (Coilcraft)

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Figure 42. **Efficiency V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ**

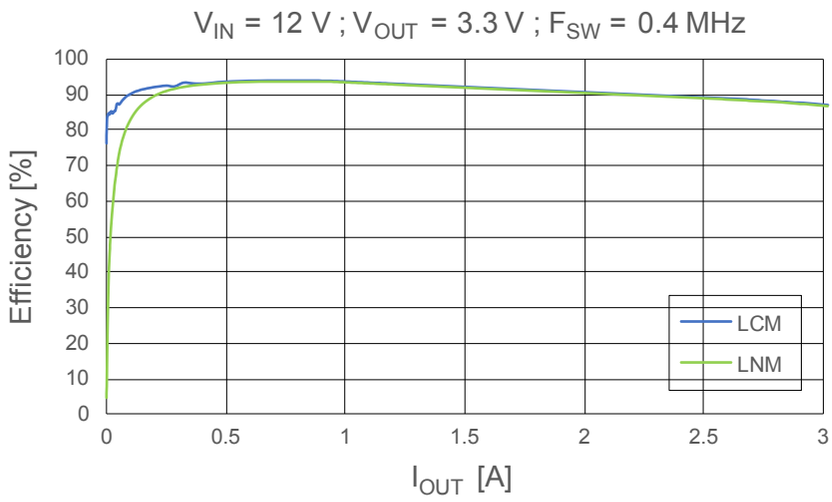
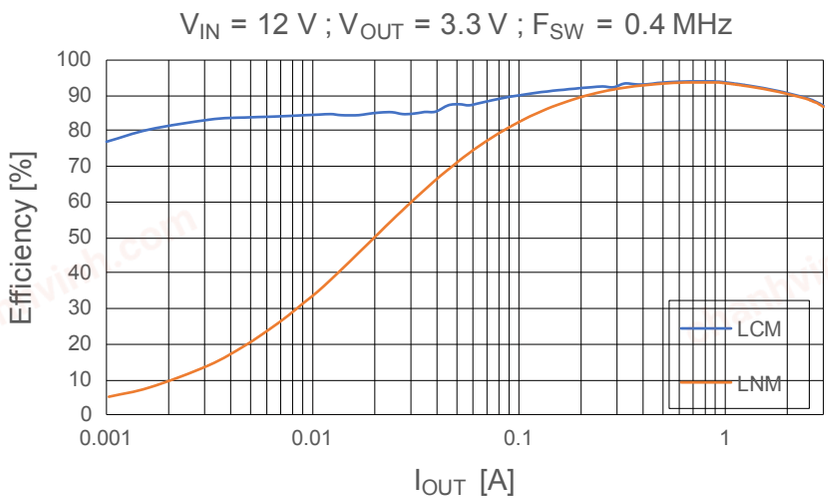
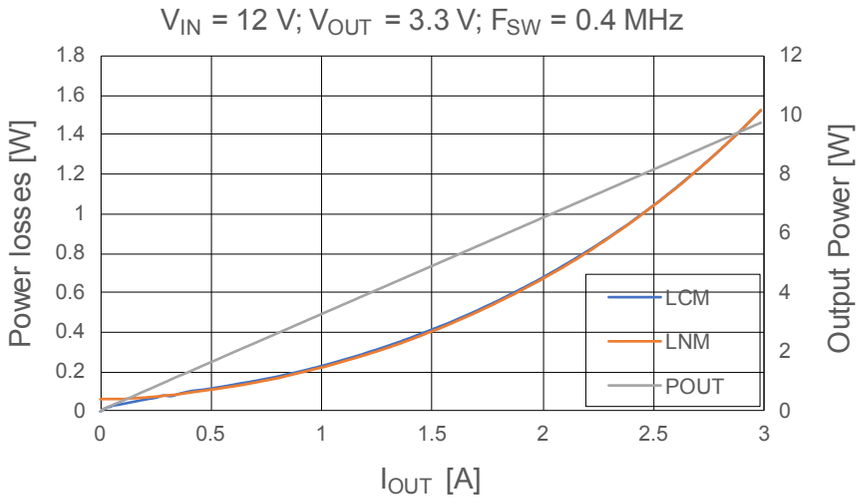


Figure 43. **Efficiency V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ (log scale)**



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Figure 44. **Power losses V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, STEVAL-ISA208V1, selecting the following output filter:

- C_{OUT}:
  - 1 x CGA6P1X7R1C226M250AC 22 µF 16 V (TDK);
  - 1 x CGA5L3X5R1H106K160AB 10 µF 50 V (TDK).
- Inductor:
  - XAL6060-472ME (Coilcraft).

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Figure 45. **Efficiency V_{IN} = 24 V; V_{OUT} = 3.3 V; F_{SW} = 1.0 MHZ**

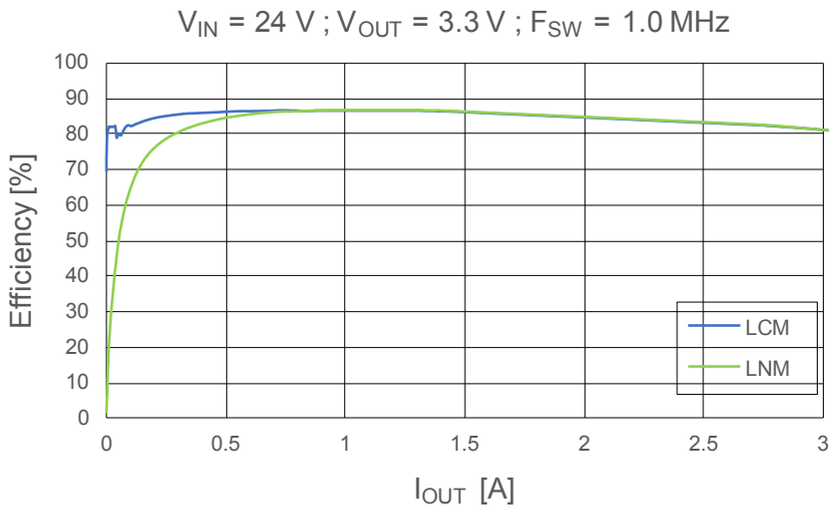
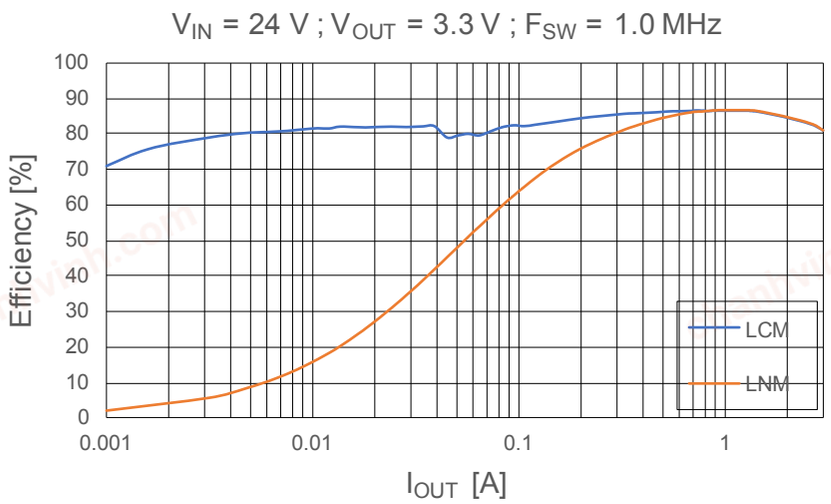
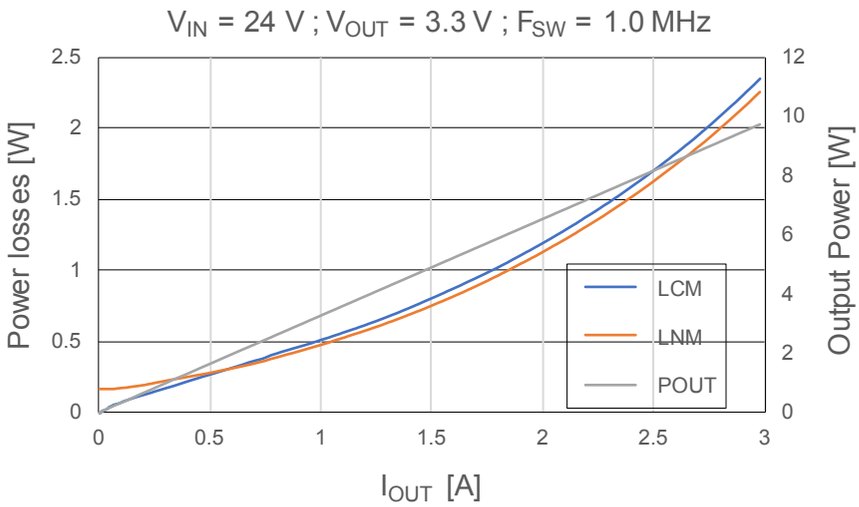


Figure 46. **Efficiency V_{IN} = 24 V; V_{OUT} = 3.3 V; F_{SW} = 1.0 MHZ (log scale)**



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Figure 47. **Power losses V_{IN} = 24 V; V_{OUT} = 3.3 V; F_{SW} = 1.0 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, STEVAL-ISA208V1, selecting the following output filter:

- C_{OUT}:
  - 1 x CGA6P1X7R1C226M250AC 22 µF 16 V (TDK);
  - 1 x CGA5L3X5R1H106K160AB 10 µF 50 V (TDK).
- Inductor:
  - XAL6060-472ME (Coilcraft).

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Figure 48. **Efficiency V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 1.0 MHZ**

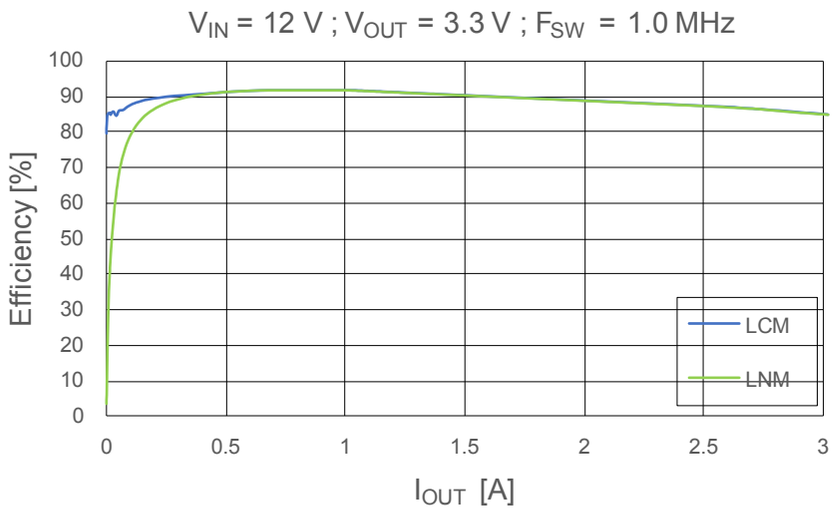
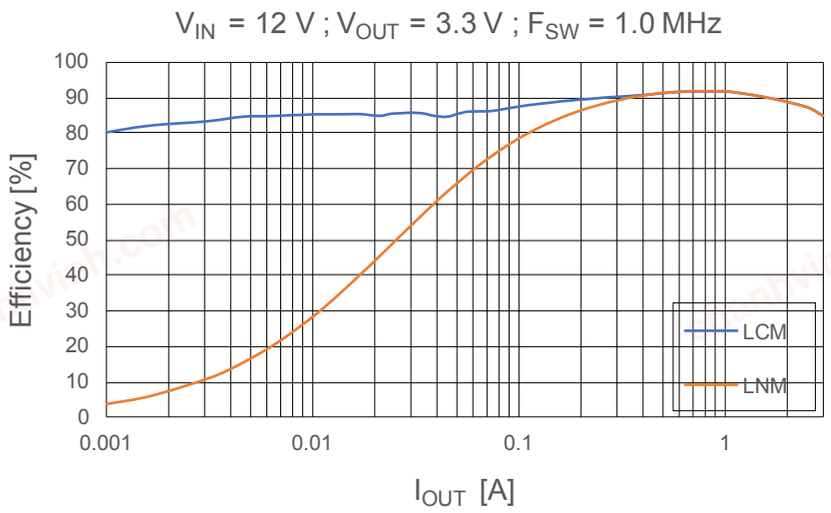
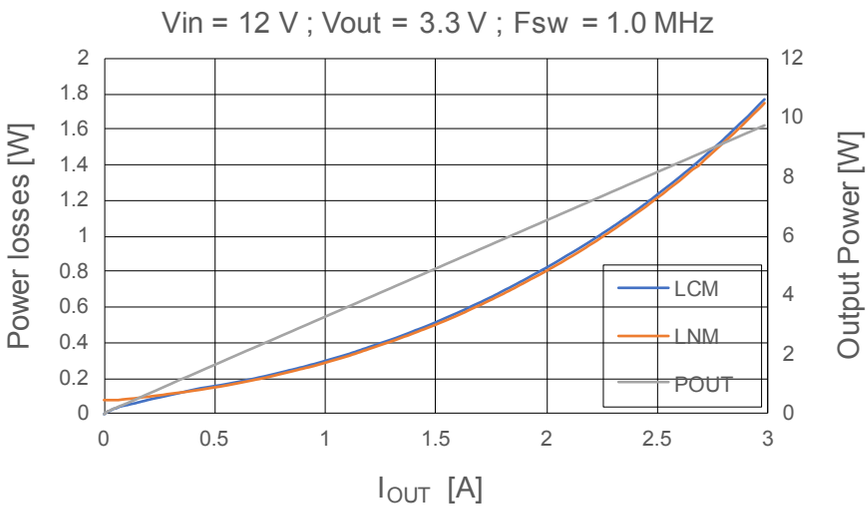


Figure 49. **Efficiency V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 1.0 MHZ (log scale)**



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Figure 50. **Power losses V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 1.0 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, STEVAL-ISA208V1, selecting the following output filter:

- C_{OUT}:
  - 1 x CGA6P1X7R1C226M250AC 22 µF 16V (TDK);
  - 2 x CGA5L3X5R1H106K160AB 10 µF 50V (TDK).
- Inductor:
  - XAL6060-472ME (Coilcraft).

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Figure 51. . Efficiency V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 1.0 MHZ

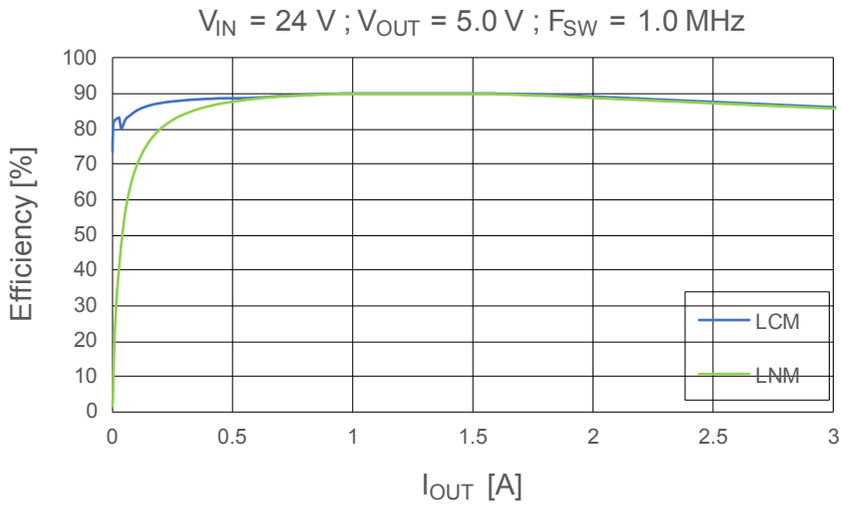


Figure 52. Efficiency V_{IN} = 24 V; V_{OUT} = 5.0 V; F_{SW} = 1.0 MHZ (log scale)

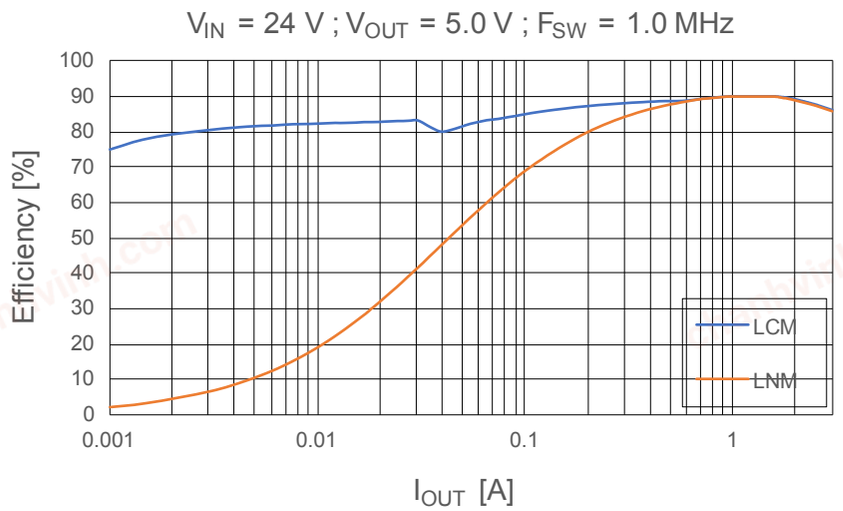
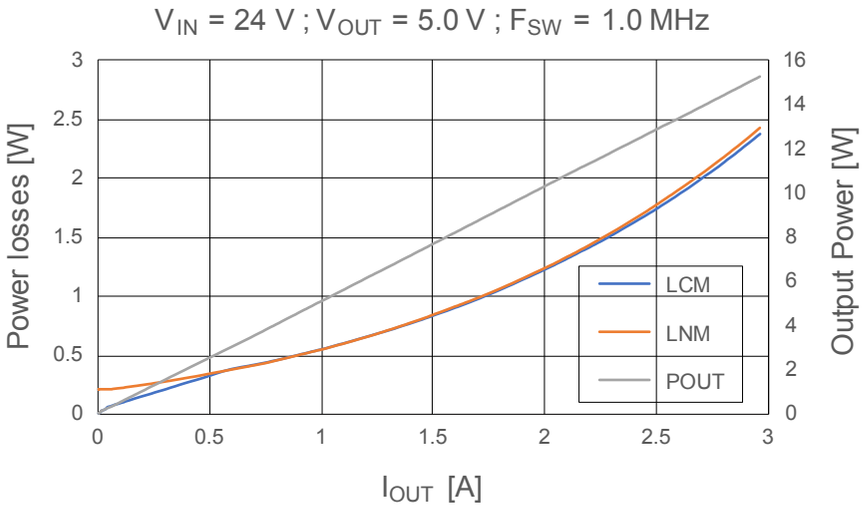


Figure 53. Power losses V_{IN} = 24 V; V_{OUT} = 5.0 V; F_{SW} = 1.0 MHZ

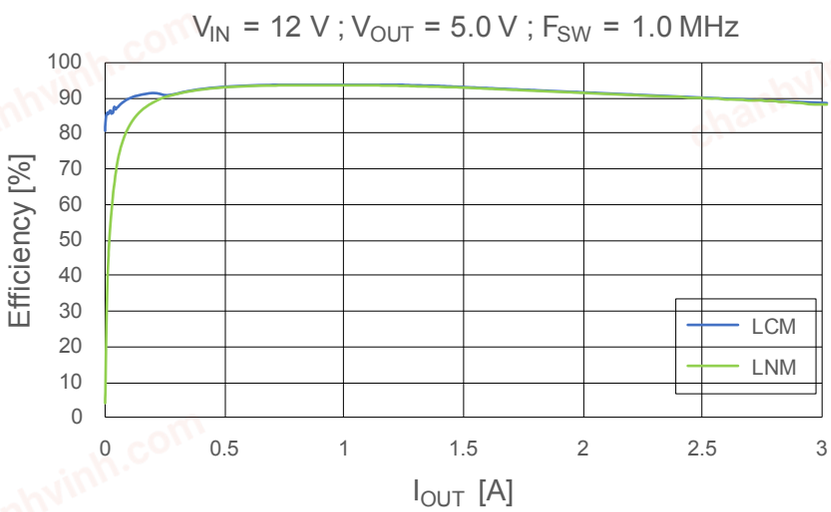
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The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, STEVAL-ISA208V1, selecting the following output filter:

- C_{OUT}:
  - 1 x CGA6P1X7R1C226M250AC 22 µF 16 V (TDK);
  - 1 x CGA5L3X5R1H106K160AB 10 µF 50 V (TDK).
- Inductor:
  - XAL6060-472ME (Coilcraft).

Figure 54. Efficiency V_{IN} = 12 V; V_{OUT} = 5.0 V; F_{SW} = 1.0 MHZ



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Figure 55. **Efficiency V_{IN} = 12 V; V_{OUT} = 5.0 V; F_{SW} = 1.0 MHZ (log scale)**

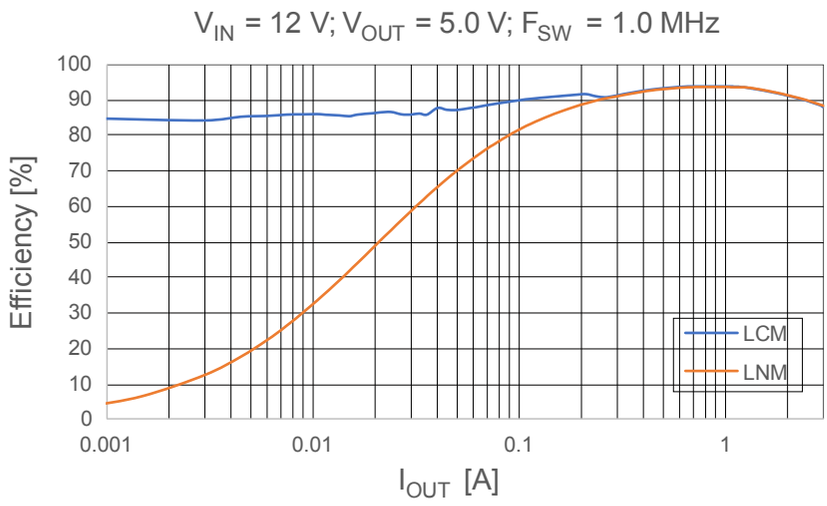
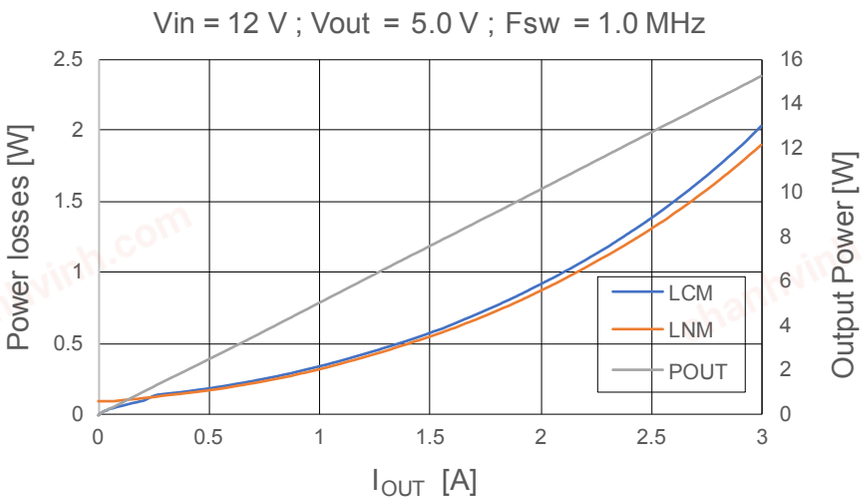


Figure 56. **Power losses V_{IN} = 12 V; V_{OUT} = 5.0 V; F_{SW} = 1.0 MHZ**



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11 Thermal dissipation

The thermal design is important in order to prevents thermal shutdown of the device if junction temperature goes above 165 °C. The three different sources of losses within the device are:

1. Conduction losses due to the on-resistance of high-side switch (R_{DSON_HS}) and low-side switch (R_{DSON_LS}); these are equal to:

$$P_{COND} = R_{DSON_HS} \cdot I_{OUT}^2 \cdot D + R_{DSON_LS} \cdot I_{OUT}^2 \cdot \left(1 - D\right) \quad (49)$$

where D is the duty cycle of the selected application and is given by the following formula:

$$D = \frac{V_{OUT} + \left(R_{DSON_LS} + DCRl\right) \cdot I_{OUT}}{V_{IN} - \left(R_{DSON_{HS}} - R_{DSON_LS}\right) \cdot I_{OUT}} \quad (50)$$

In order to obtain a more accurate extimation it is necessary to keep into account that the amount of resistance of the internal power MOSFET increases together with the temperature. For this reason, the value of R_{DSONHS} and R_{DSONLS}, should be increased from the typical of a factor equal to 15%.

1. Switching losses due to high-side power MOSFET turn-ON and OFF; these can be calculated as per below:

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} \quad (51)$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the high side power switch (VDS) and the current flowing into it during turn-ON and turn-OFF phases, as shown in Figure 57. Switching losses.

T_{SW} is the equivalent switching time. For this device the typical value for the equivalent switching time is 20 ns.

1. Quiescent current losses, calculated as the equation below:

$$P_Q = V_{IN} \cdot I_{Q,MAX} \quad (52)$$

where I_Q is the quiescent current and depends on the V_{BIAS} connections. If V_{BIAS} is connected to GND, the maximum is equal to 3 mA. Otherwise if V_{BIAS} is connected to V_{OUT} the quiescent current is given by:

$$I_{Q,MAX} = 0.8\left[mA\right] + \frac{1}{\eta_{L6983}} \cdot \frac{V_{BIAS}}{V_{IN}} \cdot 2.3\left[mA\right] \quad (53)$$

The power losses are given by:

$$P_{LOSS} = P_{COND} + P_{SW} + P_Q \quad (54)$$

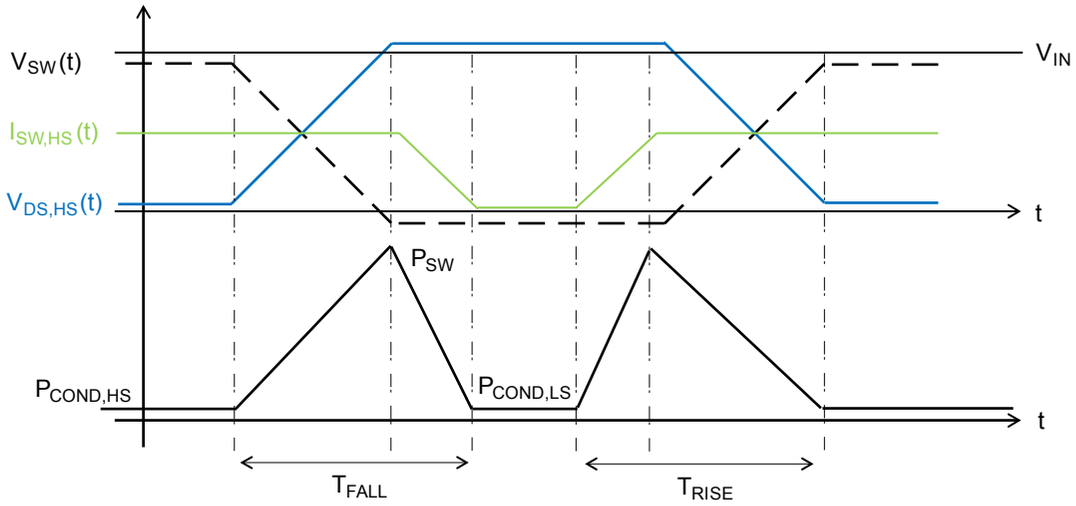
The junction temperature T_J can be calculated as:

$$T_J = T_A + R_{thJA} \cdot P_{LOSS} \quad (55)$$

where T_A is the ambient temperature. R_{thJA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junctions to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The R_{thJA} measured on the demonstration board described in the following section is about 30 °C/W.

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Figure 57. **Switching losses**



It is also possible to estimate the junction temperature directly from the efficiency measures acquired on a stationary application condition.

Considering that the power losses are given by:

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (56)$$

Neglecting the AC losses of the selected inductor, the power losses related to the L6983 are given by:

$$P_{LOSS\ L6983} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT} - DCRl \cdot I_{OUT}^2 \quad (57)$$

Therefore, the junction temperature T_J can be calculated as:

$$T_J = T_A + R_{thJA} \cdot P_{LOSS,\ L6983} \quad (58)$$

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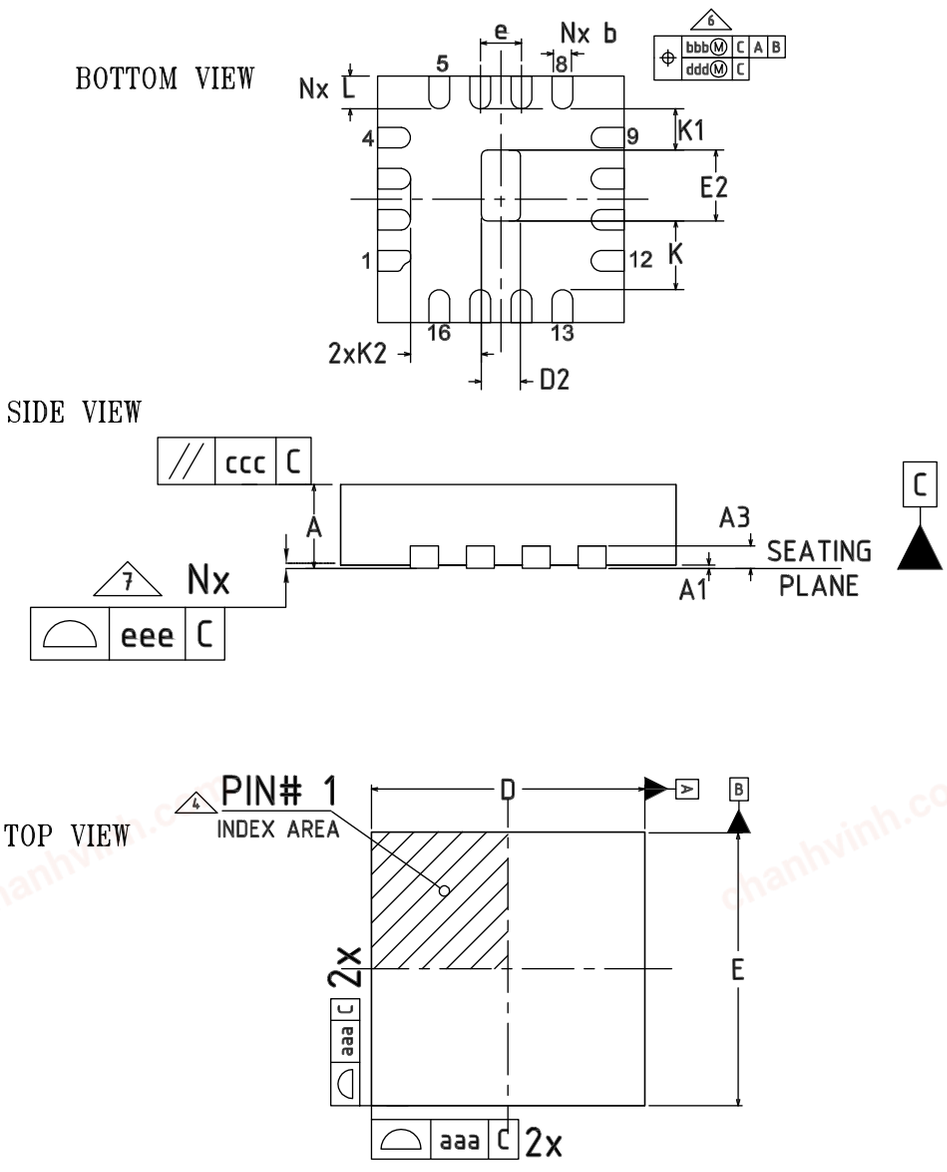
12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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12.1 QFN16 (3x3 mm) package information

Figure 58. **QFN16 (3x3 mm) package outline**

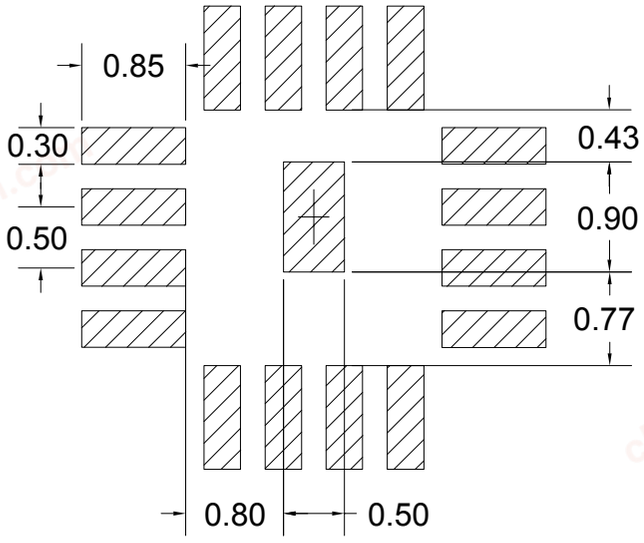


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Table 11. **QFN16 (3x3 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.7	0.75	0.8
A1	0	0.02	0.05
A3	0.203 Ref.		
b	0.18	0.25	0.3
D	3.00 BSC		
E	3.00 BSC		
e	0.50 BSC		
D2	0.43	0.48	0.53
E2	0.81	0.86	0.91
L	0.35	0.4	0.45
K	0.84		
K1	0.5		
K2	0.86		
N		16	
ND		4	
NE		4	
aaa	0.05		
bbb	0.1		
ccc	0.05		
ddd	0.05		
eee	0.05		

Figure 59. **QFN16 (3x3 mm) recommended footprint**



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13 Ordering information

Table 12. **Order codes**

Part numbers	Output voltage	Light load behavior	Package	Packaging
L6983CQTR	Adj.	LCM (Low Consumption Mode)	QFN16	Tape and reel
L6983C50QTR	5 V			
L6983C33QTR	3.3 V			
L6983NQTR	Adj.	LNM (Low Noise Mode)		
L6983N50QTR	5 V			
L6983N33QTR	3.3 V			

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Revision history

Table 13. **Document revision history**

Date	Revision	Changes
29-Oct-2019	1	Initial release.

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