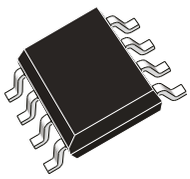
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L6982

Datasheet

38 V, 2 A synchronous step-down converter with low quiescent current



SO 8L

Maturity status link
L6982

Features

- 3.5 V to 38 V operating input voltage
- Output voltage from 0.85 V to V_{IN}
- 2 A DC output current
- Internal compensation network
- Two different versions: LCM for high efficiency at light-loads and LNM for noise sensitive applications
- 2 µA shutdown current
- Internal soft-start
- Enable
- Overvoltage protection
- Output voltage sequencing
- Thermal protection
- Synchronization to external clock for LNM devices
- SO 8L package

Applications

- Designed for 24 V buses industrial power systems
- 24 V battery powered equipment
- Decentralized intelligent nodes
- Sensors and always-on applications
- Low noise applications

Description

The L6982 is an easy to use synchronous monolithic step-down regulator capable of delivering up to 2 A DC to the load. The wide input voltage range makes the device suitable for a broad range of applications. The L6982 is based on a peak current mode architecture and is packaged in an SO 8L with internal compensation, thus minimizing design complexity and size.

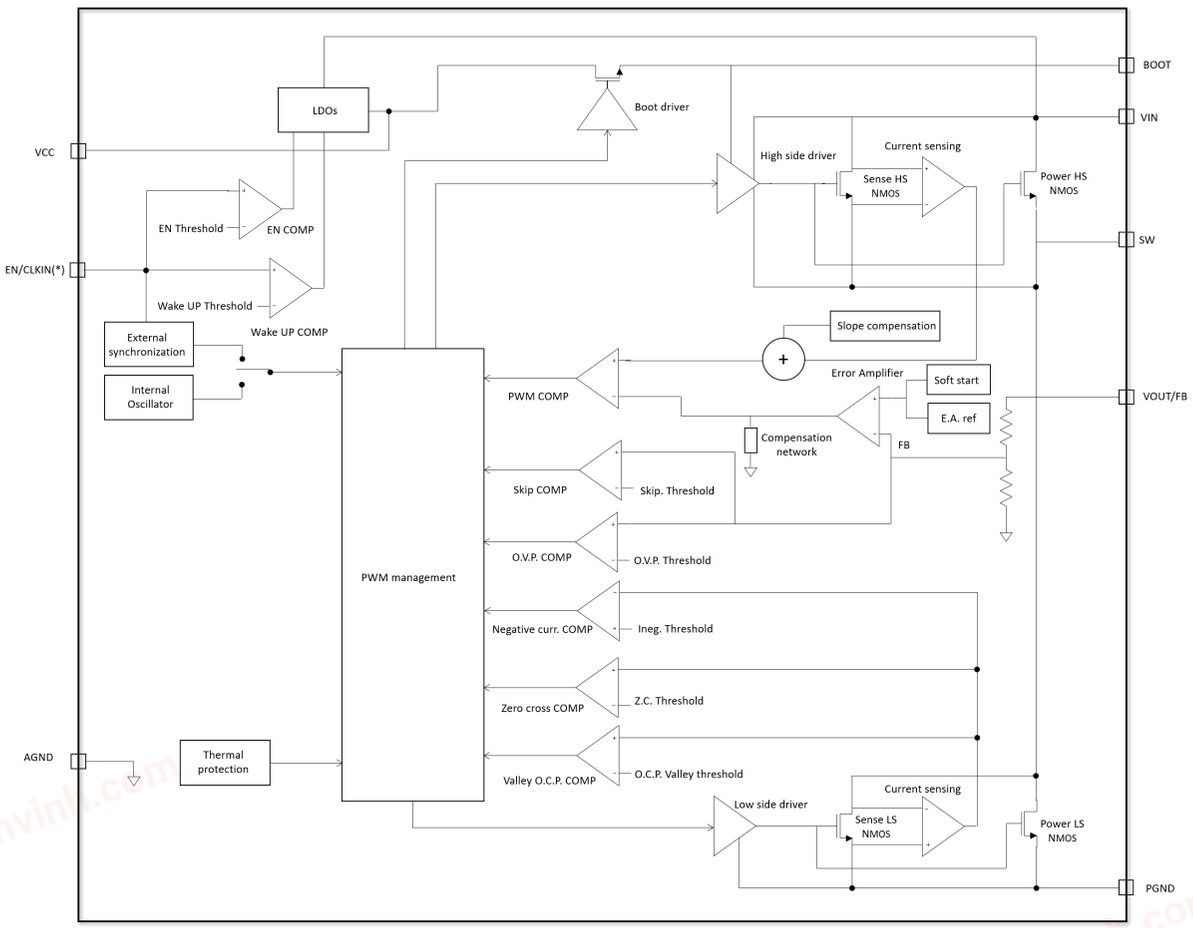
The L6982 is available both in low consumption mode (LCM) and low noise mode (LNM) versions. LCM maximizes the efficiency at light-load with controlled output voltage ripple so the device is suitable for battery-powered applications. LNM makes the switching frequency constant and minimizes the output voltage ripple for lightload operations, meeting the specification for low noise sensitive applications.

The EN pin provides enable/disable functionality. The typical shutdown current is 2 µA when disabled. As soon as the EN pin is pulled up the device is enabled and the internal 1.3 ms soft-start takes place. Pulse-by-pulse current sensing on both power elements implements an effective constant current protection and thermal shutdown prevents thermal run-away.

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1 Diagram

Figure 1. **Block diagram**

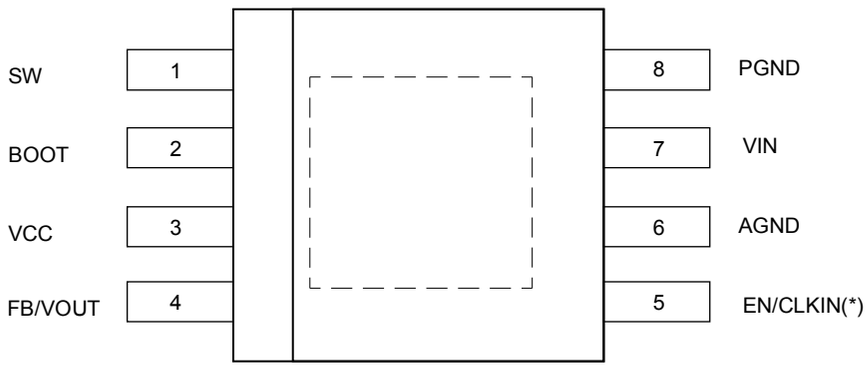


(*) Synchronization is allowed for LNM versions only.

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2 Pin configuration

Figure 2. **Pin connection (top view)**



(*) Synchronization is allowed for LNM versions only.

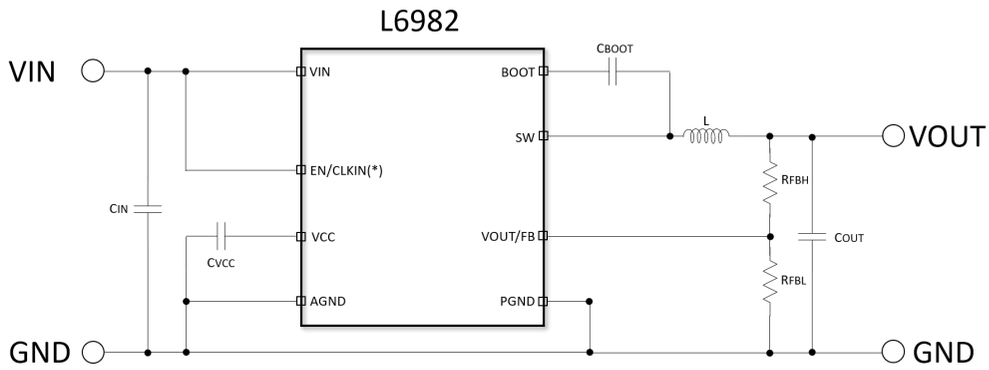
Table 1. **Pin description**

Pin #	Symbol	Function
1	SW	Switching node.
2	BOOT	Connect an external capacitor (100 nF typ.) between BOOT and SW pins. The gate charge required to drive the internal NMOS is refreshed during the low side switch conduction time.
3	VCC	This pin supplies the embedded analog circuitry. Connect a ceramic capacitor (≥ 1 µF) to filter internal voltage reference.
4	FB/VOUT	FB is output voltage sensing with eternal voltage divider.
5	EN/CLKIN	Enable pin with internal voltage divider. Pull down/up to disable/enable the device. In LNM versions, this pin is also used to provide an external clock signal, which synchronizes the device.
6	AGND	Analog ground.
7	VIN	DC input voltage.
8	PGND	Power ground.

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3 Typical application circuit

Figure 3. **Basic application (adjustable version)**



(*) Synchronization is allowed for LNM versions only.

Table 2. **Typical application component**

Symbol	Value	Description
C_{IN}	10 µF	Input capacitor
C_{VCC}	1 µF	VCC bypass capacitor
C_{BOOT}	100 nF	Bootstrap capacitor
C_{OUT}	47 µF	Output capacitor
R_{FBH}	400 kΩ	VOUT divider upper resistor
R_{FBL}	82 kΩ	VOUT divider lower resistor
L	22 µH	Output inductor

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4 Maximum ratings

Stressing the device above the ratings listed in the table below may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VIN	Maximum pin voltage	- 0.3	42	V
PGND to AGND	Maximum pin voltage	- 0.3	0.3	V
BOOT	Maximum pin voltage	SW – 0.3	SW + 4	V
VCC	Maximum pin voltage	- 0.3	Min. (VIN + 0.3 V; 4 V)	V
VOUT/FB	Maximum pin voltage	- 0.3	8	V
EN	Maximum pin voltage	- 0.3	VIN + 0.3	V
SW	Maximum pin voltage	- 0.85	VIN + 0.3	V
		- 3.8 for 0.5 ns		
I_{HS}, I_{LS}	High-side / Low-side RMS switch current		1.5	A
T_J	Operating temperature range	- 40	150	°C
T_{STG}	Storage temperature range	- 65	150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	°C

Note: All values are referred to AGND unless otherwise specified.

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD Protection voltage	HBM	2	kV
		CDM pins	500	V

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction ambient (device soldered on the STMicroelectronics demonstration board)	55	°C/W

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5 Electrical characteristics

Table 6. **Electrical characteristics T_J = 25 °C, V_{IN} = 24 V unless otherwise specified.**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		3.5		38	V
V_{INH}	V_{CC} rising threshold		2.3		3.3	V
V_{INL}	$V_{CC\ UVLO}$ falling threshold		2.15		3.15	V
I_{PK} (1)	Peak current limit	No slope contribution	2.73	3		A
		Full slope contribution	2.05	2.33		A
I_{VY}	Valley current limit		2.2	2.6	3	A
I_{SKIP} (1)(2)	Skip current limit			0.45		A
I_{VY_SINK} (1)	Reverse current limit	LNM or VOUT overvoltage	1.25	1.5	1.75	A
R_{DSON_HS}	High side RDSON			0.175		Ω
R_{DSON_LS}	Low-side RDSON			0.125		Ω
F_{SW} (3)	Switching frequency		360	400	440	KHz
T_{OFF_MIN}	Minimum off time			185		ns
T_{ON_MIN}	Minimum on time			85		ns
Enable						
V_{WAKE_UP}	Wakeup threshold	Rising			0.7	V
		Falling	0.2			V
V_{EN}	Enable threshold	Rising	1.08	1.2	1.32	V
		Hysteresis		0.2		V
VCC regulator						
V_{CC}	LDO output voltage		3.0	3.3	3.6	V
Power consumption						
I_{SHTDWN}	Shutdown current from V_{IN}	EN = GND		2	3	µA
LCM Device						
I_{Q_OPVIN}	Quiescent current from V_{IN}		20	35	60	µA
LNM Device						
I_{Q_OPVIN}	Quiescent current from VIN		1.6	2.3	3	mA
Soft start						
T_{SS}	Internal soft start		1	1.3	1.6	ms
Error amplifier						
V_{FB}	Voltage feedback	Adjustable version T_J = 25 °C	0.845	0.85	0.855	V
		Adjustable version T_J = -40 °C ≤ T_J ≤ 125 °C	0.842	0.85	0.858	V
Over voltage protection						
V_{OVP}	Overvoltage trip (VOVP/VREF)		115	120	125	%

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Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OVP_HYST}	Overvoltage Hysteresis		1	2	6	%
Synchronization (LNM versions only)						
f_{CLKIN} (3)	Synchronization range		200		500	KHz
V_{CLKIN_TH} (3)	Amplitude of synchronization clock		2.3			V
V_{CLKIN_T} (3)	Synchronization pulse ON and OFF time 2.3 ≤ V_{CLKIN_TH} ≤ 2.5 V		60			ns
	Synchronization pulse ON and OFF time V_{CLKIN_TH} > 2.5 V		20			ns
Thermal Shutdown						
T_{SHDWN} (5)	Thermal shutdown temperature			165		°C
T_{HYS} (5)	Thermal shutdown hysteresis			30		°C

1. *Parameter tested in the static condition during testing phase. The parameter value may change over a dynamic application condition.*
2. *LCM version.*
3. *LNM version.*
4. *Specifications in the - 40 to 125 °C temperature range are assured by characterization and statistical correlation.*
5. *Not tested in production.*

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6 Functional description

The L6982 device is based on a “peak current mode”, constant frequency control. Therefore, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

The device features LNM (low noise mode) that implements a forced PWM control, or LCM (low consumption mode) to increase the efficiency at light-load.

The main internal blocks shown in the block diagram in Figure 1 are:

- Embedded power elements
- The ramp for the slope compensation avoiding subharmonic instability
- A transconductance error amplifier with integrated compensation network
- The high-side current sense amplifier to sense the inductor current
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start block ramps up the reference voltage on error amplifier thus decreasing the inrush current at power-up. The EN pin inhibits the device when driven low
- The EN/CLK pin section, which, for LNM versions, allows synchronizing the device to an external clock generator
- The pulse-by-pulse high side / low-side switch current sensing to implement the constant current protection
- A circuit to implement the thermal protection function
- The OVP circuitry to discharge the output capacitor in case of overvoltage event

6.1 Enable

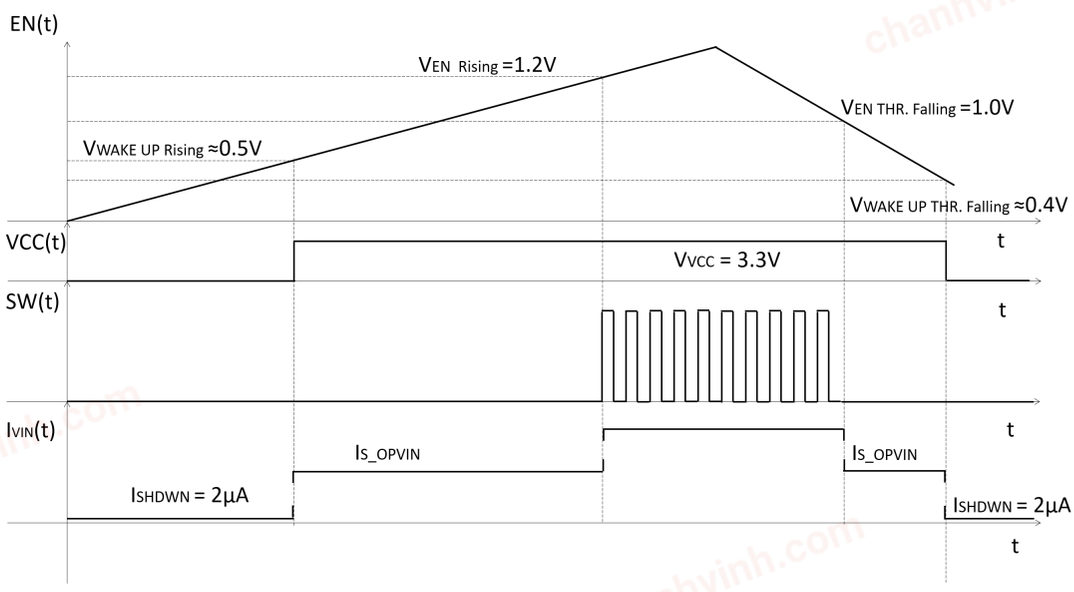
The EN pin is a digital input that turns the device on or off.

In order to maximize both the EN threshold accuracy and the current consumption, the device implements two different thresholds:

1. The Wake-Up threshold, V_{WAKE_UP} = 0.5 V (see Table 6)
2. The Start-Up threshold, V_{EN} = 1.2 V (see Table 6)

The following picture shows the device behavior.

Figure 4. Power up/down behavior



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When the voltage applied on the EN pin rises over $V_{WAKEUP, RISING}$, the device power up the internal circuit increasing the current consumption.

As soon as the voltage rises over the $V_{EN, RISING}$, the device starts the switching activities as described on Section 6.2 Soft-start.

Once the voltage becomes lower than $V_{EN, FALLING}$, the device interrupts the switching activities.

As soon as the voltage becomes lower than $V_{WAKEUP,FALLING}$, the device power down the internal circuit reducing the current consumption.

The pin is VIN compatible.

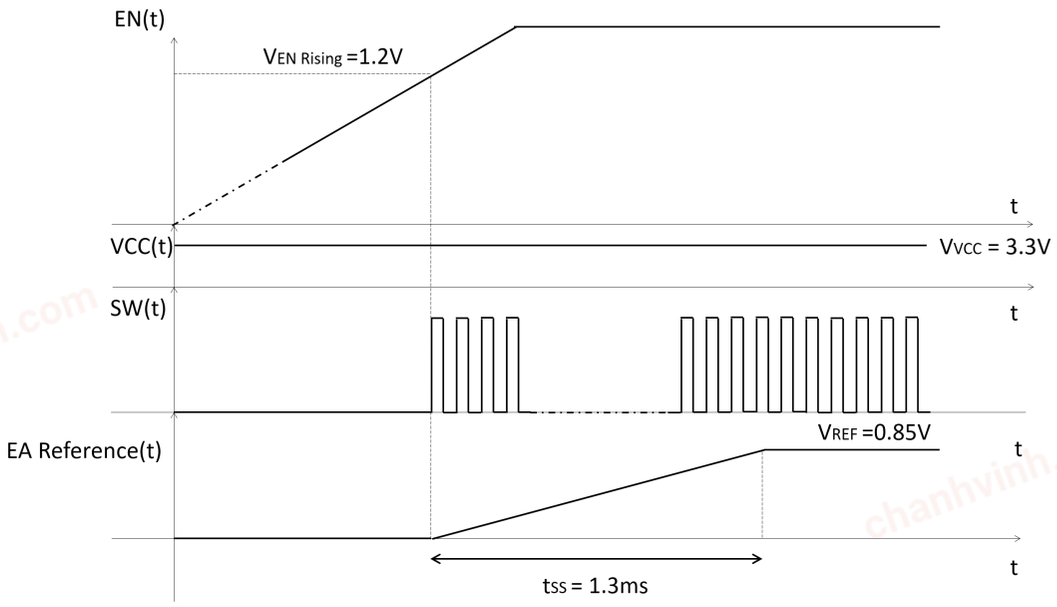
Please refer to the Table 6 for the reported thresholds.

6.2 Soft-start

The soft-start (SS) limits the inrush current surge and makes the output voltage increase monotonically.

The device implements the soft-start phase ramping the internal reference with very small steps. Once the SS ends, the Error Amplifier reference is switched to the internal value of 0.85 V coming directly from the band gap cell.

Figure 5. Soft-start procedure

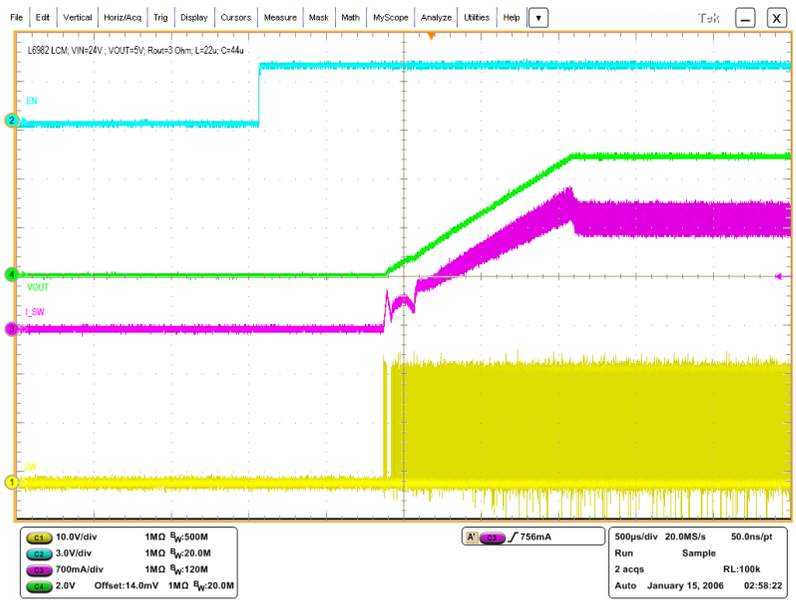


During normal operation, a new soft-start cycle takes place in case of:

1. Thermal shutdown event
2. UVLO event
3. EN pin rising over VEN threshold. Please refer to the Table 6.

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Figure 6. **Soft-start phase with R_{OUT} = 3 Ω**



6.3 Undervoltage lockout

The device implements the undervoltage lockout (UVLO) continuously sensing the voltage on the VCC pin, if the UVLO lasts more than 10 µs, the internal logic resets the device by turning off both LS and HS.

After the reset, if the EN pin is still high, the device repeats the soft-start procedure.

6.4 Light-load operation

The L6982 implements two different light load strategies:

1. Low consumption mode (LCM).
2. Low noise mode (LNM).

Please refer to Table 11 to select the part number with the preferred light load strategy.

6.4.1 Low consumption mode (LCM)

The LCM maximizes the efficiency at light-load.

When the switch peak current request is lower than the ISKIP threshold (please refer to Table 6), the device regulates V_{OUT} by the skip threshold. The minimum voltage is given by:

$$V_{OUT,\ LCM} = V_{FB,\ LCM} \cdot \frac{R_{PH} + R_{PL}}{R_{PL}} \quad (1)$$

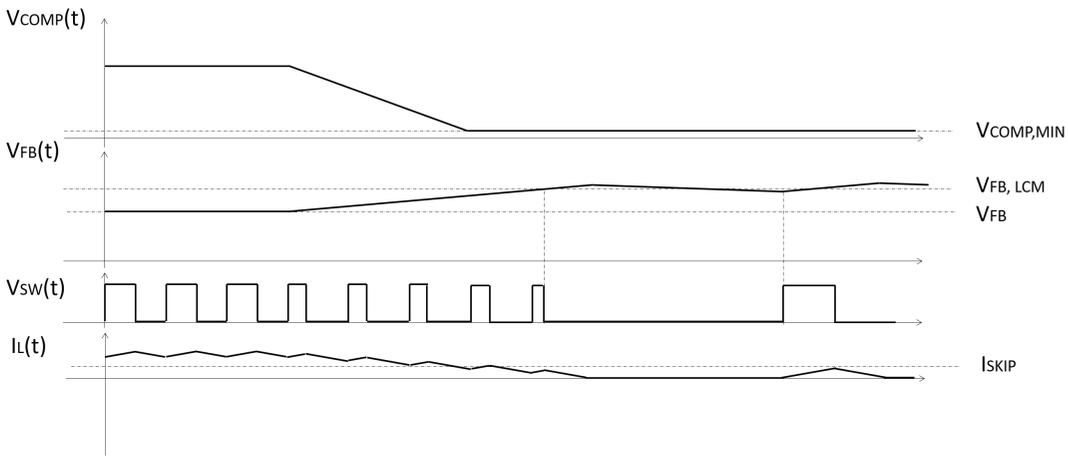
Where $V_{FB,\ LCM}$ is 1.8% (typ.) higher than V_{FB}.

The device interrupts the switching activities when two conditions happen together:

1. The peak inductor current required is lower than I_{SKIP}.
2. The voltage on the FB pin is higher than $V_{FB,\ LCM}$.

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Figure 7. **Light load operation**



A new switching cycle takes place once the voltage on the FB pins becomes lower than $V_{FB,LCM}$.

The HS switch is kept on until the inductor current reaches I_{SKIP}.

Once the current on the HS reaches the defined value, the device turns the HS off and turns the LS on. The LS is kept enabled until one of the following conditions occurs:

1. The inductor current sensed by the LS becomes equal to zero.
2. The switching period ends.

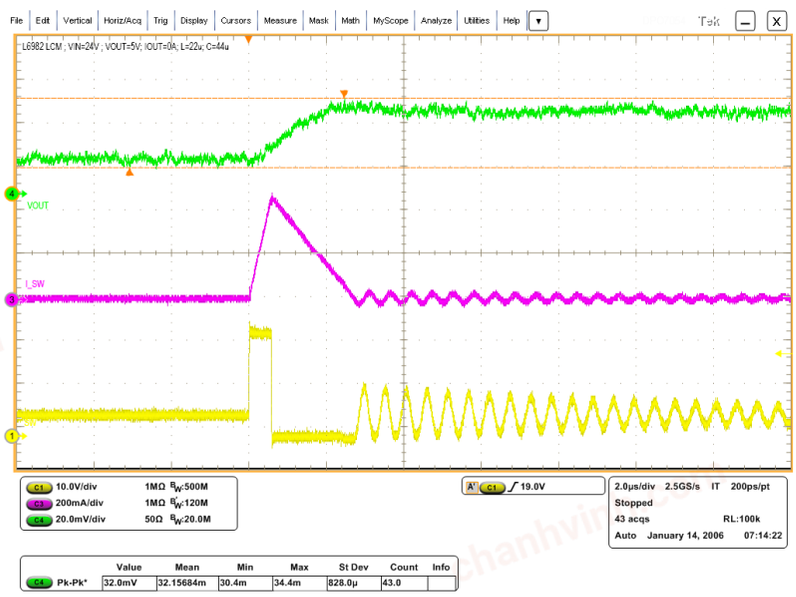
If, at the end of the switching cycle, the voltage on the FB pin rises over the $V_{FB,LCM}$ threshold, the LS is kept enabled until the inductor current becomes equal to zero. Otherwise, the device turns on again the HS and starts a new switching pulse.

During the burst pulse, if the energy transferred to C_{OUT} increases the VFB level over the threshold defined on Equation 1, the device interrupts the switching activities. The new cycle takes place only when VFB becomes lower than the defined threshold. Otherwise, as soon as the LS is turned off the HS is turned on.

Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

$$V_{OUT\ RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^{T_{BURST}} (I_L(t))dt}{C_{OUT}} \quad (2)$$

Figure 8. **LCM operation with I_{SKIP} = 40 mA typ. at zero load. L = 22 µH; C_{OUT} = 44 µF**

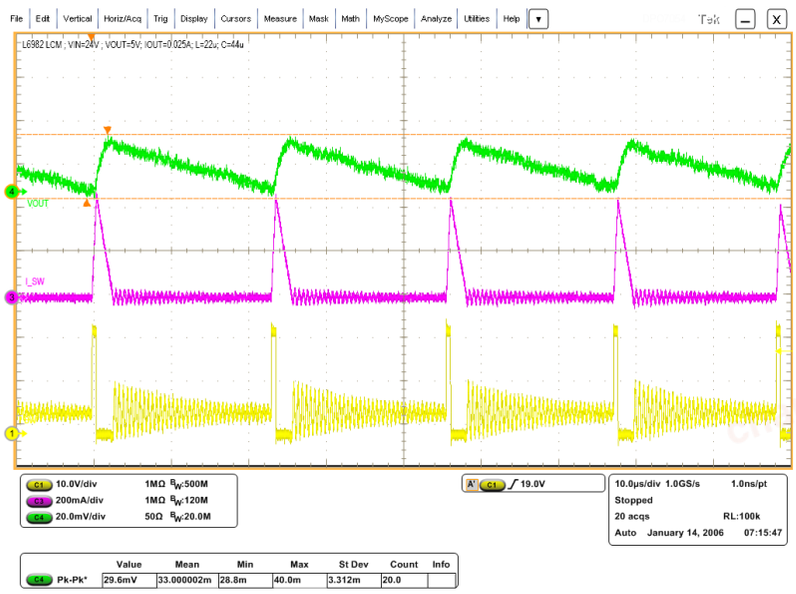


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Figure 9. **LCM operation over loading condition (part 1-pulse skipping)**



Figure 10. **LCM operation over loading condition (part 2-pulse skipping)**



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Figure 11. **LCM operation over loading condition (part 3-pulse skipping)**

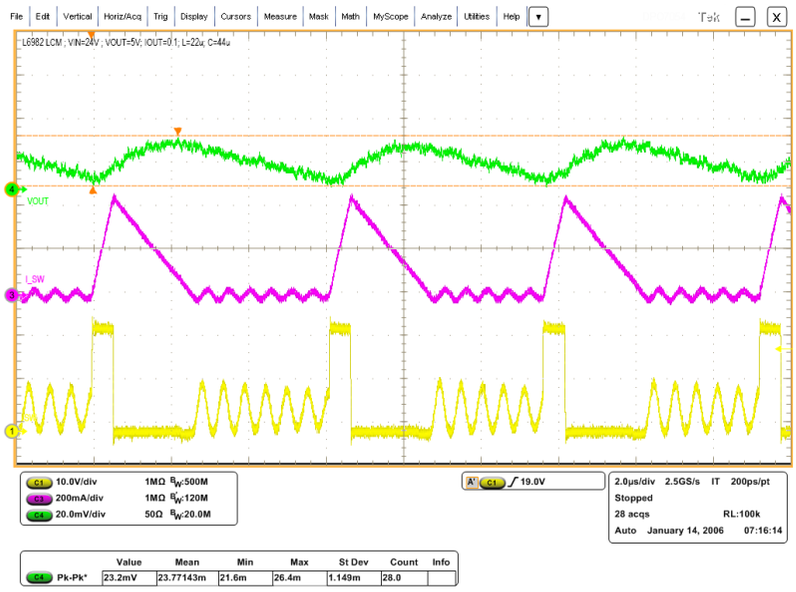
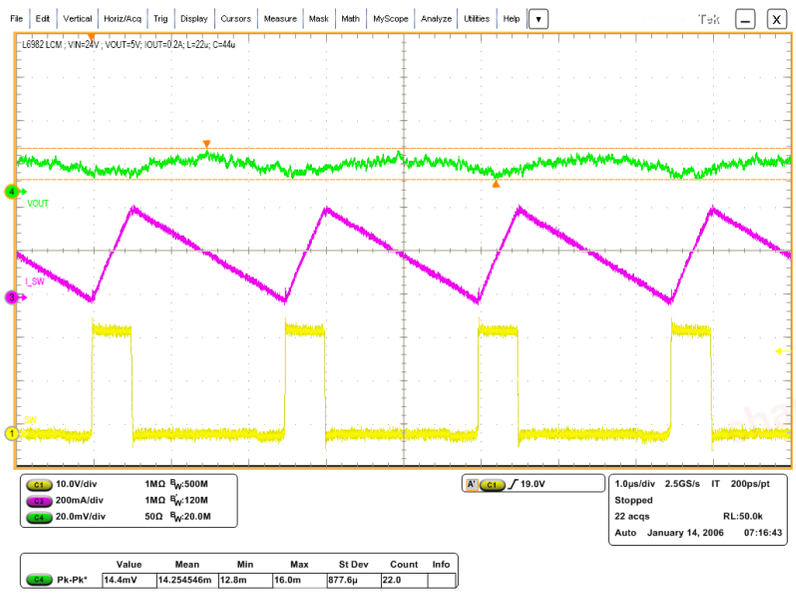


Figure 12. **LCM operation over loading condition (part 4-CCM)**



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6.4.2 Low noise mode (LNM)

The low noise mode implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed VIN.

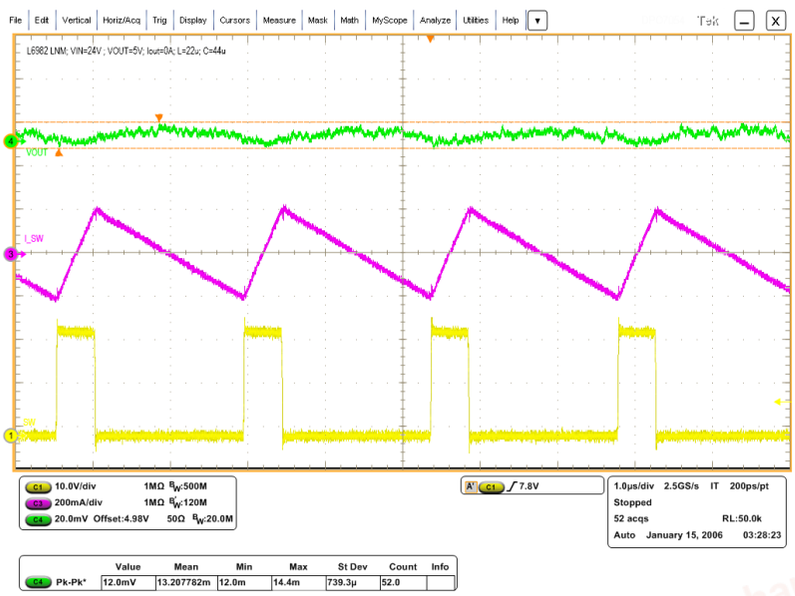
The regulator in steady loading condition operates in continuous conduction mode (CCM) over the different loading conditions.

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). Consequently, the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

$$V_{OUT\ RIPPLE} = ESR \cdot \Delta I_{LMAX} + \frac{\Delta I_{LMAX}}{8 \cdot C_{OUT} \cdot f_{SW}} \quad (3)$$

Usually the resistive component of the ripple can be neglected if the selected output capacitor is a multi-layer ceramic capacitor (MLCC).

Figure 13. Low noise mode operation at zero load



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6.4.3 Efficiency for Low consumption mode and Low noise mode part number

Figure belows report the efficiency measurements to highlight the gap at the light-load between LNM and LCM part numbers. The graph reports also the same efficiency at the medium / high load.

Figure 14. Light-load efficiency for low consumption mode and low noise mode - linear scale

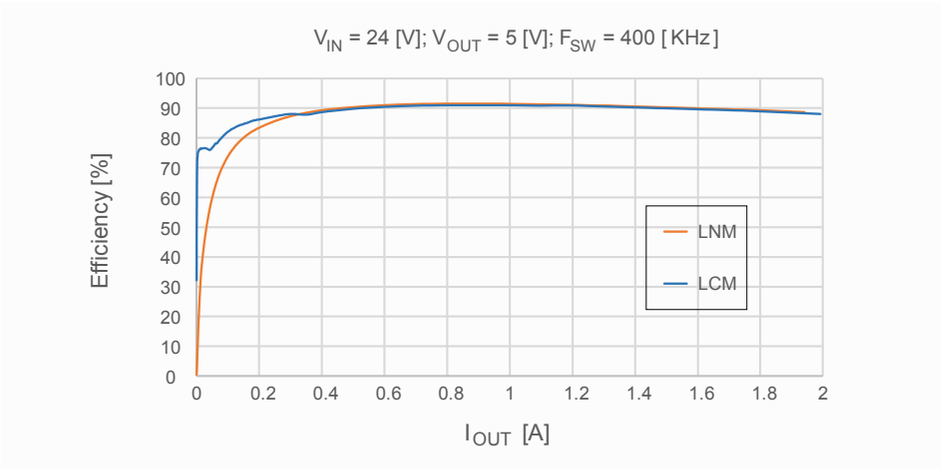
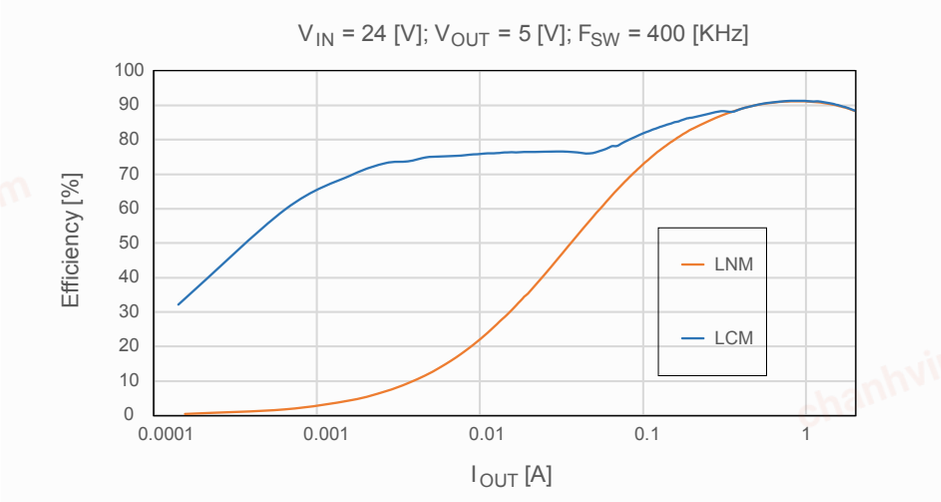


Figure 15. Light-load efficiency for low consumption mode and low noise mode - log scale



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6.4.4 Load regulation for low consumption mode and low noise mode part number

Figure belows report the load regulation to highlight the gap, given by the different regulation strategy, at the light-load between LNM and LCM part numbers. When the required I_{OUT} is higher than the threshold defined in the Low consumption mode (LCM) paragraph, the behavior of the different part numbers is the same.

Figure 16. Load regulation for LCM and LNM. V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 400 KHz - linear scale

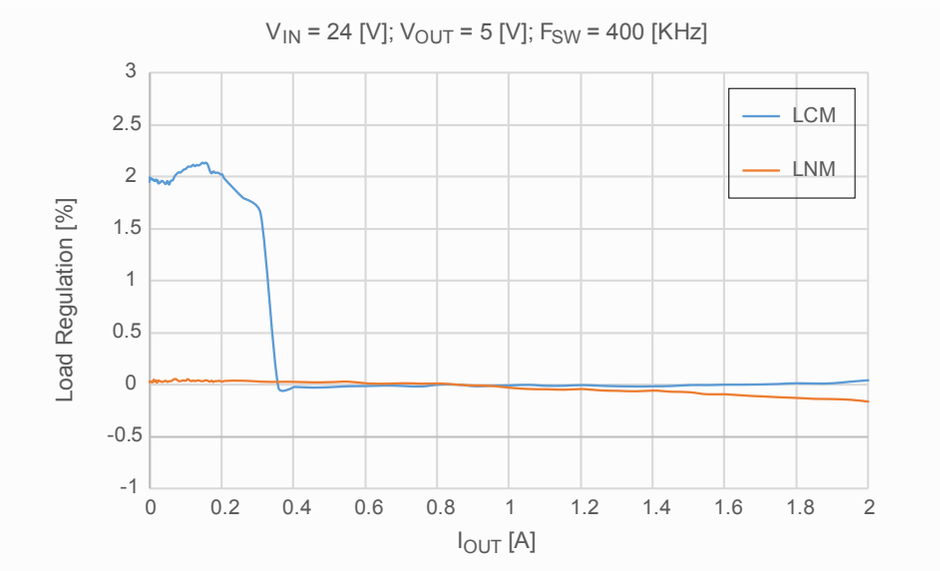
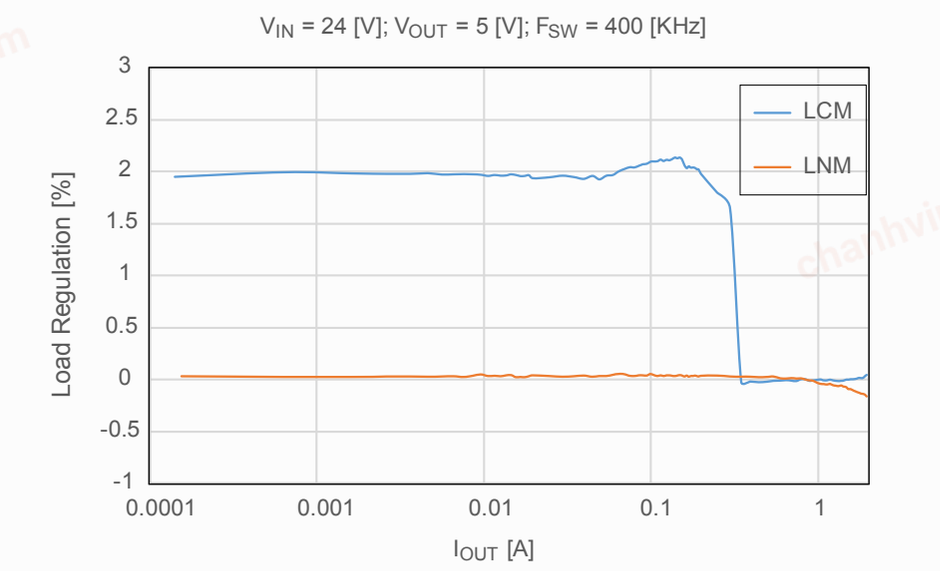


Figure 17. Load regulation for low noise mode. V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 400 KHz - log scale



6.5 Overvoltage protection

The overvoltage protection monitors the FB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% (typ.) over the nominal value.

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This is a second level protection and it should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should guarantee an output voltage regulation within the overvoltage threshold even during the worst-case scenario in terms of load transitions. The protection is reliable and able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. Consequently, the output voltage regulation would be affected.

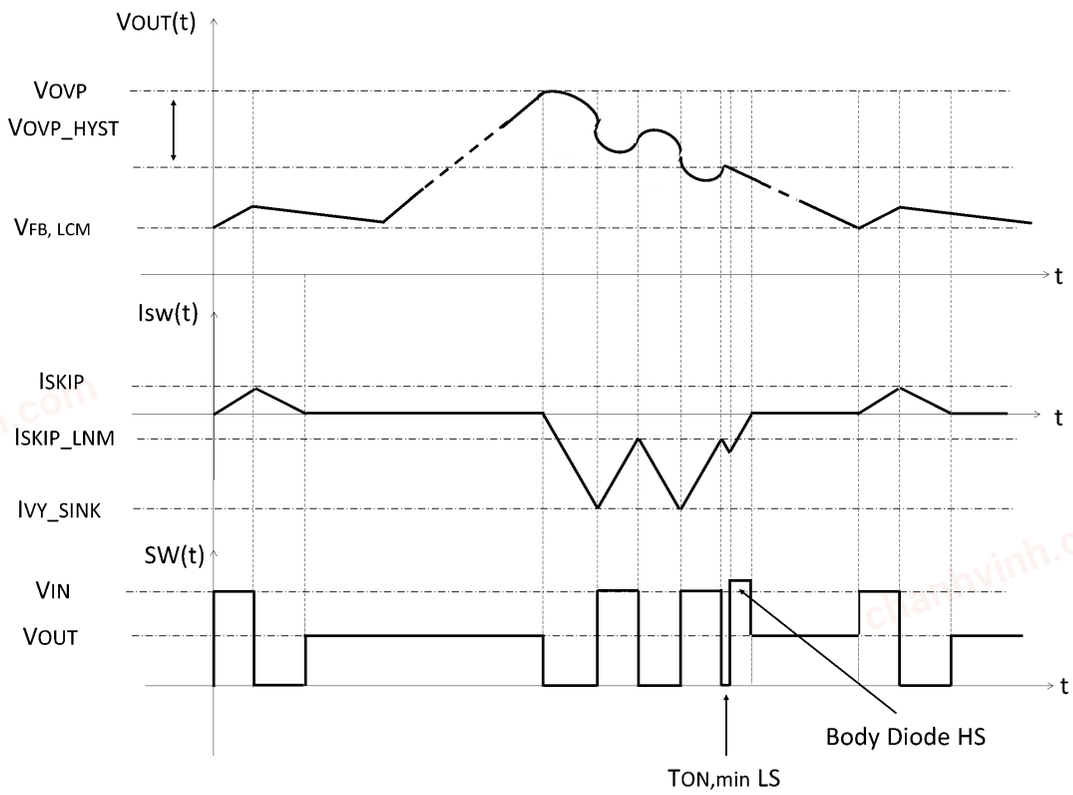
The L6982 device implements a 1.5 A (I_{VY_SINK} refer to Table 6) negative current limitation to limit the maximum reversed switch current during the overvoltage operation.

6.5.1 Low consumption mode part number

The overvoltage protection continuously compares the FB pin with 120% nominal output voltage and enables the low-side MOSFET at the beginning of the switching cycle keeping it active until 1.5 A typ. negative current limitation is reached, in order to discharge the output capacitor.

The following graph shows the LCM part number behavior during an OVP event.

Figure 18. OVP event low noise mode part number



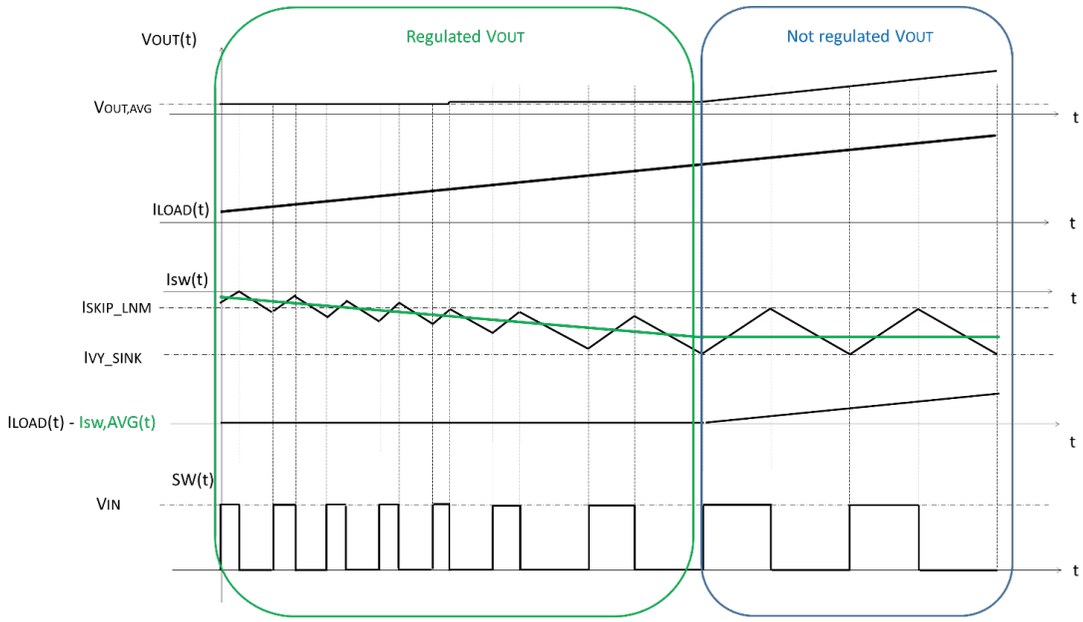
As soon as the output voltage goes out of the OVP hysteresis (typ. 2%) the L6982 device sets the switching node on high impedance. It restarts the switching activity accordingly with the main loop regulation of the peak current mode architecture.

6.5.2 Low consumption mode part number

The following graph shows the LNM part number behavior during an OVP event.

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Figure 19. **OVP event low consumption mode part number**



The LNM device regulates the output voltage with valley sinking capability down to the negative current limitation (IVY_SINK in Figure OVP Event Low Noise Mode part number). This hysteretic operating mode between peak current mode threshold (ISKIP_LNM) and modulated low side switch conduction time for VOUT regulation persists until the valley current level triggers the negative current limitation (IVY_SINK), that is the maximum sinking capability of the device (highlighted in green in figure above).

If the source injection further increases, the output voltage is a partitioning between source impedance and maximum sinking capability above described (highlighted in blue in figure above).

6.6 Over current protection

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (please refer to Table 6) in an overcurrent condition.

The L6982 device implements a pulse-by-pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak”, the low-side sensing “valley”.

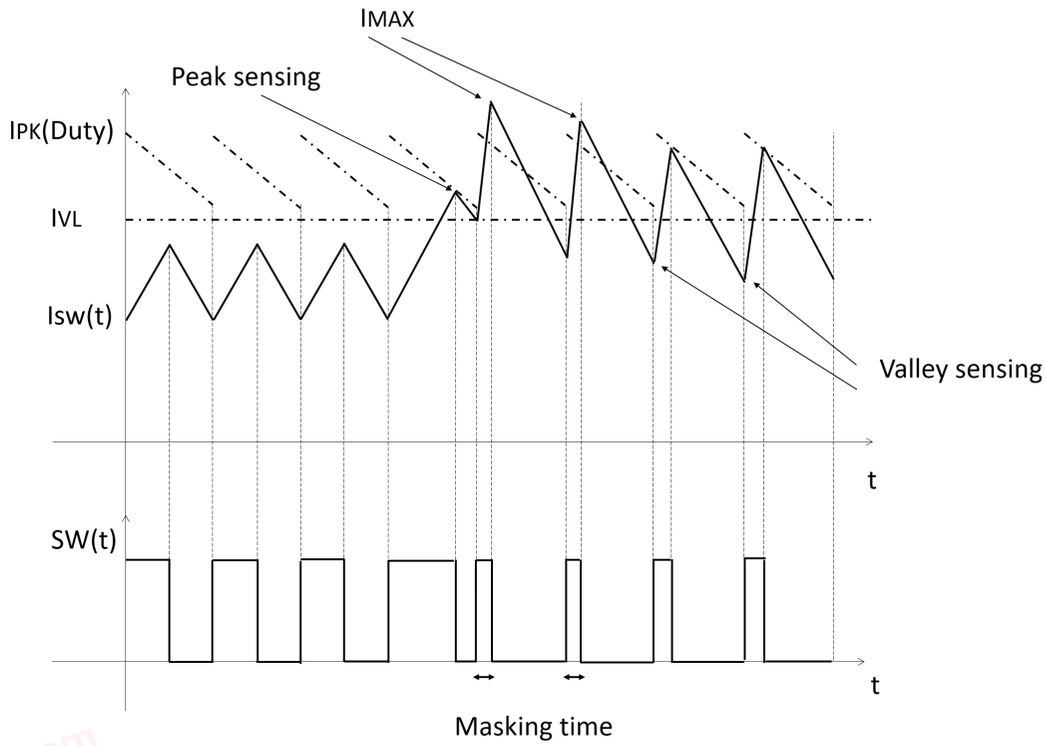
The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. Therefore, the peak current protection is disabled for a masking time after the high-side switch is turned on. The masking time for the valley sensing is activated after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, the valley current protection at extremely high duty cycles.

The L6982 device assures an effective overcurrent protection sensing the current flowing in both power elements. In case one of the two current sensing circuitries is ineffective because of the masking time, the device is protected, sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits assure the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

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In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. The low-side operation is able to prevent the high-side turn-on, so the device can skip pulses decreasing the switching frequency.

Figure 20. Over current protection behavior



In a worst case scenario, reported in Figure 20 of the overcurrent protection, the switch current is limited to:

$$I_{MAX} = I_{VY} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{MASKHS} \quad (4)$$

Where IVY is the current threshold of the valley sensing circuitry (please refer to Electrical characteristics table) and T_{MASKHS} is the masking time of the high-side switch.

In most of the overcurrent conditions, the conduction time of the high-side switch is higher than the masking time and so the peak current protection limits the switch current.

$$I_{MAX} = I_{PEAKTH} \quad (5)$$

The DC current flowing in the load in overcurrent condition is:

$$I_{DCOUT} = I_{MAX} - \frac{I_{RIPPLE}(V_{OUT})}{2} = I_{MAX} - \left(\frac{V_{IN} - V_{OUT}}{2 \cdot L} \cdot T_{ON}\right) \quad (6)$$

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Figure below shows the L6982 soft-start procedure with V_{OUT} shorted to GND.

Figure 21. Soft-start procedure with VOUT shorted to GND

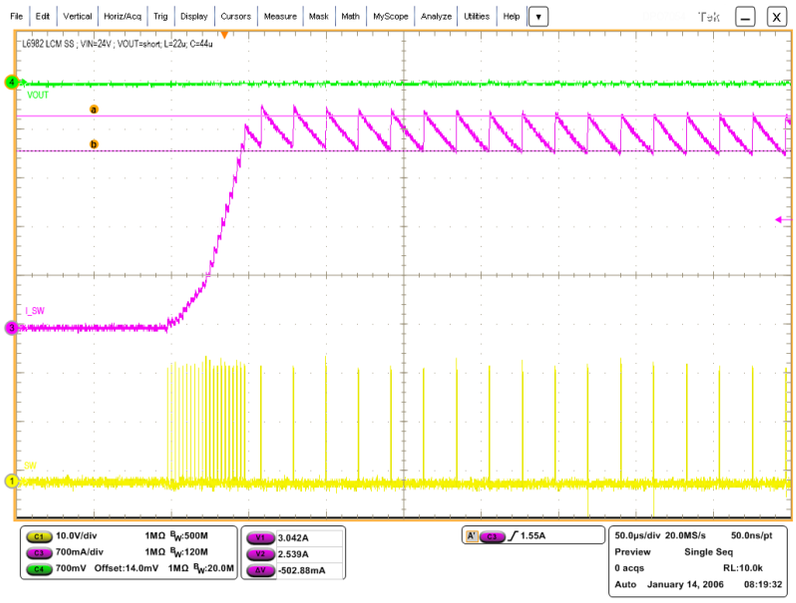
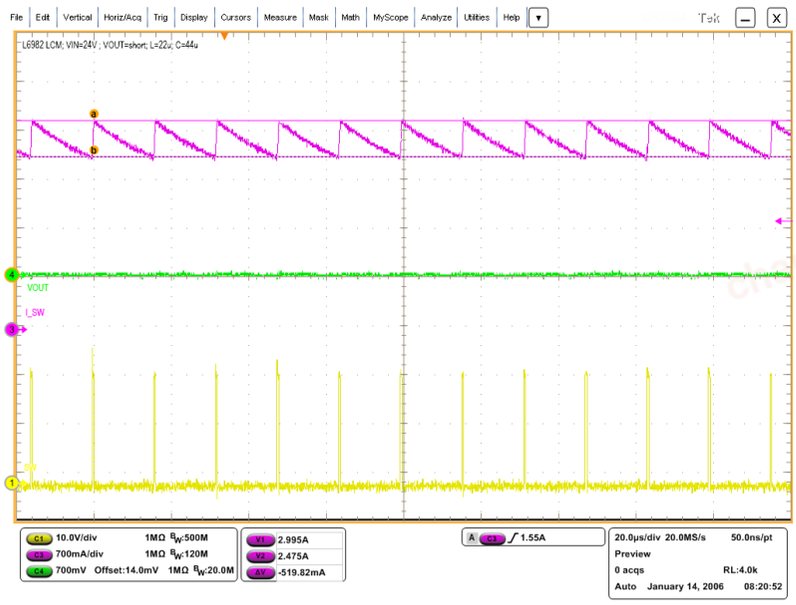


Figure below shows the L6982 over current protection with a persistent short-circuit between V_{OUT} and GND.

Figure 22. Over current procedure with persistent short circuit between V_{OUT} and GND



6.7 Thermal shutdown

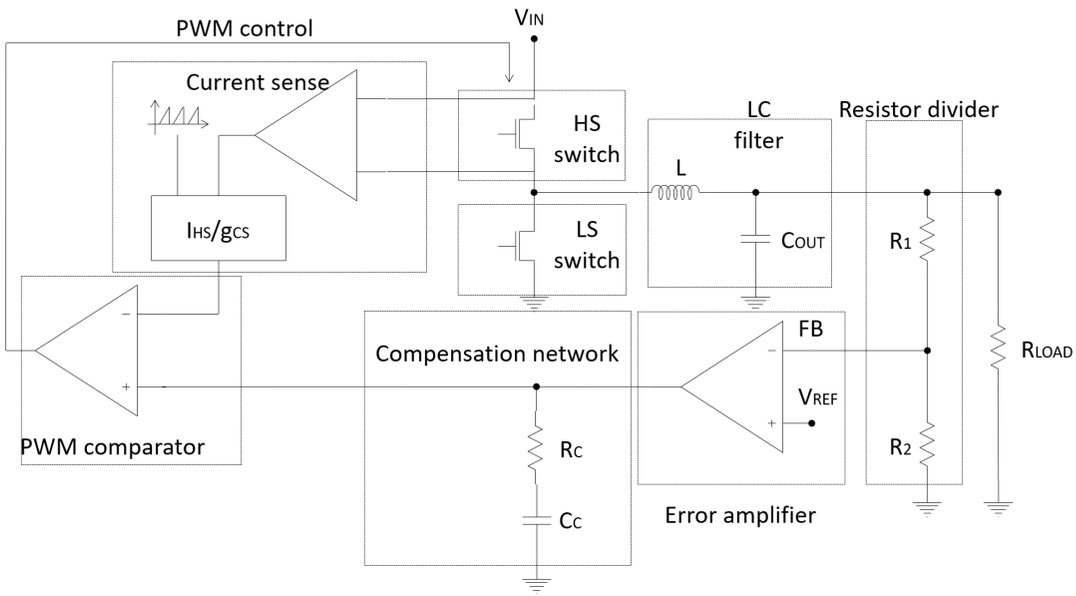
The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (T_{SHDWN} refer to Table 6). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately 30 °C prevents the device from turning ON and OFF too fast. After a thermal protection event is expired the L6982 restarts with a new soft-start.

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7 Closing the loop

The following pictures shows the typical compensation network required to stabilize the system.

Figure 23. Block diagram of the loop



7.1 GCO(s) control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

$$G_{CO}(s) = R_{LOAD} \cdot g_{CS} \cdot \frac{1}{1 + \frac{R_{LOAD} \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \cdot F_H\left(s\right) \quad (7)$$

Where R_{LOAD} represents the load resistance, g_{CS} the equivalent sensing trans-conductance of the current sense circuitry, ωP the single pole introduced by the power stage and ωZ the zero given by the ESR of the output capacitor. F_H (s) accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}} \quad (8)$$

$$\omega_P = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}} \quad (9)$$

Where:

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = I_{SLOPE} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases} \quad (10)$$

Where I_{SLOPE} is equal to 1 A.

S_n represents the ON time slope of the sensed inductor current, Se the ON time slope of the external ramp that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50 %.

The sampling effect contribution F_H (s) is:

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$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}} \quad (11)$$

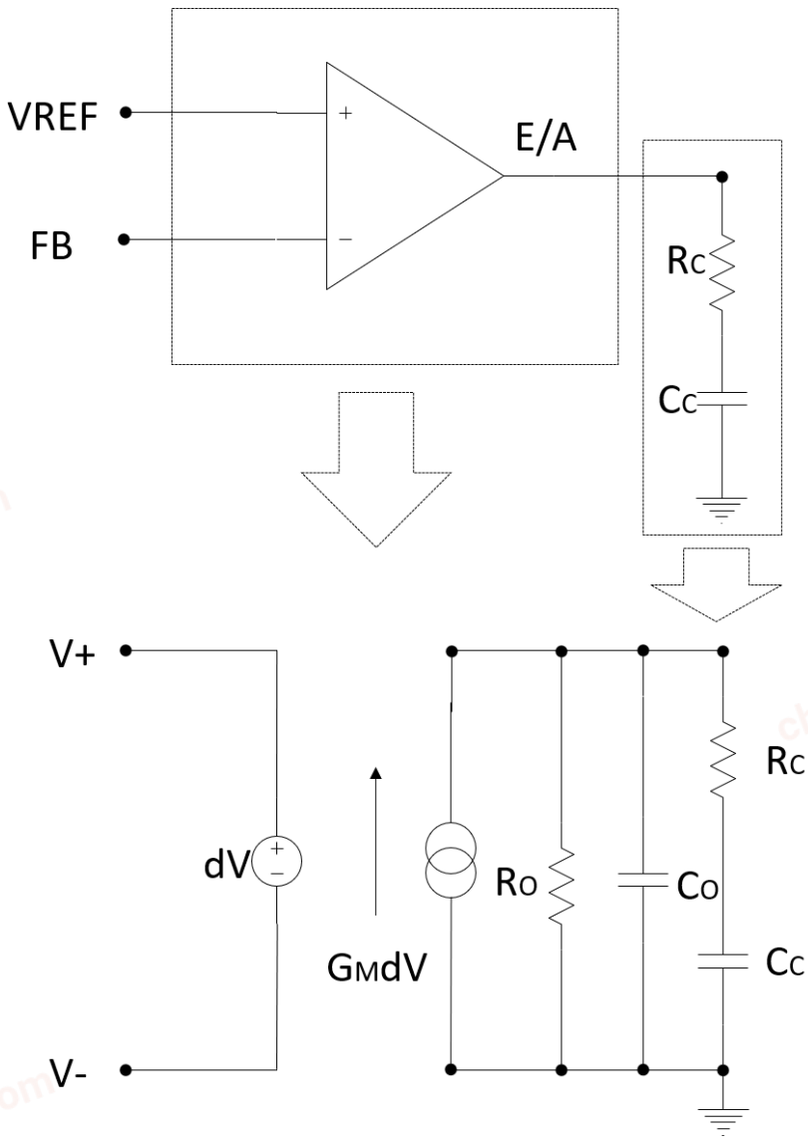
Where:

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]} \quad (12)$$

7.2 Error amplifier compensation network

The following figure shows the typical compensation network required to stabilize the system.

Figure 24. Trans-conductance embedded error amplifier



RC and CC introduce a pole and a zero in the open loop gain. The transfer function of the error amplifier and its compensation network is:

$$A_O(s) = \frac{A_{VO} \cdot (1 + s \cdot R_C \cdot C_C)}{s^2 \cdot R_O \cdot C_O \cdot R_C \cdot C_C + s \cdot (R_O \cdot C_C + R_O \cdot C_O + R_C \cdot C_C) + 1} \quad (13)$$

Where:

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$$A_{VO} = G_m \cdot R_O \tag{14}$$

The poles of this transfer function are (if C_C » C_O):

$$f_{PLF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_C} \tag{15}$$

$$f_{PHF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_O} \tag{16}$$

Whereas the zero is defined as:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C} \tag{17}$$

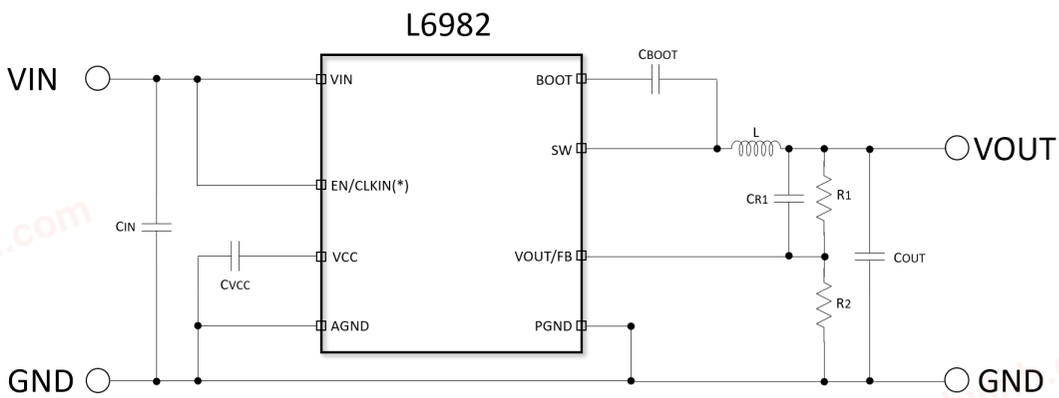
7.3 Voltage divider

The contribution of a simple voltage divider is:

$$G_{DIV}\left(s\right) = \frac{R_2}{R_1 + R_2} \tag{18}$$

A small signal capacitor in parallel to the upper resistor (only for the adjustable part number) of the voltage divider implements a leading network (f_{ZERO} < f_{POLE}), sometimes necessary to improve the system phase margin:

Figure 25. Leading network example



(*) Synchronization is allowed for LNM versions only.

Laplace transformer of the leading network:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{(1 + s \cdot R_1 \cdot C_{R1})}{\left(1 + s \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}\right)} \tag{19}$$

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{R1}} \tag{20}$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}} \tag{21}$$

$$f_Z < f_P \tag{22}$$

So closing the loop, the loop gain is:

$$G(s) = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_O(s) \tag{23}$$

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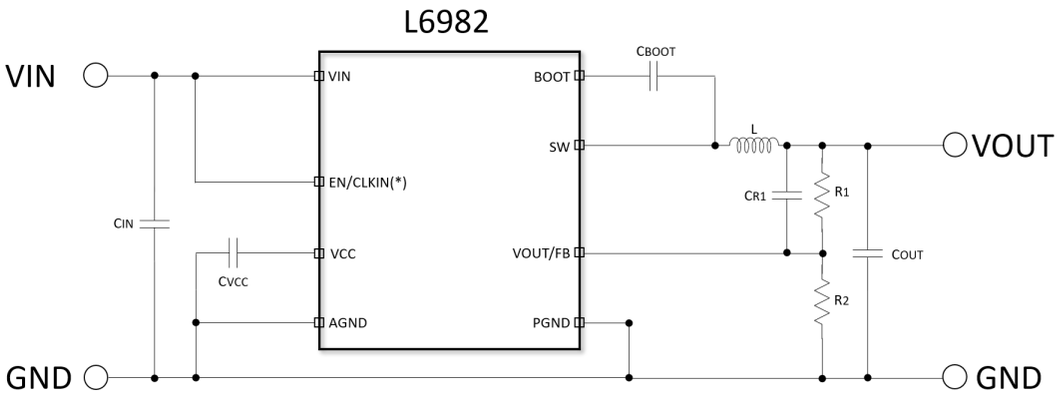
8 Application notes

8.1 Programmable power up threshold

The Enable rising threshold is equal to 1.2 V typical (refer to Table 6). The power up threshold is adjusted accordingly with the following equation:

$$V_{Power\ Up} = 1.2 \cdot \left(1 + \frac{R_{EN\ H}}{R_{EN\ L}}\right) \quad (24)$$

Figure 26. Leading network example



(*) Synchronization is allowed only for LNM versions.

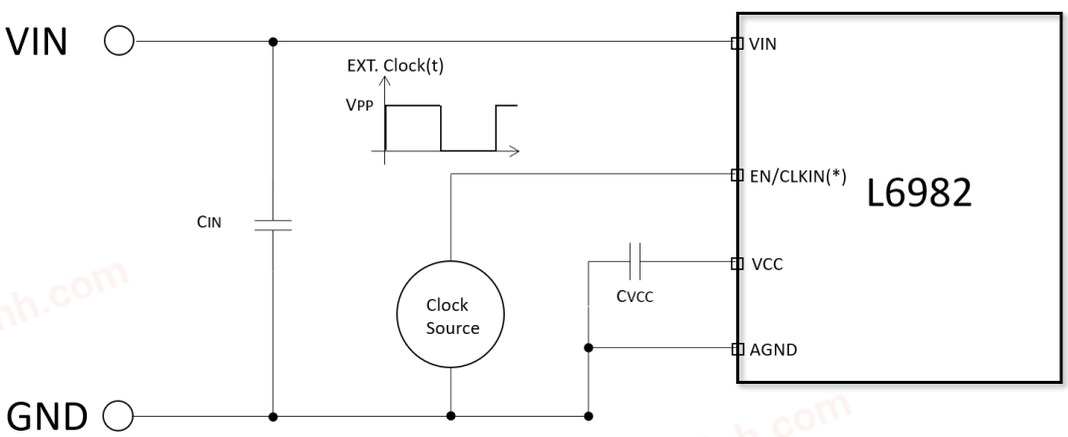
The Enable falling threshold is equal to 1.0 V typical (refer to Electrical characteristics table). The turn off threshold is obtained accordingly with the following equation:

$$V_{Power\ Down} = 1.0 \cdot \left(1 + \frac{R_{EN\ H}}{R_{EN\ L}}\right) \quad (25)$$

8.2 External synchronization (only available for Low Noise Mode)

The device allows a direct connection between a clock source and the EN/CLKIN pin.

Figure 27. External synchronization. Direct connection



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The device internally implements a low pass filter connected to EN/CLKIN pin that is able to acquire the average value of the applied signal.

The device turns on when the average of the signal applied is higher than V_{EN} rising (refer to Table 6). The device turns off when the average of the signal should be lower than V_{EN} falling (refer to Table 6).

Considering, for example, a clock source with V_{PP} = 5.0 V, the minimum duty cycle to guarantee the power-up is given by:

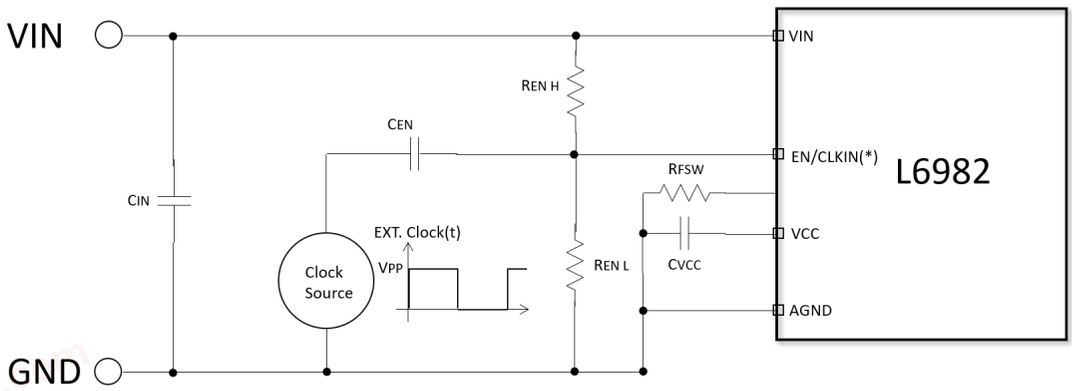
$$Duty_{min} = \frac{V_{EN,TH\ Rising}}{V_{PP}} = 0.24 \quad (26)$$

The maximum duty cycle to guarantee the turn off is given by:

$$Duty_{MAX,} = \frac{V_{EN,TH\ Falling}}{V_{PP}} = 0.2 \quad (27)$$

The device allows also the AC coupling.

Figure 28. External synchronization. AC coupling



(*) Synchronization is allowed only for LNM versions.

The AC-coupling allows the device to keep the power-up and down thresholds defined by the partition connected to the EN/CLKIN pin and described in the "Programmable power up threshold" section.

The following table resumes the minimum pulse duration and maximum duty cycle that allow the synchronization, keeping the selected power-up and down thresholds.

Table 7. External synchronization AC coupling suggested operation range

V_{PP} [V]	$T_{ON,MIN}$ [ns]	D_{MAX} [%]
2.3	70	45
3.3	20	30
5	20	20

The minimum amplitude for the external clock signal is, for both the configurations, equal to 2.3 V.

The network given by C_{EN} and R_{ENL} sets a high pass filter. Considering a resistor in the order of 220 KΩ, a capacitor equal to 1 nF is a correct choice.

8.3 Output voltage adjustment

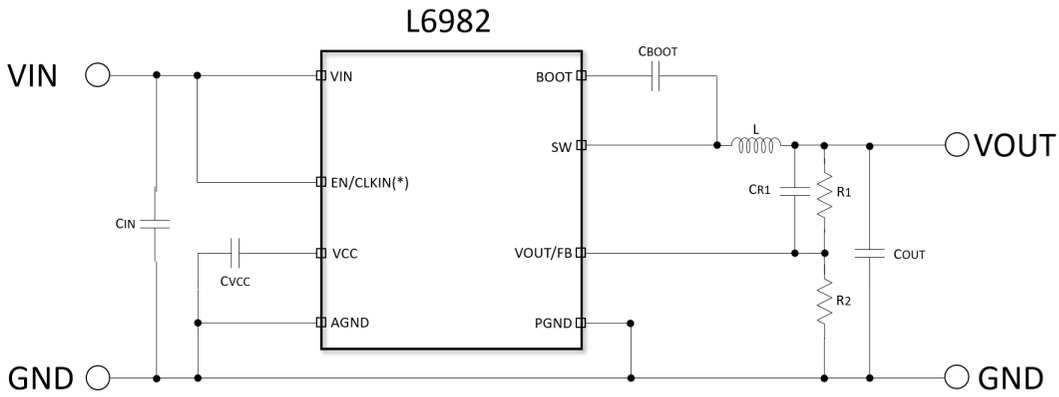
The error amplifier reference voltage is 0.85 V typical (refer to Table 6). The output voltage is adjusted accordingly with the following equation:

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$$V_{OUT} = 0.85 \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (28)$$

CR1 capacitor is sometimes useful to increase the small signal phase margin (please refer to the section Closing the loop)

Figure 29. Application circuit



8.4 Design of the power components

8.4.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so, its RMS current capability must be selected accordingly with the application conditions. Internal losses of the input filter depend on the ESR value, so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$I_{RMS} = I_{OUT} \cdot \sqrt{\left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta}} \quad (29)$$

Where I_{OUT} is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to $I_{OUT}/2$. In a specific application, the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INmin} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}} \quad (30)$$

$$D_{min} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMAX} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}} \quad (31)$$

Where $\Delta V_{HIGHSIDE}$ and $\Delta V_{LOWSIDE}$ are the voltage drops across the embedded switches. The peak to peak voltage across the input filter can be calculated as:

$$V_{PP} = \frac{I_{OUT}}{C_{IN} \cdot F_{SW}} \cdot \left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta} + ESR \cdot (I_{OUT} + \Delta I_L) \quad (32)$$

In case of negligible ESR (MLCC capacitor), the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

$$C_{IN} = \frac{I_{OUT}}{V_{PP} \cdot F_{SW}} \cdot \left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta} \quad (33)$$

Considering η = 1 this function has its maximum in D = 0.5:

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$$C_{INmin} = \frac{I_{OUT}}{4 \cdot V_{PPMAX} \cdot F_{SW}} \quad (34)$$

Typically, C_{IN} is dimensioned to keep the maximum peak-to-peak voltage across the input filter in the order of 5 % V_{INMAX}.

In the following table, some suitable capacitor part numbers are listed.

Table 8. Input capacitors

Manufacturer	Series	Size	Cap value (µF)	Rated voltage (V)
TDK	CGA5L3X5R1H106K160AB	1206	10	50
	C3216X5R1H106K160AB	1206	10	50
Murata	GRT31CR61H106KE01	1206	10	50

8.4.2 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple. Usually the inductor value is selected in order to keep the current ripple lower than 20% - 40% of the output current over the input voltage range. The inductance value can be calculated by the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF} \quad (35)$$

Where T_{ON} and T_{OFF} are the on and off time of the internal power switch. The maximum current ripple, at fixed V_{OUT}, is obtained at maximum T_{OFF} that is at minimum duty cycle. So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

$$L_{min} = \frac{V_{OUT}}{\Delta IL_{MAX}} \cdot \frac{1 - D_{min}}{F_{SW}} \quad (36)$$

For those applications requiring higher inductor value for minimized current ripple, pay attention as the maximum value must prevent the sub-harmonic instability given the designed internal slope compensation. As a consequence the inductor value must satisfy the quality factor range:

$$0.4 \leq Q_P \leq 1.33 \quad (37)$$

Where QP has been defined on the Section 7.1 GCO(s) control to output transfer function. The peak current through the inductor is given by:

$$I_{L,PK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (38)$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher the inductor value, the higher the average output current that can be delivered, without reaching the current limit.

8.4.3 Output capacitor selection

The triangular shaped current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, which depends on the capacitor value and the equivalent resistive component (ESR). Therefore, the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as:

$$\Delta V_{OUT} = ESR \cdot \Delta I_{L,MAX} + \frac{\Delta I_{L,MAX}}{8 \cdot C_{OUT} \cdot F_{SW}} \quad (39)$$

For a ceramic (MLCC) capacitor, the capacitive component of the ripple dominates the resistive one. While for an electrolytic capacitor the opposite is true. Neglecting the ESR contribution, the minimum value of the output capacitor is given by:

$$C_{OUT,min,RIPPLE} = \frac{\Delta I_{L,MAX}}{8 \cdot \Delta V_{OUT} \cdot F_{SW}} \quad (40)$$

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As the compensation network is internal, the output capacitor should be selected in order to have a proper phase margin and then a stable control loop. A good rule to obtain a proper dimensioning for the minimum amount of the output capacitor is to set the target system bandwidth equal to $F_{SW}/10$. The following equation takes into account the precedent consideration:

$$C_{OUT,BW,min} = \frac{8.04}{\frac{F_{SW}}{8} \cdot V_{OUT}} \quad (41)$$

The maximum amount of the output capacitor is given by:

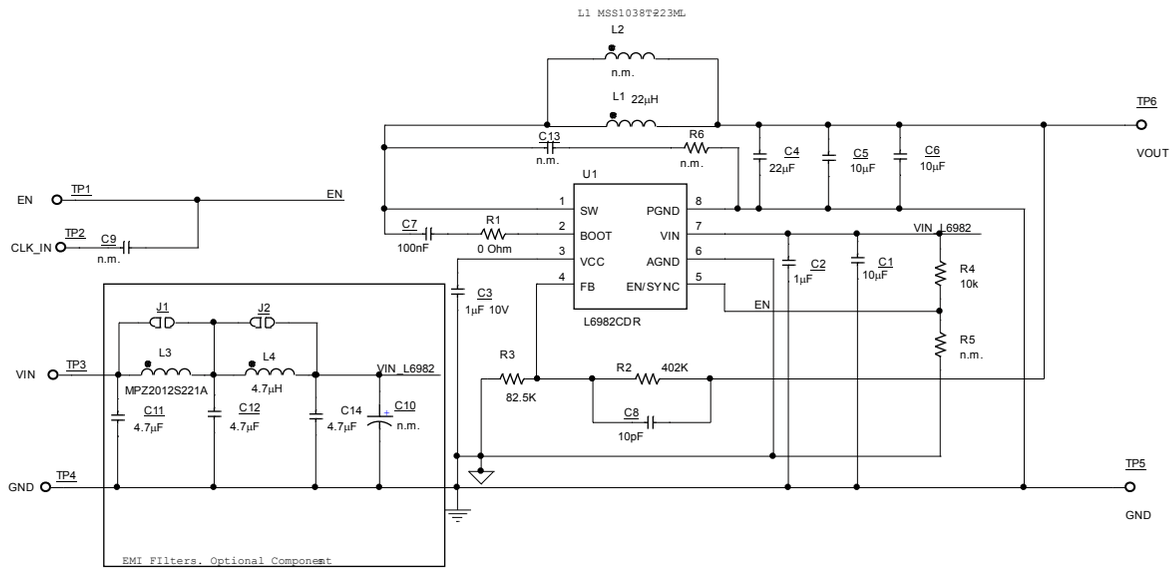
$$C_{OUT,BW,min} = \frac{0.96 \cdot 10^{-3}}{V_{OUT}} \quad (42)$$

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9 Application board

The figure below shows the reference evaluation board schematic:

Figure 30. Evaluation board schematic



The additional input filter (C11, L3, C12, L4, C14 and C10) limits the conducted emission on the power supply.

Table 9. Bill of material

Reference	Part number	Description	Manufacturer
C1	C3216X7R1H106K160AC	10 µF	TDK
C2	CGA4J3X7R1H105K125AB	1 µF	TDK
C3		1 µF	
C4	GRJ32EC71E226KE11	22 µF	Murata
C5, C6	C3216X7R1H106K160AC	10 µF	TDK
C7		100 nF	
C8		10 pF	
C9		n.m.	
C10		n.m.	
C11, C12, C14	GRM31CR71H475KA12	4.7 µF	Murata
C13			
L1	MSS1038T-223ML	22 µH	Coilcraft
L2		n.m.	
L3	MPZ2012S221AT000	220 Ω, 100 MHz	TDK
L4	XAL4030-472ME	4.7 µH	Coilcraft
R1		0 Ω	
R2		402 kΩ	

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Reference	Part number	Description	Manufacturer
R3		82.5 kΩ	
R4		10 kΩ	
R5		n.m	
R6		n.m	
U1	L6982		STMicroelectronics

Figure 31. **Top layer**

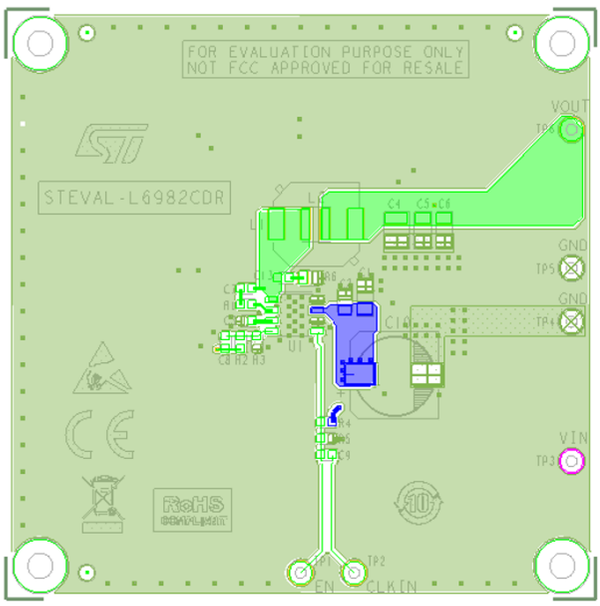
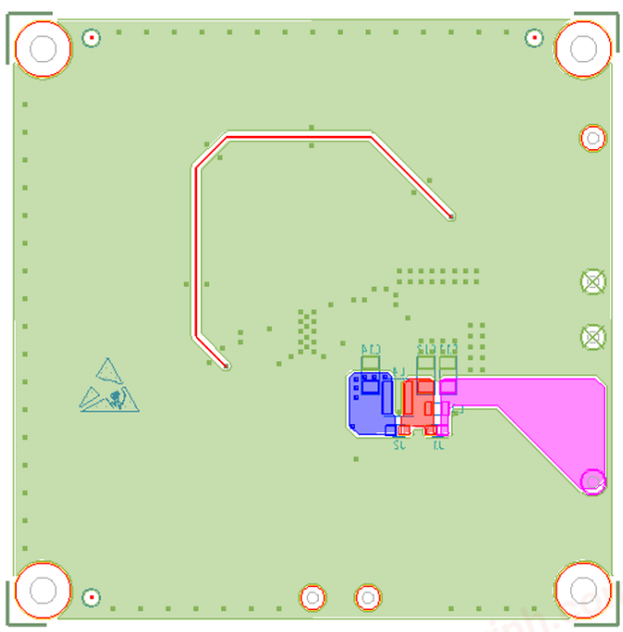


Figure 32. **Bottom layer**



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10 Efficiency curves

The following three figures the efficiency and power losses acquired on the standard evaluation board of the device, selecting the following output filter:

- COUT:
  - 1 x GRJ32EC71E226KE11 22 µF 25 V (Murata)
  - 2 x C3216X7R1H106K160AC 10 µF 50 V (TDK)
- Inductor:
  - MSS1038T-223ML (Coilcraft)
- C8:
  - 10 pF

Figure 33. Efficiency V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ

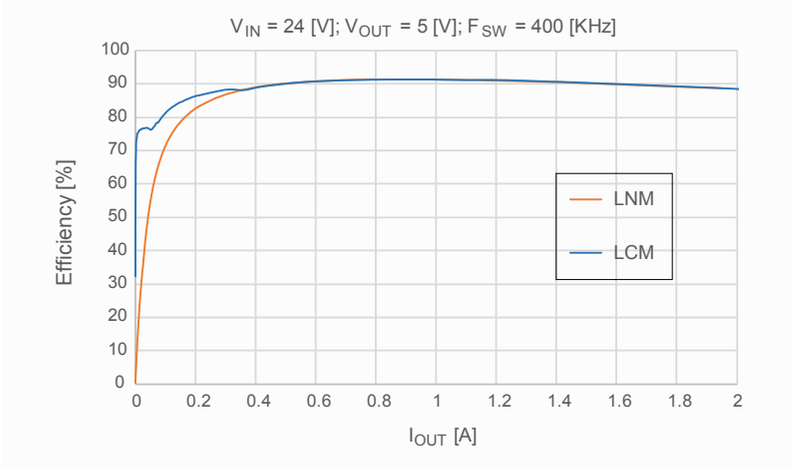
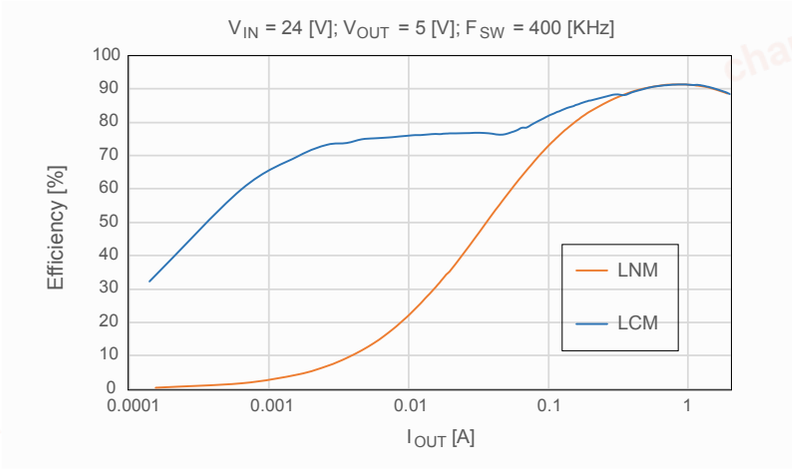
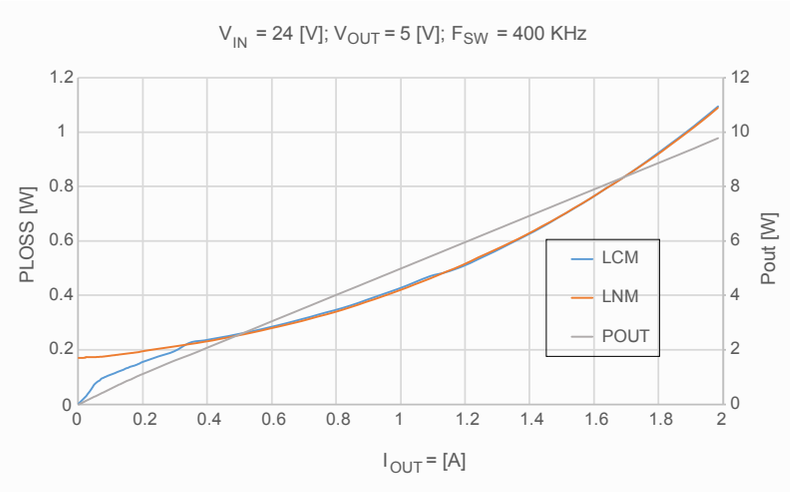


Figure 34. Efficiency V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ (log scale)



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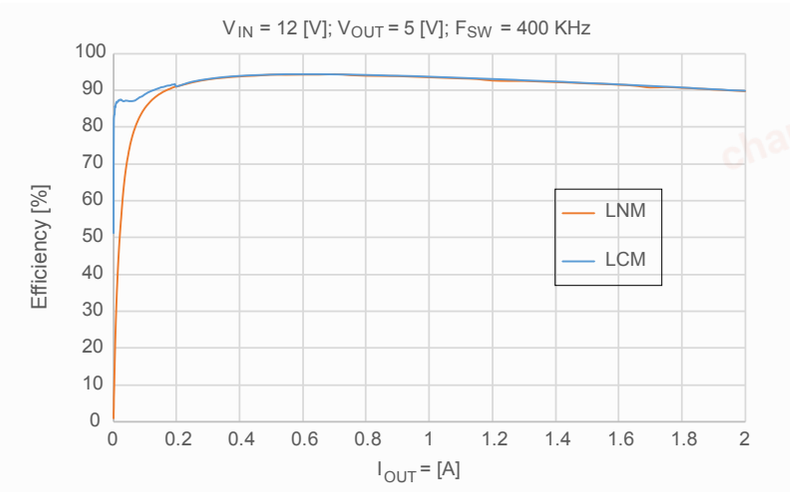
Figure 35. **Power losses V_{IN} = 24 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, selecting the following output filter:

- COUT:
  - 1 x GRJ32EC71E226KE11 22 µF 25 V (Murata)
  - 2 x C3216X7R1H106K160AC 10 µF 50 V (TDK)
- Inductor:
  - MSS1038T-223ML (Coilcraft)
- C8:
  - 10 pF

Figure 36. **Efficiency V_{IN} = 12 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ**



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Figure 37. **Efficiency V_{IN} = 12 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ (log scale)**

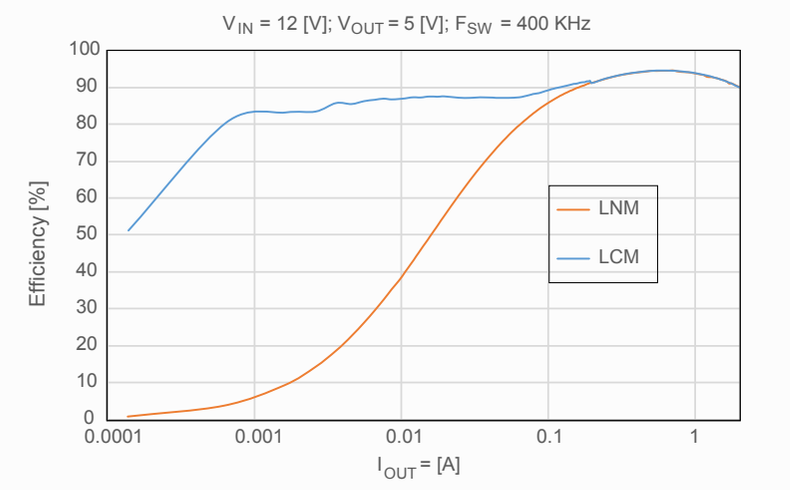
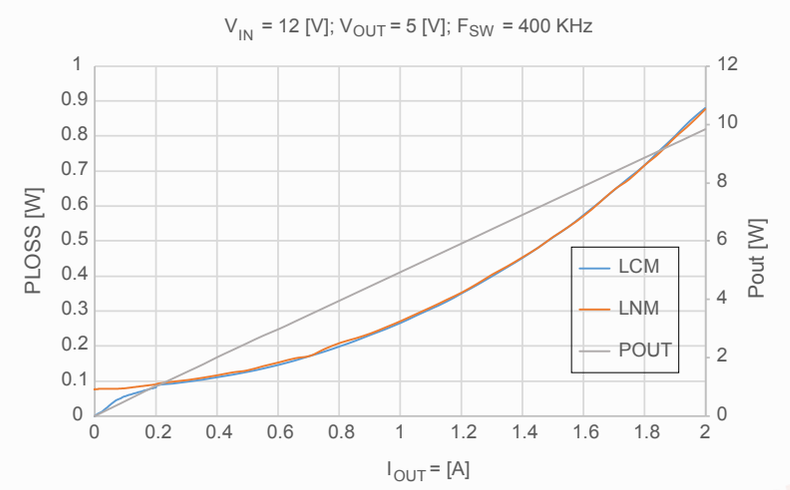


Figure 38. **Power losses V_{IN} = 12 V; V_{OUT} = 5 V; F_{SW} = 0.4 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, selecting the following output filter:

- COUT:
  - 1 x GRJ32EC71E226KE11 22 µF 25 V (Murata)
  - 2 x C3216X7R1H106K160AC 10 µF 50 V (TDK)
- Inductor:
  - MSS1038T-153ML (Coilcraft)
- C8:
  - 10 pF

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Figure 39. **Efficiency V_{IN} = 24 V; V_{OUT} = 3.3 V; FSW = 0.4 MHZ**

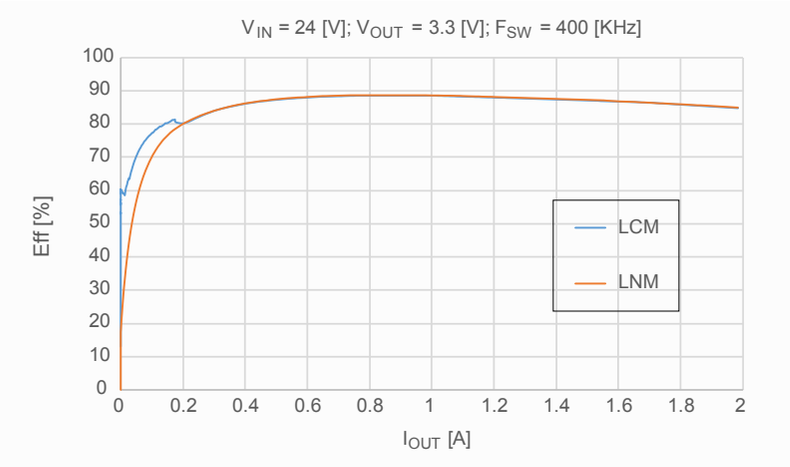


Figure 40. **Efficiency V_{IN} = 24 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ (log scale)**

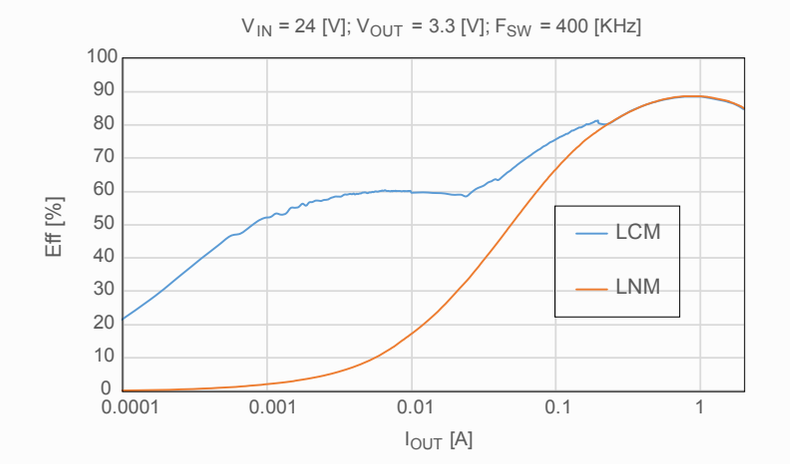
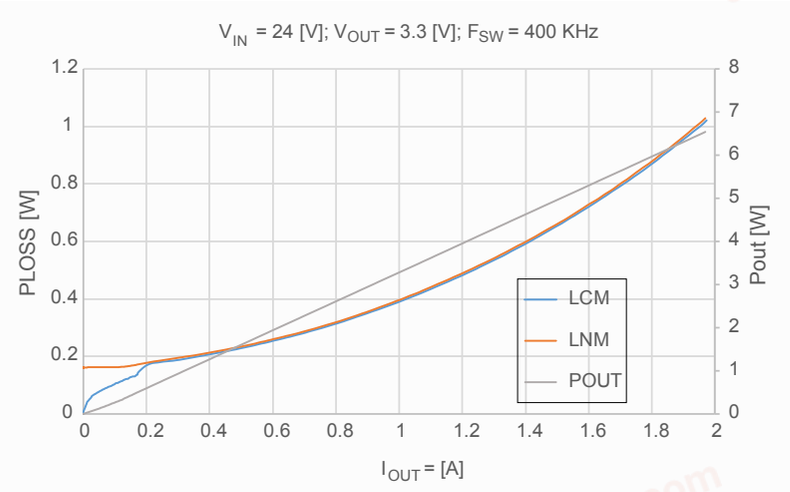


Figure 41. **Power losses V_{IN} = 24 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ**



The following three figures show the efficiency and power losses acquired on the standard evaluation board of the device, selecting the following output filter:

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- COUT:
  - 1 x GRJ32EC71E226KE11 22 µF 25 V (Murata)
  - 2 x C3216X7R1H106K160AC 10 µF 50 V (TDK)
- Inductor:
  - MSS1038T-153ML (Coilcraft)
- C8:
  - 10 pF

Figure 42. Efficiency V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ

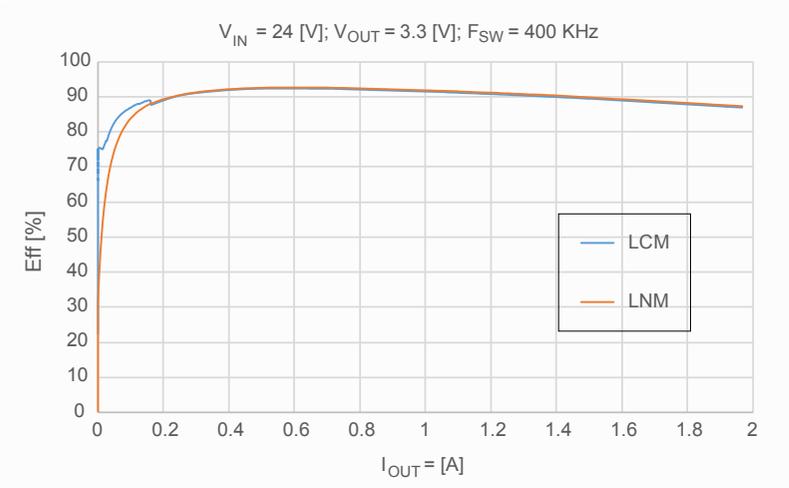
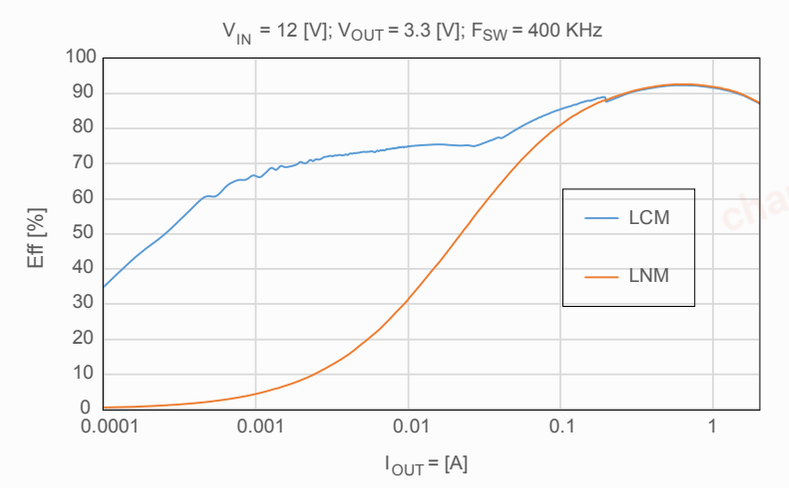
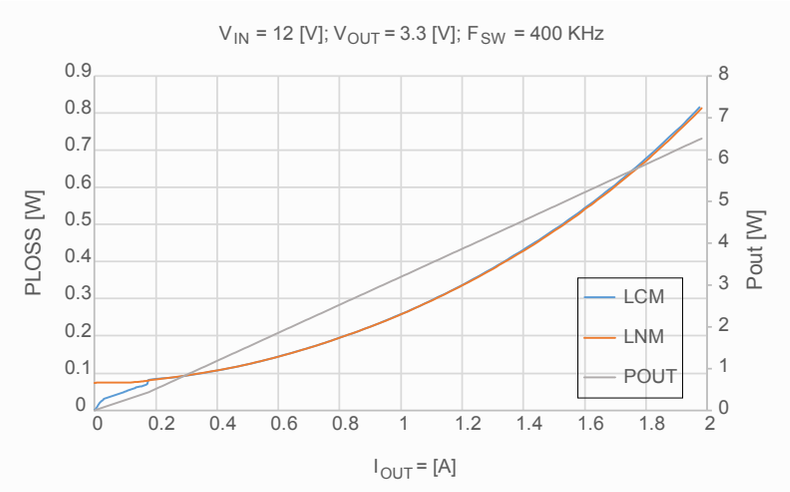


Figure 43. Efficiency V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ (log scale)



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Figure 44. **Power losses V_{IN} = 12 V; V_{OUT} = 3.3 V; F_{SW} = 0.4 MHZ**



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11 Thermal dissipation

The thermal design is important in order to prevent thermal shutdown of the device if junction temperature goes above 165°C. The three different sources of losses within the device are:

- Conduction losses due to the ON resistance of the high-side switch (R_{DSON_HS}) and low-side switch (R_{DSON_LS}); these are equal to:

$$P_{COND} = R_{DSON_HS} \cdot I_{OUT}^2 \cdot D + R_{DSON_LS} \cdot I_{OUT}^2 \cdot (1 - D) \quad (43)$$

Where D is the duty cycle of the selected application and is given by:

$$D = \frac{V_{OUT} + (R_{DSON_LS} + DCRl) \cdot I_{OUT}}{V_{IN} - (R_{DSON_{HS}} - R_{DSON_LS}) \cdot I_{OUT}} \quad (44)$$

In order to obtain a more accurate estimation it is necessary to keep in mind that the amount of resistance of the internal power MOSFET increases with the temperature. For this reason, the value of R_{DSONHS} and R_{DSONLS}, should be increased from the typical of a factor equal to 15%.

.

- Switching losses due to high side Power MOSFET turn ON and OFF; these can be calculated as:

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} \quad (45)$$

Where T_{RISE} and T_{FALL} are the overlap times of the voltage across the high-side power switch (V_{DS}) and the current flowing into it during turn ON and turn OFF phases, as shown in switching losses. T_{SW} is the equivalent switching time. For this device the typical value for the equivalent switching time is 20 ns.

- Quiescent current losses, calculated as:

$$P_Q = V_{IN} \cdot I_{Q,MAX} \quad (46)$$

The quiescent current for constant current operation is equal to 3 [mA]:
The power losses are given by:

$$P_{LOSS} = P_{COND} + P_{SW} + P_Q \quad (47)$$

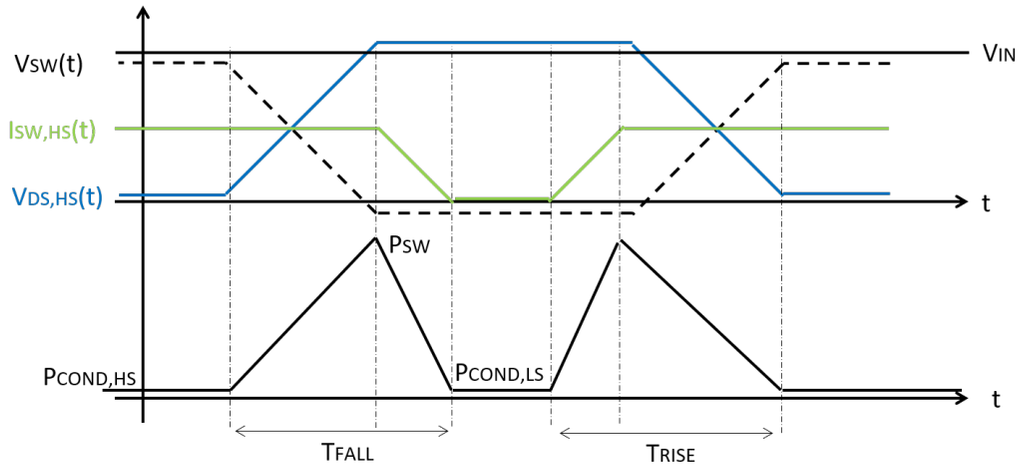
The junction temperature T_J can be calculated as:

$$T_J = T_A + R_{thJA} \cdot P_{LOSS} \quad (48)$$

Where T_A is the ambient temperature. R_{thJA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The R_{thJA} measured on the demonstration board described in the following section is about 55 °C/W.

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Figure 45. **Switching losses**



It is also possible to estimate the junction temperature directly from the efficiency measurements acquired on a stationary application condition.

Considering that the power losses are given by:

$$P_{LOSS} = P_{IN} - P_{OUT} \tag{49}$$

Neglecting the AC losses of the selected inductor, the power losses related to the L6982 are given by:

$$P_{LOSS\ L6982} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT} - DCRl \cdot I_{OUT}^2 \tag{50}$$

Consequently, the junction temperature T_J can be calculated as:

$$T_J = T_A + R_{thJA} \cdot P_{LOSS,\ L6982} \tag{51}$$

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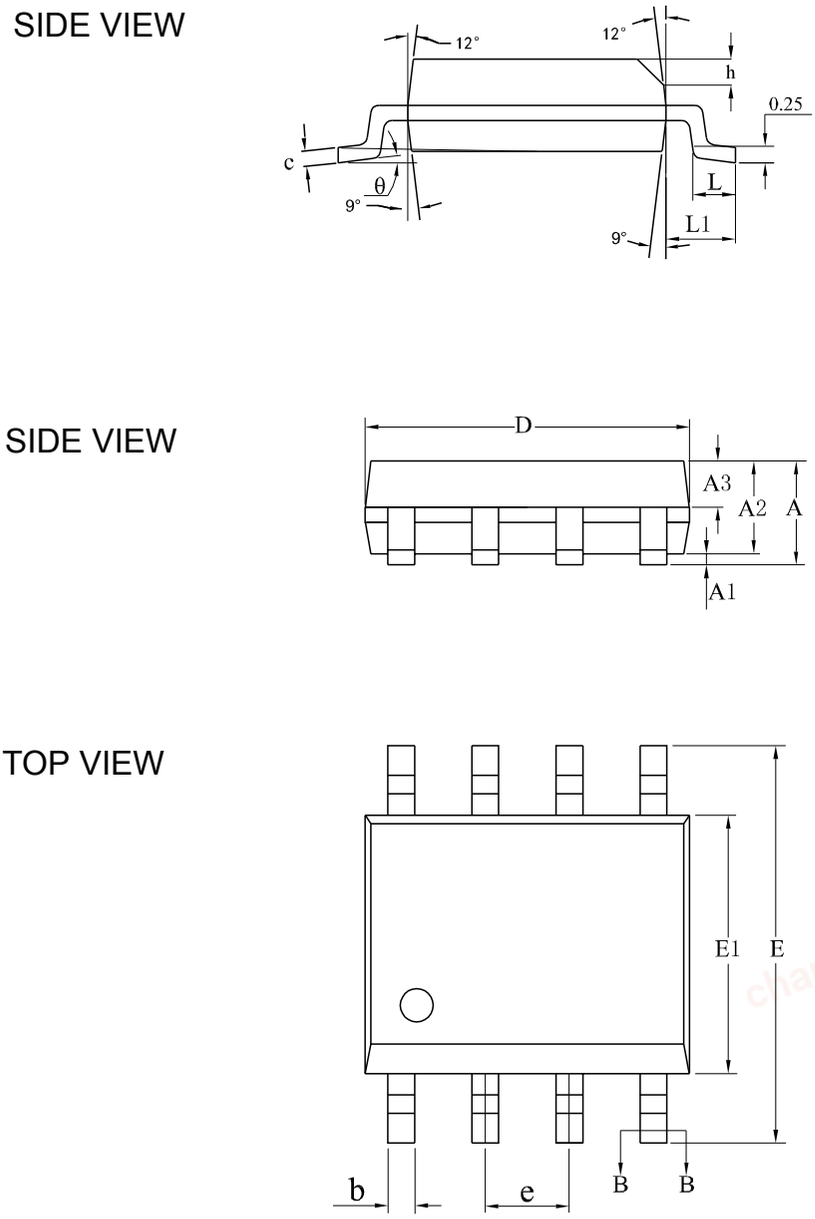
12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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12.1 SO 8L package information

Figure 46. **SO 8L package outline**

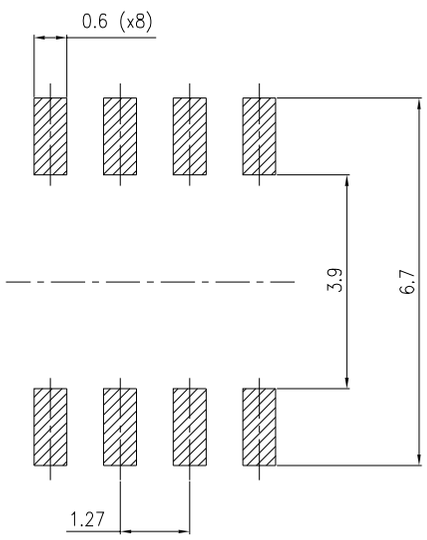


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Table 10. **SO 8L mechanical data**

Sym.	mm		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L1		1.05REF	
h	0.25	-	0.50
L	0.50	-	0.80
Θ	0	-	8°

Figure 47. **SO 8L recommended footprint**



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13 Ordering information

Table 11. **Order codes**

Part numbers	Output Voltage	Light load behavior	Package	Packaging
L6982CDR	Adj.	LCM (Low Consumption Mode)	SO 8L	Tape and reel
L6982NDR	Adj.	LNM (Low Noise Mode)		

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Revision history

Table 12. **Document revision history**

Date	Version	Changes
07-Apr-2021	1	First release.

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