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L6398

High voltage high and low-side driver

Datasheet - production data



SO-8

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability:
  - 290 mA source
  - 430 mA sink
- Switching times 75/35 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS input comparators with hysteresis
- Integrated bootstrap diode
- Fixed 320 ns deadtime
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Flexible, easy and fast design

Applications

- Motor driver for home appliances, factory automation, industrial drives and fans.

Description

The L6398 is a high voltage device manufactured with the BCD™ “offline” technology. It is a single-chip half bridge gate driver for the N-channel power MOSFET or IGBT.

The high-side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for the easy interfacing microcontroller/DSP.

This is information on a product in full production. www.st.com

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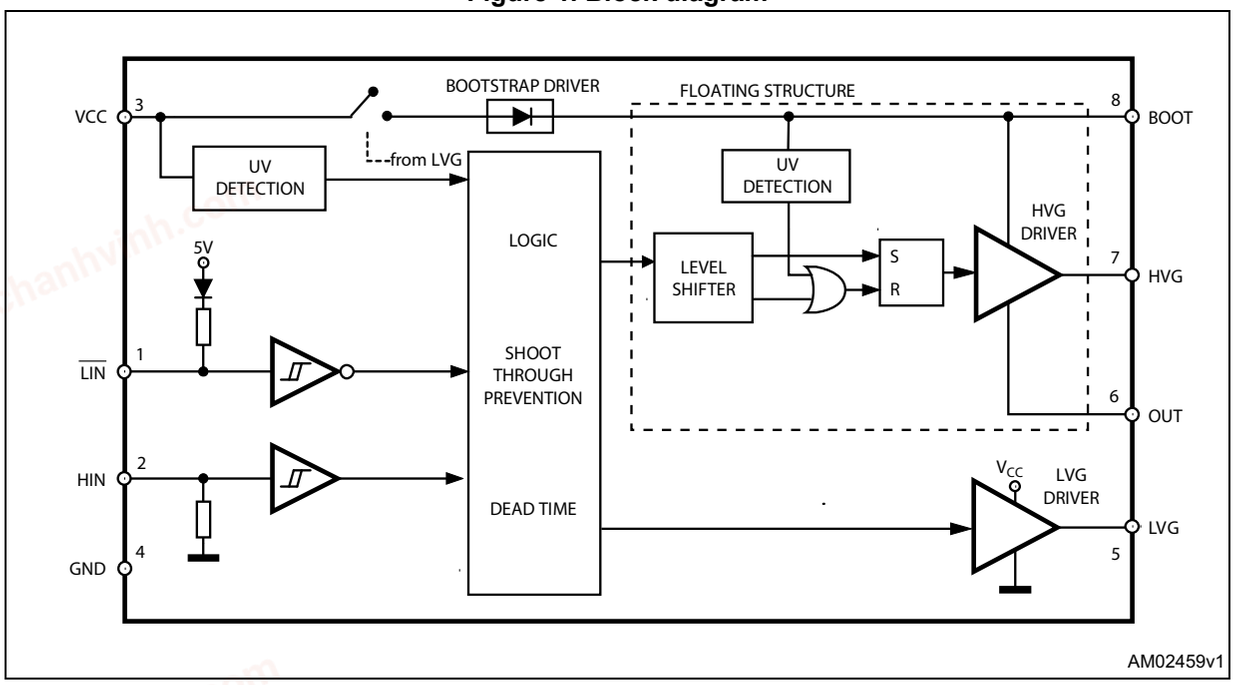
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1 Block diagram

Figure 1. Block diagram



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2 Pin connection

Figure 2. Pin connection (top view)

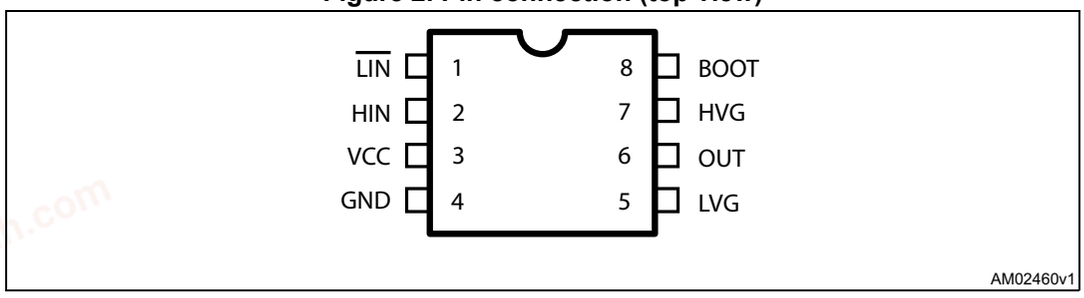


Table 1. Pin description

Pin no.	Pin name	Type	Function
1	$\overline{\text{LIN}}$	I	Low side-driver logic input (active low)
2	HIN	I	High-side driver logic input (active high)
3	VCC	P	Lower section supply voltage
4	GND	P	Ground
5	LVG (1)	O	Low-side driver output
6	OUT	P	High-side (floating) common voltage
7	HVG (1)	O	High-side driver output
8	BOOT	P	Bootstrapped supply voltage

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with V_{CC} > 3 V. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

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3 Truth table

Table 2. Truth table

Input		Output	
$\overline{\text{LIN}}$	HIN	LVG	HVG
H	L	L	L
L	H	L	L
L	L	H	L
H	H	L	H

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4 Electrical data

4.1 Absolute maximum ratings

Table 3. Absolute maximum rating

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{cc}	Supply voltage	-0.3	21	V
V_{OUT}	Output voltage	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{BOOT}	Bootstrap voltage	-0.3	620	V
V_{hvg}	High-side gate output voltage	V_{OUT} - 0.3	V_{BOOT} + 0.3	V
V_{lvg}	Low-side gate output voltage	-0.3	V_{cc} + 0.3	V
V_i	Logic input voltage	-0.3	15	V
dV_{OUT}/dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation (T_A = 25 °C)		800	mW
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	SO-8	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	150	°C/W

4.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
V_{cc}	3	Supply voltage		10	20	V
V_{BO}(1)	8 - 6	Floating supply voltage		9.8	20	V
V_{OUT}	6	Output voltage		- 11(2)	580	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF		800	kHz
T_J		Junction temperature		-40	125	°C

1. $V_{BO} = V_{BOOT} - V_{OUT}$.
2. LVG off. V_{CC} = 10 V
   Logic is operational if V_{BOOT} > 5 V.

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5 Electrical characteristics

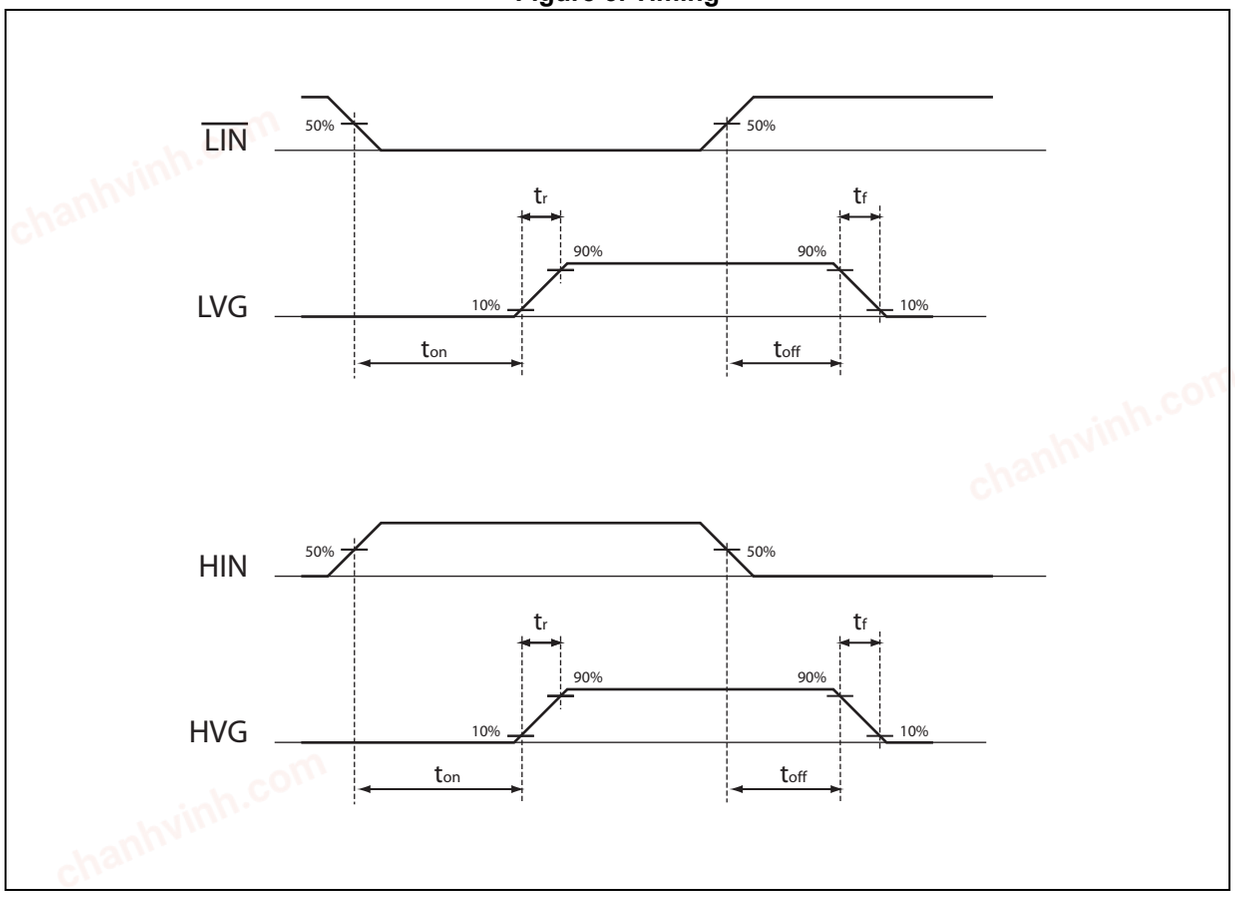
5.1 AC operation

Table 6. AC operation electrical characteristics (V_{CC} = 15 V; T_J = +25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{on}	1, 2 vs. 5, 7	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V V_{BOOT} = Vcc C_L = 1 nF V_{IN} = 0 to 3.3 V See *Figure 3*	50	125	200	ns
t_{off}		High/low side driver turn-off propagation delay		50	125	200	ns
DT		Deadtime(1)	C_L = 1 nF	225	320	415	ns
t_r	5, 7	Rise time	C_L = 1 nF		75	120	ns
t_f		Fall time	C_L = 1 nF		35	70	ns

1. See *Figure 4*.

Figure 3. Timing



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5.2 DC operation

Table 7. DC operation electrical characteristics (V_{CC} = 15 V; T_J = + 25 °C)

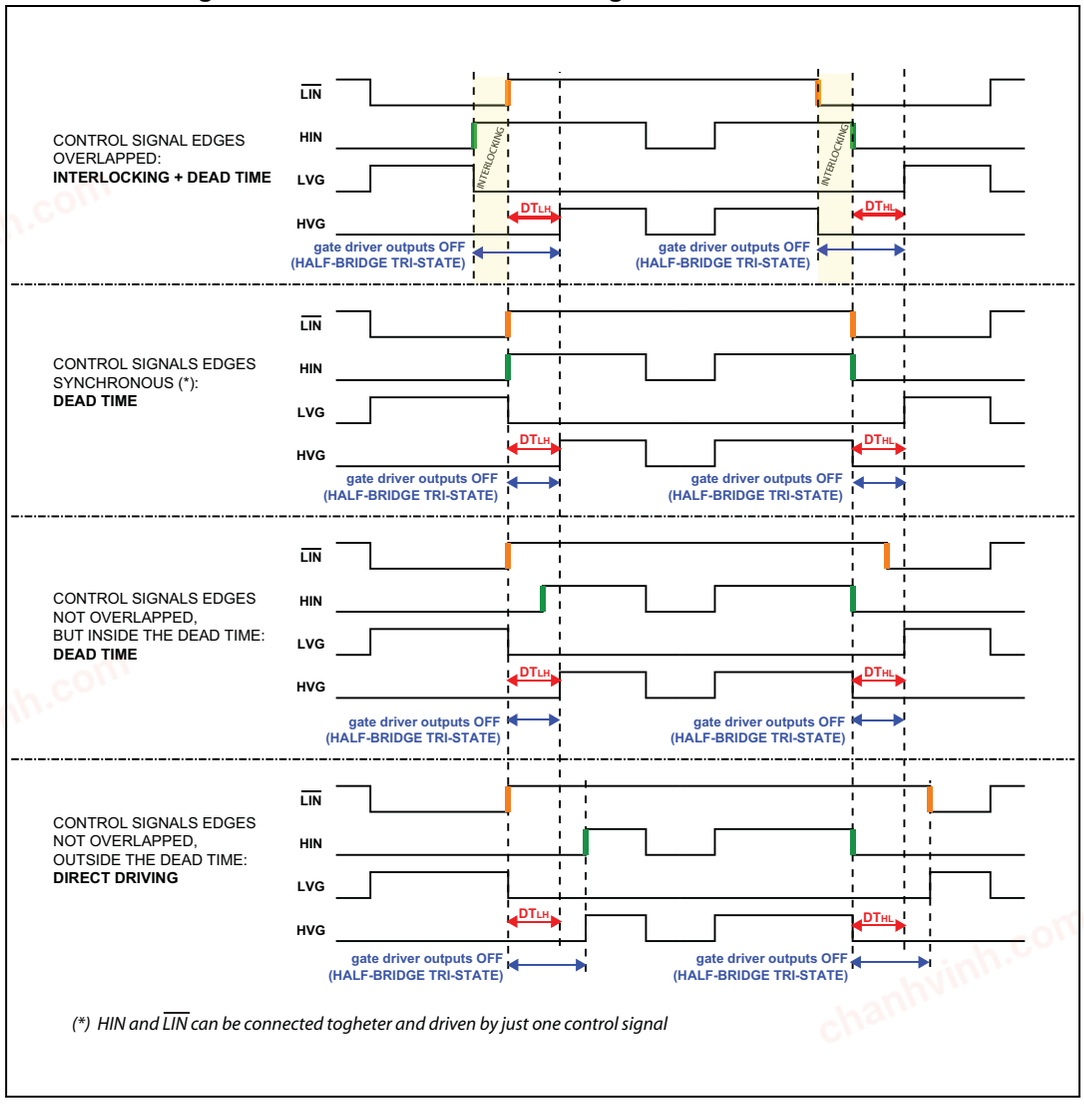
Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{cc_hys}	3	V_{cc} UV hysteresis		1.2	1.5	1.8	V
V_{cc_thON}		V_{cc} UV turn-ON threshold		9	9.5	10	V
V_{cc_thOFF}		V_{cc} UV turn-OFF threshold		7.6	8	8.4	V
I_{qccu}		Undervoltage quiescent supply current	V_{cc} = 7 V $\overline{LIN}$ = 5 V; HIN = GND;		90	150	µA
I_{qcc}		Quiescent current	V_{cc} = 15 V $\overline{LIN}$ = 5 V; HIN = GND;		380	440	µA
Bootstrapped supply voltage section(1)							
V_{BO_hys}	8	V_{BO} UV hysteresis		0.8	1	1.2	V
V_{BO_thON}		V_{BO} UV turn-ON threshold		8.2	9	9.8	V
V_{BO_thOFF}		V_{BO} UV turn-OFF threshold		7.3	8	8.7	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	V_{BO} = 7 V, $\overline{LIN}$ = HIN = 5V		30	60	µA
I_{QBO}		V_{BO} quiescent current	V_{BO} = 15 V, $\overline{LIN}$ = HIN = 5V		190	240	µA
I_{LK}		High voltage leakage current	V_{hvg} = V_{OUT} = V_{BOOT} = 600 V			10	µA
$R_{DS(on)}$		Bootstrap driver on resistance(2)	LVG ON		120		Ω
Driving buffers section							
I_{so}	5, 7	High/low-side source short-circuit current	V_{IN} = V_{ih} (t_p < 10 µs)	200	290		mA
I_{si}		High/low side sink short-circuit current	V_{IN} = V_{il} (t_p < 10 µs)	250	430		mA
Logic inputs							
V_{il}	1, 2	Low level logic threshold voltage		0.8		1.1	V
V_{ih}		High level logic threshold voltage		1.9		2.25	V
V_{il_S}	1, 2	Single input voltage	$\overline{LIN}$ and HIN connected together and floating			0.8	V
I_{HINh}	2	HIN logic “1” input bias current	HIN = 15 V	110	175	260	µA
I_{HINl}		HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	1	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 0 V	3	6	20	µA
I_{LINh}		$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 15 V			1	µA

1. V_{BO} = V_{BOOT} - V_{OUT}.
2. R_{DSON} is tested in the following way: R_{DSON} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})] where I_1 is the pin 8 current when V_{BOOT} = V_{BOOT1}, I_2 when V_{BOOT} = V_{BOOT2}.

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6 Waveforms definitions

Figure 4. Deadtime and interlocking waveforms definitions

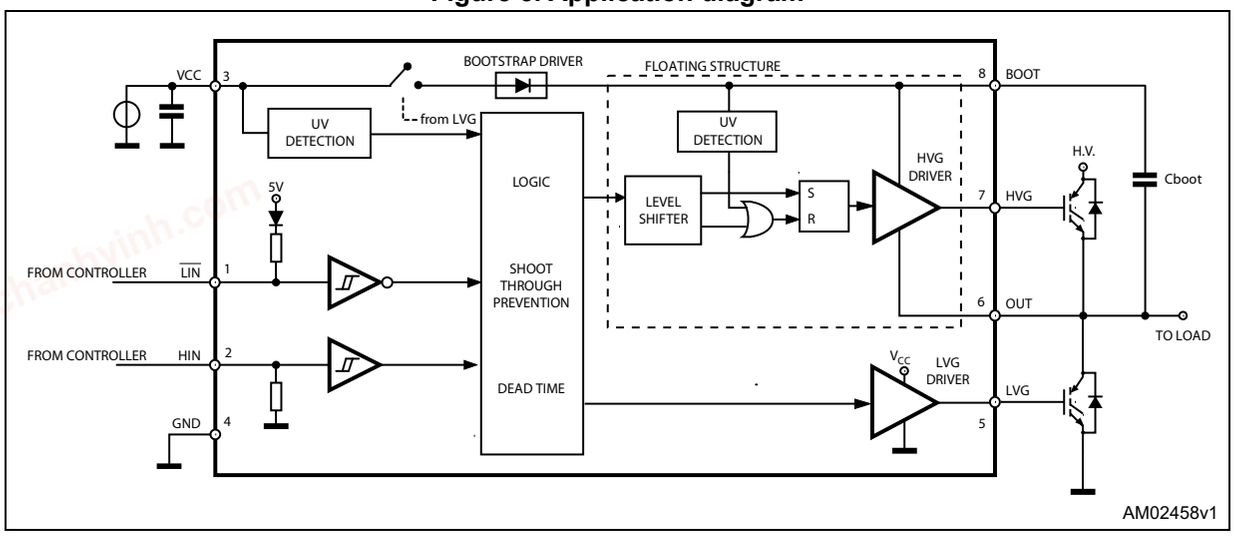


(*) HIN and $\overline{LIN}$ can be connected togheter and driven by just one control signal

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7 Typical application diagram

Figure 5. Application diagram



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8 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 6*). In the L6398 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 7*. An internal charge pump (*Figure 7*) provides the DMOS driving voltage.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} >>> C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

E.g.: HVG steady state consumption is lower than 190 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 1 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSon} (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

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For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

Equation 4

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 120\Omega \sim 0.7V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 6. Bootstrap driver with high voltage fast recovery diode

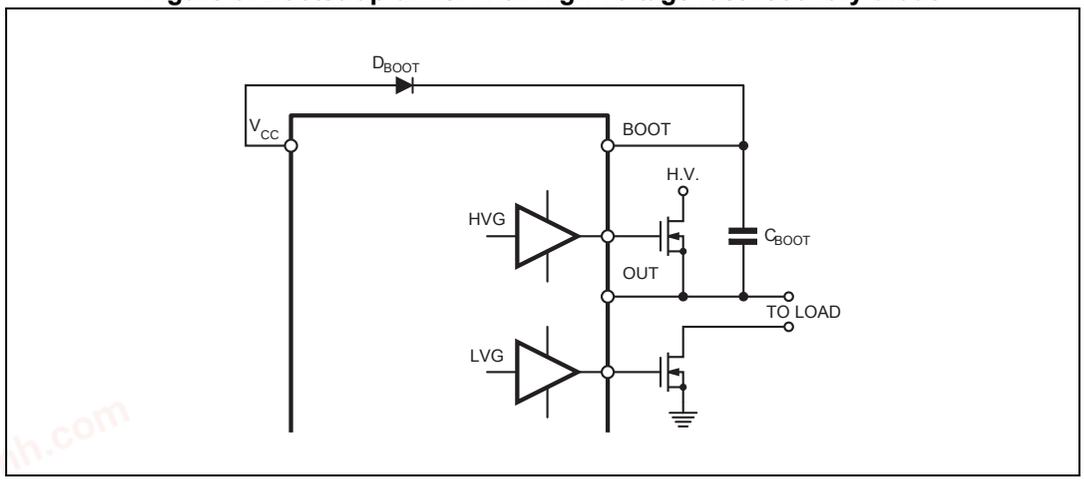
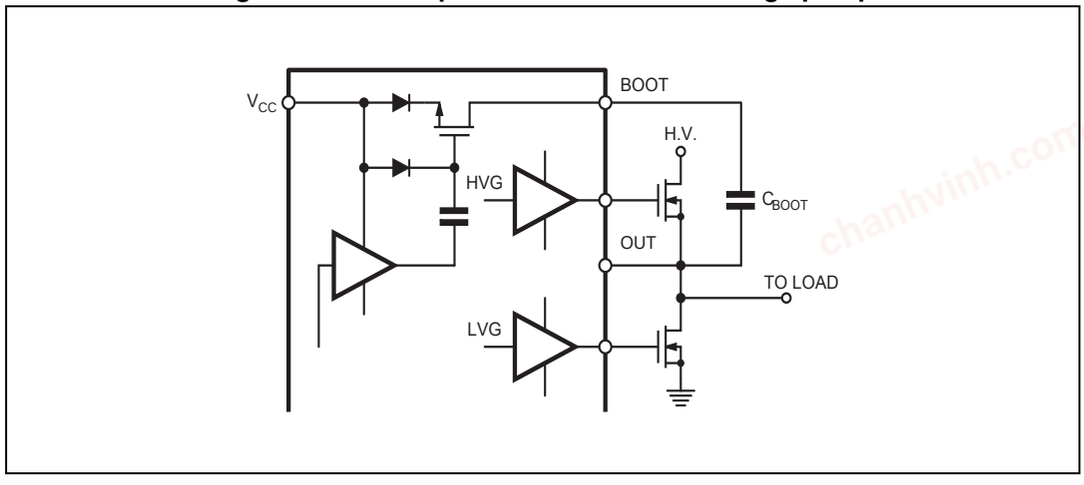


Figure 7. Bootstrap driver with internal charge pump



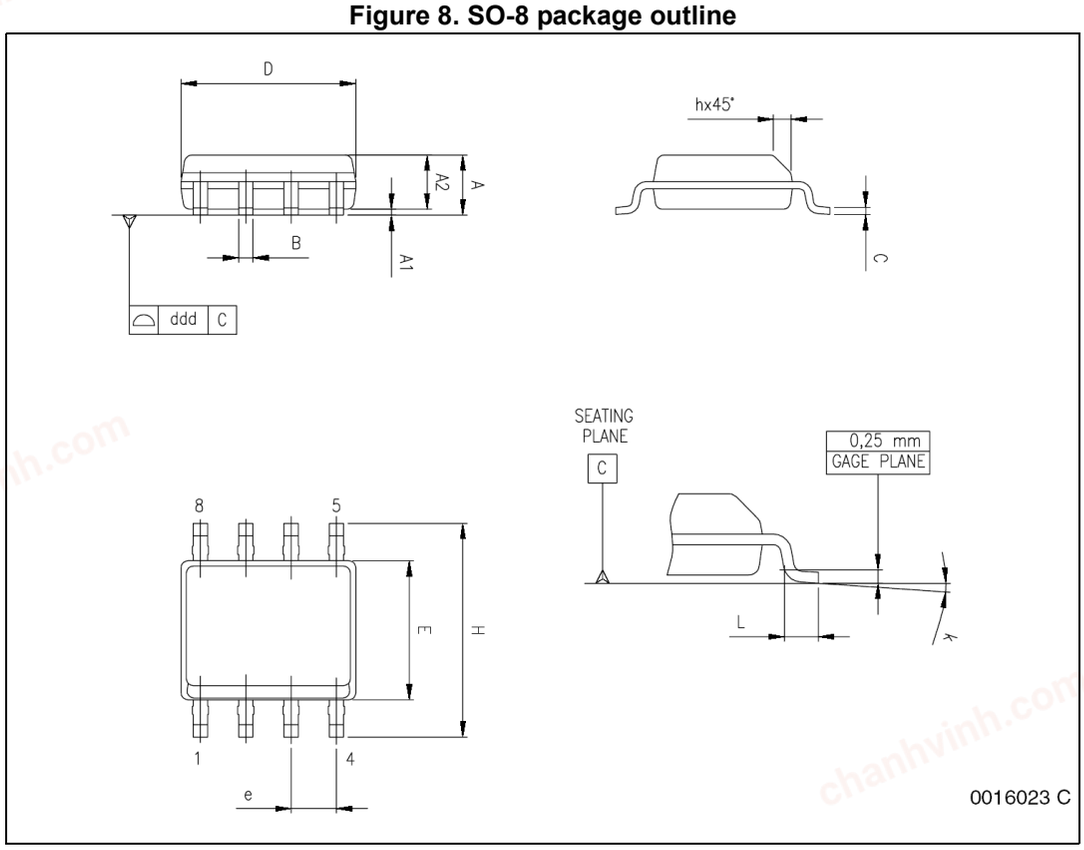
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9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

SO-8 package information

Figure 8. SO-8 package outline



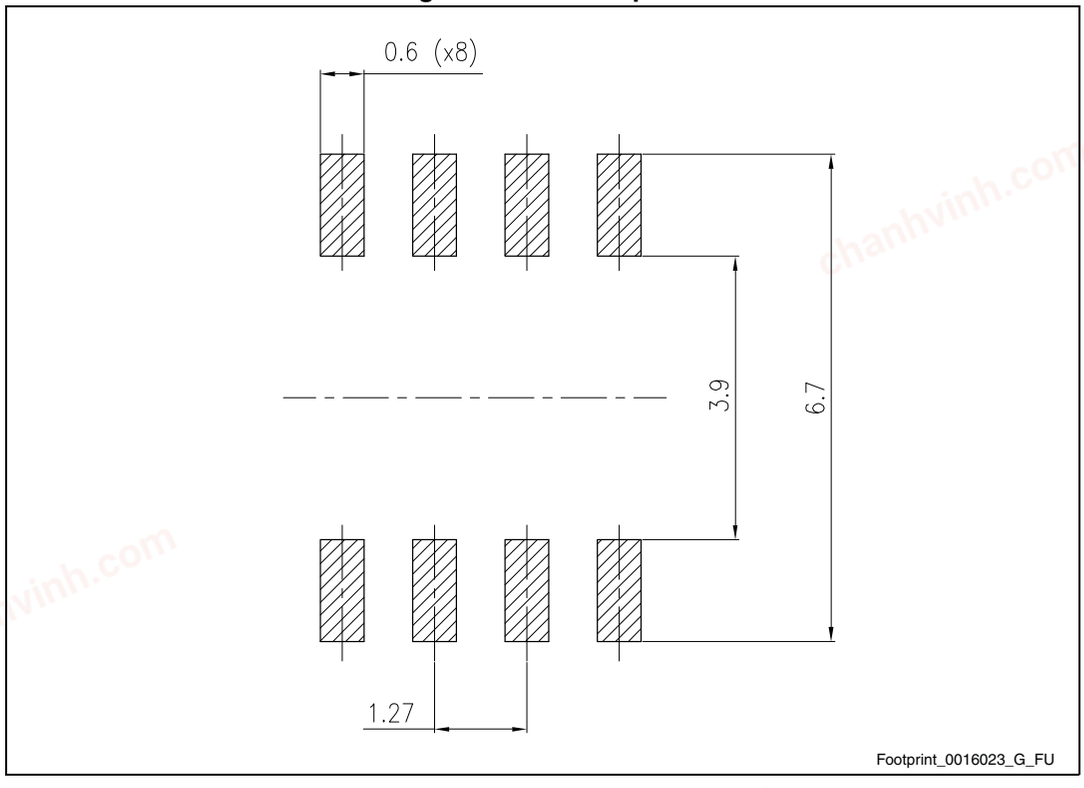
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Table 8. SO-8 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 inch) in total (both sides).

Figure 9. SO-8 footprint



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10 Order codes

Table 9. Order codes

Order codes	Package	Packaging
L6398D	SO-8	Tube
L6398DTR	SO-8	Tape and reel

11 Revision history

Table 10. Document revision history

Date	Revision	Changes
14-Dec-2010	1	First release.
16-Feb-2011	2	Updated *Table 7*.
01-Apr-2011	3	Typo in coverpage
11-Sep-2015	4	Removed DIP-8 package from the entire document. Updated *Table 3 on page 6* (added ESD parameter and value, removed note below *Table 3*). Updated V_{il} and V_{ih} parameters and values in *Table 7 on page 8* and note *2.* below *Table 7* (replaced V_{CBOOTx} by V_{BOOTx}). Updated *Section 9 on page 13* (added *Figure 9 on page 14*, minor modifications). Moved *Table 9 on page 15* (moved from page 1 to page 15, updated/added titles). Minor modifications throughout document.

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