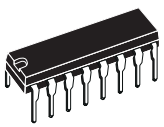
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L5991
L5991A

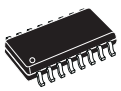
PRIMARY CONTROLLER WITH STANDBY

- CURRENT-MODE CONTROL PWM
- SWITCHING FREQUENCY UP TO 1MHz
- LOW START-UP CURRENT (< 120µA)
- HIGH-CURRENT OUTPUT DRIVE SUITABLE FOR POWER MOSFET (1A)
- FULLY LATCHED PWM LOGIC WITH DOUBLE PULSE SUPPRESSION
- PROGRAMMABLE DUTY CYCLE
- 100% AND 50% MAXIMUM DUTY CYCLE LIMIT
- STANDBY FUNCTION
- PROGRAMMABLE SOFT START
- PRIMARY OVERCURRENT FAULT DETECTION WITH RE-START DELAY
- PWM UVLO WITH HYSTERESIS
- IN/OUT SYNCHRONIZATION
- LATCHED DISABLE
- INTERNAL 100ns LEADING EDGE BLANKING OF CURRENT SENSE
- PACKAGE: DIP16 AND SO16

MULTIPOWER BCD TECHNOLOGY



DIP16



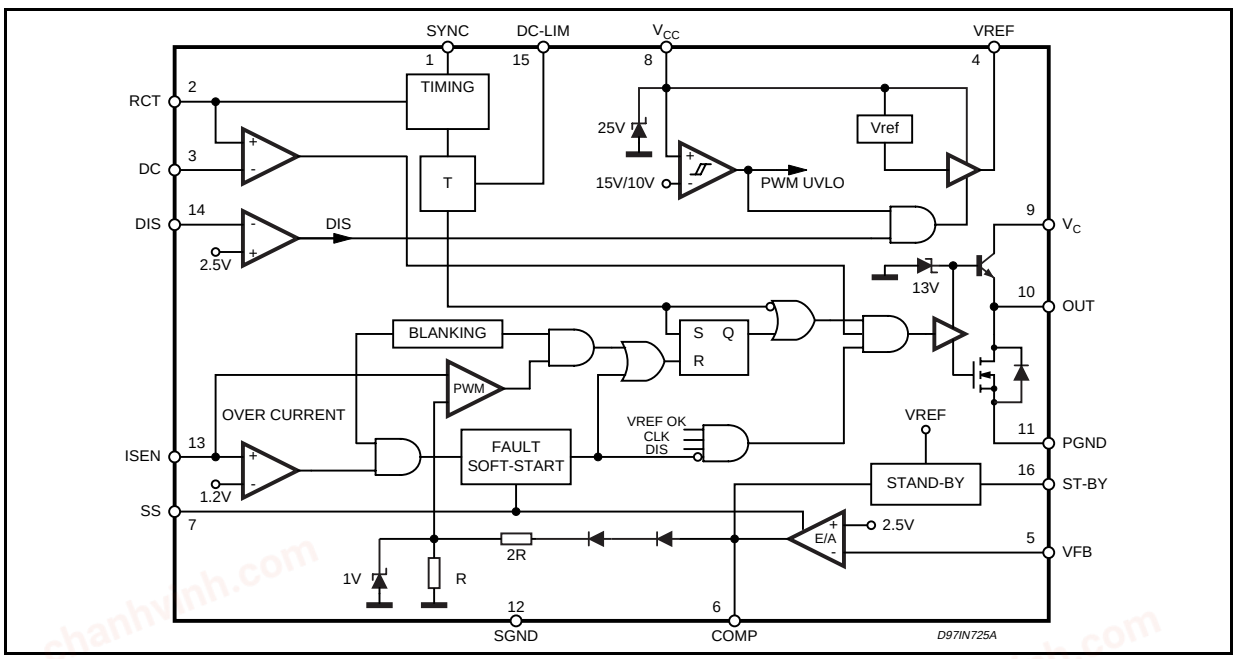
SO16

ORDERING NUMBERS: L5991/L5991A (DIP16)
L5991D/L5991AD (SO16)

DESCRIPTION

This primary controller I.C., developed in BCD60II technology, has been designed to implement off line or DC-DC power supply applications using a fixed frequency current mode control.
Based on a standard current mode PWM controller this device includes some features such as programmable soft start, IN/OUT synchronization, disable (to be used for over voltage protection and for power management), precise maximum Duty Cycle Control, 100ns leading edge blanking on current sense, pulse by pulse current limit, overcurrent protection with soft start intervention, and Standby function for oscillator frequency reduction when the converter is lightly loaded.

BLOCK DIAGRAM



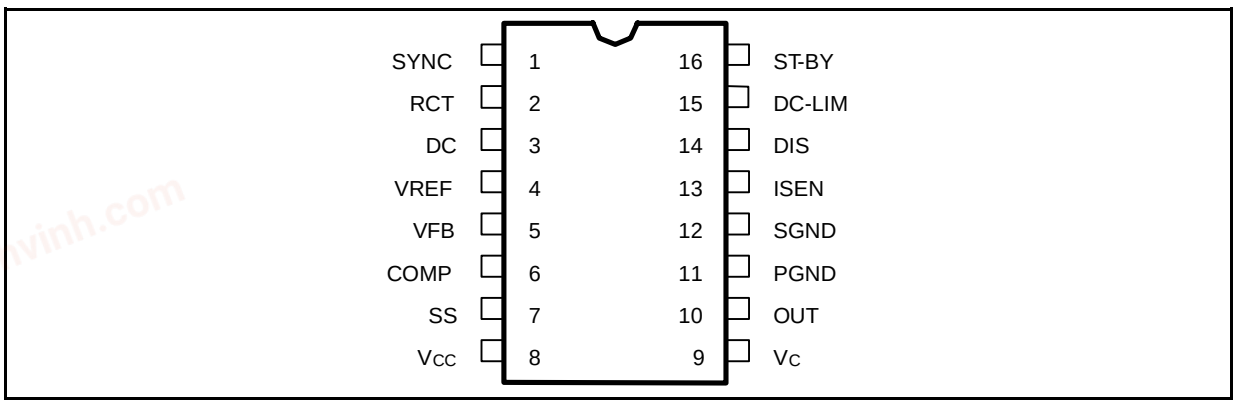
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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (I_{CC} < 50mA) (*)	selflimit	V
I_{OUT}	Output Peak Pulse Current	1.5	A
	Analog Inputs & Outputs (6,7)	-0.3 to 8	V
	Analog Inputs & Outputs (1,2,3,4,5,15,14, 13, 16)	-0.3 to 6	V
P_{tot}	Power Dissipation @ T_{amb} = 70°C (DIP16) @ T_{amb} = 50°C (SO16)	1 0.83	W W
T_j	Junction Temperature, Operating Range	-40 to 150	°C
T_{stg}	Storage Temperature, Operating Range	-55 to 150	°C

(*) maximum package power dissipation limits must be observed

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction -Ambient **(DIP16)**	80	°C/W
	Thermal Resistance Junction -Ambient **(SO16)**	120	°C/W

PIN FUNCTIONS

N.	Name	Function
1	SYNC	Synchronization. A synchronization pulse terminates the PWM cycle and discharges Ct
2	RCT	Oscillator pin for external C_T, R_A, R_B components
3	DC	Duty Cycle control
4	VREF	5.0V +/-1.5% reference voltage @ 25°C
5	VFB	Error Amplifier Inverting input
6	COMP	Error Amplifier Output
7	SS	Soft start pin for external capacitor Css
8	V_{CC}	Supply for internal "Signal" circuitry
9	V_C	Supply for Power section
10	OUT	High current totem pole output
11	PGND	Power ground
12	SGND	Signal ground
13	ISEN	Current sense
14	DIS	Disable. It must never be left floating. TIE to SGND if not used.
15	DC-LIM	Connecting this pin to Vref, DC is limited to 50%. If it is left floating or grounded no limitation is imposed
16	ST-BY	Standby. Connect a resistor to RCT. Connect to VREF or floating if not used.

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ELECTRICAL CHARACTERISTICS (V_{CC} = 15V; T_j = 0 to 105°C; R_T = 13.3kΩ (*) C_T = 1nF; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
V_{REF}	Output Voltage	T_j = 25°C; I_O = 1mA	4.925	5.0	5.075	V
	Line Regulation	V_{CC} = 12 to 20V; T_j = 25°C		2.0	10	mV
	Load Regulation	I_O = 1 to 10mA; T_j = 25°C		2.0	10	mV
T_S	Temperature Stability			0.4		mV/°C
	Total Variation	Line, Load, Temperature	4.80	5.0	5.130	V
I_{OS}	Short Circuit Current	Vref = 0V	30		150	mA
	Power Down/UVLO	V_{CC} = 6V; I_{sink} = 0.5mA		0.2	0.5	V
OSCILLATOR SECTION						
	Initial Accuracy	pin 15 = Vref; T_j = 25°C; V_{comp} = 4.5V	95	100	105	kHz
		pin 15 = Vref; V_{CC} = 12 to 20V, V_{comp} = 4.5V	93	100	107	kHz
		pin 15 = Vref; V_{CC} = 12 to 20V, V_{comp} = 2V	46.5	50	53.5	kHz
	Duty Cycle	pin 3 = 0,7V, pin 15 = V_{REF} pin 3 = 0.7V, pin 15 = OPEN			0 0	% %
		pin 3 = 3.2V, pin 15 = V_{REF} pin 3 = 3.2V, pin 15 = OPEN	47 93			% %
	Duty Cycle Accuracy	pin 3 = 2.79V, pin 15 = OPEN	75	80	85	%
	Oscillator Ramp Peak		2.8	3.0	3.2	V
	Oscillator Ramp Valley		0.75	0.9	1.05	V
ERROR AMPLIFIER SECTION						
	Input Bias Current	V_{FB} to GND		0.2	3.0	µA
V_I	Input Voltage	V_{COMP} = V_{FB}	2.42	2.5	2.58	V
G_{OPL}	Open Loop Gain	V_{COMP} = 2 to 4V	60	90		dB
SVR	Supply Voltage Rejection	V_{CC} = 12 to 20V		85		dB
V_{OL}	Output Low Voltage	I_{sink} = 2mA			1.1	V
V_{OH}	Output High Voltage	I_{source} = 0.5mA, V_{FB} = 2.3V	5	6		V
I_O	Output Source Current	V_{COMP} > 4V, V_{FB} = 2.3V	0.5	1.3	2.5	mA
	Output Sink Current	V_{COMP} = 1.1V, V_{FB} = 2.7V	2	6		mA
	Unit Gain Bandwidth		1.7	4		MHz
S_R	Slew Rate			8		V/µs
PWM CURRENT SENSE SECTION						
I_b	Input Bias Current	I_{sen} = 0		3	15	µA
I_S	Maximum Input Signal	V_{COMP} = 5V	0.92	1.0	1.08	V
	Delay to Output			70	100	ns
	Gain		2.85	3	3.15	V/V
V_t	Fault Threshold Voltage		1.1	1.2	1.3	V
SOFT START SECTION						
I_{SSC}	SS Charge Current	T_j = 25°C	14	20	26	µA
I_{SSD}	SS Discharge Current	VSS = 0.6V T_j = 25°C	5	10	15	µA
V_{SSSAT}	SS Saturation Voltage	DC = 0%			0.6	V
$V_{SSCLAMP}$	SS Clamp Voltage			7		V
LEADING EDGE BLANKING						
	Internal Masking Time			100		ns
OUTPUT SECTION						
V_{OL}	Output Low Voltage	I_O = 250mA			1.0	V
V_{OH}	Output High Voltage	I_O = 20mA; V_{CC} = 12V	10	10.5		V
		I_O = 200mA; V_{CC} = 12V	9	10		V
$V_{OUT\ CLAMP}$	Output Clamp Voltage	I_O = 5mA; V_{CC} = 20V		13		V
	Collector Leakage	V_{CC} = 20V V_C = 24V		2	20	µA

(*) $R_T = R_A // R_B$, $R_A = R_B$ = 27kΩ, see Fig. 23.

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ELECTRICAL CHARACTERISTICS (continued.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT SECTION						
	Fall Time	C_O = 1nF C_O = 2.5nF		20 35	60	ns ns
	Rise Time	C_O = 1nF C_O = 2.5nF		50 70	100	ns ns
	UVLO Saturation	V_{CC} = V_C = 0 to $V_{CCON;}$ I_{sink} = 10mA			1.0	V
SUPPLY SECTION						
V_{CCON}	Startup voltage	**L5991** **L5991A**	14 7.8	15 8.4	16 9	V V
V_{CCOFF}	Minimum Operating Voltage	**L5991** **L5991A**	9 7	10 7.6	11 8.2	V V
V_{hys}	UVLO Hysteresis	**L5991** **L5991A**	4.5 0.5	5 0.8		V V
I_S	Start Up Current	Before Turn-on at: V_{CC} = V_C = V_{CCON} -0.5V	40	75	120	µA
I_{op}	Operating Current	C_T = 1nF, R_T = 13.3kΩ, C_O =1nF		9	13	mA
I_q	Quiescent Current	(After turn on), CT = 1nF, R_T = 13.3kΩ, C_O =0nF		7.0	10	mA
V_Z	Zener Voltage	I_8 = 20mA	21	25	30	V
STANDBY FUNCTION						
V_{REF}-V_{ST-BY}		I_{ST-BY} = 2mA		45		mV
V_{T1}	Standby Threshold	V_{comp} Falling		2.5		V
		V_{comp} Rising		4.0		V
SYNCHRONIZATION SECTION						
Master Operation						
V_1	Clock Amplitude	I_{SOURCE} = 0.8mA	4			V
I_1	Clock Source Current	Vclock = 3.5V	3	7		mA
Slave Operation						
V_1	Sync Pulse	Low Level			1	V
		High Level	3.5			V
I_1	Sync Pulse Current	VSYNC = 3.5V	0.5			mA
OVER CURRENT PROTECTION						
V_t	Fault Threshold Voltage		1.1	1.2	1.3	V
DISABLE SECTION						
	Shutdown threshold		2.4	2.5	2.6	V
	Input Bias Current	V_{pin14} = 0 to 3V	-1		1	µA
I_{qSH}	Quiescent current After Disable	V_{CC} = 15V		330		µA

Figure 1. L5991 - Quiescent current vs. input voltage. (X = 7.6V and Y= 8.4V for L5991A)

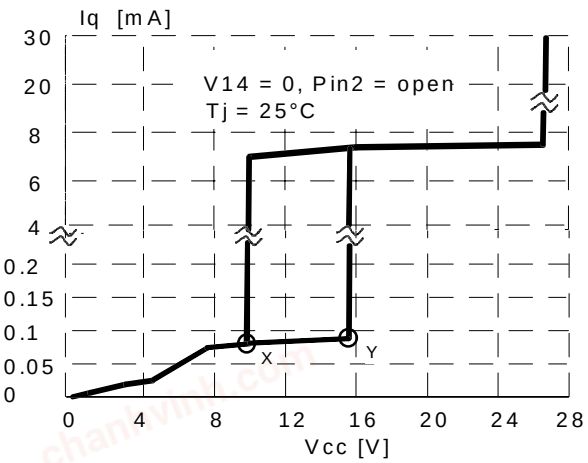
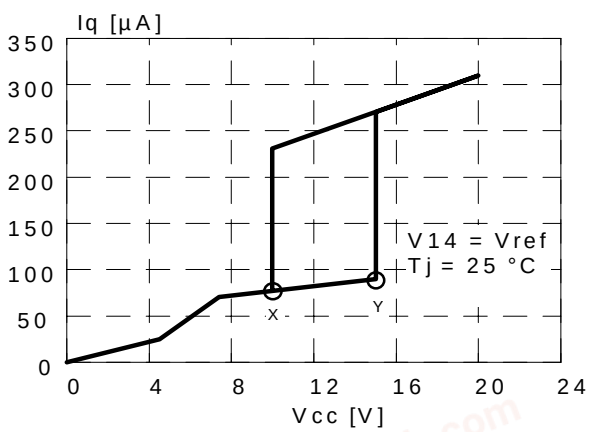


Figure 2. L5991 - Quiescent current vs. input voltage (after disable). (X = 7.6V and Y= 8.4V for L5991A)



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Figure 3. Quiescent current vs. input voltage.

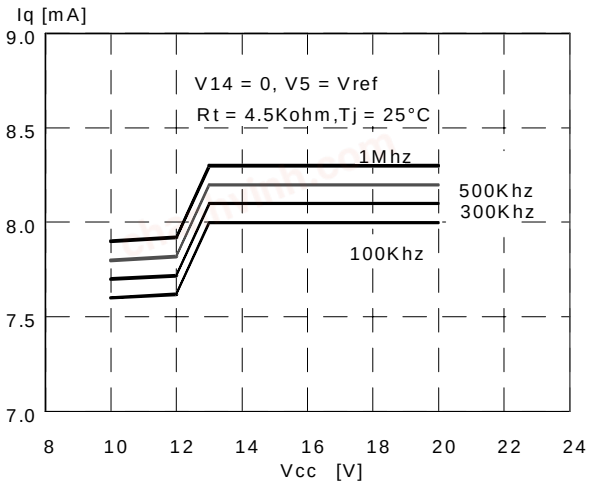


Figure 4. Quiescent current vs. input voltage and switching frequency.

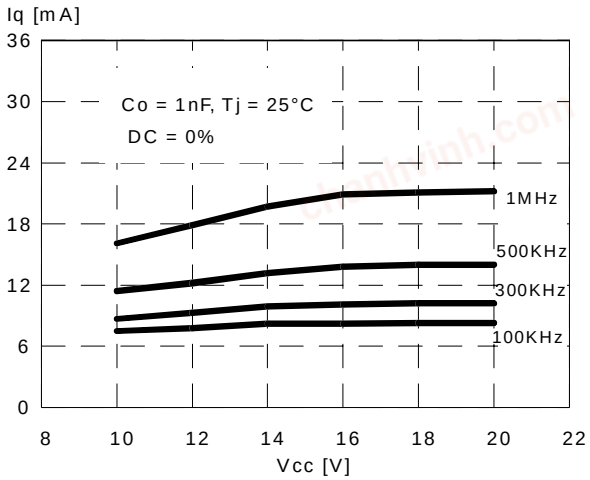


Figure 5. Quiescent current vs. input voltage and switching frequency.

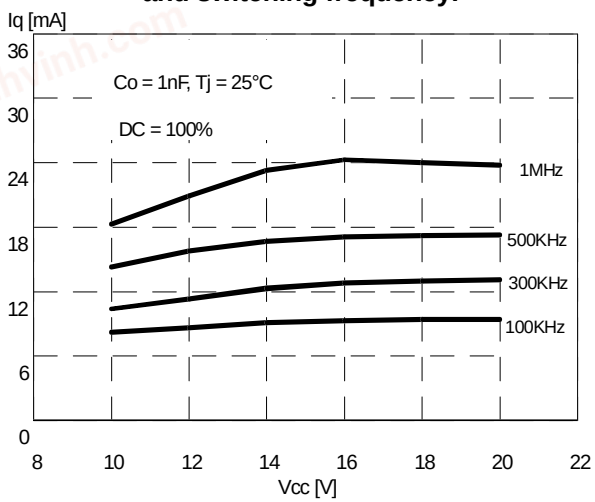


Figure 6. IC Consumption vs. Temperature.

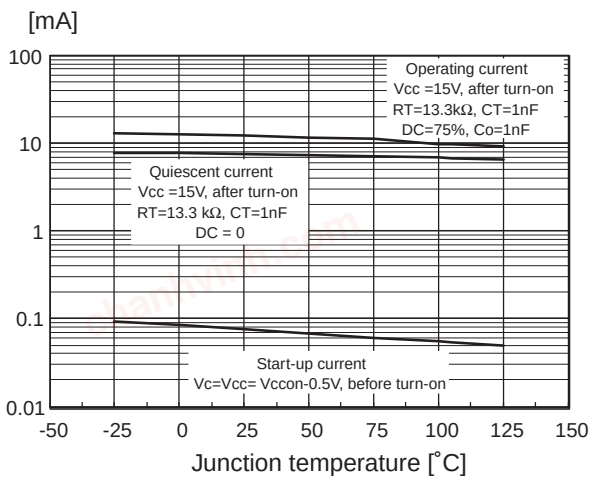


Figure 7. Reference voltage vs. load current.

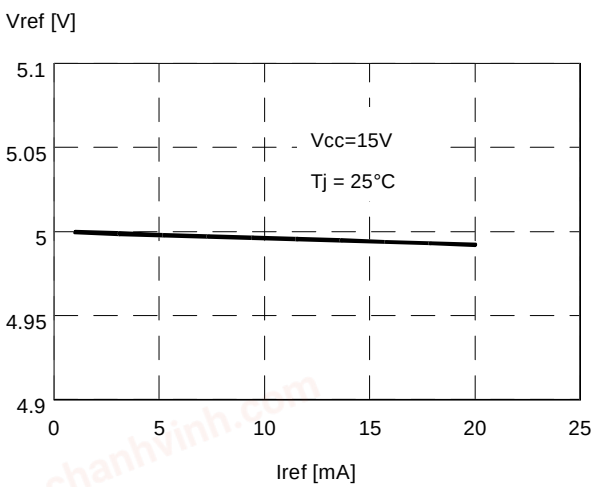
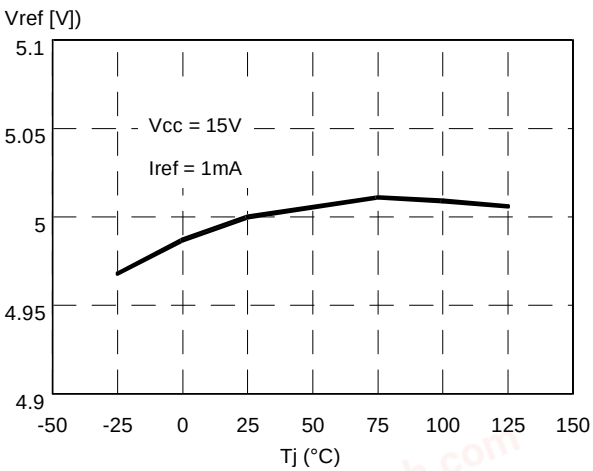


Figure 8. Vref vs. junction temperature.



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Figure 9. Vref vs. junction temperature.

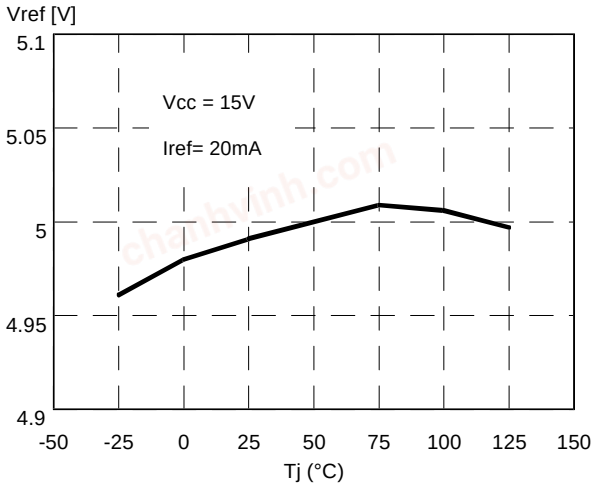


Figure 10. Vref SVRR vs. switching frequency.

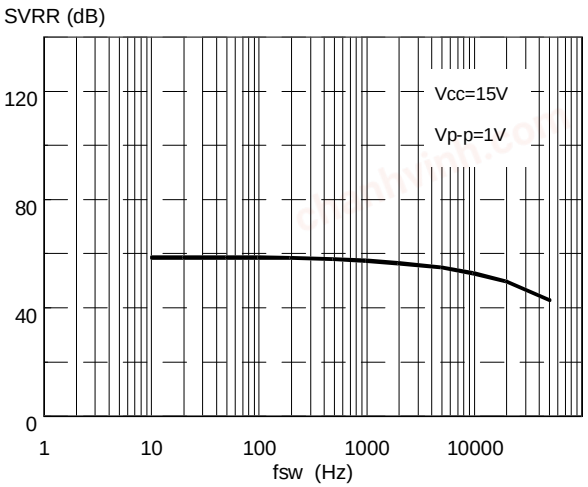


Figure 11. Output saturation.

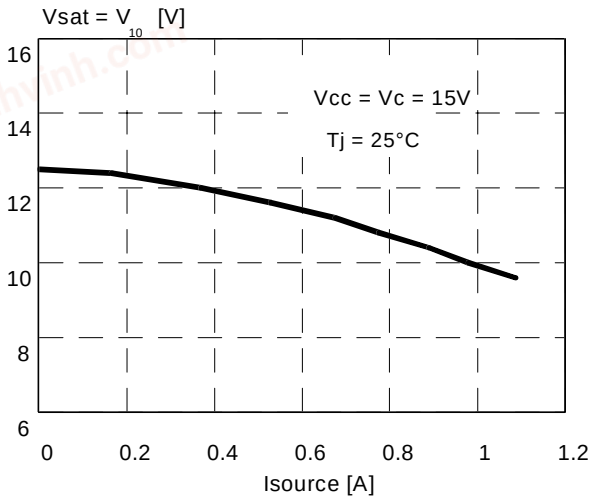


Figure 12. Output saturation.

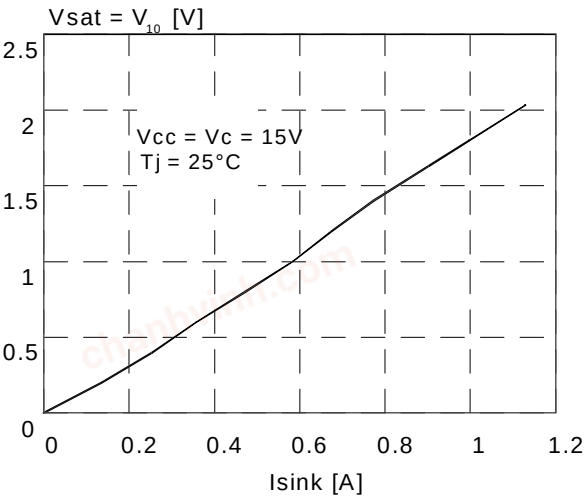


Figure 13. UVLO Saturation

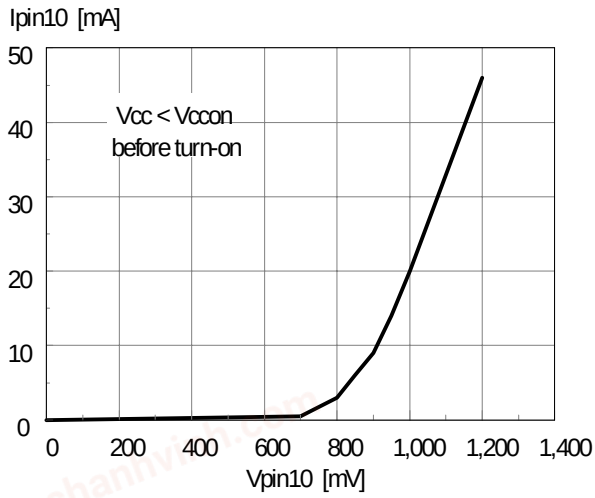
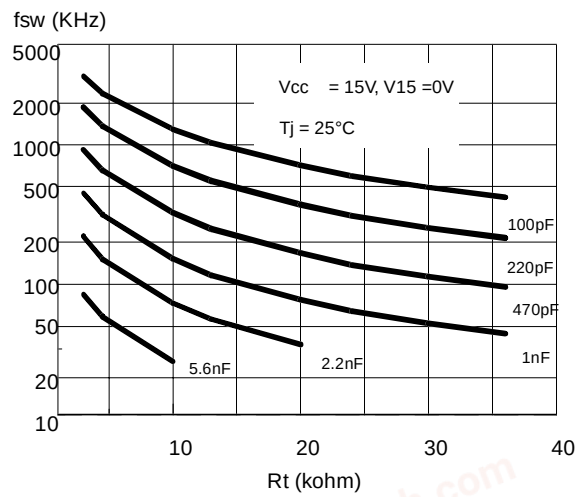


Figure 14. Timing resistor vs. switching frequency.



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Figure 15. Switching frequency vs. temperature.

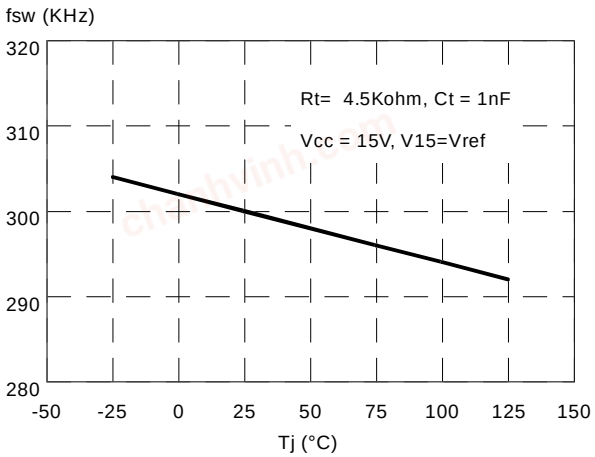


Figure 16. Switching frequency vs. temperature.

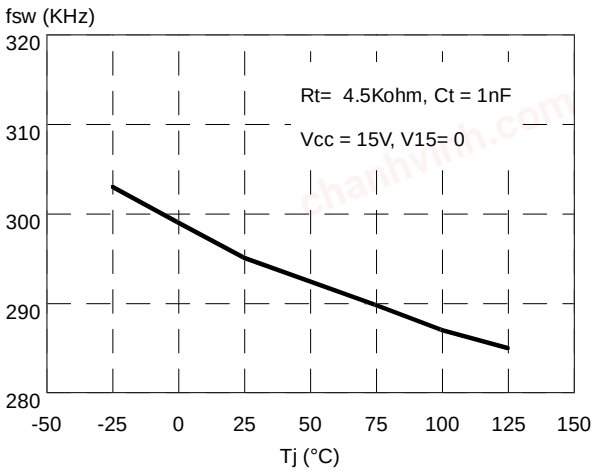


Figure 17. Dead time vs Ct.

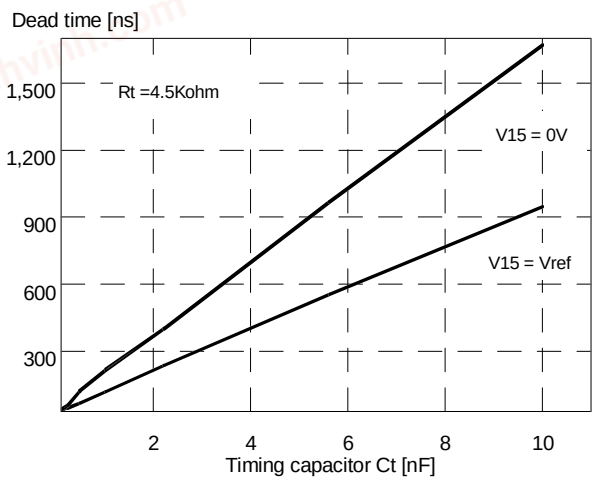


Figure 18. Maximum Duty Cycle vs Vpin3.

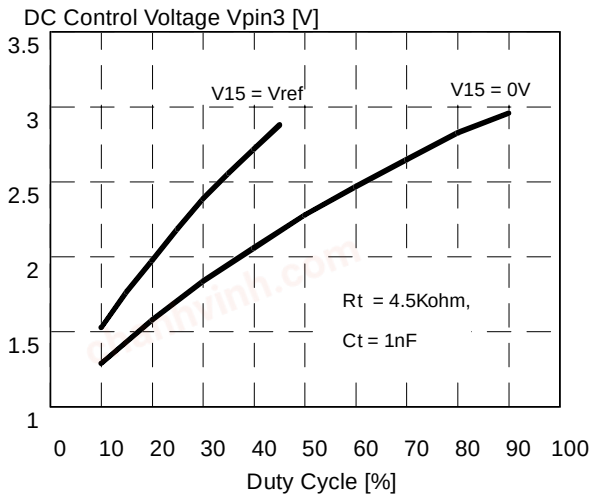


Figure 19. Delay to output vs junction temperature.

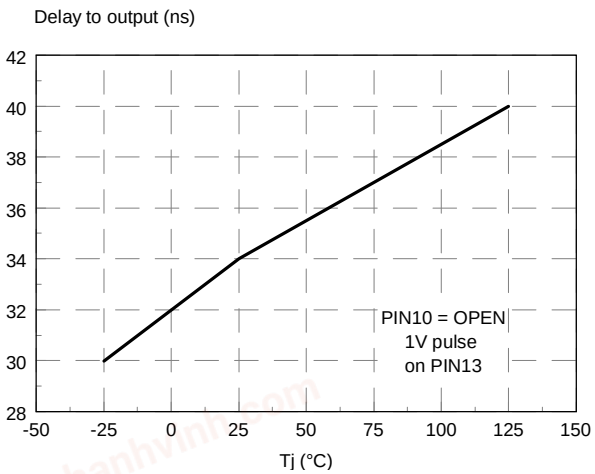
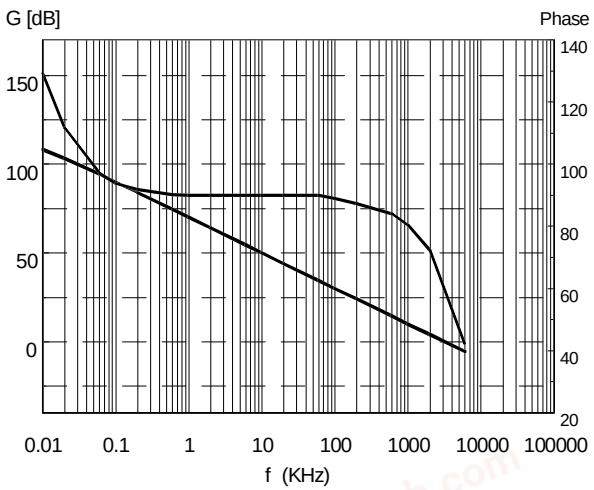


Figure 20. E/A frequency response.



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STANDBY FUNCTION

The standby function, optimized for flyback topology, automatically detects a light load condition for the converter and decreases the oscillator frequency on that occurrence. The normal oscillation frequency is automatically resumed when the output load builds up and exceeds a defined threshold.

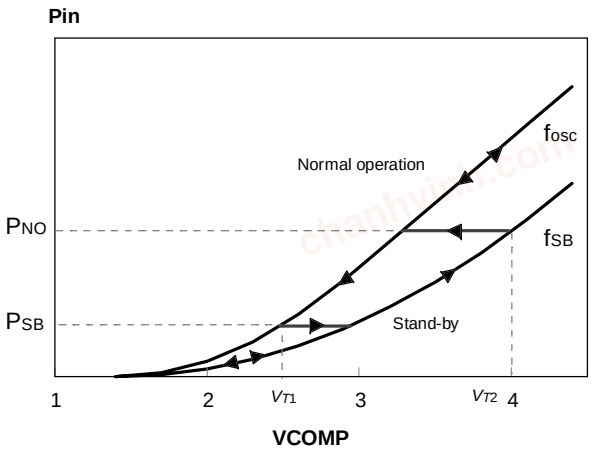
This function allows to minimize power losses related to switching frequency, which represent the majority of losses in a lightly loaded flyback, without giving up the advantages of a higher switching frequency at heavy load.

This is accomplished by monitoring the output of the Error Amplifier (V_{COMP}) that depends linearly on the peak primary current, except for an offset.

If the the peak primary current decreases (as a result of a decrease of the power demanded by the load) and V_{COMP} falls below a fixed threshold (V_{T1}), the oscillator frequency will be set to a lower value (f_{SB}). When the peak primary current increases and V_{COMP} exceeds a second threshold (V_{T2}) the oscillator frequency is set to the normal value (f_{osc}). An appropriate hysteresis (V_{T2}-V_{T1}) prevents undesired frequency change when power is such that V_{COMP} moves close to the threshold. This operation is shown in fig. 21.

Both the normal and the standby frequency are externally programmable. V_{T1} and V_{T2} are internally fixed but it is possible to adjust the thresholds in terms of input power level.

Figure 21. Standby dynamic operation.



APPLICATION INFORMATION

Detailed Pin Function Description

Pin 1. SYNC (In/Out Synchronization). This function allows the IC's oscillator either to synchronize other controllers (master) or to be synchronized to an external frequency (slave).

As a master, the pin delivers positive pulses during the falling edge of the oscillator (see pin 2). In slave operation the circuit is edge triggered. Refer to fig. 23 to see how it works. When several IC work in parallel no master-slave designation is needed because the fastest one becomes automatically the master.
During the ramp-up of the oscillator the pin is pulled low by a 600µA internal sink current generator. During the falling edge, that is when the pulse is released, the 600µA pull-down is disconnected. The pin becomes a generator whose source capability is typically 7mA (with a voltage still higher than 3.5V).

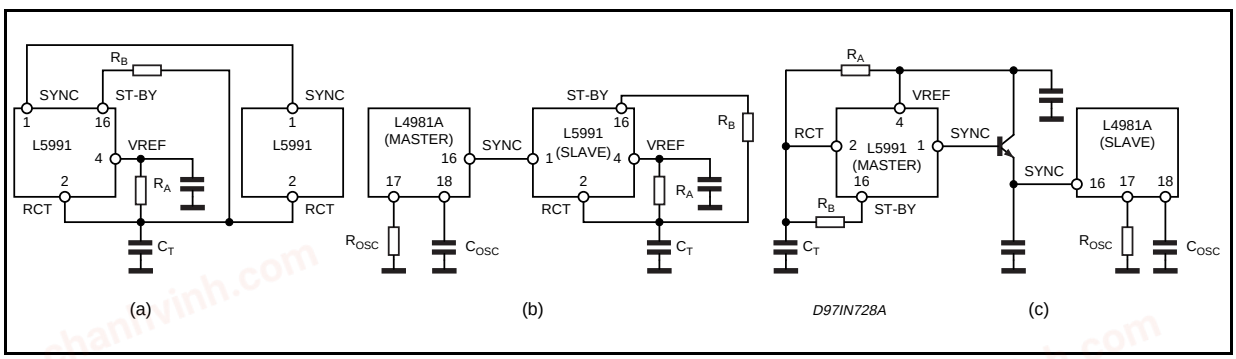
In fig. 22, some practical examples of synchronizing the L5991 are given.
Since the device automatically diminishes its operating frequency under light load conditions, it is reasonable to suppose that synchronization will refer to normal operation and not to standby.

Pin 2. RCT (Oscillator). Two resistors (R_A and R_B) and one capacitor (C_T), connected as shown in fig. 23, allow to set separately the operating frequency of the oscillator in normal operation (f_{osc}) and in standby mode (f_{SB}).

C_T is charged from Vref through R_A and R_B in normal operation ($\overline{STANDBY}$ = HIGH), through R_A only in standby ($\overline{STANDBY}$ = LOW). See pin 16 description to see how the STANDBY signal is generated.

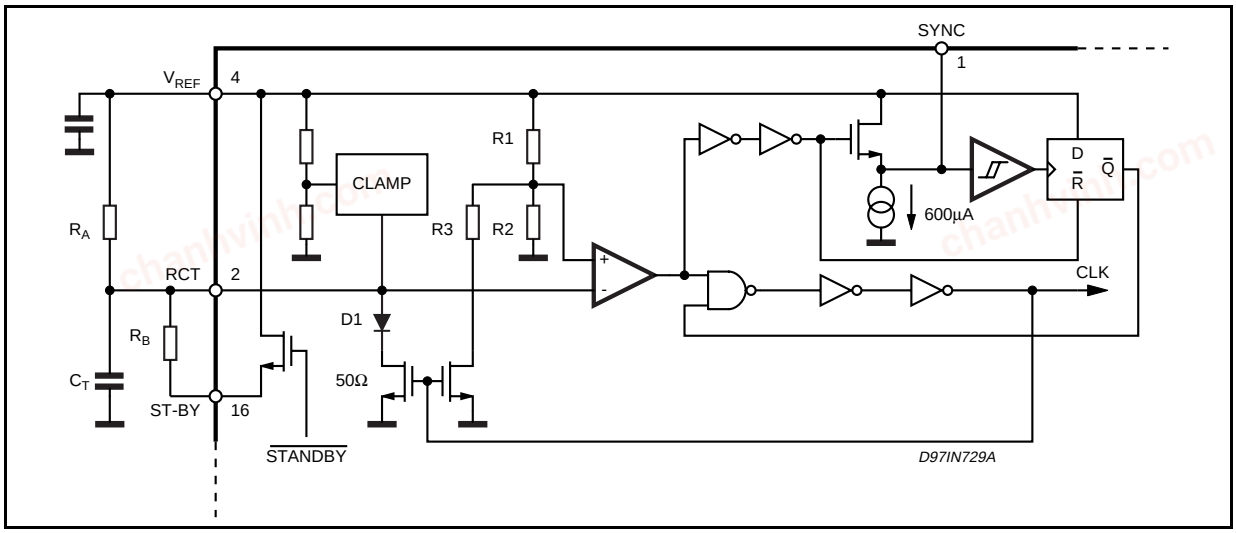
When the voltage on C_T reaches 3V, the capacitor is quickly internally discharged. As the voltage has dropped to 1V it starts being charged again.

Figure 22. Synchronizing the L5991.



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Figure 23. Oscillator and synchronization internal schematic.



The oscillation frequency can be established with the aid of the diagrams of fig. 14, where R_T will be intended as the parallel of R_A and R_B in normal operation and $R_T = R_A$ in standby, or considering the following approximate relationships:

$$f_{osc} \cong \frac{1}{C_T \cdot (0.693 \cdot (R_A // R_B) + K_T)} \quad (1),$$

which gives the normal operating frequency, and:

$$f_{SB} \cong \frac{1}{C_T \cdot (0.693 \cdot R_A + K_T)} \quad (2),$$

which gives the standby frequency, that is the one the converter will operate at when lightly loaded.

In the above expressions, RA // RB means:

$$R_A // R_B = \frac{R_A \cdot R_B}{R_A + R_B},$$

while K_T is defined as:

$$K_T = \begin{cases} 90 & V_{15} = VREF \\ 160 & V_{15} = GND/OPEN \end{cases} \quad (3),$$

and is related to the duration of the falling-edge of the sawtooth:

$$T_d \approx 30 \cdot 10^{-9} + K_T \cdot C_T \quad (4).$$

T_d is also the duration of the sync pulses delivered at pin 1 and defines the upper extreme of the duty cycle range, D_x (see pin 15 for D_X definition and calculation) since the output is held low during the falling edge.

In case V15 is connected to VREF, however, the switching frequency will be a half the values taken from fig. 14 or resulting from (1) and (2).

To prevent the oscillator frequency from switching back and forth from f_{osc} to f_{SB}, the ratio f_{osc} / f_{SB} must not exceed 5.5.

If during normal operation the IC is to be synchronized to an external oscillator, R_A, R_B and C_T should be selected for a f_{osc} lower than the master frequency in any condition (typically, 10-20%), depending also on the tolerance of the parts.

Pin 3. DC (Duty Cycle Control). By biasing this pin with a voltage between 1 and 3 V it is possible to set the maximum duty cycle between 0 and the upper extreme D_x (see pin 15).

If D_{max} is the desired maximum duty cycle, the voltage V3 to be applied to pin 3 is:

$$V_3 = 5 - 2^{(2-Dmax)} \quad (5)$$

D_{max} is determined by internal comparison between V3 and the oscillator ramp (see fig. 24), thus in case the device is synchronized to an external frequency f_{ext} (and therefore the oscillator amplitude is reduced), (5) changes into:

$$V_3 = 5 - 4 \cdot \exp\left(-\frac{D_{max}}{R_T \cdot C_T \cdot f_{ext}}\right) \quad (6)$$

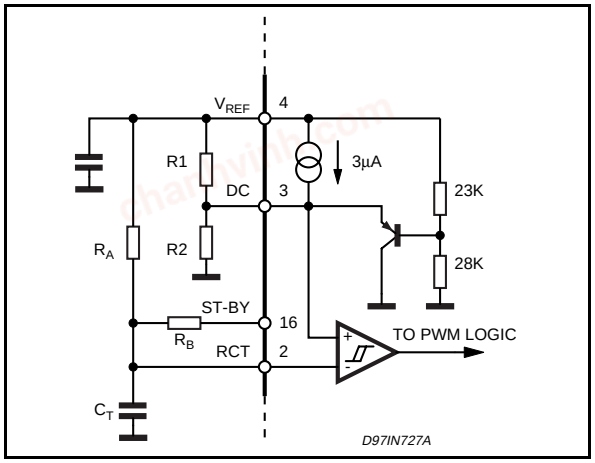
A voltage below 1V will inhibit the driver output stage. This could be used for a not-latched device disable, for example in case of overvoltage protection (see application ideas).

If no limitation on the maximum duty cycle is required (i.e. $D_{MAX} = D_X$), the pin has to be left floating. An internal pull-up (see fig. 24) holds the voltage above 3V. Should the pin pick up noise (e.g.

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during ESD tests), it can be connected to VREF through a 4.7kΩ resistor.

Figure 24. Duty cycle control.



Pin 4. VREF (Reference Voltage). The device is provided with an accurate voltage reference (5V±1.5%) able to deliver some mA to an external circuit.
A small film capacitor (0.1 µF typ.), connected between this pin and SGND, is recommended to ensure the stability of the generator and to prevent noise from affecting the reference.
Before device turn-on, this pin has a sink current capability of 0.5mA.

Pin 5. VFB (Error Amplifier Inverting Input). The feedback signal is applied to this pin and is compared to the E/A internal reference (2.5V). The E/A output generates the control voltage which fixes the duty cycle.

The E/A features high gain-bandwidth product, which allows to broaden the bandwidth of the overall control loop, high slew-rate and current capability, which improves its large signal behavior. Usually the compensation network, which stabilizes the overall control loop, is connected between this pin and COMP (pin 6).

Pin 6. COMP (Error Amplifier Output). Usually, this pin is used for frequency compensation and the relevant network is connected between this pin and VFB (pin 5). Compensation networks towards ground are not possible since the L5991 E/A is a voltage mode amplifier (low output impedance). See application ideas for some example of compensation techniques.
It is worth mentioning that the calculation of the part values of the compensation network must take the standby frequency operation into account. In particular, this means that the open-loop crossover frequency must not exceed $f_{SB}/4 \div f_{SB}/5$.
The voltage on pin 6 is monitored in order to reduce the oscillator frequency when the converter is lightly loaded (standby).

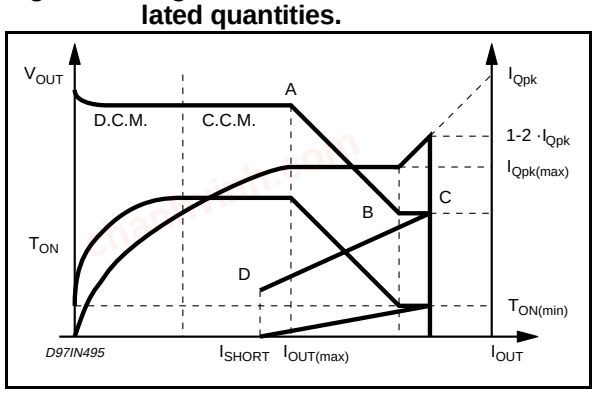
Pin 7. SS (Soft-Start). At device start-up, a capacitor (Css) connected between this pin and SGND (pin 12) is charged by an internal current generator, ISSC, up to about 7V. During this ramp, the E/A output is clamped by the voltage across Css itself and allowed to rise linearly, starting from zero, up to the steady-state value imposed by the control loop. The maximum time interval during which the E/A is clamped, referred to as soft-start time, is approximately:

$$T_{ss} \cong \frac{3 \cdot R_{sense} \cdot I_{Qpk}}{I_{SSC}} \cdot C_{ss} \qquad (7)$$

where R_{sense} is the current sense resistor (see pin 13) and I_{Qpk} is the switch peak current (flowing through R_{sense}), which depends on the output load. Usually, C_{SS} is selected for a T_{SS} in the order of milliseconds.

As mentioned before, the soft-start intervenes also in case of severe overload or short circuit on the output. Referring to fig. 25, pulse-by-pulse current limitation is somehow effective as long as

Figure 25. Regulation characteristic and related quantities.



the ON-time of the power switch can be reduced (from A to B). After the minimum ON-time is reached (from B onwards) the current is out of control.

To prevent this risk, a comparator trips an overcurrent handling procedure, named 'hiccup' mode operation, when a voltage above 1.2V (point C) is detected on current sense input (ISEN, pin 13). Basically, the IC is turned off and then soft-started as long as the fault condition is detected. As a result, the operating point is moved abruptly to D, creating a foldback effect. Fig. 26 illustrates the operation.

The oscillation frequency appearing on the soft-start capacitor in case of permanent fault, referred to as 'hiccup" period, is approximately given by:

$$T_{hic} \cong 4.5 \cdot \left(\frac{1}{I_{SSC}} + \frac{1}{I_{SSD}} \right) \cdot C_{ss} \qquad (8)$$

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Since the system tries restarting each hiccup cycle, there is not any latchoff risk.

"Hiccup" keeps the system in control in case of short circuits but does not eliminate power components overstress during pulse-by-pulse limitation (from A to C). Other external protection circuits are needed if a better control of overloads is required.

Pin 8. VCC (Controller Supply). This pin supplies the signal part of the IC. The device is enabled as VCC voltage exceeds the start threshold and works as long as the voltage is above the UVLO threshold. Otherwise the device is shut down and the current consumption is extremely low (<150µA). This is particularly useful for reducing the consumption of the start-up circuit (in the simplest case, just one resistor), which is one of the most significant contributions to power losses in standby.

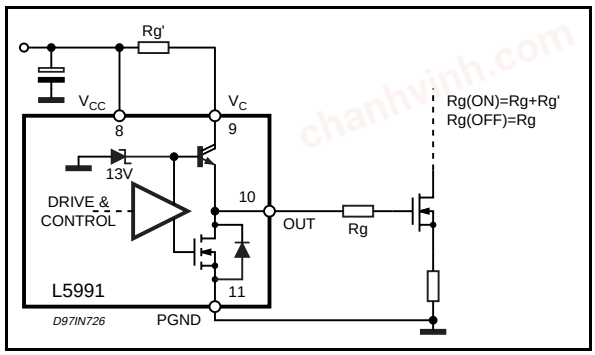
An internal Zener limits the voltage on VCC to 25V. The IC current consumption increases considerably if this limit is exceeded.

A small film capacitor between this pin and SGND (pin 12), placed as close as possible to the IC, is recommended to filter high frequency noise.

Pin 9. VC (Supply of the Power Stage). It supplies the driver of the external switch and therefore absorbs a pulsed current. Thus it is recommended to place a buffer capacitor (towards PGND, pin 11, as close as possible to the IC) able to sustain these current pulses and in order to avoid them inducing disturbances.

This pin can be connected to the buffer capacitor directly or through a resistor, as shown in fig. 27, to control separately the turn-on and turn-off speed of the external switch, typically a PowerMOS. At turn-on the gate resistance is $R_g + R_{g'}$, at turn-off is R_g only.

Figure 27. Turn-on and turn-off speeds adjustment.

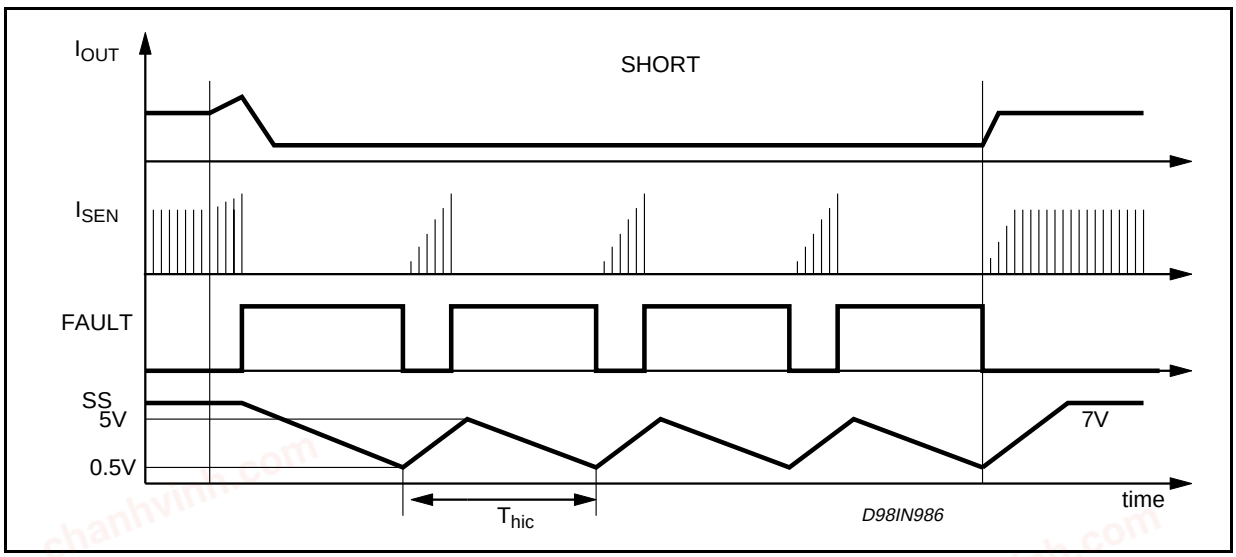


Pin 10. OUT (Driver Output). This pin is the output of the driver stage of the external power switch. Usually, this will be a PowerMOS, although the driver is powerful enough to drive BJT's (1.6A source, 2A sink, peak).

The driver is made up of a totem pole with a high-side NPN Darlington and a low-side VDMOS, thus there is no need of an external diode clamp to prevent voltage from going below ground. An internal clamp limits the voltage delivered to the gate at 13V. Thus it is possible to supply the driver (Pin 9) with higher voltages without any risk of damage for the gate oxide of the external MOS. The clamp does not cause any additional increase of power dissipation inside the chip since the current peak of the gate charge occurs when the gate voltage is few volts and the clamp is not active. Besides, no current flows when the gate voltage is 13V, steady state.

Under UVLO conditions an internal circuit (shown

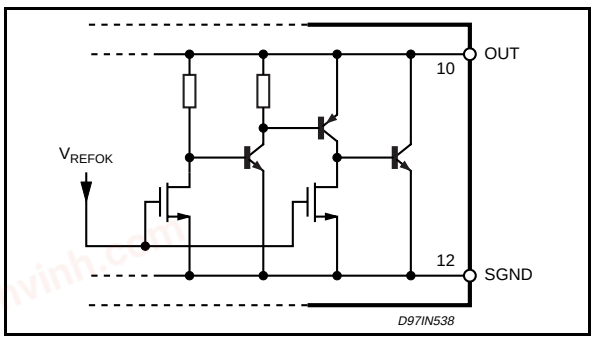
Figure 26. Hiccup mode operation.



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in fig.28) holds the pin low in order to ensure that the external MOS cannot be turned on accidentally. The peculiarity of this circuit is its ability to mantain the same sink capability (typically, 20mA @ 1V) from V_{CC} = 0V up to the start-up threshold. When the threshold is exceeded and the L5991 starts operating, V_{REFOK} is pulled high (refer to fig. 28) and the circuit is disabled.
It is then possible to omit the "bleeder" resistor (connected between the gate and the source of the MOS) ordinarily used to prevent undesired switching-on of the external MOS because of some leakage current.

Figure 28. Pull-Down of the output in UVLO.



Pin 11. PGND (Power Ground). The current loop during the discharge of the gate of the external MOS is closed through this pin. This loop should be as short as possible to reduce EMI and run separately from signal currents return.

Pin 12. SGND (Signal Ground). This ground references the control circuitry of the IC, so all the ground connections of the external parts related to control functions must lead to this pin. In laying out the PCB, care must be taken in preventing switched high currents from flowing through the SGND path.

Pin 13. ISEN (Current Sense). This pin is to be connected to the "hot" lead of the current sense resistor R_{sense} (being the other one grounded), to get a voltage ramp which is an image of the current of the switch (I_Q). When this voltage is equal to:

$$V_{13pk} = I_{Qpk} \cdot R_{sense} = \frac{V_{COMP} - 1.4}{3} \quad (9)$$

the conduction of the switch is terminated.
To increase the noise immunity, a "Leading Edge Blanking" of about 100ns is internally realized as shown in fig. 29. Because of that, the smoothing RC filter between this pin and R_{sense} could be removed or, at least, considerably reduced.

Pin 14. DIS (Device Disable). When the voltage on pin 14 rises above 2.5V the IC is shut down and it is necessary to pull VCC (IC supply voltage, pin 8) below the UVLO threshold to allow the device to restart.

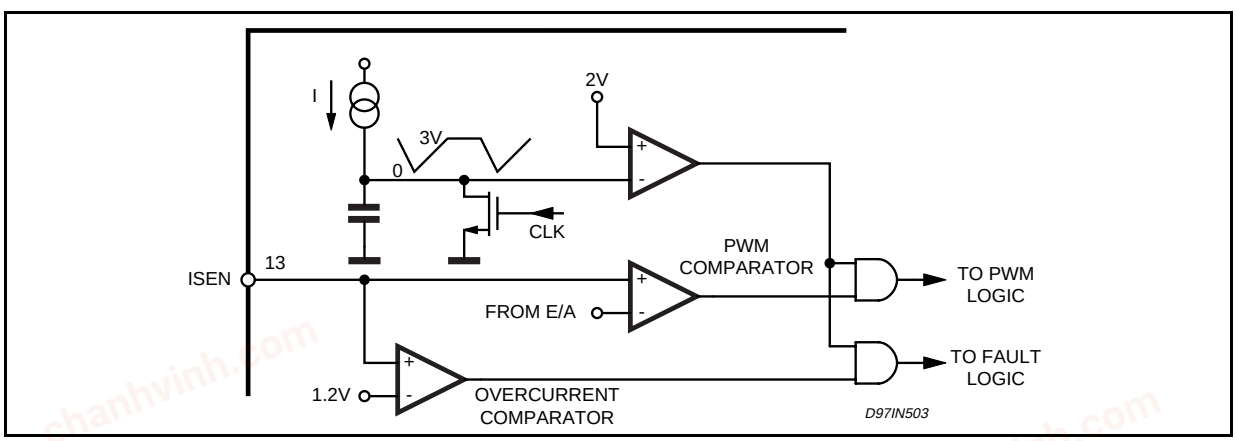
The pin can be driven by an external logic signal in case of power management, as shown in fig. 30. It is also possible to realize an overvoltage protection, as shown in the section " Application Ideas".If used, bypass this pin to ground with a filter capacitor to avoid spurious activation due to noise spikes. If not, it must be connected to SGND.

Pin 15. DC-LIM (Maximum Duty Cycle Limit). The upper extreme, Dx, of the duty cycle range depends on the voltage applied to this pin. Approximately,

$$D_x \cong \frac{R_T}{R_T + 230} \quad (10)$$

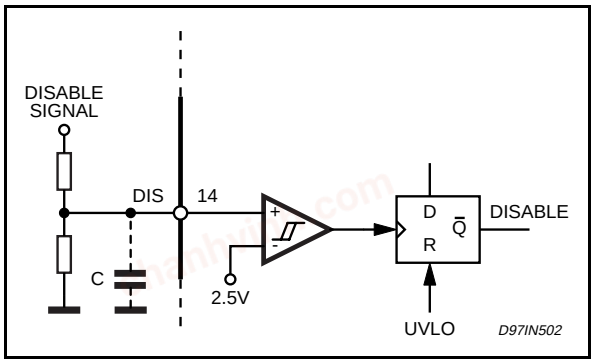
if DC-LIM is grounded or left floating. Instead,

Figure 29. Internal LEB.



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Figure 30. Disable (Latched).



connecting DC-LIM to VREF (half duty cycle option), Dx will be set approximately at:

$$D_X \cong \frac{R_T}{2 \cdot R_T + 260} \quad (11)$$

and the output switching frequency will be halved with respect to the oscillator one because an internal T flip-flop (see block diagram) is activated. Fig. 31 shows the operation.

The half duty cycle option speeds up the discharge of the timing capacitor C_T (in order to get duty cycles as close to 50% as possible) so the oscillator frequency - with the same timing components will be slightly higher.

Pin 16. S-BY (Standby Function). The resistor R_B, along with R_A, sets the operating frequency of the oscillator in normal operation (f_{osc}). In fact, as long as the $\overline{\text{STANDBY}}$ signal is high, the pin is internally connected to the reference voltage VREF by a N-channel FET (see fig. 32), so the timing capacitor C_T is charged through R_A and R_B. When the $\overline{\text{STANDBY}}$ signal goes low the N-channel FET is turned off and the pin becomes floating. R_B is

Figure 31. Half duty cycle option.

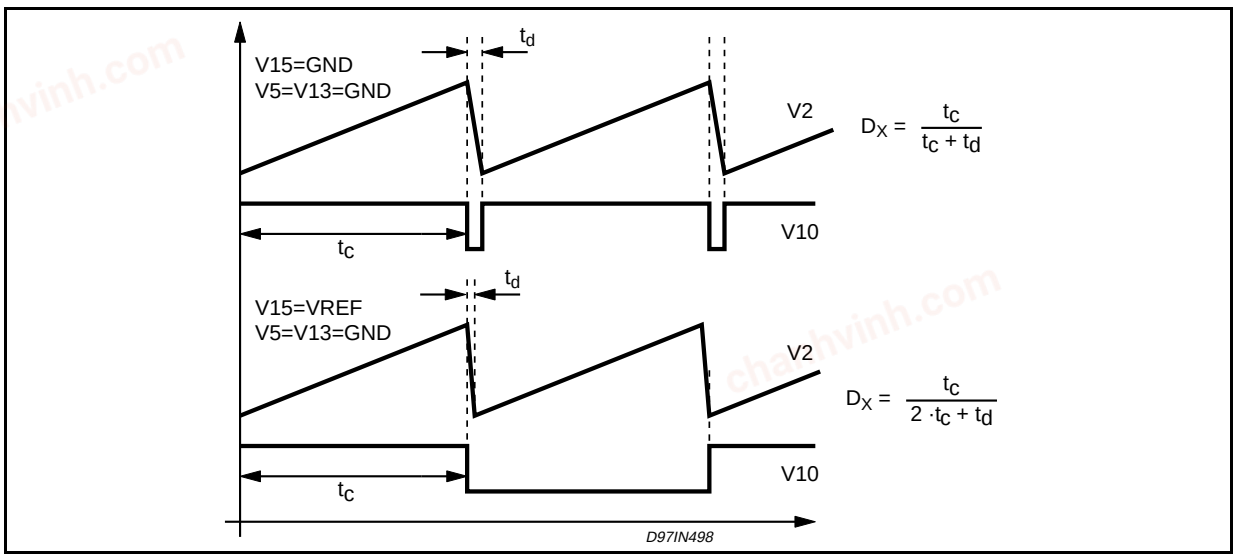
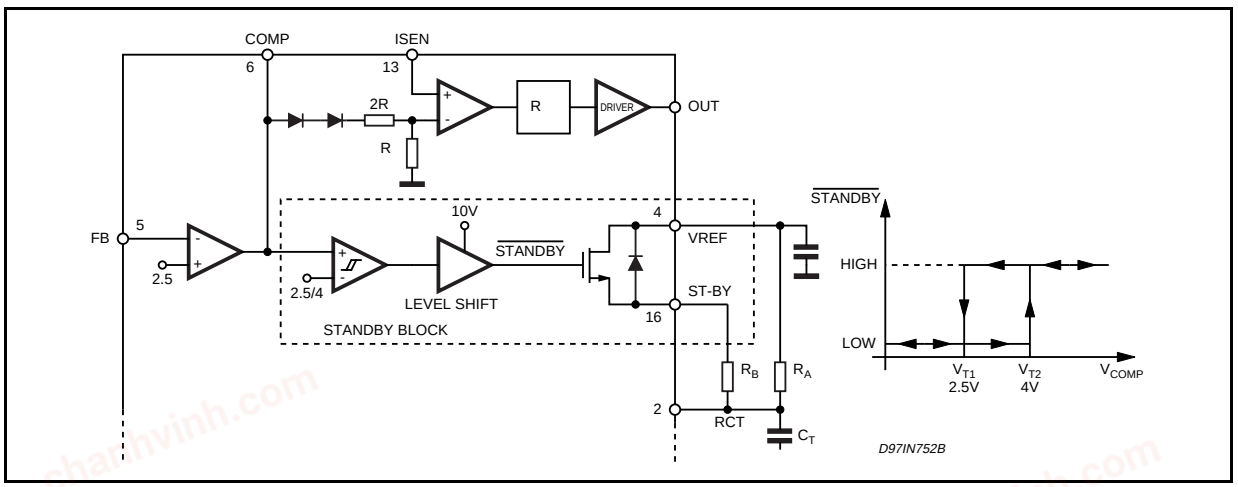


Figure 32. Standby function internal schematic and operation.



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now disconnected and C_T is charged through R_A only. In this way the oscillator frequency (f_{SB}) will be lower. Refer to pin 2 description to see how to calculate the timing components.

Typical values for V_{T1} and V_{T2} are 2.5 V and 4V respectively. This 1.5V hysteresis is enough to prevent undesired frequency change up to a 5.5 to 1 f_{osc}/ f_{SB} ratio.

The value of V_{T1} is such that in a discontinuous flyback the standby frequency is activated when the input power is about 13% of the maximum. If necessary, it is possible to decrease the power threshold below 13% by adding a DC offset (V_o) on the current sense pin (13, ISEN). This will also allow a frequency change greater than 5.5 to 1.

The following equations, useful for design, apply:

$$P_{inSB} = \frac{1}{2} \cdot L_P \cdot f_{osc} \cdot \left(\frac{0.367 - V_o}{R_{sense}} \right)^2 \quad (12),$$

$$P_{inNO} = \frac{1}{2} \cdot L_P \cdot f_{SB} \cdot \left(\frac{0.867 - V_o}{R_{sense}} \right)^2 \quad (13),$$

$$\frac{f_{osc}}{f_{SB}} < \left(\frac{0.867 - V_o}{0.367 - V_o} \right)^2 \quad (14),$$

where P_{inSB} is the input power below which the L5991 recognizes a light load and switches the oscillator frequency from f_{osc} to f_{SB}, P_{inNO} is the input power above which the L5991 switches back from f_{SB} to f_{osc} and L_p the primary inductance of the flyback transformer.

Connect to Vref or leave open this pin when stand-by function is not used.

Layout hints

Generally speaking a proper circuitboard layout is vital for correct operation but is not an easy task. Careful component placing, correct traces routing, appropriate traces widths and, in case of high voltages, compliance with isolation distances are the major issues. The L5991 eases this task by putting two pins at disposal for separate current returns of bias (SGND) and switch drive currents (PGND) The matter is complex and only few important points will be here reminded.

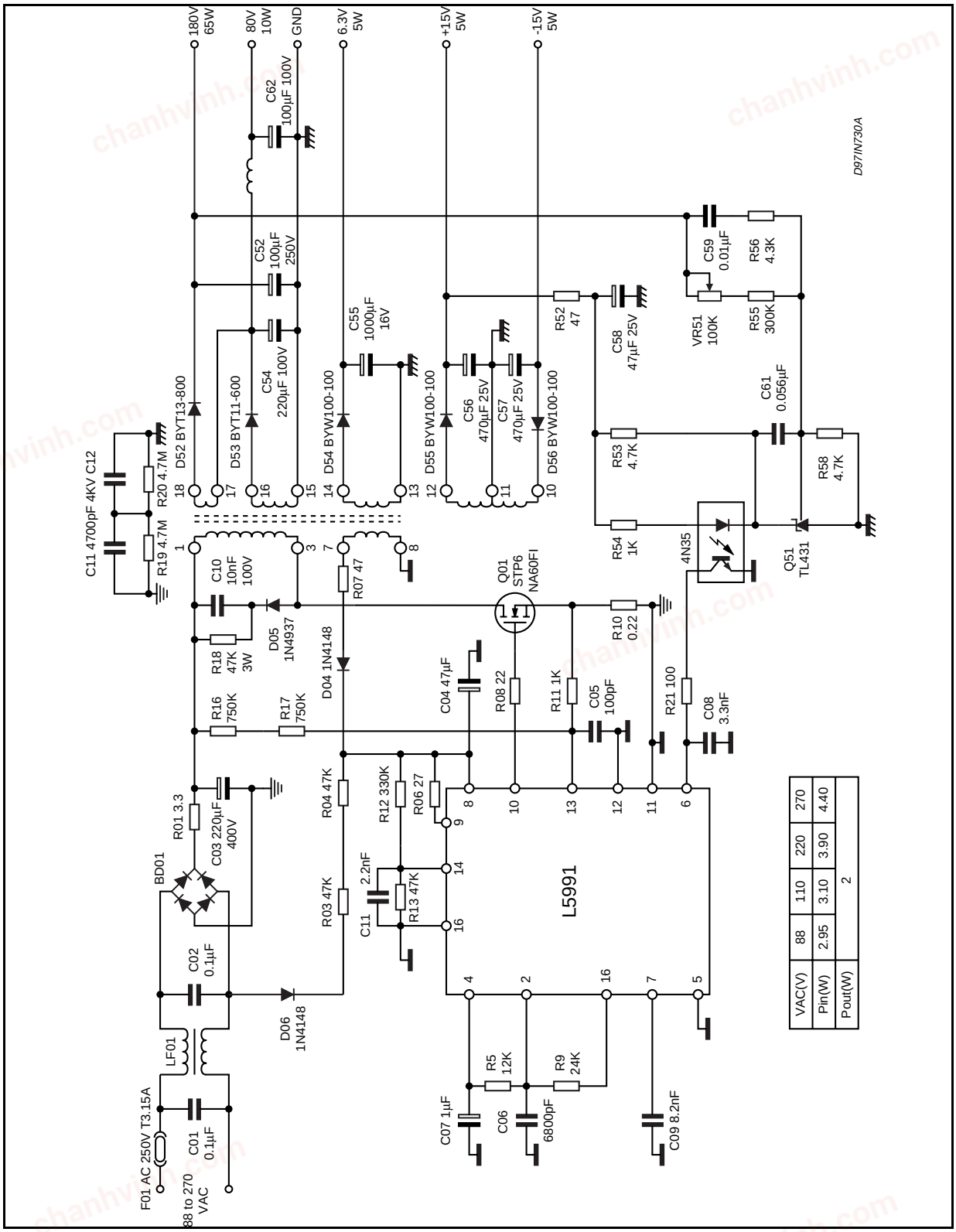
1) All current returns (signal ground, power ground, shielding, etc.) should be routed separately and should be connected only at a single ground point.
2) Noise coupling can be reduced by minimizing the area circumscribed by current loops. This applies particularly to loops where high pulsed currents flow.
3) For high current paths, the traces should be doubled on the other side of the PCB whenever possible: this will reduce both the resistance and the inductance of the wiring.
4) Magnetic field radiation (and stray inductance) can be reduced by keeping all traces carrying switched currents as short as possible.
5) In general, traces carrying signal currents should run far from traces carrying pulsed currents or with quickly swinging voltages. From this viewpoint, particular care should be taken of the high impedance points (current sense input, feedback input, ...). It could be a good idea to route signal traces on one PCB side and power traces on the other side.
6) Provide adequate filtering of some crucial points of the circuit, such as voltage references, IC's supply pins, etc.

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APPLICATION IDEAS

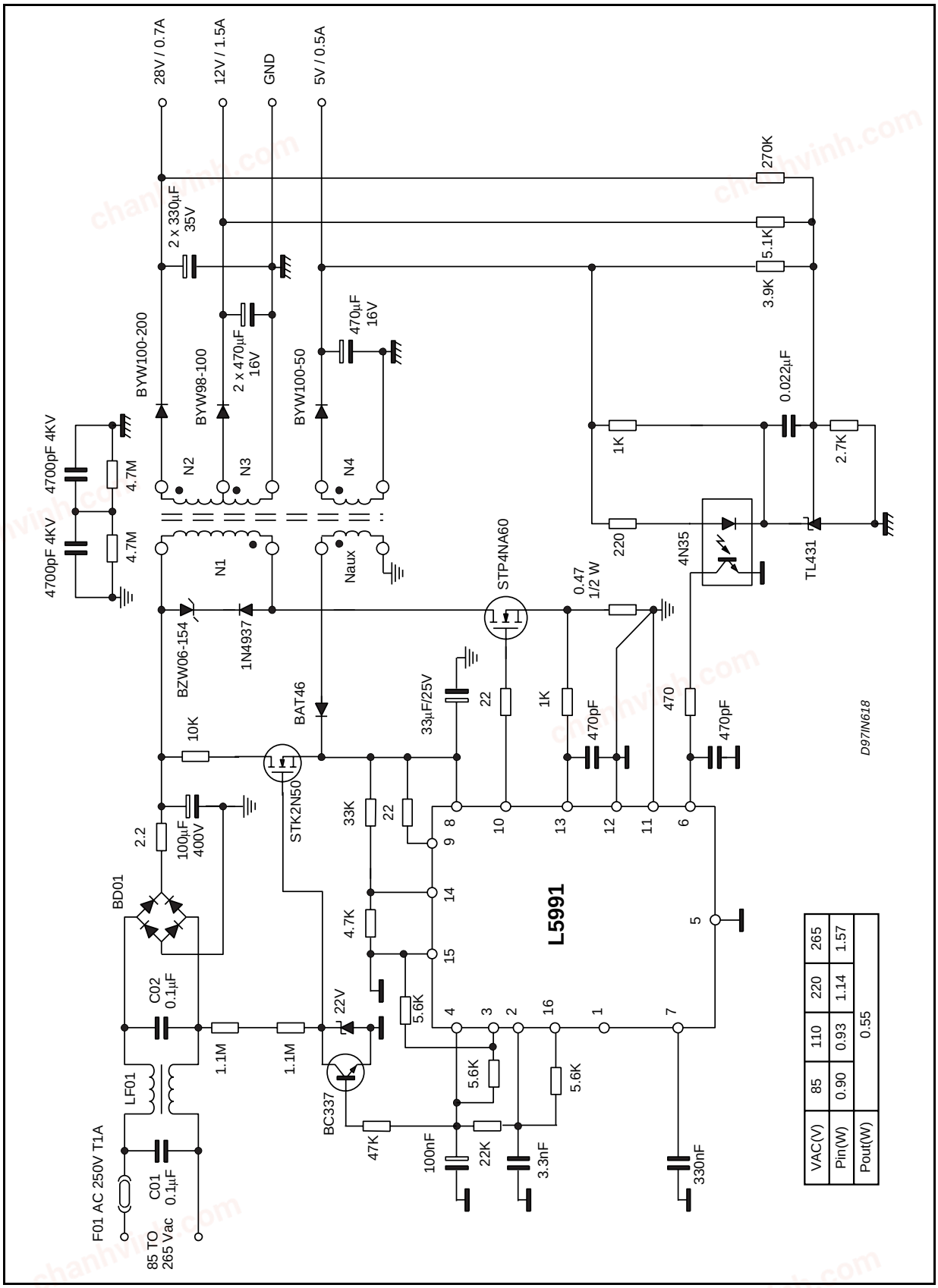
Here follows a series of ideas/suggestions aimed at either improving performance or solving common application problems of L5991 based supplies.

Figure 33. Typical application circuit for computer monitors (90W).



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Figure 34. Typical application circuit for inkjet printers (40W).



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Figure 35. Standby thresholds adjustment.

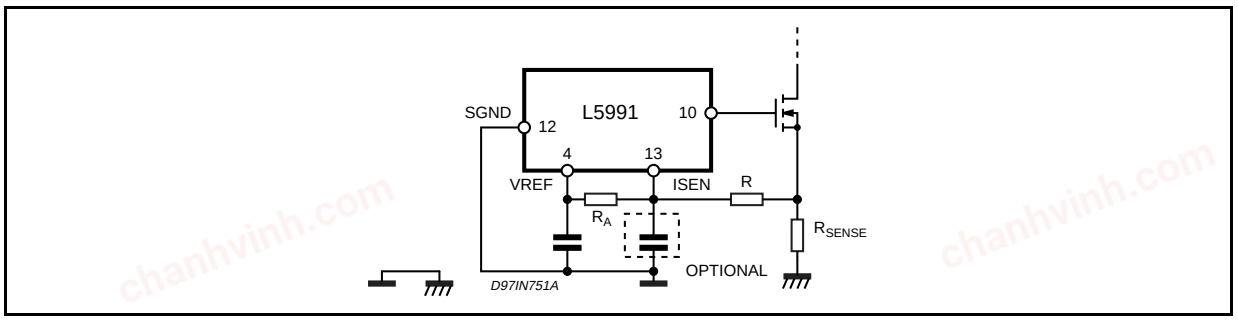


Figure 36. Isolated MOSFET Drive & Current Transformer Sensing in 2-switch Topologies.

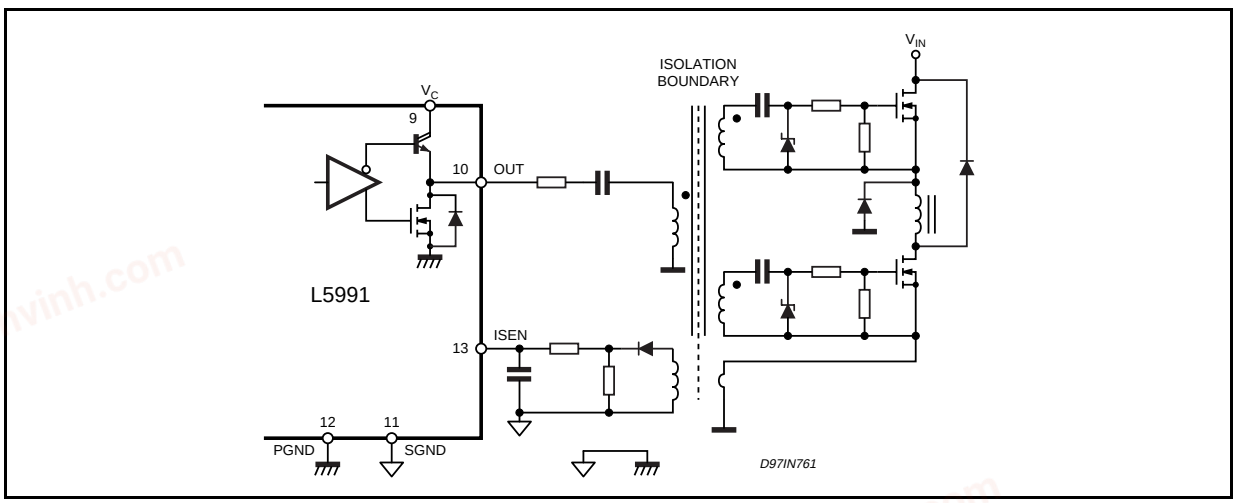


Figure 37. Low consumption start-up.

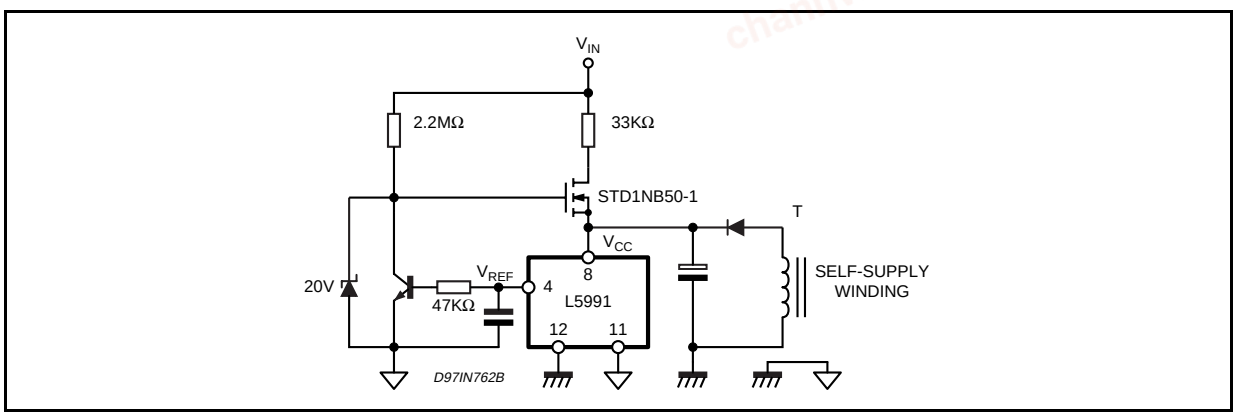
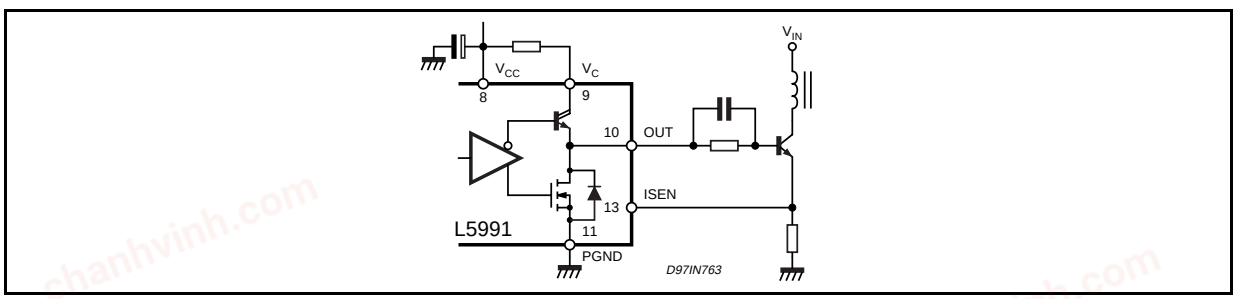
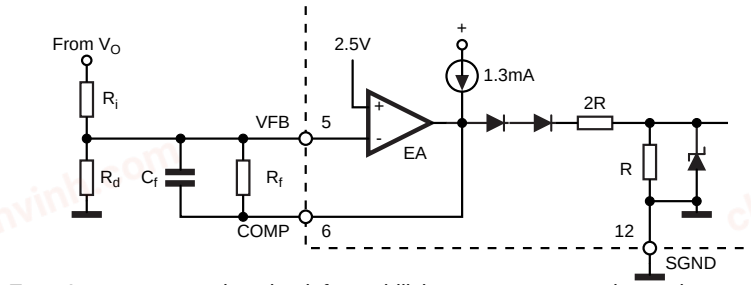


Figure 38. Bipolar transistor driver.

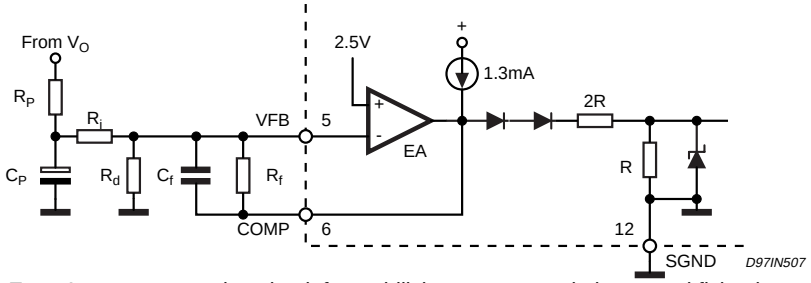


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Figure 39. Typical E/A compensation networks.



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 40. Feedback with optocoupler.

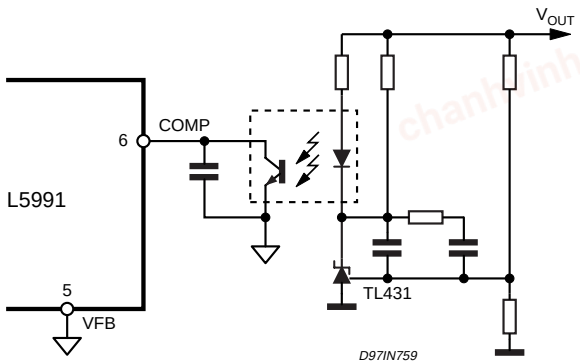
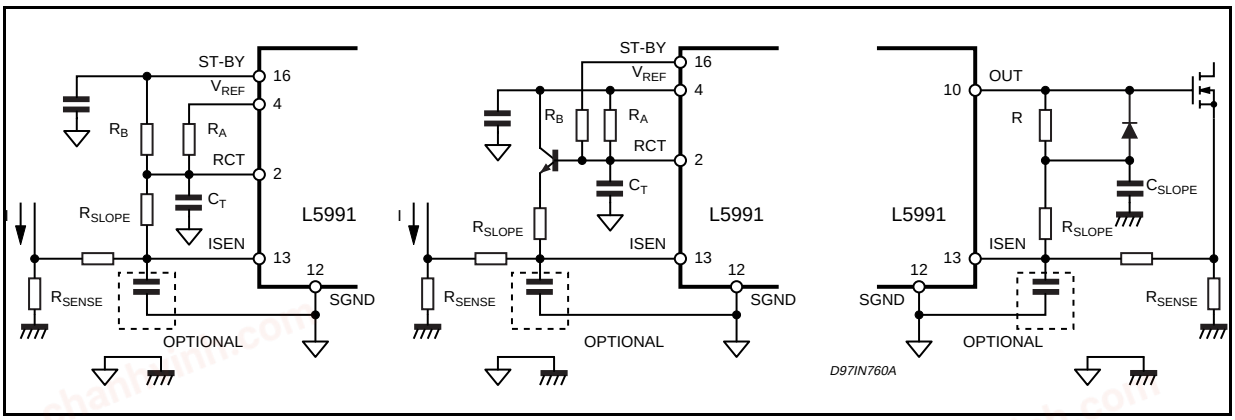


Figure 41. Slope compensation techniques.



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Figure 42. Protection against overvoltage/feedback disconnection (latched)

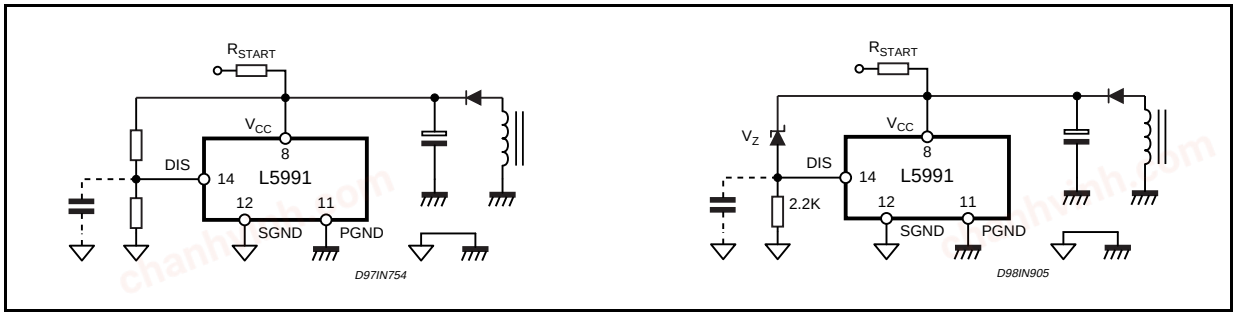


Figure 43 Protection against overvoltage/feedback disconnection (not latched)

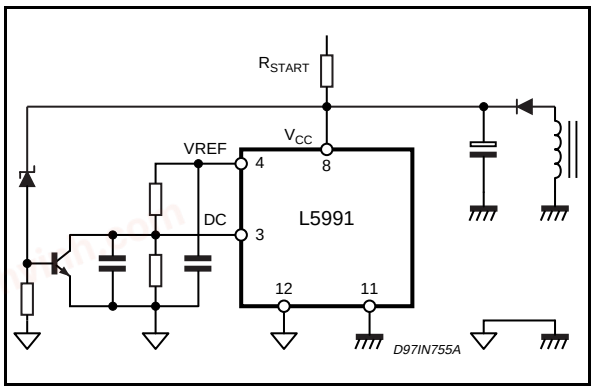


Figure 44. Device shutdown on overcurrent

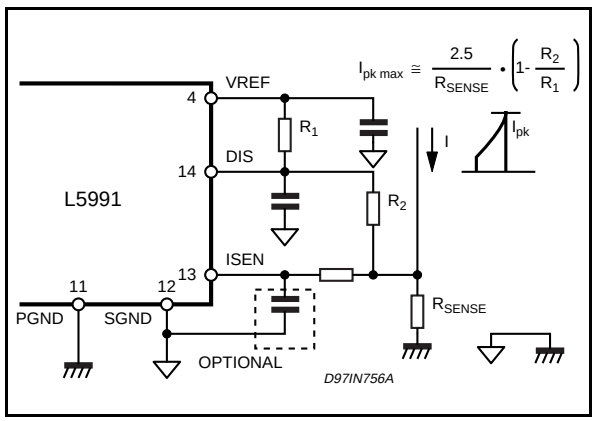


Figure 45. Constant power in pulse-by-pulse current limitation (flyback discontinuous)

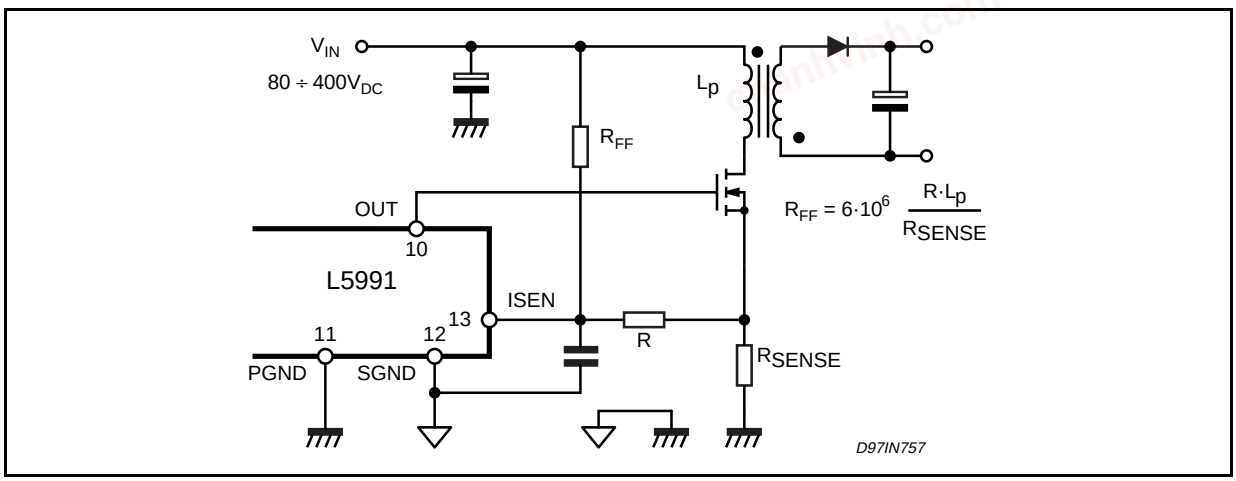
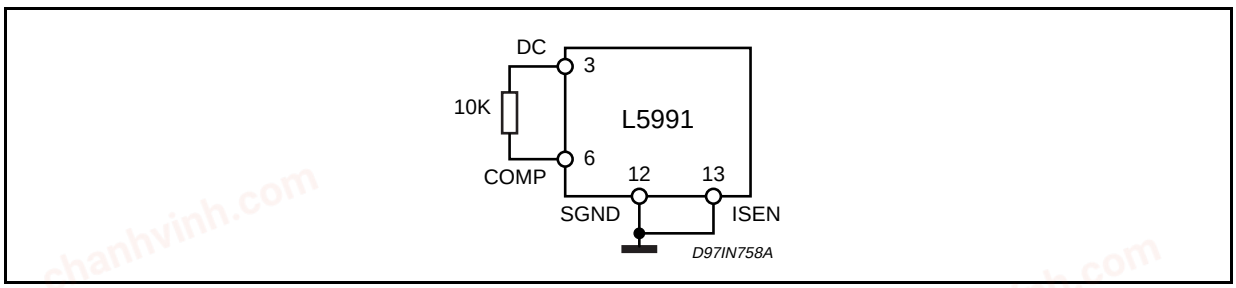


Figure 46. Voltage mode operation.



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Figure 47. Device shutdown on mains undervoltage.

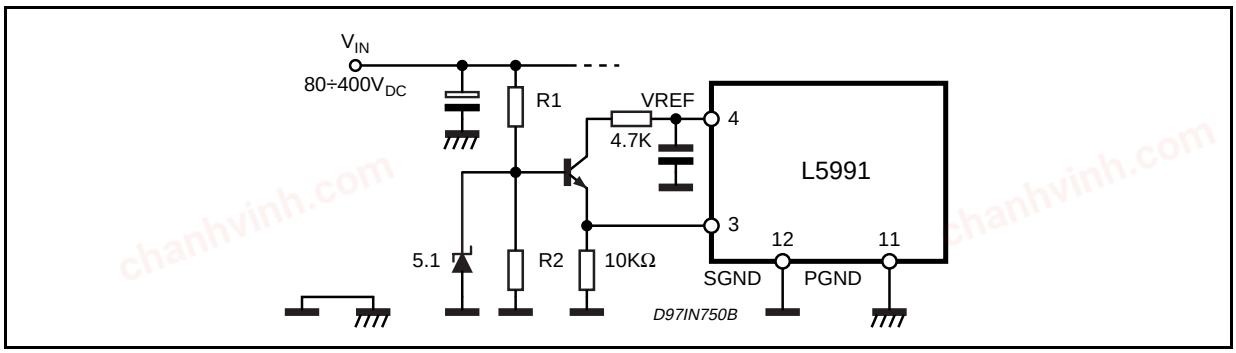
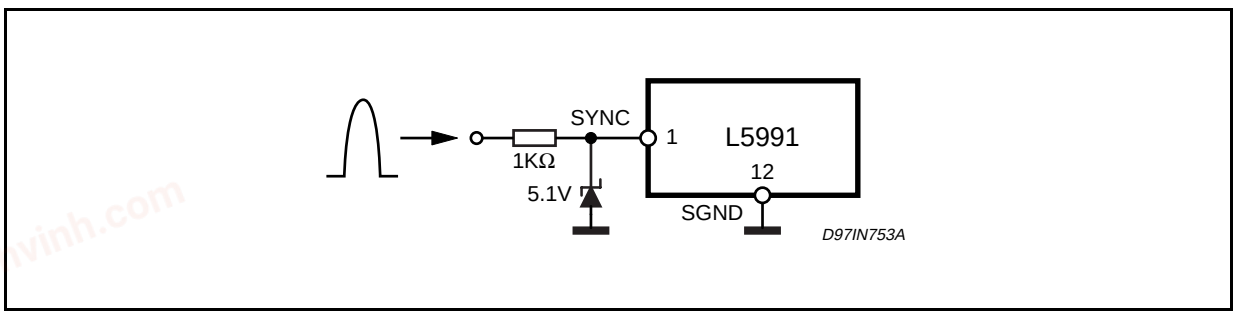


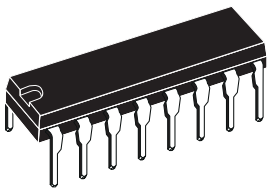
Figure 48. Synchronization to flyback pulses (for monitors).



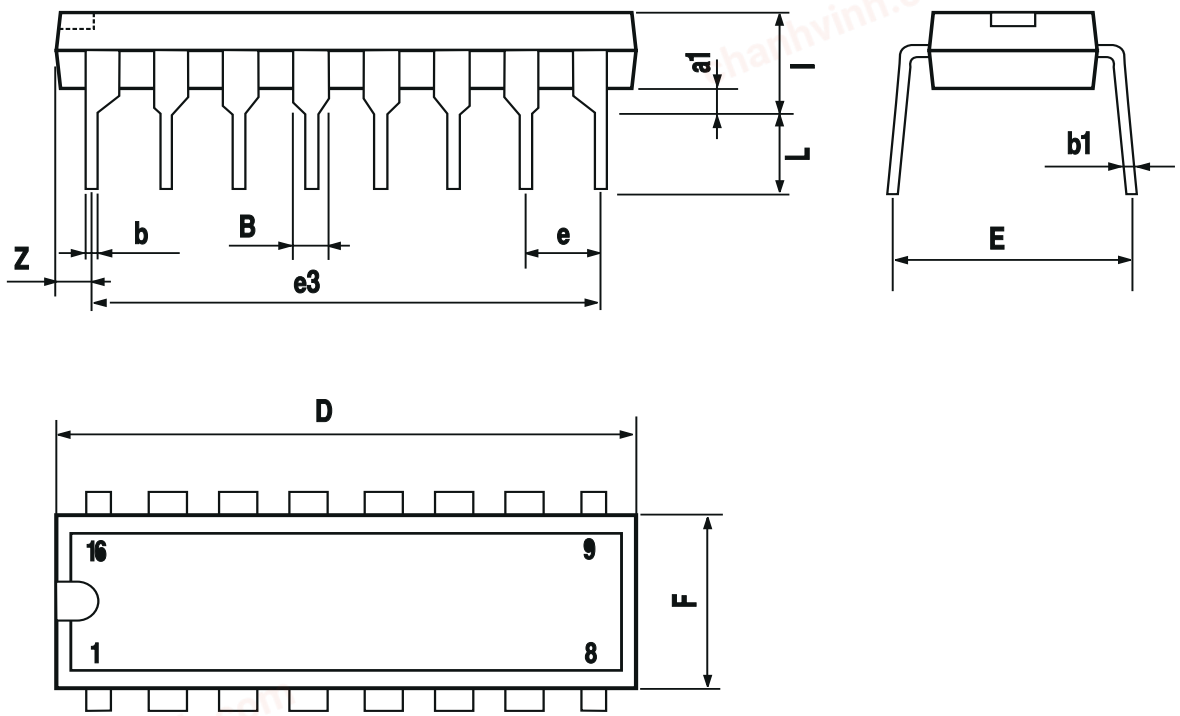
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DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



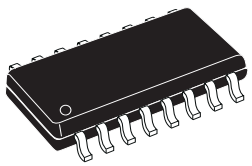
DIP16



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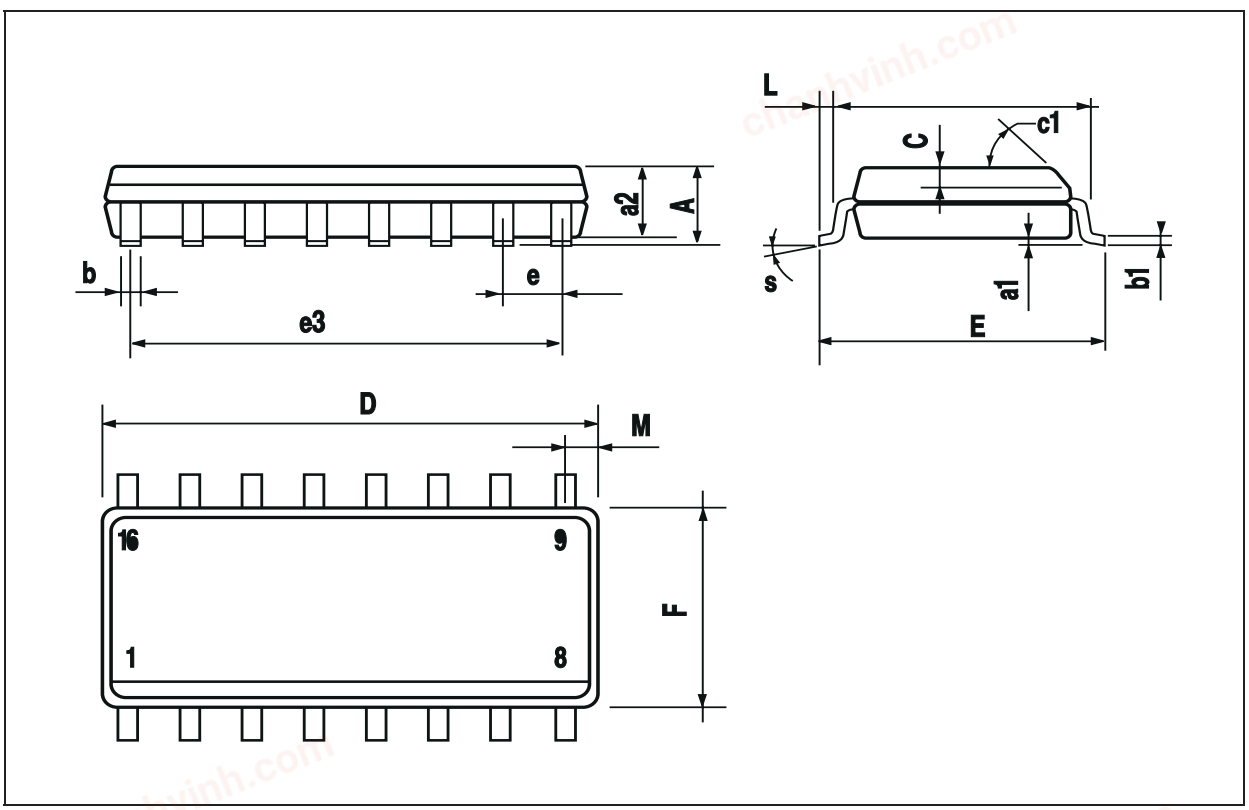
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.62			0.024
S	8°(max.)					

OUTLINE AND MECHANICAL DATA



SO16 Narrow

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).



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