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IPS8200HQ, IPS8200HQ-1

Datasheet

Octal high-side smart power solid-state relay with serial/parallel selectable interface on-chip







Product status link
IPS8200HQ
IPS8200HQ -1

Features

- Voltage operating range 10.5 V to 36 V
- UVLO with hysteresis
- Output current: 0.7 A or 1.0 A (IPS8200HQ or IPS8200HQ-1) per channel
- Low supply current in OFF (1 mA) and ON (5.3 mA) states
- 5 V and 3.3 V compatible I/Os
- Selectable interface on logic side SPI or parallel
- 5 MHz SPI (8 or 16-bits) with output enable, daisy chain, and MCU freeze detection
- 100 mA DC/DC with integrated boot diode and adjustable output voltage
- 4x2 LED matrix for efficient outputs state LEDs driving
- Can drive all types of loads (resistive, capacitive, and inductive)
- Per-channel overload and short-circuit protection
- Per-channel/independent overtemperature protection
- Fast demagnetization of inductive loads (Vout clamp)
- Overvoltage protection (VCC clamping)
- Loss of GND protection
- Power Good (supply voltage level) diagnostic
- Common fault open drain output
- IC warning temperature detection
- VFQFPN-48L (8x6 mm) package
- Designed to meet IEC61131-2, IEC61000-4-2, IEC61000-4-4, and IEC61000-4-5

Application

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines

Description

The IPS8200HQ and IPS8200HQ -1 are monolithic 8-channel drivers, designed using STMicroelectronics™ VIPower™ technology, and intended to drive any kind of load with one side connected to the ground. Both ICs operates from 10.5 V to 36 V and feature a very low supply current, parallel or 4-wire SPI control interface, a 4x2 LED matrix, and a micropower step-down switching regulator with a peak current control loop mode.

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The SPI interface (enabled by SEL2 pin = H) can work up to 5 MHz in 8-bits (SEL1 = L), or 16-bits (SEL1 = H) with a parity check and extended diagnostic (DC/DC operation, case overtemperature, SPI Communication Fail, and Power Good) information. In SPI mode the daisy chain is allowed, and both the OUT_EN signal and the MCU freeze detection by watchdog are available. If enabled (WD_EN voltage above 25% of VREG), the watchdog circuitry generates an internal reset on expiry of the internal watchdog timer. The watchdog timer reset can be achieved by applying a negative pulse on the WD pin. The watchdog timer can be programmed by the set voltage on the WD_EN pin.

The internal LED matrix driver circuitry (4 rows, 2 columns) allows the efficient driving of the 8 LEDs reporting the on/off status of each of the 8 outputs. The VREG pin supplies both the logic output buffers and LED matrix. The 100 mA output current capability of the integrated step-down (featuring overload and short-circuit conditions) can be used to supply both the VREG pin and other application components (for example: digital isolators or optocouplers).

Active per-channel current limitations (0.7 A and 1.0 A for IPS8200HQ and IPS8200HQ-1, respectively), combined with channel-independent thermal shutdown, protect the circuitry against overload and short circuits. Built-in thermal shutdown protects each channel from overtemperature and overload: each overheated channel automatically turns OFF after its junction temperature triggers the protection threshold (T_{TSD}). The channel turns back ON if its junction temperature decreases lower than the restart threshold (T_R). An additional case temperature sensor protects the whole chip against overtemperature: if the case temperature triggers the T_{CSD} threshold then overloaded channels are turned OFF and restart only when the case temperature decreases to the reset threshold (T_{CR}). Non-overloaded channels continue to operate normally.

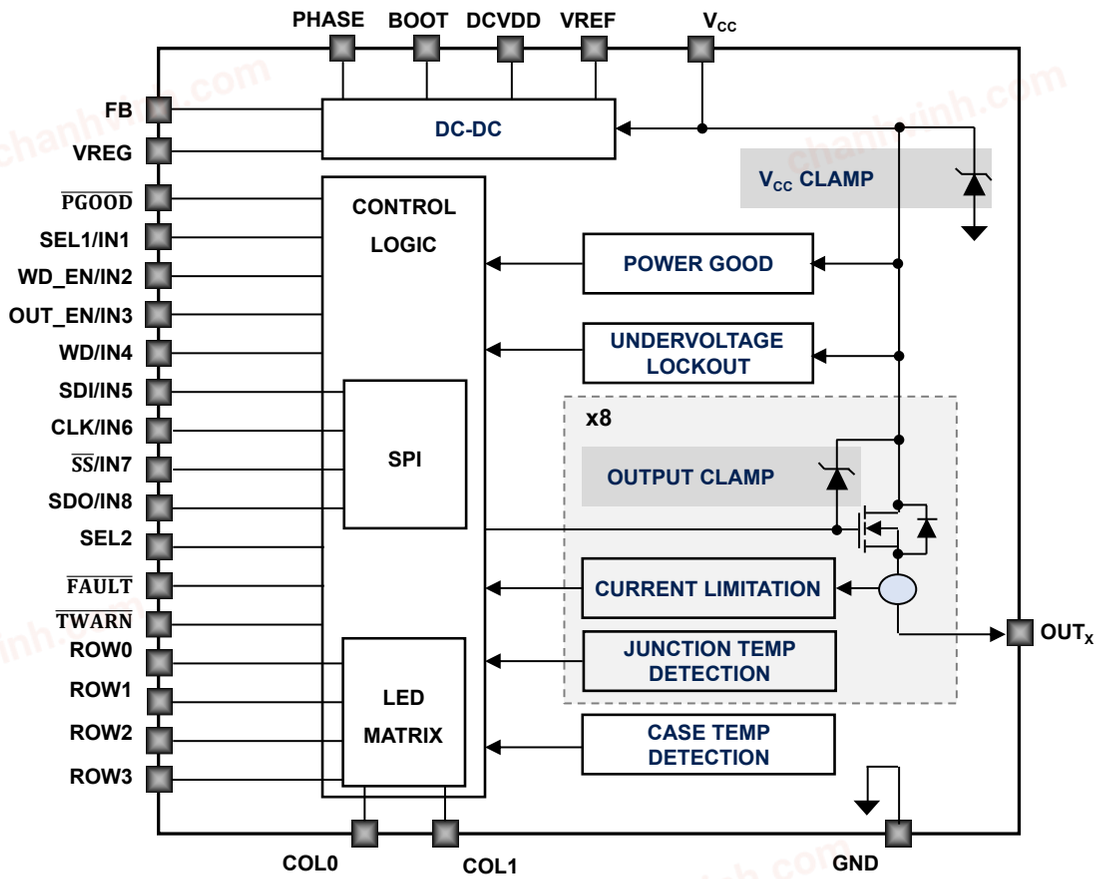
Loss of GND protection guarantees automatic turn-off of the outputs in case of a ground wire break.

Dedicated diagnostic pins report the detection of: invalid voltage range on VCC rail ($\overline{PG}$ pin), caseovertemperature ($\overline{TWARN}$ pin), SPI fault, or junction overtemperature ($\overline{FAULT}$ pin).

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1 Block diagram

Figure 1. **Block diagram**



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2 Pin connection

Figure 2. **Pin connection (top through view)**

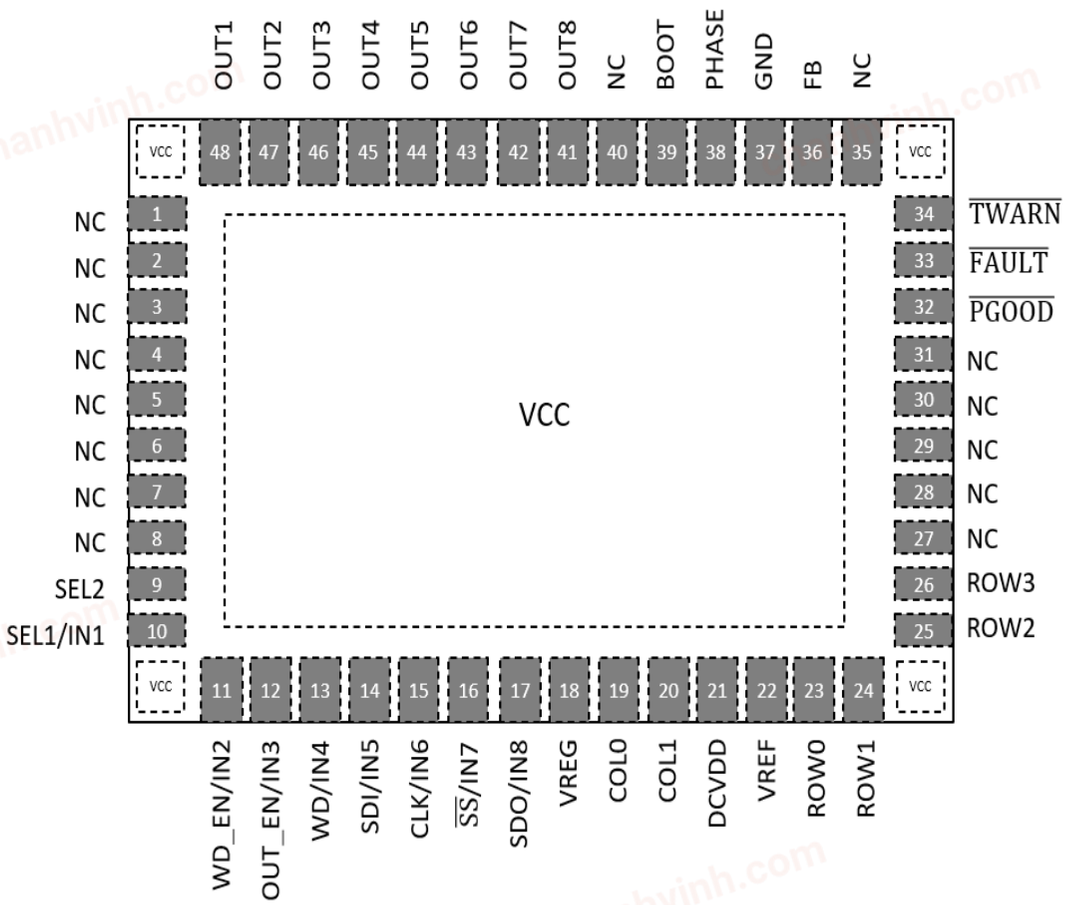


Table 1. **Pin description**

Pin	Name	Type	Description	
			SPI mode	Parallel mode
1 to 8; 27 to 31; 35, 40	NC	-	Not connected.	
9	SEL2	Logic input	SEL2 = H.	SEL2 = GND.
10	SEL1/IN1	Logic input	SEL1 = L or H selects the SPI 8-bits or 16-bits option.	IN1 = L/H drives off/on the OUT1.
11	WD_EN/IN2	Logic/analog input	WD_EN = H or L enables or disables the watchdog feature.	IN2 = L/H drives off/on the OUT2.
12	OUT_EN/IN3	Logic input	OUT_EN = L or H forces off all OUT_X or enables the control by SPI.	IN3 = L/H drives off/on the OUT3.
13	WD/IN4	Logic input	WD is the watchdog input: the internal watchdog counter is cleared on the falling edges.	IN4 = L/H drives off/on the OUT4.
14	SDI/IN5	Logic input	Connected to the MOSI port of the MCU.	IN5 = L/H drives off/on the OUT5.
15	CLK/IN6	Logic input	Serial clock/channel 6 input. Connected to the SPI Clock port of the MCU.	IN6 = L/H drives off/on the OUT6.
16	$\overline{SS}$ /IN7	Logic input	Connected to the GPIO port of the MCU controlling the SPI chip select.	IN7 = L/H drives off/on the OUT7.
17	SDO/IN8	Logic input/output	Connected to the MISO port of the MCU.	IN8 = L/H drives off/on the OUT8.

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Pin	Name	Type	Description	
			SPI mode	Parallel mode
18	VREG	Power supply	Supply of SPI, Inputs and LED Matrix.	
19	COL0	Open source output	LED matrix column driver (odd OUT_X).	
20	COL1	Open source output	LED matrix column driver (even OUT_X).	
21	DCVDD	Analog output	Internally generated DC/DC voltage (to be connected to an external 10 nF capacitor).	
22	VREF	Analog output	Internally generated DC/DC reference voltage (to be connected to an external 10 nF capacitor).	
23	ROW0	Open drain output	LED matrix row driver (OUT_1, OUT_2).	
24	ROW1	Open drain output	LED matrix row driver (OUT_3, OUT_4).	
25	ROW2	Open drain output	LED matrix row driver (OUT_5, OUT_6).	
26	ROW3	Open drain output	LED matrix row driver (OUT_7, OUT_8).	
32	$\overline{PG}$	Open drain output	Connects to VREG by a pull-up resistor. The Power Good diagnostic pin is activated (forced low) when the voltage on the VCC pin goes below V_{PGH2}.	
33	$\overline{FAULT}$	Open drain output	Connects to VREG by a pull-up resistor. The Common Fault diagnostic pin is activated (forced low) when a junction overtemperature event or SPI communication fault event (parity check error or module-8 violation) occurs.	
34	$\overline{TWARN}$	Open drain output	Connects to VREG by a pull-up resistor. The Case Temperature diagnostic pin is activated (forced low) when a case overtemperature event occurs.	
36	FB	Analog input	Step-down feedback input. Connecting the FB pin to the DCVDD pin disables the DC/DC. Connect FB to VREG to make the DC/DC supply 3.3 V. An external resistor divider is required for higher output voltage.	
37	GND		Ground.	
38	PHASE	Power output	Embedded power switch source pin of the DC/DC step-down (buck) converter.	
39	BOOT	Power output	Bootstrap voltage of the DC/DC converter. It is used to provide a drive voltage, higher than the supply voltage, to power the switch of the step-down regulator.	
41	OUT8	Power output	Channel 8 power output.	
42	OUT7	Power output	Channel 7 power output.	
43	OUT6	Power output	Channel 6 power output.	
44	OUT5	Power output	Channel 5 power output.	
45	OUT4	Power output	Channel 4 power output.	
46	OUT3	Power output	Channel 3 power output.	
47	OUT2	Power output	Channel 2 power output.	
48	OUT1	Power output	Channel 1 power output.	
TAB	TAB	Power supply	Exposed tab, internally connected to V_{CC} IC supply rail.	

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3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
V_{REG}	Logic supply voltage	-0.3 to +6	V
V_{FAULT} ,V_{TWARN}, V_{PG}	Voltage range on pins $\overline{TWARN}$, $\overline{FAULT}$, and $\overline{PGOOD}$	-0.3 to +6	V
V_{PHASE}	V_{PHASE} voltage	V_{CC}	V
V_{BOOT}	Bootstrap voltage	V_{PHASE}+6	V
V_{ROW}	Voltage range on ROW pins	-0.3 to +6	V
V_{COL}	Voltage range on COL pins	-0.3 to +6	V
V_{IN}	Voltage level range on logic input pins	-0.3 to +6	V
I_{OUT}	Output current (continuous)	Internally limited (1)	A
I_R	Reverse output current (per channel)	-5	A
I_{GND}	DC ground reverse current	-250	mA
I_{REG}	V_{REG} input current	-1 to +10	mA
I_{FAULT}, I_{TWARN}, I_{PG}	Current range on pins $\overline{TWARN}$, $\overline{FAULT}$, and $\overline{PGOOD}$	-1 to +10	mA
I_{IN}	Input current range	-1 to +10	mA
I_{ROW}	Current range on ROW pins (ROW in ON-state)	+20	mA
	Current range on ROW pins (ROW in OFF-state)	-1 to +10	mA
I_{COL}	Current range on COL pins (COL in ON-state)	-10	mA
	Current range on COL pins (COL in OFF-state)	-1 to +10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	2000	V
E_{AS}	Single pulse avalanche energy per channel, all channels driven simultaneously @T_{amb} = 125 °C, I_{OUT} = 0.5 A	0.5	J
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited (1)	W
T_J	Junction operating temperature	Internally limited	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. *Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous and repetitive operation of protection functions may reduce the IC lifetime.*

Table 3. Thermal data

Symbol	Parameter		Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case (1)	Max.	1	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient (2)	Max.	25	°C/W

1. *R_{th} between the die and the bottom case surface measured by cold plate as per JESD51.*
2. *According to JESD51-7.*

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4 Electrical characteristics

4.1 Power section

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		10.5		36	V
$V_{CC\ CLAMP}$	Clamp on V_{CC}	Current 20 mA	45	50	52	V
$R_{DS(on)}$	On-state resistance	I_{OUT} = 0.5 A at T_J = 25 °C		0.11		Ω
		I_{OUT} = 0.5 A at T_J = 125 °C			0.2	
I_S	V_{CC} supply current	All channels in OFF-state, DC/DC = OFF, V_{REG}=5 V, SPI inactive (1)	0.65	1	1.1	mA
		All channels in ON-state, DC/DC = ON, V_{REG} = 5 V, SPI active (2)		5.3		mA
		All channels in ON-state, DC/DC = OFF, V_{REG} = 5 V, SPI active (3)	3.5		5.2	mA
I_{DS}	V_{REG} supply current	DC/DC = OFF, V_{REG} = 5 V, SPI inactive, WD_EN = 0		200		µA
		DC/DC = OFF, V_{REG} = 5 V, SPI active, WD_EN = V_{REG}		250		µA
I_{LGND}	Output current at GND disconnection	All pins at 0 V except V_{OUT} = 24 V			0.5	mA
$V_{OUT(OFF)}$	OFF-state output voltage	V_{IN} = 0 V, I_{OUT} = 0 A			1	V
$I_{OUT(OFF)}$	OFF-state output current	V_{IN} = V_{OUT} = 0 V	0		2	µA
f_{CP}	Charge pump frequency	Channel in ON-state (4)		1.45		MHz

1. $\overline{SS}$ *signal high, no communication.*
2. $\overline{SS}$ *signal low, communication ON.*
3. $\overline{SS}$ *signal low, communication ON.*
4. *To cover EN55022 class A and class B normative.*

4.2 SPI characteristics

10.5 V < V_{CC} < 36 V; 2.7 V < V_{REG} < 5 V; -40 <T_j <125 °C; unless otherwise specified.

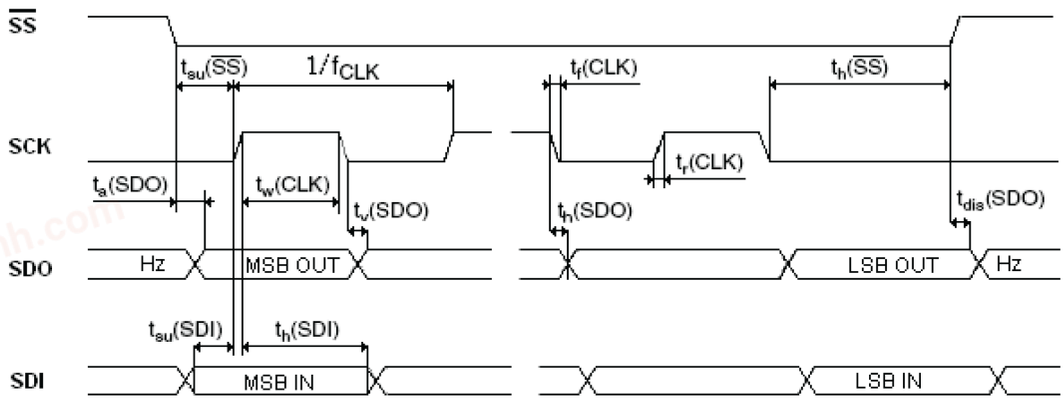
Table 5. SPI characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{CLK}	SPI clock frequency			-	5	MHz
t_r(CLK), t_f(CLK)	SPI clock rise/fall time			-	20	ns
$t_{su}(\overline{SS})$	$\overline{SS}$ setup time		120	-		ns
$t_h(\overline{SS})$	$\overline{SS}$ hold time		120	-		ns
t_w(CLK)	CLK high time		80	-		ns

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{su}(SDI)	Data input setup time		100	-		ns
t_h(SDI)	Data input hold time		100	-		ns
t_a(SDO)	Data output access time			-	100	ns
t_{dis}(SDO)	Data output disable time			-	200	ns
t_v(SDO)	Data output valid time			-	100	ns
t_h(SDO)	Data output hold time		0	-		ns
V_{SDO}	Voltage on serial data output	I_{SDO} = 15 mA	V_{REG}-0.8	-		V
		I_{SDO} = - 4 mA		-	0.8	V

Figure 3. Serial timing



GIPG030420151422LM

4.3 Switching

V_{CC} = 24 V; -40 °C < T_J < 125 °C.

Table 6. Switching

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Turn-on delay time	I_{OUT} = 0.5 A, resistive load, input rise time < 0.1 µs.	-	5	-	µs
t_r	Rise time		-	5	-	µs
$t_{d(OFF)}$	Turn-off delay time		-	10	-	µs
t_f	Fall time		-	5	-	µs
$dV/dt_{(ON)}$	Turn-on voltage slope		-	3	-	V/µs
$dV/dt_{(OFF)}$	Turn-off voltage slope		-	4	-	V/µs

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Figure 4. dV/dt(ON) and dV/dt(OFF) time diagram test conditions

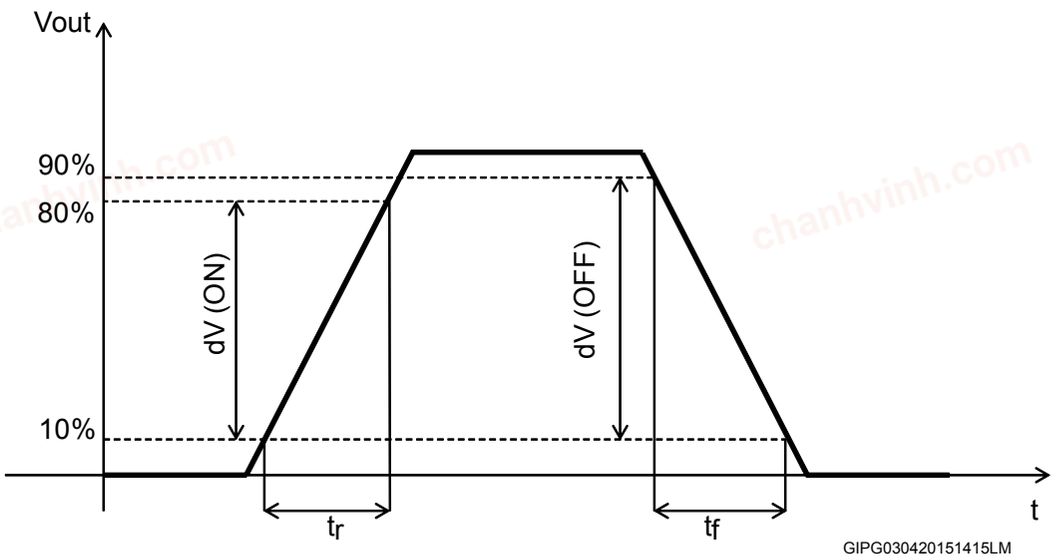
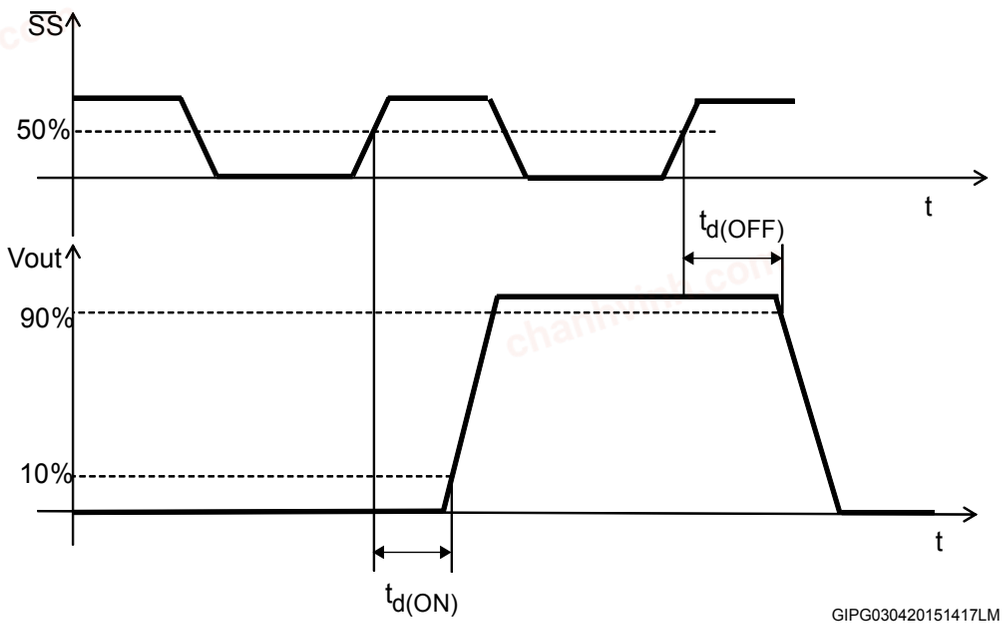


Figure 5. $t_{d(ON)}$ and $t_{d(OFF)}$ time diagram test conditions



4.4 Logic inputs

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.20			V
$V_{I(HYST)}$	Input hysteresis voltage			0.15		V
I_{IN}	Input current	V_{IN} = 5 V	8			µA

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4.5 Protection and diagnostic

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 8. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PGH1}	Power Good diagnostic ON threshold		16.5	17.5	18.4	V
V_{PGH2}	Power Good diagnostic OFF threshold		15.2	16.5	17.4	V
V_{PGHYS}	Power Good diagnostic hysteresis			1		V
V_{USD}	Undervoltage ON protection			9.5	10	V
	Undervoltage OFF protection		8.4	9		
V_{USDHYS}	Undervoltage hysteresis		0.4	0.5		V
V_{demag}	Output voltage at turn-OFF	I_{OUT} = 0.5 A; L_{LOAD} ≥ 1 mH	V_{CC}-52	V_{CC}-50	V_{CC}-45	V
V_{TWARN}	$\overline{TWARN}$ pin low-state output voltage	I_{TWARN} = 3 mA (active condition)			0.6	V
V_{FAULT}	$\overline{FAULT}$ pin low-state output voltage	I_{FAULT} = 3 mA (active condition)			0.6	V
V_{PG}	$\overline{PG}$ pin low-state output voltage	I_{PG} = 3 mA (active condition); V_{REG} = 3.3 V; V_{CC} = 0			0.7	V
I_{PEAK}	Maximum DC output current before limitation (IPS8200HQ)			1.4		A
	Maximum DC output current before limitation (IPS8200HQ-1)			2.2		
I_{LIM}	Short-circuit current limitation per channel (IPS8200HQ)	R_{LOAD} = 0; V_{CC} = 24 V; T_J = 25 °C	0.7	1.1	1.7	A
	Short-circuit current limitation per channel (IPS8200HQ-1)		1.1	1.9	2.7	
Hyst	I_{LIM} tracking limits	R_{LOAD} = 0		0.3		A
I_{LFAULT}	$\overline{FAULT}$ leakage current	$V_{open\text{-}drain\ pin}$ = 5 V			2	µA
I_{TWARN}	$\overline{TWARN}$ leakage current					
I_{PG}	$\overline{PG}$ leakage current					
T_{TSD}	Junction shutdown temperature		160	180		°C
T_R	Junction reset temperature			160		
T_{HYST}	Junction thermal hysteresis			20		
T_{CSD}	Case shutdown temperature		115	130	155	
T_{CR}	Case reset temperature			110		
T_{CHYST}	Case thermal hysteresis			20		
t_{WD}	Watchdog hold time	See Figure 12	50			ns
t_{WM}	Watchdog time	See Table 13 and Figure 12				

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{OUT_EN}	OUT_EN pin propagation delay (1)	V_{CC}= 24 V; I_{OUT}= 72 mA		10		µs
t_{RES}	OUT_EN hold time		50			ns
t_{WO}	Watchdog timeout (2)				t_{WM} + $t_{d(OFF)}$	ms

1. *Time from reset active low and power out disable.*
2. *Time from t_{WM} elapsed to power out disable.*

4.6 Step-down switching regulator

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 9. Step-down switching regulator

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DC_out}	Voltage on VREG pin supplied by the embedded DC/DC	I_{REG} from 0 to 100 mA V_{REG} 3.3 V, see Figure 16	3.1	3.3	3.5	V
		I_{REG} from 0 to 100 mA V_{REG} 5 V, see Figure 17		5		V
V_{FB}	Voltage feedback		3.1	3.3	3.5	V
$R_{DS(on)}$	MOSFET on-resistance			1.5		Ω
$I_{DC-DC(PK)}$	Inductor peak current	T_J = 25 °C	0.55		0.9	A
			0.5		0.95	A
I_{qop}	Total operating quiescent current			0.6		mA
I_{qst-by}	Total standby quiescent current	Regulator standby		15.8		µA
f_s	Switching frequency			400		kHz
D_{max}	Maximum duty cycle			80%		-
ton_{min}	Minimum on-time			150		ns
f_{sc}	Frequency in short-circuit condition			50		kHz

4.7 LED driving array

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 10. LED driving array

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{COL}	Output source voltage on COL pins	Output current 0 to 7 mA	V_{REG}-0.3	V_{REG}-0.2		V
V_{ROW}	Open drain voltage on ROW pins	Output current 0 to 15 mA		0.2	0.3	V
f_{sw}	Row refresh frequency with duty=25%			780		Hz

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5 Reverse polarity protection

Reverse polarity protection can be implemented on the board using two different solutions:

1. Placing a resistor (R_{GND}) between the IC GND pin and load GND
2. Placing a diode between the IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

$R_{GND} \geq V_{CC} / I_{GND}$

where I_{GND} is the DC reverse ground pin current and can be found in Section 3 of this datasheet.
Power dissipated by R_{GND} (when $V_{CC} < 0$: during reverse polarity situations) is:

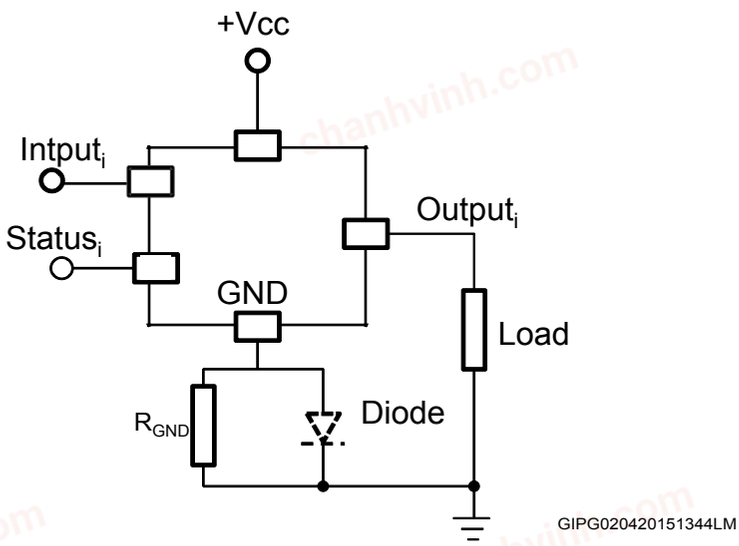
$P_D = (V_{CC})^2/R_{GND}$

If option 2 is selected, the diode has to be chosen by taking into account VRRM >$|V_{CC}|$ and its power dissipation capability:

$P_D \geq I_S*V_F$

Note: In normal conditions (no reverse polarity), due to the diode, there is a voltage drop between GND of the device and GND of the system.

Figure 6. Reverse polarity protection



This schematic can be used with any type of load.

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6 Demagnetization energy

Figure 7. Typical single pulse demagnetization: E_{OFF} vs I_{OUT} (V_{CC} = 24 V, T_{AMB} = 125 °C)

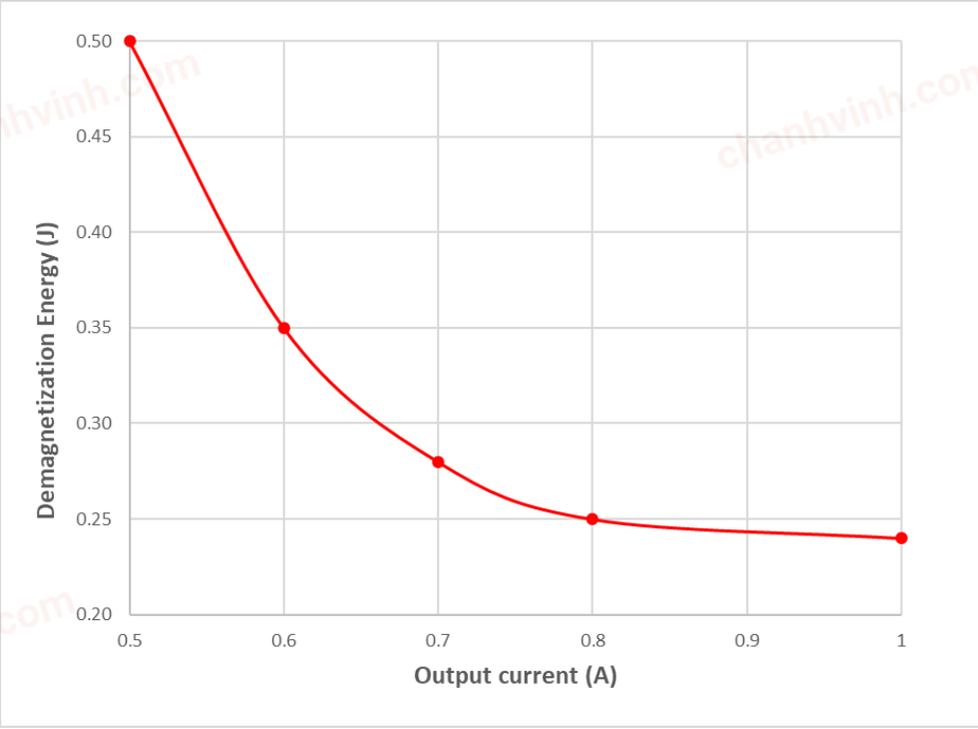
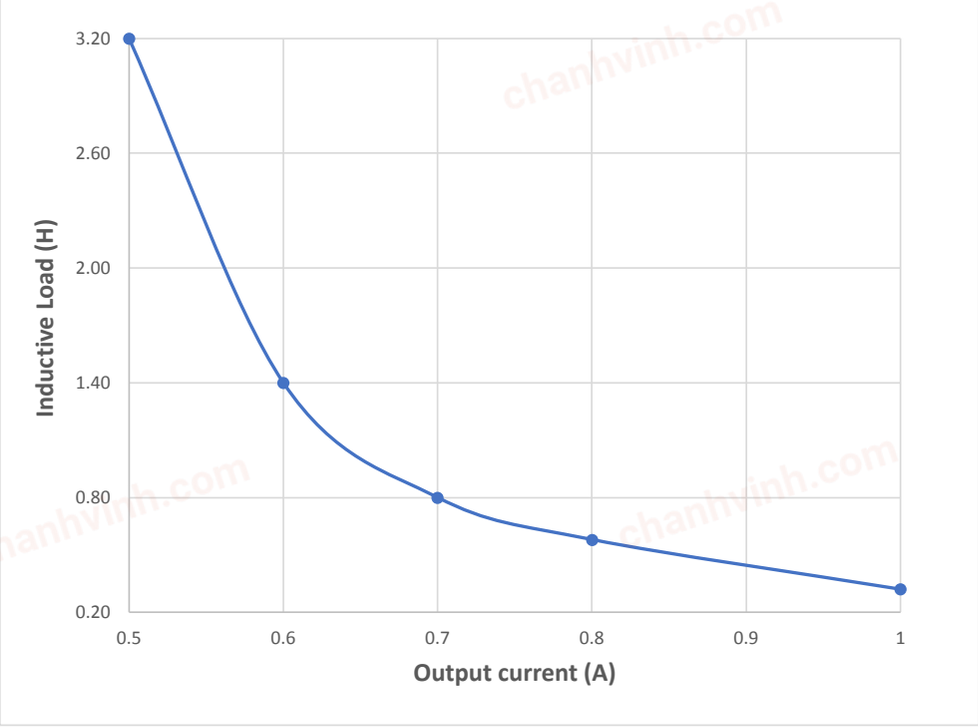


Figure 8. Typical single pulse demagnetization: L_{LOAD} vs I_{OUT} (V_{CC} = 24 V, T_{AMB} = 125 °C)



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7 Truth table

Table 11. **Truth table**

Condition	Input/ Driving bit	Output	SPI status bit	$\overline{\text{FAULT}}$	$\overline{\text{TWARN}}$	$\overline{\text{PG}}$
Normal operation	High	On	Reset	High	High	High
	Low	Off	Reset	High	High	High
Junction overtemperature	High	Off	Set	Low	X	X
	Low	Off	Set(1)	High	X	X
Case overtemperature	High	Off	Set(1)	X	Low	X
	Low	Off	Set(1)	X	Low (1)	X
Undervoltage	High	Off	Reset	X	X	X
	Low	Off	Reset	X	X	X
Power Good	High	On	Set (2)	High	High	Low
	Low	Off		High	High	Low
SPI communication fault (parity check or module-8 violation)	High	X (3)	Set	Low	High	High
	Low		Set	Low	High	High

1. *This signal becomes high after the temperature falls below the reset threshold.*
2. *If the fault expires, the reset condition occurs after SPI communication, otherwise it is set again.*
3. *When the SPI communication fails, the output is frozen at the last valid state.*

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8 Pin function description

8.1 SPI/parallel selection mode (SEL2)

This pin allows the selection of the IC interfacing mode. The SPI interface is selected if SEL2 = H, while the parallel interface is selected if SEL2 = L, according to:

Table 12. Pin function description

Pin	SEL2 = H(1) SPI operation	SEL2 = L parallel operation	-	
SDO/IN8	SDO	Serial data output	IN8	Input to channel 8
$\overline{SS}$/IN7	$\overline{SS}$	SPI Server select	IN7	Input to channel 7
CLK/IN6	CLK	Serial clock	IN6	Input to channel 6
SDI/IN5	SDI	Serial data input	IN5	Input to channel 5
WD/IN4	WD	Watchdog input	IN4	Input to channel 4
OUT_EN/IN3	OUT_EN	OUTx enable/disable	IN3	Input to channel 3
WD_EN/IN2	WD_EN	Watchdog enable/ disable and timing preset	IN2	Input to channel 2
SEL1/IN1	SEL1	8/16-bit SPI selection mode	IN1	Input to channel 1

1. *SEL2 has an internal weak pull-down.*

8.2 Serial data in (SDI)

If SEL2 = H, this pin is the input of the serial control frame. The SDI is read on CLK rising edges and, therefore, the microcontroller must change the SDI state during the CLK falling edges. After the $\overline{SS}$ falling edge, the SDI is equal to the most significant bit of the control frame (Figure 9).

8.3 Serial data out (SDO)

If SEL2 = H, this pin is the output of the serial fault frame. The SDO is updated on CLK falling edges and, therefore, the microcontroller must read the SDO state during the CLK rising edges.

The SDO pin is tri-stated when the $\overline{SS}$ signal is high and it is equal to the most significant bit of the fault frame after the $\overline{SS}$ falling edge (Figure 9).

8.4 Serial data clock (CLK)

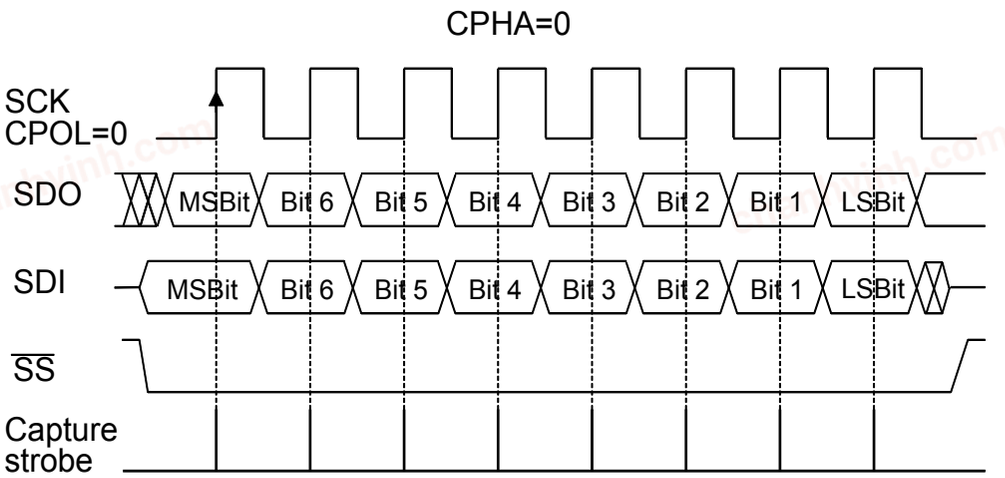
If SEL2 = H, the CLK line is the input clock for serial data sampling. On the CLK rising edge the SDI input is sampled by the IC, and the SDO output is sampled by the host microcontroller. On the CLK falling edge, both the SDI and SDO lines are updated to the next bit of the frame, from the most to the least significant one (Figure 9). When the $\overline{SS}$ signal is high, by means the SPI of the IC is not active, the microcontroller should drive the CLK low (the settings for the MCU SPI port are CPHA = 0 and CPOL = 0).

8.5 SPI server select (SS)

If SEL2 = H, the ($\overline{SS}$) signal is used to enable the IC serial communication shift register; data is flushed-in through the SDI pin and flushed-out from the SDO pin only when the $\overline{SS}$ pin is low. On the $\overline{SS}$ pin falling edge the shift register (containing the fault conditions) is frozen, so any change on the power switch status is latched until the next $\overline{SS}$ falling edge event and the SDO output is enabled. On the $\overline{SS}$ pin rising edge event the 8/16-bits present on the SPI shift register are evaluated and the outputs are driven according to this frame. If more than 8/16-bits (depending on the SPI settings) are flushed inside only the last 8/16 are evaluated; the others are flushed out from the SDO pin after fault condition bits. In this way, proper communication is also possible in a daisy chain configuration.

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Figure 9. **SPI mode diagram**



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8.6 8/16-bit selection (SEL1)

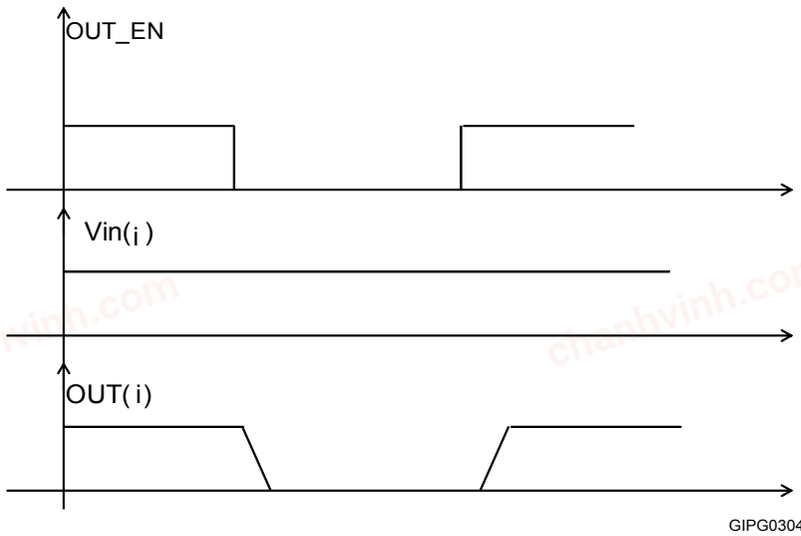
If SEL2 = H, SEL1 is used to select between two possible SPI configurations: the 8-bit SPI mode (SEL1 = L) and the 16-bit SPI mode (SEL1 = H). The 8/16-bit SPI operation is described below.

8.7 Output enable (OUT_EN)

If SEL2 = H, the OUT_EN pin provides a fast way to disable all the outputs simultaneously. When the OUT_EN pin is driven low for at least T_{RES}, the outputs are disabled while fault conditions in the SPI register are latched. To enable the outputs, the OUT_EN pin should be raised and the IC should be reprogrammed through the SPI interface. As fault conditions are latched inside the IC, the SPI interface also works while the OUT_EN pin is driven low. The SPI can be used to detect if a fault condition occurred before the reset event.

The device is ready to operate normally after a T_{SU} period. The OUT_EN pin is the fastest way to disable all outputs when a fault occurs.

Figure 10. **Output channel enable/disable behavior**



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8.8 IC warning case temperature detection ($\overline{\text{TWARN}}$)

The $\overline{\text{TWARN}}$ pin is an active low open drain output. This pin is active if the IC case temperature exceeds T_{CSD}. According to the PCB thermal design and R_{thJC} value, this function warns about a PCB overheating condition.

The $\overline{\text{TWARN}}$ bit is also available through SPI. This bit is not latched: the $\overline{\text{TWARN}}$ pin is low only while the case overtemperature condition is active ($T_C > T_{CSD}$) and is released when this condition is removed ($T_C < T_{CR}$).

8.9 Fault indication ($\overline{\text{FAULT}}$)

The $\overline{\text{FAULT}}$ pin is an open drain active low fault indication pin. One or more of the following conditions activates this pin:

- Channel overtemperature (OVT)

This pin is activated when at least one of the channels is in junction overtemperature.

Unlike the SPI fault detection bits, this signal is not latched: the $\overline{\text{FAULT}}$ pin is low only when the fault condition is active and is released if the input driving signal is OFF or after the OVT protection condition has been removed. This last event occurs if the channel temperature decreases below the threshold level and the case temperature has not exceeded T_{CSD} or is below T_{CR}. This means that the $\overline{\text{FAULT}}$ pin is low only while the junction overtemperature is active ($T_J > T_{TSD}$) and is released after this condition has been removed ($T_J < T_R$ and $T_C < T_{CR}$).

- Parity check fail

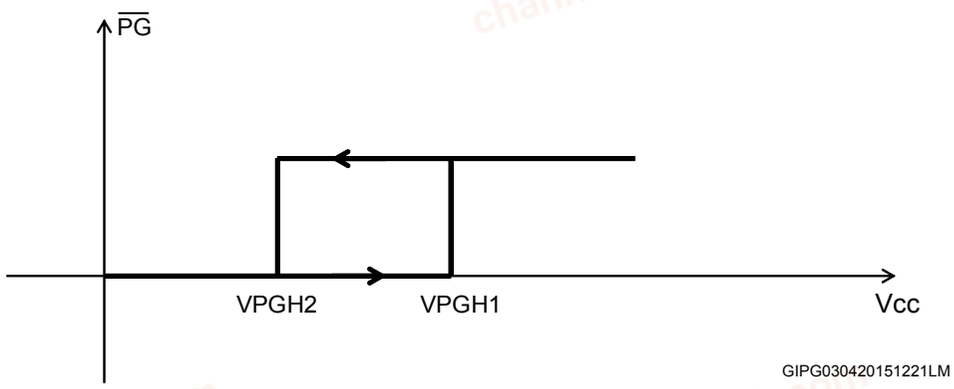
When SPI mode is used (SEL2 = H), if a parity check fault of the incoming SPI frame is detected or counted, CLK rising edges are different by a multiple of 8, the $\overline{\text{FAULT}}$ pin is kept low. When counted CLK rising edges are a multiple of 8 and the parity check is valid, the $\overline{\text{FAULT}}$ pin is kept high.

8.10 Power Good ($\overline{\text{PG}}$)

The $\overline{\text{PG}}$ terminal is an open drain, which indicates the status of the supply voltage. When the V_{CC} supply voltage reaches the V_{sth1} threshold, $\overline{\text{PG}}$ goes into a high impedance state. It goes into a low impedance state when the V_{CC} falls below the V_{sth2} threshold.

In 16-bit SPI mode, a $\overline{\text{PG}}$ bit is also available. This bit is set high when the Power Good diagnostic is active; otherwise, it is cleared.

Figure 11. Power Good diagnostic



8.11 Programmable watchdog counter reset (WD)

If SEL2 = H, and the WD_EN = H, then the embedded watchdog counter is enabled. An H-L transition on the WD pin resets the watchdog counter.

If the counter elapses before the H-L transition on the WD pin, then the IC enters into an internal reset state where all the outputs are disabled. To restart normal operation a negative pulse must be applied to the WD pin.

The WD_EN pin should be connected through an external divider to V_{REG}.

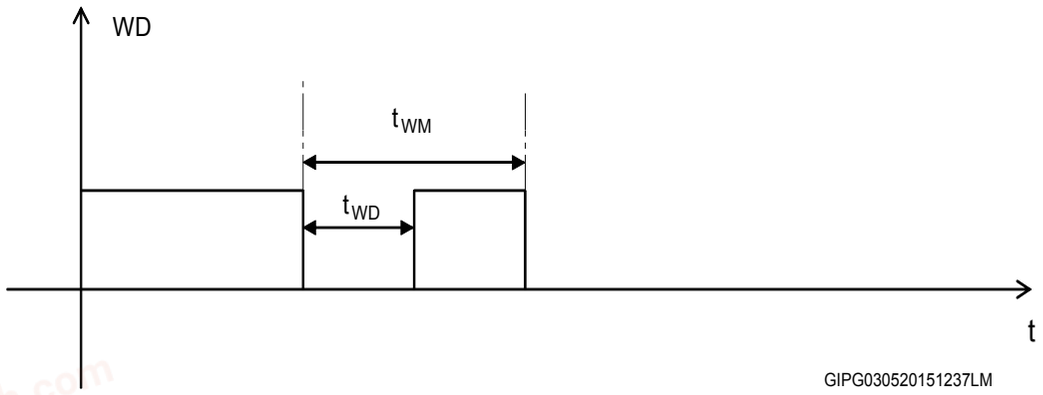
The watchdog time is fixed in the following table:

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Table 13. Programmable watchdog time

V_{WD_EN}	t_{WM}
0.25 V_{REG} > V_{WD_EN}	Disable
0.25 V_{REG} ≤ V_{WD_EN} < 0.5 V_{REG}	40 ± 25% ms
0.25 V_{REG} ≤ V_{WD_EN} < 0.75 V_{REG}	80 ± 25% ms
0.75 V_{REG} ≤ V_{WD_EN} = V_{REG}	160 ± 25% ms

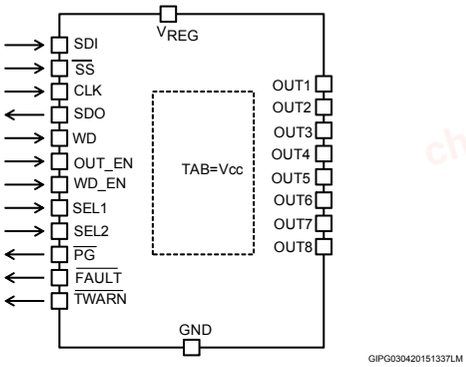
Figure 12. Watchdog reset



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9 SPI operation (SEL2 = H)

Figure 13. **SPI directional logic convention**



9.1 8-bit SPI mode (SEL1 = L)

If SEL2 = H, the 8-bit SPI mode is based on an 8-bit command frame sent from the microcontroller to the IC. Each bit directly drives the corresponding output where LSB drives output 0 and MSB drives output 7. Each bit, set to '1', activates (closes) the corresponding output.

At the same time, the IC transfers the channel fault conditions (OVT) to the microcontroller. These fault conditions are latched at the occurrence and cleared after each communication (each time the $\overline{SS}$ signal has a positive transition). Each bit, set to '1', indicates an OVT condition for the corresponding channel.

Table 14. **Command 8-bit frame (from MCU to IC)**

MSB							LSB
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Table 15. **Fault 8-bit frame (from IC to MCU)**

MSB							LSB
F7	F6	F5	F4	F3	F2	F1	F0

9.2 16-bit SPI mode (SEL1 = H)

The 16-bit SPI mode is based on a 16-bit command frame sent from the microcontroller to the IC. The first 8 bits directly drive the output channels (each bit, set to '1', activates the corresponding output), the other 8 bits contain a 4-bit parity check code where the last bit (the inversion of the previous one) is used to detect a communication error condition (providing at least a transition in each frame):

$P0 = IN0 \oplus IN1 \oplus IN2 \oplus IN3 \oplus IN4 \oplus IN5 \oplus IN6 \oplus IN7$

$P1 = IN1 \oplus IN3 \oplus IN5 \oplus IN7$

$P2 = IN0 \oplus IN2 \oplus IN4 \oplus IN6$

$nP0 = not\ P0$

where $\oplus$ is the XOR operator symbol.

Table 16. **Command 16-bit frame (from MCU to IC)**

MSB															LSB
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0					P2	P1	P0	nP0

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At the same time, the IC transfers to the microcontroller a 16-bit fault frame where the first 8 bits indicate a channel fault (OVT) condition (each bit, set to '1', indicates an OVT event), the following 4 bits provide general fault condition information. FB_OK: this bit is related to the DC/DC regulation: at the DC/DC turn-on, this bit is low and becomes high after FB rises above 90% of the nominal V_{FB} voltage and a correct SPI communication occurrs. If the FB voltage falls below 80% of the nominal V_{FB} voltage, this bit is zero; $\overline{\text{TWARN}}$ (IC warning case temperature), PC (parity check fail, the bit, set to '1', indicates a PC fail or the length is not a multiple of 8), and $\overline{\text{PG}}$ (Power Good, see Section 8.10). The last 4 bits are used as parity check bits and communication error conditions (see command 16-bit frame):

$P0 = F0 \oplus F1 \oplus F2 \oplus F3 \oplus F4 \oplus F5 \oplus F6 \oplus F7$

$P1 = PC \oplus FB_OK \oplus F1 \oplus F3 \oplus F5 \oplus F7$

$P2 = \overline{PG} \oplus \overline{TWARN} \oplus F0 \oplus F2 \oplus F4 \oplus F6$

$nP0 = \text{not } P0$

where $\oplus$ is the XOR operator symbol.

Table 17. Fault 16-bit frame (from IC to MCU)

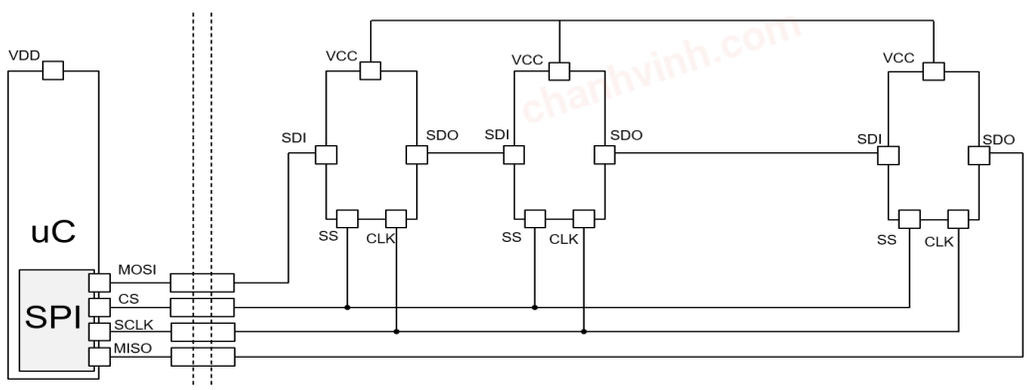
MSB															LSB
F7	F6	F5	F4	F3	F2	F1	F0	FB_OK	$\overline{\text{TWARN}}$	PC	$\overline{\text{PG}}$	P2	P1	P0	nP0

Channel indications are latched and cleared only after a communication.

9.3 Daisy chaining

The IPS8200HQ/HQ-1 can be daisy chained by connecting the MOSI port of the micro-controller to the SDI pin of the first IC of the chain; the SDO pin of the first IC of the chain to the SDI pin of the second (and similarly for the next ICs of the chain); and the SDO pin of the last IC of the chain to the MISO port of the micro-controller. See an example in Figure 14

Figure 14. Example of daisy chaining connection

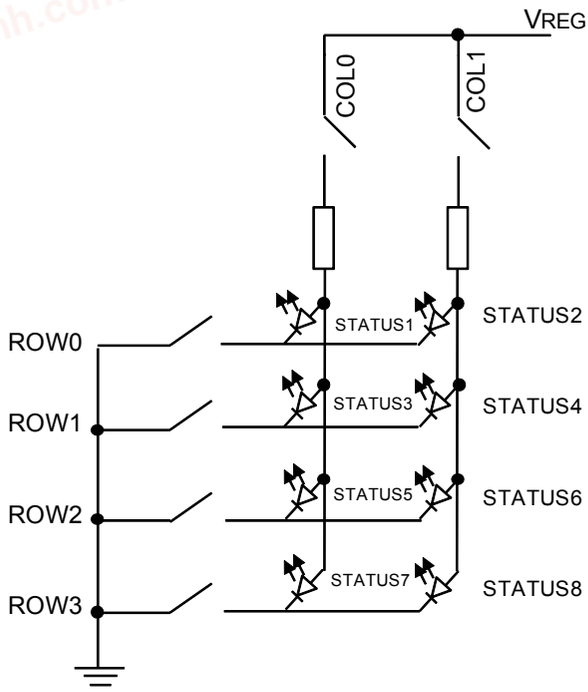


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10 LED driving array

The LED driving array carries out the status of the output channels (ON or OFF).

Figure 15. LED driving array



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The following equation is an indication of how to choose the R_{ext} resistor value:

$R_{ext}= (V_{COLmin}) - (V_{ROWmax}) - V_{F(LED)} / I_{F(LED)}$

where $I_{F(LED)} \leq 7$ mA and (V_{COLmin}) and (V_{ROWmax}) can be found in Table 10; $V_{F(LED)}$ and $I_{F(LED)}$ depend on the electrical characteristics of the LEDs.

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11 Step-down switching regulator

The IC embeds a high efficiency 100 mA micropower step-down switching regulator. The regulator is protected against short-circuits or overload conditions. Pulse-by-pulse current limit regulation is obtained in normal operation through a current loop control.

A low ESR output capacitor connected to the V_{REG} pin helps to limit the regulated voltage ripple; a low ESR (less than 10 mΩ) capacitor is preferable. The control loop pin FB allows 3.3 V to be regulated, connecting it directly to V_{REG}, or 5 V connecting it through a voltage divider. The DC/DC converter can be turned off by connecting the feedback pin to the DCVDD pin.

In some applications it is possible to switch off the embedded DC/DC and supply the V_{REG} by 5 V or 3.3 V externally. Also, in the case of two or more ICs inside the same board, the user can activate the DC/DC converter on only one IC, and also supply the V_{REG} pins of the other ICs.

If the DC/DC converter is adjusted to provide 3.3 V regulation and the V_{DC_out} is used to power an external load and not the device, a 33 kΩ resistor has to be connected on the V_{REG} pin.

Figure 16. Typical circuit for switching regulation $V_{DC\text{-}out}$ = 3.3 V

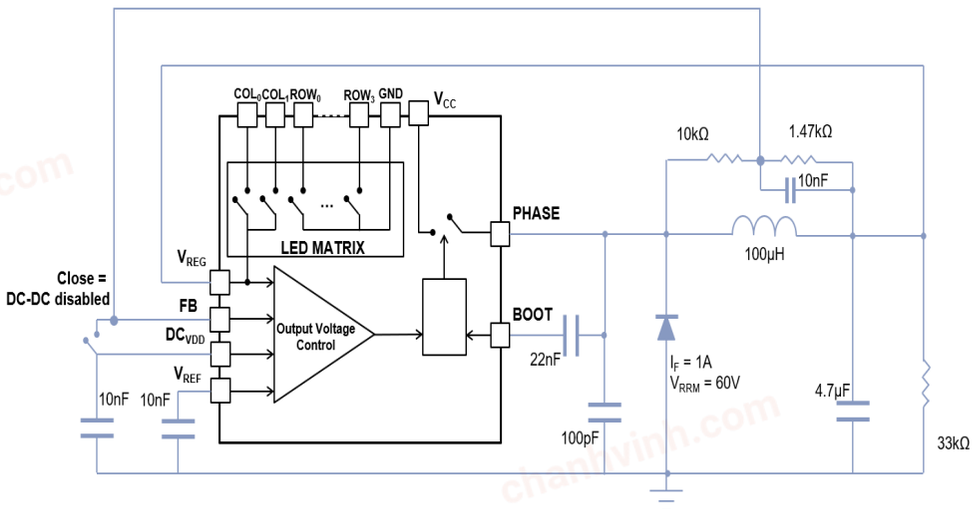
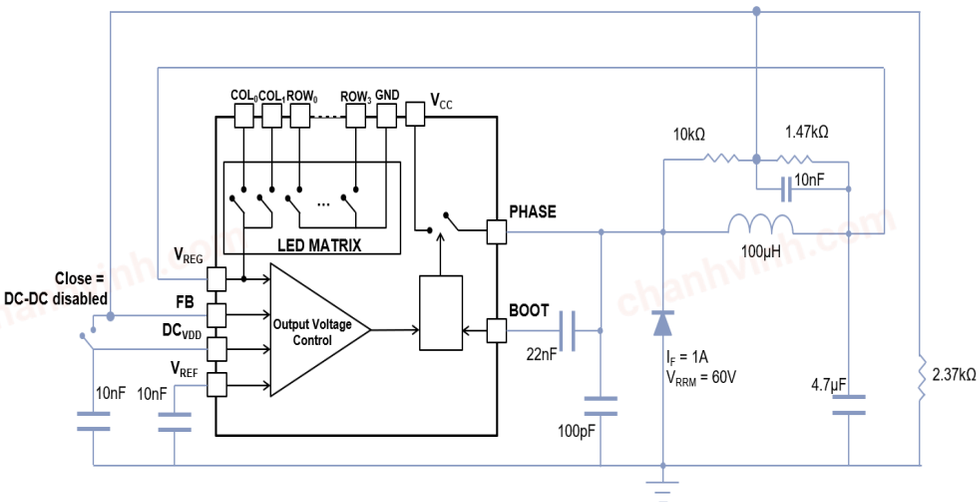


Figure 17. Typical circuit for switching regulation $V_{DC\text{-}out}$ = 5 V

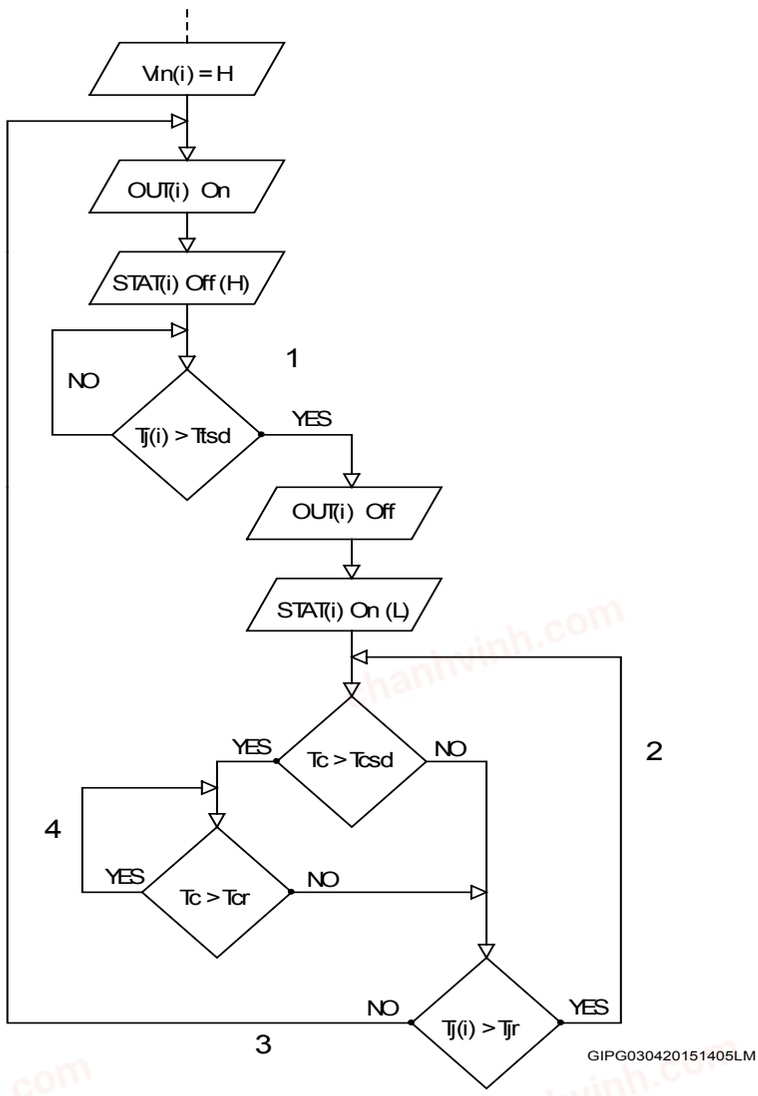


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12 Thermal management

The power dissipation in the IC is the main factor that sets the safe operating condition of the device in the application. Therefore, it must be very carefully considered. Furthermore, the available space on the PCB should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. Two different protections have been implemented to guarantee the safety of the device if it overheats due to an overloaded condition or high ambient temperature. The following flowchart explains the functionality of these protections in detail.

Figure 18. Thermal behavior



Note: *1 Thermal shutdown*
2 Junction hysteresis
3 Restore to idle condition
4 Case hysteresis

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13 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at www.st.com. ECOPACK is an STMicroelectronics trademark.

13.1 VFQFPN-48L 8x6 mm, package information

Figure 19. **VFQFPN-48L 8x6 mm, mechanical drawings**

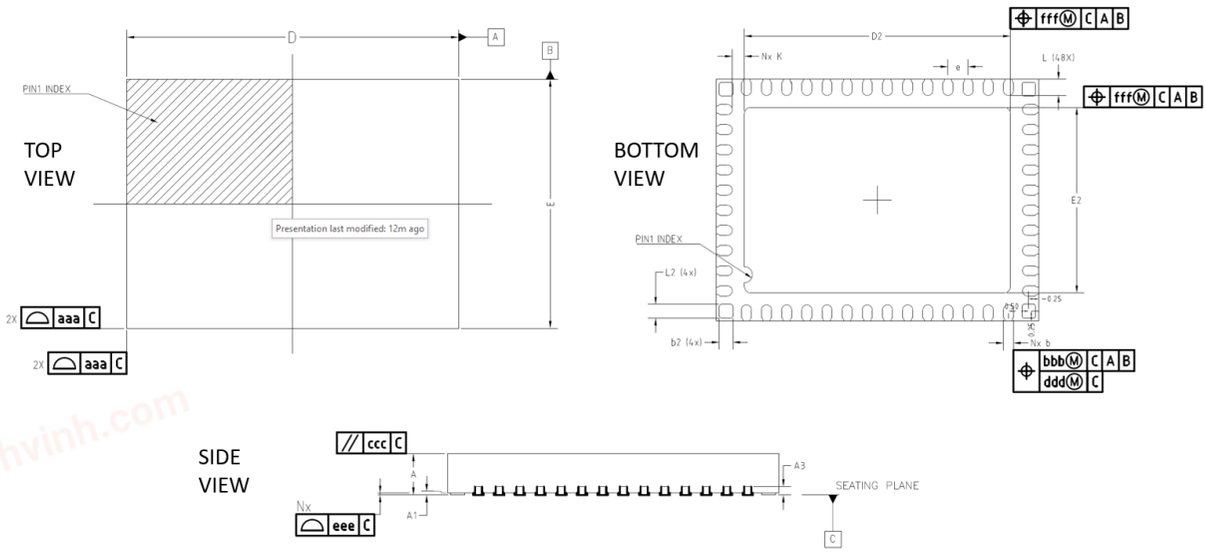


Table 18. **VFQFPN-48L 8x6 mm, mechanical data**

Symbol	Value [mm]			Note
	Min.	Nom.	Max.	
A	0.80	0.90	1.00	12
A1	0.00	-	0.05	9, 12
A3		0.20 REF		
b	0.15	0.25	0.35	5, 6, 7, 12, 13
b2	0.24	0.34	0.44	
D		8.00 BSC		4, 12
e		0.50 BSC		
E		6.00 BSC		4, 12
D2	6.5	6.60	6.70	
E2	4.50	4.60	4.70	
L	0.30	0.40	0.50	12, 13
L2	0.24	0.34	0.44	
k	0.20			12, 13
N		48		8

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Table 19. **TOLERANCE OF FORM AND POSITION (see notes 1, 12)**

Symbol	Definition	Tolerance [mm]	Notes
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	0.10	
bbb	The tolerance that controls the position of the entire terminal pattern with respect to Datum's A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to Datum's A and B.	0.10	
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	0.10	
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by the basic dimension "e."	0.05	This tolerance is normally compounded with a tolerance zone defined by bbb.
eee	The unilateral tolerance located above the seating plane where the bottom surface of all terminals must be located.	0.08	This tolerance is commonly known as the "co-planarity" of the package terminals.
fff	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone is defined by the Datum's center lines of the package body.	0.10	

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Notes:
1. Dimensioning and tolerance schemes conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters.
3. Terminal A1 identifier and terminal numbering conventions shall conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. The top side terminal A1 indicator may be a molded or metallic feature. Optional indicators on the bottom surface may be molded, marked, or metallic features.
4. Outlines with “D” and “E” in increments of less than 0.5 mm should be registered as “standalone” outlines. These outlines should use as many of the algorithms and dimensions stated in the design standard as possible to ensure predictability in manufacturing.
5. Dimension ‘b’ applies to the metallic terminal and measures between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension ‘b’ should not be measured in that radius area.
6. The inner edge of corner terminals may be chamfered or rounded in order to achieve a minimum gap “k.” This feature should not affect the terminal width “b,” which is measured L/2 from the edge of the package body.
7. The exact shape of the leads at the edge of the package is optional.
8. “N” is the maximum number of terminal positions for the specified body size. Depopulation is allowed, but only under the following conditions:

- The depopulation scheme must be consistent in each quadrant of the package.
- Non-symmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics.

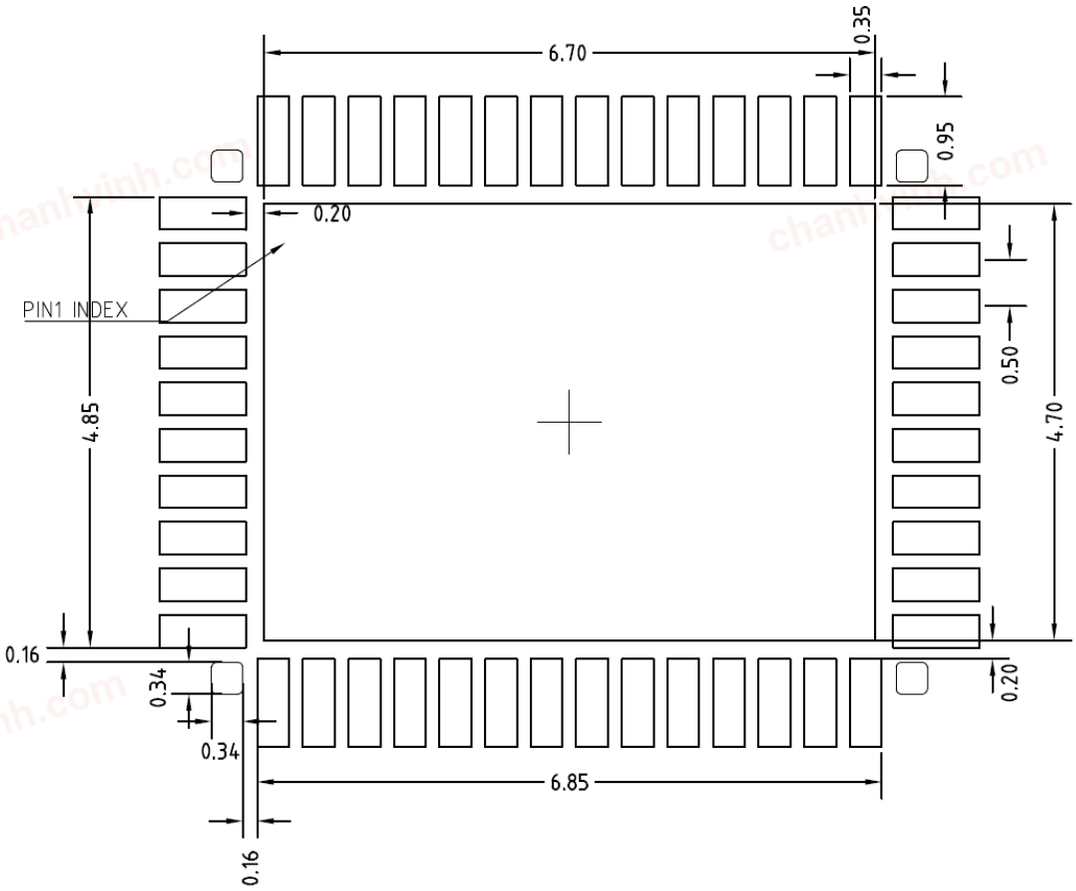
9. A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).
10. Dimensions D2 and E2 refer to the exposed pad. For the exposed pad dimensions see the Variations Table.
11. For Tolerance of Form and Position see related table.
12. Critical dimensions:

- 12.1 A
- 12.2 A1
- 12.3 D & E
- 12.4 b & L
- 12.5 e
- 12.6 D2 & E2

13. Dimensions “b” and “L” are measured on the terminal plating surface.
14. Depending on the method of lead termination at the edge of the package, pull back (L1) may be present. L minus L1 should be equal to or greater than 0.3 mm.
15. For Symbols, Recommended Values and Tolerances see the Table below: (ACCORDING TO PACKAGE OR JEDEC SPEC IF REGISTERED)

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Figure 20. **VFQFPN-48L 8x6 mm, suggested footprint**



STMicroelectronics is not responsible for PCB-related issues. The footprint shown in the above figure is a suggestion which may differ from the customer PCB supplier design rules.

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13.2 Packing information

Figure 21. **VFQFPN-48L 8x6 mm reel shipment reference**

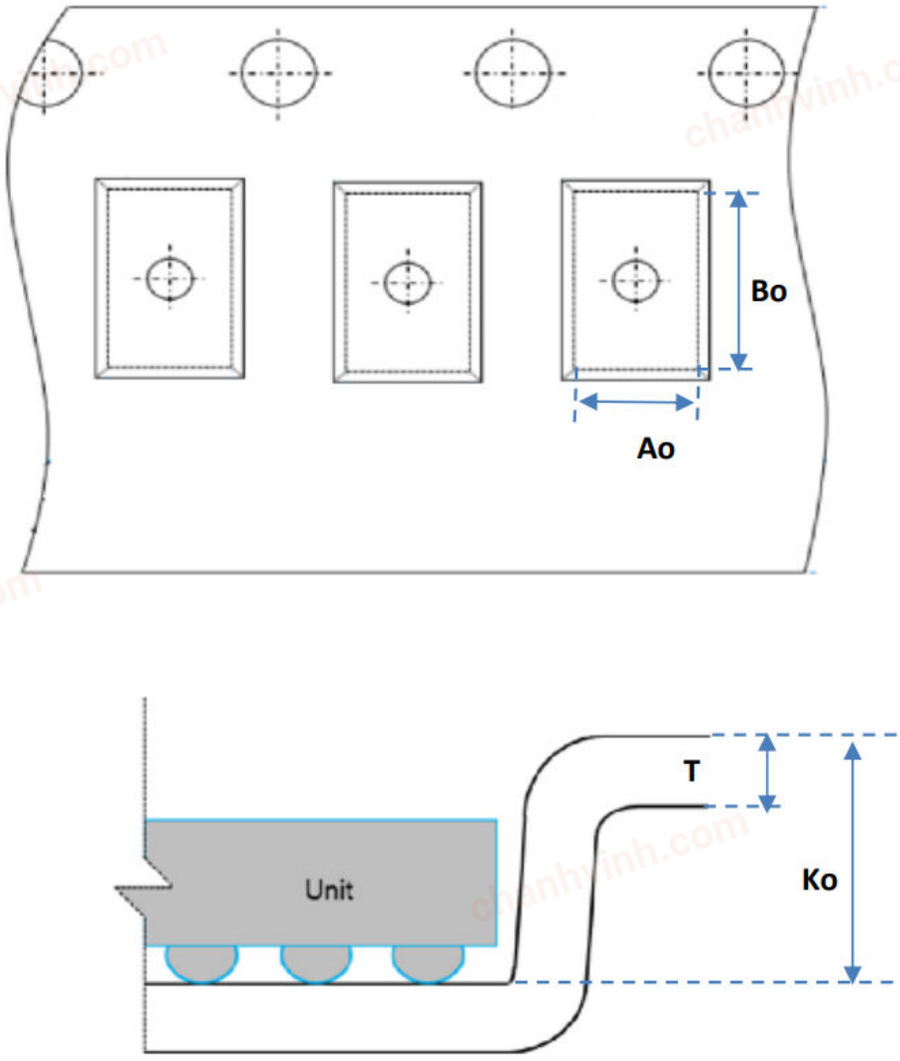
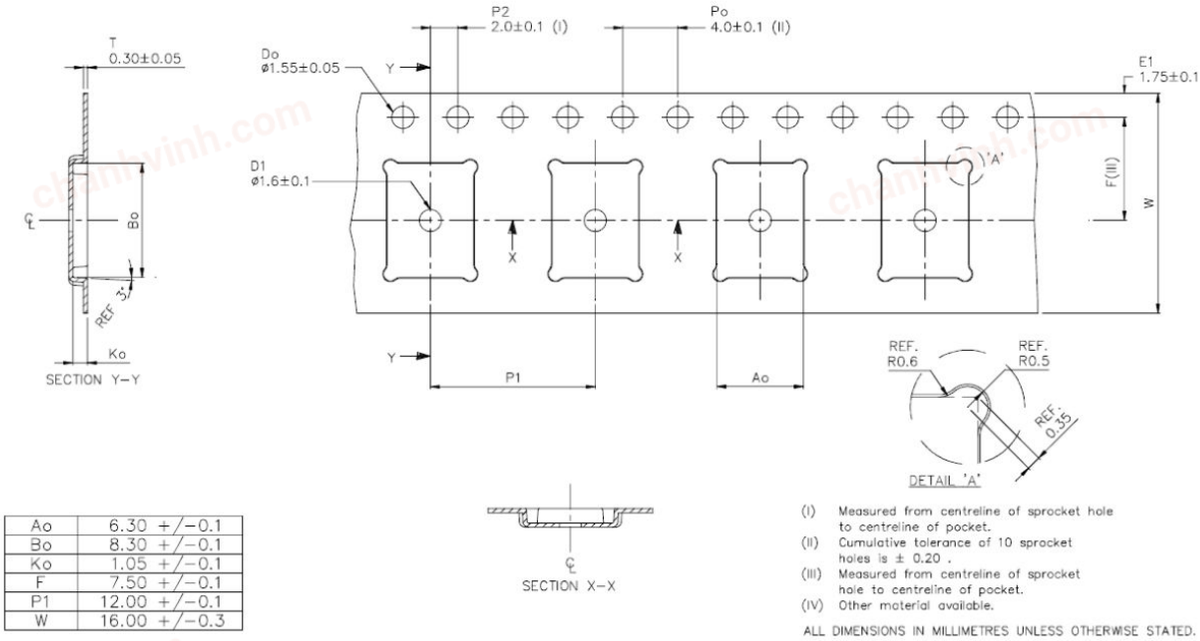


Table 20. **Standard SPC parameters**

Item	Description
Ao	Pocket Length
Bo	Pocket Width
Ko	Pocket Depth
T	Tape Thickness

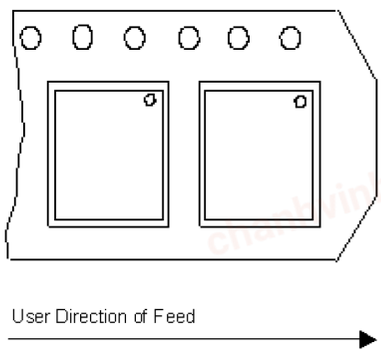
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Figure 22. **VFQFPN-48L 8x6 mm tape dimensions**



Ao	6.30 +/−0.1
Bo	8.30 +/−0.1
Ko	1.05 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

Figure 23. **VFQFPN-48L 8x6 mm tape, Pin 1 indication**



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14 Ordering information

Table 21. **Ordering information**

Part number	Package	Packaging
IPS8200HQ	VFQFPN-48L 8x6 mm	Tape and reel
IPS8200HQ-1		

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Revision history

Table 22. **Document revision history**

Date	Version	Changes
02-Oct-2023	1	Initial release.
12-Feb-2024	2	Changed XOR operator symbol in Section 9.2; some minor changes.

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Contents

1 **Block diagram** 3
2 **Pin connection** 4
3 **Maximum ratings** 6
4 **Electrical characteristics** 7
4.1 Power section 7
4.2 SPI characteristics 7
4.3 Switching 8
4.4 Logic inputs 9
4.5 Protection and diagnostic 10
4.6 Step-down switching regulator 11
4.7 LED driving array 11
5 **Reverse polarity protection** 12
6 **Demagnetization energy** 13
7 **Truth table** 14
8 **Pin function description** 15
8.1 SPI/parallel selection mode (SEL2) 15
8.2 Serial data in (SDI) 15
8.3 Serial data out (SDO) 15
8.4 Serial data clock (CLK) 15
8.5 SPI server select (SS) 15
8.6 8/16-bit selection (SEL1) 16
8.7 Output enable (OUT_EN) 16
8.8 IC warning case temperature detection ($\overline{\text{TWARN}}$) 17
8.9 Fault indication ($\overline{\text{FAULT}}$) 17
8.10 Power Good ($\overline{\text{PG}}$) 17
8.11 Programmable watchdog counter reset (WD) 17
9 **SPI operation (SEL2 = H)** 19
9.1 8-bit SPI mode (SEL1 = L) 19
9.2 16-bit SPI mode (SEL1 = H) 19
9.3 Daisy chaining 20
10 **LED driving array** 21
11 **Step-down switching regulator** 22
12 **Thermal management** 23

chanhvinh.com

13 Package information 24
13.1 VFQFPN-48L 8x6 mm, package information 24
13.2 Packing information 28
14 Ordering information 30
Revision history 31
List of tables 34
List of figures 35

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List of tables

Table 1. Pin description . . . 4
Table 2. Absolute maximum ratings . . . 6
Table 3. Thermal data . . . 6
Table 4. Power section . . . 7
Table 5. SPI characteristics . . . 7
Table 6. Switching . . . 8
Table 7. Logic inputs . . . 9
Table 8. Protection and diagnostic . . . 10
Table 9. Step-down switching regulator . . . 11
Table 10. LED driving array . . . 11
Table 11. Truth table . . . 14
Table 12. Pin function description . . . 15
Table 13. Programmable watchdog time . . . 18
Table 14. Command 8-bit frame (from MCU to IC) . . . 19
Table 15. Fault 8-bit frame (from IC to MCU) . . . 19
Table 16. Command 16-bit frame (from MCU to IC) . . . 19
Table 17. Fault 16-bit frame (from IC to MCU) . . . 20
Table 18. VFQFPN-48L 8x6 mm, mechanical data . . . 24
Table 19. TOLERANCE OF FORM AND POSITION (see notes 1, 12) . . . 25
Table 20. Standard SPC parameters . . . 28
Table 21. Ordering information . . . 30
Table 22. Document revision history . . . 31

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List of figures

Figure 1. Block diagram . . . 3
Figure 2. Pin connection (top through view) . . . 4
Figure 3. Serial timing . . . 8
Figure 4. dV/dt(ON) and dV/dt(OFF) time diagram test conditions . . . 9
Figure 5. $t_{d(ON)}$ and $t_{d(OFF)}$ time diagram test conditions . . . 9
Figure 6. Reverse polarity protection . . . 12
Figure 7. Typical single pulse demagnetization: E_{OFF} vs I_{OUT} (V_{CC} = 24 V, T_{AMB} = 125 °C) . . . 13
Figure 8. Typical single pulse demagnetization: L_{LOAD} vs I_{OUT} (V_{CC} = 24 V, T_{AMB} = 125 °C) . . . 13
Figure 9. SPI mode diagram . . . 16
Figure 10. Output channel enable/disable behavior . . . 16
Figure 11. Power Good diagnostic . . . 17
Figure 12. Watchdog reset . . . 18
Figure 13. SPI directional logic convention . . . 19
Figure 14. Example of daisy chaining connection . . . 20
Figure 15. LED driving array . . . 21
Figure 16. Typical circuit for switching regulation $V_{DC\text{-}out}$ = 3.3 V . . . 22
Figure 17. Typical circuit for switching regulation $V_{DC\text{-}out}$ = 5 V . . . 22
Figure 18. Thermal behavior . . . 23
Figure 19. VFQFPN-48L 8x6 mm, mechanical drawings . . . 24
Figure 20. VFQFPN-48L 8x6 mm, suggested footprint . . . 27
Figure 21. VFQFPN-48L 8x6 mm reel shipment reference . . . 28
Figure 22. VFQFPN-48L 8x6 mm tape dimensions . . . 29
Figure 23. VFQFPN-48L 8x6 mm tape, Pin 1 indication . . . 29

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