chanhvinh.com

IPS1025H, IPS1025H-32

High efficiency, high-side switch with extended diagnostics and smart driving for capacitive loads



Features

- 8 V to 60 V operating supply voltage range
- Smart driving of capacitive load
- Under-voltage lock-out
- V_{CC} over-voltage protection
- Fast demagnetization of inductive loads
- Output overload and over-temperature protections
- Case over-temperature protection
- Overload event diagnostic pin
- Over-temperature event diagnostic pin
- Ground disconnection protection
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- Package PowerSSO-24

Applications

- Programmable logic control
- Vending machines
- Industrial PC peripheral input/output
- Numerical control machines
- General high-side switch applications

Product status link

IPS1025H

IPS1025H-32

Product label

SUSTAINABLE TECHNOLOGY

Description

The IPS1025H and IPS1025H-32 are single high-side switch ICs able to drive capacitive, resistive or inductive loads with one side connected to ground.

The very low R_{DS-ON} (≤ 25 mΩ up to T_J = 125 °C) makes the IC suitable for the applications with up to 2.4 A/ 5.6 A steady state operating current.

The output channel is protected against junction over-temperature events by a junction temperature sensor, and a further temperature sensor is included to monitor case temperature, so the overheated output channel can only be turned back ON when the case temperature returns below the reset temperature.

The embedded overload protection circuit monitors the output current and, on triggering of the activation threshold (I_{PK}), starts modulating the impedance of the output switch to limit the output current to I_{LIM}, for both IC and load protection.

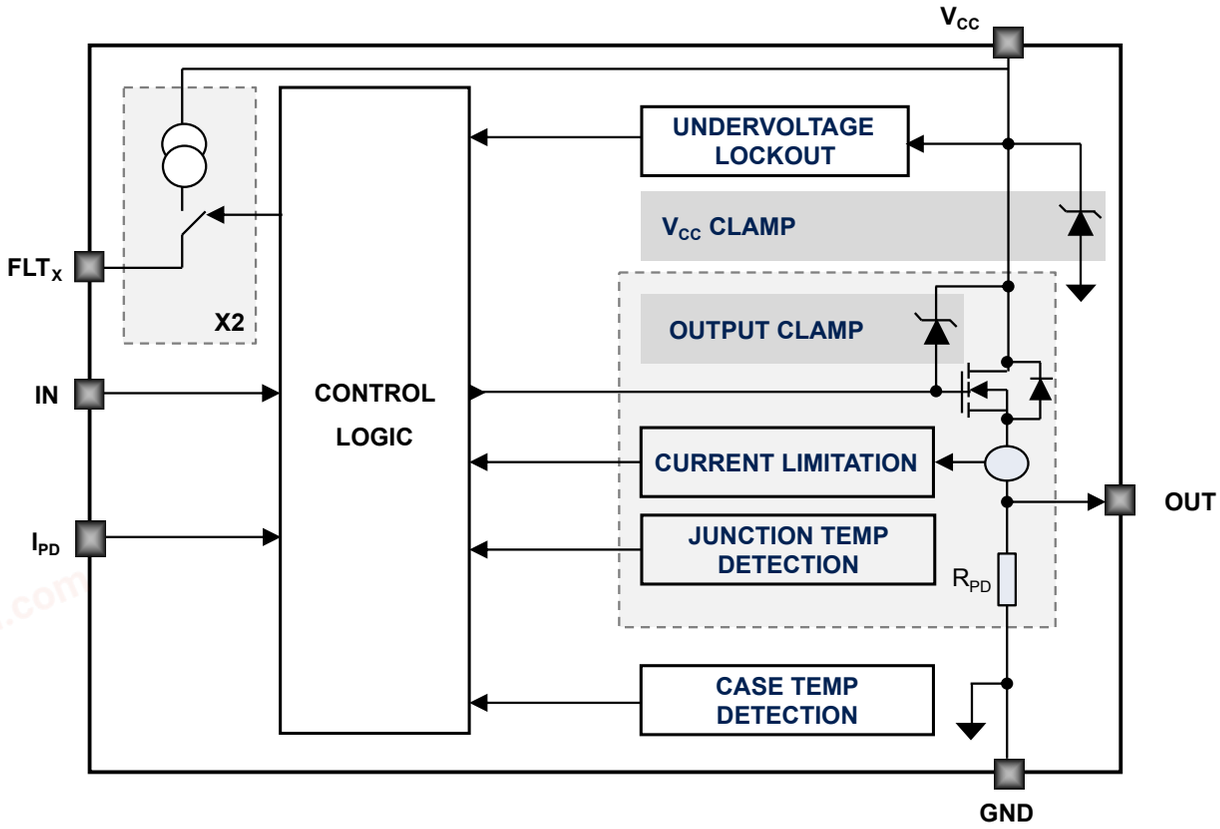
The IC offers two different sets of activation threshold and limitation levels (I_{PKH}, I_{LIMH} and I_{PKL}, I_{LIML}) for smart driving of capacitive loads (such as bulb lamps) and loads with initial peak current requirements.

The IC diagnostics is based on FLT_1 and FLT_2 pins (both current source); activated by respective overload or overtemperature events on the output channel.

chanhvinh.com

1 Block diagram

Figure 1. IPS1025H, IPS1025H-32 block diagram



chanhvinh.com

2 Pin connection

Figure 2. **Pin connections (top through view)**

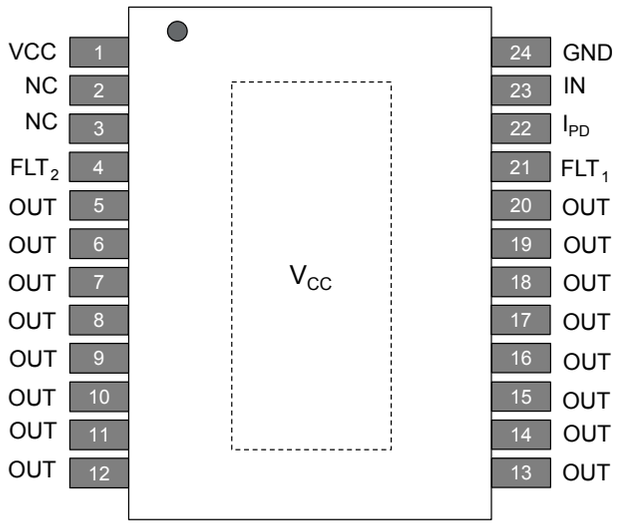


Table 1. **Pin descriptions**

Pin no.	Pin name	Type
1, exposed pad	VCC	Supply voltage
2,3	N.C.	Not connected
4	FLT2	Overload event diagnostic pin
5 to 20	OUT	Power stage output channel
21	FLT1	Over-temperature event diagnostic pin
22	IPD	Initial current duration / level selector. Connect to GND by a capacitor to set duration of I_{PKH} (see Section 7.3 and Table 9). Connect to IN pin by a 220 kΩ resistor to disable initial I_{PKH} threshold (the over-current limit is only I_{PKL}). Connect to GND by a 10 kΩ resistor to disable I_{PKL} (the over-current threshold is only I_{PKH}). *Note: Leaving I_{PD} floating is equivalent to a 1 µs duration for I_{PKH}.*
23	IN	Input
24	GND	Device ground

chanhvinh.com

3 Absolute maximum ratings

Absolute maximum ratings are the values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to 65	V
I_{CC}	Maximum DC reverse current (from GND to V_{CC})	-250	mA
I_{OUT}	Output stage current	Internally limited	A
$-I_{OUT}$	Reverse current (from OUT to V_{CC})	5	A
V_{IN}	IN pin voltage	-0.3 to V_{CC}	V
I_{IN}	IN pin current	-10/+10	mA
V_{PD}	I_{PD} pin voltage	-0.3 to 5.5	V
I_{PD}	I_{PD} pin current	-1/+10	mA
V_{FAULT}	FLT pins voltage	-0.3 to 5.5	V
I_{FAULT}	FLT pins current	-1(1)/+10	mA
E_{AS}	Single pulse avalanche energy (T_{AMB} = 125 °C, V_{CC} = 24 V, I_{OUT} = 2 A)	14	J
P_{TOT}	Power Dissipation at T_C = 25 °C	Internally limited	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Junction Operating Temperature	Internally limited	°C
T_C	Case Operating Temperature	-40 to 150	°C

1. *intended as worst case when IC is in normal operation (no fault)*

chanhvinh.com

4 Thermal data

Table 3. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{th(JC)}$ (1)	Thermal resistance junction-case per channel	0.7	°C/W
$R_{th(JA)}$ (2)	Thermal resistance junction-ambient	22	°C/W

1. *Rth between the die and the bottom case surface measured by cold plate as per JESD51.*
2. *JESD51-7.*

chanhvinh.com

5 Electrical characteristics

(8 V < V_{CC} < 60 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4. Supply

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{UVON}	Under-voltage ON threshold	-	6.9	-	8	V
V_{UVOFF}	Under-voltage OFF threshold	-	6.5	-	7.8	V
V_{UVH}	Under-voltage hysteresis	-	0.15	0.5	-	V
I_{SOFF}	Supply current in OFF state	V_{CC} = 24 V, IN = GND, OUT = open load;	0.28	-	0.64	mA
		V_{CC} = 36 V, IN = GND, OUT = open load;	0.28	-	0.64	mA
		V_{CC} = 60 V, IN = GND, OUT = open load;	0.29	-	0.685	mA
I_{SON}	Supply current in ON state	V_{CC} = 24 V, IN = 5 V, OUT = open load;	1.05	-	2.25	mA
		V_{CC} = 36 V, IN = 5 V, OUT = open load;	1.15	-	2.35	mA
		V_{CC} = 60 V, IN = 5 V, OUT = open load;	1.35	-	2.55	mA

Table 5. Output stage

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{DSON}	On-state resistance	V_{CC} = 24 V, R_{LOAD} = 12 Ω, @ T_J = 25 °C	-	12	15	mΩ
		V_{CC} = 24 V, R_{LOAD} = 12 Ω, @ T_J = 125 °C	-	-	25	mΩ
$V_{OUT(OFF)}$	OFF state output voltage	V_{IN} = 0 V and I_{OUT} = 0 A	-	-	2	V
$I_{OUT(OFF)}$	OFF state output current	V_{IN} = 0 V, V_{OUT} = 0 V	-	-	10	µA

Table 6. Switching

(V_{CC} = 24 V; -40 °C < T_J < 125 °C, R_{LOAD} = 12 Ω, input rise time < 0.1 µs)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_r	Rise time		-	30	60	µs
t_f	Fall time		-	25	60	µs
$t_{PD(L-H)}$	Propagation delay time IN to OUT, low to high		-	13	25	µs
$t_{PD(H-L)}$	Propagation delay time IN to OUT, high to low		-	60	100	µs
td(Vccon)	Propagation delay time IN to OUT at power-on	V_{IN} = V_{CC} and rising from 0 to 24 V	150	500	1600	µs

chanhvinh.com

Figure 3. **Timing**

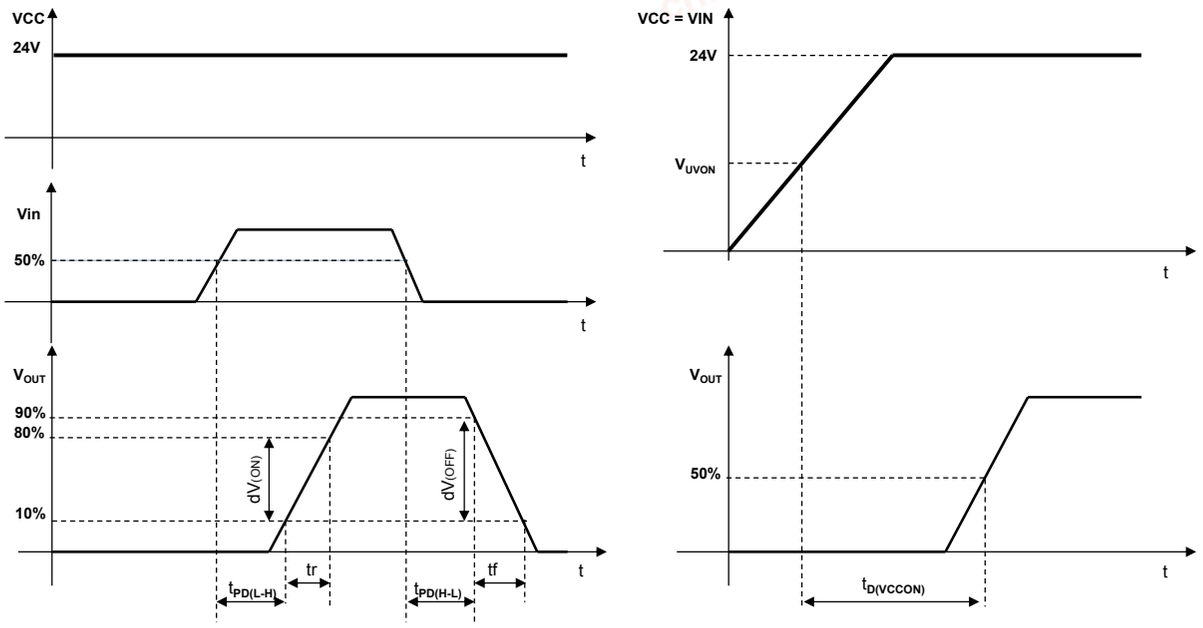


Table 7. **Input pin (IN)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input pin low level voltage	-	-	-	0.8	V
V_{IH}	Input pin high level voltage	-	2.2	-	-	V
$V_{I(HYST)}$	Input pin hysteresis voltage	-	-	0.4	-	V
I_{IN}	Input pin current	$V_{IN} = V_{CC}$ = 36 V	-	-	200	µA
		$V_{IN} = V_{CC}$ = 60 V	-	-	600	

Table 8. **Diagnostic pins (FLT_1, FLT_2)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IH_{FLT}	Diagnostic pins source current in fault condition.	V_{FLT} = 1 V (fault condition active)	-2.0	-	-4.0	mA
		V_{FLT} = 5 V (fault condition active)	-0.4	-0.7	-1.0	
IL_{FLT}	Diagnostic pins leakage current	Normal operation V_{CC} = 60 V	0	-	-25	µA
BT_{FLT}	Diagnostic pins blanking time	-	60	-	400	µs
VCL_{FLT}	Diagnostic pins clamp voltage	I_{FLT} = +1 mA	6	6.8	8	V
		I_{FLT} = -1 mA	-	-	0.7	

chanhvinh.com

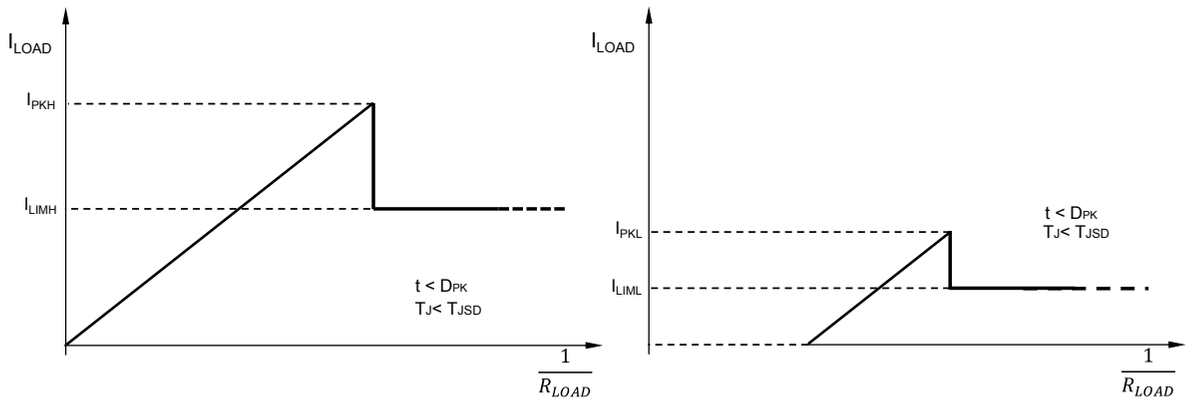
Table 9. Protections and diagnostics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
Overload with Dual Threshold Protection: I_{PD} pin to GND by C_{PD} (470 pF ≤ C_{PD} ≤ 470 nF); see Section 7.3.1							
I_{PKH}	Initial over-current activation threshold	V_{CC} = 24 V	IPS1025H	-	15.4	-	A
			IPS1025H-32		25.1		
I_{LIMH}	Initial over-current limitation level	V_{CC} = 24 V	IPS1025H	6.25	9.0	11.75	A
			IPS1025H-32	12.5	17.9	23.2	
D_{PK}	Time limit of Initial over-current	V_{CC} = 24 V		-	215*C_{PD} [nF]	-	µs
I_{PKL}	Steady state over-current activation threshold	V_{CC} = 24 V	IPS1025H	-	8.0	-	A
			IPS1025H-32		13.1	-	
I_{LIML}	Steady state over-current limitation level	V_{CC} = 24 V	IPS1025H	2.5	3.5	4.5	A
			IPS1025H-32	5.7	8.0	10.4	
I_{HYS}	Steady state output Current limitation hysteresis	V_{CC} = 24 V		-	0.3	-	A
$I_{LIML-OFF}$	Steady state over-current limitation deactivation threshold			-	I_{LIML} - I_{HYS}	-	A
Overload with Single Level (Lowest) Protection: I_{PD} pin connected to IN by 10 kΩ resistor; see Section 7.3.2							
I_{PKL}	Steady state over-current activation threshold	V_{CC}= 24 V	IPS1025H	-	8.0	-	A
			IPS1025H-32		13.1	-	
I_{LIML}	Steady state over-current limitation level		IPS1025H	2.5	3.5	4.5	A
			IPS1025H-32	5.7	8.0	10.4	
I_{HYS}	Steady state output Current limitation hysteresis	V_{CC}= 24 V		-	0.3	-	A
$I_{LIML-OFF}$	Steady state over-current limitation deactivation threshold			-	I_{LIML}-I_{HYS}	-	A
Overload with Single Level (Highest) Protection: I_{PD} pin connected to GND by 10 kΩ resistor; see Section 7.3.3							
I_{PKH}	Initial over-current activation threshold	V_{CC}= 24 V	IPS1025H	-	15.4	-	A
			IPS1025H-32		25.1		
I_{LIMH}	Initial over-current limitation level	V_{CC}= 24 V	IPS1025H	6.25	9.0	11.75	A
			IPS1025H-32	12.5	17.9	23.2	
Over-temperature protections							
T_{JSD}	Junction temperature shutdown	-		150	170	190	°C
T_{JR}	Junction temperature reset	-		-	150	-	°C
T_{JHYS}	Junction temperature hysteresis	-		-	20	-	°C
T_{CSD}	Case temperature shutdown	-		-	130	-	°C
T_{CR}	Case temperature reset	-		-	110	-	°C
T_{CHYS}	Case temperature hysteresis	-		-	20	-	°C
Ground disconnection/Wire break							
I_{LGND}	GND disconnection output current	V_{INX} = V_{CC} = 24 V, V_{OUT} = 0 V		-	-	0.5	mA
V_{CC} over-voltage							
V_{CLAMP}	V_{CC} Clamp Voltage	I_{CC} ≤ 10 mA		65.5	70.0	73.5	V

chanhvinh.com

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Demagnetization of inductive load						
V_{DEMAG}	Demagnetization Voltage	I_{OUT} = 0.5 A, Load ≥ 10 mH	Vcc-76	Vcc-72.5	Vcc-68	V

Figure 4. High (left) and Low (right) I_{LOAD} control activation thresholds (I_{PK}) and limitation levels (I_{LIM})



chanhvinh.com

6 Output Logic

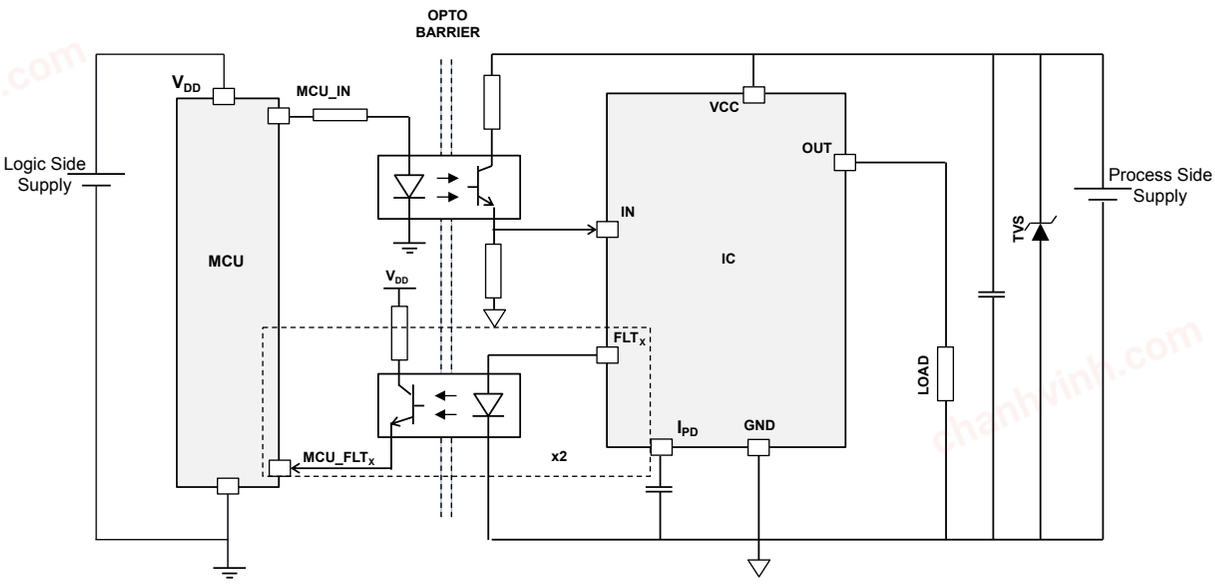
Table 10. Output stage truth table

(L = pin voltage Low, H = pin voltage High, X = not determined)

Condition	IN	OUT	FLT1	FLT2
Normal Operation	L H	L H	L L	L L
Overload protection	L H	L X(1)	L L	L H
Junction over-temperature protection (see Over-temperature)	L H	L L	L H	L L
Case over-temperature protection (see Over-temperature)	L H	L L	L H	L L
UVLO	L H	L L	X X	X X

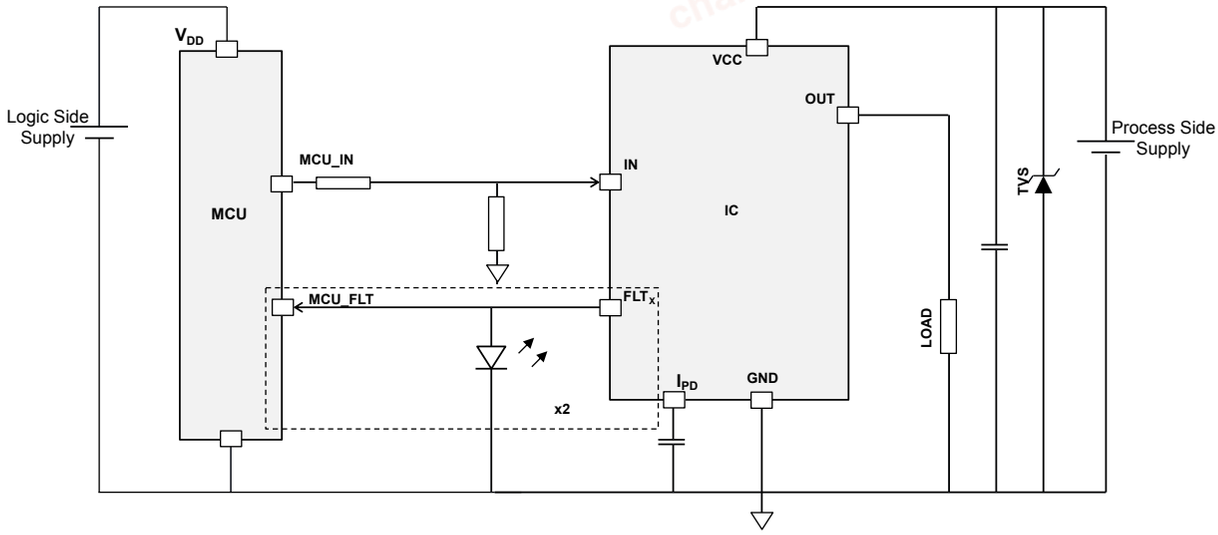
1. *Pin voltage = I_{OUT} * R_{LOAD}*

Figure 5. Typical application diagram with opto-couplers



chanhvinh.com

Figure 6. **Typical application diagram without opto-couplers**



chanhvinh.com

7 Protections and diagnostic

The IC integrates several protections to help the design of robust applications.

7.1 Under-voltage lock-out

The IC is turned off if the voltage on V_{CC} pin falls below the turn-off threshold (V_{UVOFF}). Normal operation restarts after V_{CC} exceeds the turn-on threshold (V_{UVON}). Turn-on and turn-off thresholds are defined in Table 4.

7.2 Over-temperature

The device is protected against overheating in case of overload conditions. During the driving period (when the MCU is forcing the IN pin high), if the output is overloaded, the device suffers two different thermal stresses: one related to the junction temperature of each output channel, and the other related to the whole case temperature.

The two thermal faults (Thermal Junction and Thermal Case) have different trigger thresholds: T_{JSD} and T_{CSD}, respectively.

Usually, in thermal stress conditions due to overload, the junction thermal shutdown is the first protection that is activated: the output channel (OUT) is turned off when its junction temperature (T_J) is higher than the activation threshold (T_{JSD}) and turned back on when it falls below the reset threshold (T_{JR}). This behavior continues while overload on the output persists. When the thermal protection is active, the FLT_1 (current source) becomes active accordingly.

If the thermal protection is active and the temperature of the case (T_C) increases over the case protection threshold (T_{CSD}), then the thermal case protection is activated and the output is switched off until the junction temperature and case temperature fall below their respective reset thresholds (T_{CR} and T_{JR}). The FLT_1 pin is active even when thermal case events occur.

Figure 7 shows the thermal protection behavior, while Figure 8 shows typical temperature trends and output vs. input state.

chanhvinh.com

Figure 7. **Thermal protection flowchart**

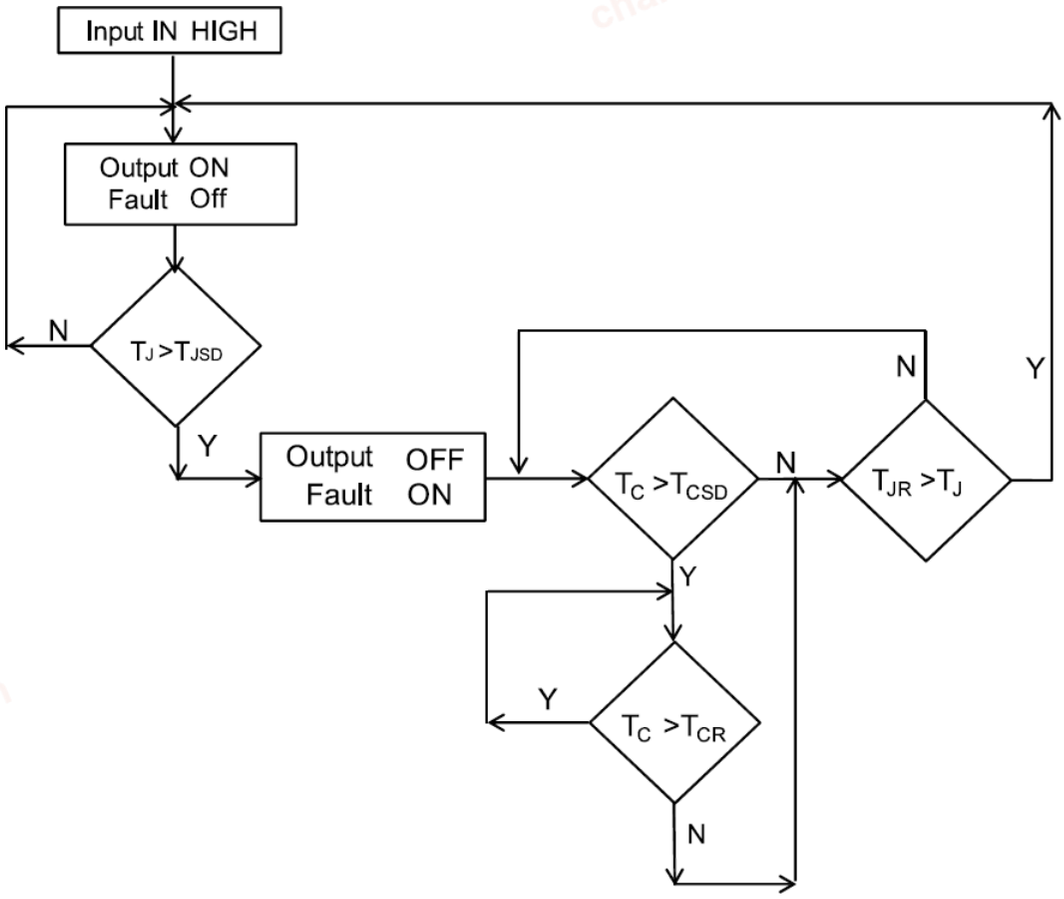
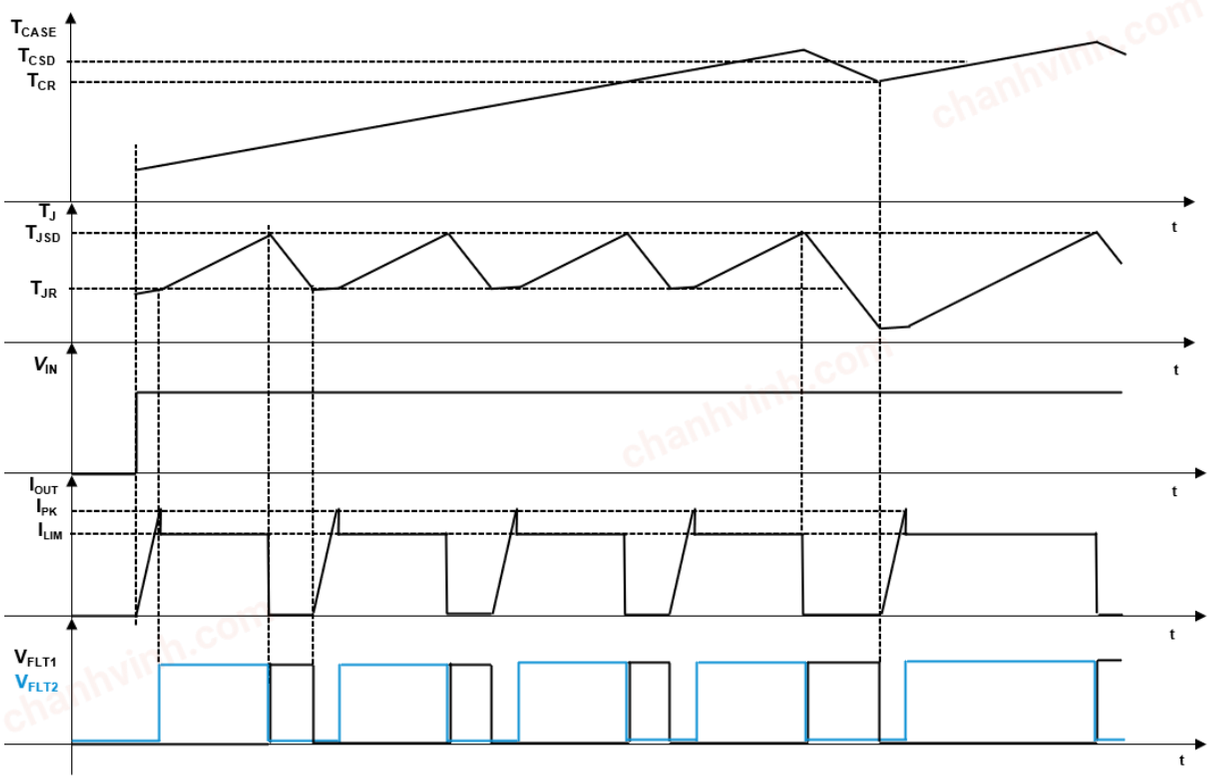


Figure 8. **Thermal protection plot**



chanhvinh.com

7.3 Overload

The IC integrates an overload protection circuit consisting of an output current sensing section and an output current limitation section.

When the output channel is ON, the sensing circuitry monitors the current supplied to the load: if the activation threshold (I_{PK}) is triggered, then the current limitation control circuitry is activated to limit output current to the current limitation level (I_{LIM}) and FLT_2 pin is activated until the overload condition is removed.

See the following sections for details and Table 9 for specific activation thresholds and limitation levels.

Note that while the output channel operates below its activation threshold, the power dissipation can be calculated by $R_{ON} * I_{OUT}^2$, but when the current limitation circuit is activated, power dissipation increases and can be calculated by $V_{DS} * I_{OUT}$, where V_{DS} is the voltage drop between the OUT and V_{CC} pins of the IC. In order to protect the IC against thermal stress, the over-temperature protection is always active and retains the highest priority.

7.3.1 Overload protection with dual threshold

This case is activated when the pin I_{PD} is connected to GND by a capacitor (C_{PD}) and the IC works with two activation thresholds I_{PKH} and I_{PKL}.

The I_{PKH} is active only in the limited time frame between the L-H transition of the IN signal and the D_{PK} delay defined by the following design rule:

$$D_{PK}\,[\mu s] = 215 \times CPD\,[nF]$$

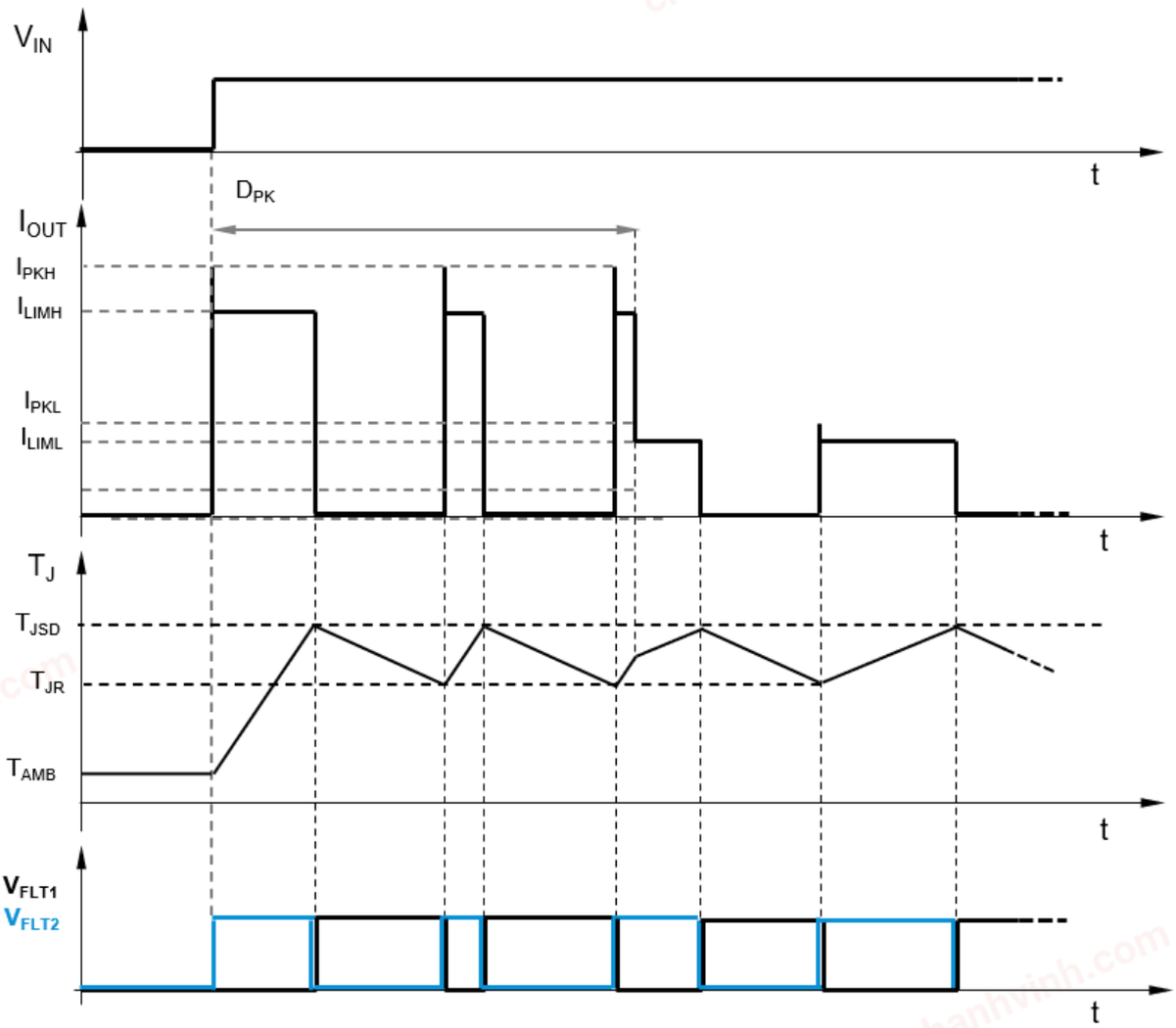
The above design rule is valid in the range 470 pF ≤ C_{PD} ≤ 470 nF (see Table 9).

If the I_{PKH} is triggered within the D_{PK} time frame, then the output current is limited to I_{LIMH}.

After D_{PK} has elapsed, the IC operates with I_{PKL} activation threshold and I_{LIML} limitation level, respectively.

chanhvinh.com

Figure 9. **Short-circuit behavior with dual threshold ($T_{CASE} < T_{CSD}$)**



7.3.2 Overload protection with single (low) threshold

The user can set the activation threshold to I_{PKL} and the limitation level to I_{LIML} by connecting the I_{PD} pin to the IN pin with a 220 KΩ resistor.

This condition is equivalent to setting D_{PK} = 0 µs.

Note: Leaving I_{PD} floating is equivalent to having an initial peak duration of 1 µs.

7.3.3 Overload protection with single (high) threshold

The user can set the activation threshold to I_{PKH} and the limitation level to I_{LIMH} by connecting the I_{PD} pin to GND with a 10 KΩ resistor.

7.4 V_{CC} disconnection protection

V_{CC} disconnection involves the disconnection of the module from the supply line. When this condition is detected, the output channel can be driven normally until the voltage on V_{CC} pin remains higher than the UVLO threshold.

In case of inductive load, if the V_{CC} is disconnected while the channel is active, the energy stored in the inductance is discharged through the power switch thanks to the integrated demagnetization circuit.

chanhvinh.com

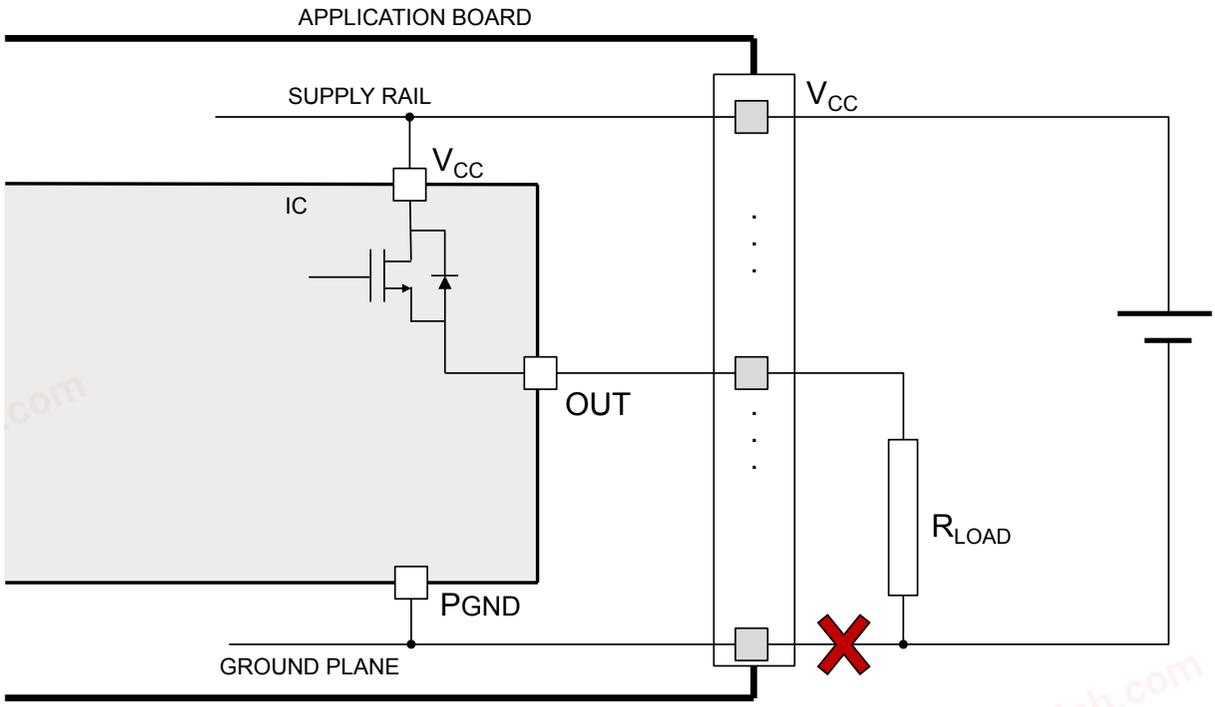
7.5 GND disconnection protection

GND disconnection is the disconnection of the module from the reference line. When this condition occurs, the output channel is turned off regardless of the input status.

When this event occurs, the IC continues working normally until the voltage between V_{CC} and GND pins of the IC results ≥ V_{UVOFF}. The voltage on the GND pin of the IC rises up to the supply rail voltage level. In case of a GND disconnection event, a current (I_{LGND}) flows through OUT pin.

For an inductive load, if the GND is disconnected while the output channel is active, the current flows through the power, which is activated by an active clamp as if the input had been deactivated.

Figure 10. Ground disconnection



chanhvinh.com

8 Active clamp

Active clamp is also known as Fast Demagnetization of inductive loads or Fast Current Decay. When a high-side driver turns off an inductance, an under-voltage on output is detected.

The OUT pin is pulled-down to V_{CC}-V_{DEMAG}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at ~V_{DEMAG} until the load energy has been dissipated. The energy is dissipated in both IC internal switch and load resistance.

Figure 11. Active clamp equivalent principle schematic

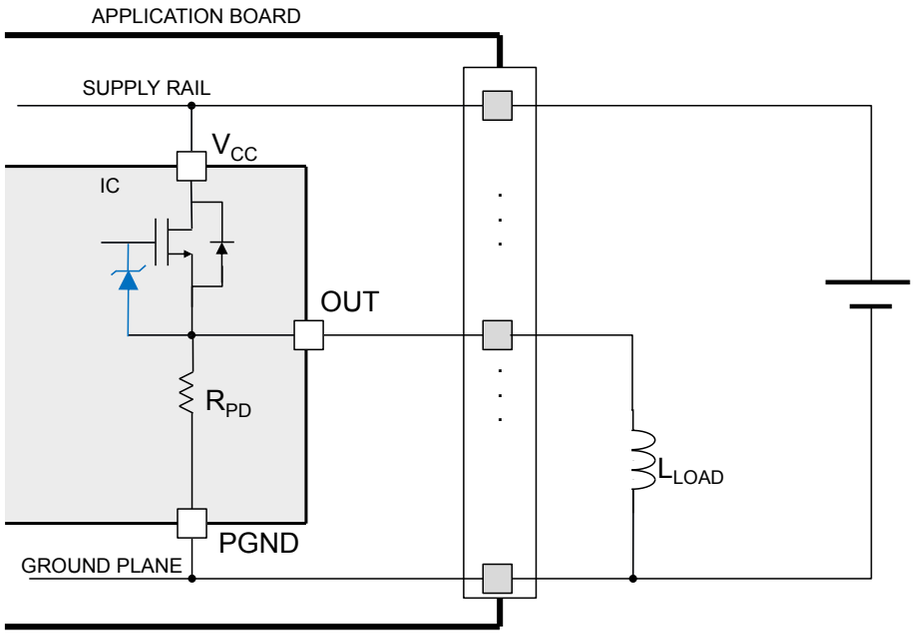
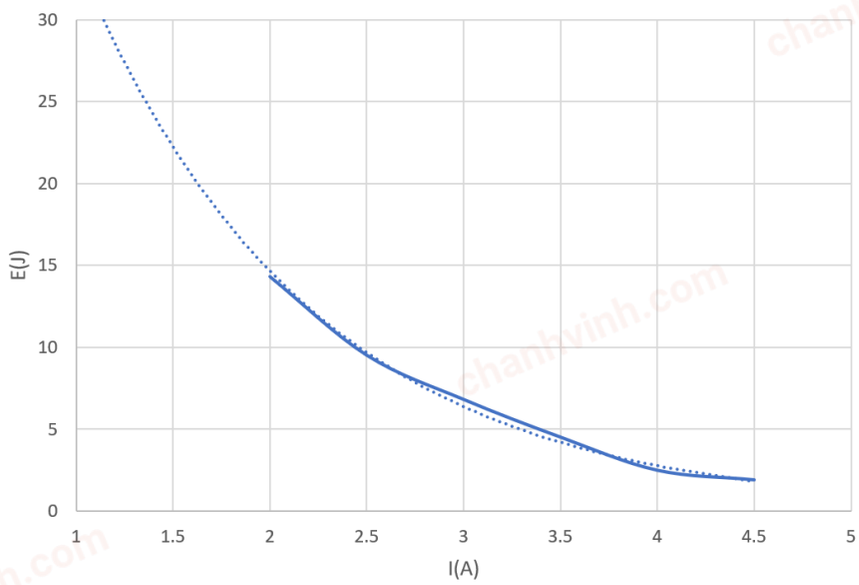


Figure 12. Typical demagnetization energy (single pulse) at V_{CC} = 24 V and T_{AMB} = 125 °C



chanhvinh.com

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Package mechanical data

Figure 13. PowerSSO-24 package dimensions [mm]

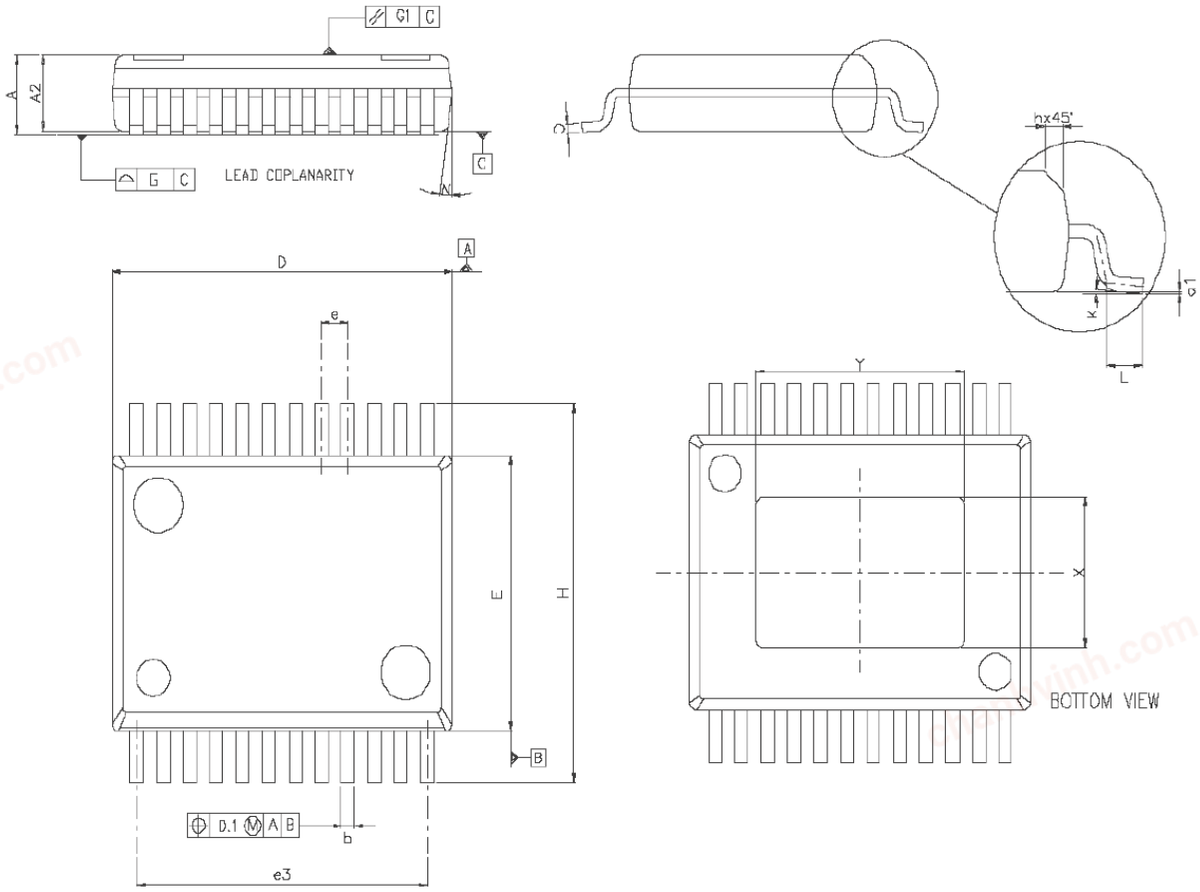


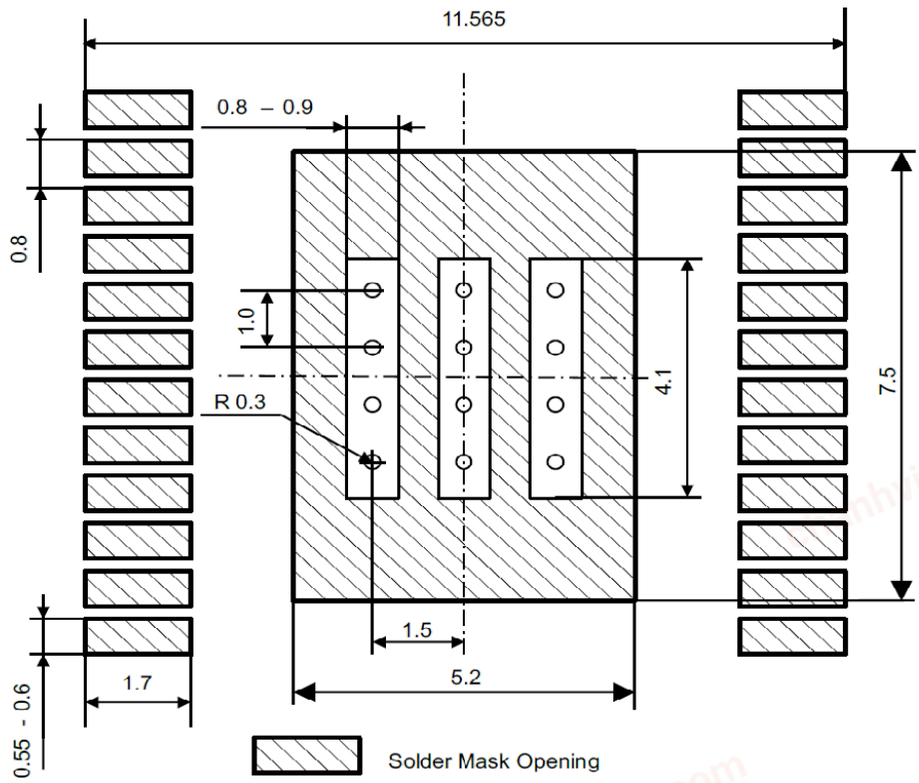
Table 11. PowerSSO-24 mechanical data

Dim.	[mm]		
	Min.	Typ.	Max.
A	2.15	-	2.47
A2	2.15	-	2.40
a1	0	-	0.075
b	0.33	-	0.51
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6

chanhvinh.com

Dim.	[mm]		
	Min.	Typ.	Max.
e	-	0.8	-
e3	-	8.8	-
G	-	-	0.1
G1	-	-	0.06
H	10.1		10.5
h	-	-	0.4
L	0.55	-	0.85
N	-	-	10 deg
X	4.1	-	4.7
Y	6.5	-	7.1

Figure 14. PowerSSO-24 suggested footprint [mm]



STMicroelectronics is not responsible for PCB-related issues. The footprint shown in the above figure is a suggestion which may differ from the customer PCB supplier design rules.

chanhvinh.com

10 PowerSSO-24 packing information

Figure 15. **PowerSSO-24 tube shipment (no suffix)**

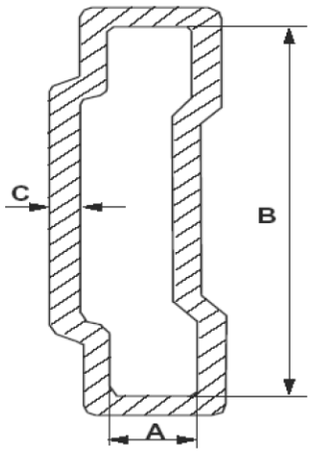


Table 12. **PowerSSO-24 tube shipment information**

All dimensions are in mm

Description	Value
Base quantity	49
Bulk quantity	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

chanhvinh.com

Figure 16. **PowerSSO-24 reel shipment**

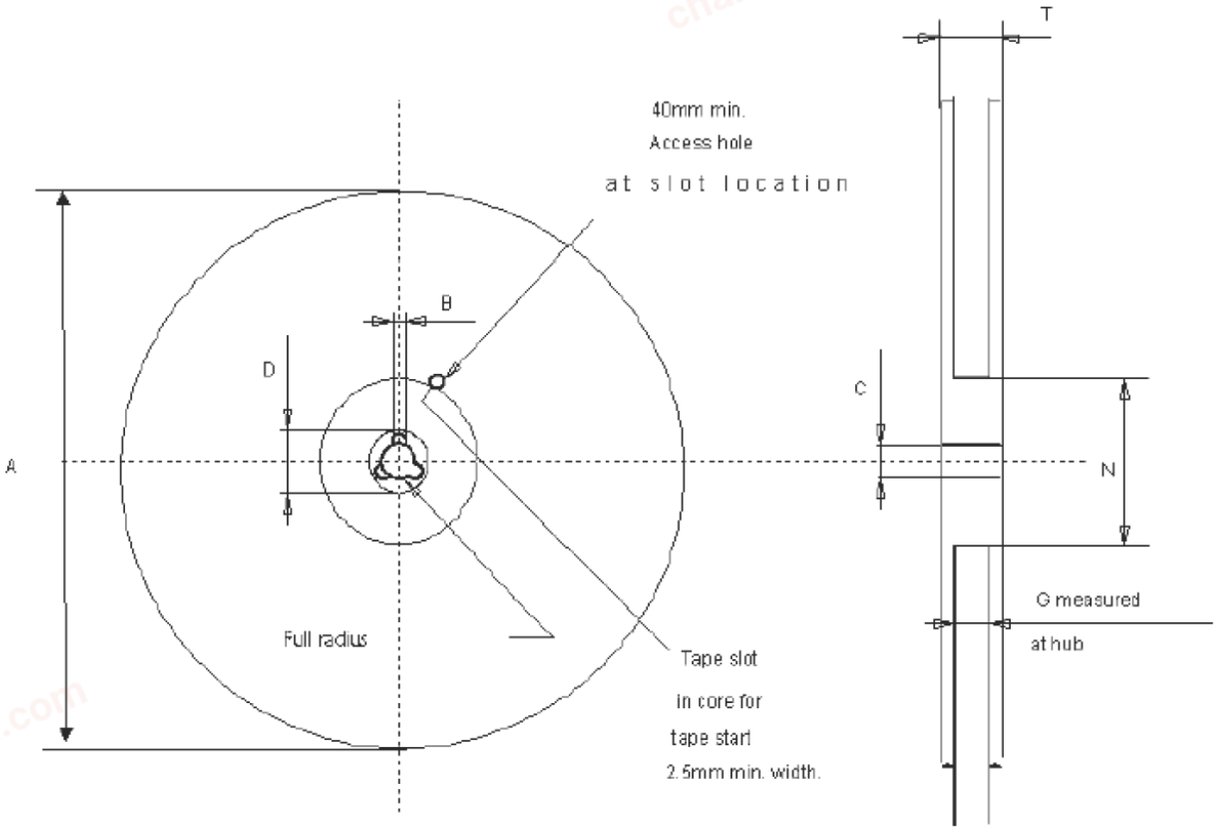


Table 13. **PowerSSO-24 reel information**

All dimensions are in mm

Description	Value
Base quantity	1000
Bulk quantity	1000
A (max.)	330
B (min.)	1.5
C (±0.2)	13
F	20.2
G (2 ±0)	24.4
N (min.)	100
T (max.)	30.4

chanhvinh.com

Figure 17. **PowerSSO-24 tape drawings**

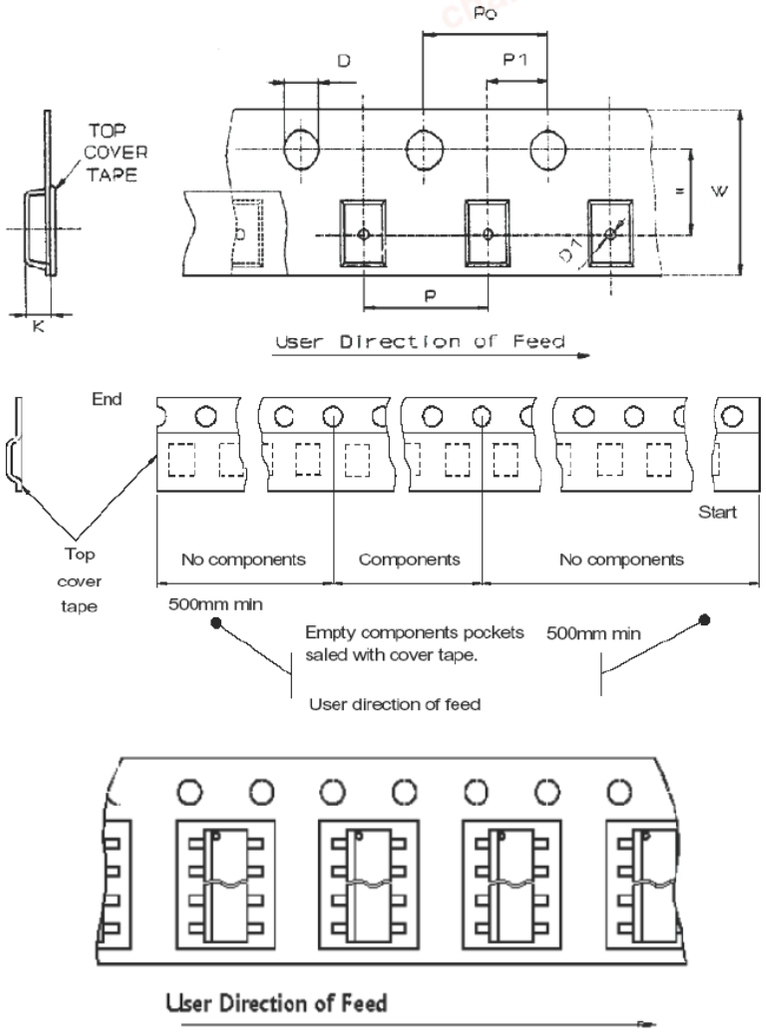


Table 14. **PowerSSO-24 tape dimension**

All dimensions are in mm

Description	Symbol	Value
Tape width	W	24
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	12
Hole diameter	D (± 0.05)	1.55
Hole diameter	D1 (min.)	1.5
Hole position	F (± 0.1)	11.5
Compartment depth	K (max.)	2.85
Hole spacing	P1 (± 0.1)	2

Note: According to the Electronic Industries Association (EIA) standard 481 rev. A, Feb 1986.

chanhvinh.com

11 Ordering information

Table 15. **Ordering information**

Part number	Package	Packaging
IPS1025H	PowerSSO-24	Tube
IPS1025HTR	PowerSSO-24	Tape and reel
IPS1025H-32	PowerSSO-24	Tube
IPS1025HTR-32	PowerSSO-24	Tape and reel

chanhvinh.com

Revision history

Table 16. **Document revision history**

Date	Version	Changes
15-Nov-2021	1	Initial release
28-Mar-2022	2	Table 9: specified only typical values for IPKH and IPKL; table 10: added column for FLT_2 behavior ; changed fig.12; some minor changes.

chanhvinh.com

Contents

1 Block diagram 2
2 Pin connection 3
3 Absolute maximum ratings 4
4 Thermal data 5
5 Electrical characteristics 6
6 Output Logic 10
7 Protections and diagnostic 12
7.1 Under-voltage lock-out 12
7.2 Over-temperature 12
7.3 Overload 14
7.3.1 Overload protection with dual threshold 14
7.3.2 Overload protection with single (low) threshold 15
7.3.3 Overload protection with single (high) threshold 15
7.4 V_{CC} disconnection protection 15
7.5 GND disconnection protection 16
8 Active clamp 17
9 Package information 18
9.1 Package mechanical data 18
10 PowerSSO-24 packing information 20
11 Ordering information 23
Revision history 24

chanhvinh.com

List of figures

Figure 1. IPS1025H, IPS1025H-32 block diagram . . . 2
Figure 2. Pin connections (top through view) . . . 3
Figure 3. Timing . . . 7
Figure 4. High (left) and Low (right) I_{LOAD} control activation thresholds (I_{PK}) and limitation levels (I_{LIM}) . . . 9
Figure 5. Typical application diagram with opto-couplers . . . 10
Figure 6. Typical application diagram without opto-couplers . . . 11
Figure 7. Thermal protection flowchart . . . 13
Figure 8. Thermal protection plot . . . 13
Figure 9. Short-circuit behavior with dual threshold ($T_{CASE} < T_{CSD}$) . . . 15
Figure 10. Ground disconnection . . . 16
Figure 11. Active clamp equivalent principle schematic . . . 17
Figure 12. Typical demagnetization energy (single pulse) at V_{CC} = 24 V and T_{AMB} = 125 °C . . . 17
Figure 13. PowerSSO-24 package dimensions [mm] . . . 18
Figure 14. PowerSSO-24 suggested footprint [mm] . . . 19
Figure 15. PowerSSO-24 tube shipment (no suffix) . . . 20
Figure 16. PowerSSO-24 reel shipment . . . 21
Figure 17. PowerSSO-24 tape drawings . . . 22

chanhvinh.com

List of tables

Table 1. Pin descriptions . . . 3
Table 2. Absolute maximum ratings . . . 4
Table 3. Thermal data . . . 5
Table 4. Supply . . . 6
Table 5. Output stage . . . 6
Table 6. Switching . . . 6
Table 7. Input pin (IN) . . . 7
Table 8. Diagnostic pins (FLT_1, FLT_2) . . . 7
Table 9. Protections and diagnostics . . . 8
Table 10. Output stage truth table . . . 10
Table 11. PowerSSO-24 mechanical data . . . 18
Table 12. PowerSSO-24 tube shipment information . . . 20
Table 13. PowerSSO-24 reel information . . . 21
Table 14. PowerSSO-24 tape dimension . . . 22
Table 15. Ordering information . . . 23
Table 16. Document revision history . . . 24

chanhvinh.com

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved