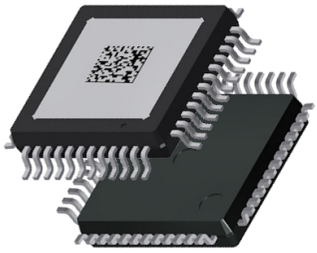
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HFA80A

Data brief

4-channel analog input class-D automotive audio amplifier with Hi-Fi audio quality, advanced diagnostics and 2 MHz switching frequency



LQFP48L exposed pad up (7x7x1.4 mm)

Product summary		
Order code	**Package**	**Packing**
HFA80A-F2Y	LQFP48L 7x7x1.4 mm	Tray
HFA80A-F2T		Tape and reel

Features

- AEC-Q100 qualified
- Supply operating range: 4.5 V - 18 V
- EMI compliant to CISPR25 level V
- Class-D BTL outputs
- Battery load dump compatible (40 V)
- Reduced size and cost of output LC thanks to 2 MHz switching PWM
- Extended audio band support
- Multiple load configurations:
  - Able to drive 4 Ω and 2 Ω speaker loads
  - Both speaker and line driver options
- MOSFET power outputs allowing high output power capability:
  - Typ 4 x 28.5 W/4 Ω at 14.4 V, 1 kHz, THD = 10%
  - Typ 4 x 23 W/4 Ω at 14.4 V, 1 kHz, THD = 1%
  - Typ 4 x 49 W/2 Ω at 14.4 V, 1 kHz, THD = 10%
  - Typ 4 x 39 W/2 Ω at 14.4 V, 1 kHz, THD = 1%
- Audio performances at 4 Ω, 14.4 V, 1 kHz:
  - THD 0.015% typ at 1 W, 1 kHz on 4 Ω loads
  - Output noise 52 typ µV at 26 dB gain
  - Crosstalk 86 dB typ at 1 W, 1 kHz on 4 Ω loads
  - PSRR 80 dB typ at 1 W, 1 kHz on 4 Ω loads
- Fast turn-on and very low latency for high-speed audio processing applications
- I^2C full configurability with channel independent mute/play/gain selection/ diagnostic
- 4 I^2C addresses
- I^2C bus driving: fast I^2C (1Mhz clock) option
- Output PWM clock spread spectrum
- Full diagnostic matrix with info available both on I^2C and CD/DIAG pin:
  - Independent by-channel DC and AC load detection diagnostic with selectable threshold
  - Startup diagnostic for shorts to VCC/GND
  - Overcurrent protection with configurable threshold (2 selectable)
  - Input voltage DC offset detector
  - Free-running output current offset detector
- Thermal protection and thermal warning (4 thermal warnings)
- DAM (digital admittance meter)
- Synchronization input/output pin
- Immune to pop/tick noise at turn on/off, battery variations, during diagnostic
- Legacy (backup mode without I^2C control)
- ESD integrated protections (2 kV HBM, 500 V/750 V corner CDM)
- LQFP48L exposed pad up package

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Description

The HFA80A is a new STMicroelectronics class-D audio amplifier, specifically designed for automotive applications in BCD9s technology.

The HFA80A integrates advanced solutions for an excellent radiated noise immunity combined with the advantages of 2 MHz switching PWM class-D output stages. This configuration allows outstanding audio performances while designing a compact and inexpensive application.

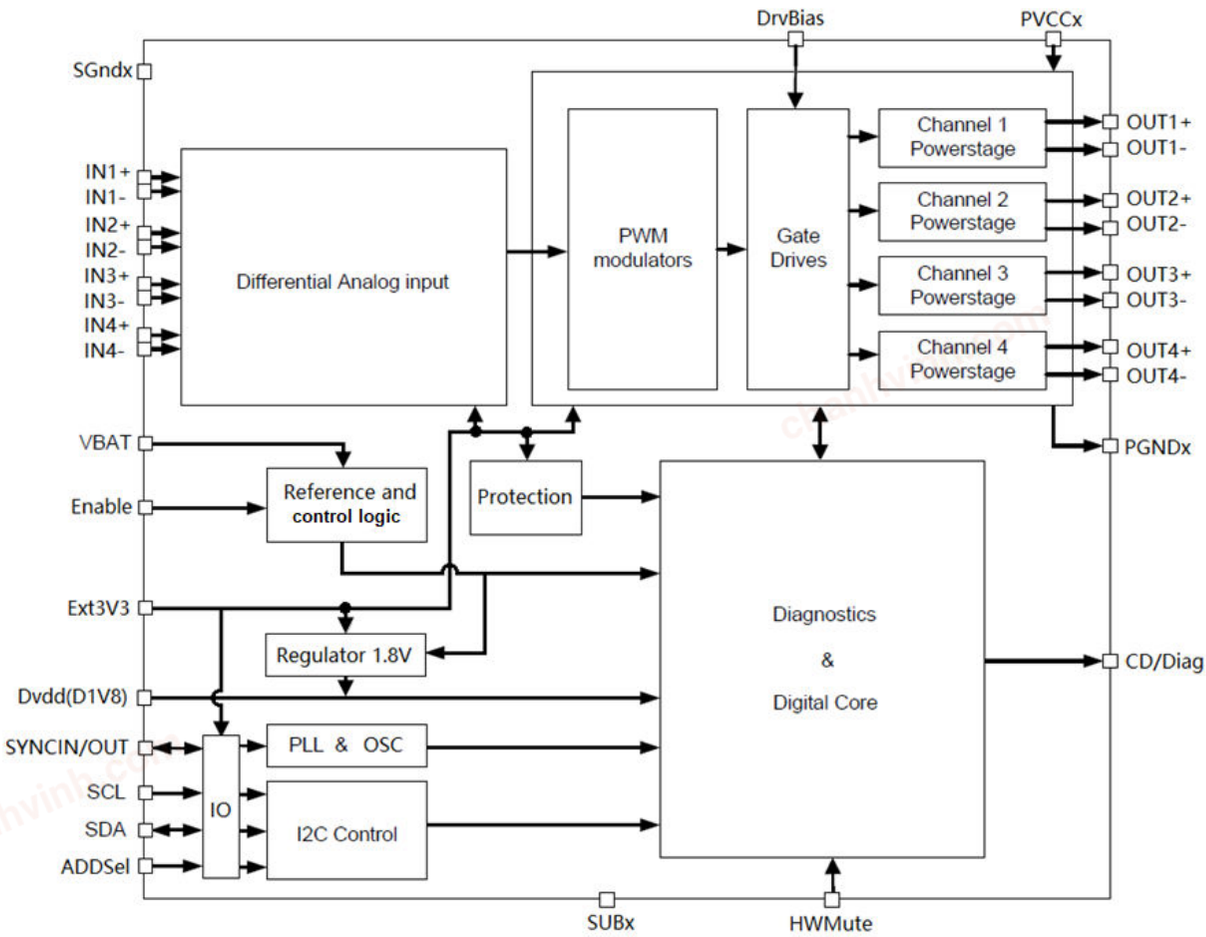
The HFA80A supports wide band applications with extremely low level of noise and low THD. Moreover, it features a broad diagnostics matrix able to support the most demanding OEM requirements in terms of speaker control and system robustness/reliability. The HFA80A supports start/stop cranking down to 4.5 V and is housed in a very compact and thin LQFP 7x7 package, making it suitable for any level of automotive application.

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1 Block diagram and pin description

1.1 Block diagram

Figure 1. **Block diagram**



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1.2 Pin description

Figure 2. **Device pinout**

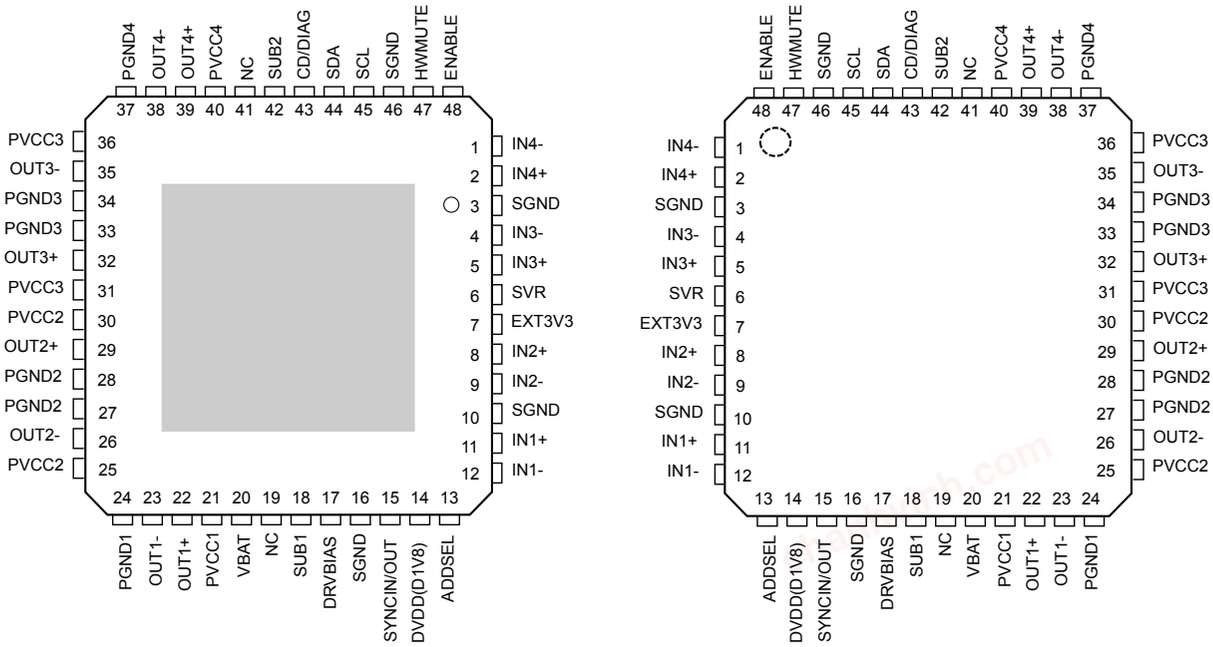


Table 1. **Pin function**

#	Name	Function	Definition	Internal structure
1	IN4-	CH 4, half bridge minus	Input	-
2	IN4+	CH 4, half bridge plus	Input	-
3	SGND	Signal ground	Supply	-
4	IN3-	CH 3, half bridge minus	Input	-
5	IN3+	CH 3, half bridge plus	Input	-
6	SVR	Supply voltage rejection	Internal reference	-
7	EXT3V3	Auxiliary external 3.3 V supply	Supply	-
8	IN2+	CH 2, half bridge plus	Input	-
9	IN2-	CH 2, half bridge minus	Input	-
10	SGND	Signal ground	Supply	-
11	IN1+	CH 1, half bridge plus	Input	-
12	IN1-	CH 1, half bridge minus	Input	-
13	ADDSEL	Address selection	Input	-
14	DVDD(D1V8)	Digital power supply	Supply	-
15	SYNCIN/OUT	Synchronization clock in/out	Input/Output	Push-pull
16	SGND	Signal ground	Supply	-
17	DRVBIAS	Gate driver Bias	Internal reference	-
18	SUB1	Ground die substrate pin	Supply	-
19	NC	Not connected	-	-
20	VBAT	Battery voltage pin	Supply	-
21	PVCC1	CH 1, power supply	Supply	-

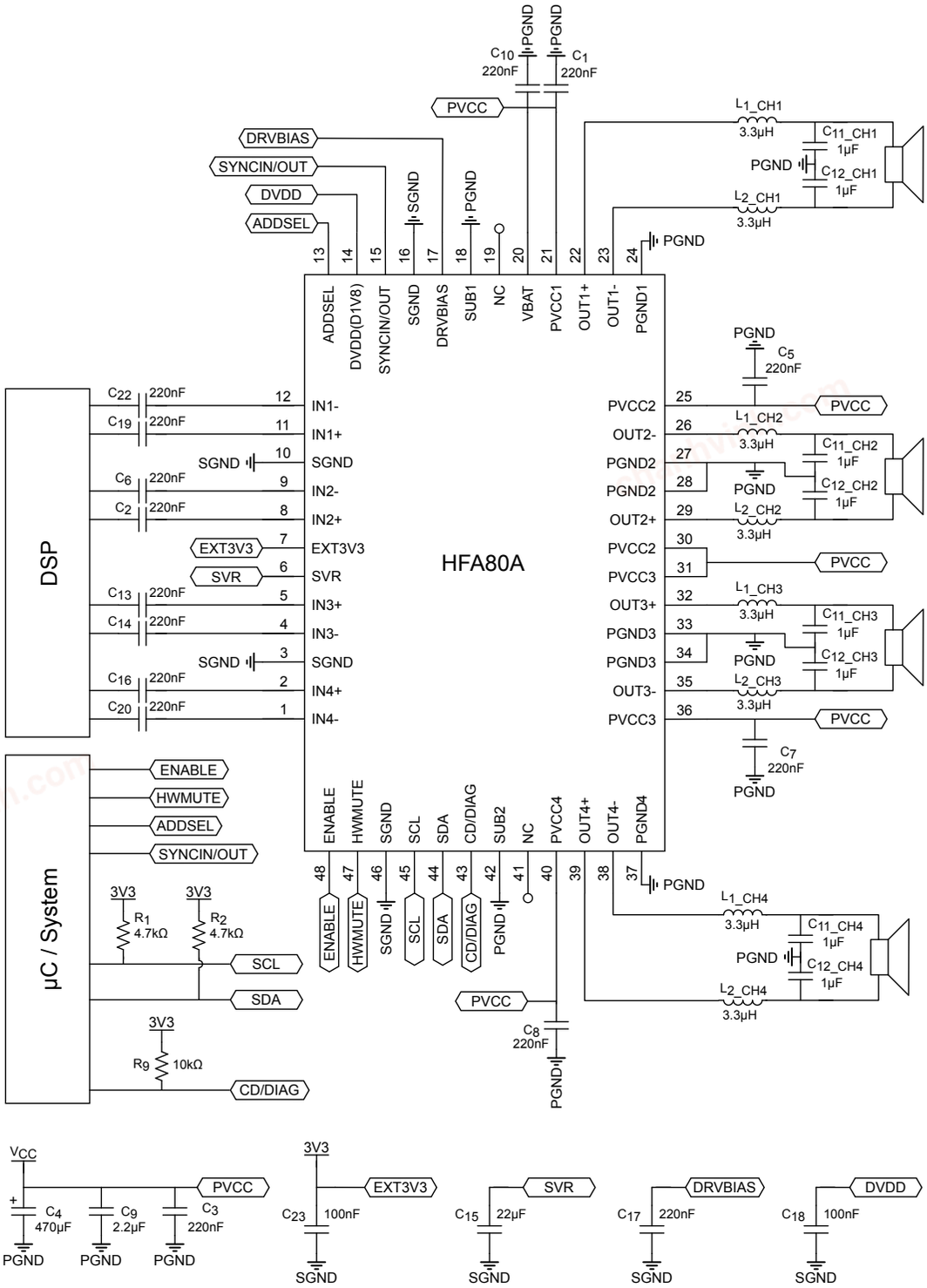
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#	Name	Function	Definition	Internal structure
22	OUT1+	CH 1, half bridge plus	Output	-
23	OUT1-	CH 1, half bridge minus	Output	-
24	PGND1	CH 1, power ground	Supply	-
25	PVCC2	CH 2, power supply	Supply	-
26	OUT2-	CH 2, half bridge minus	Output	-
27	PGND2	CH 2, power ground	Supply	-
28	PGND2	CH 2, power ground	Supply	-
29	OUT2+	CH 2, half bridge plus	Output	-
30	PVCC2	CH 2, power supply	Supply	-
31	PVCC3	CH 3, power supply	Supply	-
32	OUT3+	CH 3, half bridge plus	Output	-
33	PGND3	CH 3, power ground	Supply	-
34	PGND3	CH 3, power ground	Supply	-
35	OUT3-	CH 3, half bridge minus	Output	-
36	PVCC3	CH 3, power supply	Supply	-
37	PGND4	CH 4, power ground	Supply	-
38	OUT4-	CH 4, half bridge minus	Output	-
39	OUT4+	CH 4, half bridge plus	Output	-
40	PVCC4	CH 4, power supply	Supply	-
41	NC	Not connected	-	-
42	SUB2	Ground die substrate pin	Supply	-
43	CD/DIAG	Clipping detector and diagnostic	Output	Open-drain
44	SDA	I^2C data	Input/Output	Open-drain
45	SCL	I^2C clock	Input	-
46	SGND	Signal ground	Supply	-
47	HWMUTE	Hardware mute	Input	Internal pull-up
48	ENABLE	Enable	Input	-

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2 Application schematic

Figure 3. **Application schematic**



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3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC\ max}$	DC supply pins [VBAT, PVCC(x)]	-0.3 to 40	V
$OUT_{(x)}^{+}$, $OUT_{(x)}^{-}$	Output ± pin	-0.3 to 25	V
EXT3V3	Voltage on EXT3V3 pin	-0.3 to 4.6	V
$IN_{(x)}^{+}$, $IN_{(x)}^{-}$	Analog input ± max	-0.3 to 4.6	V
$I2C_{data}$, $I2C_{clk}$	I^2C bus pins [SDA, SCL]	-0.3 to 4.6	V
SYNCHIN/OUT	Synchronization pin	-0.3 to 4.6	V
ADDSEL	Address selection pin	-0.3 to 4.6	V
ENABLE	Enable pin	-0.3 to 4.6	V
CD/DIAG	Clipping detector and diagnostic pin	-0.3 to 4.6	V
HWMUTE	Hardware mute pin	-0.3 to 4.6	V
GND_{max}	Voltage difference between ground pins [SGND, $PGND_{(x)}$, $SUB_{(x)}$]	-0.3 to 0.3	V
DRVBIAS	Gate driver bias pin (1)	-0.3 to 20	V
SVR	Internal reference pin(1)	-0.3 to 4.6	V
DVDD(D1V8)	Digital power supply pin(1)	-0.3 to 2.5	V
T_{amb}	Ambient operating temperature	-40 to 125	°C
T_{stg},T_j	Storage and junction temperature	-55 to 150	°C
ESD_{HBM}	ESD protection HBM(2)	2000	V
ESD_{CDM}	ESD protection CDM standard(2)	500	V
	ESD protection CDM corner(2)	750	V

1. *Internal circuit output pin: not to be controlled externally.*
2. *Conforming to ESD standard.*

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthjc	Rth junction to case(1)	2.05	°C/W

1. *By simulation with top cold plate as per Jedec best practice guidelines (JESD51) in contact with package top side (e-pad). Ambient temperature set to 85 °C.*

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4 General description

The HFA80A is a quad channel, analog input, class-D BTL audio amplifier with advanced diagnostics, high PWM switching frequency and high-resolution audio. The high integration level and the embedded signal processing allow achieving excellent audio performances.

The HFA80A includes an I^2C-bus interface to control the operation and read the state of the power amplifier, performs diagnostics and in general accesses the features reported in this datasheet.

The communication load towards the microcontroller is eased by the presence of a dedicated clipping detector and diagnostics output pin, CD/DIAG, that can trigger the host to read important information as it becomes available. All useful information derived from internal detectors (thermal warnings, output offset, overcurrent protection etc.) can in fact be selectively set to toggle the CD/DIAG pin, according to programmable configuration registers.

The HFA80A implements a new concept of load diagnostics specifically designed for automotive applications, embedding a highly reliable noise-immune load diagnostic algorithm with self-generated stimuli: this allows to detect anomalous load connections or variations and makes this information available through the I^2C-bus.

4.1 Input stage

The HFA80A can work with differential or single-ended input signals. Using either has no impact on the gain of the device.

4.2 Gain selection

The HFA80A has four possible gain configurations for each channel. Each channel can be configured independently with a different gain.

4.3 Pulse-width modulator - PWM

The HFA80A channels output a modulated version of the analog input, through in-phase pulse-width modulation. Thanks to proprietary technology, this is performed with excellent stability, high bandwidth, low noise and low distortion. The PWM signal is demodulated by an external LC filter.

The choice of a high PWM switching frequency allows the use of a small-sized inductor for the demodulator filter, thus contributing to the minimization of PCB real estate occupation and cost, and makes the PWM tones lie outside the AM band, thus avoiding by design EMC interference due to the PWM harmonics.

4.4 Feedback before LC filter topology

The device works with a “feedback before the LC filter” output topology. This choice, together with the 2 MHz switching PWM, allows for the usage of smaller and cost-effective components for the demodulator filter. The HFA80A is guaranteed with a flat frequency response up to around 40 kHz, but can reach up to 80 kHz of bandwidth by tailoring the demodulator filter for this task.

4.5 Load configurations

The HFA80A supports several load configurations. The default configuration is suitable for a 4-speaker (front/rear - left/right) application. A line driver option is also available: this mode improves performance when driving high impedance loads that require a lower output current.

The maximum allowed supply voltage depends on the impedance of the loads.

4.6 Low latency

The HFA80A offers a very low latency signal processing pipeline: the delay from input analog signal to output PWM is in the order of few µs.

This makes the HFA80A eligible for high-speed audio processing applications like noise cancelling.

4.7 Spread spectrum

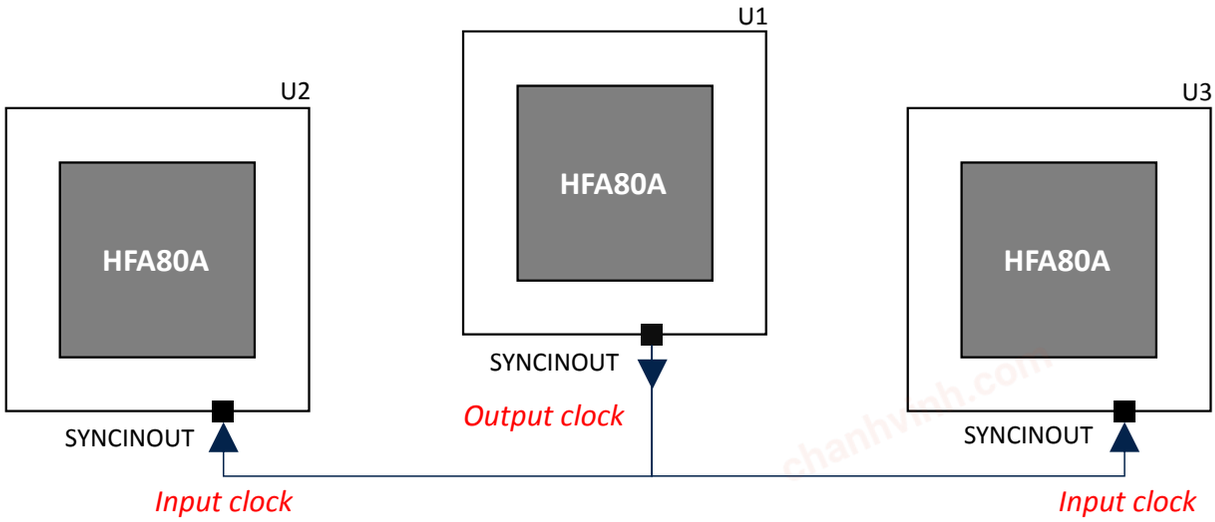
Thanks to the spread spectrum feature, HFA80A is EMI-compliant according to CISPR25 up to Class V.

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4.8 System clock and synchronization

The HFA80A features a synchronization pin that can be used to either receive and use a synchronization signal to generate the internal clock, or to synchronize the clock of other devices to the clock generated inside the device in question in case of multiple device applications (see the Figure 4).

Figure 4. Example of multiple channels system with synchronized clock



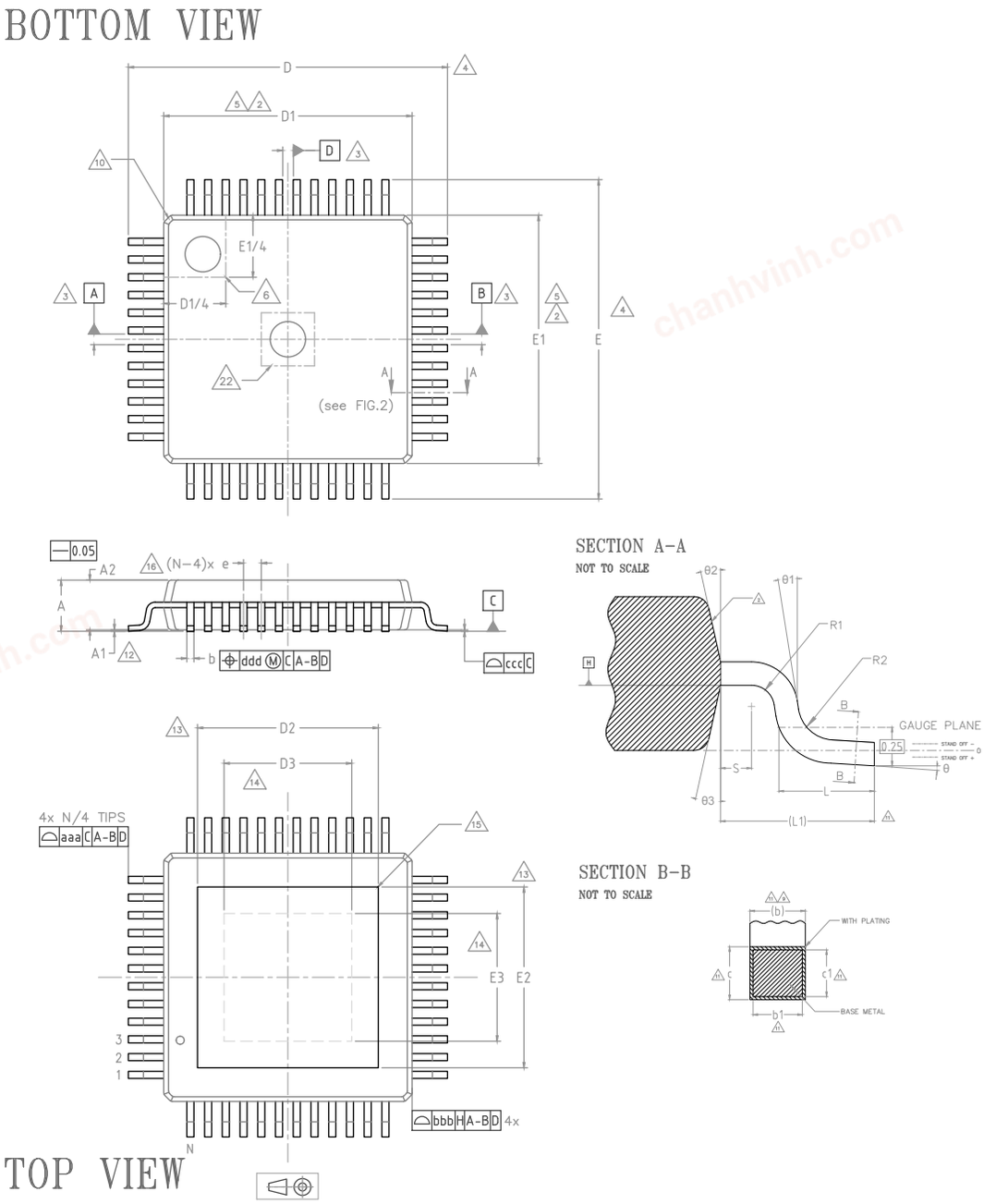
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5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LQFP48L (7x7x1.4 mm exp. pad up) package information

Figure 5. LQFP48L (7x7x1.4 mm exp. pad up) package outline



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Table 4. **LQFP48L (7x7x1.4 mm exp. pad up) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ	0°	3.5°	7°
Θ1	0°	-	-
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A	-	-	1.49
A1	-0.03	-	0.05
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
D2	-	-	5.60
D3	3.90	-	-
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
E2	-	-	5.60
E3	3.90	-	-
L	0.45	0.60	0.75
L1	1.00 REF		
N	48		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		

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Revision history

Table 5. **Document revision history**

Date	Revision	Changes
05-Jun-2024	1	First release.

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