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HCF4094

8-stage shift and store bus register with 3-stage outputs

Datasheet - production data



SO-16

Features

- 3- state parallel outputs for connection to common bus
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Medium speed operation 5 MHz at 10 V
- Quiescent current specified up to 20 V
- Standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings
- Input leakage current I_I = 100 nA (max.) at V_{DD} = 18 V, T_A = 25 °C
- 100% tested for quiescent current
- ESD performance
  - HBM: 1 kV
  - MM: 200 V
  - CDM: 1 kV

Applications

- Automotive
- Industrial
- Computer
- Consumer

Description

The HCF4094 is a monolithic integrated circuit fabricated in metal oxide semiconductor technology available in an SO-16 package. The HCF4094 is an 8-stage, serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data are shifted on positive clock transition. The data in each shift register stage are transferred to the storage register when the STROBE input is high. Data in the storage register appear at the outputs whenever the OUTPUT-ENABLE signal is high. Two serial outputs are available for cascading a number of HCF4094 devices. Data are available at the Q_S serial output terminal on positive clock edges to allow for high speed operation in a cascaded system in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading HCF4094 devices when the clock rise time is slow.

Table 1. Device summary table

Order code	Temperature range	Package	Packing	Marking
HCF4094M013TR	-55 ° C to +125 ° C	SO-16	Tape & reel	HCF4094
HCF4094YM013TR(1)	-40 ° C to +125 ° C	SO-16 (automotive grade)(1)		HCF4094Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

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1 Pin information

Figure 1. Pin connections (top view)

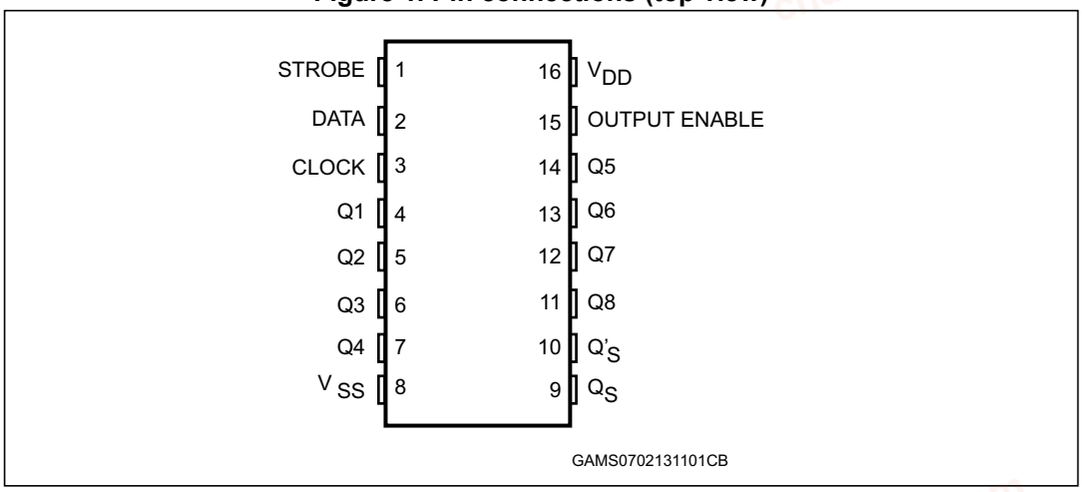

Table 2. Pin description

Pin no	Symbol	Name and function
2	DATA	Data input
1	STROBE	Strobe input
3	CLOCK	Clock input
9, 10	Q_S, Q'_S	Serial outputs
4, 5, 6, 7, 14, 13, 12, 11	Q1 to Q8	Parallel outputs
15	OUTPUT ENABLE	Output enable input
8	V_{SS}	Negative supply voltage
16	V_{DD}	Positive supply voltage

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2 Functional description

Figure 2. Logic diagram

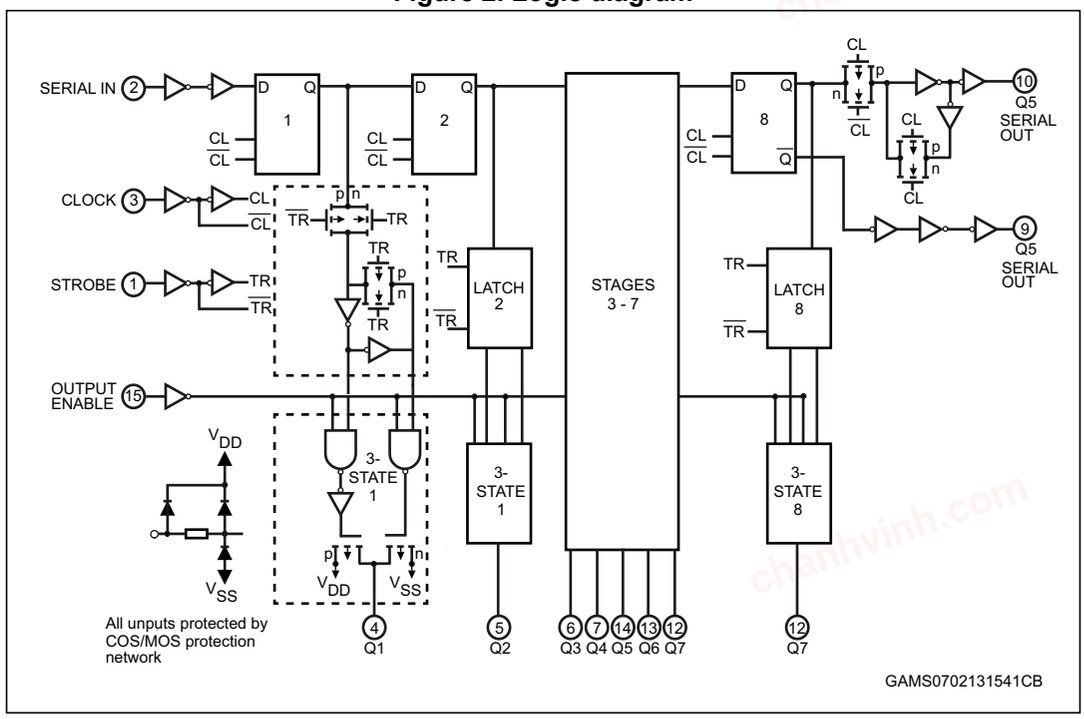

Table 3. Truth table

Clock	Output enable	Strobe	Data	Parallel outputs		Serial outputs	
				Q_1	Q_n	Q_S(1)	Q'_S
⎍	L	X(2)	X(2)	OC(3)	OC(3)	Q7	No change
⎎	L	X(2)	X(2)	OC(3)	OC(3)	No change	Q7
⎍	H	L	X(2)	No change	No change	Q7	No change
⎍	H	H	L	L	Q_n-1	Q7	No change
⎍	H	H	H	H	Q_n-1	Q7	No change
⎎	H	H	H	No change	No change	No change	Q7

1. At the positive clock edge, information on the 7th shift register stage is transferred to the 8th register stage and the Q_S output.
2. Don't care
3. Open circuit

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Figure 3. Functional diagram

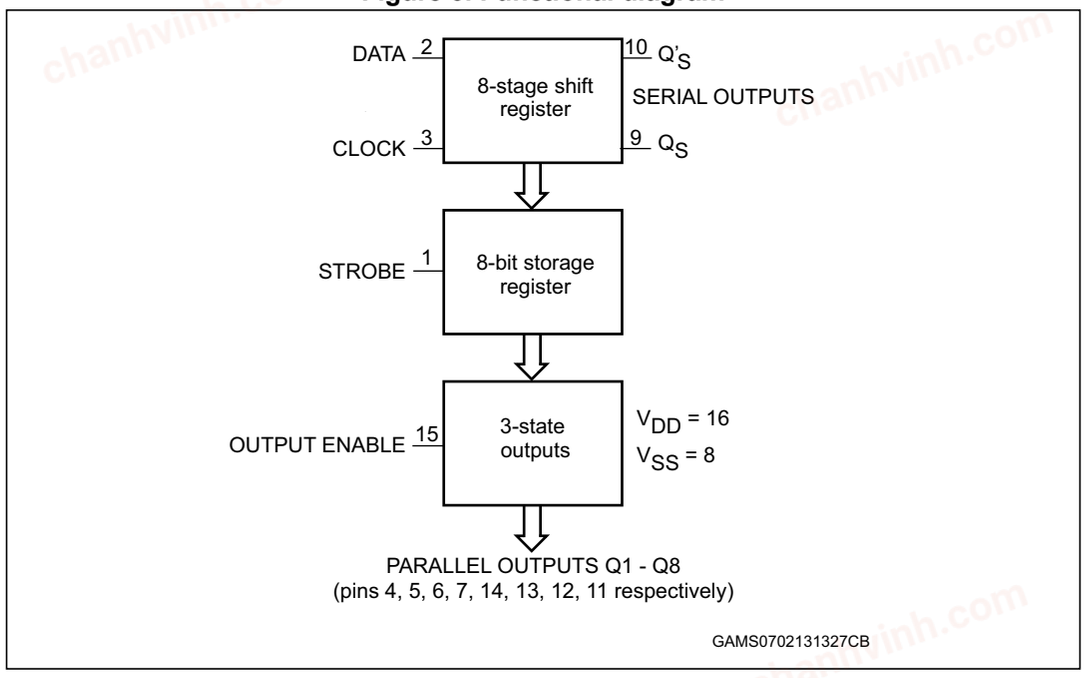

Figure 4. Input equivalent circuit

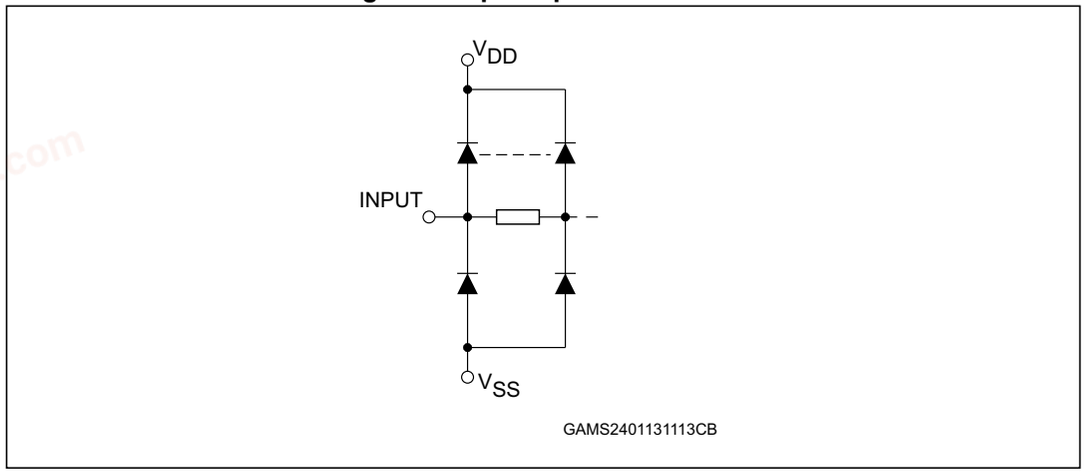

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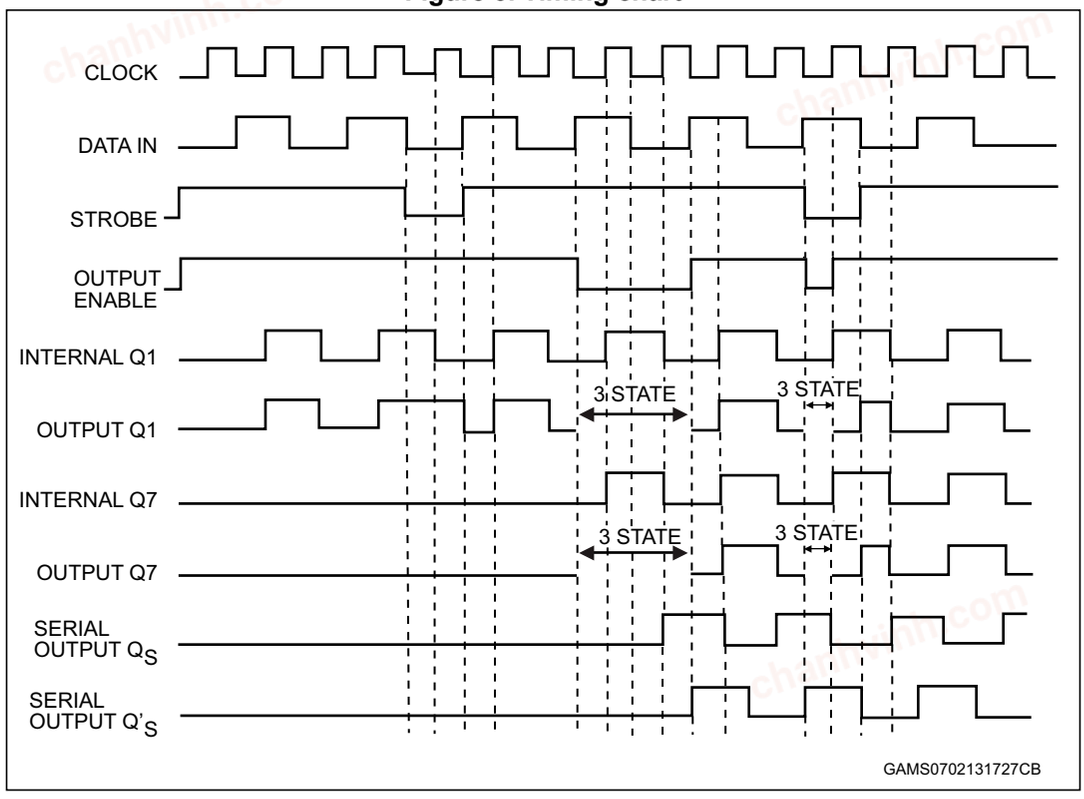
Figure 5. Timing chart



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3 Electrical characteristics

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to V_{SS} pin voltage.

Table 4. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to +22	V
V_I	DC input voltage	-0.5 to V_{DD} + 0.5	
I_I	DC input current	±10	mA
P_D	Power dissipation per package	500(1)	mW
	Power dissipation per output transistor	100	
T_{op}	Operating temperature	-55 to +125	°C
T_{stg}	Storage temperature	-65 to +150	

1. 500 mW at 65 °C; lower to 300 mW by 10 mW/°C from 65 °C to 85 °C.

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	3 to 20	V
V_I	Input voltage	0 to V_{DD}	
T_{op}	Operating temperature	-55 to 125	°C

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Table 6. DC specifications(1)

Sym.	Parameter	Test condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD}(V)	T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent current	0/5			5			5		150		150	µA
		0/10			10		0.04	10		300		300	
		0/15			15			20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High-level output voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10			10	9.95			9.95		9.95		
		0/15			15	14.95			14.95		14.95		
V_{OL}	Low-level output voltage	5/0		<1	5								
		10/0			10		0.05			0.05		0.05	
		15/0			15								
V_{IH}	High-level input voltage		0.5/4.5	<1	5	3.5			3.5		3.5		
			1/9		10	7			7		7		
			1.5/13.5		15	11			11		11		
V_{IL}	Low-level input voltage		4.5/0.5	<1	5			1.5		1.5		1.5	
			9/1		10			3		3		3	
			13.5/1.5		15			4		4		4	
I_{OH}	Output drive current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
			4.6			-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output sink current	0/5	0.4	<1	5	0.44	1		0.36		0.36		
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I_I	Input leakage current	0/18	Any input		18		$\pm10^{-5}$	±0.1		±1		±1	µA
I_{OH}, I_{OL}	3-state output leakage current	0/18			18		$\pm10^{-4}$	±0.4		±12		±12	
C_I	Input capacitance		Any input				5	7.5					pF

1. The noise margin for both level "1" and "0" is: 1 V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, and 2.5 V min. with V_{DD} = 15 V.

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Table 7. Dynamic electrical characteristics (T_{amb} = 25 °C, C_L = 50 pF, R_L = 200 kΩ, t_r = t_f = 20 ns)

Symbol	Parameter	Test condition	Value(1)			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time (clock to serial output Q_S)	5		300	600	ns
		10		125	250	
		15		95	190	
	Propagation delay time (clock to serial output Q'_S)	5		230	460	
		10		110	220	
		15		75	150	
	Propagation delay time (clock to parallel output)	5		420	840	
		10		195	390	
		15		135	270	
	Propagation delay time (strobe to parallel output)	5		290	580	
		10		145	290	
		15		100	200	
t_{PZL}, t_{PZH}	Propagation delay time (output enable to parallel out: output high to high impedance)	5		140	280	
		10		75	150	
		15		55	110	
	Propagation delay time (output enable to parallel out: output low to high impedance)	5		225	450	
		10		95	190	
		15		70	140	
t_w	Strobe pulse width	5	200	100		
		10	80	40		
		15	70	35		
	Clock pulse width	5	200	100		
		10	100	50		
		15	83	40		
t_s	Data setup time	5	125	60		
		10	55	30		
		15	35	20		
t_h	Minimum hold time	5	0	0	0	
		10				
		15				
t_{TLH}, t_{THL}	Transition time	5		100	200	
		10		50	100	
		15		45	80	

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Table 7. Dynamic electrical characteristics (T_{amb} = 25 °C, C_L = 50 pF, R_L = 200 kΩ, t_r = t_f = 20 ns) (continued)

Symbol	Parameter	Test condition	Value(1)			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_r, t_f	Clock input rise or fall time	5	15			µs
		10	5			
		15	5			
f_{max}	Maximum clock input frequency	5	1.25	2.5		MHz
		10	2.5	5		
		15	3	6		

1. The typical temperature coefficient for all V_{DD} values is 0.3 %/°C.

Figure 6. Typical application (remote control holding register)

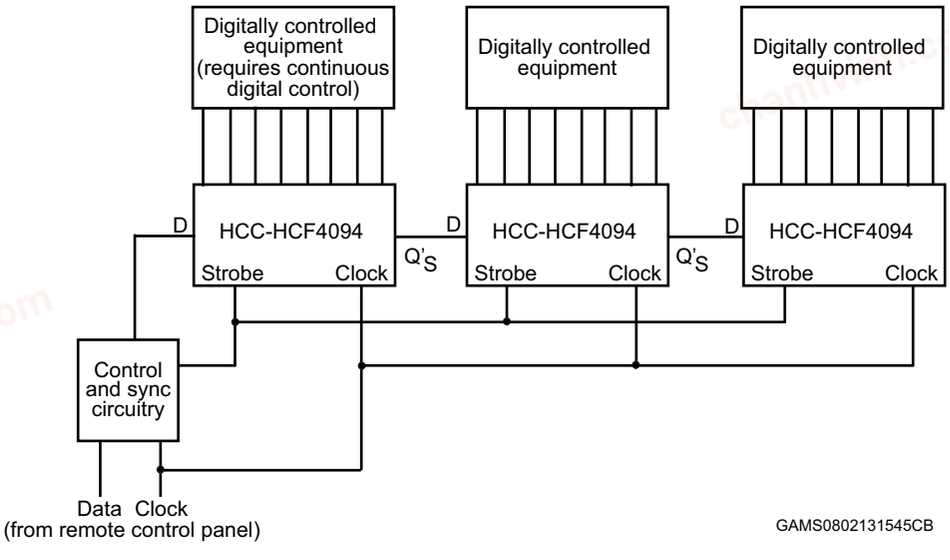

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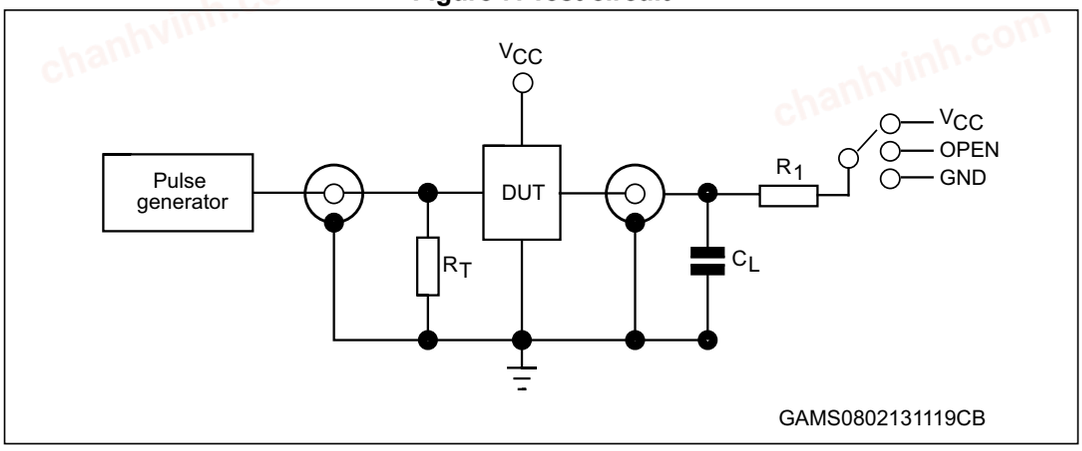
Figure 7. Test circuit



1. Legend: C_L = 50 pF or equivalent (includes jig and probe capacitance), R_L = 200 KΩ, R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Table 8. Propagation delay time configuration

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PZH}	V_{CC}
t_{PZH}, t_{PHZ}	GND

Figure 8. Waveform 1: Data in to Q_n timings (50 % clock duty cycle)

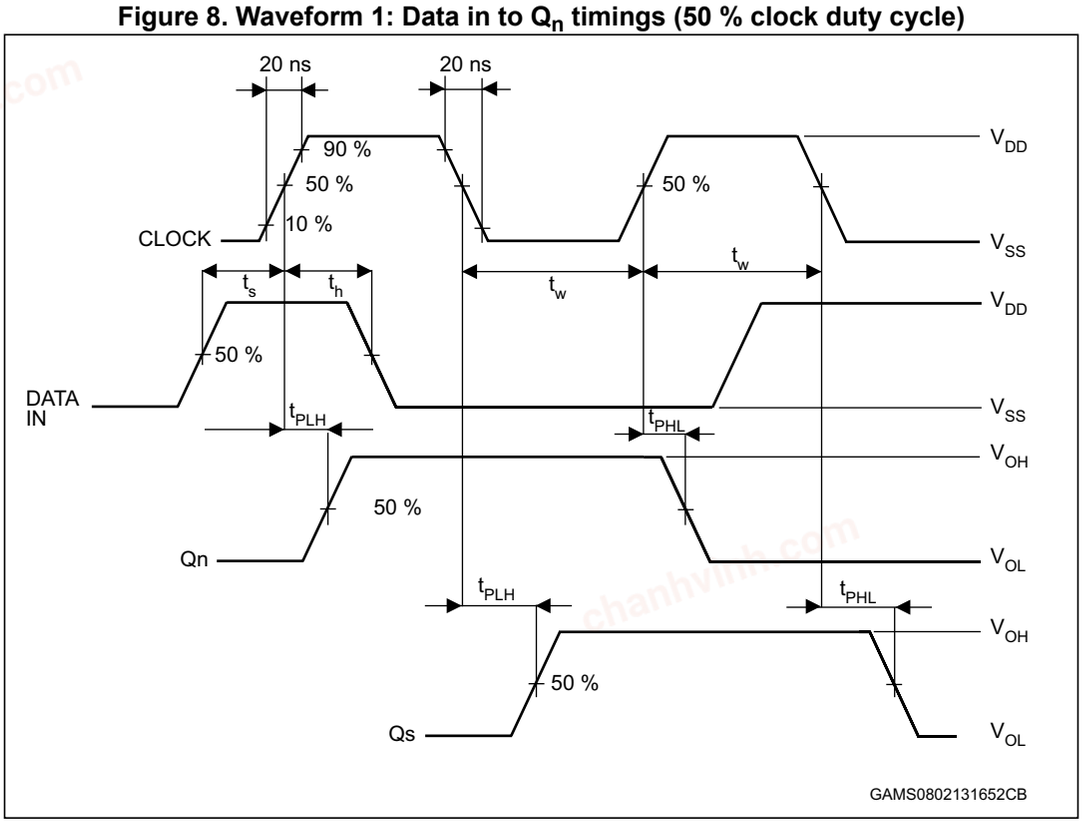


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Figure 9. Waveform 2: Setup and hold times (SI to CLOCK)
(f = 1 MHz; 50 % duty cycle)

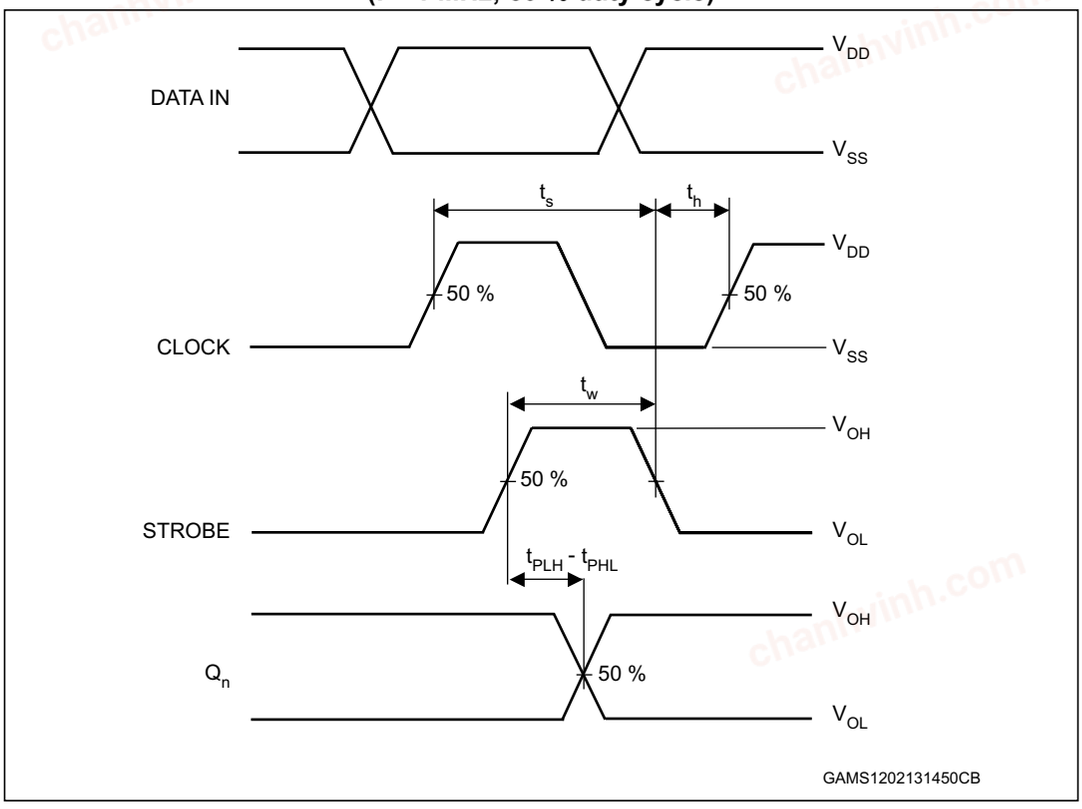
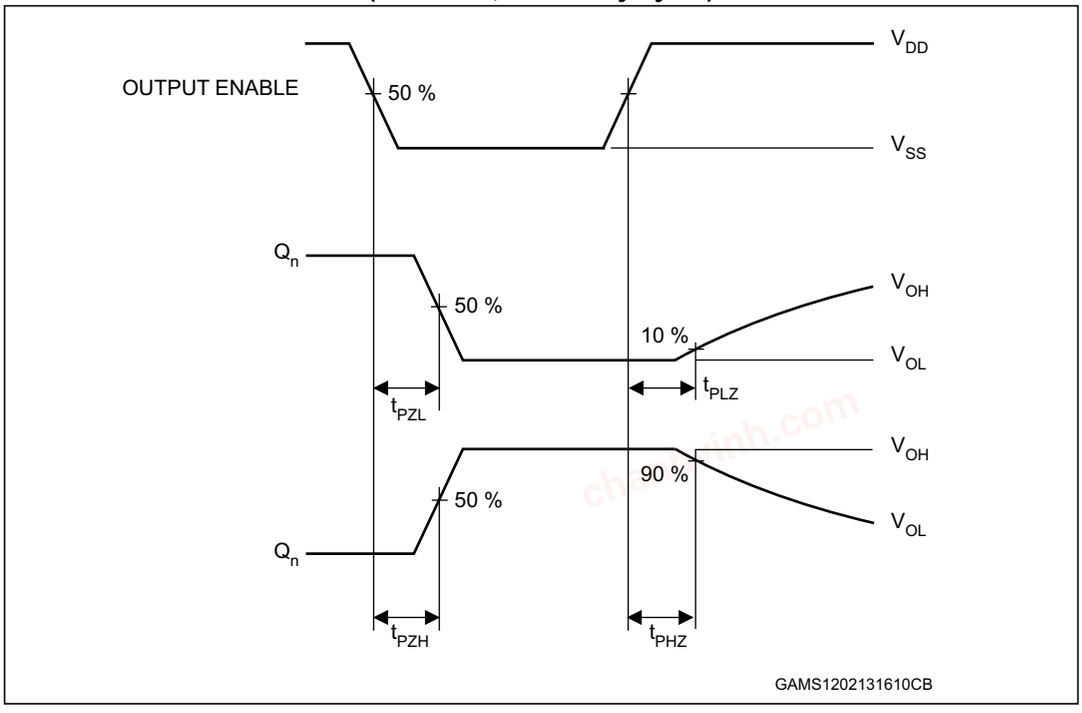


Figure 10. Waveform 3: Setup and hold time (PI to P/S)
(f = 1 MHz; 50 % duty cycle)



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

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Figure 11. SO-16 package mechanical drawing

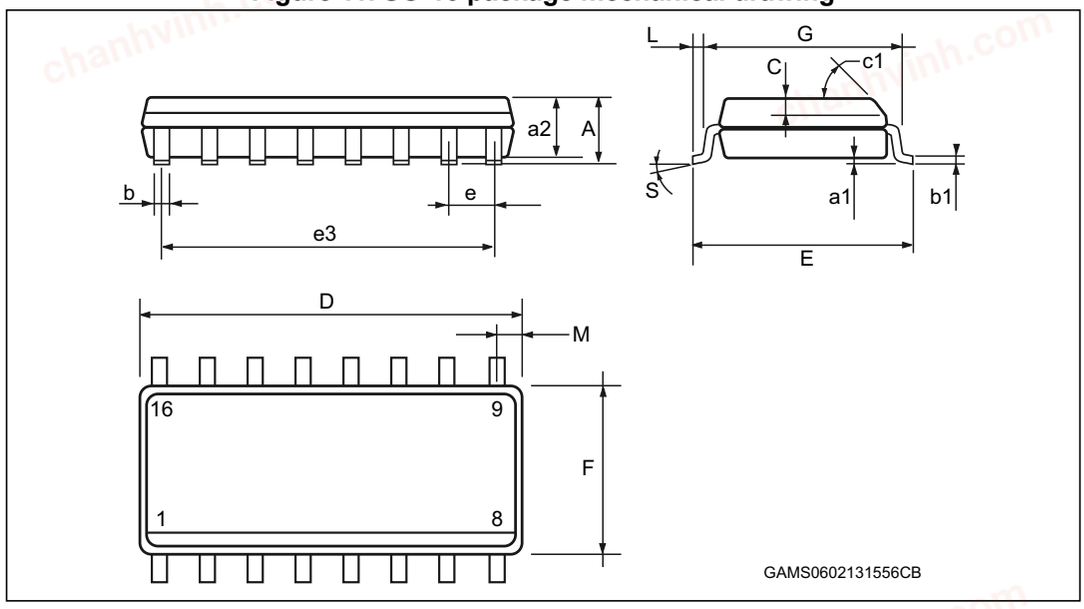

Table 9. SO-16 package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1		45 °			45 °	
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S			8 °			8 °

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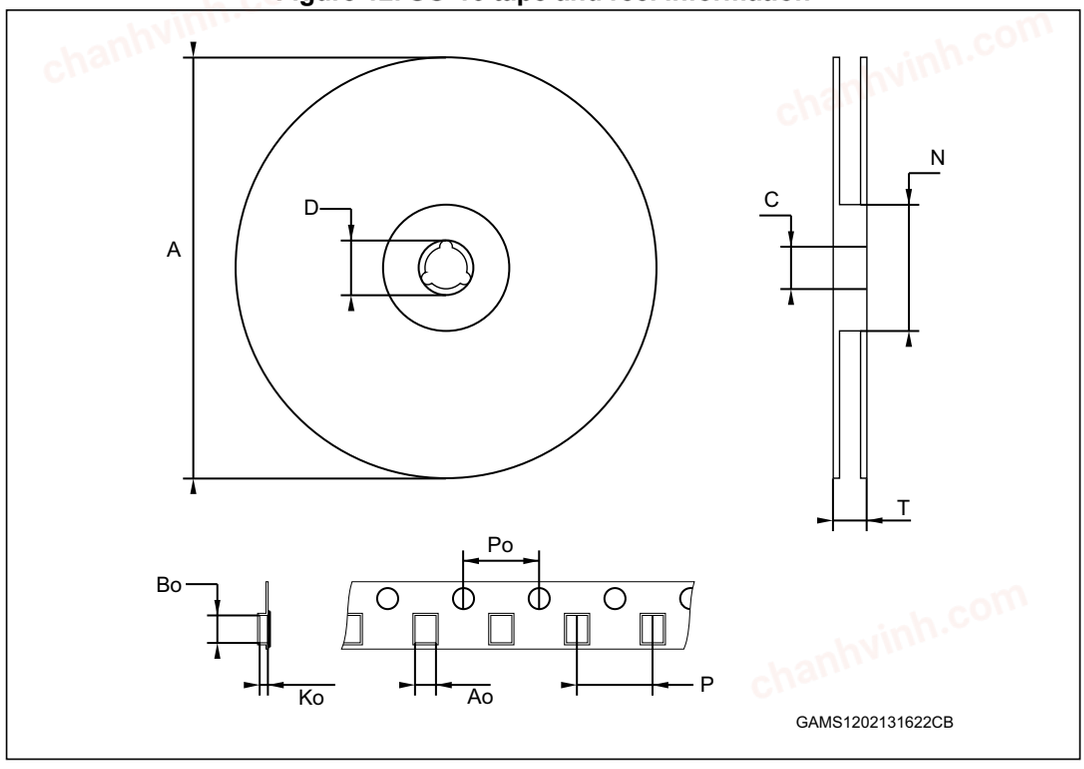
Figure 12. SO-16 tape and reel information



1. Drawing is not to scale.

Table 10. SO-16 tape and reel information

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

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5 Ordering information

Table 11. Order codes

Order code	Temperature range	Package	Packing	Marking
HCF4094M013TR	-55 ° C to +125 ° C	SO-16	Tape & reel	HCF4094
HCF4094YM013TR(1)	-40 ° C to +125 ° C	SO-16 (automotive grade)(1)		HCF4094Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent

6 Revision history

Table 12. Document revision history

Date	Revision	Changes
19-Feb-2013	4	Document template and layout updated Removed “B” from part number Updated package names (PDIP-16 and SO-16 instead of DIP-16 and SOP-16). Added *Applications* Added *Device summary table* Updated symbol names in *Table 7* Added *Section 5: Ordering information*
06-Jan-2014	5	Removed DIP package option Added ESD performance to *Features* Updated footnote *1* of *Table 1: Device summary table* Updated footnote *1* of *Table 11: Order codes*

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