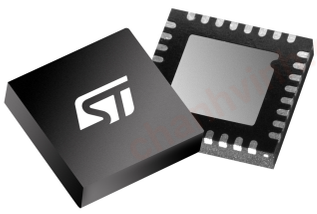
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# FDA803S

Data brief

## 1x10 W digital input class-D automotive audio amplifier with advanced diagnostics, wide voltage operating range for telematics and e-Call application



QFN32 (exposed pad down)

| Product status link |
|---|
| FDA803S |

| Product summary | | |
|---|---|---|
| **Order code** | **Package** | **Packing** |
| FDA803S-6DY | QFN32 (exp. pad down) | Tray |
| FDA803S-6DT | | Tape and reel |

## Features

- AEC-Q100 qualified
- Integrated 100 dB D/A conversion
- $I^2S$ and TDM digital input (up to 16CH TDM)
- Selectable input sample rate frequency (8/16/32/44.1/48/96 kHz)
- Wide supply operating range: 3.3 V - 18 V
- PWM frequency switching selectable by $I^2C$
  - 352.8 kHz, 384kHz, 411.6 kHz, 448 kHz
- 2 $I^2C$ addresses
- MOSFET power outputs
  - Typ 10 W 4 Ω at 14.4 V, 1 kHz THD = 1%
  - Typ 5 W 8 Ω at 14.4 V, 1 kHz THD = 1%
- Noise: 38 µV A-weighted: 20 kHz
- 8 Ω, 4 Ω driving capability
- Input amplitude limiter (configurable through $I^2C$)
- $I^2C$ full configurability and diagnostic
  - Startup diagnostic
  - Input voltage amplitude limiter function (configurable through $I^2C$)
  - 4 x Thermal warning
  - DC diagnostic
  - OCP protection scheme configurable
  - Mute time configuration
- Capability to run complete diagnostic in play
  - Configurable Clipping Detector
  - One of the Thermal Warnings
  - Over Current Protection
  - Open Load detection
  - High voltage mute
- 2 CD/Diag pin
- Integrated ESD and short circuit protection
- QFN32 wettable flanks
- Tested according to CISPR 25 - Class V (Fourth edition)

## Description

The FDA803S is the new ST single channel class-D audio amplifier, specifically designed for automotive applications. The FDA803S integrates a 24-bit, 100 dB DAC conversion and PWM class-D output stage with feedback before LC filter. This configuration enables the design of a compact and inexpensive application.

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The FDA803S supports $I^2S$ and TDM digital bit stream up to 16CH with several sampling frequencies from 8 kHz up to 96 kHz. FDA803S embeds a complete diagnostic in play to support the most demanding OEM requirements in terms of speaker control and system robustness/ reliability.

The FDA803S supports start stop cranking down to 3.3 V and it is available in a very compact and thin QFN 5x5 package. Thus the FDA803S is suitable for any level of automotive application especially e-Call and Telematics.

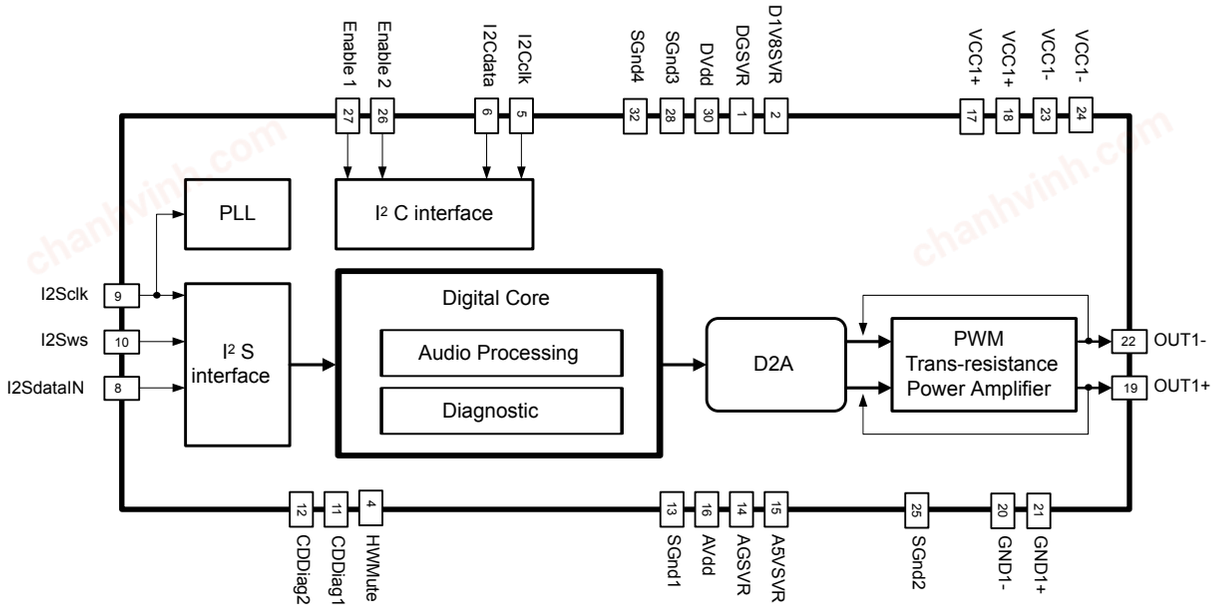
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# 1 Block diagram and pins description

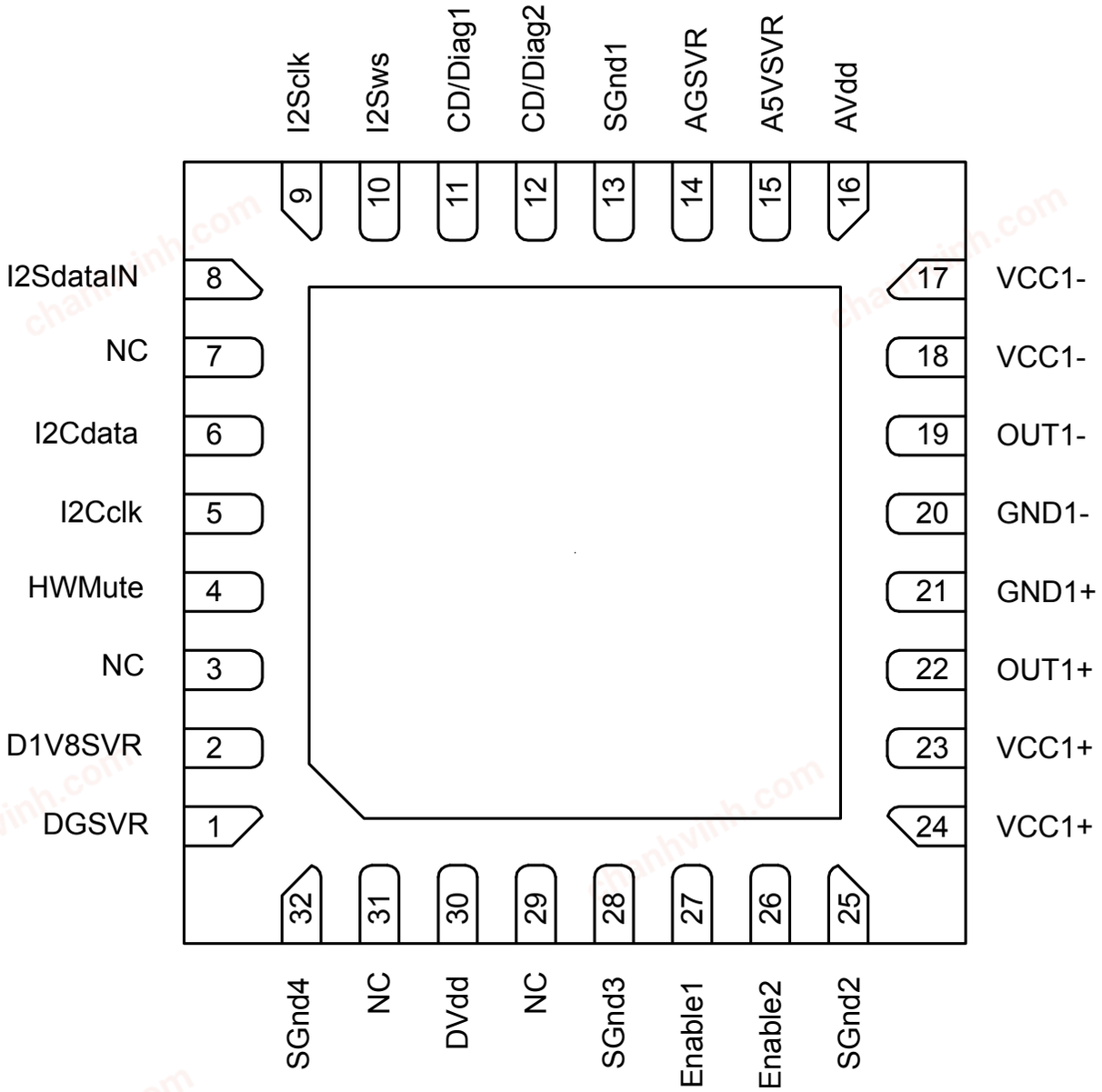
Figure 1. **Block diagram**



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Figure 2. **Pin connection diagram (bottom view)**



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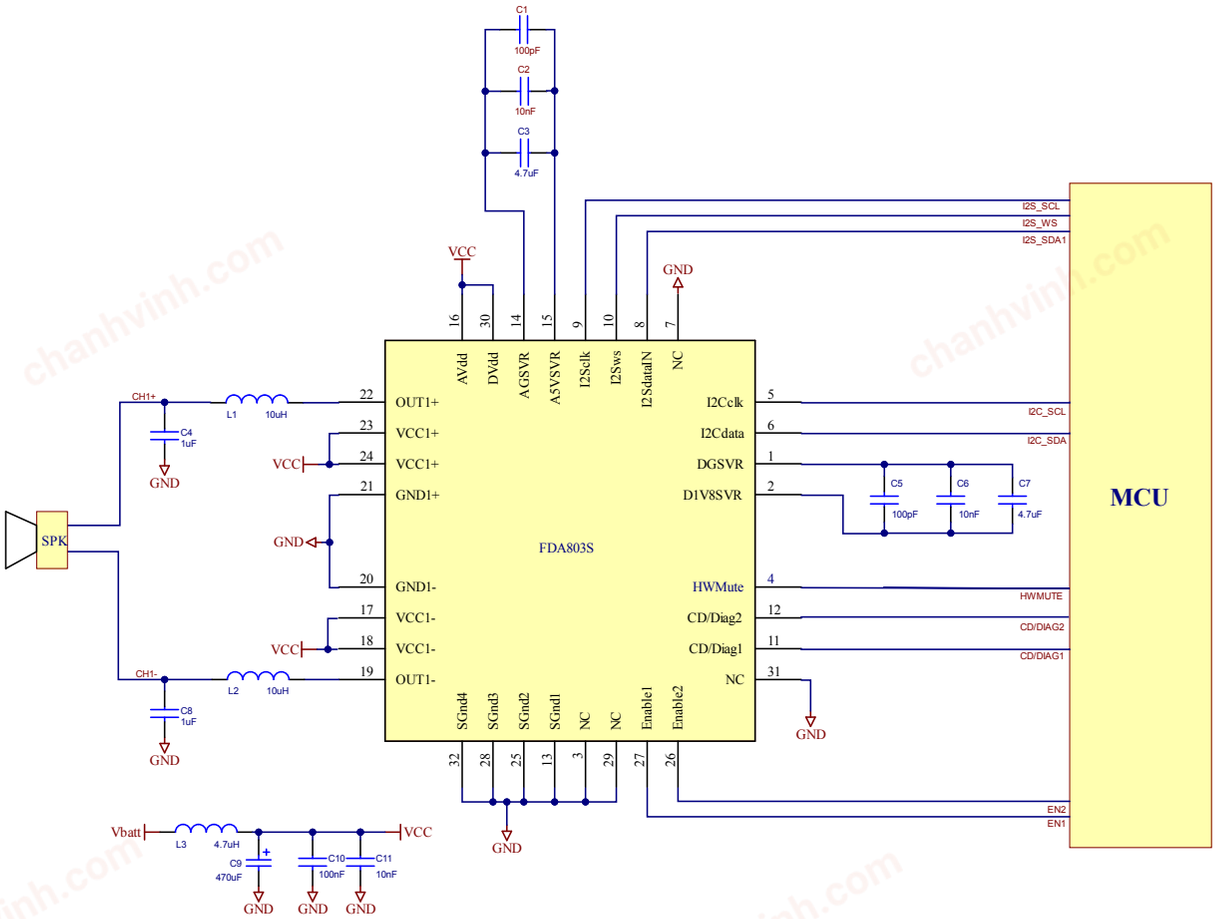
**Table 1. Pins description**

| N# | Pin | Function | Definition | Internal structure |
|---|---|---|---|---|
| 1 | DGSVR | Negative digital supply (Internally generated) | Internal Regulator | - |
| 2 | D1V8SVR | Positive digital supply (Internally generated) | Internal Regulator | - |
| 3 | NC | Connected to GND | - | - |
| 4 | HWMute | Hardware mute pin | Input | - |
| 5 | $I^2C$clk | $I^2C$ Clock | Input | - |
| 6 | $I^2C$data | $I^2C$ Data | Input/Output | Open-Drain |
| 7 | NC | Connected to GND | - | - |
| 8 | $I^2S$dataIN | $I^2S$/TDM Data | Input | - |
| 9 | $I^2S$clk | $I^2S$/TDM Clock | Input | - |
| 10 | $I^2S$ws | $I^2S$/TDM Sync | Input | - |
| 11 | CD/Diag1 | Clipping detector and diagnostic | Output | Open-Drain |
| 12 | CD/Diag2 | Clipping detector and diagnostic | Output | Open-Drain |
| 13 | SGnd1 | Ground of lower side of circuit, connected to GND | Supply | - |
| 14 | AGSVR | Negative digital supply (Internally generated) | Internal Regulator | - |
| 15 | A5VSVR | Positive digital supply (Internally generated) | Internal Regulator | - |
| 16 | AVdd | Analog supply | Supply | - |
| 17 | VCC1- | Channel 1, half bridge minus, Power Supply | Supply | - |
| 18 | VCC1- | Channel 1, half bridge minus, Power Supply | Supply | - |
| 19 | OUT1- | Channel 1, half bridge minus | Output | - |
| 20 | GND1- | Channel 1, half bridge minus, Power Ground | Supply | - |
| 21 | GND1+ | Channel 1, half bridge plus, Power Ground | Supply | - |
| 22 | OUT1+ | Channel 1, half bridge plus | Output | - |
| 23 | VCC1+ | Channel 1, half bridge plus, Power Supply | Supply | - |
| 24 | VCC1+ | Channel 1, half bridge plus, Power Supply | Supply | - |
| 25 | SGnd2 | Ground of upper side of circuit, connected to GND | Supply | - |
| 26 | Enable2 | Enable pin | Input | - |
| 27 | Enable1 | Enable pin | Input | - |
| 28 | SGnd3 | Ground of upper side of circuit, connected to GND | Supply | - |
| 29 | NC | Connected to GND | - | - |
| 30 | DVdd | Digital supply | Supply | - |
| 31 | NC | Connected to GND | - | - |
| 32 | SGnd4 | Ground of upper side of circuit, connected to GND | Supply | - |

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Figure 3. **Application diagram**



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# 2 Electrical specifications

## 2.1 Thermal data

**Table 2. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}a\text{-}2s2pv}$ | Thermal resistance junction-to-ambient (2s2p+vias) | 32.4 | °C/W |

*Note:*
- *2s2p is referred to a board with 2 layers dedicated to the signals and 2 layers dedicated to the power signals and supplies.*
- *from simulation according to Jedec best practice guidelines (JESD51-12) TAMB = 25 °C Infinite Heat Sink.*

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# 3 General information

The FDA803S is a fully digital single channel class-D audio amplifier with feedback before LC filter, designed for compact and low-cost Application, such as Telematics and eCall. The feedback before LC architecture has been chosen for allowing smaller components for the demodulator filter, saving cost and space occupation.

The $I^2S$ interface is used to provide the audio bit stream, with several sampling frequency from 8 kHz up to 96 kHz. The standard format is used for 4 channels applications, while the TDM allows to work up to 16 channels. The $I^2C$ interface is used to communicate and control the state of the power amplifier, perform the diagnostic and other features.

The FDA803S embeds an internal 24 bits DAC with 100 dB of resolution. Thanks to interpolation and noise shaping, the digital signal processing allows to reach up a good audio performance in a small device area. The internal PLL uses the clock frequency of the bit stream to generate the internal clock for the digital part and PWM for the outputs.

The innovative self-diagnostic algorithm, available also in play, allows the automatic detection of wrong load connections or variation of the load and provides this information through the $I^2C$ bus to an external microcontroller.

The communication to the microcontroller is improved by two dedicated CD/Diag. All the useful information, such as thermal warnings, input and output offset detection, and some more can be selected by the $I^2C$ setting and addressed to the one of the CD/Diag pins. Furthermore, one of these pins could be used to synchronize other devices on the platform for better EMC management.

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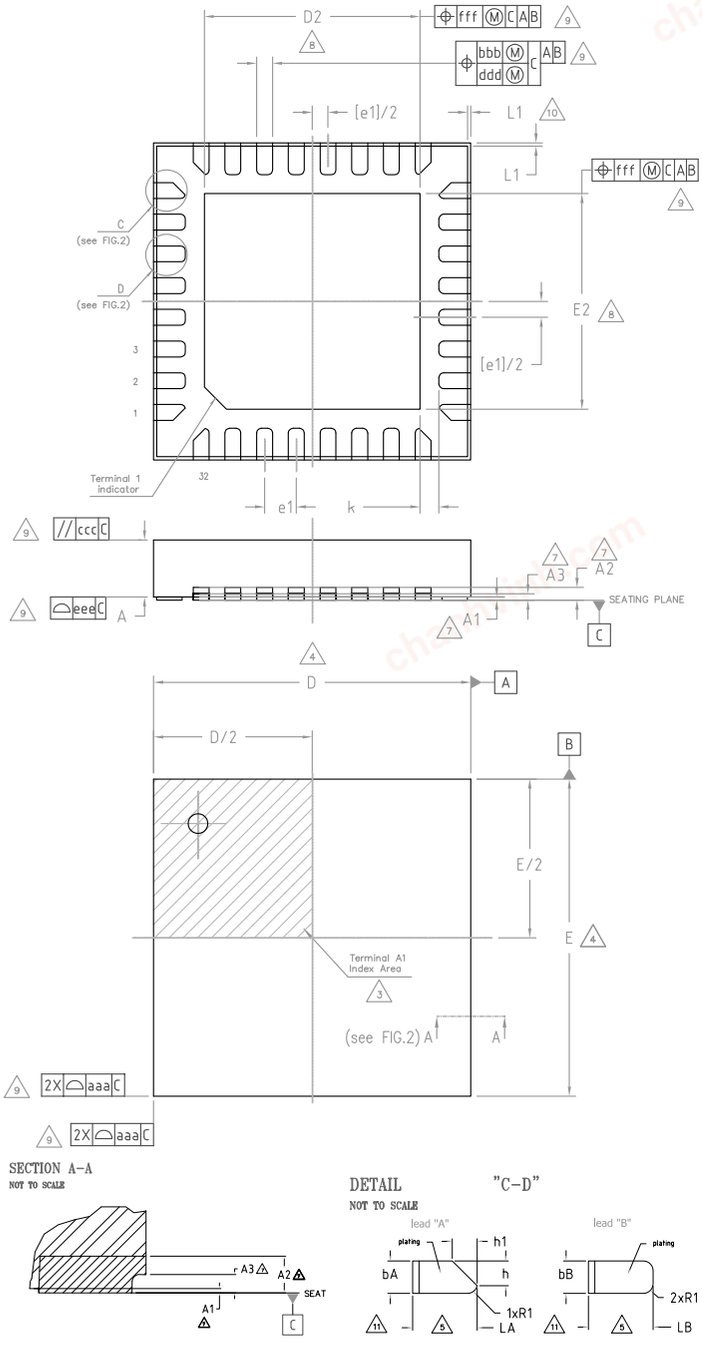


# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 4.1 QFN32 5x5x1 (3.5x3.5 32L exp. pad down) package information

**Figure 4. QFN 5X5 EP 3.5x3.5 32L WITH WETTABLE FLANKS package outline**



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Table 3. **QFN 5X5 EP 3.5x3.5 32L WITH WETTABLE FLANKS mechanical data**

| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0 | - | 0.05 |
| A2 | - | 0.2 REF | - |
| A3 | 0.10 | - | - |
| D | | 5.00 BSC | |
| D2 | 3.40 | 3.50 | 3.60 |
| E | | 5.00 BSC | |
| E2 | 3.40 | 3.50 | 3.60 |
| e1 | | 0.50 BSC | |
| k | 0.20 | - | - |
| L1 | - | - | 0.05 |
| La | 0.40 | 0.50 | 0.60 |
| bA | 0.20 | 0.25 | 0.30 |
| h | - | 0.19 REF | - |
| h1 | - | 0.19 REF | - |
| LB | 0.45 | 0.50 | 0.55 |
| bB | 0.20 | 0.25 | 0.30 |
| N | | 32 | |
| R1 | - | - | 0.10 |
| Tolerance of form and position | | | |
| aaa | - | 0.15 | - |
| bbb | - | 0.10 | - |
| ccc | - | 0.10 | - |
| ddd | - | 0.05 | - |
| eee | - | 0.08 | - |
| fff | - | 0.10 | - |

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## Revision history

Table 4. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 07-Mar-2022 | 1 | Initial release. |
| 29-Jun-2022 | 2 | Updated *Section Features*. |
| 09-Jan-2023 | 3 | Updated Section Device summary.<br>Minor text changes in Section Features. |

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