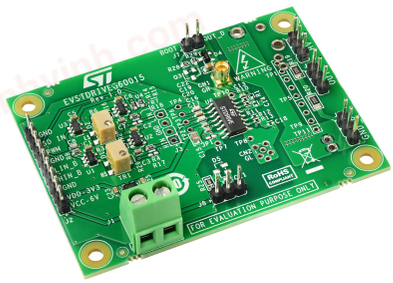
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EVSTDRIVEG60015

Data brief

Demonstration board for STDRIVEG600 600 V high speed half-bridge gate driver with SGT120R65AL e-mode GaN HEMT



Features

- Half-Bridge topology featuring 600 V STDRIVEG600 gate driver
- Equipped with 75 mΩ typ, 650 V e-mode GaN HEMT
- GaN in 5x6 mm PowerFLAT HV package with Kelvin source
- HV bus up to 500 V
- 4.75 to 6.5 V VCC gate driver supply voltage, limited by GaN V_{GS} rating
- On-board adjustable deadtime generator to convert single PWM signal in independent High-Side and Low-Side deadtimes
- Separated inputs with external deadtime can also be used
- On-board 3.3 V regulator for external circuitry supply
- 25° C/W junction-to-ambient thermal resistance to evaluate large power topologies
- High frequency connector for GaN gate monitoring
- Optional low-side shunt
- RoHS compliant.

Product status link
EVSTDRIVEG60015

Description

The STDRIVEG600 is a high-speed half-bridge gate driver optimized to drive high-voltage enhanced mode GaN HEMTs. It features an integrated bootstrap diode and allows supplying external switches up to 20 V, with undervoltage protection tailored for GaN HEMTs.

The EVSTDRIVEG60015 board is easy to use and quick and adapt for evaluating the characteristics of STDRIVEG600 driving the SGT120R65AL 75 mΩ typ., 650 V E-Mode GaN switches.

It provides an on-board programmable dead time generator and a 3.3 V linear voltage regulator to supply external logic controllers like microcontrollers.

Spare footprints are also included to allow customizing the board for the final application, such as separate LIN and HIN input signals or single PWM signal, use of optional external bootstrap diode, separate supply for VCC, PVCC or BOOT and the use of low-side shunt resistor for peak current mode topologies.

The EVSTDRIVEG60015 is 50 x 70 mm wide, FR-4 PCB resulting in 25 °C/W $R_{th(J-A)}$ in still air.

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1 Safety and operating instructions



1.1 General terms

Warning:

During assembly, testing, and operation, the evaluation board poses several inherent hazards, including bare wires, moving or rotating parts and hot surfaces

Danger: *There is danger of serious personal injury, property damage or death due to electrical shock and burn hazards if the kit or components are improperly used or installed incorrectly.*

The kit is not electrically isolated from the high-voltage supply DC input. No insulation is ensured between the accessible parts and the high voltage. All measuring equipment must use adequately insulated probes, clamps and connecting wires. Never touch the evaluation board while it is energized as it is capable of causing electrical shock hazard.

All operations involving transportation, installation and use, and maintenance must be performed by skilled technical personnel able to understand and implement national accident prevention regulations. For the purposes of these basic safety instructions, “skilled technical personnel” are suitably qualified people who are familiar with the installation, use and maintenance of power electronic systems.

1.2 Intended use of demonstration board

The board is designed for demonstration purposes only, and must not be used for electrical installations or machinery. Technical data and information concerning the power supply conditions are detailed in the documentation and should be strictly observed.

1.3 Installing the demonstration board

- The installation and cooling of the demonstration board must be in accordance with the specifications and target application.
- The board must be protected against excessive strain. In particular, components should not be bent or isolating distances altered during transportation or handling.
- No contact must be made with other electronic components and contacts.
- The board contains electrostatically-sensitive components that are prone to damage if used incorrectly. Do not mechanically damage or destroy the electrical components (potential health risks).

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1.4 Operating the demonstration board

To operate properly the board, follow these safety rules.

1. Work Area Safety:
   - The work area must be clean and tidy.
   - Do not work alone when boards are energized.
   - Protect against inadvertent access to the area where the board is energized using suitable barriers and signs.
   - A system architecture that supplies power to the evaluation board must be equipped with additional control and protective devices in accordance with the applicable safety requirements (i.e., compliance with technical equipment and accident prevention rules).
   - Use non-conductive and stable work surface.
   - Use adequately insulated clamps and wires to attach measurement probes and instruments.
2. Electrical Safety:
   - Remove power supply from the board and electrical loads before performing any electrical measurement.
   - Proceed with the arrangement of measurement setup, wiring or configuration paying attention to high voltage sections.
   - Once the setup is complete, energize the board.

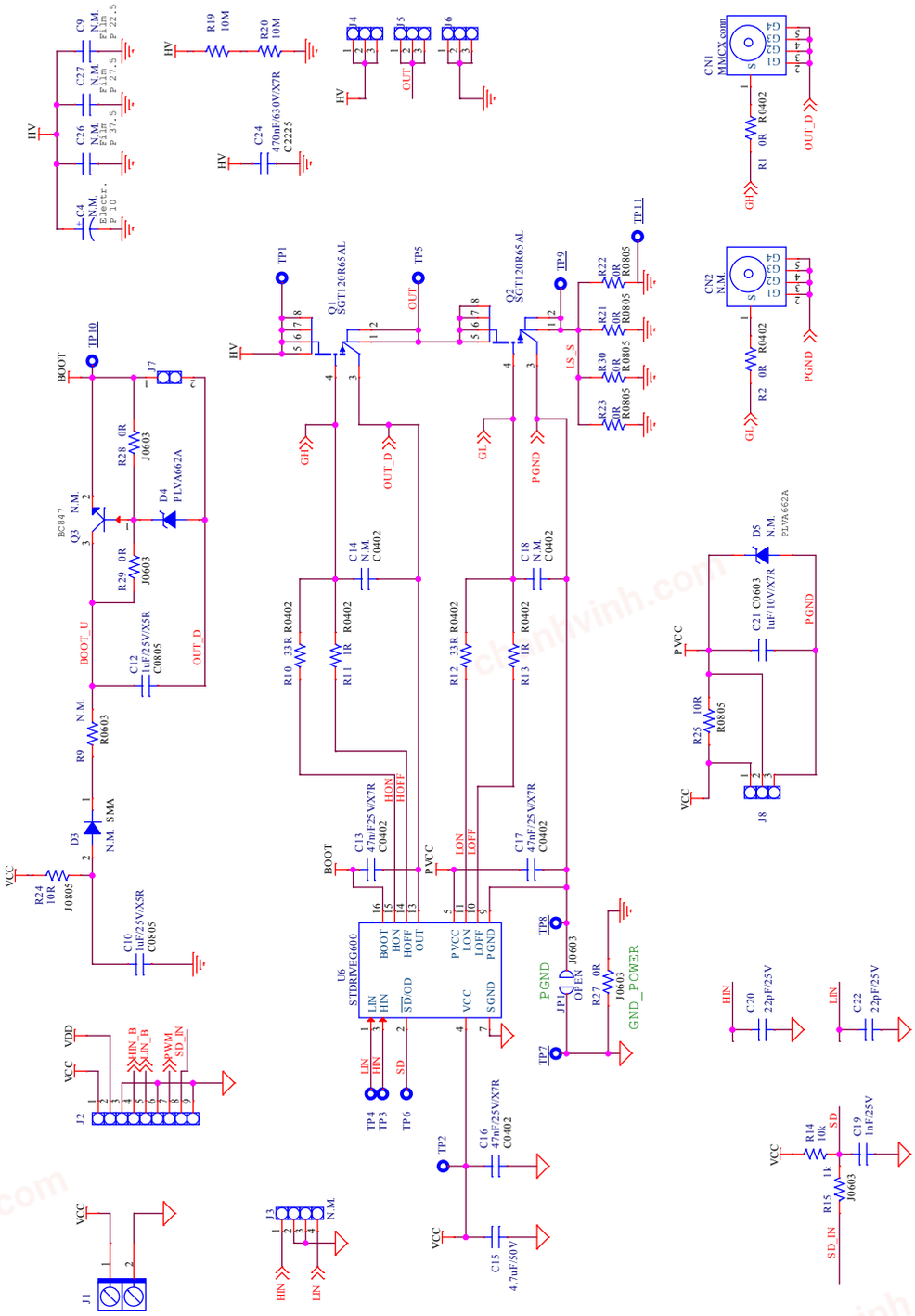
Danger: *Do not touch the board when it is energized or immediately after it has been disconnected from the voltage supply as several parts and power terminals containing potentially energized capacitors need time to discharge.*
Do not touch the boards after disconnection from the voltage supply as several parts, included PCB, may still be very hot.
The kit is not electrically isolated from DC input.

3. Personal Safety
   - Always wear suitable personal protective equipment such as, for example, insulating gloves and safety glasses.
   - Take adequate precautions and install the board in such a way to prevent accidental touch. Use protective shields such as, for example, insulating box with interlocks if necessary.

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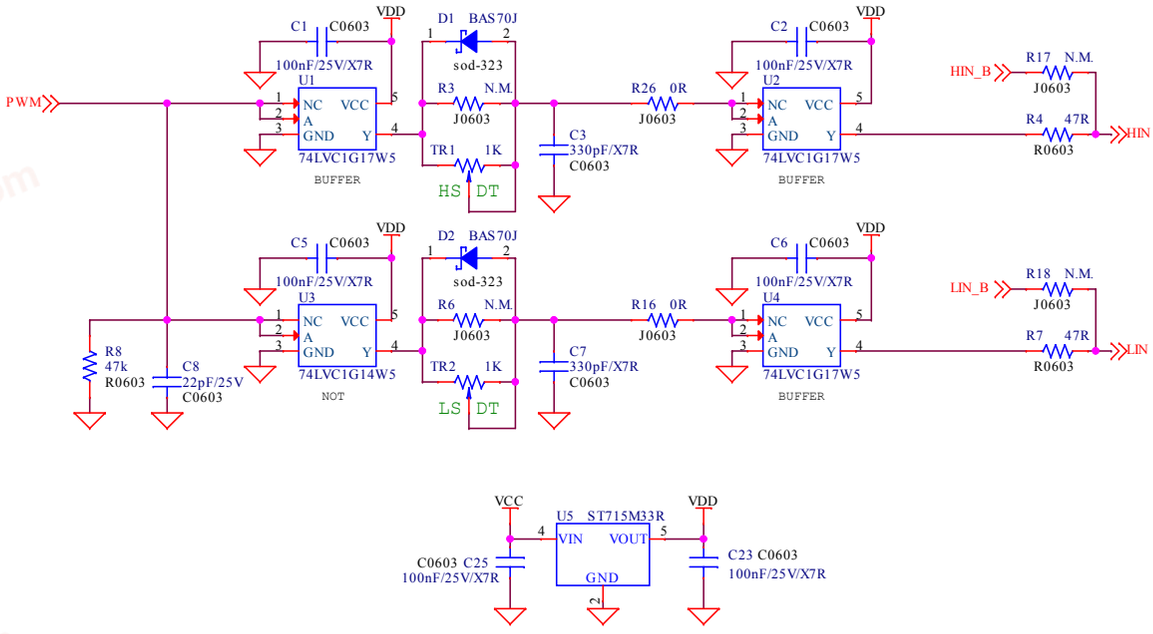
2 Schematic diagrams

Figure 1. EVSTDRIVEG60015 schematic - STDRIVEG600 gate driver and SGT120R65AL e-mode GaN power stage



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Figure 2. **EVSTDRIVEG60015 schematic - Deadtime generator and connectors**

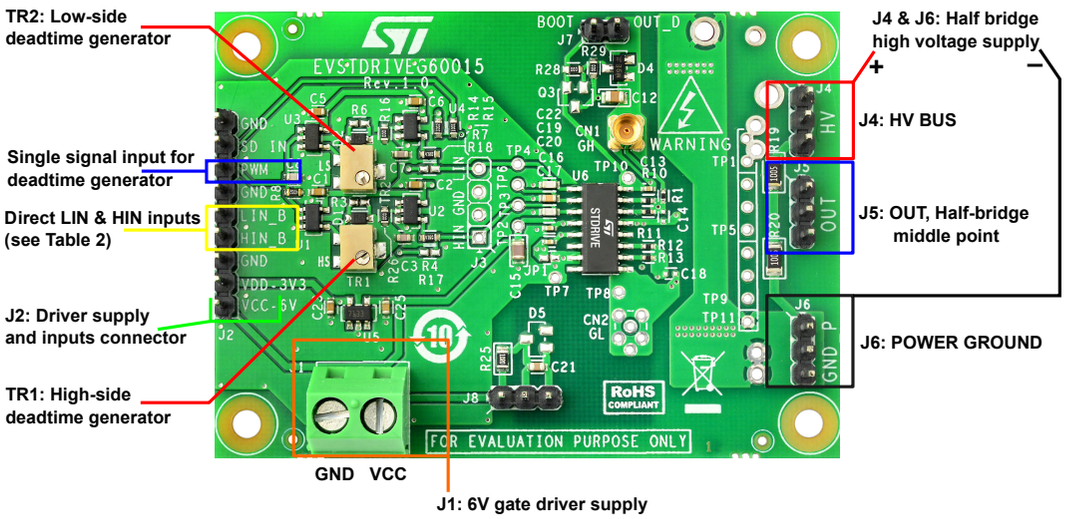


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3 Board power-up and input connection

The following picture shows how to supply the EVSTDRIVEG60015, how to provide LIN and HIN inputs and set the programmable deadtime generator.

Figure 3. EVSTDRIVEG60015 - Supply and signal connection



The LIN, HIN inputs can be provided form the on-board deadtime generator or directly from an external generator or control device (as DSP/MCU).

The deadtime value set by the on-board dead time generator, fed by PWM input signal on J2, can be tuned by setting TR1 and TR2. The typical dead time value with the trimmer in the default manufacturing middle position is about 100 ns. It is possible to change dead time generator range by changing C3 and C7.

TR2 sets the deadtime before low side turn-on.

TR1 sets the deadtime before high side turn-on.

Table 1. Connector Map

Ref	Pin #	Name	Function	Description
J2	1	VCC	INPUT power	Board Supply voltage (recommended value 6 V)
	2	VDD (3V3)	OUT power	Output voltage of on-board 3.3 V regulator: it can be used to supply external circuitry (up to about 50 mA)
	3	GND	PWR	Board reference potential
	4	HIN_B	INPUT digital	HIN direct input signal (0 to 3.3 V or up to 20 V): mount R17 and remove R4 - see Table 2 and Table 3
	5	LIN_B	INPUT digital	LIN direct input signal (0 to 3.3 V or up to 20 V): mount R18 and remove R7 - see Table 2 and Table 3
	6	GND	PWR	Board reference potential
	7	PWM	INPUT digital	PWM input signal (0 to 3.3 V or 5 V) – see Table 2 and Table 3
	8	SD_IN	INPUT / OUT digital	Disable input signal (0 to 3.3 V or up to 20 V) – see Table 3 Open-drain output signals over-temperature protection
	9	GND	PWR	Board reference potential
J4	1,2,3	HV	INPUT Power	These three pins are connected to high voltage (HV) of GaN power stage. Connect the half bridge high voltage positive supply.
J5	1,2,3	OUT	OUTPUT Power	These three pins are connected to OUT pin of power stage: connect the load to this terminal

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Ref	Pin #	Name	Function	Description
J6	1,2,3	GND_POWER	PWR	These three pins are connected to power ground. Connect the half bridge high voltage negative supply.
J12	1	VCC	INPUT Power	Board driver supply voltage (recommended value 6 V)
	2	GND	POWER	Board reference potential
CN1		GH	OUTPUT	To be used to monitor the gate of high-side GaN power transistor (GH) with high bandwidth, high voltage differential probes (optically isolated probes with MMCX connector are strongly recommended)
CN2		GL	OUTPUT	To be used to monitor the gate of low-side GaN power transistor (GL). Recommended to be used with high bandwidth differential probes (optically isolated) with proper MMCX male connector.

Table 2. Device input selection

R4, R7	R17, R18	Input source	Function and description
0-47 Ω (closed)	Open	J2: PWM pin	LIN & HIN are generated by the on-board deadtime generator from a single PWM signal on J2, pin 7.
Open	0-47 Ω (closed)	J2: LIN_B & HIN_B pins	Direct connection to LIN and HIN STDRIVEG600 pins. LIN, HIN input range: up to 20 V.

Table 3. Input signal truth table

$\overline{SD}$/OD	PWM	LIN	HIN	Low side	High side
L	X	X	X	Off	Off
H	L	H	L	On	Off
H	H	L	H	Off	On(1)

1. *If $V_{BO} > V_{BOthON}$*

The recommended power-on sequence is to turn VCC on first, then apply the HV bus voltage. The recommended power-off sequence is to turn-off the HV bus supply first, then VCC.

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4 Bill of materials

Table 4. **EVSTDRIVEG60015 bill of materials**

Reference	Description	Value or Generic Part Number Package
CN1	MMCX Straight Receptacle	Cinch 135-3701-201 or equivalent
CN2	MMCX Straight Receptacle	N.M.
C1, C2, C5, C6, C23, C25	SMT ceramic capacitor	100 nF / 25 V / X7R, 0603
C3, C7	SMT ceramic capacitor	330 pF / X7R, 0603
C4	THT Electrolytic Capacitor, diam 22 mm, pitch 10mm	N.M.
C9	Polypropylene Film Capacitor, pitch 22.5 mm	N.M
C8, C20, C22	SMT ceramic capacitor	22 pF / 25 V, 0603
C10, C12	SMT ceramic capacitor	1 µF / 25 V / X5R, 0805
C13, C16, C17	SMT ceramic capacitor	47 nF / 25 V / X7R, 0402
C14, C18	SMT ceramic capacitor	N.M., 0402
C15	SMT ceramic capacitor	4.7 µF / 25 V / X7R, 0805
C19	SMT ceramic capacitor	1 nF / 25 V, 0603
C21	SMT ceramic capacitor	1 µF / 10 V / X7R, 0603
C24	SMT ceramic capacitor	470 nF / 630 V / X7R, 2225
C26	Polypropylene Film Capacitor, pitch 37.5 mm	N.M.
C27	Polypropylene Film Capacitor, pitch 27.5 mm	N.M
D1, D2	Low capacitance, low series inductance and resistance Schottky diodes	BAS70JFILM, SOD-323
D3	Fast Rectifier	N.M., SMA
D4	6.2 V Low-voltage avalanche regulator diodes	PLVA662A, SOT23
D5	6.2 V Low-voltage avalanche regulator diodes	N.M., SOT23
JP1, JP2	SMT jumper	OPEN, Soldering pads
J1	Terminal block T.H. 2 pos, 5.08 mm	2 Poles, Pitch 5.08 mm
J2	Strip connector 9 pos, 2.54 mm	STRIP 1x9
J3	Strip connector 4 pos, 2.54 mm	N.M.
J4, J5, J6, J8	Strip connector 3 pos, 2.54 mm	STRIP 1x3
J7	Strip connector 2 pos, 2.54 mm	STRIP 1x2
Q1, Q2	Bottom-side cooled 650 V E-mode GaN transistor	SGT120R65AL, PowerFLAT 5x6 mm HV
Q3	NPN General Purposes Transistor	N.M., SOT23
R1, R2	SMT resistor	0 Ω, 0402
R3, R6, R17, R18	SMT resistor	N.M., 0603
R4, R7	SMT resistor	47 Ω, 0603
R8	SMT resistor	47 kΩ, 0603
R9	SMT resistor	N.M., 0603
R10, R12	SMT resistor	50 Ω, 0402
R11, R13	SMT resistor	1 Ω, 0402
R14	SMT resistor	10 kΩ, 0603
R15	SMT resistor	1 kΩ, 0603

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Reference	Description	Value or Generic Part Number Package
R16, R26, R27, R28, R29	SMT resistor	0 Ω, 0603
R19, R20	SMT resistor	10 MΩ, 1206
R21, R22, R23, R30	SMT resistor	0 Ω, 0805
R24	SMT resistor	10 Ω, 0603
R25	SMT resistor	10 Ω, 0805
TR1, TR2	5 mm Square Surface Mount Miniature Trimmers Multi-Turn Cermet Sealed	1 kΩ, TSM4YJ
TP1, TP2, TP3, TP4, TP5, TP6, TP8, TP9, TP10, TP11	Test point for probe	Metallized Hole, 0.8 mm diameter
U1, U2, U4	Single Schmitt-trigger buffer	74LVC1G17W5, SOT23-5L
U3	Single Schmitt-trigger inverter	74LVC1G14W5, SOT23-5L
U5	High input voltage, 85 mA LDO linear regulator	ST715M33R, SOT23-5L
U6	High voltage and high-speed half-bridge gate driver	STDRIVEG600, SO16

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5 Layout and component placements

Figure 4. **EVSTDRIVEG60015 - Layout (component placement top view)**

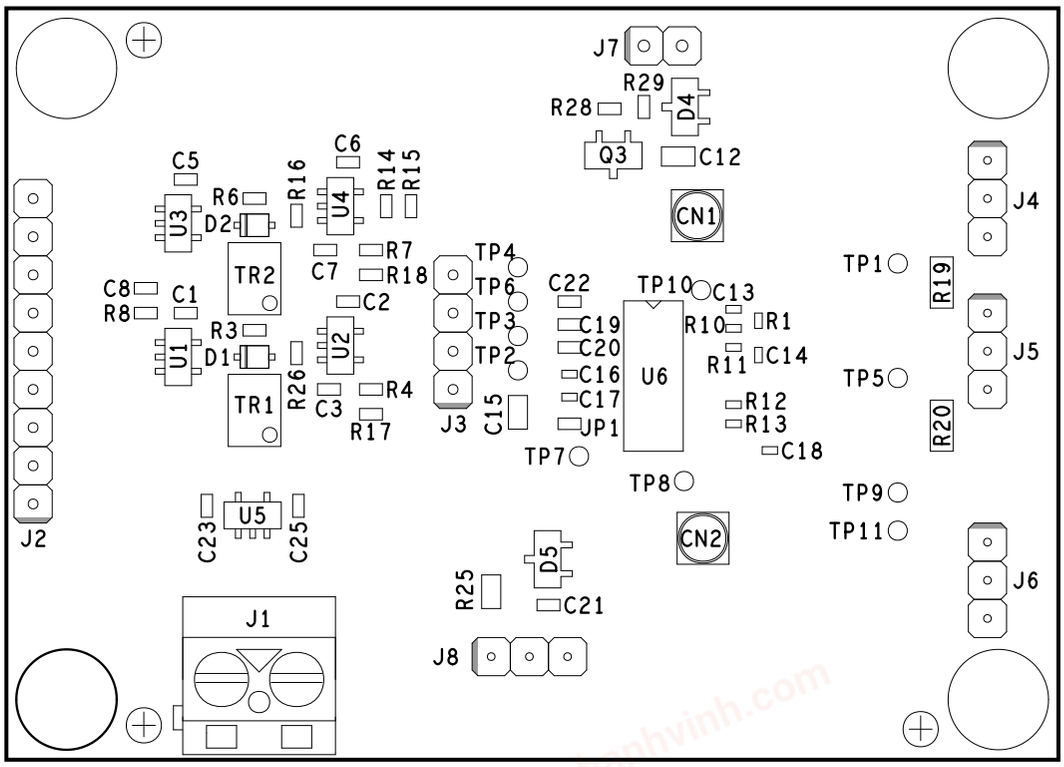
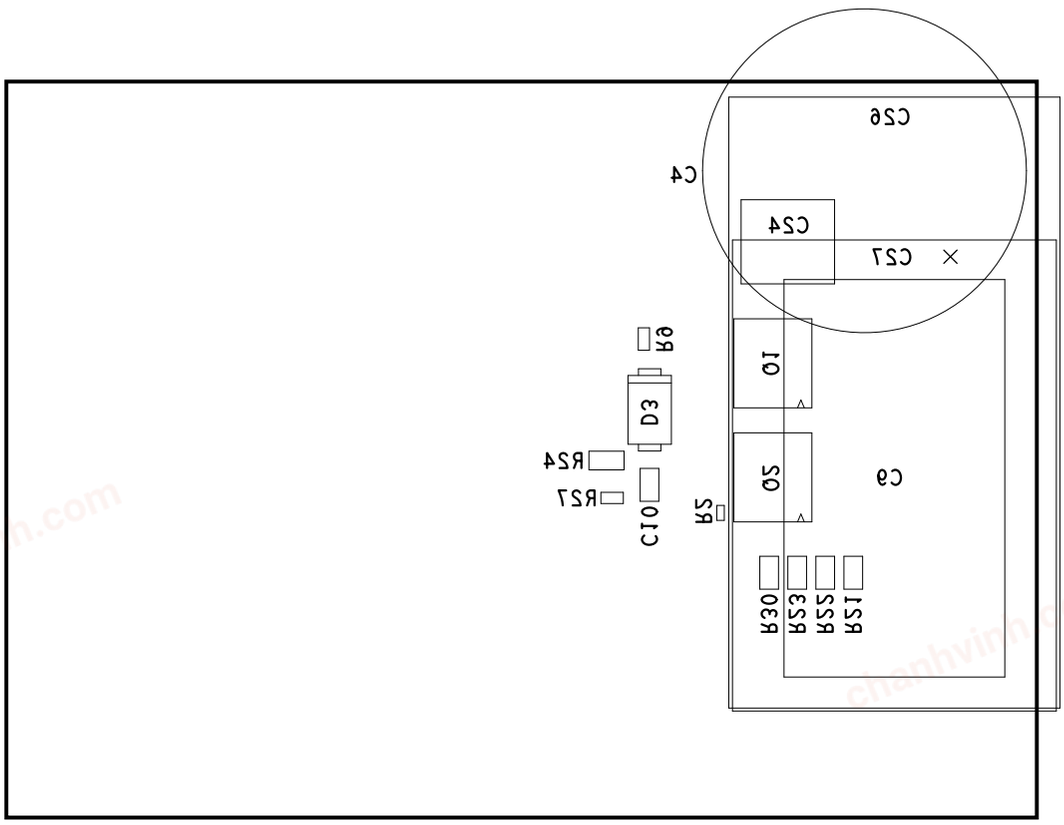


Figure 5. **EVSTDRIVEG60015 - Layout (component placement bottom view)**



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Figure 6. **EVSTDRIVEG60015 - Layout (top layer)**

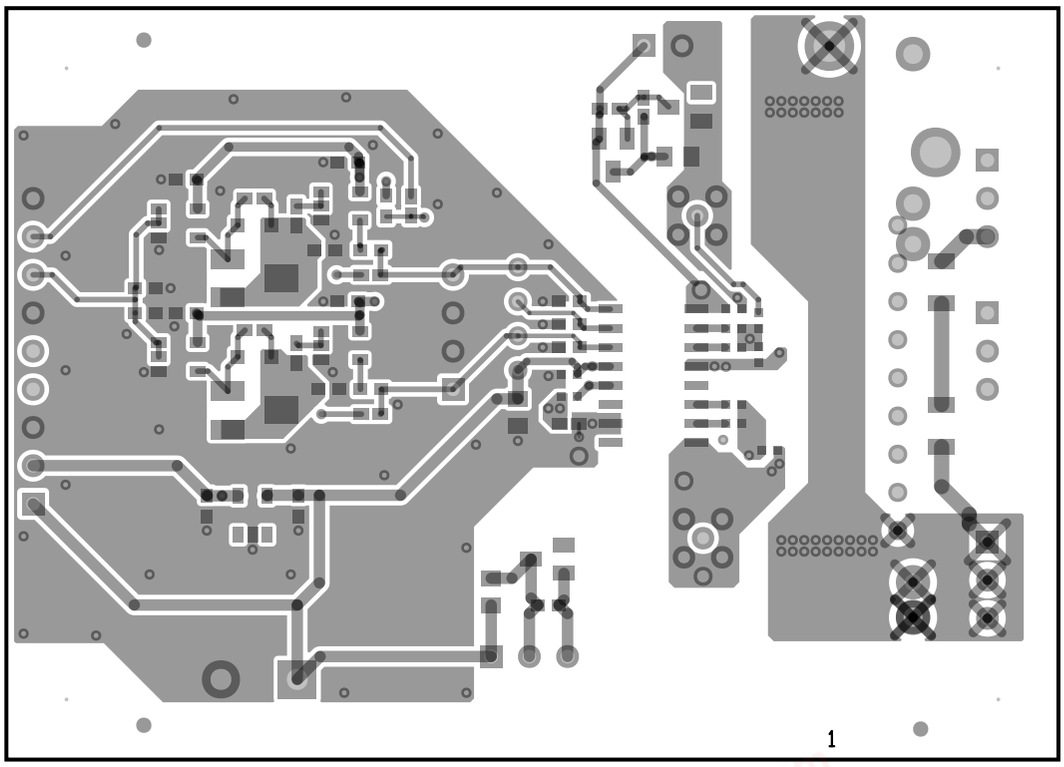
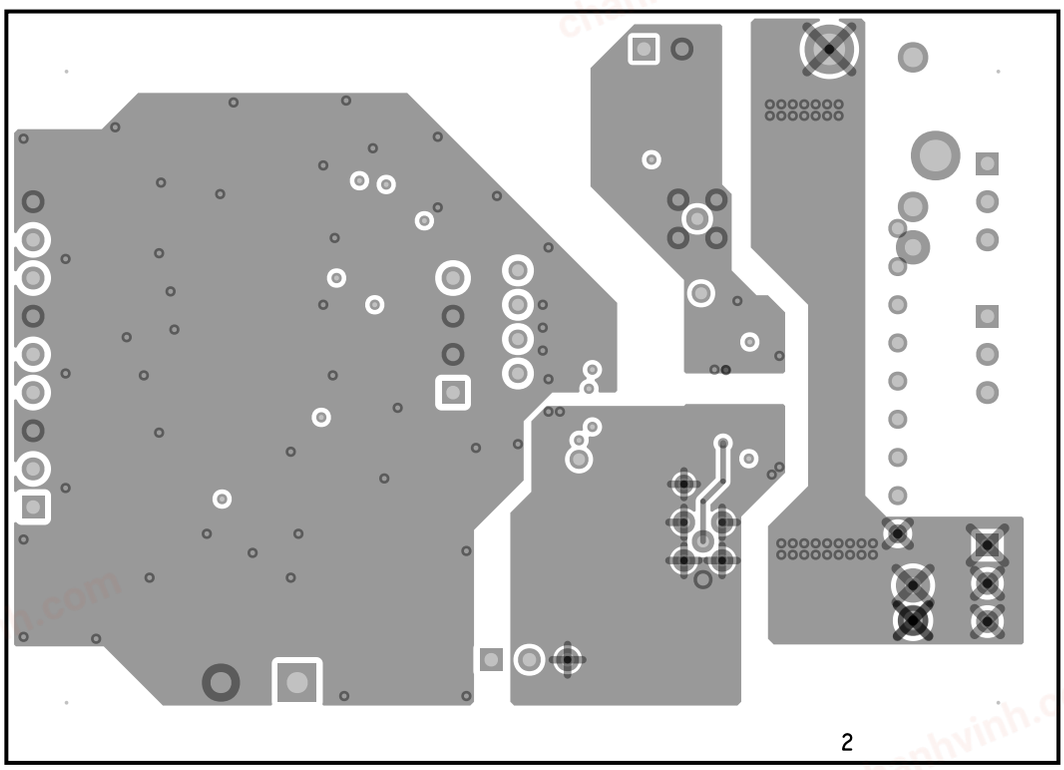


Figure 7. **EVSTDRIVEG60015 - Layout (inner 2 layer)**



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Figure 8. **EVSTDRIVEG60015 - Layout (inner 3 layer)**

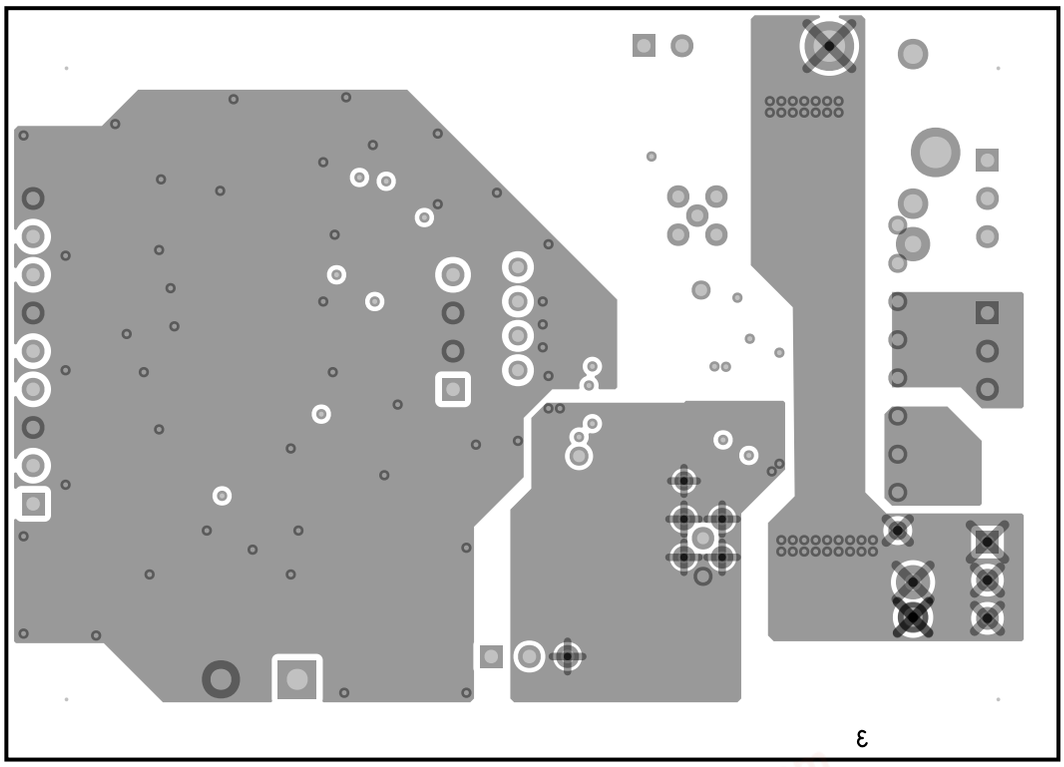
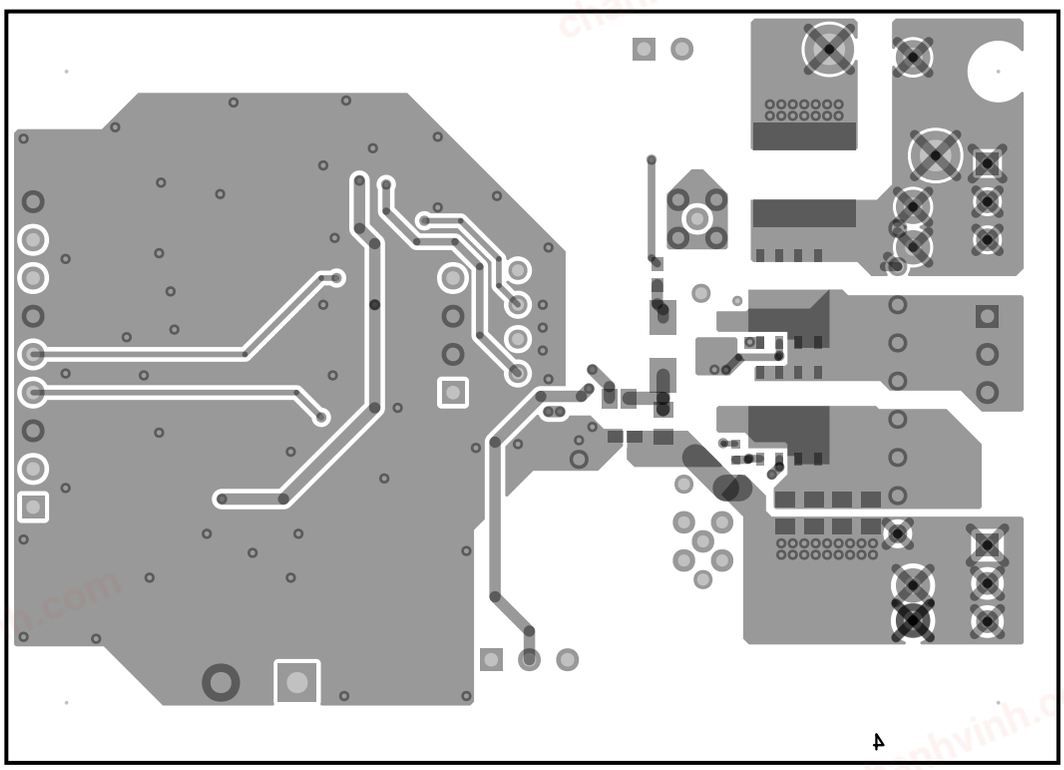


Figure 9. **EVSTDRIVEG60015 - Layout (bottom layer)**



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Revision history

Table 5. **Document revision history**

Date	Version	Changes
18-Apr-2023	1	Initial release.

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