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EVAL6472PD

Fully integrated stepper motor driver mounting the L6472 in a high power PowerSO package

Data brief



EVAL6472PD

Description

The EVAL6472PD demonstration board is a fully integrated microstepping motor driver. In combination with the STEVAL-PCC009V2 communication board and the SPIN evaluation software, the board allows the user to investigate all the features of the L6472 device. In particular, the board can be used to regulate the L6472 parameters in order to fit application requirements.

The 4-layer layout and the PowerSo package allow the top thermal performance to be obtained.

The EVAL6472PD supports the daisy chain configuration making it suitable for the evaluation of the L6472 in the multi motor applications.

Features

- Voltage range from 8 V to 45 V
- Phase current up to 3 $A_{r.m.s.}$
- Dual SPI connector (with daisy chain configuration suitable)
- SW input
- FLAG and BUSY LED indicators
- High thermal performance ($R_{thj\text{-}a}$12 °C/W typical)
- Suitable for use in combination with the STEVAL-PCC009V2

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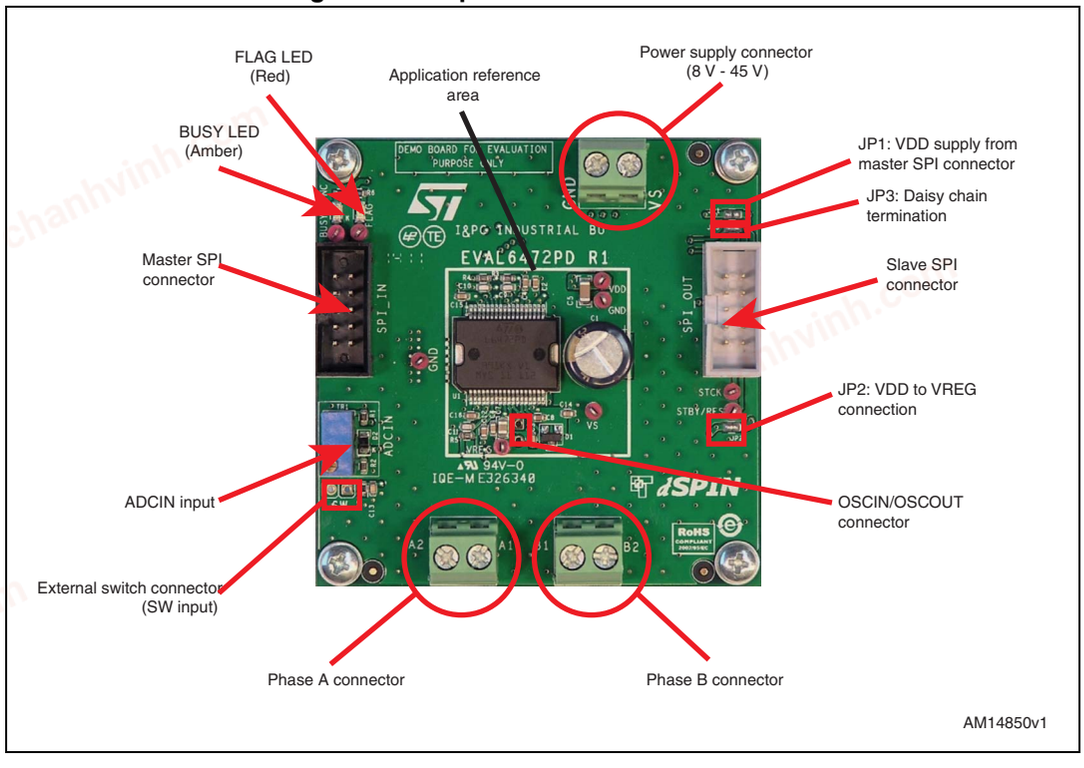
Board description

Table 1. EVAL6472PD specifications

Parameter	Value
Supply voltage (VS)	8 to 45 V
Maximum output current (each phase)	3 $A_{r.m.s.}$
Logic supply voltage (VREG)	Externally supplied: 3.3 V Internally supplied: 3 V typical
Logic interface voltage (VDD)	Externally supplied: 3.3 V or 5 V Internally supplied: VREG
Low level logic input voltage	0 V
High level logic input voltage	VDD(1)
Operating temperature	-25 to +125 °C
L6472PD thermal resistance junction to ambient	12 °C/W typical

1. All logic inputs are 5 V tolerant.

Figure 1. Jumper and connector location



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Table 2. Jumper and connector description

Name	Type	Function
M1	Power supply	Motor supply voltage
M2	Power output	Bridge A outputs
M3	Power output	Bridge B outputs
CN1	SPI connector	Master SPI
CN2	SPI connector	Slave SPI
CN3	NM connector	OSCIN and OSCOUT pins
CN4	NM connector	External switch input
TP1 (VS)	Test point	Motor supply voltage test point
TP2 (VDD)	Test point	Logic interface supply voltage test point
TP3 (VREG)	Test point	Logic supply voltage/L6472 internal regulator test point
TP5 (GND)	Test point	Ground test point
TP6 (GND)	Test point	Ground test point
TP8 (STCK)	Test point	Step-clock input test point
TP9 (STBY/RES)	Test point	Standby/reset input test point
TP10 (FLAG)	Test point	FLAG output test point
TP11 (BUSY/SYNC)	Test point	BUSY/SYNC output test point

Table 3. Master SPI connector pinout (J10)

Pin number	Type	Description
1	Open drain output	L6472 BUSY output
2	Open drain output	L6472 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI “Master In Slave Out” signal (connected to L6472 SDO output through daisy chain termination jumper JP2)
6	Digital input	SPI serial clock signal (connected to L6472 CK input)
7	Digital input	SPI “Master Out Slave In” signal (connected to L6472 SDI input)
8	Digital input	SPI slave select signal (connected to L6472 CS input)
9	Digital input	L6472 step-clock input
10	Digital input	L6472 standby/reset input

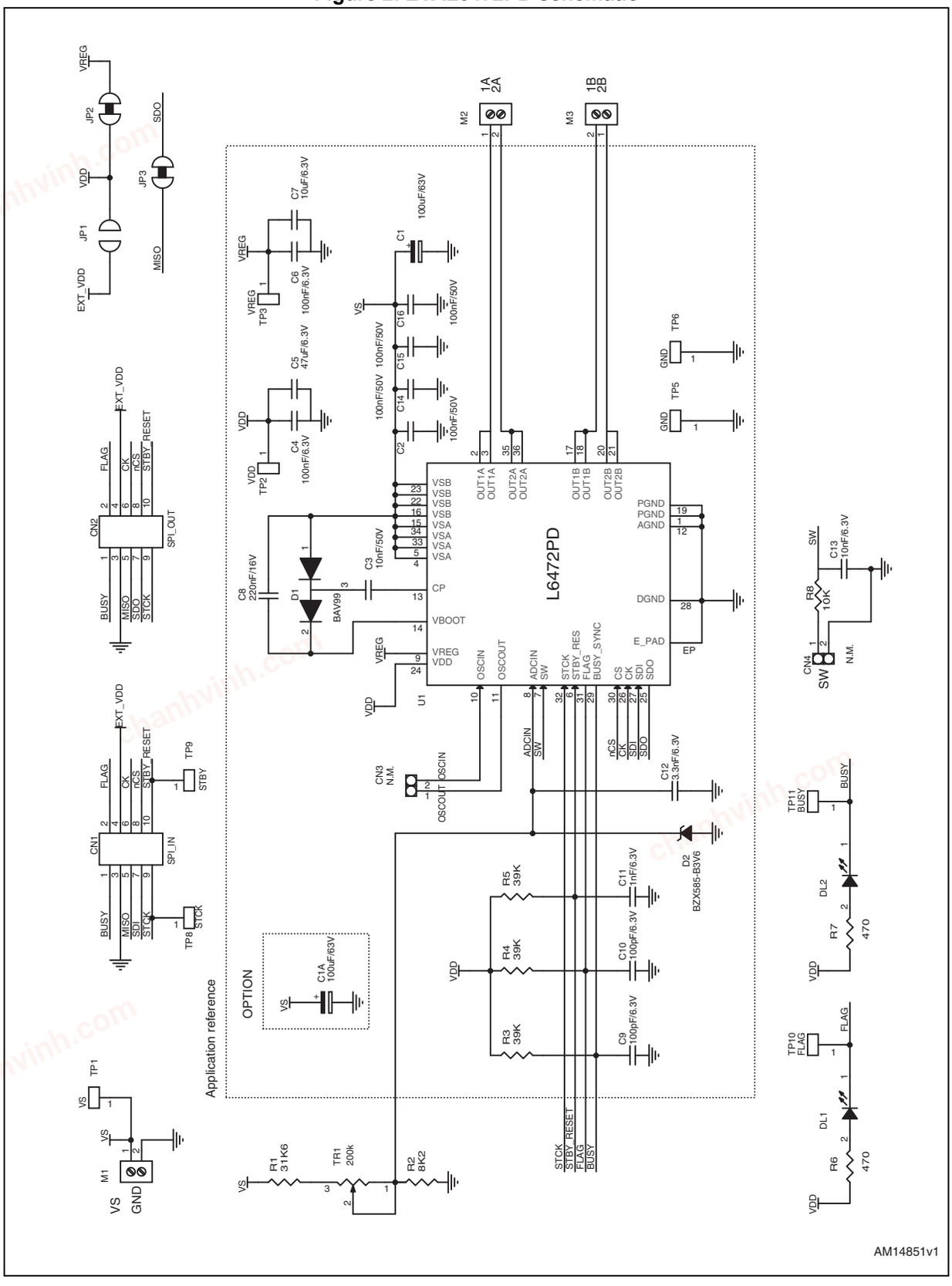
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Table 4. Slave SPI connector pinout (J11)

Pin number	Type	Description
1	Open drain output	L6472 BUSY output
2	Open drain output	L6472 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI “Master In Slave Out” signal (connected to pin 5 of J10)
6	Digital input	SPI serial clock signal (connected to L6472 CK input)
7	Digital input	SPI “Master Out Slave In” signal (connected to L6472 SDO output)
8	Digital input	SPI slave select signal (connected to L6472 CS input)
9	Digital input	L6472 step-clock input
10	Digital input	L6472 standby/reset input

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Figure 2. EVAL6472PD schematic



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Table 5. Bill of material

Index	Quantity	Reference	Value	Package
1	1	CN1	Pol. IDC male header vertical 10 poles (black)	CON-FLAT-5X2-180M
2	1	CN2	Pol. IDC male header vertical 10 poles (gray)	CON-FLAT-5X2-180M
3	2	CN3, CN4	N.M	STRIP254P-M-2
4	1	C1A	100 µF/63 V	CAPE-R10HXX-P5
5	1	C1	100 µF/63 V	CAPES-R10HXX
6	4	C2, C14, C15, C16	100 nF/50 V	CAPC-0603
7	1	C3	10 nF/50 V	CAPC-0603
8	2	C4, C6	100 nF/6.3 V	CAPC-0603
9	1	C5	47 µF/6.3 V	CAPC-1206
10	1	C7	10 µF/6.3 V	CAPC-0805
11	1	C8	220 nF/16 V	CAPC-0603
12	2	C9, C10	100 pF/6.3 V	CAPC-0603
13	1	C11	1 nF/6.3 V	CAPC-0603
14	1	C12	3.3 nF/6.3 V	CAPC-0603
15	1	C13	10 nF/6.3 V	CAPC-0603
16	1	JP1	LED red	LEDC-0805
17	1	DL2	LED amber	LEDC-0805
18	1	D1	BAV99	SOT23
19	1	D2	BZX585-B3V6	SOD523
20	1	JP1	Jumper OPEN	JP2SO
21	2	JP2, JP3	Jumper CLOSED	JP2SO
22	3	M1, M2, M3	Screw connector 2 poles	MORSV-508-2P
23	1	R1	31.6 kΩ	RESC-0603
24	1	R2	8.2 kΩ	RESC-0603
25	3	R3, R4, R5	39 kΩ	RESC-0603
26	2	R6, R7	470 Ω	RESC-0603
27	1	R8	10 kΩ	RESC-0603
28	7	TP1, TP2, TP3, TP8, TP9, TP10, TP11	TPTH-ring-1 mm (red)	TPTH-RING-1 MM
29	2	TP5, TP6	TPTH-ring-1 mm (black)	TPTH-RING-1 MM
30	1	TR1	200 k	TRIMM-100 x 50 x 110 - 64 W
31	1	U1	L6472	POWERSO065P-145X36-36-EP

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Figure 3. EVAL6472PD - layout (top layer)

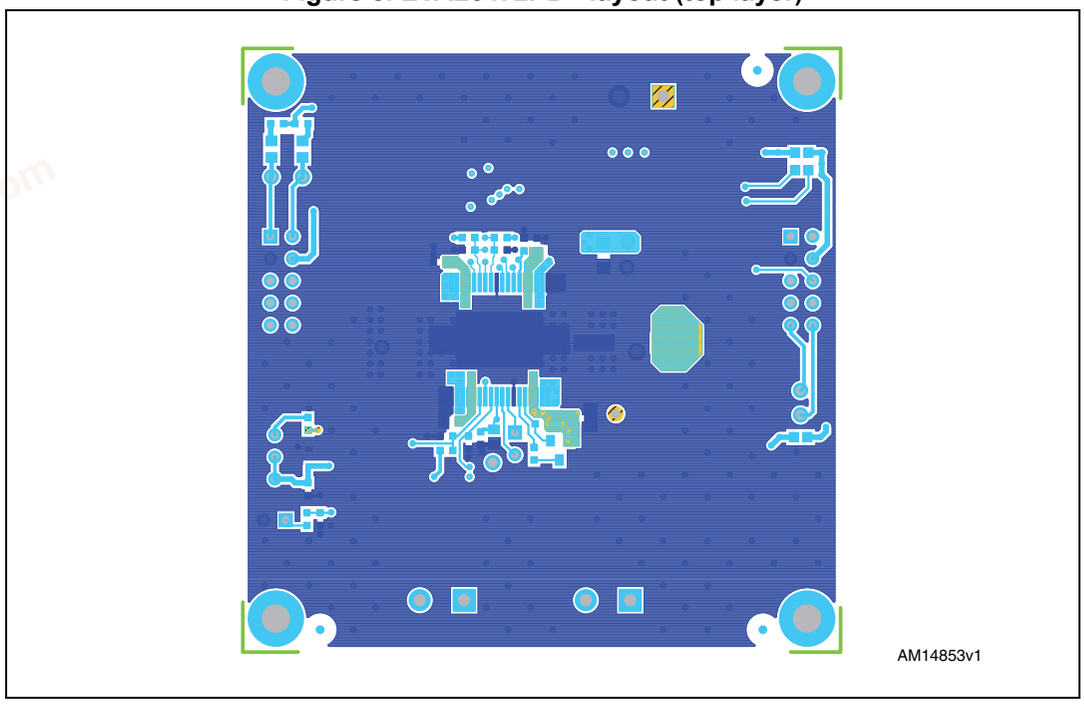
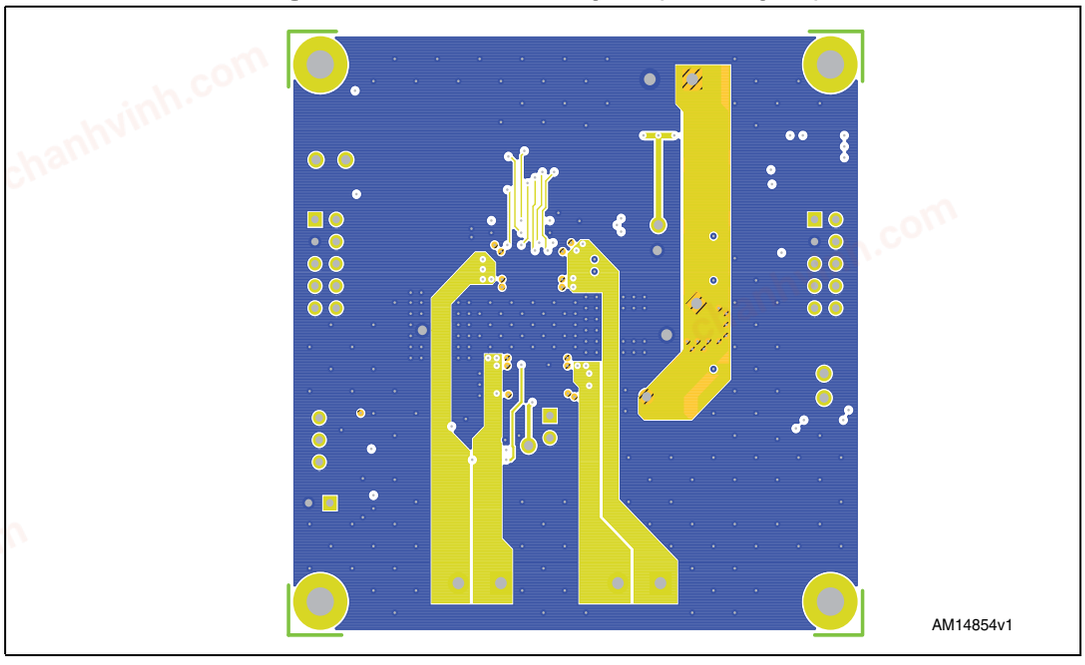


Figure 4. EVAL6472PD - layout (inner layer2)



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Figure 5. EVAL6472PD - layout (inner layer3)

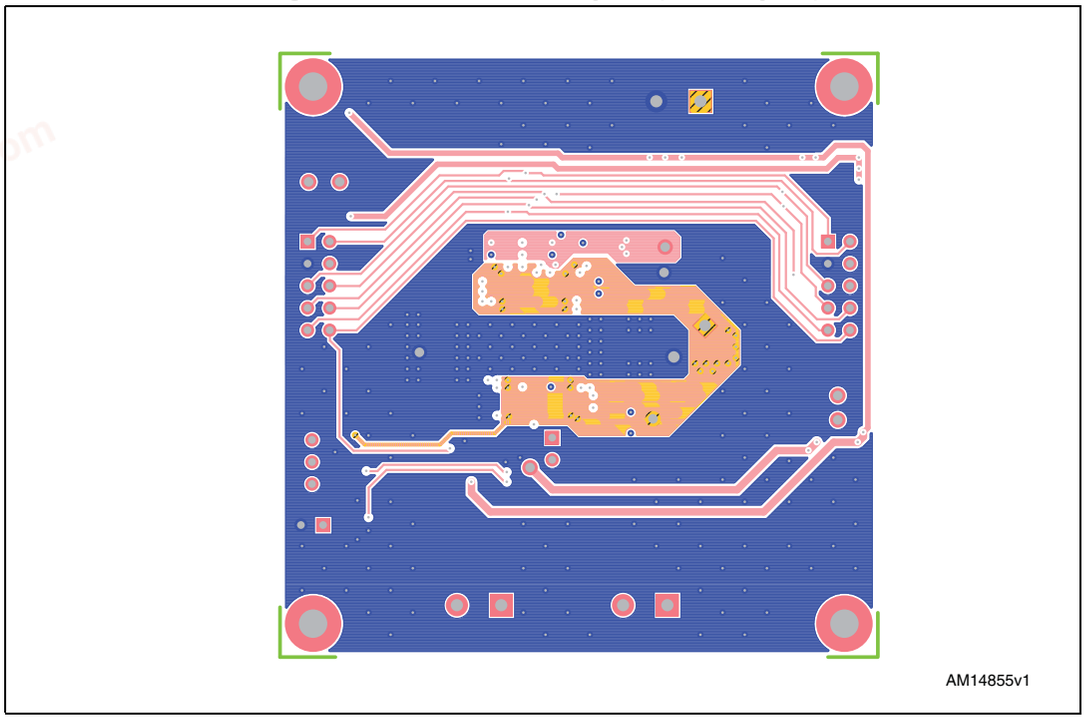
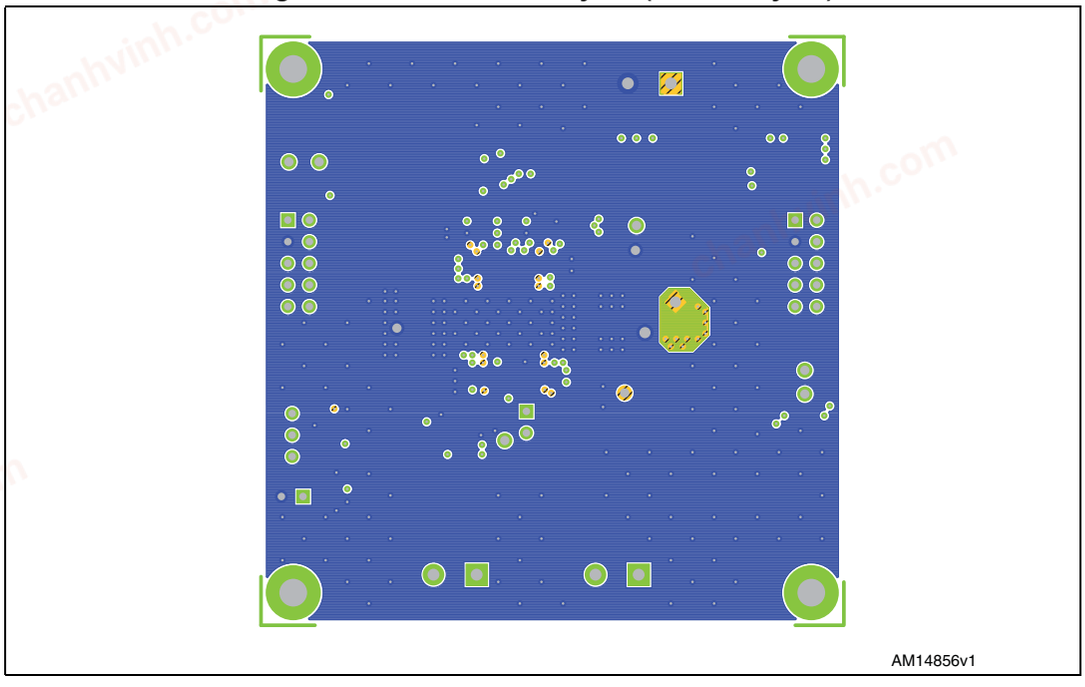


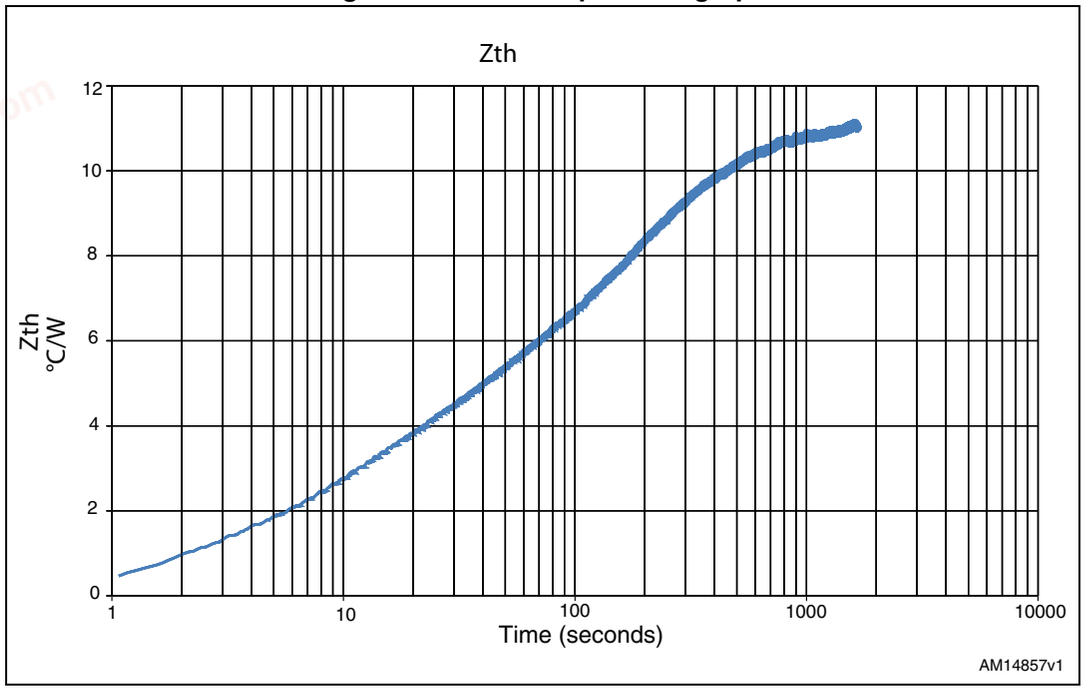
Figure 6. EVAL6472PD - layout (bottom layer3)



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Thermal data

Figure 7. Thermal impedance graph



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Revision history

Table 6. Document revision history

Date	Revision	Changes
30-Nov-2012	1	Initial release.
17-Mar-2015	2	Replaced “dSPIN” by “SPIN” in *Section : Description on page 1*. Removed Figure 3. EVAL6472PD - silkscreen from page 7. Minor modifications throughout document.

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