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ESDAXLC6-1BT2

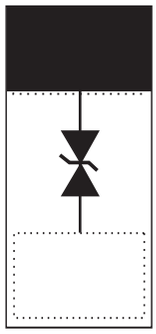
Single-line bidirectional ESD protection for high speed interface

Datasheet - production data



SOD882T
ESDAXLC6-1BT2

Figure 1. Functional diagram (top view)



Features

- Bidirectional device
- Multiple ESD strike sustainability
- Extra low diode capacitance: 0.4 pF
- Low leakage current
- Thin SOD882 package - 0402 size compatible
- Ultra small: 0.6 mm^2
- RoHS compliant

Complies with the following standards:

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phone and accessories
- Tablets, netbooks and notebooks
- Portable multimedia players and accessories
- Digital cameras and camcorders
- Communication systems

Description

The ESDAXLC6-1BT2 is a bidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

This is information on a product in full production. www.st.com

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1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	Peak pulse voltage: IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	 ± 16 ± 25	kV
P_{PP}	Peak pulse power (8/20 µs)	40	W
I_{PP}	Peak pulse current (8/20 µs)	1.3	A
T_j	Operating junction temperature range	- 40 to +150	°C
T_{stg}	Storage temperature range	- 65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s	260	°C

Note: For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 2. Electrical characteristics (definitions)

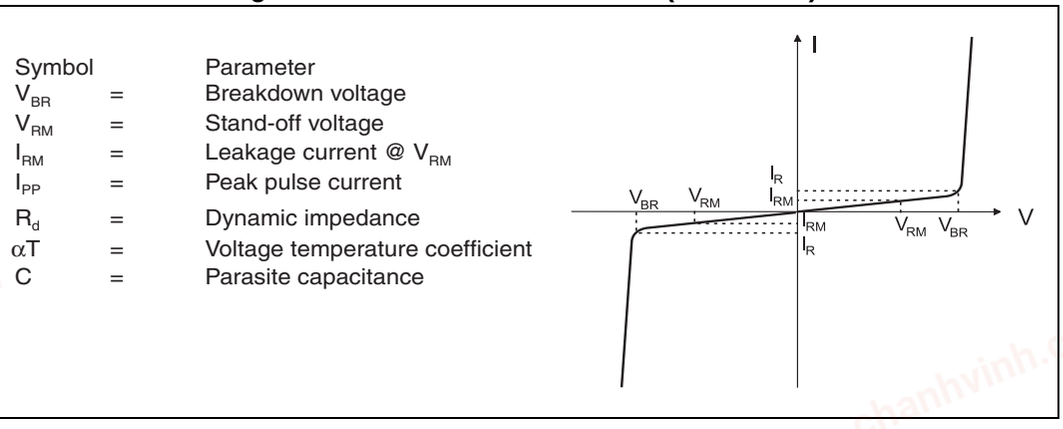


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 3 V			70	nA
V_{CL}	I_{PP} = 1 A, 8/20 µA			17	V
C_{line}	F = (200 MHz- 3000 MHz), V_R = 0 V		0.4	0.5	pF

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Figure 3. Leakage current versus junction temperature (typical values)

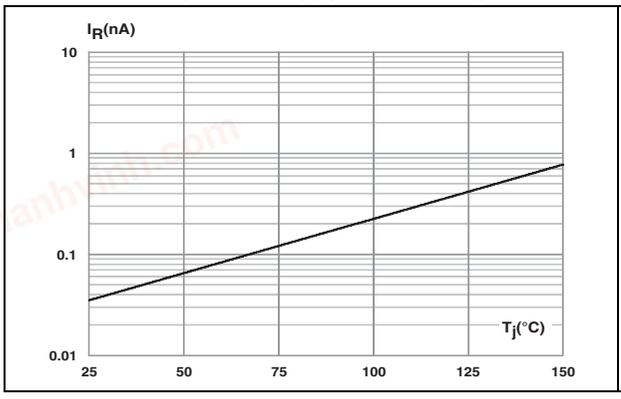


Figure 4. Junction capacitance versus applied voltage (typical values)

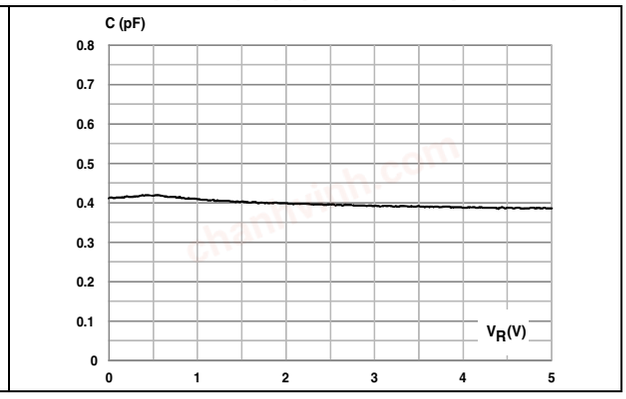


Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

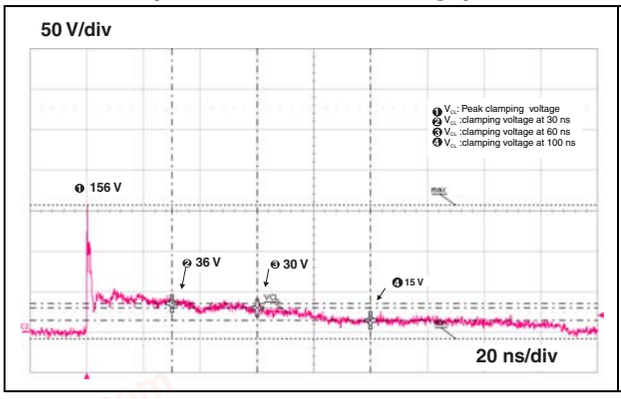


Figure 6. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

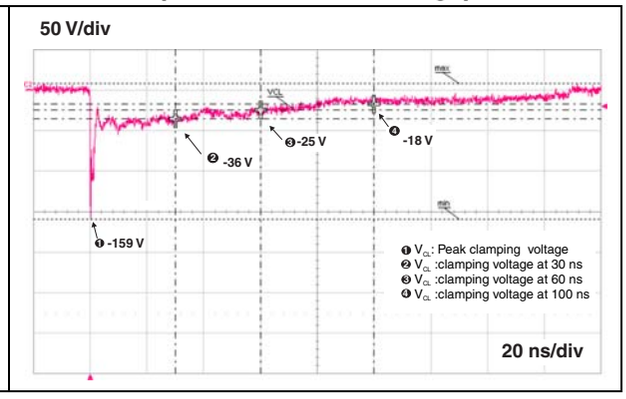
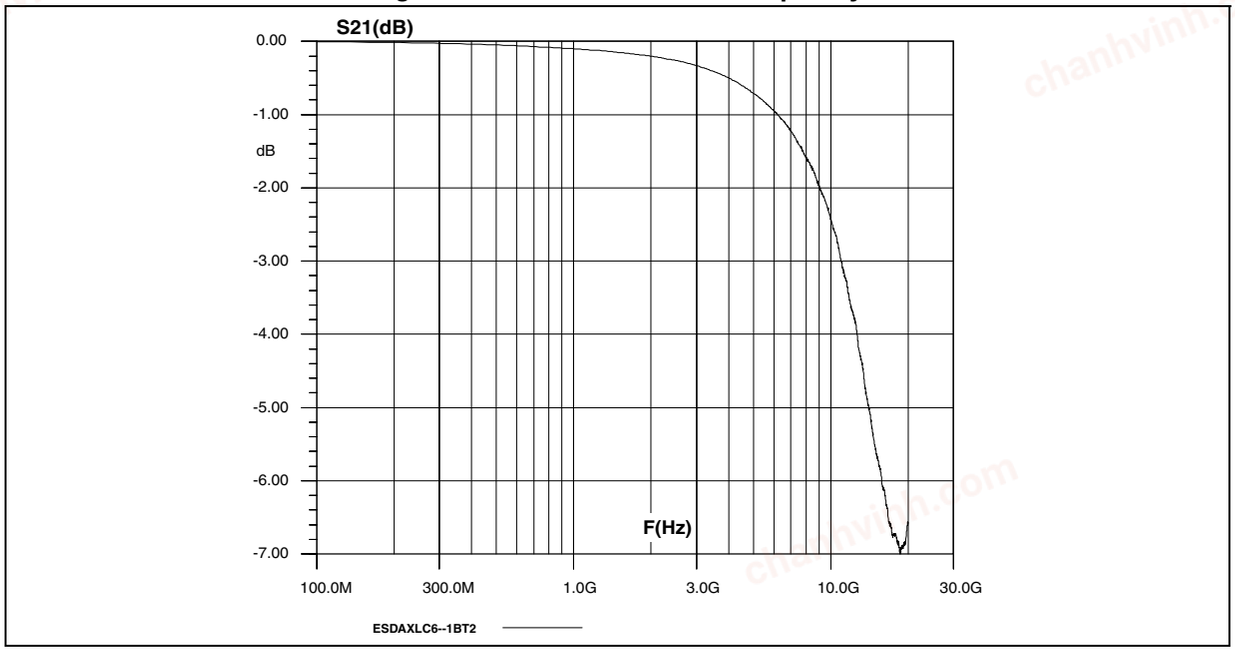


Figure 7. Attenuation versus frequency



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2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

Figure 8. SOD882 thin dimension definitions

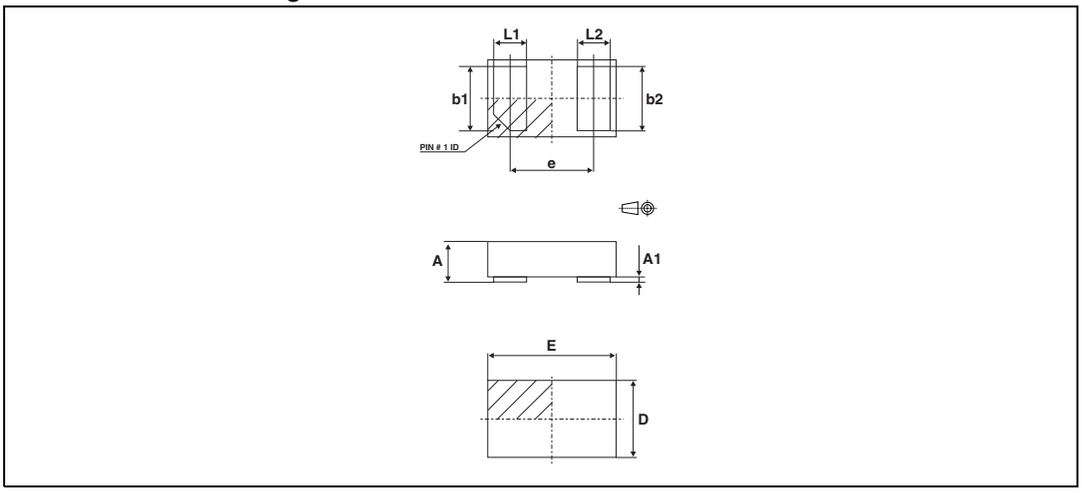


Table 3. SOD882 thin dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.30		0.40	0.012		0.016
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

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Figure 9. Footprint dimension in mm (inches)

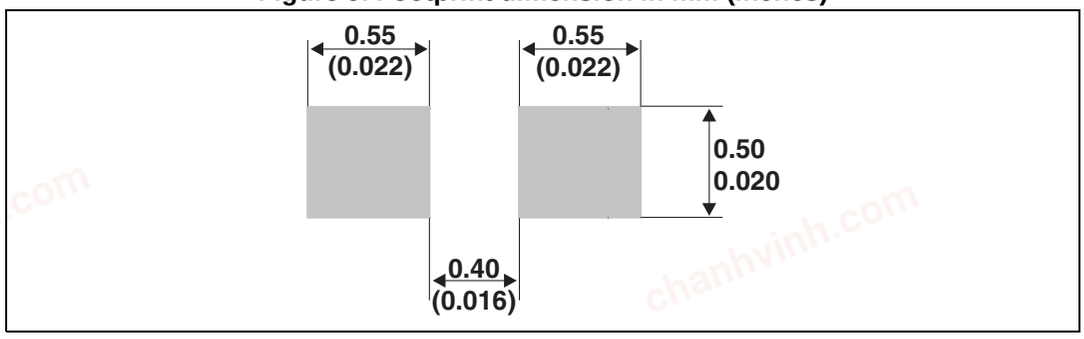
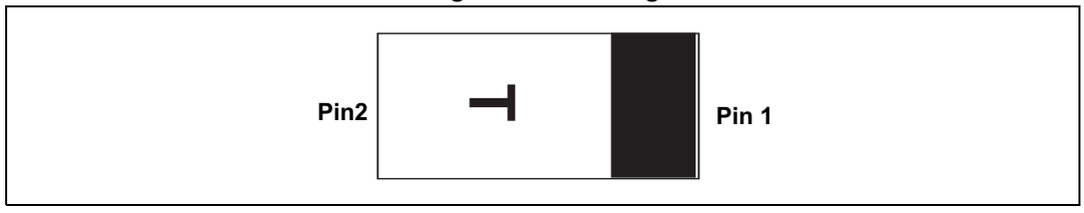
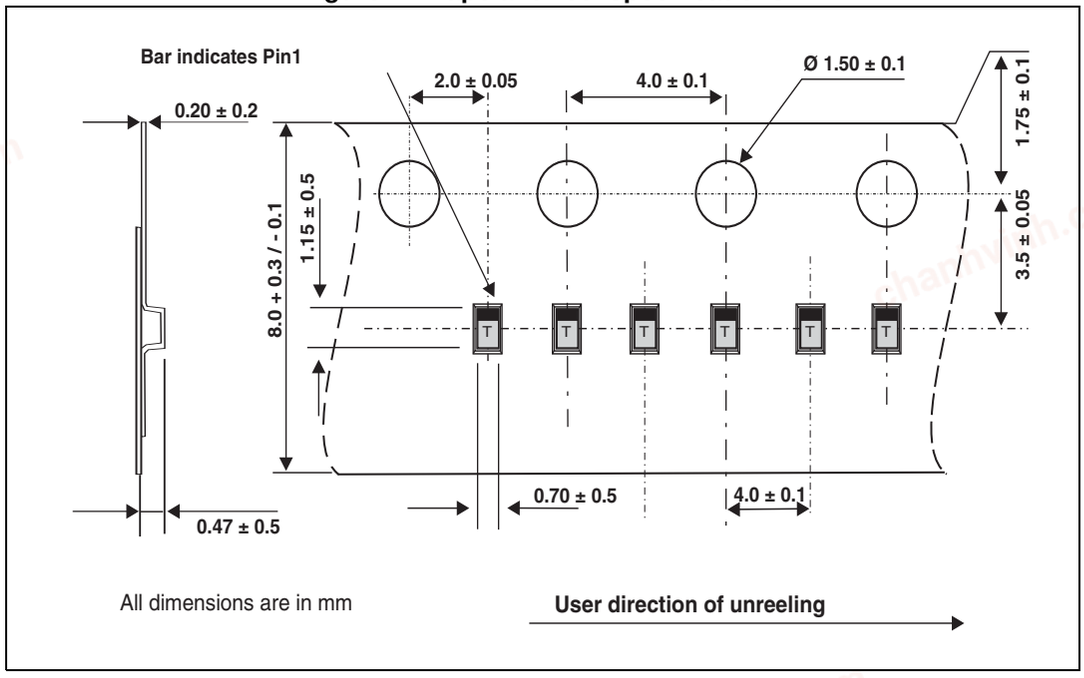


Figure 10. Marking



Note: Product marking may be rotated by multiples of 180° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 11. Tape and reel specifications



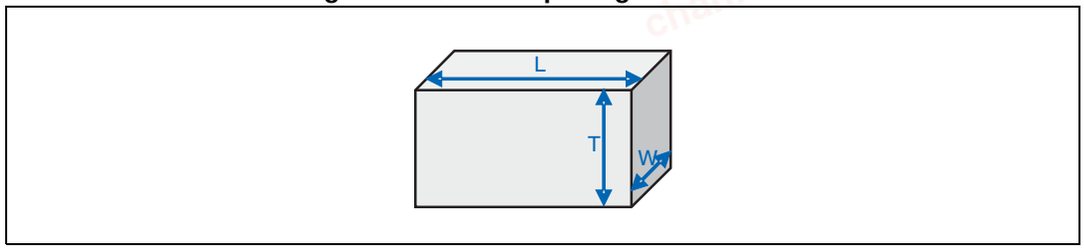
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3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 12. Stencil opening dimensions



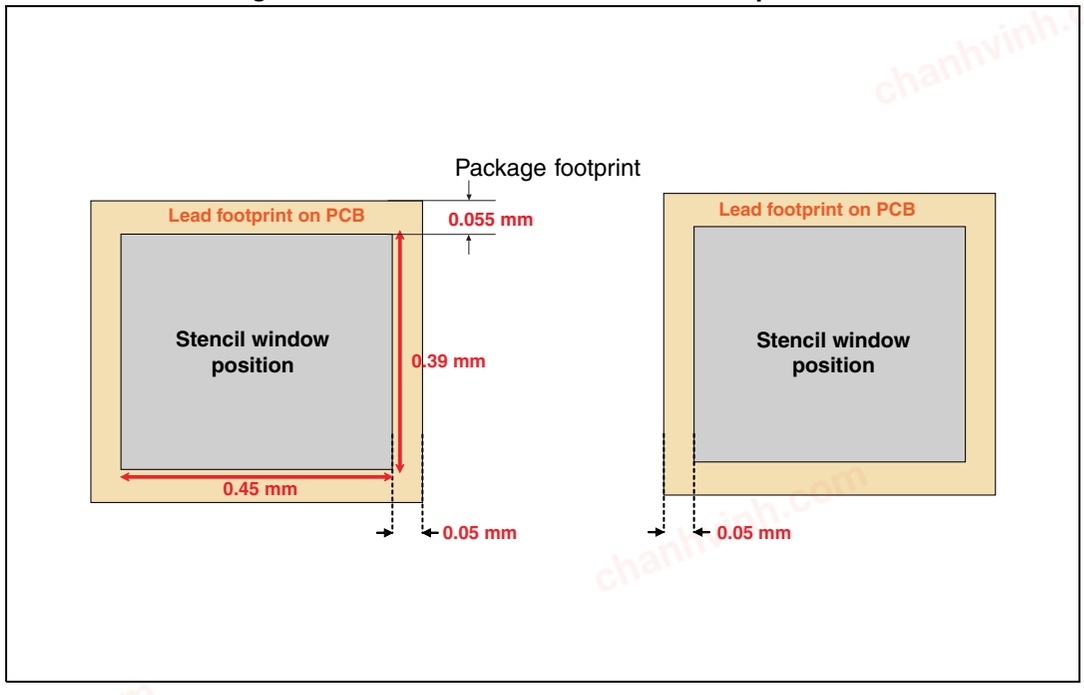
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1{,}5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0{,}66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 13. Recommended stencil window position



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3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

3.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

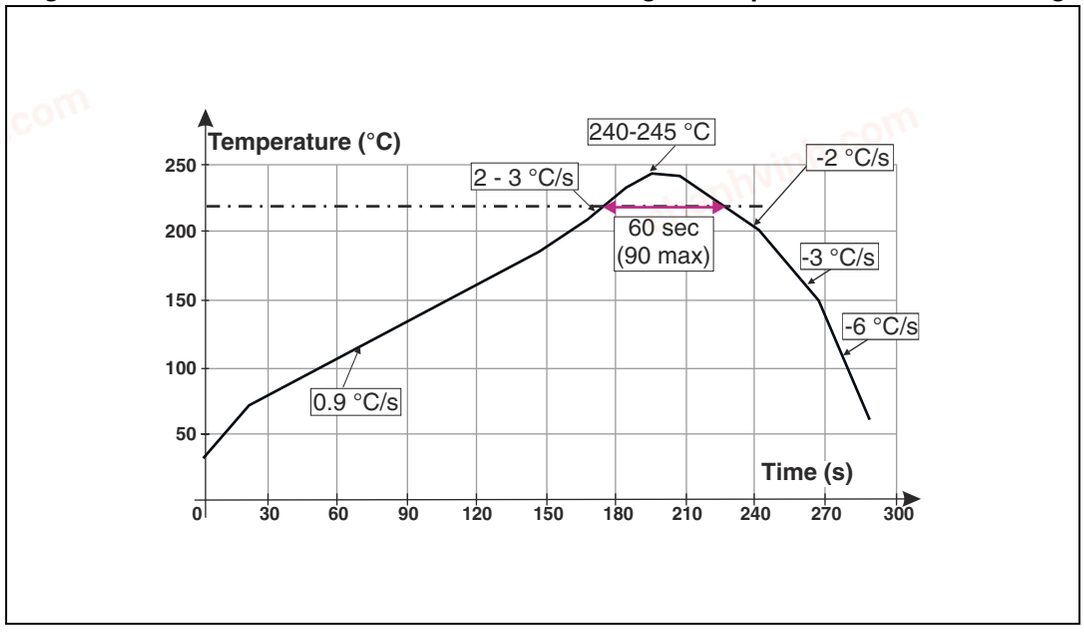
3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

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3.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.
Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

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4 Ordering information

Figure 15. Ordering information scheme

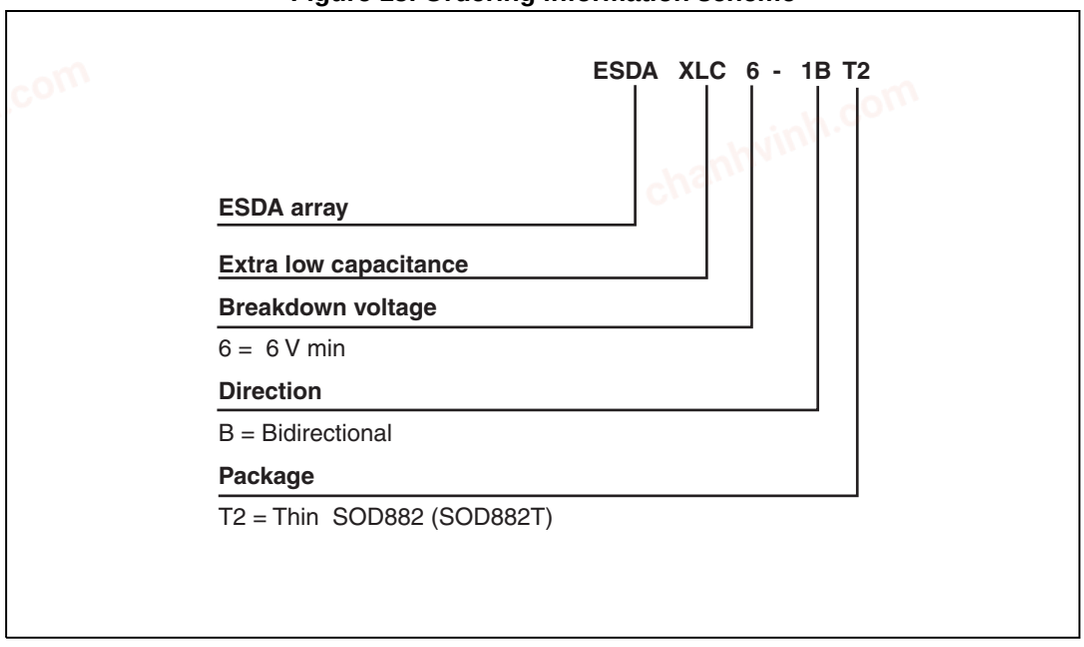


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDAXLC6-1BT2	T(1)	SOD882T	0.8 mg	12000	Tape and reel

1. The marking can be rotated by multiples of 180° to differentiate assembly location

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
04-Sep-2012	1	Initial release.
12-Aug-2013	2	Updated *Figure 4*, *Figure 5*, *Figure 6*, *Figure 11* and *Table 4*.

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