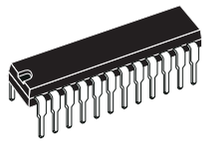
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L6219

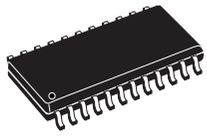
Stepper motor driver

Features

- Able to drive both windings of bipolar stepper motor
- Output current up to 750 mA each winding
- Wide voltage range: 10 V to 46 V
- Half-step, full-step and microstepping mode
- Built-in protection diodes
- Internal PWM current control
- Low output saturation voltage
- Designed for unstabilized motor supply voltage
- Internal thermal shutdown



PDIP24 (20+2+2)



SO24 (20+2+2)

Description

The L6219 is a bipolar monolithic integrated circuits intended to control and drive both winding of a bipolar stepper motor or bidirectionally control two DC motors.

The L6219 with a few external components form a complete control and drive circuit for LS-TTL or microprocessor controlled stepper motor system. The power stage is a dual full bridge capable of sustaining 46V and including four diodes for current recirculation.

A cross conduction protection is provided to avoid simultaneous cross conduction during switching current direction.

An internal pulse-width-modulation (PWM) controls the output current to 750 mA with peak startup current up to 1 A.

Wide range of current control from 750 mA (each bridge) is permitted by means of two logic inputs and an external voltage reference. A phase input to each bridge determines the load current direction. A thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

Table 1. Device summary

Part number	Package	Packing
E-L6219	PDIP24	Tube
E-L6219DS	SO24	Tube
E-L6219DS013TR	SO24	Tape & reel

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Contents

1 **Block diagram** 5

2 **Functional description** 9

2.1 Input logic (I0 and I1) 9

2.2 Phase 9

2.3 Current sensor 9

2.4 Single-pulse generator 10

2.5 Output stage 10

2.6 VS, VSS, VRef 11

3 **Application informations** 12

4 **Package information** 13

5 **Revision history** 15

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List of tables

Table 1. Device summary 1
Table 2. Absolute maximum rating 5
Table 3. Pin functions 6
Table 4. Thermal data 7
Table 5. Electrical characteristcs 8
Table 6. Current levels 9
Table 7. Document revision history 15

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List of figures

Figure 1. Block diagram 5
Figure 2. SO24/PDIP24 pins connection (top view) 6
Figure 3. Timing diagram 7
Figure 4. Principle operating sequence 10
Figure 5. Typical application circuit 12
Figure 6. SO24 mechanical data and package dimensions 13
Figure 7. PDIP24 mechanical data and package dimensions 14

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1 Block diagram

Figure 1. Block diagram

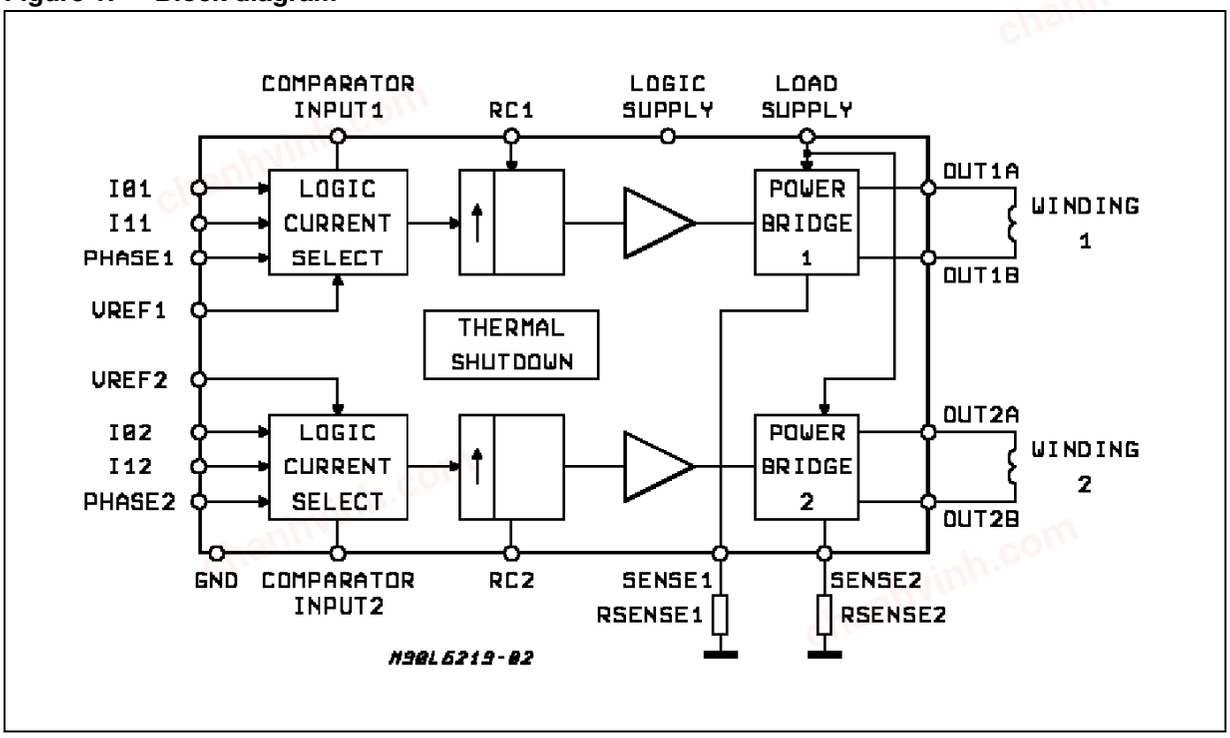


Table 2. Absolute maximum rating

Parameter	Description	Value	Unit
V_s	Supply voltage	50	V
I_O	Output current (peak)	±1	A
I_O	Output current (continuous)	±0.75	A
V_{ss}	Logic supply voltage	7	V
V_{in}	Logic input voltage range	-0.3 to +7	V
V_{sense}	Sense output voltage	1.5	V
T_j	Junction temperature	+150	°C
T_{op}	Operating temperature range	-20 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

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Figure 2. SO24/PDIP24 pins connection (top view)

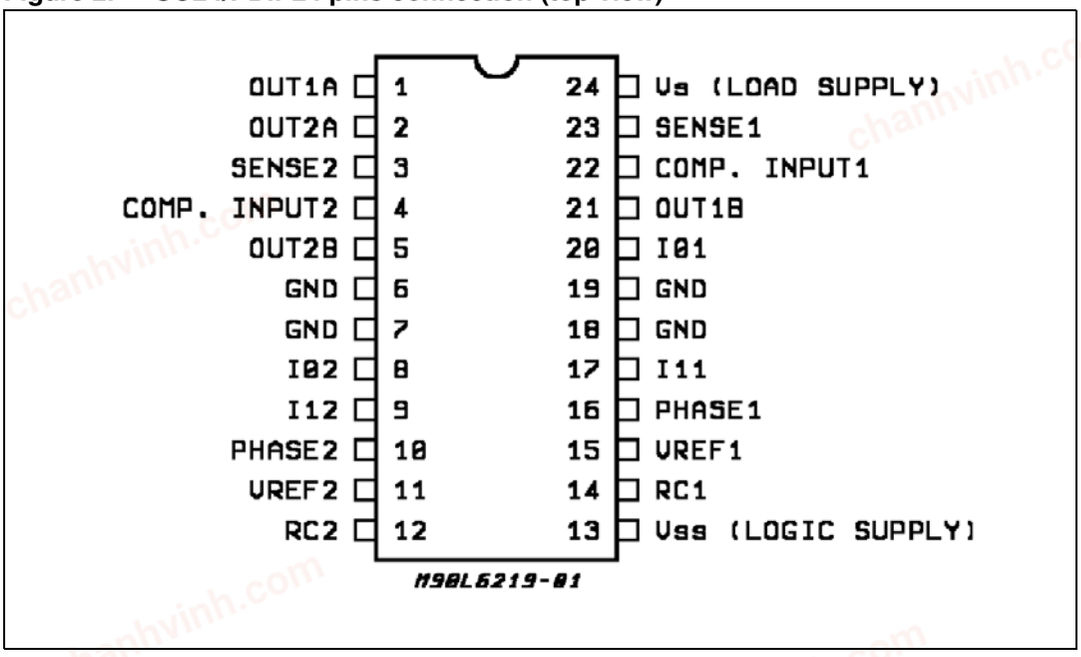


Table 3. Pin functions

Pin #	Name	Description
1, 2	Output A	See pins 5, 21
3, 23	Sense resistor	Connection to lower emitters of output stage for insertion of current sense resistor
4, 22	Comparator input	Input connected to the comparators. The voltage across the sense resistor is feedback to this input throught the low pass filter RC CC. The higher power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by RT CT (toff = 1.1 RT CT). See *Figure 3*.
5, 21	Output B	Output connection. The output stage is a H bridge formed by four transistors and four diodes suitable for switching applications
6, 19	Ground	See pins 7, 18
7, 18	Ground	Ground connection. With pins 6 and 19 also conducts heat from die to printed circuit copper
8, 20	Input 0	See Input 1 (pins 9, 17)
9, 17	Input 1	These pins and pins 8, 20 (input 0) are logic inputs which select the outputs of the comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See functional description

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Table 3. Pin functions (continued)

Pin #	Name	Description
10, 16	Phase	This TTL-compatible logic inputs sets the direction of current flow through the load. A high level causes current to flow from output A (source) to output B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching
11, 15	Reference voltage	A voltage applied to this pin sets the reference voltage of the comparators, this determining the output current (also thus depending on Rs and the two inputs input 0 and input 1)
12, 14	RC	A parallel RC network connected to this pin sets the OFF time of the higher power transistors. The pulse generator is a monostable triggered by the output of the comparators (toff = 1.1 RT CT)
13	V_{SS} - Logic supply	Supply voltage input for logic circuitry
24	V_S - Load supply	Supply voltage input for the output stages

Note: ESD on GND, V_S, V_{SS}, OUT 1 A and OUT 2 A is guaranteed up to 1.5 KV (human body model, 1500 W, 100 pF).

Figure 3. Timing diagram

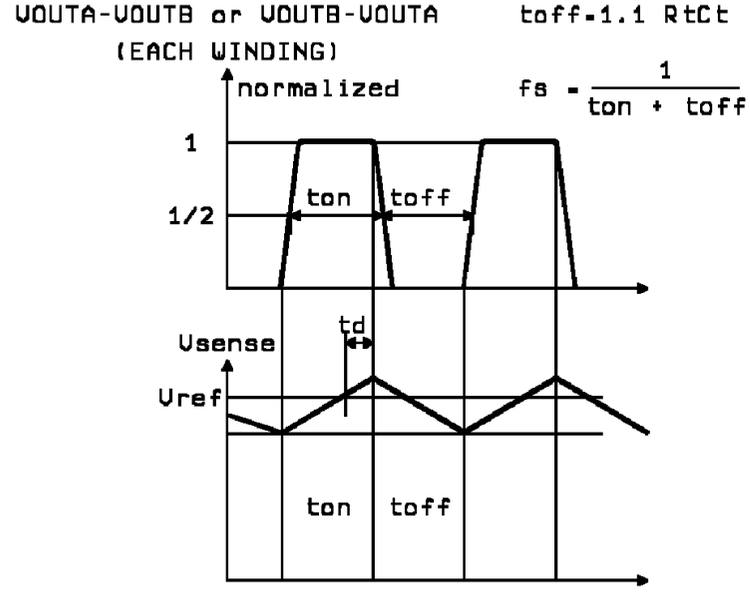


Table 4. Thermal data

Parameter	Description		PDIP	SO	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	max.	14	18	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max.	60 (1)	75 (1)	°C/W

1. With minimized copper area.

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Table 5. Electrical characteristcs

(T_j = 25 °C, V_S = 46 V, V_{SS} = 4.75 V to 5.25 V, V_{REF} = 5 V, unless otherwise specified) See *Figure 5*

Parameter	Description	Test condition	Min.	Typ.	Max.	Unit
Output drivers (OUT_A or OUT_B)						
V_S	Motor supply range		10		46	V
I_{CEX}	Output leakage current	V_{OUT} = Vs, V_{OUT} = 0	- -	<1 <-1	50 -50	µA µA
$V_{CE(sat)}$	Output saturation voltage	Sink driver, I_{OUT}= +500 mA Sink driver, I_{OUT} = +750 mA Source driver, I_{OUT} = -500 mA Source driver, I_{OUT} = -750 mA	- - - -	0.3 0.7 1.1 1.3	0.6 1 1.4 1.6	V V V V
I_R	Clamp diode leakage current	V_R = 50 V	-	<1	50	µA
V_F	Clamp diode forward voltage	Sink diode Source diode I_F = 750 mA		1 1	1.5 1.5	V V
$I_{S(on)}$	Driver supply current	Both bridges ON, no load	-	8	15	mA
$I_{S(off)}$	Driver supply current	Both bridges OFF	-	6	10	mA
Control logic						
$V_{IN(H)}$	Input voltage	All inputs	2.4	-	-	V
$V_{IN(L)}$	Input voltage	All inputs	-	-	0.8	V
$I_{IN(H)}$	Input current	V_{IN} = 2.4 V	-	<1	20	µA
$I_{IN(L)}$	Input current	V_{IN} = 0.84 V	-	-3	-200	µA
V_{REF}	Reference voltage	Operating (1)	1.5	-	7.5	V
$I_{SS(ON)}$	Total logic supply current	I_o = I_1 = 0.8 V, no load	-	64	74	mA
$I_{SS(OFF)}$	Total logic supply current	I_o = I_1 = 2.4 V, no load	-	10	14	mA
Comparators						
V_{REF}/ V_{sense}	Current limit threshold (at trip point)	I_o = I_1 = 0.8 V	9.5	10	10.5	-
		I_o = 2.4 V, I_1 = 0.8 V	13.5	15	16.5	-
		I_o = 0.8 V, I_1 = 2.4 V	25.5	30	34.5	-
t_{off}	Cutoff time	R_t = 56 KΩ C_t = 820 pF	-	50		µs
t_d	Turn off delay	*Figure 3*	-	1		µs
Protection						
T_J	Thermal shutdown temperature		-	170	-	°C

1. To reduce the switching losses the base bias of the bridge's low side NPN transistor is proportional to the DAC output, then the output current driving capability is also proportional to the DAC output voltage, having as reference 750 mA with V_{REF} = 5 V and DAC =100%. For example using V_{REF} = 2 V and DAC = 67% the output maximum current driving capability will become 750 mA*(2V*0.67)/(5V*1) = 200 mA.

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2 Functional description

The circuit is intended to drive both windings of a bipolar stepper motor.

The peak current control is generated through switch mode regulation. There is a choice of three different current levels with the two logic inputs I01 - I11 for winding 1 and I02 - I12 for winding 2.

The current can also be switched off completely.

2.1 Input logic (I_0 and I_1)

The current level in the motor winding is selected with these inputs. (See *Figure 4*). If any of the logic inputs is left open, the circuit will treat it has a high level input.

Table 6. Current levels

I0	I1	Current level
H	H	No current
L	H	Low current 1/3 IO max
H	L	Medium current 2/3 IO max
L	L	Maximum current IO max

2.2 Phase

This input determines the direction of current flow in the windings, depending on the motor connections. The signal is fed through a schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift. High level on the phase input causes the motor current flow from out A through the winding to out B.

2.3 Current sensor

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_o and I_1. The motor current flows through the sensing resistor RS. When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator goes high, which triggers the pulse generator.

The max peak current Imax can be defined by:

$$I_{max} = \frac{V_{ref}}{10R_s}$$

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2.4 Single-pulse generator

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, toff, which is determined by the time components Rt and Ct.

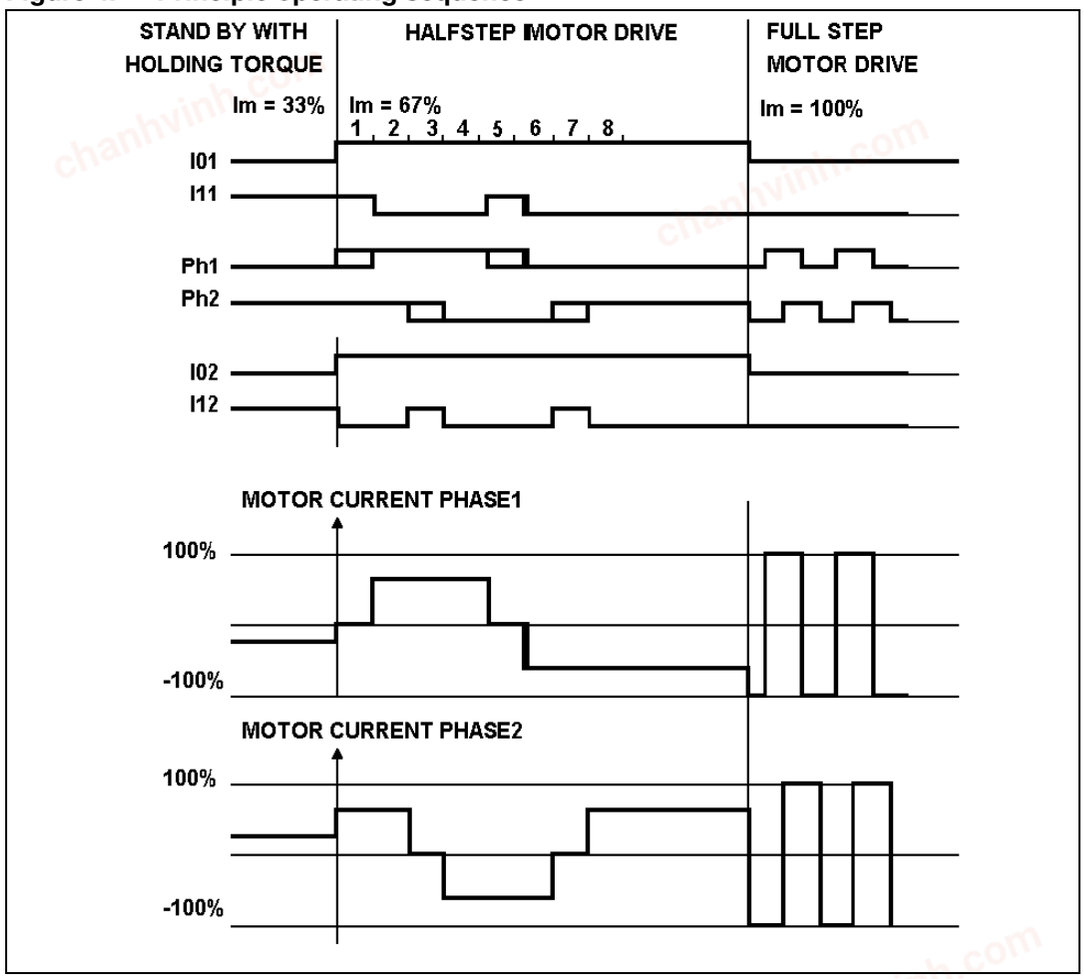
$$t_{off} = 1.1 \cdot R_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}. If a new trigger signal should occur during t_{off}, it is ignored.

2.5 Output stage

The output stage contains four darlington transistors (source drivers) four saturated transistors (sink drivers) and eight diodes, connected in two H bridge.

Figure 4. Principle operating sequence



The source transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding. It should be noted however, that is not permitted to short circuit the outputs.

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Internal circuitry is added in order to increase the accuracy of the motor current particularly with low current levels.

2.6 V_S, V_{SS}, V_{Ref}

The circuit will stand any order of turn-on or turn-off the supply voltages V_S and V_{SS}. Normal dV/dt values are then assumed.

Preferably, V_{Ref} should be tracking V_{SS} during power-on and power-off if V_S is established.

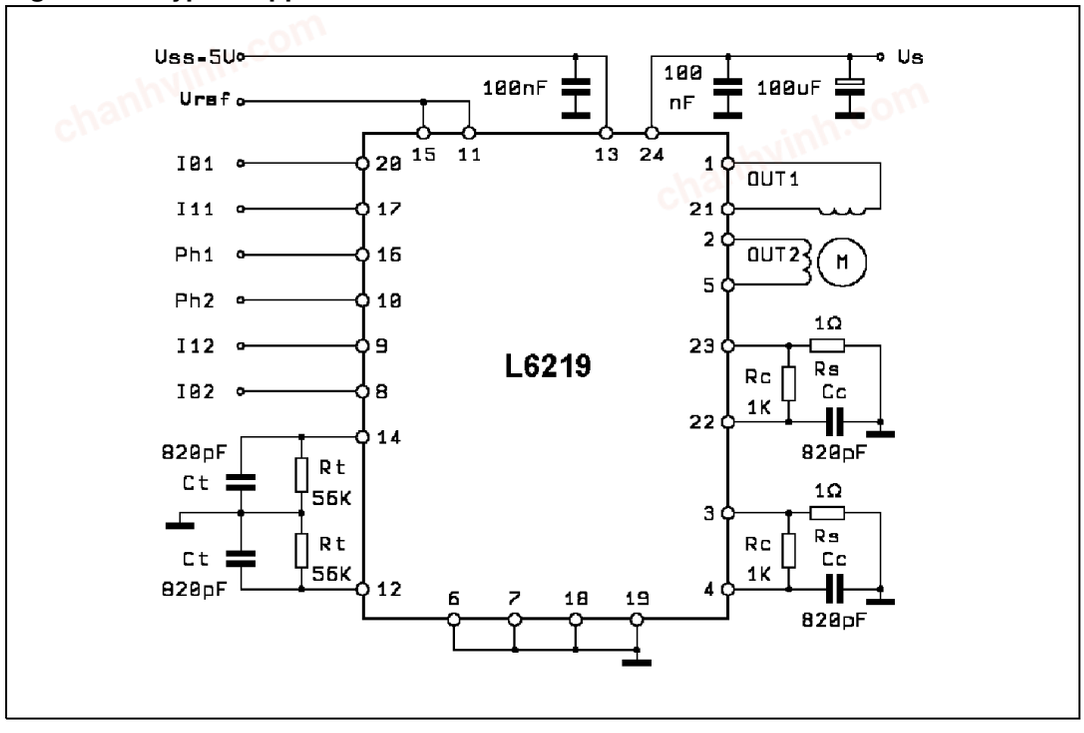
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3 Application informations

Some stepper motors are not designed for contin-uous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation. Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.

Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity. As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 100 nF capacitor, located near the package between power line and ground. The ground lead between Rs, and circuit GND should be kept as short as possible. A typical application circuit is shown in *Figure 5*. Note that C_t must be NPO type or similar else. To sense the winding current, paralleled metal film resistors are recommended (R_s).

Figure 5. Typical application circuit



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4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

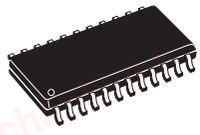
Figure 6. SO24 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

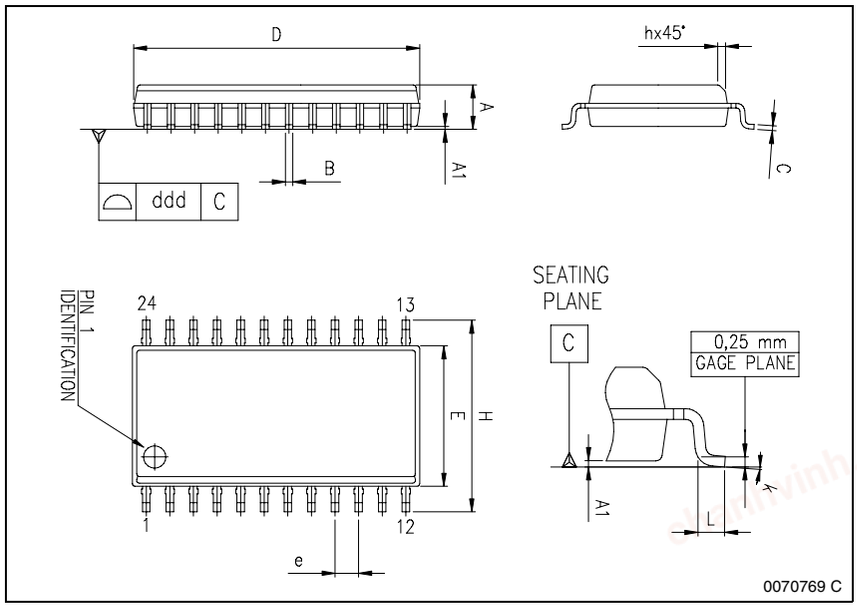
(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

Weight: 0.60gr



SO24

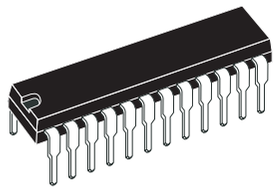


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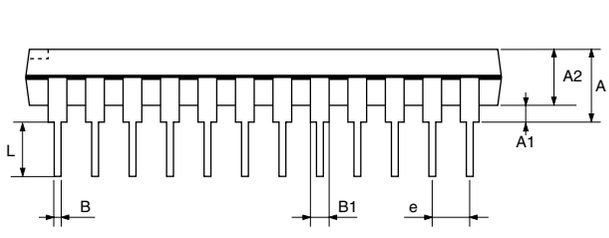
Figure 7. PDIP24 mechanical data and package dimensions

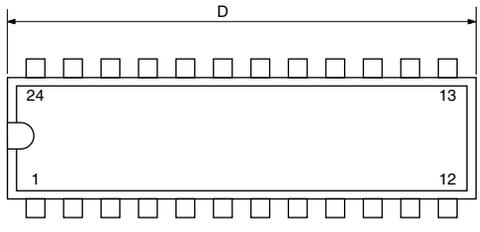
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.320			0.170
A1	0.380			0.015		
A2		3.300			0.130	
B	0.410	0.460	0.510	0.016	0.018	0.020
B1	1.400	1.520	1.650	0.055	0.060	0.065
c	0.200	0.250	0.300	0.008	0.010	0.012
D	31.62	31.75	31.88	1.245	1.250	1.255
E	7.620		8.260	0.300		0.325
e		2.54			0.100	
E1	6.350	6.600	6.860	0.250	0.260	0.270
e1		7.620			0.300	
L	3.180		3.430	0.125		0.135
M	0° min, 15° max.					

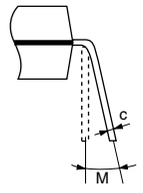
OUTLINE AND MECHANICAL DATA



PDIP 24 (0.300")







SDIP24L

0034965 D

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5 Revision history

Table 7. Document revision history

Date	Revision	Changes
30-Oct-2001	7	First Issue on the EDOCS DMS.
11-May-2005	8	Changed the look & feel layout. Modified *Table 6 on page 9*.
14-Sep-2005	9	Change in the *Features* sections: Wide voltage range 10 V to 46 V Output current up to 750 mA each winding.
19-Dec-2005	10	Corrected in the *Table 5* the max. value of the V_{REF} parameter from 2 V to 7.5 V.
28-Mar-2006	11	Corrected $I_{SS(ON)}$ values in the *Table 5*.
18-Mar-2008	12	Document reformatted.
01-Sep-2008	13	Added note 1 in *Table 5 on page 8*.

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