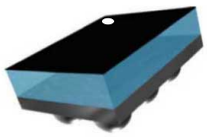
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BALF-SPI2-03D3

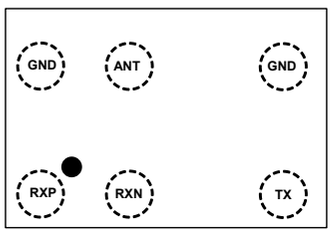
Datasheet

50 Ω nominal input / conjugate matched balun to ST S2-LP, 860 - 930 MHz with integrated harmonic filter



Flip-Chip (6 bumps) package

Pinout diagram - Top view



Product status
BALF-SPI2-03D3

Features

- 50 Ω nominal input / conjugate matched to ST S2-LP for for 860 - 930 MHz frequency operation
- Low insertion loss
- Low amplitude imbalance
- Low phase imbalance
- Small footprint
- Very low profile < 620 µm after reflow
- High RF performance
- RF BOM and area reduction
- ECOPACK2 compliant component

Applications

- 860 - 930 MHz impedance matched balun filter
- Optimized for ST S2-LP sub GHz RFIC

Description

This device is an ultra-miniature balun. The BALF-SPI2-03D3 integrates matching network and harmonics filter. Matching impedance has been customized for the ST S2-LP transceiver. The BALF-SPI2-03D3 uses STMicroelectronics IPD technology on non-conductive glass substrate which optimize RF performance.

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1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
P_{IN}	Input power RF_{IN}	20	dBm
V_{ESD}	ESD ratings human body model (JESD22-A114), all I/O one at a time while others connected to GND	2000	V
	ESD ratings machine model (JESD22-A115), all I/O	200	
T_{OP}	Operating temperature	-40 to +105	°C

Table 2. Impedances (T_{amb} = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z_{RX}	Nominal differential RX balun impedance	-	matched ST S2-LP	-	Ω
Z_{TX}	Nominal TX filter impedance				
Z_{ANT}	Antenna impedance	-	50	-	Ω

Table 3. Electrical characteristics and RF performances (T_{amb} = 25 °C)

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
f	Frequency range (bandwidth)		860		930	MHz
I_{L_RX-ANT}	Insertion loss in bandwidth without mismatch loss (RX balun)			1.85	2.05	dB
I_{L_TX-ANT}	Insertion loss in bandwidth without mismatch loss (TX filter)			1.90	2.35	dB
R_{L_RX-ANT}	Input return loss in bandwidth (RX balun)		16	19		dB
R_{L_TX-ANT}	Input return loss in bandwidth (TX filter)		17	21.5		dB
ϕ_{imb}	Output phase imbalance (RX balun) - absolute value		7.5	12.5	18	°
A_{imb}	Output amplitude imbalance (RX balun) - absolute value		0.1	0.85	1.65	dB
Att	Harmonic levels (TX filter)	Attenuation at 2fo	45	48		dB
		Attenuation at 3fo	60	75		
		Attenuation at 4fo	53	59		
		Attenuation at 5fo	41	43		
		Attenuation at 6fo	42	46		

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1.1 RF measurements (RX balun)

Figure 1. Insertion loss

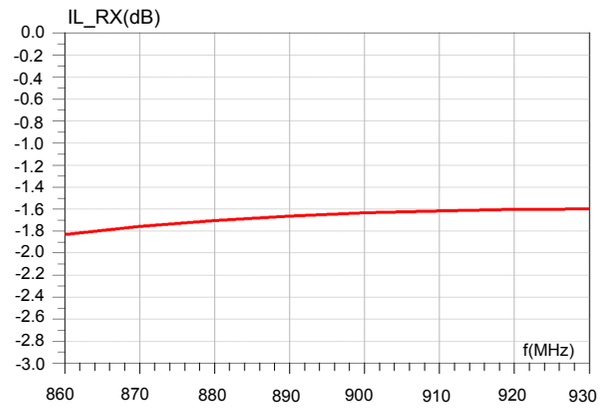


Figure 2. Return loss on antenna

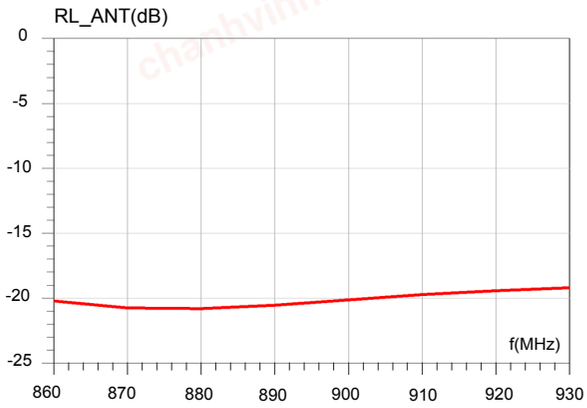


Figure 3. Amplitude imbalance

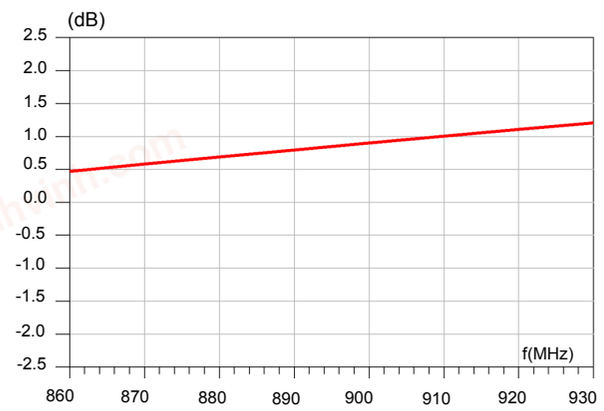
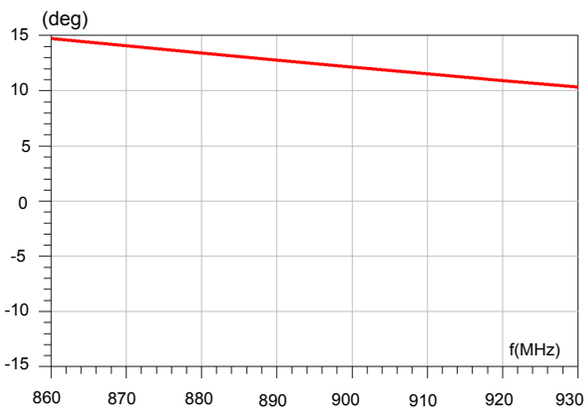


Figure 4. Phase imbalance



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1.2 RF measurements (TX filter)

Figure 5. Transmission

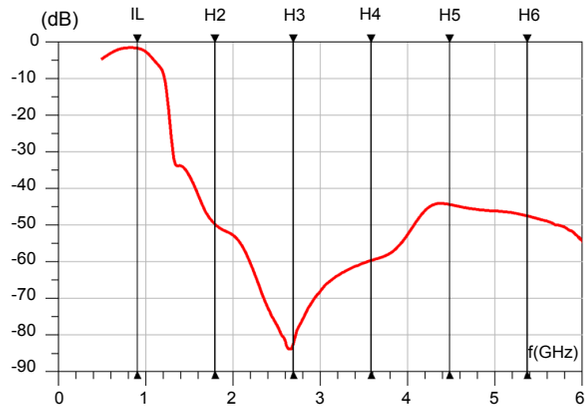


Figure 6. Insertion loss

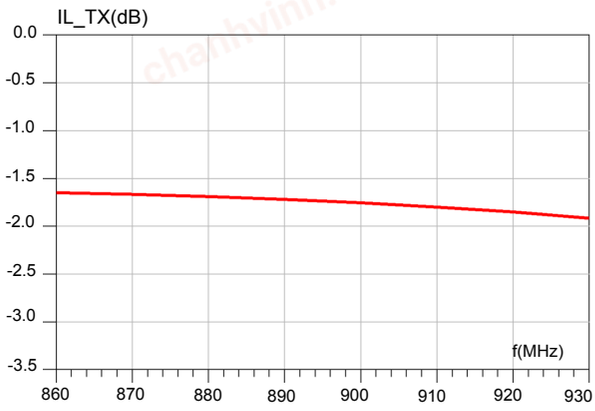


Figure 7. 2nd harmonic

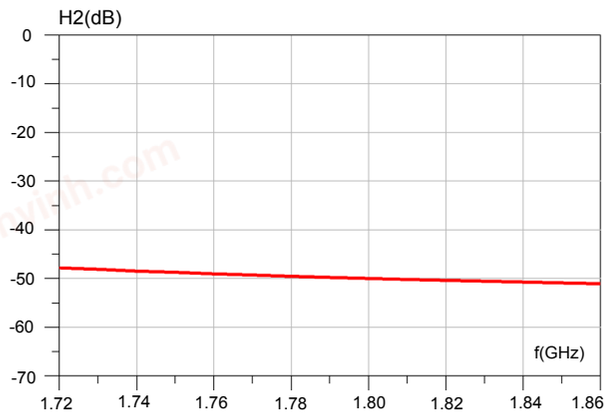


Figure 8. 3rd harmonic

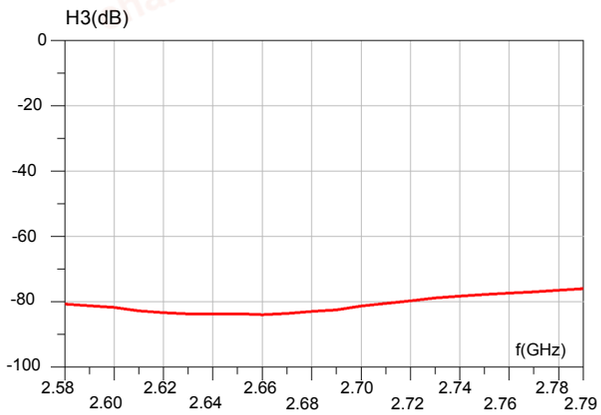


Figure 9. 4th harmonic

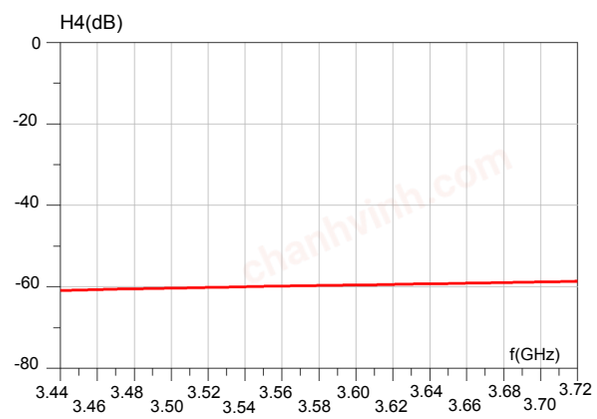
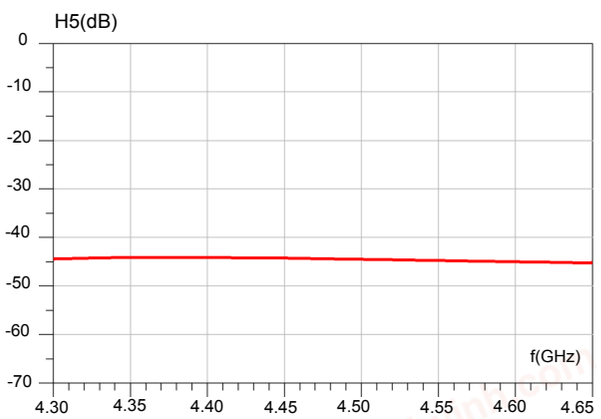


Figure 10. 5th harmonic



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Figure 11. 6th harmonic

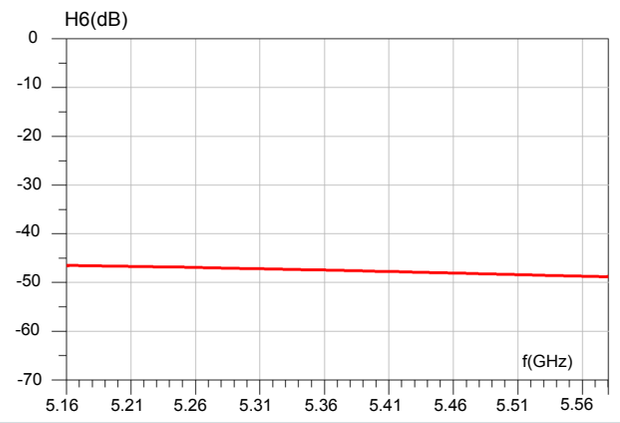
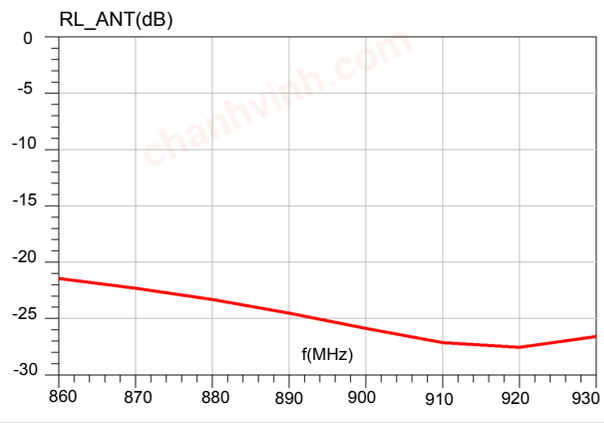


Figure 12. Return loss on antenna



1.3 RF measurement (performances system on 2 layers PCB)

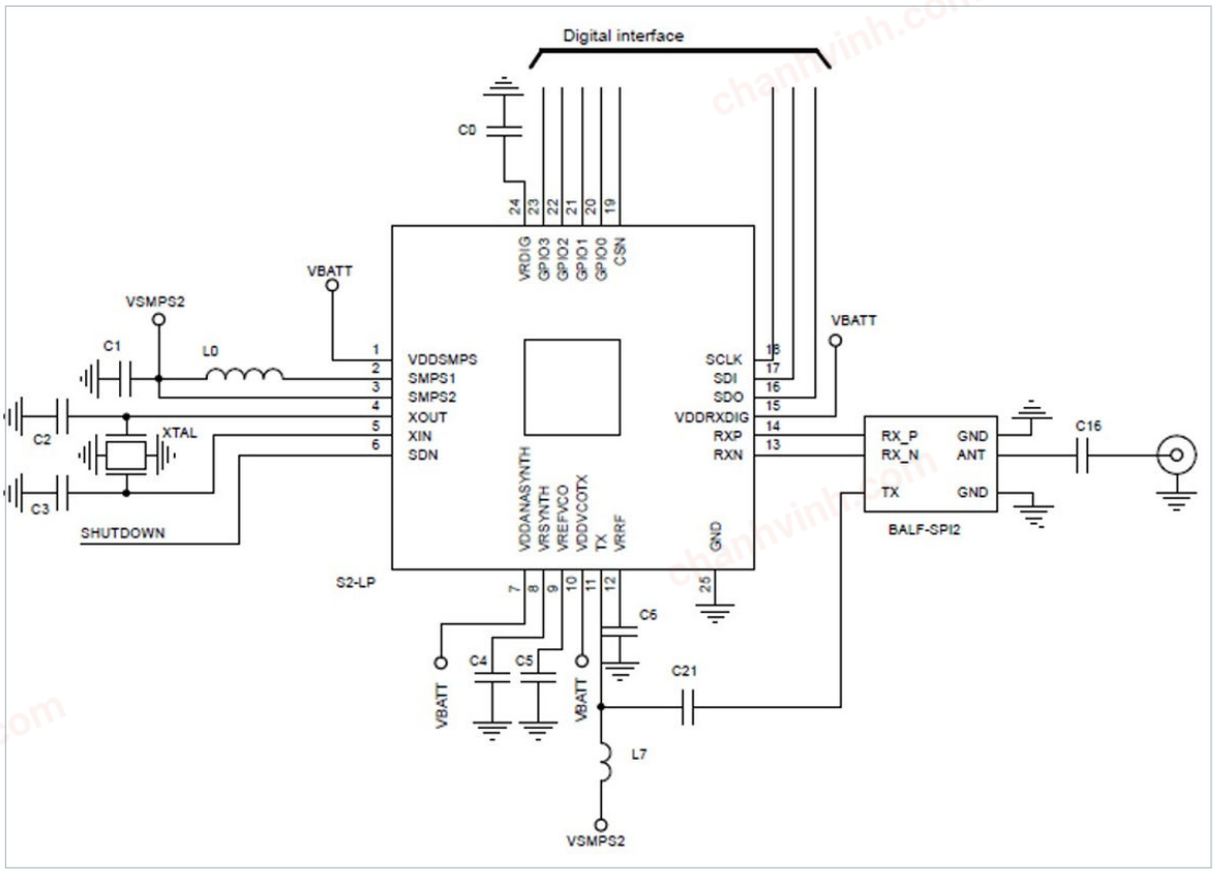
Table 4. RF measurement

RF tests		IPD BALF-SPI2-03D3 (PCB 2 layers 1.6 mm)
RX current (mA)		10.1
Sensitivity (1% BER)	4 kHz RX BW	-122
	100 kHz RX BW	-108.5
	500 kHz RX BW	-100
High power mode (14 dBm)	P_{OUT} (dBm)	14.5
	TX current (mA)	21.7
	Harmonics (dBm)	H2: -42.2 / H3: -53 / H4: -52.3 / H5: -41.4 / H6: -53.9
Boost mode (16 dBm)	P_{OUT} (dBm)	15.9
	TX current (mA)	29.2
	Harmonics (dBm)	H2: -42 / H3: -49.6 / H4: -51.6 / H5: -39.6 / H6: -52.9

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1.4 ST S2-LP application diagram example

Figure 13. **ST S2-LP application diagram example**



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2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 Flip-Chip 6 bumps package information

Figure 14. Flip-Chip 6 bumps package outline (bottom and side view)

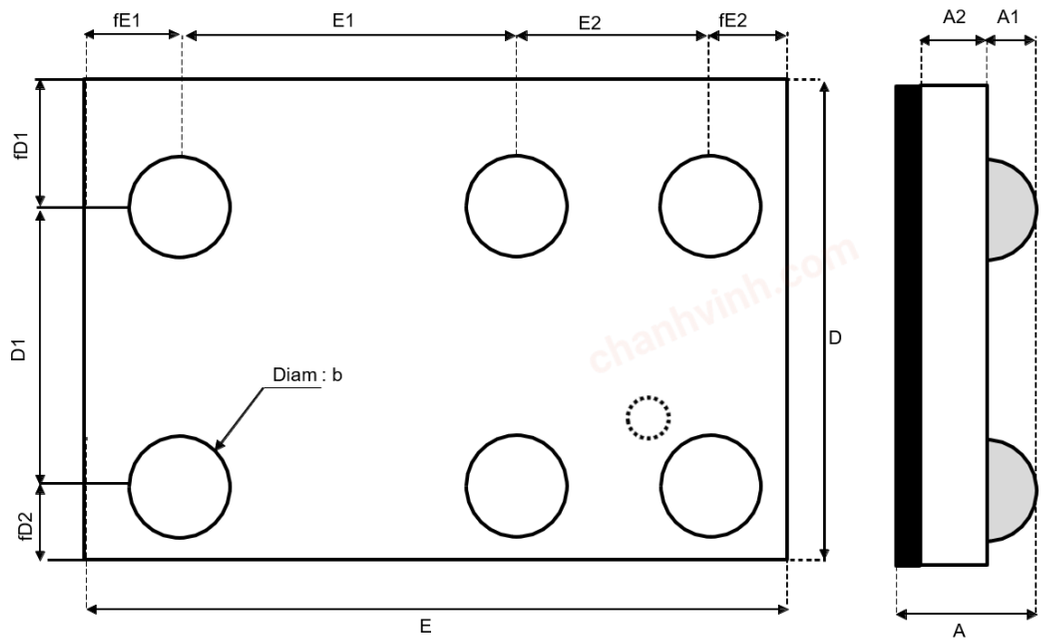


Table 5. Flip-Chip 6 bumps dimensions (in mm)

Parameter	Min.	Typ.	Max.
A	0.585	0.630	0.675
A1	0.180	0.205	0.230
A2	0.380	0.400	0.420
b	0.230	0.255	0.280
D	1.572	1.602	1.632
D1		1.060	
E	2.146	2.176	2.206
E1		1.210	
E2		0.500	
fD1		0.299	
fD2		0.223	
fE1		0.223	
fE2		0.223	

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2.2 Flip-chip 6 bumps packing information

Figure 15. **Marking**

Dot, ST logo
ECOPACK grade
zz = marking
x = manufacturing location
yww = datecode



Figure 16. **Top view**

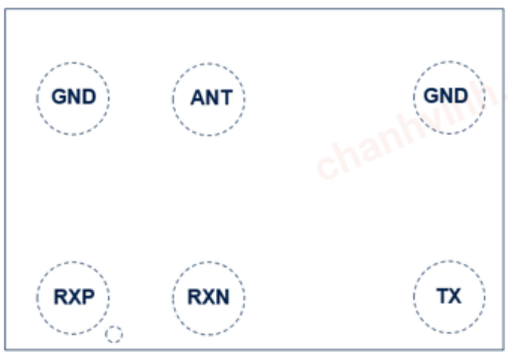
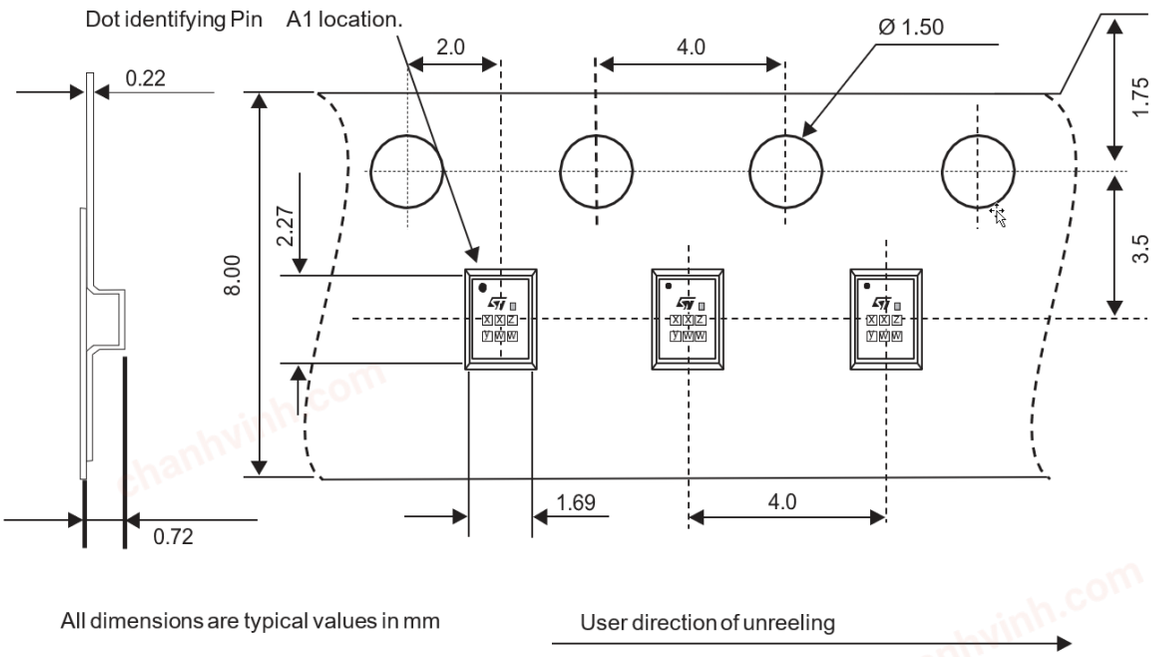


Figure 17. **Flip Chip tape and reel specifications**



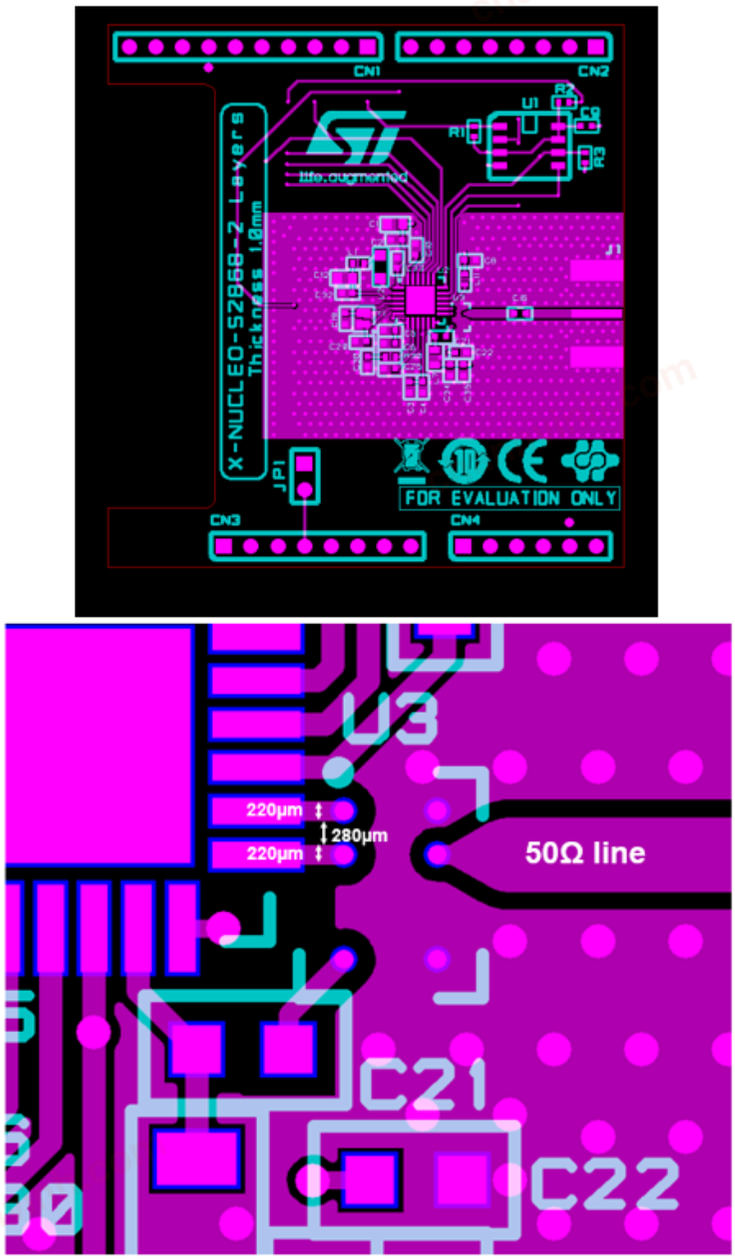
Note: More packing information is available in the application note AN2348: IPAD™ 400 µm Flip Chip: package description and recommendations for use.

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3 PCB assembly recommendations

3.1 Land pattern

Figure 18. **Recommended balun land pattern**



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Figure 19. **PCB 1 mm stack-up recommendations (FR4 IS400 Er = 3.9)**

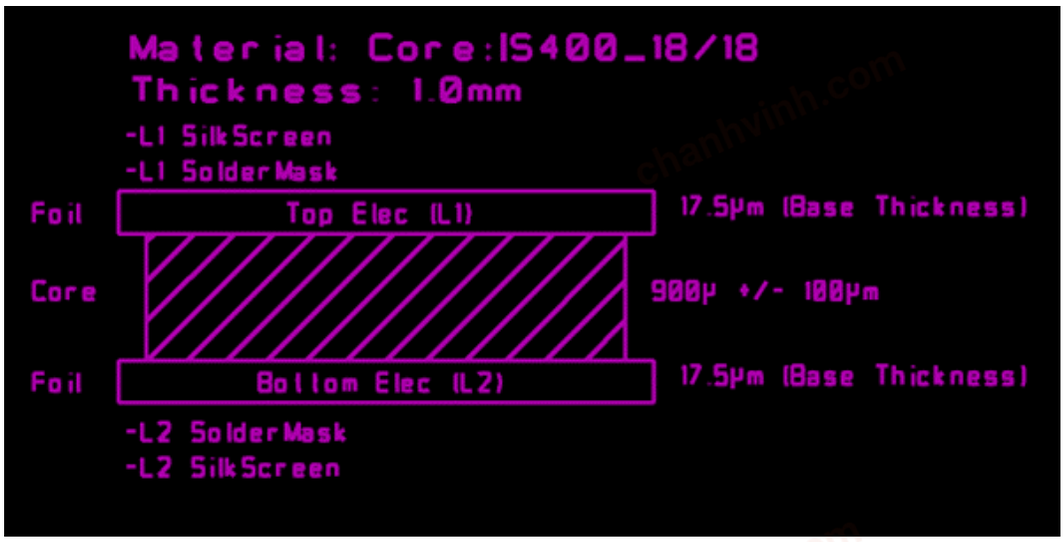
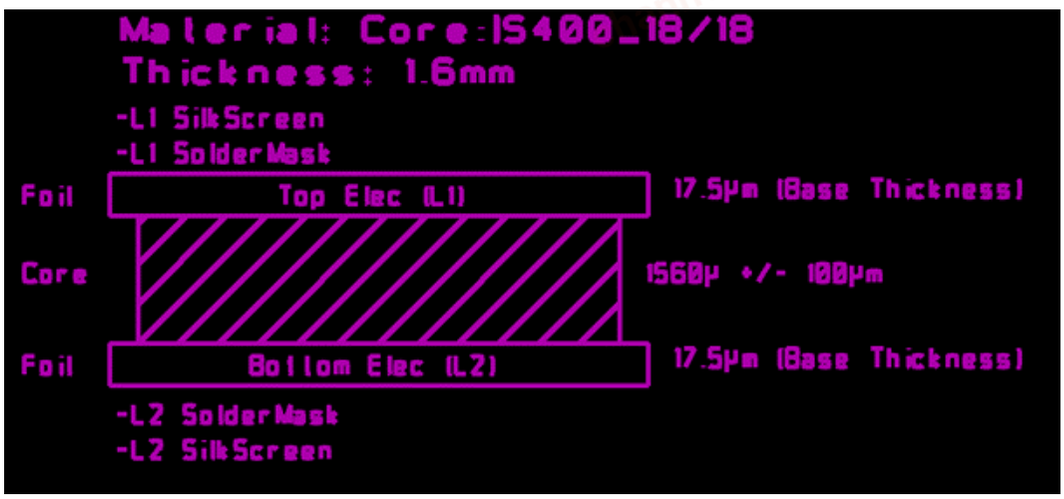


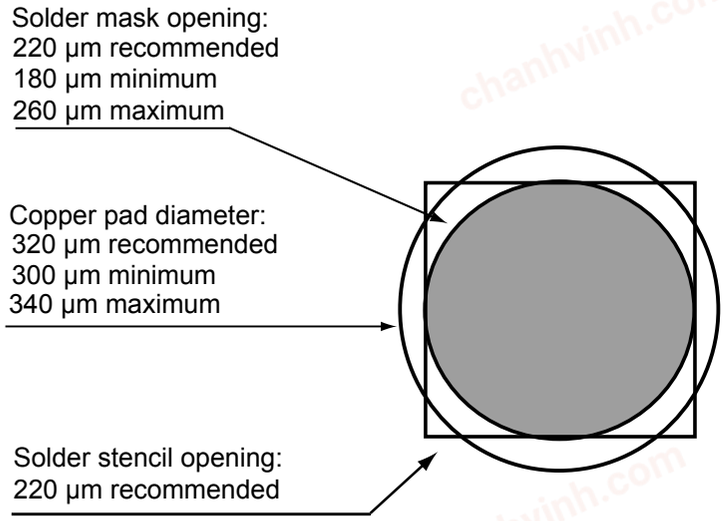
Figure 20. **PCB 1.6 mm stack-up recommendations (FR4 IS400 Er = 3.9)**



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3.2 Stencil opening design

Figure 21. **Footprint - 3 mils stencil - solder mask defined**



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

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3.4 Placement

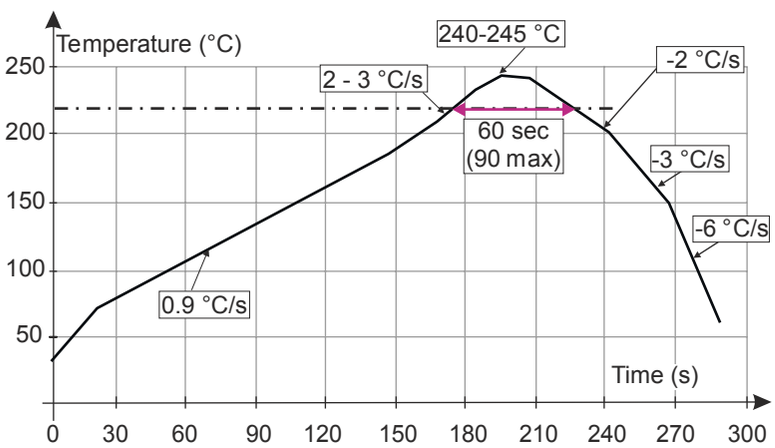
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 22. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: More information is available in the application note:

- *AN2348 Flip-Chip: "Package description and recommendations for use"*

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4 Ordering information

Table 6. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
BALF-SPI2-03D3	UH	Flip-Chip 6 bumps	3.4 mg	5000	Tape and reel

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Revision history

Table 7. **Document revision history**

Date	Revision	Changes
24-Jul-2024	1	Initial release.

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