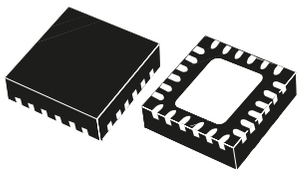
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ALED7709

Datasheet

Automotive LED driver 4-channel 200 mA with a DC-DC controller



QFN24L (5x5 mm)

Product status link
ALED7709

Features

- AEC-Q100 Grade1 qualified
  - Operating temperature range -40 °C < T_J < 150 °C
- 4.5 V to 42 V operating input voltage range
  - Up to 60 V tolerant for load dump @ 24 V battery
  - Supports battery cranking events down to 4 V supply
- Simultaneous or exclusive control by PWMI and I^2C interface
- Switching controller section
  - Low shutdown current: I_{SHDN} < 15 µA
  - Fixed frequency peak current-mode controller
  - Cycle-by-cycle power switch OCP
  - Adjustable (250 kHz to 2.2 MHz) switching frequency with optional spread spectrum
  - Synchronized boost and SEPIC topologies support
  - Line switch control for standby power saving and inrush current protection
  - Input overvoltage and output short-circuit protection
- LED strings control section
  - 4 x 40 V rated constant current outputs
  - Adjustable up to 200 mA per channel
  - ±2 % typ. output current accuracy
  - Mixed PWM and Analog dimming
  - 100 Hz to 12.8 kHz dimming frequency
  - Dimming ratio 10000:1 at 100 Hz
  - LED temperature sensor (NTC) management
  - Selectable channels phase-shifting and adjustable Rise/Fall time for reducing EMI
  - Open channel, LED short-circuit detection
  - Two versions available: ALED7709A and ALED7709B

Applications

- Automotive lighting and backlighting for:
  - Cluster / Infotainment display
  - Head-Up Display (HUD)
  - Instrument lighting system
  - Ambient light

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Description

ALED7709x are automotive-grade (AEC-Q100 Grade1 qualified) LED drivers combining a boost/SEPIC controller and four low-side constant-current sinkers, designed to drive strings of high brightness LEDs. The switching converter section provides the supply rail for the LED strings, whose value is constantly optimized for maximum efficiency. The boost/SEPIC controller supports the external synchronization and spread spectrum. ALED7709x can work simultaneously or exclusively in standalone mode (SAM), controlled only by PWMI signal, and in bus driven mode (BDM) through an I^2C serial interface. The brightness of the four LED strings can be controlled either in global or local mode. In global mode, the ALED7709x supports a mixed PWM and analog dimming to improve the brightness range capability. Only the BDM provides full access to ALED7709x advanced features. PWM dimming frequency can be programmed changing the setting of the internal 16-bit counter, while an internal oscillator avoids the use of an external clock source.

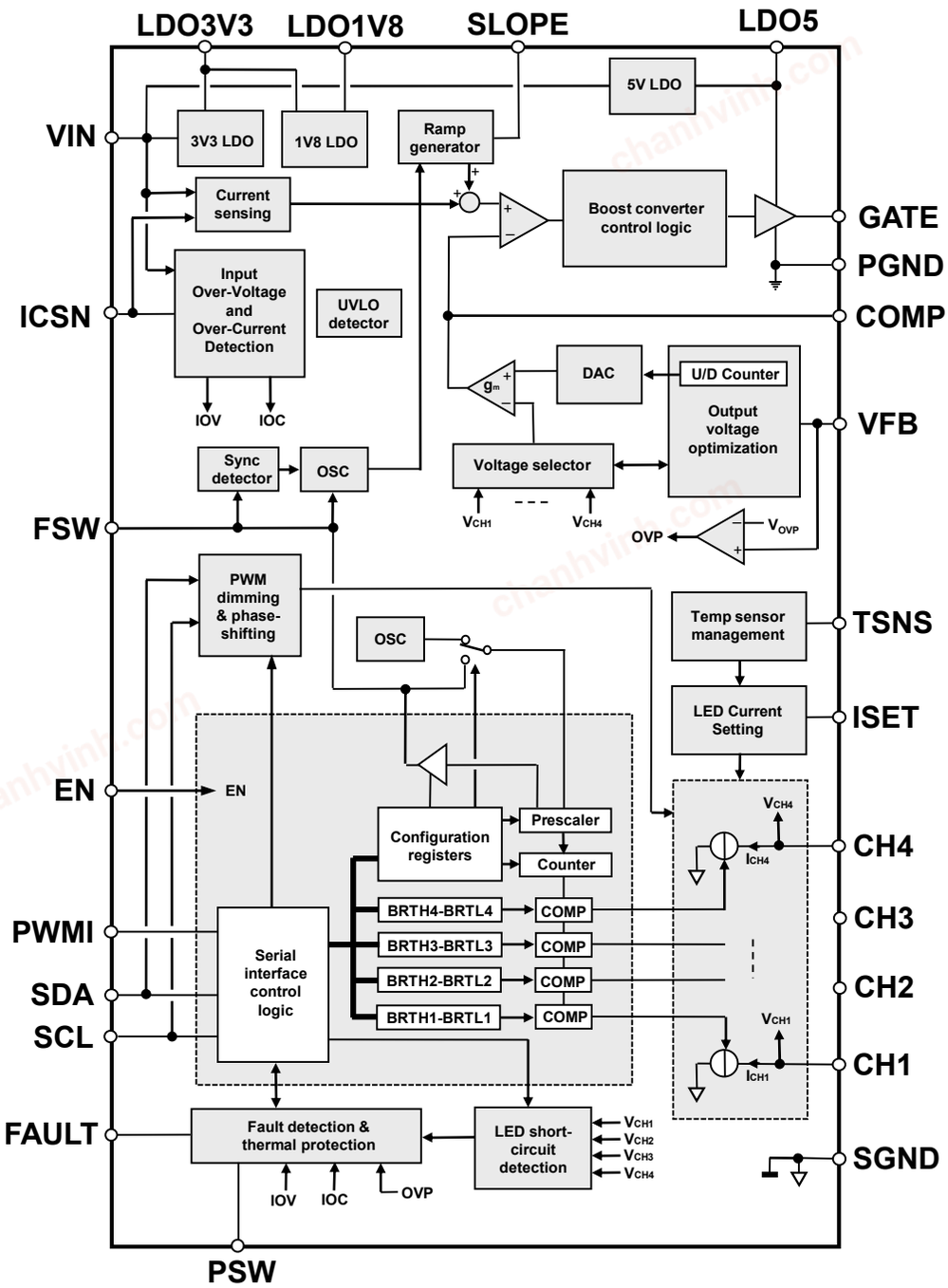
The ALED7709A is dedicated to BDM while ALED7709B is more suitable for SAM. ALED7709x implement basic protections (overvoltage, overcurrent, and thermal shutdown) as well as “Open and Short” LED fault detection, with optional channel auto-disconnect in case of fault.

The devices support an optional P-channel MOSFET in series to the input. It protects the system, LED strings and channels in case of some faulty conditions, output short-to-ground or excessive input voltage transients and it also reduces the power consumption when in standby.

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1 Diagram

Figure 1. **Block diagram**



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2 Pin configuration

The ALED7709x are in QFN24L (5x5 mm), 0.65 mm pitch small package with exposed pad.

Figure 2. Pin connection (top view)

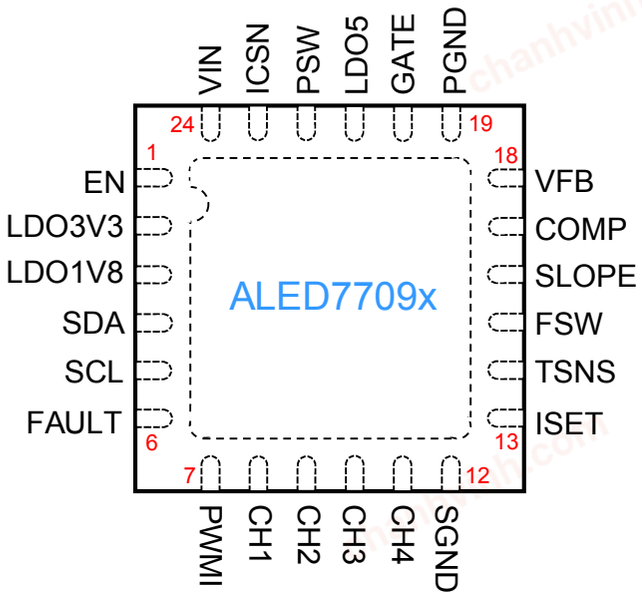


Table 1. Pin description

Pin #	Symbol	Function
1	EN	ENABLE the device and the internal DC-DC converter by using two different thresholds. An internal circuit clamps maximum voltage on the pin, allowing the use of high value pull-up resistor connected to input rail.
2	LDO3V3	3.3 V linear regulator output. Connect a 1 µF bypass capacitor between this pin and SGND as close as possible to the device.
3	LDO1V8	1.8 V linear regulator output. Connect a 1 µF bypass capacitor between this pin and SGND as close as possible to the device.
4	SDA	DATA pin of the I^2C interface
5	SCL	CLOCK pin of the I^2C interface
6	FAULT	This pin is an open-drain and must be connected to SGND through a resistor. It is tied high to report a fault condition.
7	PWMI	PWM/brightness dimming control input.
8	CH1	Output pin to be connected to the negative terminal of the LED string.
9	CH2	Output pin to be connected to the negative terminal of the LED string.
10	CH3	Output pin to be connected to the negative terminal of the LED string.
11	CH4	Output pin to be connected to the negative terminal of the LED string.
12	SGND	Signal and channel ground. All external setting components must refer to this ground pin.
13	ISET	LED current setting pin. Connect a resistor between this pin and SGND to set the full-scale output current.
14	TSNS	External temperature sensor input. Connect to a remote NTC thermistor network to gradually reduce the LED current starting from a desired temperature level. Connect to LDO3V3 in case the function is not used.

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Pin #	Symbol	Function
15	FSW	Switching frequency setting. A resistor between this pin and SGND sets the desired switching frequency. This pin is also the synchronization input using a direct pulse signal.
16	SLOPE	Control loop compensation slope setting. A resistor between this pin and SGND sets the proper amount of compensation slope for the control loop of the DC-DC converter.
17	COMP	DC-DC converter loop compensation. A proper RC filter must be connected between this pin and SGND for loop compensation.
18	VFB	Output voltage feedback input by an external resistor ladder.
19	PGND	Power ground connection. External components of the DC-DC converter must refer to this ground pin.
20	GATE	External power NMOS switch gate driver output.
21	LDO5	5.1 V linear regulator supplies the external power NMOS switch gate driver. Connect a 1 µF bypass capacitor between this pin and PGND as close as possible to the device.
22	PSW	Switch gate control pin for optional external PMOS for system input protection. Can be left floating or connected through a resistor to ICSN pin if unused.
23	ICSN	Input and external power NMOS switch current sensing, negative terminal. Connect this pin to the negative terminal of the input current sensing resistor. The differential voltage between the VIN and ICSN pins is used to sense the current flowing in the DC-DC converter stage and to set the threshold for the overcurrent protection.
24	VIN	Supply voltage input. Place a 1 µF bypass capacitor to ground as close as possible to the device.
-	TPAD	Thermal pad. Connect to a suitable (JESD51-7) copper area (it could or not be electrically connected to ground) for power dissipation improvement.

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3 Typical application circuits

Figure 3. **Example of boost topology application with I²C and PWMI control**

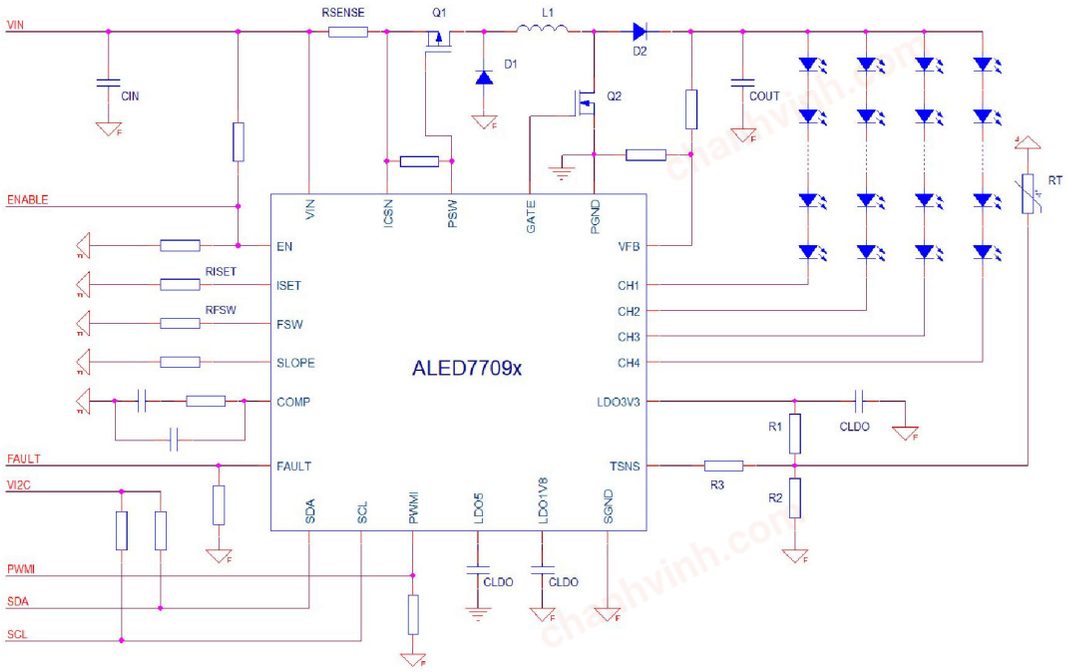


Table 2. **Typical main components for boost application**

Symbol	Value	Description	Note
C_{IN}	2 x 10 µF	GCJ32EC71H106KA01L- Input capacitor	Murata
R_{SENSE}	0.039 Ω	Input sense resistor	2 W
Q_1	STD40P8F6AG	PMOS	ST
D_1	STPS1H100	Diode	ST
L_1	15 µH	XGL1010-153 - inductor	Coilcraft
Q_2	STL8N10LF3	NMOS	ST
D_2	STPS2L60-Y	Diode	ST
C_{OUT}	4 x 10 µF	GRT31CR61H106KE01L - Output capacitor	Murata
C_{LDO}	1 µF	LDOs capacitor	One for each LDO pin
R_{ISET}	6.8 kΩ	I_{OUT} setting	150 mA
R_{FSW}	62 KΩ	Converter oscillator resistor	400 KHz
R_T	NCG18XH103F0SRB	NTC resistor	Murata
R_1	1.8 KΩ	NTC working range setting	T1 = 65 °C T2 = 125 °C
R_2	1.1 KΩ		
R_3	2.0 KΩ		
LED	4 x 10 x KW DPLS34.KD	LEDs	OSRAM

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Figure 4. **Example of simplified SAM application in SEPIC topology**

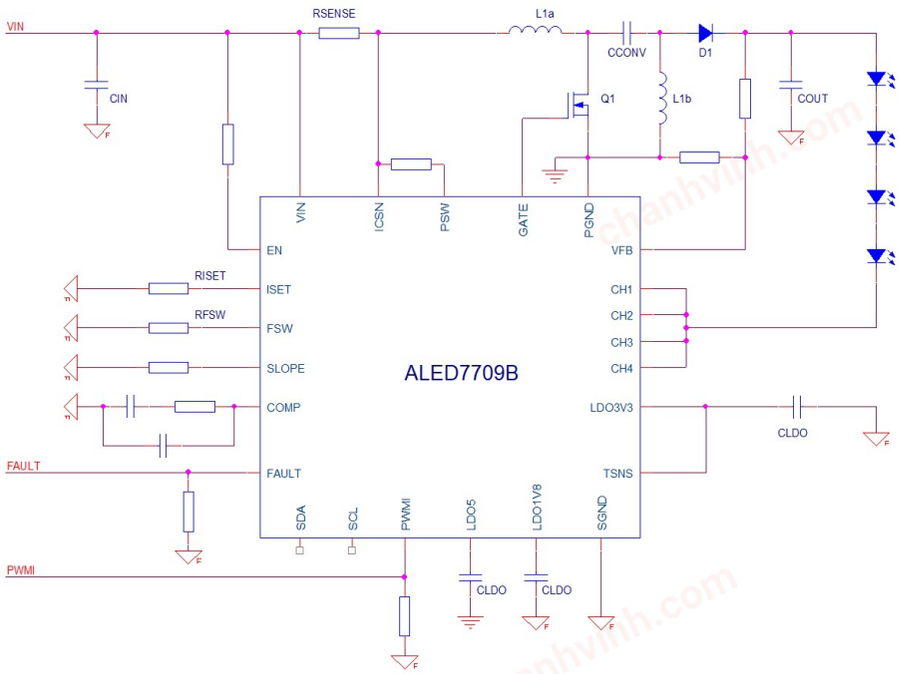


Table 3. **Typical main components for standalone SEPIC application**

Symbol	Value	Description	Note
C_{IN}	10 µF	GCM32EC7YA106KA03 – Input capacitor	Murata
R_{SENSE}	0.082 Ω	Input sense resistor	1 W
L_{1a}	15 µH	MSD1260H-153ME – Coupled inductor	Coilcraft
L_{1b}	15 µH		
C_{CONV}	4.7 µF	GRT32ER71H475KE01 - SEPIC capacitor	Murata
Q_1	STS8N6LF6AG	NMOS	ST
D_1	STPS3L40-Y	Diode	ST
C_{OUT}	2 x 10 µF	GCM32EC71H106KA03 - Output capacitor	Murata
C_{LDO}	1 uF	LDOs capacitor	One for each LDO pin
R_{ISET}	5.83 kΩ	I_{OUT} setting	175 mA
R_{FSW}	62 KΩ	Converter oscillator resistor	400 KHz
LED	4 x KW KW DMLS33.SG	LEDs	OSRAM

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4 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
I_{EN}	Maximum pin supported current	200	uA
VIN, EN, ICSN & PSW to SGND	Maximum pin voltage	-0.3 to 60	V
CH1 through CH4 to SGND		-0.3 to 42	V
FSW, SDA, SCL & PWMI to SGND		-0.3 to 6	V
LDO3V3, VFB, FAULT, COMP, SLOPE, ISET & TSNS to SGND		-0.3 to 4	V
LDO5 & GATE to PGND		-0.3 to 6	V
LDO1V8 to SGND		-0.3 to 2.3	V
PGND to SGND		-0.3 to 0.3	V

Note: Stressing the device above the rating listed in this table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	± 2	kV
		CDM corner pins	± 750	V
		CDM non-corner pins	± 500	

Table 6. Package thermal data

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal resistance junction-ambient	25.4	°C/W
$R_{\theta JC}$	Thermal resistance junction-case	2.2	°C/W
$R_{\theta JB}$	Thermal resistance junction-board	8.3	°C/W
Ψ_{JT}	Thermal parameter junction-top	0.2	°C/W
Ψ_{JB}	Thermal parameter junction-board	8.6	°C/W

Note: Thermal value as defined in standard JESD51-7 on 2s2p board (with 4x4 PCB vias pitch 1 mm).

Table 7. Thermal data, warning and shutdown

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{STG}	Storage temperature range	-55		150	°C
T_J	Operating junction temperature range	-40		150	°C
T_a	Operating ambient temperature	-40		125	°C
T_{OTA}	Overtemperature alert threshold	110	125	145	°C
	Overtemperature alert hysteresis		20		°C

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Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{SHDN}	Thermal shutdown threshold	150	165	180	°C
	Thermal shutdown hysteresis		20		°C

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5 Electrical characteristics

V_{IN} = 12 V, V_{EN} = high, T_J = -40 °C to +125 °C unless otherwise specified.

Table 8. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage	LDO5 as output	4.5		42	V
		LDO5 as input (LDO5 shorted to VIN)	4.5		5.5	
$V_{UVLO,ON}$	Undervoltage lockout upper threshold	V_{IN} rising	3.75	4.0	4.2	V
$V_{UVLO,OFF}$	Undervoltage lockout lower threshold	V_{IN} falling	3.5	3.7	3.9	
$V_{UVLO,HYS}$	Undervoltage lockout hysteresis			0.3		
V_{LDO3V3}	3V3 LDO output voltage		3.2	3.33	3.45	V
V_{LDO1V8}	1V8 LDO output voltage		1.7	1.8	1.87	V
V_{LDO5}	5V LDO output voltage		4.8	5.1	5.35	V
$I_{VIN,SHDN}$	Shutdown current	EN pin < V_{EN1} (shutdown mode)		7	15	µA
$I_{VIN,STBY}$	Standby current	EN pin > V_{EN2}; bit DEN = 0		1.5	3	mA
$I_{VIN,OP}$	Operating current	EN pin > V_{EN2}; bit DEN = 1; CHs & Boost OFF		3	4	
$I_{VIN,ON}$	Full operating current (1)	Boost ON @1 MHz; All CHs ON @100 mA		15		
Enable						
V_{EN1}	Device enable threshold		0.3		0.7	V
V_{EN2}	Converter enable threshold	Rising	1.12	1.22	1.32	
		Falling	0.97	1.07	1.17	
		Hysteresis		0.15		
Converter controller						
F_{SW_int}	Internal switching frequency	FSW[1:0] = 10	CLK_{INT} / 8			Hz
K_{FSW}	Switching frequency constant	R_{FSW} = 24.9 kΩ	23	25	27	MHz * kΩ
F_{SW_adj}	Adjustable switching frequency FSW[1:0] = 00	R_{FSW} = 100 kΩ => K_{FSW} / R_{FSW} = F_{SW}		250		kHz
		R_{FSW} = 12.4 kΩ => K_{FSW} / R_{FSW} = F_{SW}		2016		
	Synchronization signal frequency capture range	$t_{CLK,H}$ = 200 ns, $V_{CLK,L}$ < 0.3 V, $V_{CLK,H}$ > 2.8 V	250		2200	
F_{SWH}	FSW synchronization input high level		2.8			V
F_{SWL}	FSW synchronization input low level				0.3	
$F_{SWPulse}$	Synchronization input high level pulse width		200			ns
$V_{ICSN,PK}$	Power switch max. peak detection threshold	V_{IN} - V_{ICSN}	180	200	220	mV
$DRVR_{_on_HS}$	$R_{_on}$ of high-side driver (1)			2.00		Ω
$DRVR_{_on_LS}$	$R_{_on}$ of low-side driver (1)			1.07		Ω
$t_{SS,max}$	Max. soft-start duration (1) (2)			3.5		ms

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{VFB,max}$	Internal reference voltage for output regulation		1.02	1.08	1.14	V
$V_{VFB,min}$			0.75	0.795	0.84	
$V_{VFB,skip}$	Internal reference voltage to force converter in pulse skip mode		1.03	1.09	1.15	
Current generators						
V_{HRREF}	Minimum headroom voltage across reference channel	R_{ISET} = 5.11 kΩ	0.83	1.1	1.3	V
I_{CH_SETmin}	Output current (3)	R_{ISET} = 40.7 KΩ I_{CH_SET} = 1022 / R_{ISET}		25.1		mA
I_{CH_SETmax}	Output current	R_{ISET} = 5.11 KΩ I_{CH_SET} = 1022 / R_{ISET}		200		
ΔI_{CHn}	Absolute channel accuracy (each channel to nominal value) (4)	R_{ISET} = 10 KΩ 100% dimming and V_{HRCHx} = 1.0 V		±2	±4	%
ΔI_{CHx}	Channel to channel mismatch (each channel to device average value) (5)	R_{ISET} = 10 KΩ 100% dimming and V_{HRCHx} = 1.0 V		±1	±3	%
I_{CHoff}	Output current in OFF mode	EN = High; DEN = 0 V_{HRCHx} = 35 V		0.1	0.5	µA
PWM dimming control						
CLK_{INT}	Internal dimming oscillator frequency		5.9	6.553	7.34	MHz
CLK_{SS}	Spread spectrum of internal oscillator frequency	DCLKMS[1:0] = 00	±3.75	±4.75	±5.0	%
F_{PWM}	Dimming frequency	FDIM[2:0] = 110	CLK_{INT} / (2^10)			Hz
D_{PWM}	Dimming duty-cycle range		0		100	%
t_{PWM_ON}	Output pulse ON-time (1)	PWMx[0x0003]		0.46		µs
F_{PWMI}	PWMI frequency		0.06		14	kHz
$t_{PWMImin}$	PWMI minimum pulse transferred to output	PWMI_DRCT = 1		0.5		µs
V_{PWMIH}	PWMI high level		1.3			V
V_{PWMIL}	PWMI low level				0.5	
PMOS driving						
$I_{PSW,OFF}$	PSW pin leakage current			0.07	1	µA
$I_{PSW,ON}$	PSW pin driving current		80	105	135	
Fault / protection management						
$V_{IN,OVPT-UP}$	Input overvoltage protection upper threshold	V_{IN} rising	36	40	42	V
$V_{IN,OVPT-DW}$	Input overvoltage protection lower threshold	V_{IN} falling	33	37.5	40	
$V_{IN,OVPH}$	Input overvoltage protection hysteresis			2.5		
$V_{ICSN,OCPT}$	Input overcurrent protection threshold	V_{IN} – V_{ICSN}	220	240	260	mV
$V_{VFB,OVPT}$	Output overvoltage protection threshold	Output voltage converter turning OFF threshold on V_{FB}	1.1	1.18	1.26	V
$V_{CHx,FLT}$	LED short-circuit detection threshold		4.6	4.9	5.2	V
V_{FAULTH}	FAULT output high level	R_{FAULT} = 3.3 KΩ	2.9			V
I_{FAULT}	FAULT leakage current				1	µA

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I²C compatible interface						
V_{IH}	High level input voltage		1.3			V
V_{IL}	Low level input voltage				0.5	
V_{OL}	Low level output voltage	I_{TEST} = 5 mA			0.4	
C_{IO}	I/O pins capacitance (1)				10	pF

1. *Not tested in production.*
2. *Overall soft-start duration depends on application.*
3. *The accuracy between the programmed I_{CH} and the output current is not guaranteed for: $I_{CH} < I_{CH_SETmin}$.*
4. $\Delta I_{CHn} = MAX\left(\frac{|I_{CHn} - I_{CHnom}|}{I_{CHnom}}\right)*100$
5. $\Delta I_{CHx} = MAX\left(\frac{|I_{CHx} - I_{CHavg}|}{I_{CHavg}}\right)*100\ ;\ I_{CHavg} = \frac{\sum I_{CHn}}{4}$

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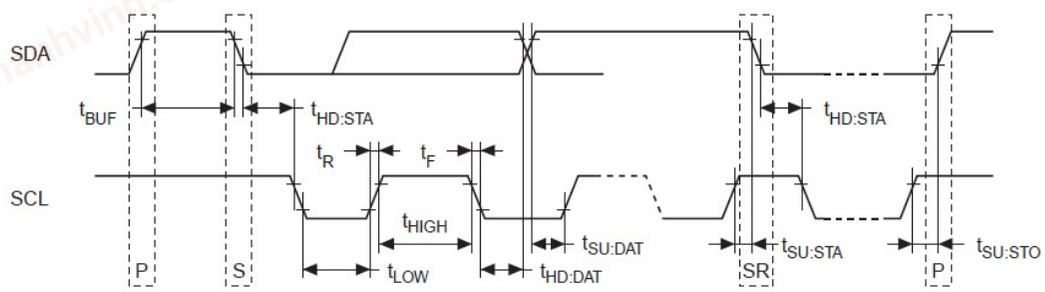
6 I²C switching characteristics

V_{IN} = 12 V, V_{EN} = High, T_A = 25 °C unless otherwise specified.

Table 9. I²C fast-mode switching characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency				400	kHz
t_{LOW}	Minimum clock low period		1.3			µs
t_{HIGH}	Minimum clock high period		600			ns
t_F	SDA and SCL fall time				300	ns
t_R	SDA and SCL rise time				300	ns
$t_{HD:STA}$	Start condition hold time		600			ns
$t_{SU:STA}$	Start condition setup time		600			ns
$t_{SU:DAT}$	Data setup time		100			ns
$t_{HD:DAT}$	Data hold time		0			µs
$t_{SU:STO}$	Stop condition setup time		600			ns
t_{BUF}	Minimum delay between operations		1.3			µs

Figure 5. I²C timing reference



P : STOP
S : START
SR : Repeated START or RESTART

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7 Functional description

7.1 Overview

ALED7709x are LED drivers, which integrate a DC-DC converter controller and four high precision constant-current sinkers. They have been specifically designed to work controlled by an MCU through an I^2C Bus and/or by a control signal applied on the PWMI pin. For both ALED7709A and ALED7709B, the two control methods are not mutually exclusive, either or both can be used.

ALED7709x can drive four strings of LEDs connected in series with high efficiency and flexible brightness control. The devices can support both boost and SEPIC topologies to cover most applications.

The DC-DC converter architecture is based on a constant peak current control; it has a specific adaptive output voltage regulation to reduce the internal power dissipation. An adaptive algorithm manages the DC-DC converter reference voltage looking at the CHs minimum voltage needed to guarantee the sinkers current regulation.

The brightness of the LED strings can be adjusted in two manners:

1. **Global**: all the outputs are driven to the same brightness level allowing mixed PWM and current dimming; this is also possible by driving the device through PWMI signal only.
2. **Local**: the PWM and current adjustments are independent for each channel; this mode is possible through I^2C register setting only.

Phase-shifting function (interleaved operation of the output channels) and edge control (rise and fall time adjustment), are useful to reduce EMI and audible noise.

7.2 Device supply

ALED7709x have a power tree composed by three different linear voltage regulators.

A 3V3 low-dropout linear regulator (LDO3V3), which supplies the analog circuitry of the chip; it is the master enabler of the device.

A 1V8 low-dropout linear regulator (LDO1V8), supplied by 3V3 LDO, powers the digital circuitry of the chip.

A 5.1 V low-dropout linear regulator (LDO5), supplied directly by V_{IN}, is dedicated to supply the gate driver of the external power MOS for the DC-DC converter.

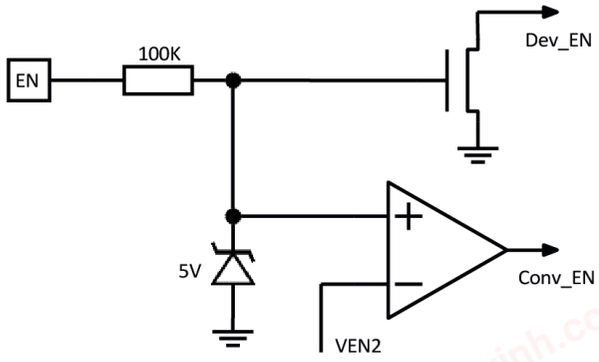
All LDOs are protected against short circuit, nevertheless it is not suggested to use them for supplying external circuitry. LDO3V3 can be used for I^2C pull-ups and reference NTC resistor ladders.

An undervoltage lockout (UVLO) protection is connected on LDO5 output to control the complete power tree: in case the input voltage on V_{IN} pin is below the value to guarantee the proper power supply levels, the device is blocked and therefore disabled to work.

EN pin is the device enabler. It has a main threshold that brings the device in/out from shutdown.

Above this threshold LDO3V3 goes ON and activates the rest of the power tree; below it is turned OFF and, as consequence, the device enters in Shutdown setting at minimum the quiescent current; the volatile registers are not kept and I^2C communication is disabled.

Figure 6. Enable pin circuit



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The second threshold of EN pin enables the DC-DC converter stage and sinkers activity.

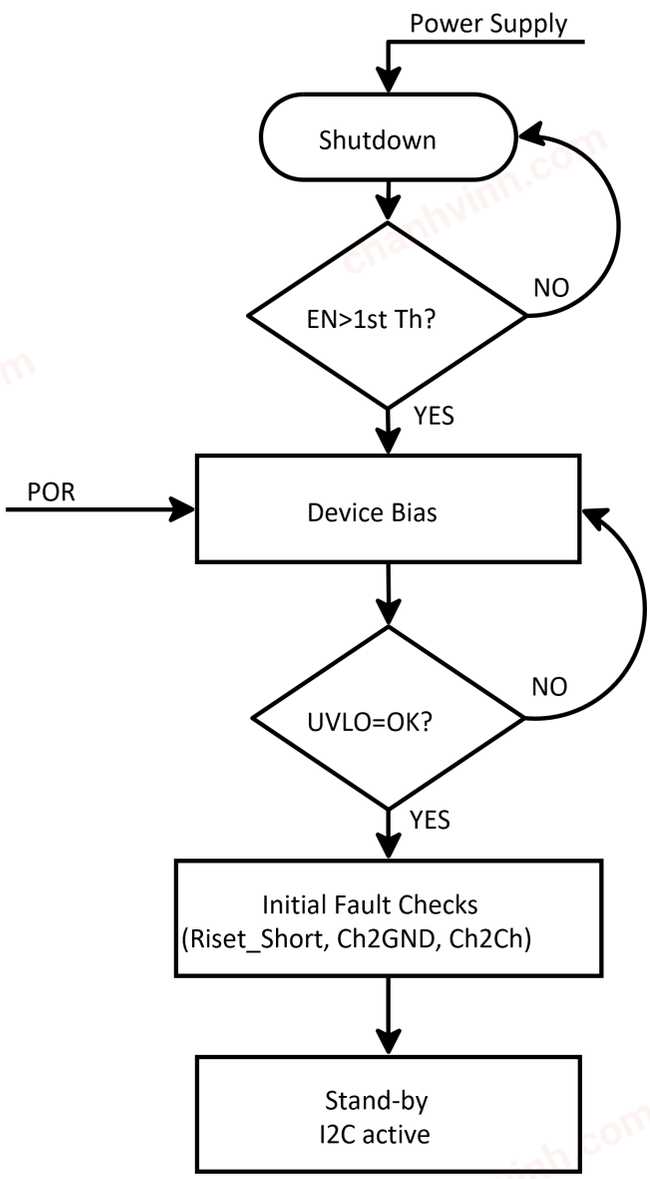
Properly setting a resistor divider connected to V_{IN}, it is possible to disable the DC-DC converter and channels when V_{IN} goes below a defined value. If the voltage on EN pin goes below the second threshold but stays above the main one, the rest of the device remains ON, keeping the content of volatile registers and I^2C communication active, being ready to restart from the previously programmed condition as soon as EN pin rises above V_{EN2}.

When EN pin voltage is high, the device exits from shutdown and enters in standby; in this condition, the I^2C communication is active, and the volatile register content is kept. To move from standby to operative mode, DEN bit must be set to high.

There is a 5 V clamp, for internal circuit protection, connected on EN pin through a 100 kΩ resistor, to avoid any unnecessary current flowing inside the pin it is suggested to keep V_{EN} below 4.5 V. Anyway, it is possible to connect EN pin to a higher voltage but taking care to limit the max. current below 200 µA.

As soon as the Power-on Reset (PoR) is released ALED7709x check the initial fault; after that ALED7709A enters in standby enabling also the I^2C communication, while ALED7709B enters directly in operation mode.

Figure 7. Startup sequence for ALED7709A



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7.3 Initial fault check

ALED7709x perform a specific fault verification each time the device exits from shutdown and before the first turn ON, to avoid any system malfunction if:

- R_{Iset} resistance is short-to-ground,
- channels are short-to-ground,
- adjacent channels are short among them (ALED7709A only).

Such tests cannot be executed on demand and during operating mode are no longer active.

The user can overtake any condition of initial fault and force anyway the device to start, only acting on both CLRF and DEN bits through I^2C communication (write 0x81 to register DEVEN).

Before performing this action, which could be potentially dangerous for the system, it is suggested to read the INITSTA register and decide whether the detected fault is manageable or not.

7.3.1 R_{Iset} short

5.11 KΩ is the minimum operative value of R_{Iset} that corresponds to a maximum I_{CH} current of 200 mA.

If R_{ISET} is, for any reason, short-to-ground, ALED7709x enter a non-linear zone and drive an unknown current in the LED strings. A current that could be higher than the safe limit of LEDs.

To avoid such phenomena, each time the ALED7709x exit from shutdown, it checks the status of R_{Iset}; if it is found shorted-to-ground the devices stop in standby mode. ALED7709B does not reach the operational mode.

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7.3.2 CH to GND

This function detects if one or more channels are shorted-to-ground.

This test is performed only during initial fault verification when all channels and DC-DC converter are OFF.

This function prevents extra current from flowing into LED strings in case of accidental short-circuit from any channel to ground.

7.3.3 CH to CH short (ALED7709A only)

This function detects if adjacent channels are shorted together and it is performed among: CH0-CH1, CH1-CH2 and CH2-CH3.

The validity of the output of this test relies on the fact that it is fulfilled at the beginning of the startup sequence when all channels and DC-DC converter are OFF, under this condition it is expected to have Vboost close to ground. If this is not the case, and the startup begins when Vboost still has a residual voltage, enough to allow a current flowing in the LED string, the test could give false result.

7.4 Fault detection

As soon as ALED7709x exit from standby, they execute various steps to reach operation mode; at each step, different fault detections are activated and kept running during operation mode as well.

7.4.1 V_{IN}_OVP by external PMOS

This circuit prevents damage to the output stage when input voltage rises above 40 V.

In boost configuration, to avoid a direct path from V_{IN} to the DC-DC converter out, a PMOS in series to the coil is needed.

If the fault is detected, the PMOS is immediately switched OFF to disconnect OUT from IN.

When the fault occurs, the device enters auto-recovery mode by trying to recover continuously from fault; if V_{IN} remains above the falling threshold, the device does not switch ON PMOS to keep the system safe. If the fault is removed/resolved, the device restarts from the soft-start procedure to return in operative mode.

In auto-recovery mode, the I^2C communication is active, therefore internal registers can be read and written.

If the DEN bit is reset to 0, the device moves from recovery mode to standby mode.

This fault, when it occurs, is latched in the IOVP bit and externally signalized by the FAULT pin, if not masked.

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7.4.2 V_{IN}_OCP and V_{OUT}_OCP by external PMOS

This circuit prevents input current from going higher than the limit imposed by the used external components.

It also protects the system in case of overcurrent due to the DC-DC converter output short-to-ground. To protect the circuitry from the short, the PMOS turn-OFF is executed very quickly. When the fault occurs, the device enters auto-recovery mode; the fault is latched in the IOCP bit and externally signalized through the FAULT pin, if not masked.

7.4.3 V_{IN}_UVLO

When V_{IN} is too low to have VLDO5 above the $V_{UVLO, ON}$ threshold, the device is blocked and communication is disabled. Once running, V_{IN} must fall down enough to bring VLDO5 below $V_{UVLO, OFF}$ to stop the operation.

7.4.4 Thermal shutdown

This fault is detected when the device temperature is higher than T_{SHDN}.

When this fault is detected, the devices immediately turn OFF the DC-DC converter and then, after a delay that depends on PWM output frame duration, all the channels are also turned OFF.

The devices restart automatically when the temperature is reduced by the thermal hysteresis value. This fault, when it occurs, is latched in the THSD bit, and externally communicated through the FAULT pin, if not masked.

7.4.4.1 Over temperature early alert indicator

This warning is issued when device temperature increases above T_{OTA}.

When this event is detected the OTEA bit is latched and externally signalized by FAULT pin, if not masked.

The devices do not move to shut down as consequence of this alert.

7.4.5 V_{OUT}_OVP

This circuitry prevents DC-DC converter output voltage from rising over 42 V. As soon as OVP is detected the DC-DC converter section is switched OFF.

This function is obtained monitoring the VFB pin voltage; V_{OUT}_OVP is triggered when V_{FB} reaches $V_{VFB,OVPT}$.

The VFB pin is internally protected from any accidental low-side resistor disconnection.

If this fault occurs, the OOVP bit is latched and signalized by the FAULT pin, if not masked.

7.4.6 Channel fault detection

The ALED7709x implement both open and short LED detection.

Setting the auto-disconnection bits (OCAD for open LED and SCAD for short LED) the failing channel is properly disabled, clearing the respective CENx bit, only when the adaptive loop is active (OVRE bit to 1).

If the OCAD and SCAD bits are reset, the faulty channel is always signaled but it remains enabled and connected, potentially affecting the adaptive loop.

Channel fault detection is active if the channels are ON for a period longer than 32 main clocks (about 5 µs).

7.4.6.1 Open LED

The detection of open LED fault is fulfilled by sensing the headroom voltage versus an internal reference. To confirm the fault, a specific algorithm has been implemented to identify real open LED fault from false detection due to some dynamic transitions.

When an open LED event is detected by the open LED comparator, it is not immediately reported as a fault.

An LED open path forces the headroom voltage to fall, and the adaptive control provides the UP signal to allow V_{OUT} to rise. If the open LED information is confirmed when the DAC reaches the reference value, the FAULT is managed according to the device configuration.

If during the V_{OUT} rising the open LED information from the comparator disappears, the open LED fault interrupt is not generated and the V_{OUT} is frozen or moves down to the target value according to a new adaptive phase. If confirmed, the open LED fault is latched to the LEDF bit and the faulty channel is reported by the OPx bit, and the fault indication is exported to the FAULT pin, if not masked.

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7.4.6.2 *Short LED*

In the case of LED short-circuit, the drop across the LED string is reduced and the voltage in excess remains on the output channel.

The ALED7709x compare the headroom voltage with the reference, and when it is higher the fault is immediately latched on the LEDF bit and on SHx to identify the faulty channel. The fault indication is also exported to the FAULT pin, if not masked.

7.5 Line switch P-MOS control

The ALED7709x have a line switch control circuit, which can drive an optional P-channel MOSFET placed in series to the input. In this manner the LED strings, channels, and DC-DC converter are protected in case of faulty conditions output short-circuit to ground or input voltage transient above 40 V. The switch control circuit is also helpful to reduce the power consumption in standby.

The line switch control senses the input voltage level on the V_{IN} pin and the current drawn from V_{IN} checking the voltage across the R_{SNS} on the ICSN pin.

PSW pin is the gate driver of the external PMOS, it provides a controlled current, which generates, across a resistor, an appropriate VGS to keep the PMOS active during the normal operation.

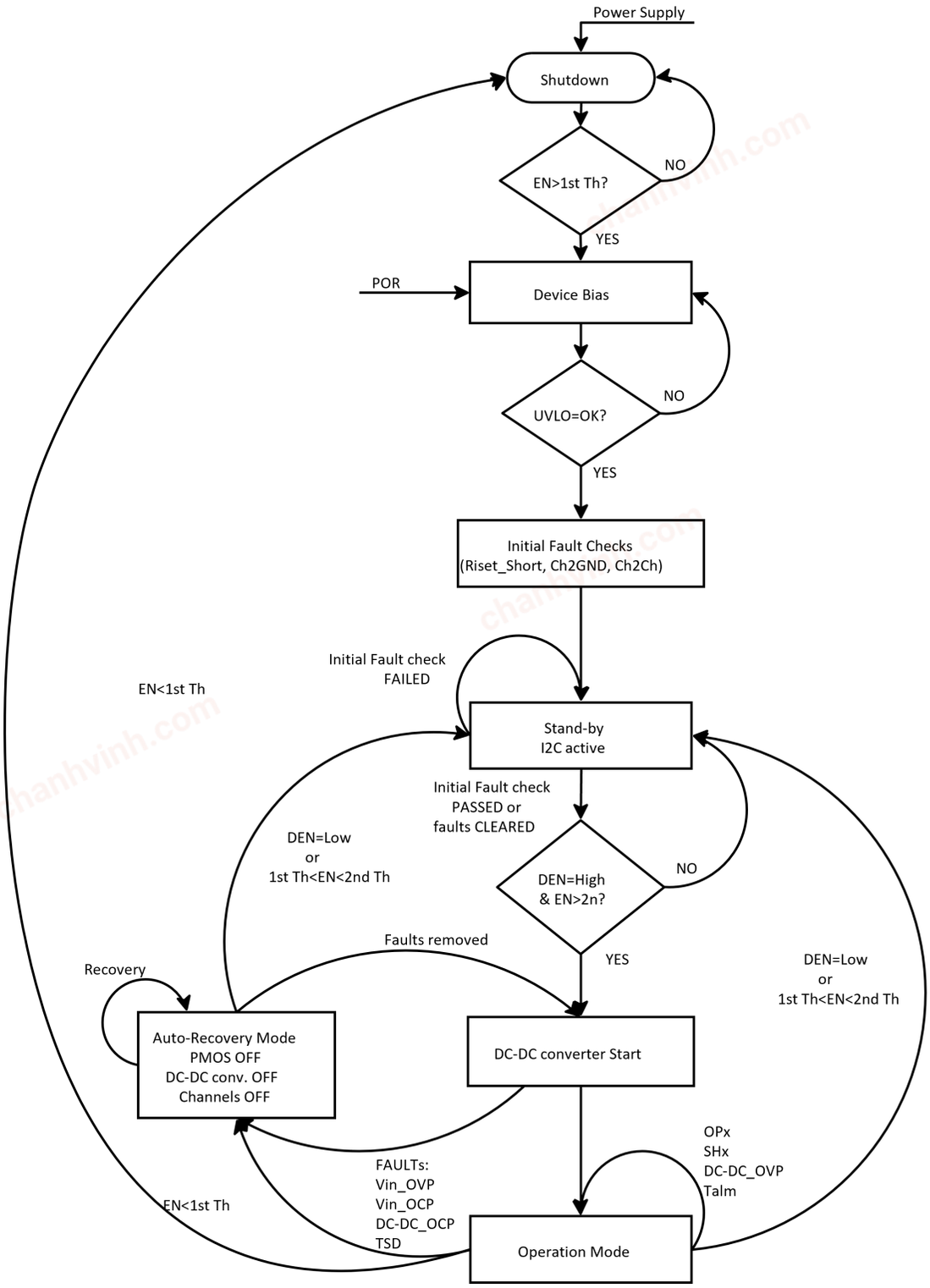
As soon as a critical fault is detected and auto-recovery mode is activated, the line switch circuit immediately sets the external PMOS OFF to protect the following circuits and a new startup sequence is activated. If the fault continues, the auto-recovery mode remains active repeating the PMOS OFF and new startup; as soon as the fault is solved, the startup goes to the end driving the device to normal operational mode.

In standby (bit DEN = 0) the PMOS is kept OFF to avoid any possible current leakage in boost and LED strings.

Since the external PMOS is optional, the line switch control circuit can be disabled through the LSWE bit. Disabling this circuit, the Input OVP and OCPs are no longer active.

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Figure 8. **Complete working flow**



7.6 Device shutdown and standby

The ALED7709x can be shut down by lowering the EN pin below the V_{EN1} threshold at any time.

However, when the device is controlled through the serial interface, there is also the possibility to act on DEN bit in the main configuration register (DEVCFG); this brings the device in standby preserving the content of the registers. This should be the simplest way to control the device unless further power consumption reduction is necessary.

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7.7 DC-DC converter controller section and output voltage optimization

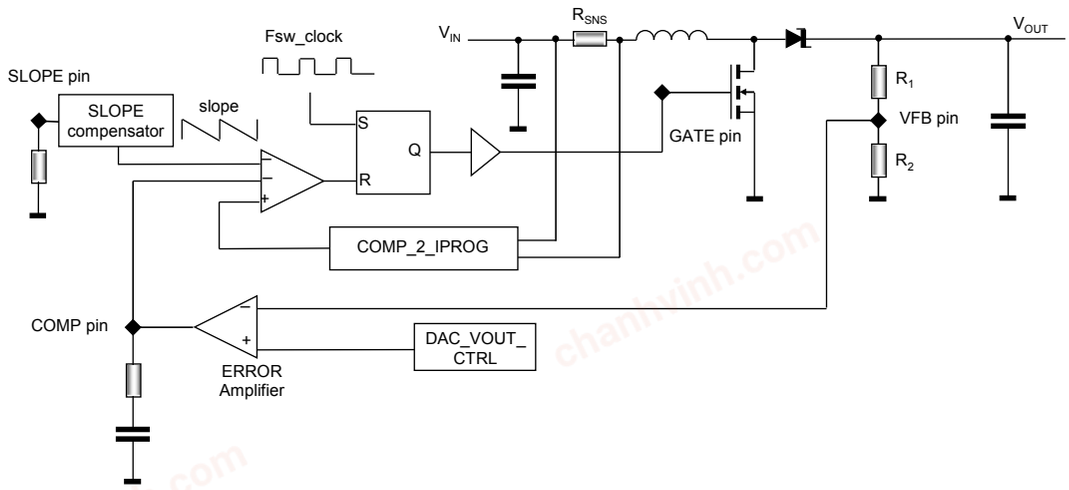
The purpose of this macro-block is to convert the input voltage to the needed output voltage using the peak-current mode as control loop.

The output voltage is sensed by an external resistor voltage divider, whose output is connected to the VFB (feedback) pin; the target value is set providing to a transconductance amplifier (Error Amplifier) a reference voltage generated by a 7-bit DAC.

The current generated by this block is proportional to the output voltage error and it is sent to an external compensation network, mainly composed by an RC series, connected on the COMP pin.

The voltage of this pin is then used as a reference to set the peak current of the external inductor to control the “closed loop”.

Figure 9. Converter stage circuitry



Each switching cycle starts with the FSW clock rising edge, which triggers the gate driver of the external NMOS; it starts a $t_{ON,min}$ pulse during which the turning-off of the gate driver is not allowed.

This masking time has a double function:

- to avoid a too short ON pulse that is potentially dangerous for the circuits
- to avoid wrong current readings from current sensors due to the noise generated during transitions

The current flowing through the external inductor L is sensed by reading the voltage drop across the sense resistor R_{SNS} connected in series with the inductor itself.

To avoid intrinsic instability present in the current loop of the current mode control, it’s mandatory to add to the information coming from the current sensing (the voltage drop across external sense resistor) an extra ramp whose slope should be equal to that of current sensed during t_{OFF}. Slope can be set by an external resistor on the SLOPE pin.

When the sum of the current sense voltage and the compensation ramp meets the threshold proportional to COMP pin voltage, the NMOS driver is turned OFF and the inductor current starts flowing through the external diode toward the load.

The overall DC-DC converter functions of the ALED7709x consist of:

- Fixed-frequency current-mode controller
- Output voltage optimization loop
- External MOSFET gate driver
- Related protection circuitry

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7.7.1 Fixed-frequency current-mode controller main blocks

7.7.1.1 *DAC_VOUT_CTRL*

This block is a 7-bit digital to analog converter whose main purpose is to provide the voltage reference to the converter block for optimizing V_{OUT}.

From this block are derived also three thresholds for specific actions:

- output overvoltage: if this threshold is reached on the VFB pin, a fault is generated and the converter is switched OFF ($V_{VFB,OVPT}$ = 1.18 V)
- skip mode: for VFB pin voltage slightly higher than $V_{VFB,SKIP}$ = 1.09 V, the converter enters in skip mode to avoid reaching the overvoltage protection threshold
- open fault: it is the value to be reached on VFB pin before getting an open channel fault recognition ($V_{VFB,OD}$ = 1.03 V)

In normal operational mode, the 7-bit addresses 128 voltage steps, the minimum voltage step is 2.244 mV granting a range of 285 mV between the $V_{DAC,min}$ of 0.795 V to the $V_{DAC,max}$ of 1.08 V.

Table 10. Converter reference voltages

$V_{DAC,max}$ [V]	$V_{DAC,min}$ [V]	$V_{VFB,OD}$ [V]	$V_{VFB,SKIP}$ [V]	$V_{VFB,OVPT}$ [V]
1.08	0.795	1.03	1.09	1.18

7.7.1.2 *Error amplifier and COMP pin*

The error amplifier is a transconductance amplifier, with a typical Gain of 600 µS, that generates a current proportional to the error between DC-DC converter voltage reference (V_{DAC} output) and feedback voltage (V_{VFB}) on the VFB pin.

If the error amplifier tries to drive the COMP pin below 0.725 V, a SKIP signal is asserted to stop switching activity preventing the output voltage to diverge.

To avoid the COMP pin voltage going above its maximum limit of 1.9 V, a sink current clamp is present.

The reference value of this clamp is gradually increased during the soft-start, allowing a progressive current control.

The stability of this block is granted only if a resistor in series to a compensation capacitor is connected on the COMP pin.

7.7.1.3 *COMP_2_IPROG and peak current comparator*

This block is the core of the DC-DC converter control since it is responsible for controlling the peak current flowing into the coil and, as a consequence, controlling the output power.

The COMP_2_IPROG block manages the voltage V_{IN}-V_{CSNS} = R_{SNS}*I_L.

The COMP pin voltage is buffered with a typical gain of 0.29167 and then it is modulated by SLOPE compensation and compared to the voltage drop on R_{SNS}, which is directly proportional to the coil current I_L.

The above-described voltages are the inputs of the peak current comparator that is the sub-block used to turn OFF the converter PWM cycle-by-cycle.

The peak current comparator is very fast and sensitive because input voltage could be of few tenths of mV.

There are a couple of thresholds, 200 mV and 240 mV, to have a better circuit protection.

These two thresholds are used for cycle-by-cycle current limitation and for overcurrent protection, the latter causes a fault and then opening the external PMOS, if present.

7.7.1.4 *Slope compensator*

The constant frequency, peak current-mode topology has the advantage of very easy loop compensation with output ceramic caps (reduced cost and size of the application), and fast transient response. In addition, the intrinsic peak current measurement simplifies the current limit protection, avoiding undesired saturation of the inductor. However, this topology has a drawback: there is inherent open loop instability when operating with a duty-cycle greater than 0.5. This phenomenon is known as “sub-harmonic instability” and can be avoided by adding an external ramp to the one coming from the sensed current. This compensating technique, based on the additional ramp, is called “slope compensation”.

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The slope compensator generates a correction ramp set by a resistor connected to the SLOPE pin; such ramp modulates the COMP pin voltage before to comparing it with the one present on the sensing resistor (R_{SNS}).

To avoid sub-harmonic instability, the compensating slope should be greater than one-half of the slope of the inductor current during the OFF phase when the duty-cycle is greater than 50%. For an effective compensation, the value of R_{SLOPE} can be defined according to the following formula, for boost case:

$$R_{SLOPE} \leq K_S \cdot K_{FS} \cdot \frac{L}{(V_{OUTmax} - V_{INmin}) \cdot R_{SNS}} \quad \Omega \tag{1}$$

and with the following formula for SEPIC case:

$$R_{SLOPE} \leq K_S \cdot K_{FS} \cdot \frac{L}{K_{FS} \cdot V_{OUTmax} \cdot R_{SNS}} \quad \Omega \tag{2}$$

Where: V_{OUTmax} is the maximum output voltage set by resistor divider; V_{INmin} is the minimum voltage for which the converter is enabled to work; K_{FS} = 1.4 is an extra margin for a robust calculation; K_S = 5.833*10^9 [Ω*V/s] is the SLOPE coefficient derived from the internal circuit implementation.

7.7.2 Device turning-on and soft-start sequence

As soon as the DEN bit is asserted, the ALED7709A executes the soft-start steps.

The ALED7709B executes the soft-start steps as soon as the EN pin is released since DEN is asserted at POR. For both devices, the soft-start sequence is the same.

If no critical faults have been detected, the DC-DC converter starts switching with a frequency 25% of the nominal value and current limit set at 20% of nominal level. Converter switching frequency and current limitation are increased according to specific steps until their nominal values.

This sequence is assumed to be concluded when the output voltage reaches the target level of skip mode; the switching frequency and the current limit are released to their respective nominal values and the channels are enabled according to their own enable setting.

Once the channels are enabled, the operating point (voltage and current) of all active channels is monitored and used as feedback to minimize the output voltage for maximum efficiency.

In practice, the internal DAC, in charge of providing the reference voltage to the control loop, starts rolling down as soon as a valid dimming is applied.

The output voltage optimization can only be performed when at least one channel is active, and all the active channels have an ON-time longer than 48 master clock cycles.

7.7.3 DC-DC converter working frequency

The working frequency of DC-DC converter, F_{SW}, can be selected either from local oscillator or from internal main clock.

The selection is done through FSW[1:0] bits in register BOOSTCFG (refer to Section 8.3.8).

When the local oscillator is chosen (FSW[1:0]=00, which is the POR value of ALED7709B), the value of F_{SW}, in MHz,is defined by the external resistor R_{FSW}, in KΩ, by the following formula:

F_{SW} = 25 / R_{FSW}

Local oscillator has a dedicated spread spectrum capability; spread spectrum, which is active by default, can be disabled setting to 1 DFSW_DIS bit.

The internal spread spectrum circuit changes the switching frequency in a range of ±5%.

$$\Delta F_{SW} = 5\% \cdot F_{sw} \tag{3}$$

The device updates the frequency every clock period by fixed steps:

- Ramps up in 63 steps from minimum to maximum F_{SW}.
- Ramps down in 64 steps from maximum to minimum F_{SW}

The modulation shape is almost triangular with a frequency of

$$F_{Spr} = \frac{F_{sw}}{127} \tag{4}$$

Local oscillator can be directly synchronized, within the working range, by an external signal

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There is the possibility to use the DC-DC converter frequency F_{SW} derived from the main clock of ALED7709A, the value depends on the FSW[1:0] setting (refer to Section 8.3.8).

Under this configuration, the spread spectrum modulation of F_{SW} is a direct consequence of depth and speed applied to the main clock, configured by DCLKMS[1:0] bits and enabled/disabled by DCLK_DIS bit available in BOOSTCFG register.

When F_{SW} is derived from main clock the synchronization is not possible; the resistor connected to FSW pin is not necessary, the pin could be left floating or, better, connected to LDO3V3 to inhibit the local oscillator.

7.7.4 Output voltage optimization and control

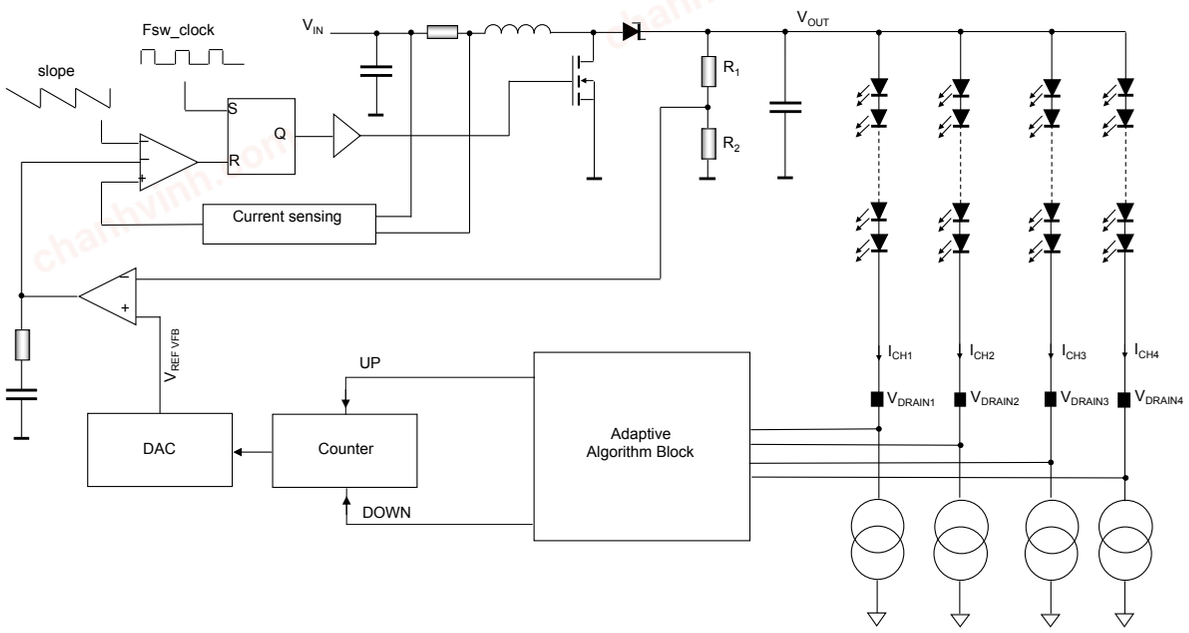
The output voltage of the DC-DC converter section, which is the supply rail for the LED strings, is regulated in an adaptive way to improve the overall system efficiency.

A dedicated Digital to Analog Converter (DAC) sets the reference voltage of the control loop; value is defined to set the output voltage enough to guarantee the required current but also to keep the power dissipation of the LED driving section to the minimum level.

This optimization is performed by keeping the voltage of the leading channel, the one with lower V_{DRAIN}, over the headroom reference voltage (V_{HRREF}) which is an absolute value internally defined and dependent from $I_{OUT,max}$ current set by R_{ISET}.

The V_{HRREF} includes an additional margin from the absolute minimum value that brings the I_{LED} current out of regulation, this to avoid any current variation in the channels due to the dynamic variation of V_{OUT}.

Figure 10. Simplified V_{OUT} regulation circuitry



During normal operation, the status of all the channels is checked and the information is transferred to a proprietary algorithm, a mixed analog-digital solution, to optimize the V_{OUT}.

The ideal target is to have all the V_{DRAIN} between V_{HRREF} and $V_{HRREF,H}$ (an hysteresis window of about 200 mV), but in reality it is the leading channel to take stronger control of the V_{OUT} adjustment to get itself inside the window.

- if a channel has a V_{DRAIN} voltage higher than the reference $V_{HRREF,H}$ the algorithm records it; if during a PWM period all the active channels are in agreement, the system counts DOWN to reduce V_{OUT}, until the leading channel V_{DRAIN} crosses $V_{HRREF,H}$ and it is no longer in agreement with other channels:
  - V_{OUT} going DOWN up to CHx_V_{DRAIN} < $V_{HRREF,H}$

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- if the leading channel has the voltage drop lower than the reference V_{HRREF}, the system immediately counts UP to increase V_{OUT} until V_{DRAIN} crosses V_{HRREF}:
  - V_{OUT} going UP up to CHx_V_{DRAIN} > V_{HRREF}

The DC-DC converter block is always active regardless of how many channels are active (that is, even if all channels are OFF) to improve the load transient dynamic response.

The output voltage regulation can be enabled/disabled (OVRE bit) allowing the user to perform the optimization continuously or on demand.

In real applications, the spread of the forward voltage of the LEDs may lead the channels to have different headroom voltages; in any case, the leading channel (that is, the channel requiring the highest voltage to drive its LED string) is the one that determines the V_{OUT} for all the strings.

The adaptive algorithm works properly if all the channels have an ON-time longer than 10 µs. If at least one channel is set with an ON-time shorter but longer than 5 µs, the adaptive loop can only rise the voltage, while if all the channels have an ON-time shorter than 5 µs, the ALED7709x keep the V_{OUT} constant, like having set the OVRE bit to 0.

OFF channels are kept out from the control algorithm, so the algorithm stays active up to when at least one channel is ON while enters in freeze mode if all the channels are OFF.

The reference voltage, provided by the internal DAC driven by the UP/DOWN counter, spans between the minimum and maximum values; as a consequence, the output voltage can be adjusted by the device in the following range:

$$V_{OUT,min} = \left(\frac{R_1 + R_2}{R_2}\right) * V_{DAC,min} \quad (5)$$

$$V_{OUT,max} = \left(\frac{R_1 + R_2}{R_2}\right) * V_{DAC,max} \quad (6)$$

Where R_1 and R_2 are the high-side and low-side resistors of the divider connected to the output rail and V_{DAC} is the voltage expected at the VFB pin.

It must be ensured that $V_{OUT,min}$ and $V_{OUT,max}$ are below the minimum and above the maximum needed working output voltage to guarantee enough steering room for the optimization. In addition, the temperature of the LEDs significantly affects their forward voltage, which must be considered mainly when calculating the minimum expected output voltage.

The best way to proceed, when designing the external components, is to determine the output voltage range required by the LED strings, considering V_F spread and temperature variation:

$$V_{LED} = \max_{1 \le strings \le N} \left(\sum_{j=1}^{m_{LEDS}} V_{F,j} \right) \quad (7)$$

calculate the output divider through the following equations:

$$\frac{V_{OUT,max}}{R_1 + R_2} \le 300\,\mu A \quad (8)$$

The first is to choose the resistors to limit the current drawn from the output rail. Automotive applications could require a maximum resistance value (e.g., 100 kΩ) for all setting resistors to avoid the risk of significant changes due to moisture. If for this reason, it is not possible to reach a current lower than 300 µA, set R_1 to 100 kΩ and calculate R_2:

$$R_2 = \frac{V_{DAC}}{V_{OUT} - V_{DAC}} \cdot R_1 \quad (9)$$

7.7.4.1 *Voltage optimization vs. PWM and phase shift*

Adaptive control takes care of the information on each active channel V_{DRAIN}. Disabled channels or channels temporarily in the “OFF” phase, because of PWM control, must be excluded from the V_{DRAIN} MIN evaluation. The Phase Shift option further complicates the scenario for the final V_{DRAIN} MIN selection.

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In practice, the V_{DRAIN} MIN selector algorithm before taking the decision to move DOWN must verify the status of all the channels, even if they are not active at the same time; otherwise, the risk is to generate oscillations on V_{OUT} adjustment.

While if an UP action is required by a channel, it is immediately executed to get out as quick as possible from any channel suffering condition, which could bring the I_{LED} current out of control.

7.8 Current generators

The LED-driving section consists of four current generators connected to the internal control logic. The channels can sustain up to 40 V and sink up to 200 mA each.

The brightness of the LEDs connected to the ALED7709x is controlled by:

- PWM modulation, performed independently on each channel (local digital dimming) or on all channels as a group (global digital dimming).
- Current level regulated independently on each channel (local analog dimming) or on all channels as a group (global analog dimming).

The full-scale current level is set by the resistor connected between the I_{SET} pin and ground.

$$I_{OUT,max} = \frac{V_{Iset}}{R_{Iset}} * K_{GAIN} \quad (10)$$

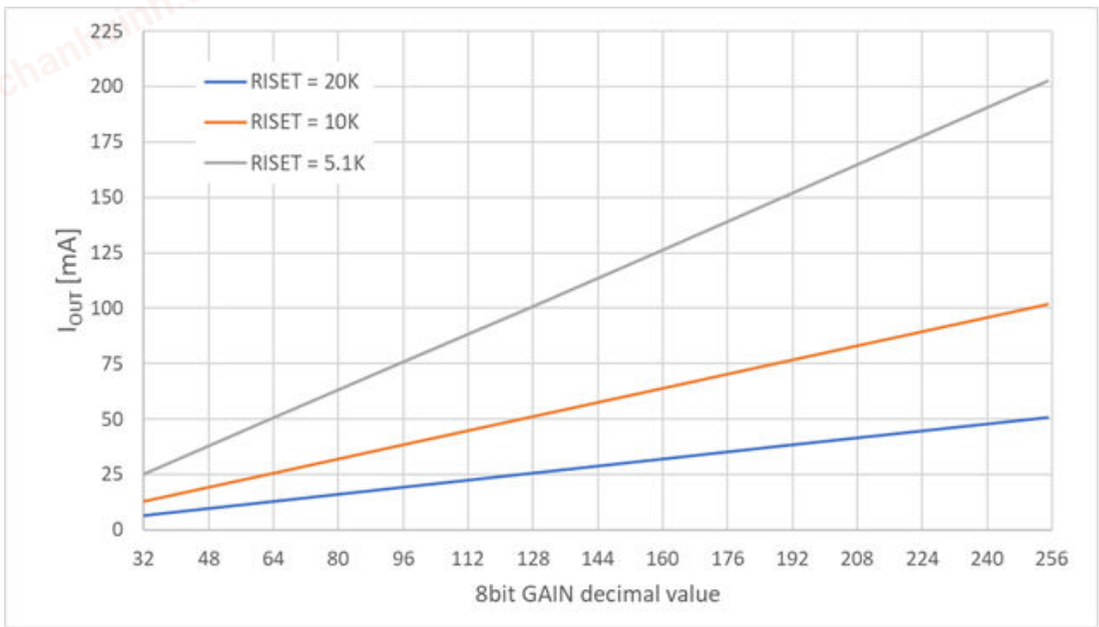
Where V_{Iset} = 1 V and K_{GAIN} = 1022 typ.

The current generators of the ALED7709x have been designed to be grouped (that is, connected in parallel) if required by the application. For stability reasons, the parallelization of the current generators should be done when the programmed current per channel is above 50% of I_{OUT} set by R_{Iset}.

The current accuracy among different devices typically is better than ±2% at 100 mA.

To obtain better performances, it is suggested to work with I_{OUT} current above 25 mA.

Figure 11. I_{OUT} linearity with GAIN at different R_{ISET}



Unused channels must be disabled through the internal CHSEL register to remove them from the adaptive algorithm.

During operation, a channel left floating and not disabled results in an open-channel faulty condition. This condition can be self-fixed by ALED7709x if the auto-disconnection on the open fault bit has been set.

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While a channel connected to ground is recognized during the initial fault check procedure, once detected, and notified, the only way to proceed toward normal operation is to act on the CLRF bit and after setting the DEN bit to release the ALED7709x from standby. As described for a floating channel, if a grounded channel is not disabled it results in an open-channel faulty condition.

The POR configuration of the ALED7709B allows unused channels to be left floating; once in operation the floating channels are recognized as OPEN and auto-disconnected, removing them from the adaptive algorithm.

7.8.1 Local dimming

In local dimming, each LED string is independently controlled by a dedicated PWM and current setting. The output current level of each channel can be adjusted through the “GAINx” register, while the “PWMx” register is used to define the digital dimming.

The PWM frequency and output control are set by the appropriate register value and are applied to all the channels.

Local dimming is fully adjustable only with I^2C control and can be achieved in user mode only, where GAINx and PWMx registers are independently adjustable.

7.8.2 Global dimming

In global dimming mode all the LED strings are driven at the same brightness value, by either PWMI or I^2C registers, depending on the Reg-PWMI bit setting.

The PWM dimming frequency is achieved changing the configuration (number of active bits) of the internal 16-bit counter; with this method the PWM step resolution is not related to the selected PWM frequency but depends only on the used clock; for ALED7709x the step resolution is 152.6 ns, due to the internal clock set at a target value of 6.5536 MHz.

Controlling the device with PWMI signal, the frequency can either follow exactly the PWMI signal or readjust to a predefined frequency as explained later, depending on the PWMI_direct bit setting.

Global dimming allows either user mode or mixed dimming mode.

In user mode the analog current and PWM values are unique for all the outputs; “GAIN1” and “PWM1” registers become the used reference and can be freely written by the user.

Mixed dimming mode combines both PWM and analog current control providing one optimal way to drive LEDs. At higher brightness the dimming is performed controlling only the constant-current; on the contrary, at lower brightness the dimming is performed acting on PWM duty-cycle.

This way to control the LED helps to improve the overall system efficiency (lower V_F requires also lower V_{OUT}), increase the dimming ratio (respect to a single dimming mode) and reduce EMI (PWM works at lower current value).

Each time mixed dimming mode is active, the analog and PWM values are computed by ALED7709x starting from the brightness value coming from PWMI or the register. The result of such a calculation is readable by the user in the read only registers: PWM(H/L)_STS and GAIN_STS.

7.8.3 Output control setting

ALED7709x implement a couple of methods to control the LED current peak taken from V_{OUT}.

One way is to control the speed of output switching ON/OFF; there is the possibility to select an appropriate rise/fall time through the bits OCS[1:0] in register OUTCFG, which allows 4 different configurations:

Table 11. Output control setting configuration

OCS[1:0]	Rise/fall time
00	Nominal (100 ns typ.)
01	2xNom
10	4xNom
11	8xNom

The second way to control the current peak is to avoid the switching ON of all the channels simultaneously. This also reduces the ripple on the V_{OUT} allowing a smaller value of the filter capacitor; a smaller ripple helps in avoiding audible noise coming from ceramic capacitors.

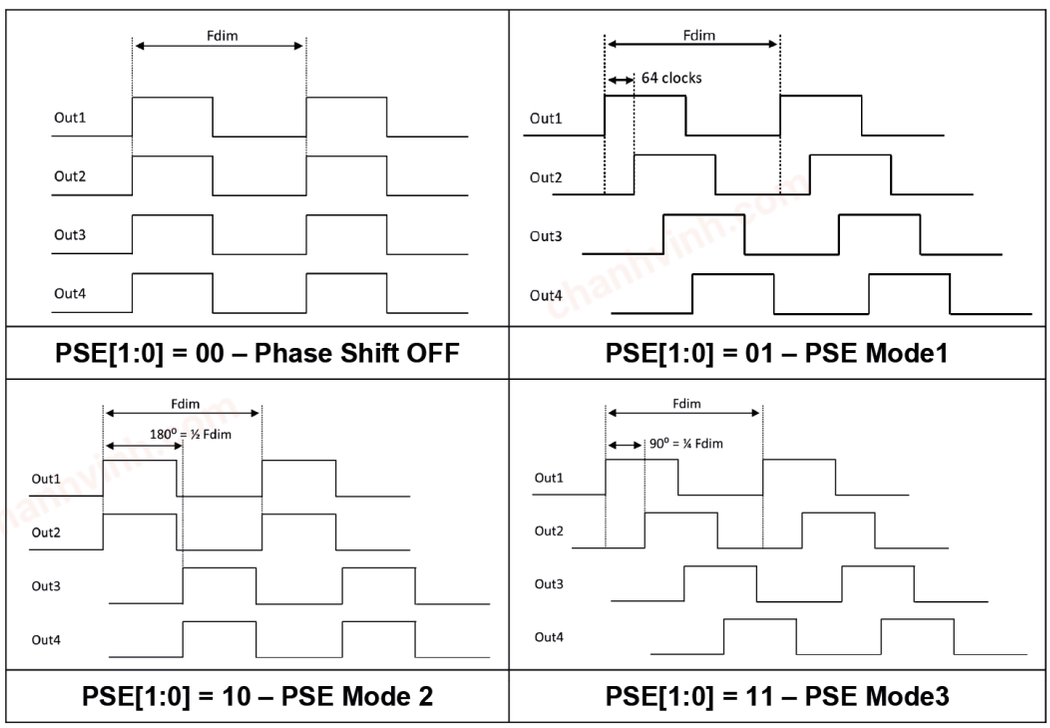
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The phase shift can be selected through the bits PSE[1:0] in register OUTCFG and has four different working modes as reported in the following table:

Table 12. Phase shift mode configuration

PSE[1:0]	Phase shift mode
00	OFF
01	64 clock staggered delay
10	1&2 – 3&4 180° phase shift
11	90° phase shift

Figure 12. Output signal vs. phase shift modes



7.9 Clock generation

The internal oscillator at 6.55 MHz is used for clocking all the internal digital blocks and to control internal timings also for analog parts.

A spread spectrum modulation can be enabled/disabled on main clock through DCLK_DIS bit; the depth of the modulation can be adjusted by properly setting DCLKMS[1:0] in BOOSTCFG register, while the modulation speed is fixed to $F_{CLK}/127$.

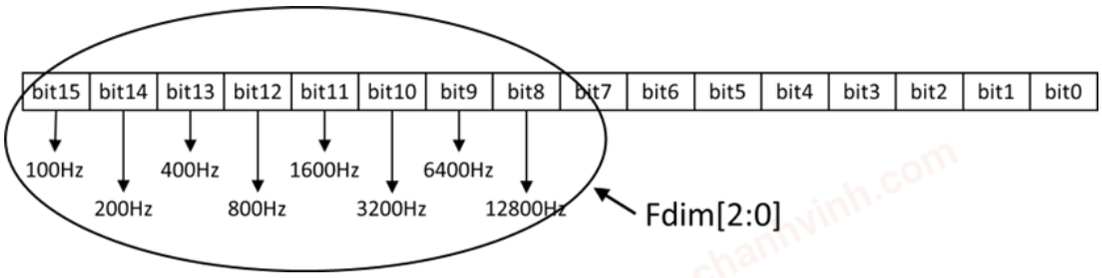
This clock is used to sample the PWMI input signal to perform duty-cycle and frequency measurement and, as well, it is used to feed the PWM counter defining the PWM step resolution.

7.9.1 PWM frequency and step resolution

Output PWM dimming frequency depends on the ALED7709A configuration set by FDIM [2:0] bits inside the register DIMCFG. Dimming frequency is achieved by defining the bit depth of the counter which is always fed with the same 6.55 MHz internal clock:

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Figure 13. **Number of bit vs. Fdim**



The ON-time step resolution is the clock period; there isn't any internal control to limit the minimum value of PWM, meaning that also 1 is a valid code managed by digital part and transferred to analog section.

On top of the external components, the output capability and shape also depend on the Rise and Fall time setting.

ALED7709B uses a PWM frequency set by the PWMI signal as per Table 13.

7.10 PWMI direct control

In this control mode the PWM output of all the channels follows exactly PWMI signal.

This mode is enabled setting Reg_PWMI bit to 0 and PWMI_direct bit to 1; it is the simplest way to control all the outputs at the same time.

Even when PWMI is the main control of the device the I^2C is not disabled, so the possibility to access the advanced features of both ALED7709A and ALED7709B is always there.

7.10.1 PWMI as control for brightness information

When both Reg-PWMI and PWMI_DRCT bits are set to 0, the PWMI signal duty-cycle is used as reference for setting the LED brightness while the PWMI frequency is used to select the Fdim, as per the following table.

Table 13. **PWM frequency vs. PWMI range**

PMWI frequency range		PWM generator frequency (Hz)
Min. (Hz)	Max. (Hz)	
>60	≤150	100
>150	≤300	200
>300	≤600	400
>600	≤1200	800
>1200	≤2400	1600
>2400	≤4800	3200
>4800	≤9600	6400
>9600	≤14000	12800

The PWM detector block measures the duty-cycle and period of the signal present on the PWMI pin using the 6.55 MHz as sampling clock. Depending on UMDM bit and LECC bit setting, there are three different modes to control the LED brightness.

When UMDM = 0 (in this case the LECC setting does not matter), the LED brightness is controlled by setting the duty-cycle of output PWM with the same duty-cycle value measured from PWMI, the current is kept to the defined value of GAIN1.

When UMDM = 1, the duty-cycle of the PWMI signal defines the LED BRIGHT, which is the input for the mixed dimming mode block that combines analog current and PWM controls.

With UMDM = 1, if LECC = 0, the PWMI duty-cycle is measured in a 16-bit brightness value, and a linear conversion law is used for computing the mixed dimming parameters.

While, when LECC = 1, an exponential law is applied starting from the PWMI duty-cycle value measured in 8-bit.

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The ALED7709B, at POR, is configured to use PWMI as driving signal in not direct mode (Reg-PWMI = 0 and PWMI_DRCT = 0) for global mixed mode with exponential curve (GLDM = 0, UMDM = 1 and LECC = 1).

7.11 Global dimming by I²C control

In this mode the value of brightness to be applied to the LED strings is written directly to the 16-bit registers BRIGHT%H & BRIGHT%L for linear curve or to 8-bit register BRIGHT%L only for exponential curve. This is active when Reg-PWMI bit is set to 1.

7.12 Mixed dimming mode

This is a mode that combines analog current and PWM dimming controls. Once activated, the mixed dimming mode uses the brightness information to compute the appropriate GAIN and PWM values.

We can consider the brightness range split in two parts, above and below the transition point.

The transition point can be set, by TPOINT[1:0] bits in register OUTCFG, between 12.5% to 50%.

Table 14. Transition point setting

TPOINT[1:0]	Transition point %
00	12.5
01	25
10	37.5
11	50

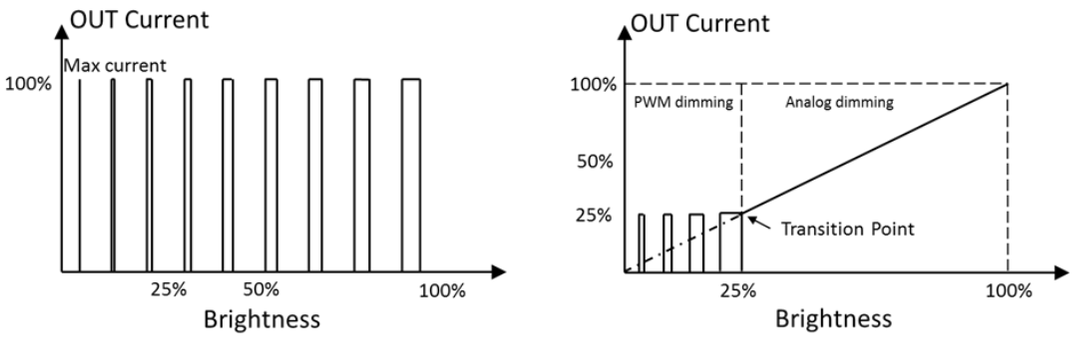
Above the transition point the dimming is done adjusting the analog current and leaving PWM to 100%; below transition point the brightness is controlled acting on PWM while GAIN stays set to the minimum value.

The conversion law is selectable between linear, with unity slope, or exponential, with a 3.9% progressive step.

There are few advantages in using a mixed dimming approach, the first one to minimize EMI because the PWM works only for mid/low current values. The other is a better efficiency of the overall system since lowering the analog current there is a reduction of the V_F of each LED and, as a consequence, the reduction of V_{LED} managed by the DC-DC converter section.

For a linear conversion, the mixed dimming works as shown in the right side of the following figure:

Figure 14. Pure digital dimming vs. mixed dimming mode



Mixed dimming mode helps in keeping a good resolution also for high Fdim value when the number of bits in the counter are reduced.

To have a linear correspondence of brightness control with human perception it is possible to enable an exponential conversion to determine the value of overall brightness using only 255 steps (8-bit). This could also simplify the sampling of PWMI, when the control is not done with registers, avoiding being so precise in retrieving a 16-bit value.

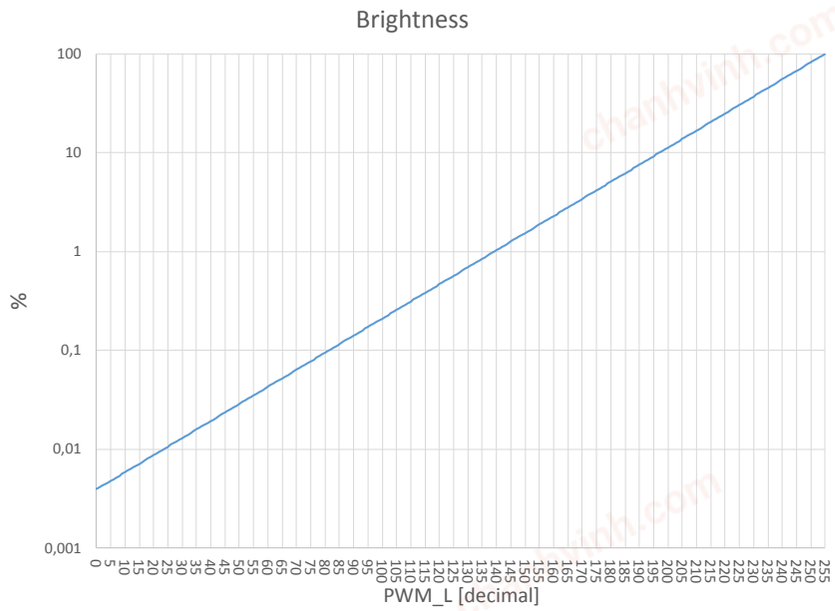
The correspondence brightness-step is based on the following formula:

$Bright\% = 0.961^{(255-i)} * 100$

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we have a curve with a constant step variation of 3.9%, reaching a potential dimming ratio of about 25000:1 in 255 steps, as shown in the figure below:

Figure 15. Dimming curve shown with logarithmic vertical axis



Even though the brightness value is limited to only 8-bit, the device adjusts the PWM dimming with 16-bit precision, and current gain is set with an 8-bit regulation.

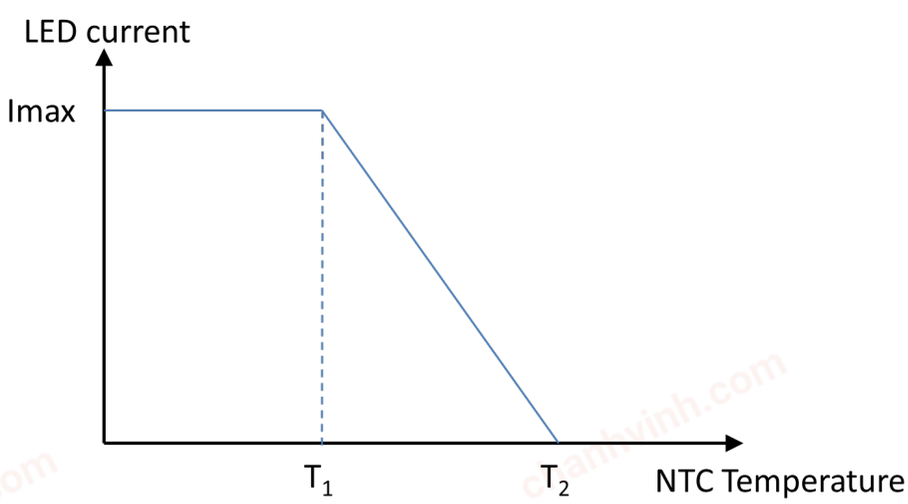
The GAIN and PWM values computed by the internal block and applied to the output are reported in the GAIN_STS and PWM(H/L)_STS read only registers.

7.13 Current control with external NTC

ALED7709x are supporting the capability to de-rate the maximum output current to keep under control the LED temperature using an external NTC based network.

The working principle is simple: NTC is used to generate a temperature dependent current; this current is subtracted to the I_{SET} so that I_{OUT} is progressively reduced to keep LED temperature under control.

Figure 16. Current control by NTC



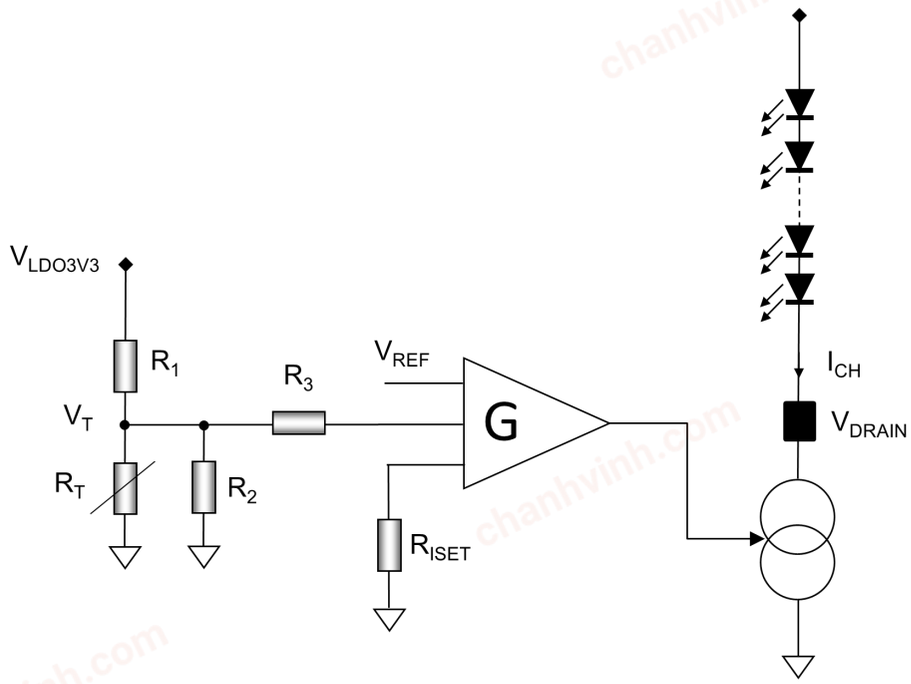
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T_1 and T_2 can be set with the appropriate external resistor calculation.

T_1 is the Breakpoint at which NTC circuit starts to reduce the current, T_2 is the Cutoff at which I_{OUT} goes to 0 mA.

ALED7709x are implementing this feature using a single pin circuit; it can be enabled or disabled using the bit TSA (Temperature Sensing Active) in the register OUTCFG. In case this feature is never activated or used, it is suggested to connect the pin TSNS directly to LDO3V3 to inhibit the current modulation

Figure 17. Temperature control circuit



In the circuit shown in the above Figure R_1 and R_2 are used to linearize the behavior of NTC in the working range, from T_1 to T_2, and in the meantime to set T_1.

While R_3 determines the de-rating slope to reach I_{OUT} = 0 mA at T_2

7.13.1 Calculation Procedure

We can start writing the formula to calculate the current flowing into R_3.

Using the Kirchoff equations applied to the resistors circuit of Figure 17, we can write the following relations:

$$\begin{cases} I_T = I_1 + I_3 \\ 0 = V_{LDO3V3} - V_1 - V_T \\ 0 = V_{REF} - V_3 - V_T \end{cases} \quad (11)$$

where the subscript gives a relation to the respective resistor, the only variation is I_T that refers to the current in R_P, which is the value reported hereafter:

$$R_p = \frac{R_T * R_2}{R_T + R_2} \quad (12)$$

doing some substitution and grouping in a specific way, we get:

$$I_{R3} = \frac{V_{REF} - V_{LDO3V3} * \frac{R_p}{R_p + R_1}}{R_p + R_3 - \frac{R_p^2}{R_p + R_1}} \quad (13)$$

T_1 is the point at which the current flowing into R_3 is crossing zero.

So, we can write:

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$$V_{REF} = V_{LDO3V3} * \frac{R_{p(T1)}}{R_{p(T1)} + R_1} \quad (14)$$

where $R_{p(T1)}$ is the parallel value due to the NTC at T_1.

Doing some item substitution and simplification, we get:

$$\frac{V_{LDO3V3}}{V_{REF}} = 1 + \frac{R_1}{R_2} + \frac{R_1}{R_{T(T1)}} \quad (15)$$

To linearize the NTC response in the working range we must compute the R_{lin} value at T_{mid}, middle point of the working range

$$T_{mid} = \frac{T_1 + T_2}{2} \quad (16)$$

By literature such value is:

$$R_{lin} = R_{Tmid} * \frac{B - 2*T_{mid}}{B + 2*T_{mid}} \quad (17)$$

Since we are not using a single parallel or series resistor to NTC but both, we must consider R_{lin} as the result of parallelism of R_1 and R_2.

So, we can use the following equation for replacing R_1 in a previous formula and to resolve for R_2:

$$R_1 = \frac{R_2 * R_{lin}}{R_2 - R_{lin}} \quad (18)$$

$$R_2 = \frac{R_{T(T1)} * R_{lin} * \frac{V_{LDO3V3}}{V_{REF}}}{\left(\frac{V_{LDO3V3}}{V_{REF}} - 1\right) * R_{T(T1)} - R_{lin}} \quad (19)$$

Now we can define the value of R_3 to reach the condition of I_{OUT} = 0 mA at T_2.

To achieve it, R_3 must generate in T_2 a current $I_{sense(T2)}$ equal to I_{set}, where:

$$I_{set} = \frac{V_{ref}}{R_{Iset}} \quad (20)$$

considering $I_{3(T2)} = I_{sense(T2)}$ we can calculate R_3 as

$$R_3 = \frac{V_{REF} - V_{LDO3V3} * \frac{R_{p(T2)}}{R_{p(T2)} + R_1}}{I_{sense(T2)}} - R_{p(T2)} + \frac{{R_{p(T2)}}^2}{R_{p(T2)} + R_1} \quad (21)$$

Now all the former unknown values are defined, and the circuit is completely quoted.

Note: In all the previous equations, the temperature must be in Kelvin (Celsius + 273.15).

NTC value is normally defined with two specific parameters: Sensitivity index (B) and Resistor value at reference temperature (R_0).

$$R_T = R_0 * e^{\left(B * \left(\frac{1}{T} - \frac{1}{T_0}\right)\right)} \quad (22)$$

7.13.1.1 *Numerical example:*

NTC {B = 3455; R_0 = 10 KΩ @ 25 °C ≡ 298.15 K}

V_{REF} = 1.0 V

V_{LDO3V3} = 3V3

R_{Iset} = 5.11 KΩ => for 200 mA (G = 1022)

T_1 = 65 °C ≡ 338.15 K

T_2 = 125 °C ≡ 398.15 K

Calculated values:

$R_{T(T1)}$ = 2539 Ω

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T_{mid} = 95 °C ≡ 368.15 K
R_{lin} = 716 Ω

$$R_2 = \frac{2539*716*\frac{3.3}{1.0}}{\left(\frac{3.3}{1.0}-1\right)*2539-716} = 1171\ \Omega \quad (23)$$

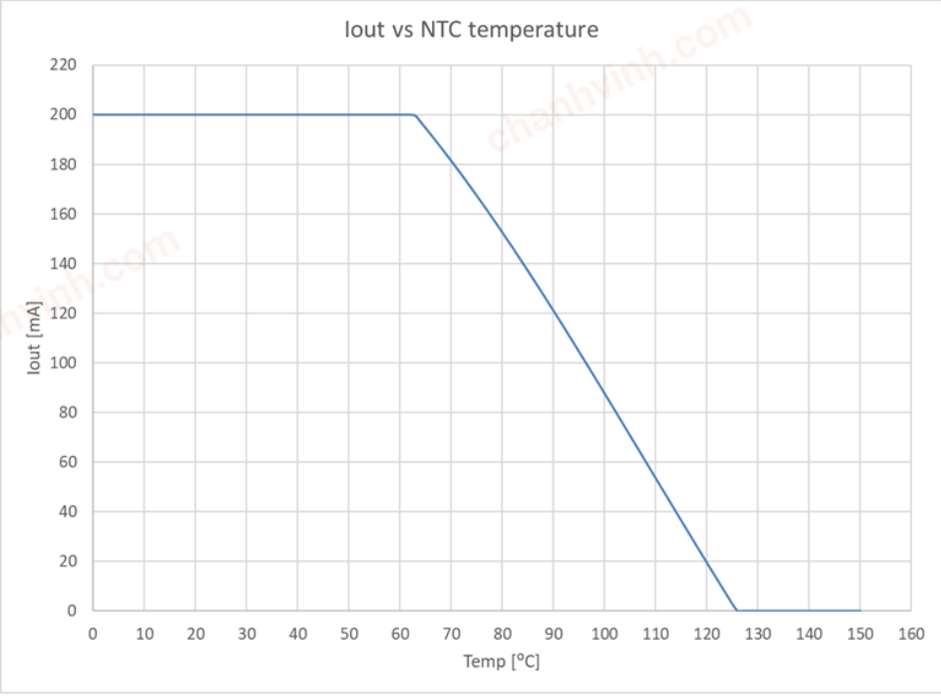
$$R_1 = \frac{1171*716}{1117-716} = 1844\ \Omega \quad (24)$$

$I_{sense(T2)}$ = 1 V / 5.11 KΩ = 196 uA
$R_{T(T2)}$ = 554 Ω
$R_{p(T2)}$ = 372 Ω

$$R_3 = \frac{1.0-3.3*\frac{372}{372+1844}}{0.000196} - 372 + \frac{372^2}{372+1844} = 1967\ \Omega \quad (25)$$

Using commercial values: R_1 = 1.8 KΩ, R_2 = 1.1 KΩ and R_3 = 2.0 KΩ;
we get theoretical values of: T_1 = 62.83 °C and T_2 = 125.93 °C

Figure 18. Simulated I_{OUT} vs. NTC temperature



7.14 Table of different working modes

Table 15. DIMCFG bit settings for different working modes

DIMCFG bits setting					Mode	Notes
Reg_PWMI = 0 (PWMI control; acts as PWM1 global) FDIM[2:0] = xxx (Dimming frequency depends on PWMI signal)	GLDM = 0 (GLOBAL; GAIN1 is global)	UMDM = 0 (USER; GAIN1 can be modified by Reg)	PWM_DRCT = 0	LECC = 0	M1	
				LECC = 1	M2	
			PWMI_DRCT = 1	LECC = x	M3	In PWMI direct control, linear and exponential conversion have no meaning

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DIMCFG bits setting					Mode	Notes
Reg_PWMI = 0 (PWMI control; acts as PWM1 global) FDIM[2:0] = xxx (Dimming frequency depends on PWMI signal)	GLDM = 0 (GLOBAL; GAIN1 is global)	UMDM = 1 (MIXED; GAIN1 is controlled by PWMI)	PWMI_DRCT = 0	LECC = 0	M4	In mixed mode only global dimming is possible
				LECC = 1	M5	
	GLDM = 1 (LOCAL; GAINx are active)	UMDM = 0 (LOCAL can be only USER; GAINx can be modified by Reg)	PWM_DRCT = 0	LECC = 0	M6	
				LECC = 1	M7	
			PWMI_DRCT = 1	LECC = x	M8	In PWMI direct control, linear and exponential conversion have no meaning
Reg_PWMI = 1 (Register control; PWM and GAIN are fully adjustable depending on other bit settings) FDIM[2:0] = SET (Dimming frequency is defined by Reg value)	GLDM = 0 (GLOBAL; PWM1 and GAIN1 are global)	UMDM = 0 (USER; PWM1 and GAIN1 can be modified by Reg)	PWMI_DRCT = x	LECC = 0	M9	
				LECC = 1	M10	
		UMDM = 1 (MIXED; PWM1 value acts as Bright and control both Digital and Analog output values)		LECC = 0	M11	In mixed mode only global dimming is possible
				LECC = 1	M12	
	GLDM = 1 (LOCAL; PWMx and GAINx are active and fully independent)	UMDM = 0 (LOCAL can be only USER; PWMx and GAINx can be modified by Reg)		LECC = 0	M13	
				LECC = 1	M14	

Following the description of each working mode, the value of DIMCFG to set the corresponding working mode is reported in the section title. The value is in binary, the bits written as “x” mean “don’t care”, the ones written as “X” mean “customer setting”, this is mainly related to FDIM[2:0] bits.

7.14.1 Working mode M1 (Reg DIMCFG = 00xxx000b)

PWMI is sampled to recover duty-cycle and frequency to be applied to all the outputs; frequency is set as for Table 13 while duty-cycle sets the output pulse duration following the linear curve.

All the outputs go to OFF if the PWMI signal stays at LOW level for more than 20 ms.

Current is set for all the channels by the register GAIN1 value.

7.14.2 Working mode M2 (Reg DIMCFG = 00xxx100b)

PWMI is sampled to recover duty-cycle and frequency to be applied to all the outputs; frequency is set as for Table 13 while duty-cycle sets the output pulse duration following the exponential curve.

All the outputs go to OFF if the PWMI signal stays at LOW level for more than 20 ms.

Current is set for all the channels by the register GAIN1 value.

7.14.3 Working mode M3 (Reg DIMCFG = 01xxxx00b)

PWMI directly controls the digital behavior of outputs; the PWMI signal is reconstructed by the internal clock, but it is not post-processed and so the LECC bit has no meaning.

Current is set for all the channels by the register GAIN1 value.

7.14.4 Working mode M4 (Reg DIMCFG = 00xxx010b)

PWMI is sampled to recover duty-cycle and frequency to be applied to all the outputs; frequency is set as for Table 13 while duty-cycle defines the brightness value using mixed dimming mode that combines analog current and PWM adjustments.

This mode applies the linear curve to convert brightness value in gain and PWM components.

Hereafter, a couple of examples to clarify the mode behavior, transition point is set to 25%:

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1. PWMI is a signal at 350 Hz and 15% duty-cycle
   a. applying the linear curve, the duty-cycle value is the brightness value which results to be below the defined TP
   b. GAIN1, valid for all channels, is set at 25% of maximum
   c. PWM is set to a frequency of 400 Hz, as for Table 13, and with a duty-cycle of 60%; because to have 15% brightness with current set to 25% we need to multiply by 4 the PWM
2. PWMI is a signal at 350Hz and 35% duty-cycle
   a. applying the linear curve, the duty-cycle value is the brightness value which results to be above the defined TP
   b. GAIN1, valid for all channels, is set at 35% of maximum
   c. PWM is set at 100%, outputs always ON

All the outputs go to OFF if the PWMI signal stays at LOW level for more than 20 ms.

7.14.5 Working mode M5 (Reg DIMCFG = 00xxx110b) – Variant B configuration

PWMI is sampled to recover duty-cycle and frequency to be applied to all the outputs; frequency is set as for Table 13 while duty-cycle defines the brightness value using mixed dimming mode that combines analog current and PWM adjustments.

The exponential curve to convert the duty-cycle, measured in 8-bit depth, into the brightness value is applied before to define the gain and PWM components.

Hereafter, a couple of examples to clarify the mode behavior, transition point is set to 25%:

1. PWMI is a signal at 350 Hz and 65% duty-cycle
   a. applying the exponential curve 65% duty-cycle (166d in 8-bit) becomes 2.9% of brightness which is below the defined TP
   b. GAIN1, valid for all channels, is set at 25% of maximum
   c. PWM is set to a frequency of 400 Hz, as for Table 13, and with a duty-cycle of 11.6%; because to have 2.9% brightness with current set to 25% we need to multiply by 4 the PWM
2. PWMI is a signal at 350 Hz and 90% duty-cycle
   a. applying the exponential curve 90% duty-cycle (230d in 8-bit) becomes 37% of brightness which is above the defined TP
   b. GAIN1, valid for all channels, is set at 37% of maximum
   c. PWM is set at 100%, outputs always ON

All the outputs go to OFF if the PWMI signal stays at LOW level for more than 20 ms.

7.14.6 Working mode M6 (Reg DIMCFG = 00xxx001b)

PWMI is sampled to recover duty-cycle and frequency to be applied to all the outputs; frequency is set as for Table 13 while duty-cycle sets the output pulse duration following the linear curve.

All the outputs go to OFF if the PWMI signal stays at LOW level for more than 20 ms.

Current can be set differently for each channel acting on the proper channel register GAINx.

7.14.7 Working mode M7 (Reg DIMCFG = 00xxx101b)

PWMI is sampled to recover duty-cycle and frequency to be applied to all the outputs; frequency is set as for Table 13 while duty-cycle sets the output pulse duration following the exponential curve.

All the outputs go to OFF if the PWMI signal stays at LOW level for more than 20 ms.

Current can be set differently for each channel acting on the proper channel register GAINx.

7.14.8 Working mode M8 (Reg DIMCFG = 01xxxx01b)

PWMI directly controls the digital behavior of outputs; the PWMI signal is reconstructed by the internal clock but it is not post-processed and so the LECC bit has no meaning.

Current can be set differently for each channel acting on the proper channel register GAINx.

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7.14.9 Working mode M9 (Reg DIMCFG = 1xXXX000b)

PWM frequency is set by FDIM[2:0] bits as for Table 32 description while the PWM for all the outputs is defined by registers PWM1H and PWM1L. The duty-cycle value written in the PWM1 registers is applied as is (liner curve) to all the channels.

Current is set for all the channels by the register GAIN1 value.

7.14.10 Working mode M10 (Reg DIMCFG = 1xXXX100b)

PWM frequency is set by FDIM[2:0] bits as for Table 32 description while the PWM for all the outputs is defined by register PWM1L only. The 8-bit value written in the PWM1L register is converted by exponential curve and applied to all the channels.

Current is set for all the channels by the register GAIN1 value.

7.14.11 Working mode M11 (Reg DIMCFG = 1xXXX010b)

PWM frequency is set by FDIM[2:0] bits as for Table 32 description.

Being in mixed dimming mode, the value written in registers BRIGHT is used to compute both analog current and PWM settings that are applied to all the channels. The conversion is based on linear curve.

Hereafter, a couple of examples to clarify the mode behavior, transition point is set to 25%:

1. BRIGHT registers are programmed for setting 15%
   a. because of the linear curve application, the 16-bit value in BRIGHT registers is exactly the brightness value to be considered, which results to be below the defined TP
   b. GAIN1, valid for all channels, is set at 25% of maximum
   c. PWM is set to a duty-cycle of 60% because to have 15% brightness with current set to 25% we need to multiply by 4 the PWM
2. BRIGHT registers are programmed for setting 60%
   a. because of the linear curve application, the 16-bit value in BRIGHT registers is exactly the brightness value to be considered, which results to be above the defined TP
   b. GAIN1, valid for all channels, is set at 60% of maximum
   c. PWM is set at 100%, outputs always ON

7.14.12 Working mode M12 (Reg DIMCFG = 1xXXX110b)

PWM frequency is set by FDIM[2:0] bits as for Table 32 description.

Being in mixed dimming mode the value written in register BRIGHT is used to compute both analog current and PWM settings that are applied to all the channels. The conversion is based on exponential curve and so only the 8-bit value in BRIGHT%L is considered for the final brightness computation.

Hereafter, a couple of examples to clarify the mode behavior, transition point is set to 25%:

1. BRIGHT%L register is programmed for setting 65%
   a. because of the exponential curve application, the 8-bit value in BRIGHT%L register becomes 2.9% brightness as value to be considered, which results to be below the defined TP
   b. GAIN1, valid for all channels, is set at 25% of maximum
   c. PWM is set to a duty-cycle of 11.6%; because to have 2.9% brightness with current set to 25% we need to multiply by 4 the PWM
2. BRIGHT%L register is programmed for setting 90%
   a. because of the exponential curve application, the 8-bit value in BRIGHT%L register becomes 37% brightness as value to be considered, which results to be above the defined TP
   b. GAIN1, valid for all channels, is set at 37% of maximum
   c. PWM is set at 100%, outputs always ON

7.14.13 Working mode M13 (Reg DIMCFG = 1xXXX001b)

PWM frequency is set by FDIM[2:0] bits as for Table 32 description while the PWM value for each channel is defined by registers PWMxH and PWMxL. The duty-cycle value written in the PWMx registers is applied as is (liner curve) to the respective channel.

Current is independently set for each channel by the register GAINx value.

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7.14.14 Working mode M14 (Reg DIMCFG = 1xXXX101b)

PWM frequency is set by FDIM[2:0] bits as for Table 32 description.

The 8-bit duty-cycle value written in the PWMxL registers is converted by exponential curve and applied to the respective “x” channel.

The current can also be independently set for each channel by respective register GAINx.

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8 Programming

8.1 Serial interface and internal registers overview

ALED7709x have the capability to operate in different working mode, depending on the configuration written into registers directly at POR or later, while the LED brightness can be adjusted both or either by PWMI signal and/or by I^2C serial interface.

The devices have 26 internal registers: 6 of them dedicated to configuration, 12 related to the brightness control of the LED strings connected to the channels, 7 registers are read only for device status information and 1 to Enable/Disable the device.

All registers are 8-bit wide.

8.2 I^2C serial bus

The I^2C bus consists of two digital signals: serial data (SDA) and serial clock (SCL) connected to the respective pins of ALED7709x.

ALED7709x can operate as slave supporting fast-mode I^2C protocol (400 KHz). I^2C bus communication must be managed by an MCU acting as master and ALED7709x interact with it when valid commands appear on the bus. When the pin EN is kept low, ALED7709x do not reply to I^2C communication but it leaves SDA and SCL free; this allows the MCU to communicate with any other device present on the same I^2C bus.

The communication to ALED7709x must be initiated by the master issuing a START condition. The START condition is detected by all slave devices connected to the bus; to have a communication with a specific device the bus master must send the device address to specify the destination slave.

The ALED7709A slave address is hardwired to 28h @ 7-bit, while the ALED7709B slave address is hardwired to 29h @ 7-bit.

The 8^{th}bit of the device address is the Read/Write bit (RW). This bit is asserted for read operations and cleared for write operations; meaning slave address 0x50 (ALED7709A) or 0x52 (ALED7709B) for write and 0x51 (ALED7709A) or 0x53 (ALED7709B) for read in standard 8-bit mode.

If a device address matching occurs, the ALED7709x reply with an acknowledgment (ACK), that is, pulling down the SDA line during the 9^{th} bit of the device address. In case the device address does not match, the ALED7709x deselect it from the bus.

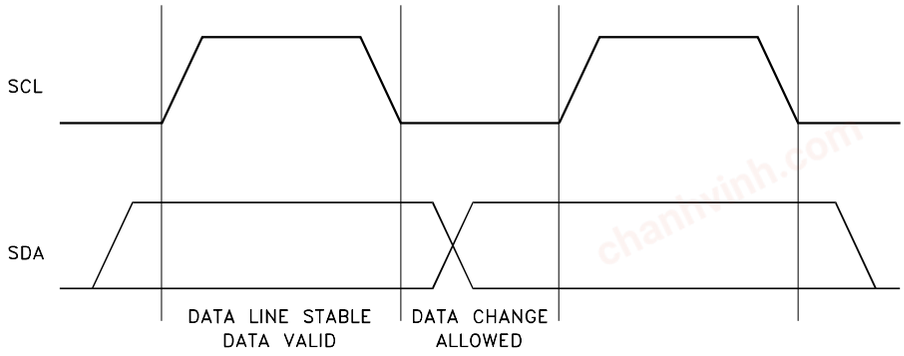
Because some values are 16-bit long (they occupy 2 registers, like PWMxH and PWMxL) or some configurations need to modify more registers (like to change PWM and GAIN independently per each channel), ALED7709x apply the updated values only when the STOP is issued on the I^2C bus. In this way all the changes are applied in a synchronous mode independently on the status of the device. In case a user would like to force the immediate change of only a portion of configuration (for example PWM2H only), it is possible to call only such register and issue the STOP just after.

8.2.1 Data validity

As shown in Figure 19, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

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Figure 19. **Data validity on the I²C bus**



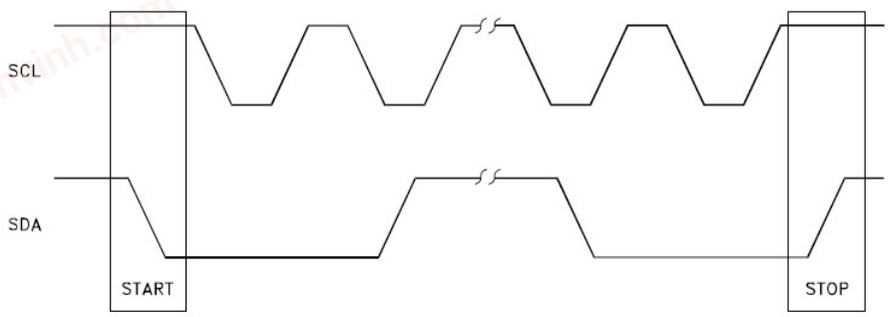
8.2.2 Start and Stop conditions

Both DATA and CLOCK lines remain HIGH when the bus is not busy. As shown in Figure 20, a START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

START and STOP are conditions always generated by master; after a START the bus is considered busy and becomes free again a certain time after STOP. For this reason, a STOP condition must be sent at the end of each communication.

A second START condition sent before a STOP condition is called Repeated START (or RESTART) and it is normally used to change the communication direction, typically from Write to Read.

Figure 20. **Start and Stop on the I²C bus**



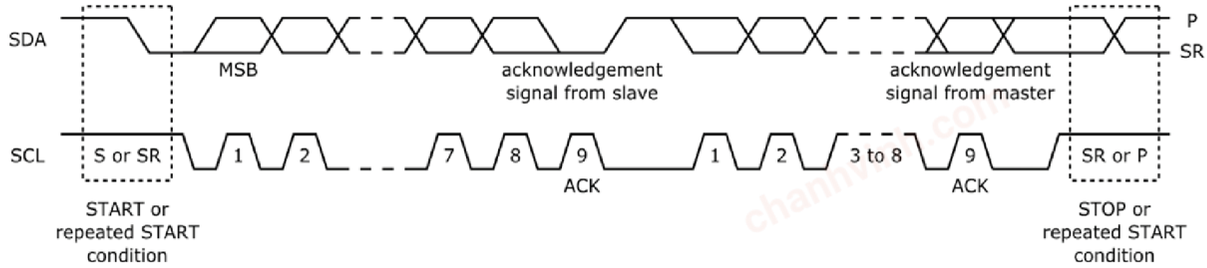
8.2.3 Byte format

Every packet transferred on the SDA line must contain eight bits, each byte is followed by an acknowledge bit. Each clock pulse transfers a single bit of the packet, the data transfer is MSB (Most Significant Bit) first.

The level on the SDA line must remain stable during the HIGH period of the clock pulse, any change in the SDA line at this time is considered as a control signal (START or STOP condition).

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Figure 21. **Bit transfer**



8.2.4 Acknowledge (ACK) and not acknowledge (NACK)

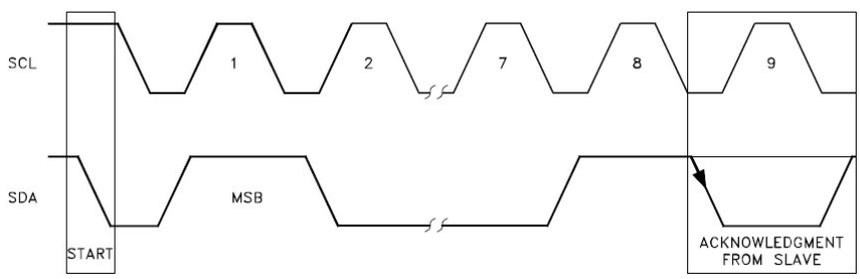
After every byte the acknowledge take place, this allows the receiver to inform the transmitter if the byte was successfully received and another byte can be sent or if the transmission failed. It is a duty of the master to generate all the needed clock pulses, including the acknowledge ninth pulse.

The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse so the receiver can force and keep LOW the SDA line during this clock pulse (see Figure 22).

If the receiver left HIGH the SDA line during the ninth clock pulse, it generates the so called Not Acknowledge signal. In this case, the master can generate either a STOP condition to abort the transfer, or a Repeated START condition to initiate a new transfer.

The ALED7709x do not generate acknowledge if the V_{IN} supply is below the undervoltage Lockout threshold or if EN pin is driven LOW; these conditions are not allowing the I^2C block to be active and so able to reply to any master request.

Figure 22. **Acknowledge on the I^2C bus**



8.2.5 Interface protocol

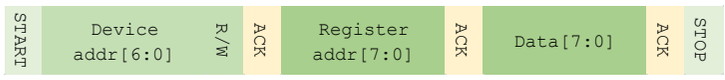
The interface protocol is composed of:

- Start condition (START)
- Device address (7-bit) + R/W bit (read = 1 / write = 0)
- Register address byte
- Sequence of N data packet (1 byte + acknowledge)
- Stop condition (STOP)

The register address byte determines the first register in which the read or write operation takes place. When the read or write operation is finished, the internal register address pointer is automatically incremented allowing multiple register writing or reading.

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Figure 23. **Interface protocol**

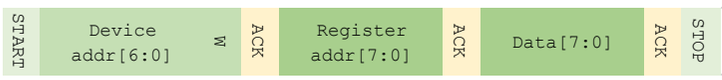


8.2.5.1 *Writing to a single register*

Writing to a single register starts with a START condition followed by the 7-bit device address of ALED7709x, the 8th bit of the byte is the R/W bit, which is 0 for writing operations.

Then the master waits for ALED7709x acknowledge. Then the 8-bit address of the register is sent to ALED7709x and it is also followed by an acknowledge pulse. The last transmitted byte is the data to be written into the register, the ALED7709x generate the acknowledge pulse at the end of packet. The master then generates a STOP condition, and the communication is over.

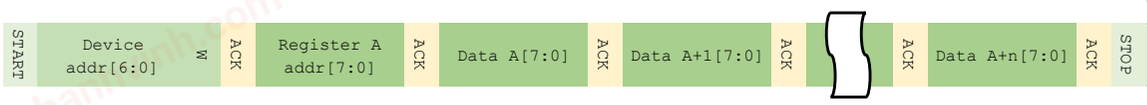
Figure 24. **Writing to a single register**



8.2.5.2 *Writing to multiple registers with incremental addressing*

It would not be easy to send the device address and the address of the register several times when writing to multiple sequential registers. The ALED7709x support writing to multiple registers with incremental addressing. When data is written to register, the internal address register pointer is automatically incremented, so the next data can be sent without repeating the device address and new register address.

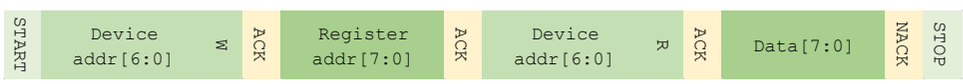
Figure 25. **Writing to multiple registers**



8.2.5.3 *Reading from a single register*

The reading operation starts with a START condition followed by the 7-bit device address of ALED7709x, the 8th bit of the byte is the R/W bit, which must be set to 0 as writing operations. ALED7709x confirm the receiving of the address + R/W bit by an acknowledge pulse. The address of the register which should be read is sent afterwards and confirmed again with an acknowledge pulse by ALED7709x. Then the master generates a RESTART condition and sends the 7-bit device address followed by the R/W bit, which now is set to 1 for reading operations. The ALED7709x confirm the receiving of the address + R/W bit by an acknowledge pulse and start to send the data to the master, one data per clock pulse always generated by master. No acknowledge pulse from the master is required after receiving the data. Then the master generates a STOP condition to terminate the communication.

Figure 26. **Reading to a single register**



8.2.5.4 *Reading from multiple registers with incremental addressing*

Reading from multiple registers starts in the same way as reading from a single register. As soon as the first register is read, the internal register address pointer is automatically incremented. If the master generates an acknowledge pulse after receiving the data from the first register, then reading of the next register can start immediately without sending again the device address and the new register address. The last acknowledge pulse before the STOP condition is not required.

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Figure 27. **Reading from multiple registers**



8.3 Accessing internal registers

Access to a specific register of ALED7709x is achieved by specifying the register address.

Write and read operations can be performed on a single register or over a group of sequential registers.

Table 16. **ALED7709A register map**

ADD	Name	POR vers A	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
00h	DEVID	13h	VERS_ID				REV_ID			
01h	DEVEN	00h	CLRF	0	0	0	0	0	0	DEN
02h	PWM1H	00h	PWM Channel1/BRIGHT [15:8]							
03h	PWM1L	00h	PWM Channel1/BRIGHT [7:0]							
04h	GAIN1	00h	Gain Channel1/All [7:0]							
05h	PWM2H	00h	PWM Channel2 [15:8]							
06h	PWM2L	00h	PWM Channel2 [7:0]							
07h	GAIN2	00h	Gain Channel2 [7:0]							
08h	PWM3H	00h	PWM Channel3 [15:8]							
09h	PWM3L	00h	PWM Channel3 [7:0]							
0Ah	GAIN3	00h	Gain Channel3 [7:0]							
0Bh	PWM4H	00h	PWM Channel4 [15:8]							
0Ch	PWM4L	00h	PWM Channel4 [7:0]							
0Dh	GAIN4	00h	Gain Channel4 [7:0]							
0Eh	PWMH_STS	00h	PWM Channels [15:8]							
0Fh	PWML_STS	00h	PWM Channels [7:0]							
10h	GAIN_STS	00h	Gain Channels [7:0]							
11h	CHCFG	0Fh	0	CH3CH4	CH2CH3	CH1CH2	CEN4	CEN3	CEN2	CEN1
12h	OUTCFG	00h	OCS[1:0]		PSE[1:0]		TPOINT[1:0]		TSA	0
13h	BOOSTCFG	00h	FSW[1:0]		DCLKMS[1:0]		0	OVRE	DCLK_DIS	DFSW_DIS
14h	DIMCFG	00h	REG_PWMI	PWMI_DRCT	FDIM[2:0]			LECC	UMDM	GLDM
15h	FMCFG	01h	0	0	LSWE	FALT	OCAD	SCAD	SH_DIS	1
16h	FMASK	00h	IOCP_M	IOVP_M	CHCK_M	OTEA_M	LEDF_M	OOVP_M	THSD_M	0
17h	DEVSTA	00h	IOCP	IOVP	CHCK	OTEA	LEDF	OOVP	THSD	0
18h	CHSTA	00h	SH4	SH3	SH2	SH1	OP4	OP3	OP2	OP1
19h	INITSTA	00h	RISET	CH3-CH4	CH2-CH3	CH1-CH2	CH4GND	CH3GND	CH2GND	CH1GND

R/W	R only
Reserved	W only

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Table 17. **ALED7709B register map**

ADD	Name	POR vers B	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
00h	DEVID	13h	VERS_ID				REV_ID			
01h	DEVEN	01h	CLRF	0	0	0	0	0	0	DEN
02h	PWM1H	00h	PWM Channel1/BRIGHT [15:8]							
03h	PWM1L	00h	PWM Channel1/BRIGHT [7:0]							
04h	GAIN1	FFh	Gain Channel1/All [7:0]							
05h	PWM2H	00h	PWM Channel2 [15:8]							
06h	PWM2L	00h	PWM Channel2 [7:0]							
07h	GAIN2	00h	Gain Channel2 [7:0]							
08h	PWM3H	00h	PWM Channel3 [15:8]							
09h	PWM3L	00h	PWM Channel3 [7:0]							
0Ah	GAIN3	00h	Gain Channel3 [7:0]							
0Bh	PWM4H	00h	PWM Channel4 [15:8]							
0Ch	PWM4L	00h	PWM Channel4 [7:0]							
0Dh	GAIN4	00h	Gain Channel4 [7:0]							
0Eh	PWMH_STS	00h	PWM Channels [15:8]							
0Fh	PWML_STS	00h	PWM Channels [7:0]							
10h	GAIN_STS	00h	Gain Channels [7:0]							
11h	CHCFG	7Fh	0	CH3CH4	CH2CH3	CH1CH2	CEN4	CEN3	CEN2	CEN1
12h	OUTCFG	3Eh	OCS[1:0]		PSE[1:0]		TPOINT[1:0]		TSA	0
13h	BOOSTCFG	06h	FSW[1:0]		DCLKMS[1:0]		0	OVRE	DCLK_DIS	DFSW_DIS
14h	DIMCFG	06h	REG_PWMI	PWMI_DRCT	FDIM[2:0]			LECC	UMDM	GLDM
15h	FMCFG	69h	0	1	LSWE	FALT	OCAD	SCAD	SH_DIS	1
16h	FMASK	10h	IOCP_M	IOVP_M	CHCK_M	OTEA_M	LEDF_M	OOVP_M	THSD_M	0
17h	DEVSTA	00h	IOCP	IOVP	CHCK	OTEA	LEDF	OOVP	THSD	0
18h	CHSTA	00h	SH4	SH3	SH2	SH1	OP4	OP3	OP2	OP1
19h	INITSTA	00h	RISET	CH3-CH4	CH2-CH3	CH1-CH2	CH4GND	CH3GND	CH2GND	CH1GND

R/W	R only
Reserved	W only

8.3.1 Device Identification register (DEVID)

This is a read only register and contains the silicon version identification (bit 7:4) and revision identification (bit 3:0).

Table 18. **DEVID register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 00h	VERS_ID				REV_ID			
POR A = 13h	0	0	0	1	0	0	1	1
POR B = 13h	0	0	0	1	0	0	1	1
Comments	R	R	R	R	R	R	R	R

REV_ID: Silicon revision identification

- 3h: cut x.3 (hardwired)

VERS_ID: Silicon version identification

- 1h: cut 1.x (hardwired)

8.3.2 Device enable register (DEVEN)

This register includes the write only CLRF bit, used to clear all fault bits latched by device and to reset FAULT pin if latched. It also includes the DEN bit, which is the one to take ALED7709x out from standby condition to operation mode.

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Table 19. **DEVEN register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 01h	CLRF	Reserved						DEN
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 01h	0	0	0	0	0	0	0	1
Comments	W	-	-	-	-	-	-	R/W

DEN: Enable device

- 0: device is in standby
- 1: device is in operation mode

CLRF: Clear faults (auto-cleared bit)

- 0: normal mode
- 1: reset faults (faults registers DEVSTA, CHSTA and INITSTA are cleared, and FAULT pin restored)

CLRF bit is write only and it must be set to 1 to clear the bits reporting any fault and to restore the status of the FAULT pin (in case it is set as Latched). It returns to 0 as soon as the clear is completed.

8.3.3 PWM registers (PWMxH, PWMxL)

The PWMxH and PWMxL (where x = 1 to 4) registers are arranged in 4 pairs (upper 8-bit and lower 8-bit), clearly associated to their respective output channels.

In user mode, these registers directly control the PWM duty-cycle applied to the outputs; ALED7709x support two PWM dimming control options: global dimming and local dimming.

The first option uses the PWM1H:PWM1L pair to set the same dimming level to all the channels, while the second one allows setting a different dimming level on each channel (all PWMxH:PWMxL pairs are active).

To avoid a not synchronous update of the channels the register value is transferred to the output only when the I^2C STOP, or RESTART, is issued. In local mode, it is possible to update only one channel writing the respective PWMxH and PWMxL and issuing immediately an I^2C STOP or RESTART. While to have all the channels updated at the same time it is enough to write all the registers, including also GAINx, from 0x02 to 0x0D, in the same I^2C frame before issuing the STOP.

It is always possible to update PWMxH or PWMxL or GAINx (where x = 1 to 4) by using a single register write procedure.

The PWM signals at the outputs are generated by comparing the content of the PWMxH:PWMxL registers to the 16-bit counter.

All the PWM registers are connected to the digital comparators of digital dimming circuitry through a 64-bit buffer. This is used to store the values and the transfer to the digital dimming circuit happens only at the end of the Fdim cycle taking also into account if Phase Shift is active.

Table 20. **PWMxH registers**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDH (1)	PWMxH							
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. *ADDH = 02h for PWM1H; 05h for PWM2H; 08h for PWM3H; 0Bh for PWM4H*

PWMxH: represents the highest 8-bit of PWM duty-cycle value for channel x.

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Table 21. **PWMxL registers**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDL (1)	PWMxL							
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. *ADDL = 03h for PWM1L; 06h for PWM2L; 09h for PWM3L; 0Ch for PWM4L*

PWMxL: represents the lowest 8-bit of PWM duty-cycle value for channel x.

8.3.3.1 *PWM registers used as BRIGHT setting*

In mixed mode, this pair of registers is used to input the value of the required brightness.

In mixed mode, ALED7709x compute internally the value of PWM and GAIN to be applied to outputs to achieve the required brightness level.

In case of linear curve selection (LECC bit set to 0), all the 16-bit are used since the value is linearly converted into a percentage of MAX brightness capability.

If the exponential curve is selected (LECC bit set to 1), only the 8 bits of PWM1L are used since the device applies the following equation to get the expected brightness percentage; the full scale is covered in 256 steps (from 0x00 to 0xFF):

$$Bright\% = 0.961^{(255 - PWM1L)} * 100$$

Using linear curve, the brightness value is considered only when both PWM1H & PWM1L are updated, and the STOP is issued.

Table 22. **PWM1H register used as BRIGHT%H**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 02h	BRIGHT%H							
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BRIGHT%H: represents the highest 8-bit of brightness for all channels when linear curve is selected, not used if exponential curve is selected.

Table 23. **PWM1H register used as BRIGHT%L**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 03h	BRIGHT%L							
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BRIGHT%L: represents the lowest 8-bit of brightness for all channels when linear curve is selected, or the chosen step when exponential curve is selected.

8.3.4 Analog Gain registers (GAINx)

These registers are active in user mode, while in mixed mode they are inhibited.

In local mode, each GAINx register is independent, and the value written in these registers controls the output current of the relative channel. While in global mode only GAIN1 is active, and its value is applied to all the channels.

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Users can define 256 different current levels starting from the maximum current set by R_{ISET} using the 8-bit register.

$I_{OUT} = I_{OUT,max} * GAIN[7:0] / 255$

ALED7709x work well for a $I_{OUT,min}$ higher than 25 mA; but there is not any internal limitation to go lower.

Meaning that it is possible to define a $I_{OUT,max}$ at 100 mA, using the appropriate R_{ISET}, and write a GAIN of 25d to get about 10 mA as I_{OUT}; simply the accuracy of such value is not guaranteed.

When ALED7709x are configured in mixed dimming mode the internal circuit uses the complete gain resolution of 8 bits to compute the expected current value from $I_{OUT,max}$ to the transition point value.

Table 24. GAIN1 register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 04h	GAIN1							
POR A = 00h	0	0	0	0	0	0	0	0
POR B = FFh	1	1	1	1	1	1	1	1
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25. GAINx registers

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDG (1)	GAINx							
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. *ADDG = 07h for GAIN2; 0Ah for GAIN3; 0Dh for GAIN4*

GAINx: Current gain value for channel x.

8.3.5 PWM and GAIN status registers (PWMH_STS, PWML_STS, GAIN_STS)

These read only registers report the actual PWM and GAIN values computed and applied to the outputs when ALED7709x are in global and mixed mode.

In all the other operational modes the content of such STS registers is the copy of PWM1H/L and GAIN1.

Table 26. PWMH_STS register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 0Eh	PWM_H							
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R	R	R	R	R	R	R	R

PWM_H: Highest PWM value computed from mixed mode and applied to all the channels.

Table 27. PWML_STS register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 0Fh	PWM_L							
POR A = 00h	0	0	0	0	0	0	0	0

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	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R	R	R	R	R	R	R	R

PWM_L: Lowest PWM value computed from mixed mode and applied to all the channels.

Table 28. GAIN_STS register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add 10h	GAIN							
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R	R	R	R	R	R	R	R

GAIN: Current gain value computed from mixed mode and applied to all the channels.

8.3.6 Channels configuration register (CHCFG)

This register is used to enable/disable the channels in operation mode.

Bit CH_XCH_{X+1} set allows to short the 2 adjacent channels and skip the execution of the specific channel to channel initial fault test.

These bits have no influence in operation mode.

Bit CEN_X set defines the related channel to be ON and so the initial channel to ground test is executed and considered. In standby or operational mode, the initial tests are no longer possible.

In operation mode CEN_X bits act as channel ON/OFF.

Table 29. CHCFG register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add 11h	Reserved	CH3CH4	CH2CH3	CH1CH2	CEN4	CEN3	CEN2	CEN1
POR A = 0Fh	0	0	0	0	1	1	1	1
POR B = 7Fh	0	1	1	1	1	1	1	1
Comments	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CEN_X: Channel x control

- 0: Channel OFF
- 1: Channel ON

CH_XCH_{X+1}: Channel x and Channel x+1 HW configuration

- 0: Normal configuration, channels are independent. Initial fault test result is stored.
- 1: The 2 channels can be shorted by HW. Initial fault test is not considered

8.3.7 Output configuration register (OUTCFG)

Table 30. OUTCFG register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add 12h	OCS[1:0]		PSE[1:0]		TPOINT[1:0]		TSA	Reserved
POR A = 00h	0	0	0	0	0	0	0	0

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	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR B = 3Eh	0	0	1	1	1	1	1	0
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-

TSA: Temperature sensing selection (channel current reduction controlled by external NTC circuit)

- 0: Disable
- 1: Enable

TPOINT[1:0]: Transition point for mixed dimming

- 00: 12.5%
- 01: 25%
- 10: 37.5%
- 11: 50%

PSE[1:0]: Phase shift mode selection

- 00: Disable
- 01: 64 clock staggered delay
- 10: CH1&CH2 – CH3&CH4 180° phase shift
- 11: CH1 – CH2 – CH3 – CH4 90° phase shift

OCS[1:0]: Output control slope selection

- 00: Nominal (100 ns typ.)
- 01: 2xNom
- 10: 4xNom
- 11: 8xNom

8.3.8 DC-DC converter configuration register (BOOSTCFG)

Table 31. BOOSTCFG register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add 13h	FSW[1:0]		DCLKMS[1:0]		Reserved	OVRE	DCLK_DIS	DFSW_DIS
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 06h	0	0	0	0	0	1	1	0
Comments	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

DFSW_DIS: Disable spread spectrum for F_{SW} set by external resistor

- 0: Enable
- 1: Disable

DCLK_DIS: Disable spread spectrum for main clock

- 0: Enable
- 1: Disable

OVRE: Output voltage regulation

- 0: Disable
- 1: Enable

DCLKMS[1:0]: Spread spectrum for main clock modulation selection

- 00: ±4.75%
- 01: ±9.15%
- 10: ±14.0%
- 11: ±2.35%

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FSW[1:0]: Converter switching frequency selection

- 00: F_{SW} defined by external resistor
- 01: CLK_{INT} / 16 => 409 kHz
- 10: CLK_{INT} / 8 => 819 kHz
- 11: CLK_{INT} / 4 => 1638 kHz

Note: FSW[1:0] are critical device configuration bits. DO NOT change them on the fly.

8.3.9 Dimming configuration register (DIMCFG)

Table 32. **DIMCFG register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add 14h	REG_PWMI	PWMI_DRCT	FDIM[2:0]			LECC	UMDM	GLDM
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 06h	0	0	0	0	0	1	1	0
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

GLDM: Global-local dimming mode selection

- 0: Global mode
- 1: Local mode

UMDM: User-mixed dimming mode selection

- 0: User dimming mode
- 1: Mixed dimming mode

LECC: Linear-exponential conversion curve

- 0: Linear conversion
- 1: Exponential conversion

FDIM[2:0]: PWM dimming frequency selection

- 000: $CLK_{INT} / 2^{16}$ => 100 Hz
- 001: $CLK_{INT} / 2^{15}$ => 200 Hz
- 010: $CLK_{INT} / 2^{14}$ => 400 Hz
- 011: $CLK_{INT} / 2^{13}$ => 800 Hz
- 100: $CLK_{INT} / 2^{12}$ => 1600 Hz
- 101: $CLK_{INT} / 2^{11}$ => 3200 Hz
- 110: $CLK_{INT} / 2^{10}$ => 6400 Hz
- 111: $CLK_{INT} / 2^{9}$ => 12800 Hz

PWMI_DRCT: PWMI way of usage

- 0: PWMI used to get period and duty-cycle
- 1: PWMI direct control of output

REG_PWMI: Brightness control selection

- 0: PWMI driven
- 1: Registers driven

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8.3.10 Fault-management configuration register (FMCFG)

Table 33. **FMCFG register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 15h	Reserved	Reserved	LSWE	FALT	OCAD	SCAD	SH_DIS	Reserved
POR A = 01h	0	0	0	0	0	0	0	1
POR B = 69h	0	1	1	0	1	0	0	1
Comments	-	-	R/W	R/W	R/W	R/W	R/W	-

SH_DIS: LED short-circuit detection disable
- 0: Enable
- 1: Disable

SCAD: Shorted channels auto-disconnection
- 0: Disable
- 1: Enable

OCAD: Open channels auto-disconnection
- 0: Disable
- 1: Enable

FALT: Fault pin Latch selector
- 0: Fault pin not latched (real-time faults indicator)
- 1: Fault pin latched

LSWE: External PMOS control circuit and Input OVP
- 0: PMOS not driven and Input OVP disabled
- 1: PMOS driven and Input OVP enabled

8.3.11 Fault mask register (FMASK)

This register is used to mask which Status indication bit in register DEVSTA activates the FAULT pin

Table 34. **FMASK register**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 16h	IOCP_M	IOVP_M	CHCK_M	OTEA_M	LEDF_M	OOVP_M	THSD_M	Reserved
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 10h	0	0	0	1	0	0	0	0
Comments	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-

THSD_M: Thermal shutdown to FAULT mask
- 0: Not masked
- 1: Masked

OOVP_M: Output overvoltage to FAULT mask
- 0: Not masked
- 1: Masked

LEDF_M: LED fault to FAULT mask
- 0: Not masked
- 1: Masked

OTEA_M: Overtemperature early alert to FAULT mask
- 0: Not masked

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- 1: Masked

CHCK_M: Initial channels check failure to FAULT mask

- 0: Not masked
- 1: Masked

IOVP_M: Input overvoltage to FAULT mask

- 0: Not masked
- 1: Masked

IOCP_M: Input overcurrent to FAULT mask

- 0: Not masked
- 1: Masked

8.3.12 Device status register (DEVSTA)

The DEVSTA register is a read only status register. All the bits in the DEVSTA register are latched. They are cleared only writing CLRF = 1 or by a POR.

Table 35. DEVSTA register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 17h	IOCP	IOVP	CHCK	OTEA	LEDF	OOVP	THSD	Reserved
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R	R	R	R	R	R	R	-

THSD: Thermal shutdown indicator

- 0: Normal
- 1: Active (Fault)

OOVP: Output overvoltage indicator

- 0: Normal
- 1: Active (Fault)

LEDF: LED fault indicator

- 0: No Fault (CHSTA = 00h)
- 1: Fault (CHSTA != 00h)

OTEA: Overtemperature early alert indicator

- 0: Normal
- 1: Active (Warning)

CHCK: Initial channels check failure indicator

- 0: No Fault (INITSTA = 00h)
- 1: Fault (INITSTA != 00h)

IOVP: Input overvoltage indicator

- 0: Normal
- 1: Active (Fault)

IOCP: Input overcurrent indicator

- 0: Normal
- 1: Active (Fault)

8.3.13 Channel status register (CHSTA)

The CHSTA register is a read only status register. Each bit of this register shows the status of the corresponding channel. The channels having an excessive voltage drop (LEDs short-circuit) or not able to regulate the nominal current (open channels) are tagged as faulty and the related CHSTA bits are asserted.

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The CHCFG register is not affected by the error detection. The channels disabled by clearing the corresponding CEN bits of the CHCFG register are not involved in the error detection and the corresponding bits of the CHSTA register are forced low. The CHSTA register is automatically overwritten during subsequent error detection occurrences.

If at least one bit of the CHSTA register is asserted because of an error detection, the LEDF bit of the DEVSTA register is set and the FAULT pin is tied high if not masked by the LEDF_M bit of the FMASK register. The CHSTA register and FAULT pin are reset by setting the CLRF bit of DEVCFG or by performing a POR.

Table 36. CHSTA register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 18h	SH4	SH3	SH2	SH1	OP4	OP3	OP2	OP1
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R	R	R	R	R	R	R	R

OP_X: Channel x open LED indicator

- 0: Channel is working properly, or it is not used (CEN_X = 0)
- 1: OPEN channel detected

SH_X: Channel x LED short-circuit indicator

- 0: Channel is working properly, or it is not used (CEN_X = 0)
- 1: LEDs short-circuit detected

8.3.14 Initial fault status register (INITSTA)

The INITSTA register is a read only status register. Each bit of this register shows the result of the Initial Fault tests performed during the startup sequence.

If at least one bit of the INITSTA register is asserted after the Initial Fault Check sequence, the CHCK bit of the DEVSTA register is set and the FAULT pin is tied high if not masked by the CHCK_M bit of the FMASK register. The INITSTA register and FAULT pin are reset by setting the CLRF bit of DEVCFG or by performing a POR.

Table 37. INISTA register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Add = 19h	RISET	CH3-CH4	CH2-CH3	CH1-CH2	CH4GND	CH3GND	CH2GND	CH1GND
POR A = 00h	0	0	0	0	0	0	0	0
POR B = 00h	0	0	0	0	0	0	0	0
Comments	R	R	R	R	R	R	R	R

CH_XGND: Channel x short to GND

- 0: Normal
- 1: Channel x short to GND

CH_X-CH_{X+1}: Channel x and Channel x+1 short-circuit

- 0: Normal
- 1: Channels in short-circuit

RISET: External resistor on ISET pin short to GND or too small value

- 0: Normal
- 1: Fault

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9 Variants

9.1 ALED7709A

This variant is the most generic one, it must be controlled through I^2C since at POR almost all registers are clean.

This means that ALED7709A stops in standby waiting to be configured and enters in operation mode once the DEN bit is set.

The only register with a not clean POR value (excluding Reserved bit) is the CHCFG, the value of 0Fh allows to execute all the initial fault checks. In any case it is allowed to short 2 adjacent channels or an unused channel to ground. If so, the initial fault procedure reports the found conditions, but the user can always check if the faults are the expected ones, clear the flag acting on CLRF bit, configuring the device and run the operation setting DEN bit.

9.2 ALED7709B

This variant is configured to be able to run without the support of any microcontroller; even if the I^2C bus is not removed from the device and so, if needed, it can be used also with this device variant.

Register DEVEN is configured for moving the device directly in operation mode since the DEN bit is set by default.

To allow the possibility of shorting adjacent channels the initial fault check has been removed (CHCFG register set to 7Fh); this to avoid any fault detection, which blocks the device in standby, that without I^2C communication looks like a stuck condition. All the channels are enabled by default and so the initial check to verify if the channel is short to ground is executed and recorded. This means that unused channels cannot be shorted to ground if there is not any I^2C communication which can override the fault detected.

Unused channels can be left open, during the normal operation such channels are detected as OPEN and the Fault is notified, but the device is configured with OCAD bit set (auto-disconnection of OPEN faulty channels) so that once the fault is confirmed the channel is switched OFF and the device goes back to normal operation with less active channels.

FAULT pin is set in not latched mode so that it can notify only FAULT currently present and not something past and fixed.

The only masked notification to FAULT pin is overtemperature alarm since it is just a warning and not a real Fault.

The selected working mode is M5, as for Table 15 .

Phase shift is defined at 90º, transition point at 50%, the converter frequency must be set by external resistor so that it is allowed also the synchronization by external signal. The adaptive algo is active as well the spread spectrum for the converter. PMOS is driven, so the resistor between ICSN and PSW pins is required, but if a simpler/cheaper application is wanted, the PMOS could be not assembled; as well NTC circuit is enabled but it can be inhibited simply connecting TSNS pin to LDO3V3.

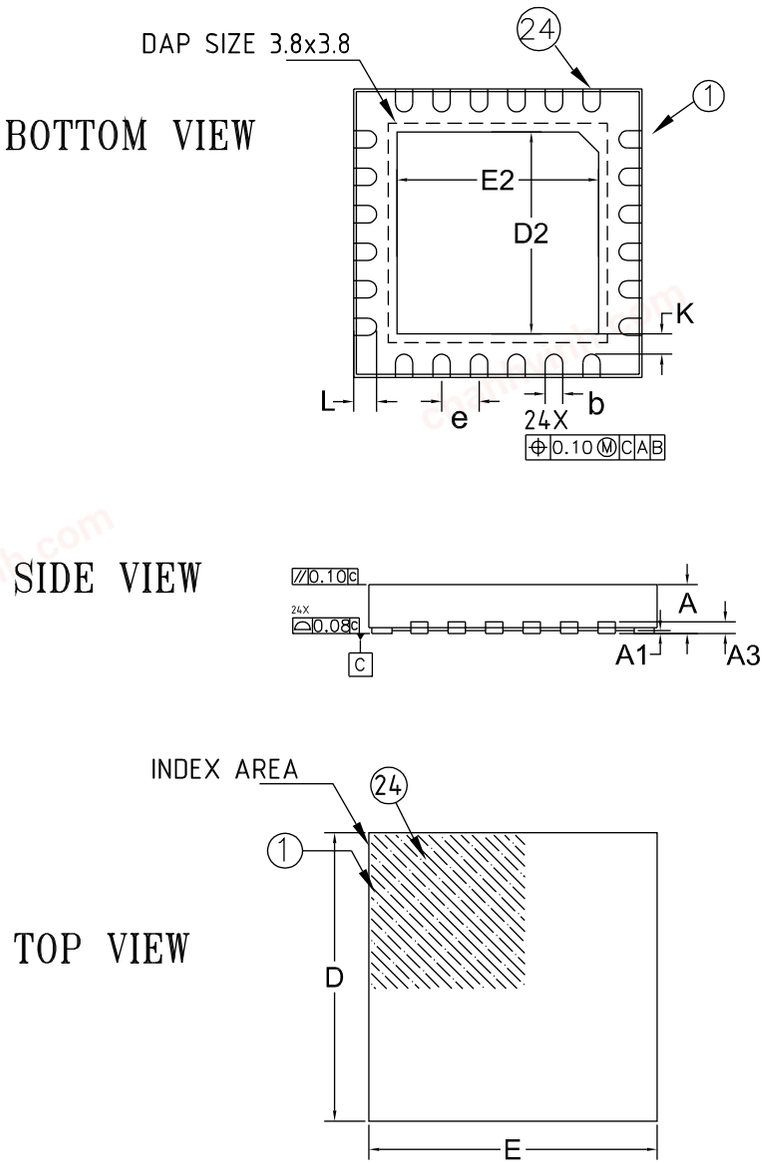
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10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 QFN24L (5x5 mm) package information

Figure 28. QFN24L (5x5 mm) package outline

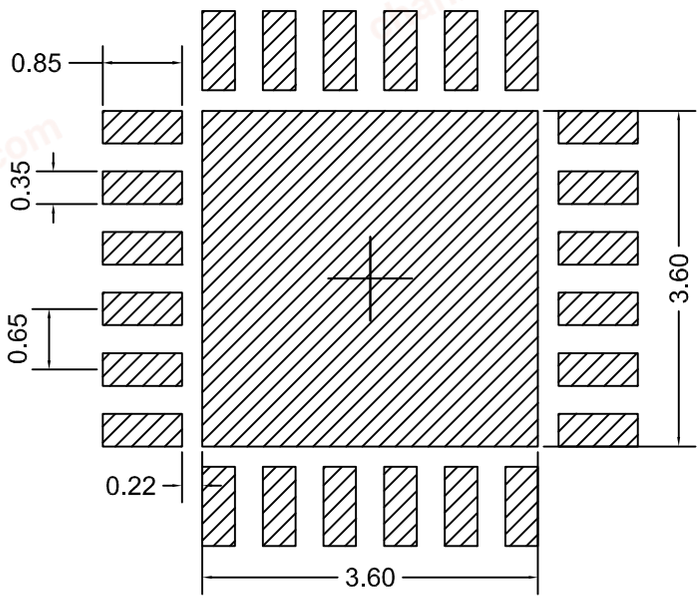


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Table 38. **QFN24L (5x5 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00	-	0.05
A3		0.203 Ref.	
b	0.25	0.30	0.35
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.65 BSC	
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
K		0.35 Ref.	
L	0.30	0.40	0.50
N		24	

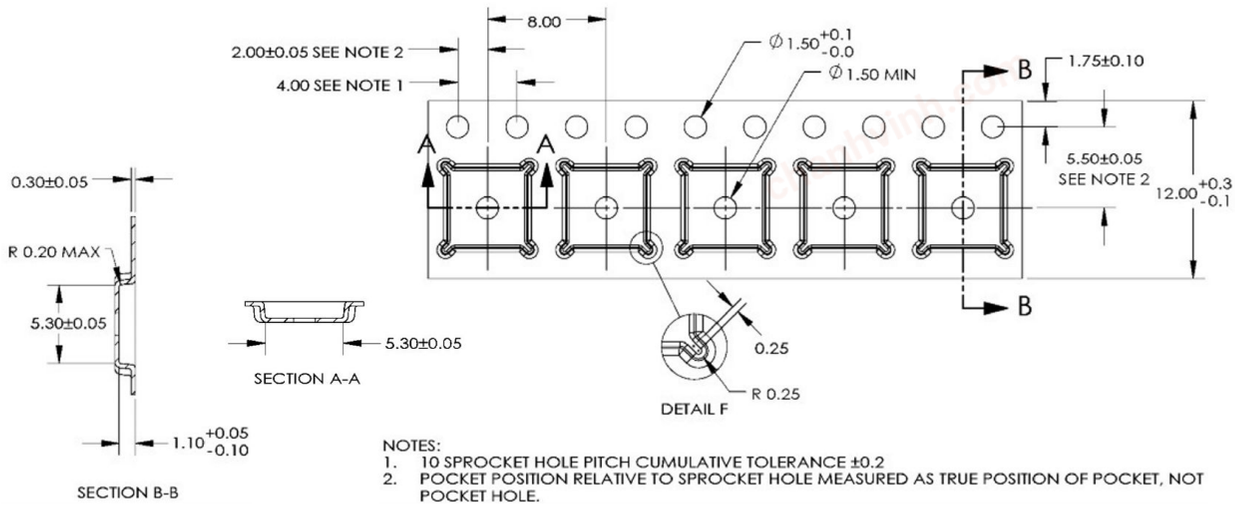
Figure 29. **QFN24L (5x5 mm) recommended footprint (dimensions are in mm)**



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10.2 QFN24L (5x5 mm) packing information

Figure 30. **QFN24L (5x5 mm) carrier tape outline (dimensions are in mm)**



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11 Ordering Information

Table 39. **Order codes**

Order code	Marking
ALED7709ATR	ALED7709A
ALED7709BTR	ALED7709B

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Revision history

Table 40. **Document revision history**

Date	Revision	Changes
13-Feb-2023	1	Initial release.
24-Apr-2023	2	Updated Table 16. ALED7709A register map Added Table 17. ALED7709B register map
10-May-2023	3	Minor text changes.
20-Jun-2023	4	Updated title on the cover page.

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