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UG498: Si858x-EVB User's Guide

The Si858x EVB is designed for the functionality and performance evaluation of the isolated RS-485 transceiver.

The board provides the MCU host interface and RS-485 cable interface to connect the Si858x transceiver to the RS-485 bus/network. The Si858x product family integrates Skyworks' proprietary CMOS digital isolator and standard RS-485 transceiver into a small-footprint and low power consumption solution. The Si858x supports up to 5 kVrms isolation voltage. The nature of this isolation provides a very high CM (common-mode) impedance between the main controller and the RS-485 bus. The high CM impedance makes the Si858x the ideal solution for high-voltage safety isolation systems and environments characterized by harsh CM noise or low CM EMI radiation requirements.

Various Si858x EVB ordering part numbers (OPNs) are available to evaluate the performance of different product family options. The block diagram and functionality later described in this user's guide are universal to all Si858x EVBs. The physical layer performance varies depending on the Si858x chip present on the EVB.

The Si858x EVB provides connector interfaces for the signal and power connections on both the host and bus sides. Several jumper headers are used to select the standalone loopback test mode or to enable the onboard 120 Ω ac termination. Status indicator LEDs and test points make evaluation and prototyping easy. The figure below shows the Si858x full-duplex/half-duplex ISO-RS485 EVB.

KEY FEATURES

- Si858x isolated RS-485 transceiver
- Compliance to TIA/EIA-485-A (RS-485) and EN 50170 (ProfiBus)
- 5 kVrms safety rated isolation
- Up to 10 Mbps data rate
- RS-485 bus signal slew rate control (on 1 Mbps data rate device)
- Onboard optional 120 Ω ac termination
- 100 kV/µs common mode transient immunity (CMTI) performance
- 128/256 Unit Load (UL) support
- Half/full duplex communication
- Flexible isolated power supplies
- Reverse polarity protection for input supplies

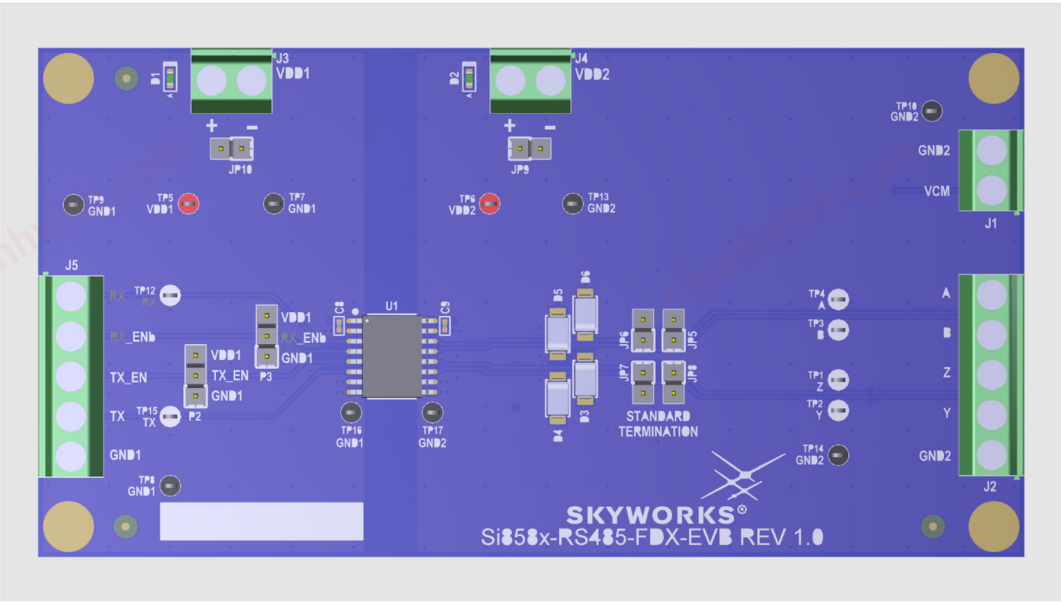

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Table of Contents

1. Block Diagram 3
2. Identifying EVB Ordering Part Number (OPN) 4
3. Connectors, LEDs, and Jumper Settings 5
4. Powering up the EVB 7
5. RS-485 Bus Interface Connection and Optional AC Termination 8
6. Controller Interface Connection 10
7. Standalone Loopback Mode 11
8. Current Consumption Measurement 13
9. Si858x-HDX-EVB Schematics 14
10. Si858x-HDX-EVB Bill of Materials 15
11. Si858x-FDX-EVB Schematics 16
12. Si858x-FDX-EVB Bill of Materials 17

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1. Block Diagram

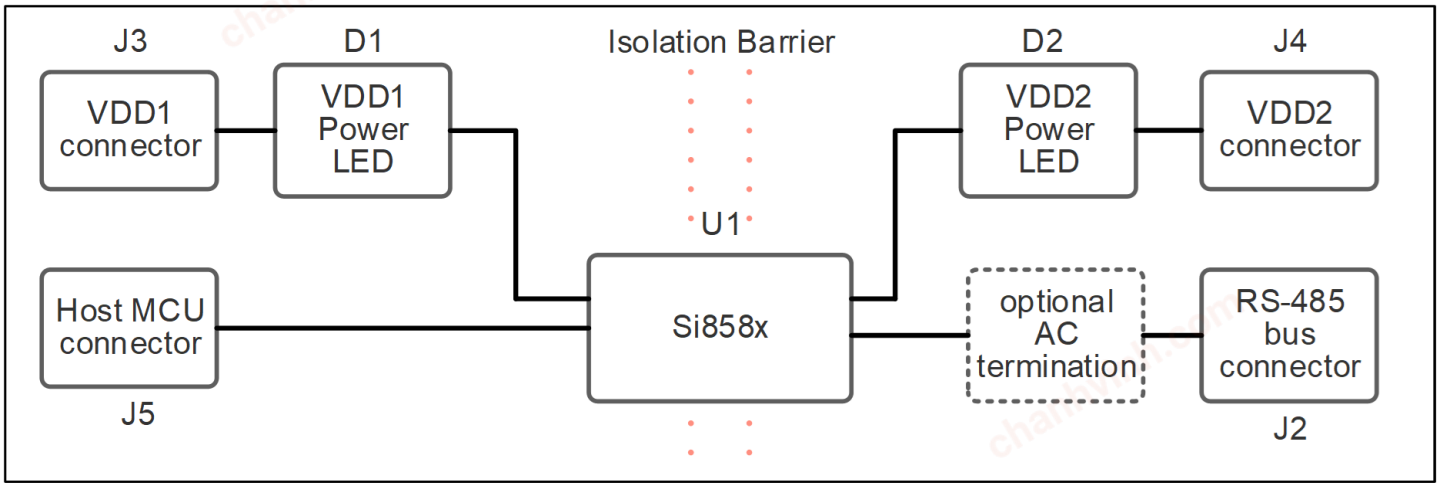

Figure 1.1. Si858x Full-Duplex/Half-Duplex EVB Block Diagram

The EVB contains the Si858x chip, the power connectors, the host MCU connector, and the RS-485 bus connector. The functionality of the Si858x is similar to other RS-485 compliant transceivers, except that it provides signal isolation. Since the Si858x is an isolated RS-485 transceiver, two power supplies are needed to operate the board.

The following figure shows a typical connection for interfacing with an MCU controller and RS-485 network.

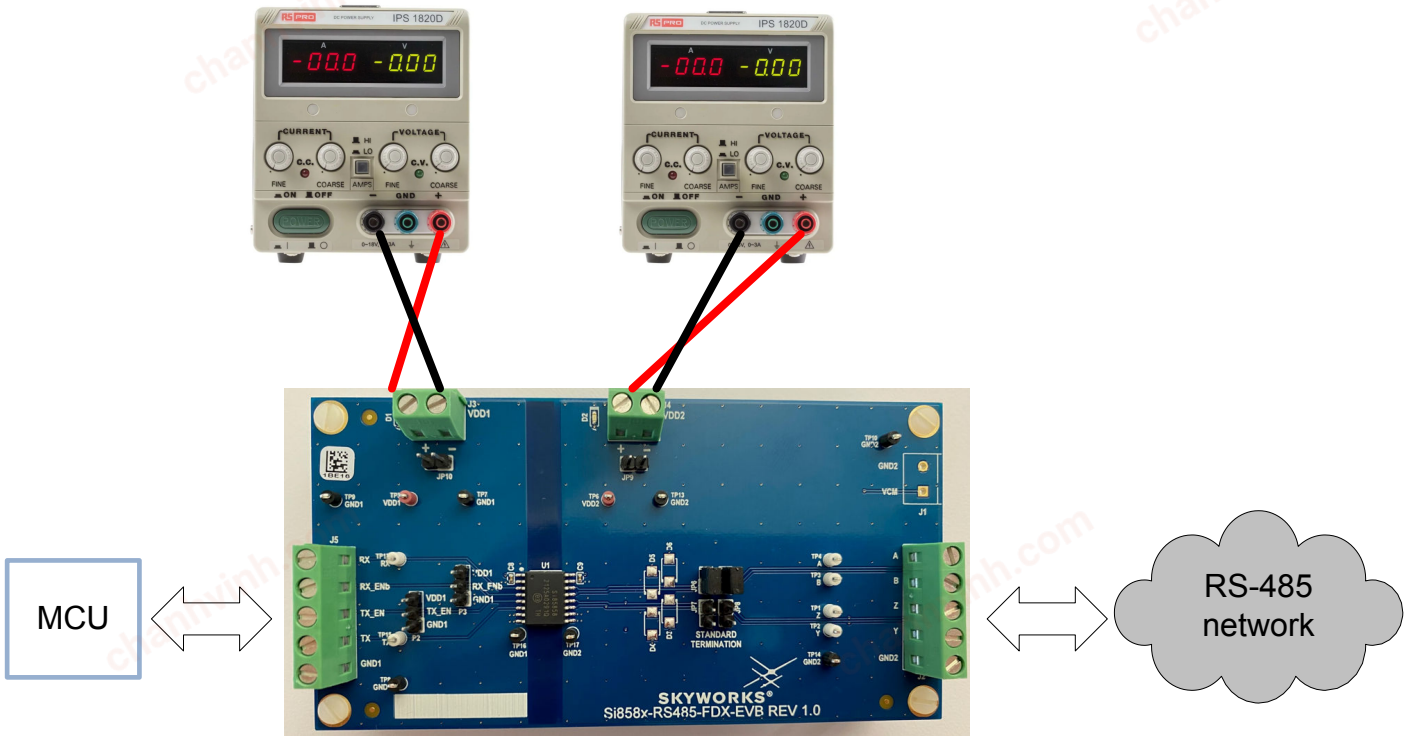

Figure 1.2. Si858x Typical Connection with an MCU and RS-485 Network

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2. Identifying EVB Ordering Part Number (OPN)

This user's guide covers a range of Si858x EVB options. Since there are many board variations, it is suggested that users first identify the EVB ordering part number from the OPN label. There are two major types of Si858x EVBs: full-duplex (FDX) and half-duplex (HDX). The full-duplex EVB supports the separate differential pairs for bus signal transmission and reception. By contrast, the half-duplex EVB uses the same differential pair for bus signal transmission and reception.

Each type of EVB also includes several board variants based on the Si858x chip being populated on the EVB. The label on the PCB can be used to identify the exact board variant, as shown in the following figure.



Figure 2.1. Example EVB Label String

Table 2.1. EVB Label Strings

EVB Label String	Si858x Part Number	RS-485 Configuration	Nodes	Slew Rate Control/ Data Rate	VDD1	VDD2
Si85853-EVB	Si85853D-IS	Half Duplex	256	Yes / 1 Mbps	3 ~ 5.5 V	5 V
Si85833-EVB	Si85833D-IS	Half Duplex	128	Yes / 1 Mbps	3 ~ 5.5 V	3.3 V
Si85855-EVB	Si85855D-IS	Half Duplex	256	No / 10 Mbps	3 ~ 5.5 V	5 V
Si85835-EVB	Si85835D-IS	Half Duplex	128	No / 10 Mbps	3 ~ 5.5 V	3.3 V
Si85856-EVB	Si85856D-IS	Half Duplex with isolated Tx_EN pin	256	No / 10 Mbps	3 ~ 5.5 V	5 V
Si85836-EVB	Si85836D-IS	Half Duplex with isolated Tx_EN pin	128	No / 10 Mbps	3 ~ 5.5 V	3.3 V
Si85857-EVB	Si85857D-IS	Full Duplex	256	Yes / 1 Mbps	3 ~ 5.5 V	5 V
Si85837-EVB	Si85837D-IS	Full Duplex	256	Yes / 1 Mbps	3 ~ 5.5 V	3.3 V
Si85858-EVB	Si85858D-IS	Full Duplex	256	No / 10 Mbps	3 ~ 5.5 V	5 V
Si85838-EVB	Si85838D-IS	Full Duplex	256	No / 10 Mbps	3 ~ 5.5 V	3.3 V

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3. Connectors, LEDs, and Jumper Settings

In the figure below, the Pin 1 position is marked, and the JP5 and JP6 jumpers are only available on a full-duplex Si858x EVB.

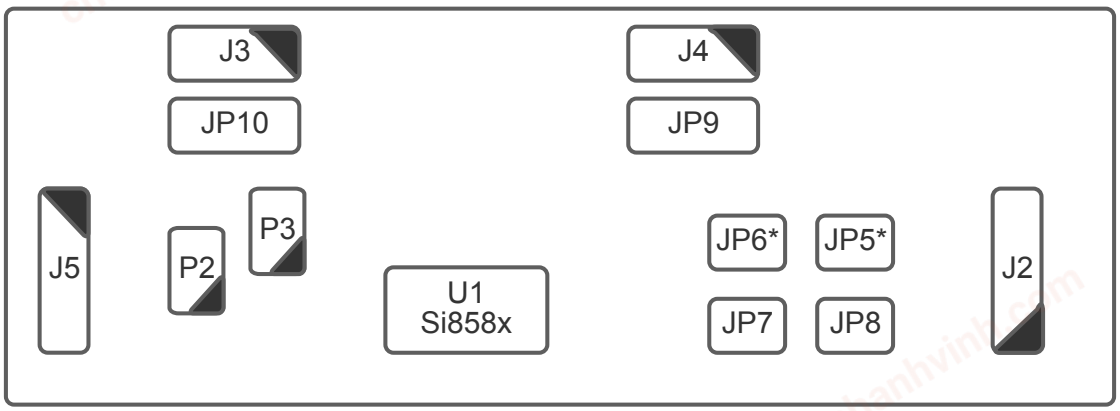

Figure 3.1. Connector and Jumper Position Diagram

Table 3.1. Si858x EVB Connector Description

Connector	Pin Number	Name	Description
J2	1	GND2	The isolated bus side reference ground, which can be used to connect the bus cable shield (if it exists).
	2	Y / NC	Full duplex EVB: Noninverting bus driver output pin Y. Half duplex EVB: NC.
	3	Z / NC	Full duplex EVB: Inverting bus driver output pin Z. Half duplex EVB: NC.
	4	B / A	Full duplex EVB: Inverting bus receiver input pin B.Half duplex EVB: Noninverting bus receiver input pin A.
	5	A / B	Full duplex EVB: Noninverting bus receiver input pin A.Half duplex EVB: Inverting bus receiver input pin B.
J3	1	GND1	The logic side reference ground.
	2	VDD1	The logic side VDD supply. Connect to 3.0 ~ 5.5 V voltage source.
J4	1	GND2	The isolated bus side reference ground.
	2	VDD2	The bus side VDD supply. Connect to either isolated 3.3 V or isolated 5 V voltage source.
J5	1	Rx	Bus received data output.
	2	Rx_ENb	Receiver enable signal (active low input).
	3	Tx_EN	Bus driver enable signal (active high input).
	4	Tx	Data input to the bus driver.
	5	GND1	The logic side reference ground.

Table 3.2. LED Indication

LED	Color	Description
D1	Green	Lit when the VDD1 supply on J3 is present
D2	Green	Lit when the VDD2 supply on J4 is present

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Table 3.3. Si858x EVB Jumper Settings

Setting Jumper	Default Setting	Description
JP5	Open	Short JP5 and JP6 together to enable the EVB on-board 120 Ω termination resistor for the bus driver. Only available on full-duplex EVB.
JP6	Open	
JP7	Open	Short JP7 and JP8 together to enable the EVB on-board 120 Ω termination resistor for the bus receiver.
JP8	Open	
JP9	Short	Short JP9 to bypass EVB VDD2 current sense resistor. When it is open, the voltage across JP9 can be used to measure the VDD2 input current.
JP10	Short	Short JP10 to bypass EVB VDD1 current sense resistor. When it is open, the voltage across JP10 can be used to measure the VDD1 input current.
P2	Pin 2–3	**Tx_EN Bus Driver Enable Signal** Place the jumper at Pin 1–2 position to tie Si858x Tx_EN signal to GND1. Place the jumper at Pin 2–3 position to tie Si858x Tx_EN signal to VDD1. Remove the jumper when feeding the external Tx_EN control signal from J5.
P3	Pin 1–2	**Rx_ENb Receiver Enable Signal** Place the jumper at Pin 1–2 position to tie the Si858x Rx_ENb signal to GND1. Place the jumper at Pin 2–3 position to tie the Si858x Rx_ENb signal to VDD1. Remove the jumper when feeding the external Rx_ENb control signal from J5.

Table 3.4. Si858x EVB Test Points

Test Point	Label	Description
TP1	Z / B	Full duplex EVB: Inverting bus driver output pin Z. Half duplex EVB: Inverting bus receiver input pin B.
TP2	Y / A	Full duplex EVB: Noninverting bus driver output pin Y. Half duplex EVB: Noninverting bus receiver input pin A.
TP3	B	Inverting bus receiver input pin B. Only available on full duplex EVB.
TP4	A	Noninverting bus receiver input pin A. Only available on full duplex EVB.
TP12	RX	Bus received data output.
TP15	TX	Data input to the bus driver.
TP5	VDD1	The logic side VDD supply.
TP6	VDD2	The bus side VDD supply.
TP7, TP8, TP9, TP16	GND1	The logic side reference ground.
TP10, TP13, TP14, TP17	GND2	The isolated bus side reference ground.
P2 pin 2	Tx_EN	Bus driver enable signal.
P3 pin 2	Rx_ENb	Receiver enable signal.
TP11	ISO_TX_EN	The output signal on the bus side as the isolated version of the Tx_EN signal. Only available on Si85856 and Si85836 EVBs.

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4. Powering up the EVB

Two isolated voltage power supplies for VDD1 and VDD2, respectively, are required to power up the Si858x EVB. No software is required to operate the board.

VDD1 accepts a voltage level ranging from 3 V to 5.5 V. VDD2 should be either 3.3 V or 5 V depending on the part number of Si858x chip set being populated on the EVB. Please use the EVB label string in Figure 2.1 Example EVB Label String on page 4 to look up the correct VDD2 voltage level from Table 2.1 EVB Label Strings on page 4. There is no special power-up sequence for the Si858x EVB.

VDD1 and VDD2 current consumption should be less than 100 mA. The EVB implements input voltage polarity protection. If a voltage of reverse polarity is applied to VDD1 or VDD2 (e.g., –5 V), it will be blocked from the Si858x power pins in order to avoid damage. The D1 and D2 LEDs indicate that voltage supplies with the correct polarity are present.

The onboard jumper shorts are used to configure the board for operation, which will be covered in the following sections. JP9 and JP10 are used to bypass the 1 Ω current measurement shunt resistor. The open or short status of JP9 and JP10 do not affect the EVB operation.

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5. RS-485 Bus Interface Connection and Optional AC Termination

The user should use the J2 connector for the bus wire connection of the RS-485 full/half duplex network. Table 3.1 Si858x EVB Connector Description on page 5 depicts the pin definition of the J2 connector.

The original RS-485 standard defines up to 32 transceivers in one network. Each Si858x EVB represents one node in the network. To evaluate the performance of the Si858x EVB, it requires at least two RS-485 nodes; otherwise, the Si858x needs to be configured in the standalone loopback mode.

Figure 5.1 RS-485 Half-Duplex Network Connection on page 8 and Figure 5.2 RS-485 Full-Duplex Network Connection on page 9 show the typical half-duplex and full-duplex RS-485 network connection. The full-duplex bus requires two separate pairs of bus wires, which allows data transmission and reception between two nodes to occur at the same time. The half-duplex bus only requires one pair of bus wires, but two communicating nodes should not transmit the data at the same time. Tx_EN and Rx_ENb signals are used to avoid signal contention in the RS-485 bus. The bus termination resistors (represented by R_T and located at both ends of the bus wires) serve to reduce signal reflections (edge overshoot or undershoot) in long wires and/or high-data-speed applications.

By the default jumper position, the 120 Ω onboard termination resistors are not enabled. If Si858x EVB is connected to the RS-485 bus in the middle of the cable, these termination resistors are not needed. When Si858x EVB is connected to the bus as the "end-point" in the long bus wires and/or the high data speed application, the on-board termination resistors can be enabled by shorting JP5~JP8. Please refer to Table 3.3 Si858x EVB Jumper Settings on page 6 for more details.

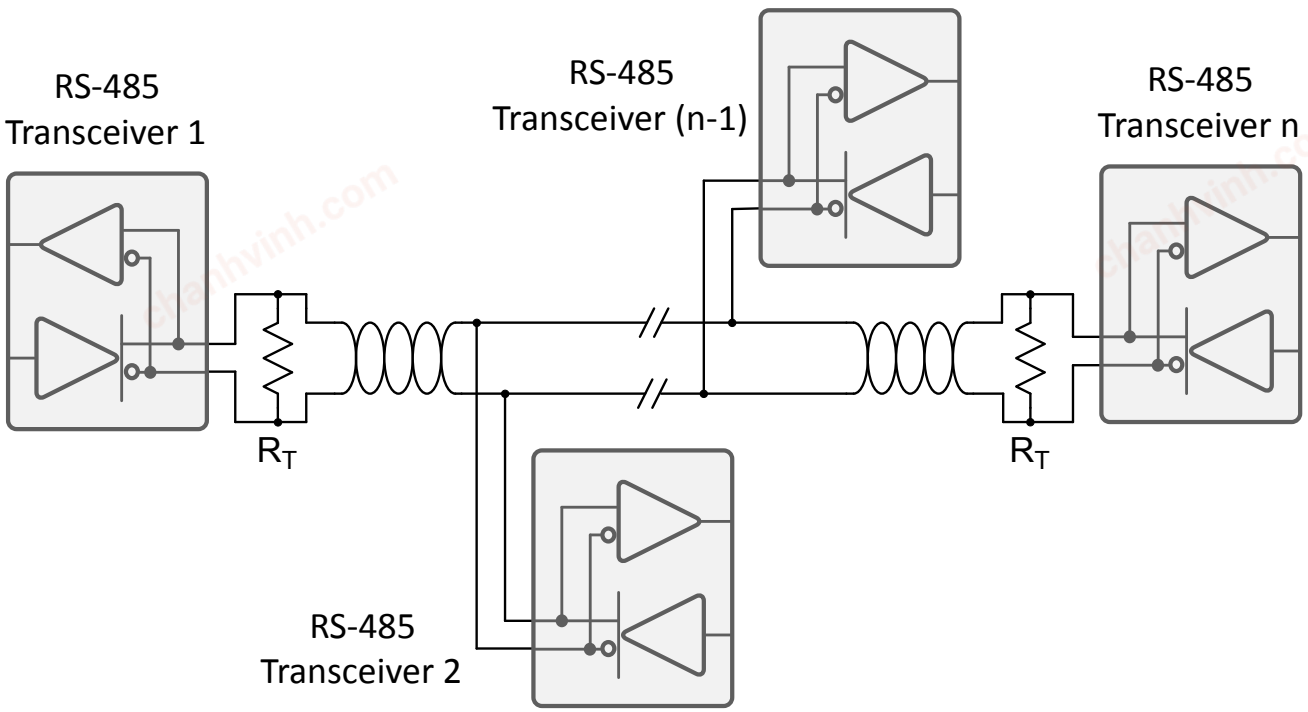

Figure 5.1. RS-485 Half-Duplex Network Connection

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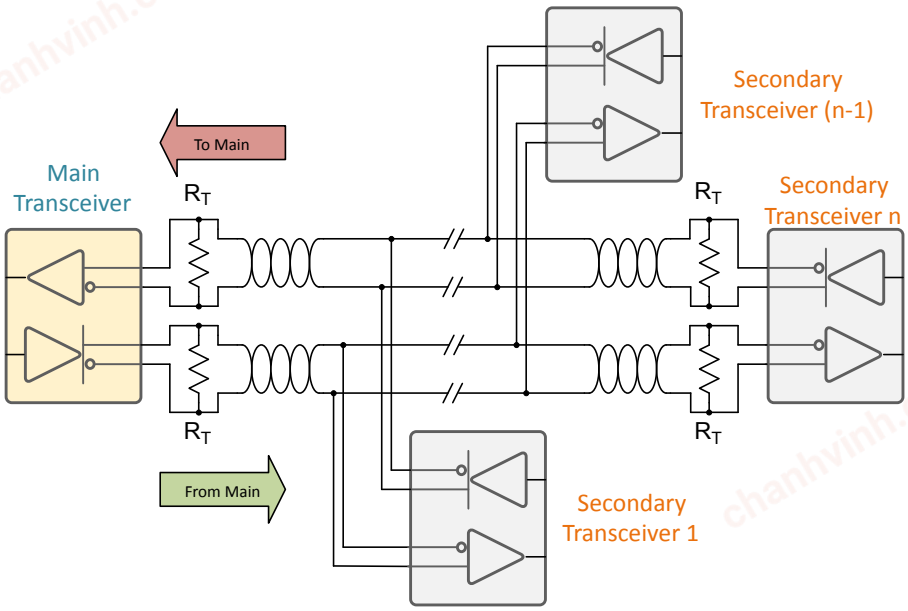

Figure 5.2. RS-485 Full-Duplex Network Connection

Please note that the user should understand whether the Si858x EVB is used as the main or secondary devices in the full duplex bus. Typically, there are only one main device and multiple secondary devices in the full duplex bus as shown in Figure 5.2 RS-485 Full-Duplex Network Connection on page 9. The receiver input pins of all secondary devices should be connected to the driver output pin of the main device and vice versa. Attention should be taken for the node's role in the full duplex connection to ensure the correct signal direction.

Pin 1 of the J2 connector is the reference ground for the isolated transceiver. This pin is not required to connect to RS-485 bus as the original standard mainly relies on the differential signals on the twisted pair. However, if the additional ground wire is utilized in the bus wiring, it is recommended that the ground wire be connected to the transceiver-side reference ground (GND2) instead of the controller-side reference ground (GND1). The following figure shows an example connection with the additional ground wire (green color) in the bus with the combination of isolated and non-isolated transceivers.

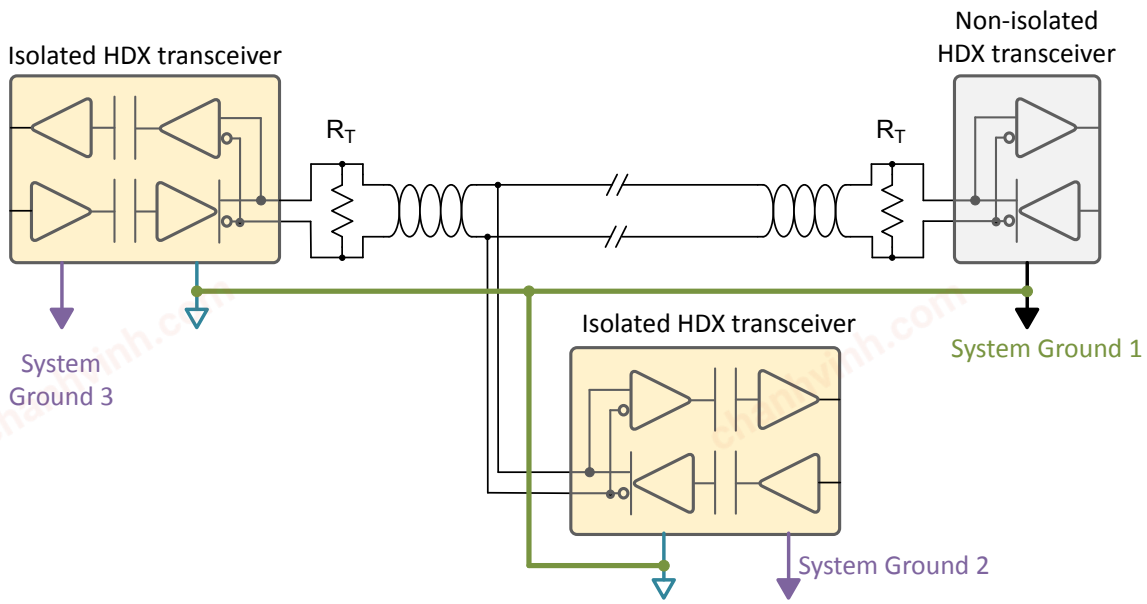

Figure 5.3. Example Connection of Isolated and Non-Isolated Transceivers with the Additional Ground (Green) Wire

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6. Controller Interface Connection

J5 is the host controller interface connector with the pin definition listed in Table 3.1 Si858x EVB Connector Description on page 5. The following figure shows an example connection with an 8051 MCU.

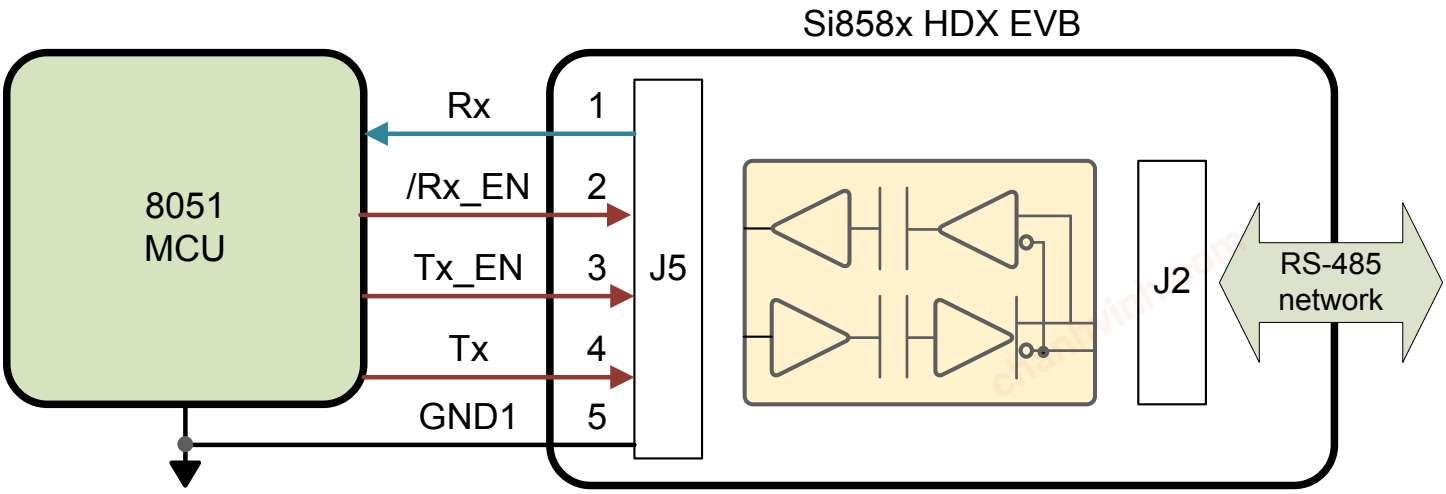

Figure 6.1. Example Connection of MCU and Si858x EVB

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7. Standalone Loopback Mode

Si858x EVB can also be evaluated by itself without connecting to the other RS-485 transceiver. This can be done by configuring the EVB in the standalone loopback mode. The data fed on Tx pin of J5 will be looped back and appear on Rx pin of J5. The standalone loopback mode is ideal for demonstration purposes.

By nature, the half-duplex Si858x EVB has the bus driver and receiver connected together inside the chip. As long as the EVB is detached to other RS-485 node, no special treatment is necessary to get the loop-back data. Because of that, we can simply use the function generator to provide the data on Tx pin of J5 to run the loopback test while Tx_EN = HIGH and Rx_ENb = LOW. Please also check Table 3.3 Si858x EVB Jumper Settings on page 6 for the jumper short positions on P2 and P3 for Tx_EN and Rx_ENb signals.

On the full-duplex Si858x EVB, in addition to detaching the EVB from other RS-485 nodes, the user should also connect J2 Pin 5 to Pin 2 and connect J2 Pin 3 to Pin 4 by the external wire. Below is the example connection to use the function generator to run the loopback test on the full-duplex Si858x EVB.

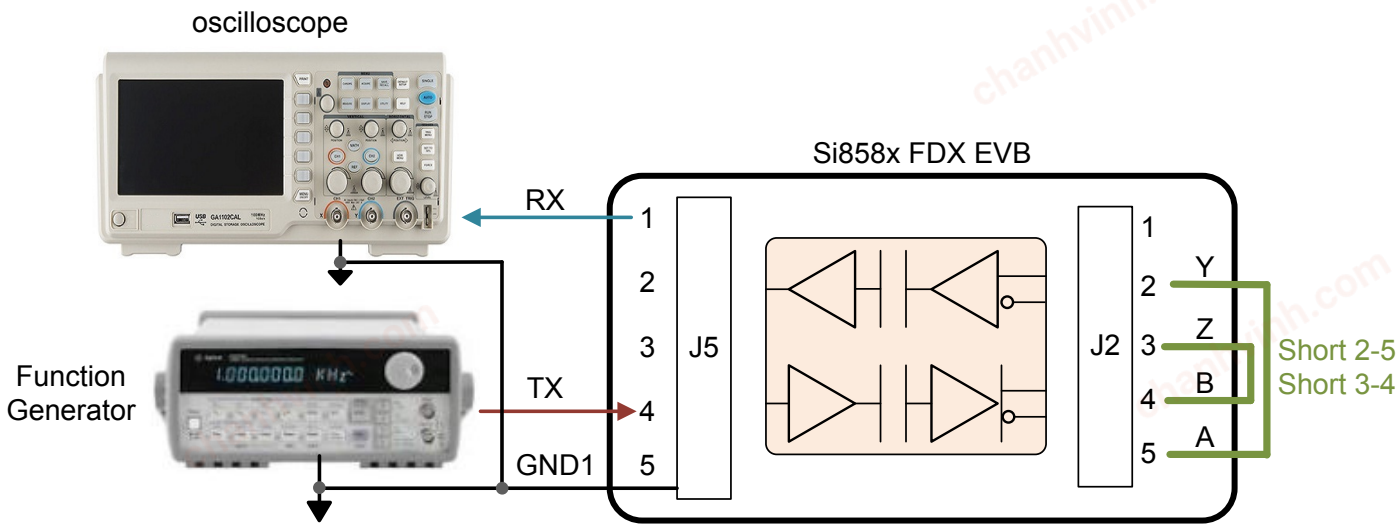

Figure 7.1. Example Connection of FDX Loopback Test Using the Function Generator

The figure below is the example scope waveforms of the Si858x FDX EVB loopback test. The 1 Mbps Tx data (yellow trace) was fed by the external function generator and the corresponding RS-485 bus signals were shown as the blue and red traces. Since the transmitting signal was looped back to the receiver, the identical data waveform was obtained at Rx pin (green trace) with certain data latency.

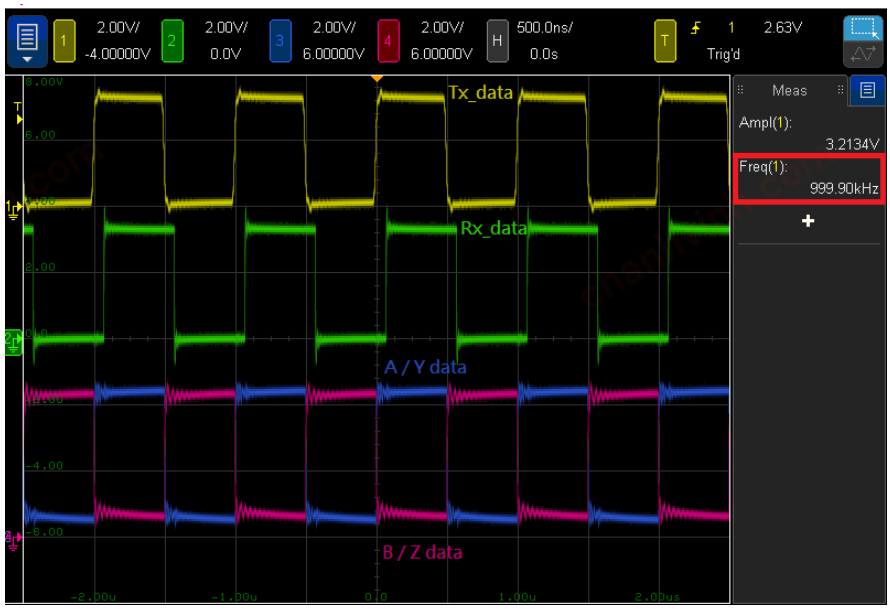

Figure 7.2. Example FDX Loopback Waveforms (Si85858 EVB with VDD1 = 3.3 V and VDD2 = 5 V)

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The figure below is the other example waveform of the Si85833 EVB configured in the loopback mode. The smooth signal transition can be seen on RS-485 bus wires due to the slew rate control feature.

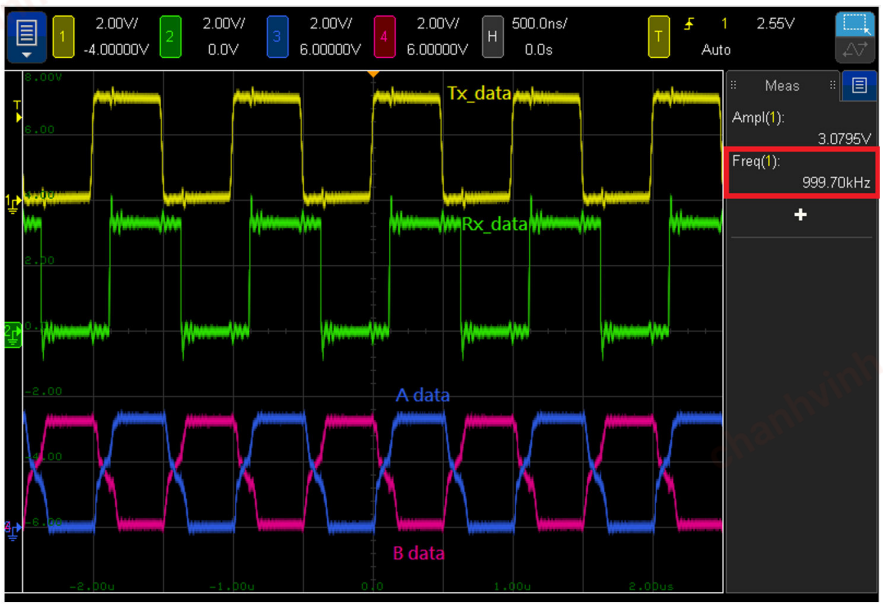

Figure 7.3. Example HDX Loopback Waveforms (Si85833 EVB with VDD1 = 3.3 V and VDD2 = 3.3 V)

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8. Current Consumption Measurement

The 1 Ω shunt resistors, on VDD1 and VDD2 respectively, can be used to measure the dc current consumption. By default, these two 1 Ω resistors are bypassed by the jumper short on JP9 and JP10, so they have no effect to the VDD power supply. After removing the jumper short on JP9 and JP10, the voltage meter can be used to measure the voltage across the resistor to obtain the dc current consumption.

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9. Si858x-HDX-EVB Schematics

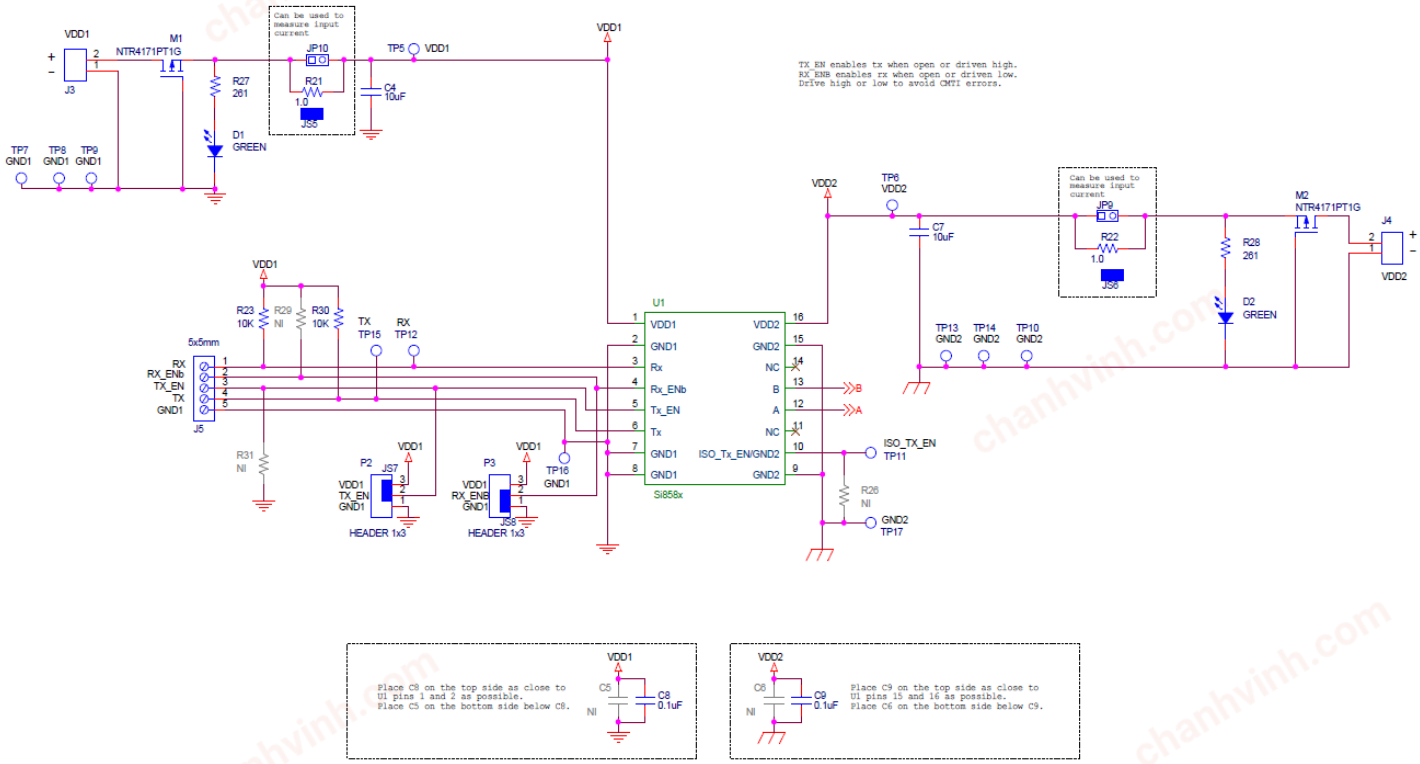

Figure 9.1. Si858x HDX EVB Schematics 1

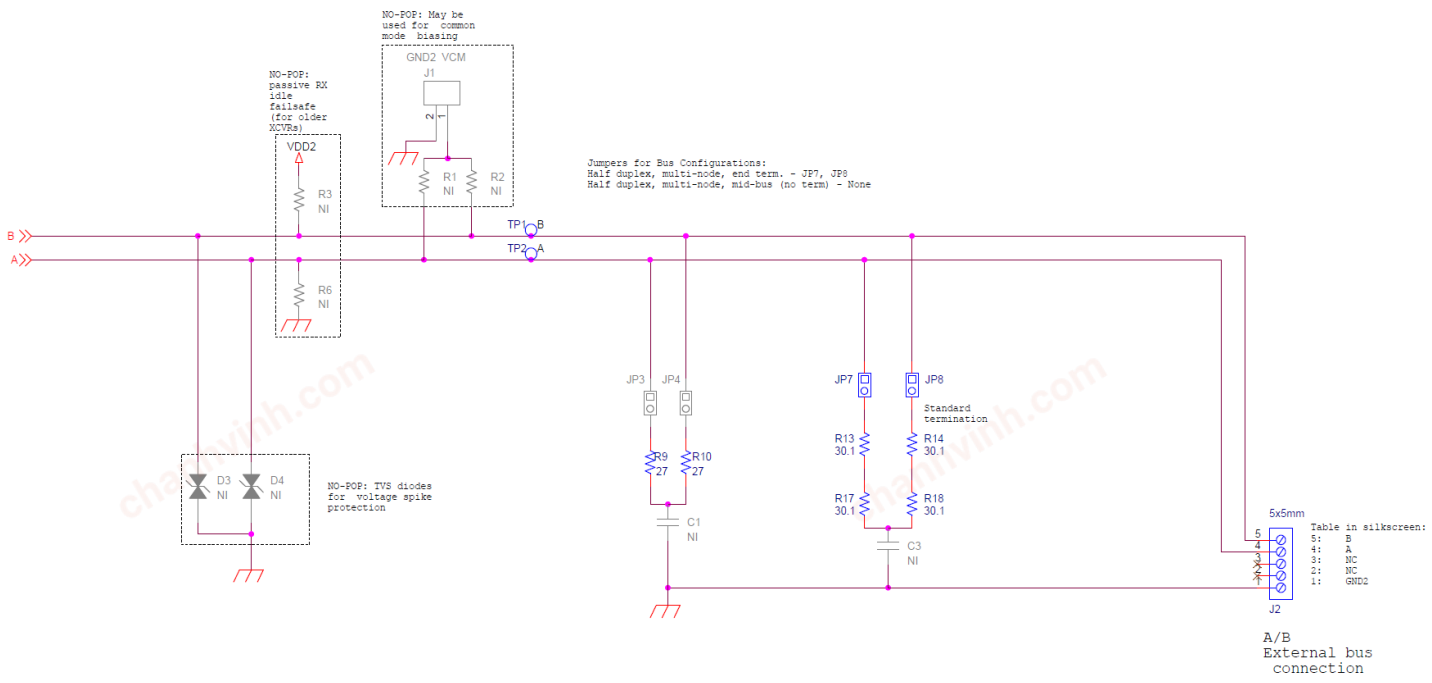

Figure 9.2. Si858x HDX EVB Schematics 2

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10. Si858x-HDX-EVB Bill of Materials

Table 10.1. Si858x HDX EVB Bill of Materials

Ref	Value	Rating	Voltage	PCB Footprint	Mfr Part Number	Mfr
C1, C3	4.7 nF		1 kV	C1206	GRM31BR73A472K	Murata
C4, C7	10 µF		10 V	C1206	C1206X7R100-106K	Venkel
C5, C6	0.1 µF		25 V	C0603	C0603X7R250-104K	Venkel
C8, C9	0.1 µF		16 V	C0402	C0402X7R160-104K	Venkel
D1, D2	Green	20 mA		LED-0603	LTST-C193TGKT-5A	Lite-On Technology Corp.
D3, D4	40 V	400 W	40 V	DO-214AC	SMAJ40CA	Diodes Inc.
JP3, JP4, JP7, JP8, JP9, JP10	Header 1 x 2			CONN1X2	TSW-102-07-T-S	Samtec
JS5, JS6, JS7, JS8	Jumper Shunt			N/A	SNT-100-BK-T	Samtec
J1, J3, J4	CONN TRBLK 2			CONN-1X2-TB	1729018	Phoenix Contact
J2, J5	5 x 5 mm	10 A	300 V	CONN-1X5-5MM-TB	1729047	Phoenix Contact
M1, M2	NTR4171PT1G	–3.5 A	–30 V	SOT23-GSD	NTR4171PT1G	ON Semiconductor
P2, P3	HEADER 1x3			CONN-1X3	TSW-103-07-L-S	Samtec
R1, R2	374 kΩ	1/8 W		R0805	ERJ-6ENF3740V	Panasonic
R3, R6	1.2 kΩ	1/8 W	150 V	R0805	CR0805-8W-1201F	Venkel
R9, R10	27 Ω	1/2 W		R1206	CRGP1206F27R	TE Connectivity
R13, R14, R17, R18	30.1 Ω	1/4 W		R1206	CR1206-4W-30R1F	Venkel
R21, R22	1 Ω	1/16 W		R0402	CR0402-16W-1R00F	Venkel
R23, R29, R30, R31	10 kΩ	1/10 W		R0603	CR0603-10W-1002F	Venkel
R26	0 Ω	1 A		R0402	CR0402-16W-000	Venkel
R27, R28	261 Ω	1/10 W		R0603	CR0603-10W-2610F	Venkel
TP1, TP2, TP11, TP12, TP15	White			Testpoint	151-201-RC	Kobiconn
TP5, TP6	Red			Testpoint	151-207-RC	Kobiconn
TP7, TP8, TP9, TP10, TP13, TP14, TP16, TP17	Black			Testpoint	151-203-RC	Kobiconn
U1	Si858x	5000 VRMS		SO16	Si85853D-IS	Skyworks Solutions, Inc.

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11. Si858x-FDX-EVB Schematics

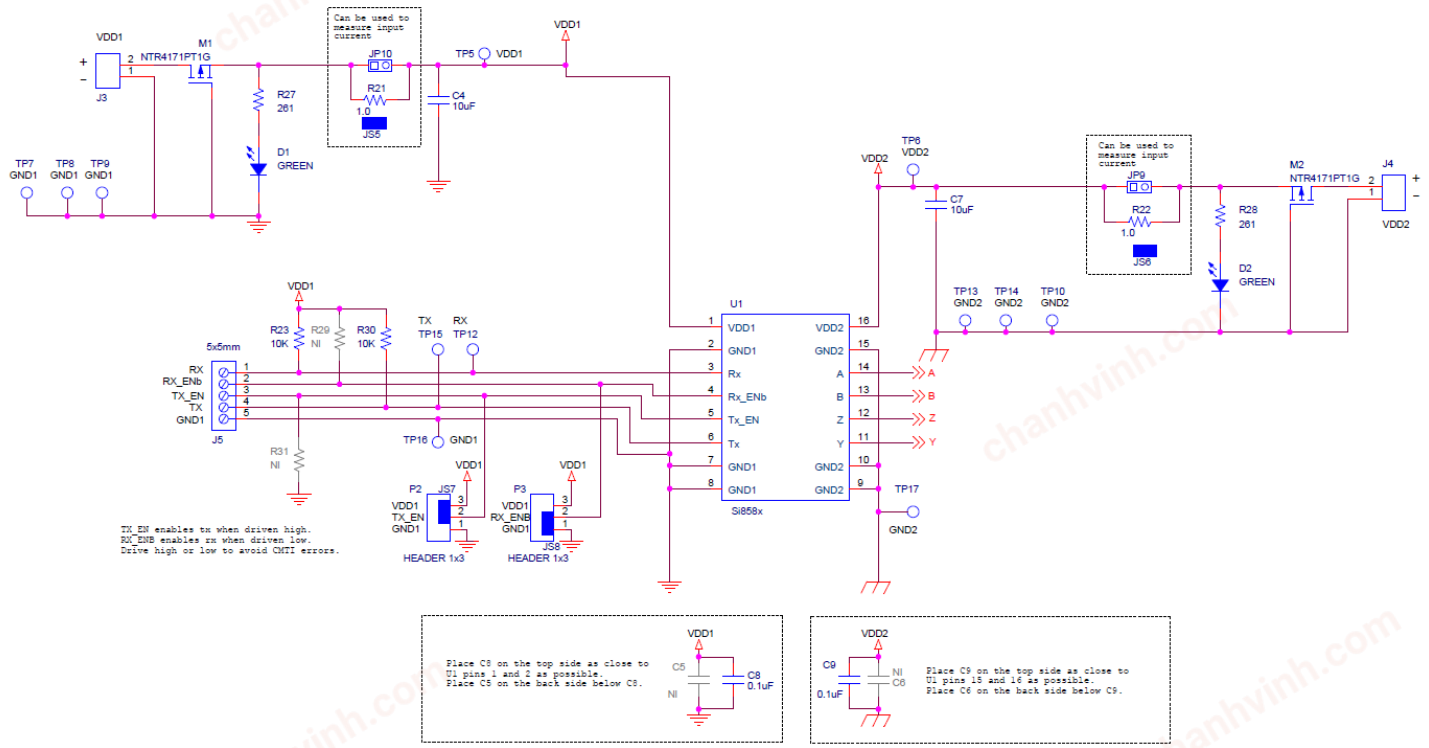

Figure 11.1. Si858x FDX EVB Schematics 1

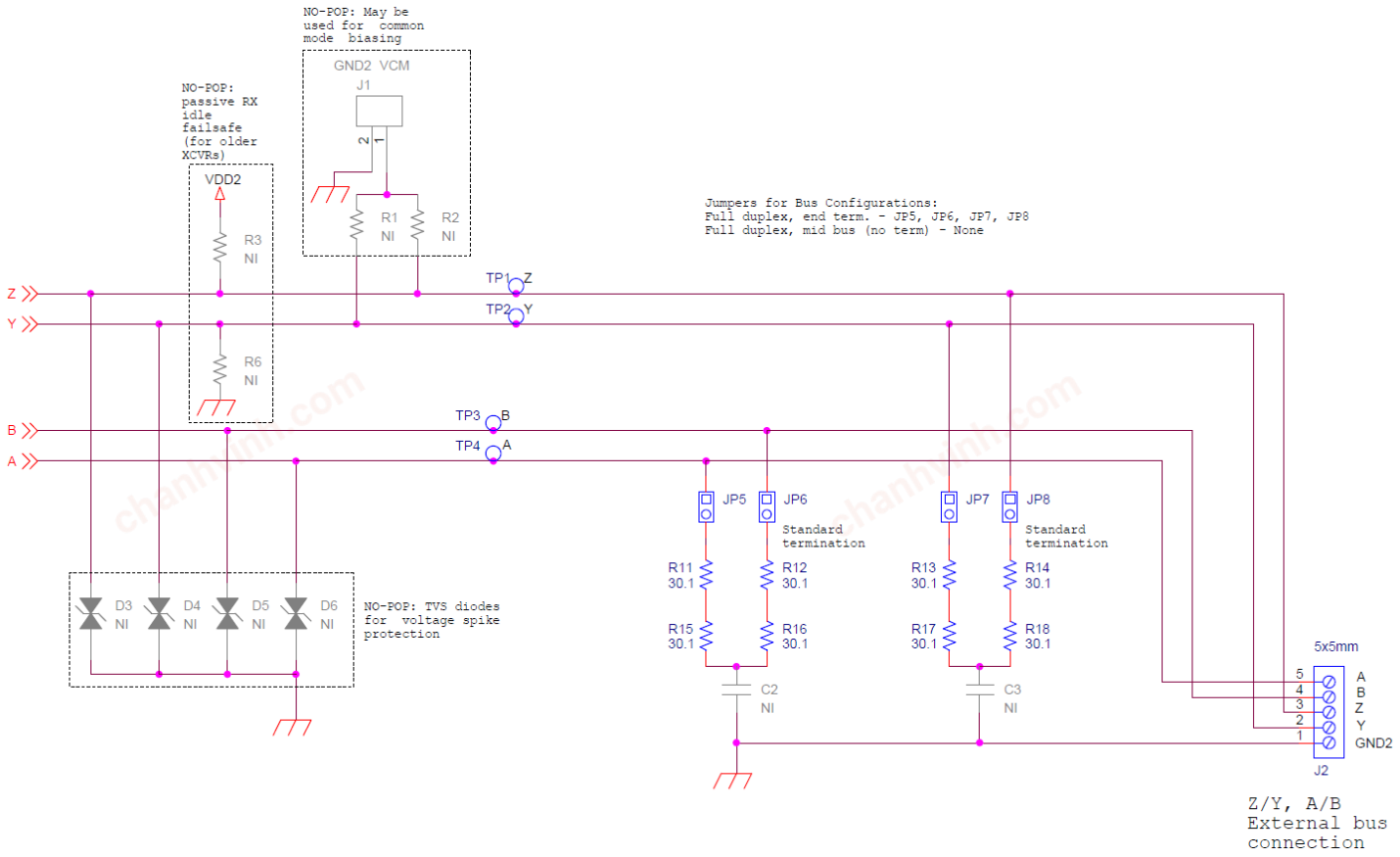

Figure 11.2. Si858x FDX EVB Schematics 2

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12. Si858x-FDX-EVB Bill of Materials

Table 12.1. Si858x FDX EVB Bill of Materials

Ref	Value	Rating	Voltage	PCB Footprint	Mfr Part Number	Mfr
C2, C3	4.7 nF		1 kV	C1206	GRM31BR73A472K	Murata
C4, C7	10 µF		10 V	C1206	C1206X7R100-106K	Venkel
C5, C6	0.1 µF		25 V	C0603	C0603X7R250-104K	Venkel
C8, C9	0.1 µF		16 V	C0402	C0402X7R160-104K	Venkel
D1,D2	Greed	20 mA		LED-0603	LTST-C193TGKT-5A	Lite-On Technology Corp.
D3, D4, D5, D6	40 V	400 W	40 V	DO-214AC	SMAJ40CA	Diodes Inc.
JP5, JP6, JP7, JP8, JP9, JP10	Header 1 x 2			CONN1X2	TSW-102-07-T-S	Samtec
JS5,JS6,JS7,JS8	Jumper Shunt			N/A	SNT-100-BK-T	Samtec
J1, J3, J4	CONN TRBLK 2			CONN-1X2-TB	1729018	Phoenix Contact
J2,J5	5 x 5 mm	10 A	300 V	CONN-1X5-5MM-TB	1729047	Phoenix Contact
MH1, MH2, MH3, MH4	Apr-40			MH-125NP	NSS-4-4-01	Richco Plastic Co.
M1, M2	NTR4171PT1G	–3.5 A	–30 V	SOT23-GSD	NTR4171PT1G	ON Semiconductor
P2, P3	Header 1 x 3			CONN-1X3	TSW-103-07-L-S	Samtec
R1, R2	374 Ω	1/8 W		R0805	ERJ-6ENF3740V	Panasonic
R3, R6	1.2 kΩ	1/8 W	150 V	R0805	CR0805-8W-1201F	Venkel
R11, R12, R13, R14, R15, R16, R17, R18	30.1 Ω	1/4 W		R1206	CR1206-4W-30R1F	Venkel
R21, R22	1 Ω	1/16 W		R0402	CR0402-16W-1R00F	Venkel
R23, R29, R30, R31	10 kΩ	1/10 W		R0603	CR0603-10W-1002F	Venkel
R27, R28	261	1/10 W		R0603	CR0603-10W-2610F	Venkel
SO1, SO2, SO3, SO4	Standoff				1902D	Keystone Electronics
TP1, TP2, TP3, TP4, TP12, TP15	White			Testpoint	151-201-RC	Kobiconn
TP5, TP6	Red			Testpoint	151-207-RC	Kobiconn
TP7, TP8, TP9,TP10, TP13, TP14, TP16, TP17	Black			Testpoint	151-203-RC	Kobiconn
U1	Si858x	5000 VRMS		SO16	Si85858D-IS	Skyworks Solutions, Inc.

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