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ROHM Co., Ltd.
April 1, 2024

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ROHM GROUP
LAPIS TECHNOLOGY

FEBL22Q254RB-01

RB-S22Q254TD20
User's Manual

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Issue Date: March 30, 2021

ROHM SEMICONDUCTOR

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1. Overview

This instruction manual is for the RB-S22Q254TD20 which is the reference board for ML22Q254 (hereinafter referred to as "Speech Synthesis LSIs").

This board can be combined with Sound Device Control Board 3 (hereinafter referred to as "SDCB3") to do the following:

- Voice playback by ML22Q254.
- Writing sound code data into ML22Q254.

2. Operational notes

The following describes the precautions to follow when handling the RB-S22Q254TD20.

- Turn off the power when attaching the RB-S22Q254TD20 to the SDCB3.
- Turn off the power when loading Speech Synthesis LSIs into the RB-S22Q254TD20. Pin 1 is the position of the board silk ▲ at the bottom left with respect to the socket opening. The Figure 1 shows the setting directions of Speech Synthesis LSIs.
- The ML22Q254 supply voltages 2.0 to 5.5V. Use the RB-S22Q254TD20 with a power supply voltage of 3.0 to 5.5V. When connecting to SDCB3, the power supply voltage of RB-S22Q254TD20 is 3.0V.
- Connect jack to the mono speaker.

- RB-S22Q254TD20 is a device used only by experts in R&D facilities for research and development purposes. RB-S22Q254TD20 is not intended to be used in mass-produced products or parts thereof.
- The information in this document is subject to change without notice due to product improvement and technological improvement. Prior to use, please ensure that the information is up to date.
- LAPIS Technology does not provide any RB-S22Q254TD20 support. Replace only in case of initial failure.

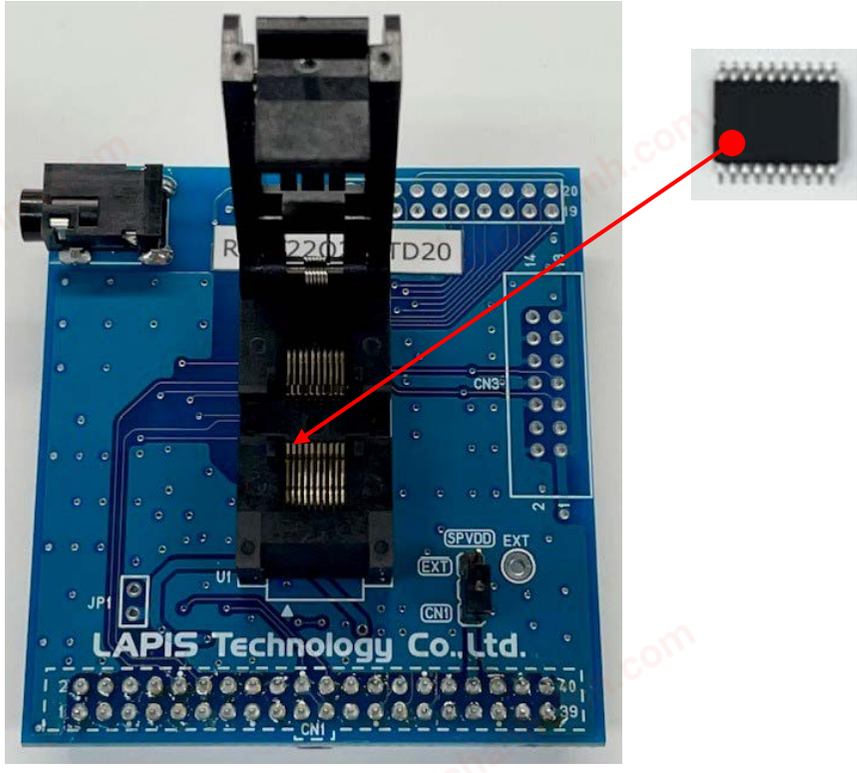


Figure 1 Outline Diagram

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3. Specification

3.1. SPVDD jumper pin, EXT through hall

SPVDD jumper pin is jumper pin that switch the connection of SPVDD pin of Speech Synthesis LSIs.

SPVDD	Contents
CN1	SPVDD pin is connected to 34pin of CN1.
EXT	SPVDD pin is connected to the EXT through hall.

When supplying from SDCB3, set SPVDD jumper pin to CN1.
To supply from an external source, set SPVDD jumper pin to EXT and input SPVDD from the EXT through hole.

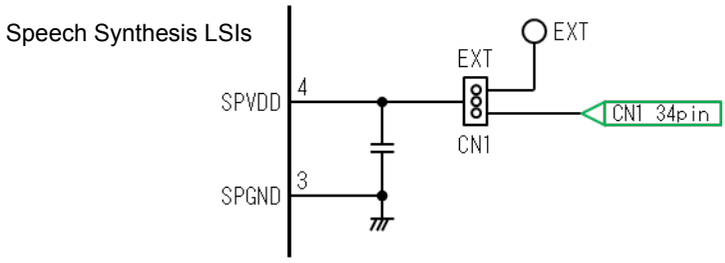


Figure 2 SPVDD jumper pin, EXT through hall

3.2. Jack

Jack is a jack where the signal from SPP,SPM pins of Speech Synthesis LSIs is output.
Connect a monaural speaker.

3.3. JP1 jumper terminal

JP1 jumper terminal is a jumper terminal that enables or disables the signal input from CN1 (SDCB3) to the input pin (TEST1_N, TEST0) of Speech Synthesis LSIs.

JP1 terminal Through hall	Contents
Not connect	Enables: Signals are input from CN1 to the input pins of Speech Synthesis LSIs.
Connect	Disables: No signals are input from CN1 to the input pins of Speech Synthesis LSIs.

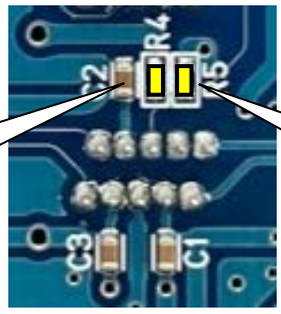
When connecting to a SDCB3 for use, not connect the through holes of the JP1 jumper terminal.
When using this board alone, connect the through holes of the JP1 jumper terminal.
When this board is shipped, there is no connection between the through holes of the JP1 jumper terminal.

3.4. R4,R5 land

R4is a pull up resistor mounting land for BUSYB pin of Speech synthesizer LSIs.
R5 is a pull down resistor mounting land for BUSYB pin of Speech synthesizer LSIs.
R4,R5 are not mounted at the time of shipment from this board.

BUSYB pin of Speech Synthesis LSIs select the pin status from CMOS output, Nch open drain output, Pch open drain output, and Hi-Z output according to Code Option setting. (Refer to Speech LSI Utility User's Manual.)
When using BUSYB pin with Nch open drain output, mount resistor (10kΩ or less, size:1608) to R4 on the back of the board.
When using BUSYB pin with Pch open drain output, mount resistor (1kΩ or less, size:1608) to R5 on the back of the board.

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R4
Mounted resistor when using with Nch open drain output.

R5
Mounted resistor when using with Pch open drain output.

Figure 3 R4,R5 land

3.5. CN1 connector

CN1 connector is used to connect to SDCB3.

3.6. CN2 connector

CN2 connector is used to connect to the pins of Speech Synthesis LSIs.

CN2 Pin No	LSI		I/O	
	Pin No	Pin Name	SDCB3 connection	Single unit *2
1	1	SPP	O	O
2	2	SPM	O	O
3	3	SPGND	O	I
4	4	SPVDD *1	O	I
5	5	BUSYB	O	O
6	6	DGND	O	I
7	7	VDDL	O	O
8	8	DVDD *1	O	I
9	9	NC	-	-
10	10	NC	-	-
11	11	NC	-	-
12	12	NC	-	-
13	13	CSB	O	I
14	14	SDA	O	I
15	15	SCL	O	I
16	16	TEST1_N	O	I
17	17	TEST0	O	I
18	18	NC	-	-
19	19	NC	-	-
20	20	RESET_N	O	I

*1 Do not supply DVDD,SPVDD from CN2 when connecting SDCB3.
*2 When using a single unit, connect the terminals of JP1 jumper terminal. (Refer to 3.3 JP1 jumper terminal.)

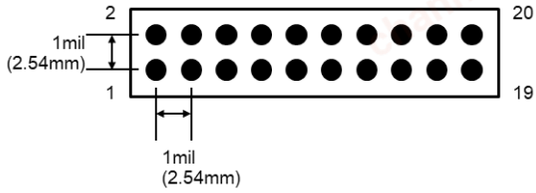


Figure 4 CN2 connectors hole pattern

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4. Appendix

4.1. PCB layout

Figure 5 shows the RB-S22Q254TD20 PCB layout.

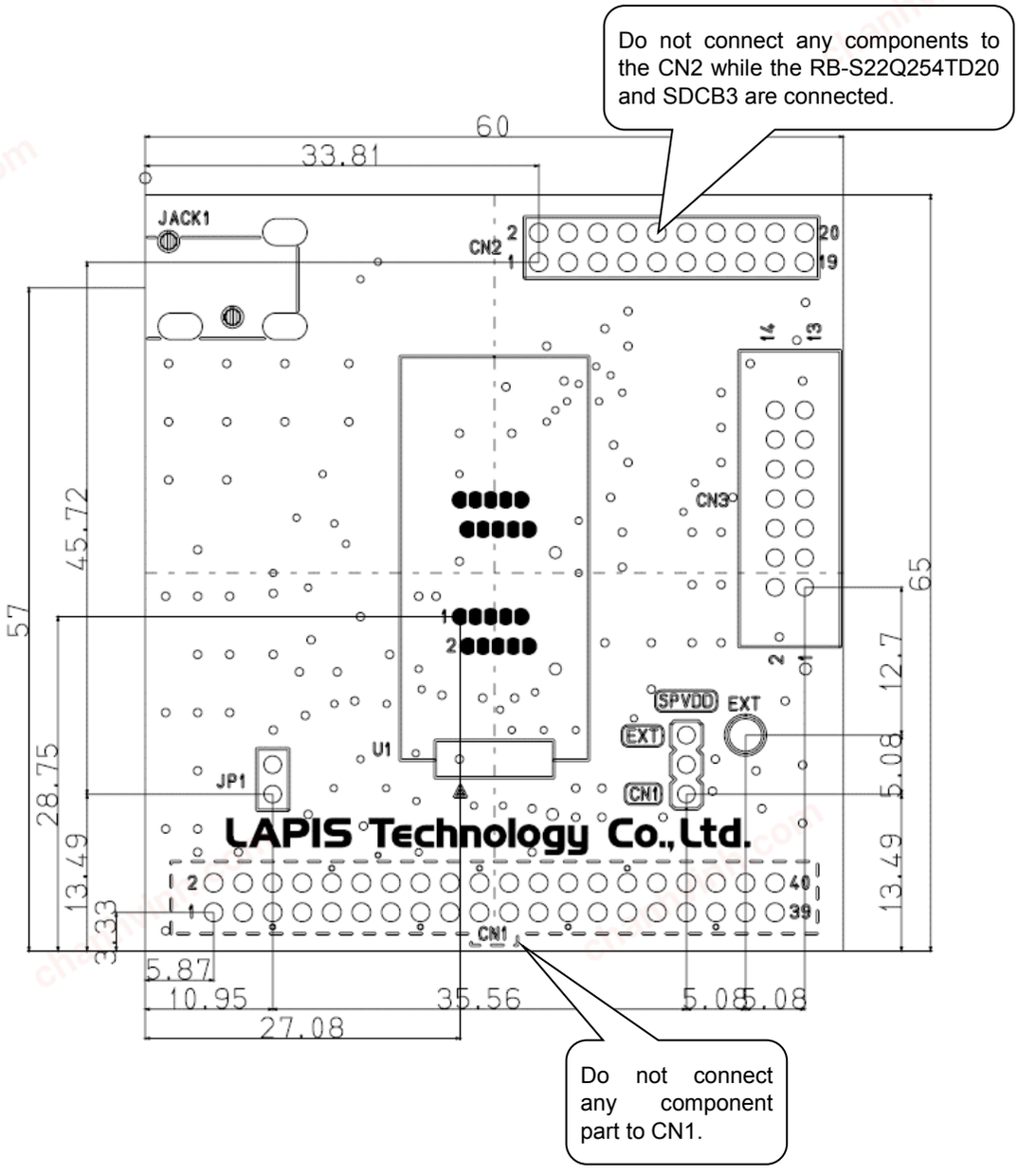


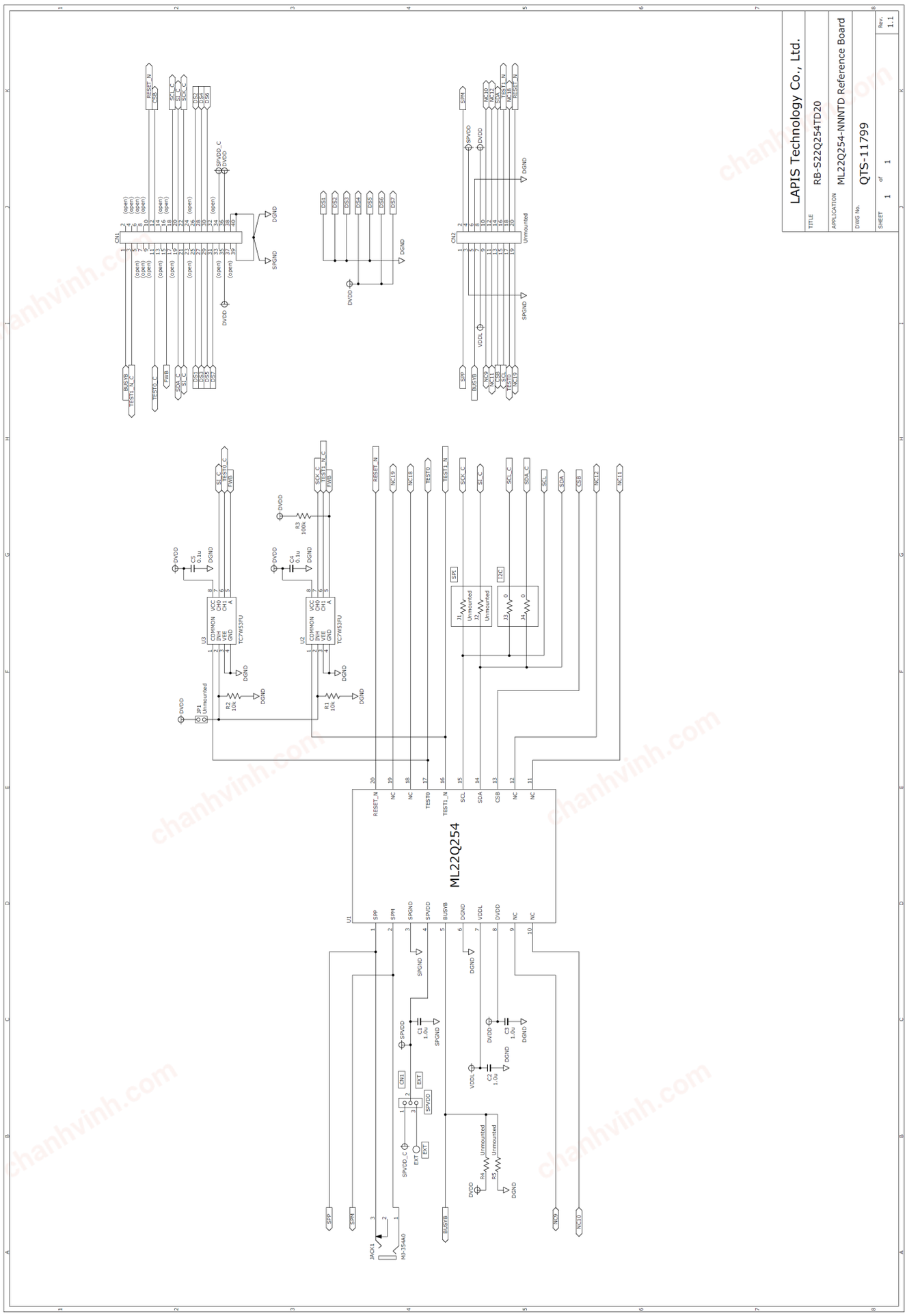
Figure 5 PCB layout

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4.2. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11925	RB-S22Q254TD20	PCB	1	LAPIS Technology Co., Ltd.
2	CGA3E1X7R1C105K080AC	C1,C2,C3	Ceramic Capacitor 1.0μF/16V X7R	3	TDK Corporation
3	CGA3E2X7R1E104K080AA	C4,C5	Ceramic Capacitor 0.1μF/25V X7R	2	TDK Corporation
4	HIF3FB-40DA-2.54DSA(71)	CN1	40pin Receptacle	1	Hirose Electric Co., Ltd.
5	-	CN2	Unmounted	1	-
6	-	CN3	Unmounted	1	-
7	-	EXT	Unmounted	1	-
8	MCR01MZPJ000	J3,J4	Resistor 0Ω	2	ROHM Co., Ltd.
9	-	J1,J2	Unmounted	2	-
10	MJ-354A0	JACK1	2-Conductor Miniature Jack	1	MARUSHIN ELECTRIC MFG. Co., Ltd.
11	-	JP1	Unmounted	1	-
12	MCR03EZPJ103	R1,R2	Resistor 10kΩ ±5%	2	ROHM Co., Ltd.
13	MCR03EZPJ104	R3	Resistor 100kΩ ±5%	1	ROHM Co., Ltd.
14	-	R4,R5	Unmounted	2	-
15	A2-3PA-2.54DSA(71)	SPVDD	3pin Pin Header	1	Hirose Electric Co., Ltd.
16	IC51-0202-779	U1	TSSOP20 Socket	1	YAMAICHI ELECTRONICS Co., Ltd.
17	TC7W53FU	U2,U3	2-Channel Multiplexer/Demultiplexer	2	Toshiba Corporation
18	HIF3GA-2.54SP	-	Short Pin	1	Hirose Electric Co., Ltd.

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5. Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL22Q254RB-01	March 30, 2021	–	–	First edition.

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