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QH8MA3

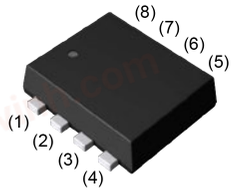
30V Nch+Pch Middle Power MOSFET

Datasheet

Symbol	Tr1:Nch	Tr2:Pch
V_{DSS}	30V	-30V
$R_{DS(on)}$(Max.)	29mΩ	48mΩ
I_D	±7.0A	±5.5A
P_D	2.5W	

●Outline

TSMT8

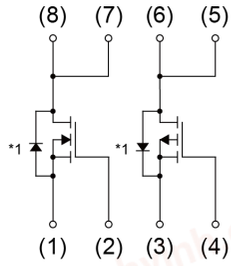


●Features

1) Low on - resistance.
2) Small Surface Mount Package (TSMT8).
3) Pb-free lead plating ; RoHS compliant.
4) Halogen Free.

●Inner circuit

(1) Tr1 (Nch) Source
(2) Tr1 (Nch) Gate
(3) Tr2 (Pch) Source
(4) Tr2 (Pch) Gate
(5) Tr2 (Pch) Drain
(6) Tr2 (Pch) Drain
(7) Tr1 (Nch) Drain
(8) Tr1 (Nch) Drain
*1 Body Diode



●Application

Switching

●Packaging specifications

Type	Packing	Embossed Tape
	Reel size (mm)	180
	Tape width (mm)	8
	Basic ordering unit (pcs)	3000
	Taping code	TR
	Marking	MA3

●Absolute maximum ratings (T_a = 25°C) ,unless otherwise specified.

Parameter		Symbol	Value		Unit
			Tr1:Nch	Tr2:Pch	
Drain - Source voltage		V_{DSS}	30	-30	V
Continuous drain current		I_D *1	±7.0	±5.5	A
Pulsed drain current		$I_{D,\ pulse}$ *2	±18	±18	A
Gate - Source voltage		V_{GSS}	±20	±20	V
Avalanche energy, single pulse		E_{AS} *4	1.8	1.1	mJ
Avalanche current		I_{AS} *4	5.0	-4.0	A
Power dissipation	total	P_D *1	2.5		W
	total	P_D *3	1.5		
	element	P_D *3	1.25		
Junction temperature		T_j	150		℃
Range of storage temperature		T_{stg}	-55 to +150		℃

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●Thermal resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction - ambient	R_{thJA} *3	-	83.3	-	

●Electrical characteristics (T_a = 25°C) , unless otherwise specified

Parameter	Symbol	Type	Conditions	Values			Unit
				Min.	Typ.	Max.	
Drain - Source breakdown voltage	$V_{(BR)DSS}$	Tr1	V_{GS} = 0V, I_D = 1mA	30	-	-	V
		Tr2	V_{GS} = 0V, I_D = -1mA	-30	-	-	
Breakdown voltage temperature coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_j}$	Tr1	I_D = 1mA, referenced to 25°C	-	21	-	mV/°C
		Tr2	I_D = -1mA, referenced to 25°C	-	-22	-	
Zero gate voltage drain current	I_{DSS}	Tr1	V_{DS} = 30V, V_{GS} = 0V	-	-	1	μA
		Tr2	V_{DS} = -30V, V_{GS} = 0V	-	-	-1	
Gate - Source leakage current	I_{GSS}	Tr1	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
		Tr2	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	
Gate threshold voltage	$V_{GS(th)}$	Tr1	V_{DS} = V_{GS}, I_D = 1mA	1.0	-	2.5	V
		Tr2	V_{DS} = V_{GS}, I_D = -1mA	-1.0	-	-2.5	
Gate threshold voltage temperature coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	Tr1	I_D = 1mA, referenced to 25°C	-	-3	-	mV/°C
		Tr2	I_D = -1mA, referenced to 25°C	-	2.9	-	
Static drain - source on - state resistance	$R_{DS(on)}$ *5	Tr1	V_{GS} = 10V, I_D = 7.0A	-	22	29	mΩ
			V_{GS} = 4.5V, I_D = 5.0A	-	35	46	
		Tr2	V_{GS} = -10V, I_D = -5.5A	-	37	48	
			V_{GS} = -4.5V, I_D = -4.0A	-	55	72	
Transconductance	g_{fs} *5	Tr1	V_{DS} = 5V, I_D = 5A	2.7	-	-	S
		Tr2	V_{DS} = -5V, I_D = -4A	3.3	-	-	

*1 Pw ≦ 1s, Limited only by maximum temperature allowed.

*2 Pw ≦ 10μs, Duty cycle ≦ 1%

*3 MOUNTED ON A CERAMIC BOARD

*4 Tr1: L ≃ 100μH, V_{DD} = 15V, R_G = 25Ω, STARTING T_{ch} = 25°C Fig.3-1,3-2

Tr2: L ≃ 100μH, V_{DD} = -15V, R_G = 25Ω, STARTING T_{ch} = 25°C Fig.6-1,6-2

*5 Pulsed

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●Electrical characteristics (T_a = 25°C)

<Tr1>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	V_{GS} = 0V	-	300	-	pF
Output capacitance	C_{oss}	V_{DS} = 15V	-	50	-	
Reverse transfer capacitance	C_{rss}	f = 1MHz	-	40	-	
Turn - on delay time	$t_{d(on)}$ *5	V_{DD} ≃ 15V, V_{GS} = 10V	-	7.2	-	ns
Rise time	t_r *5	I_D = 3.5A	-	8.0	-	
Turn - off delay time	$t_{d(off)}$ *5	R_L = 4.3Ω	-	12	-	
Fall time	t_f *5	R_G = 10Ω	-	5.7	-	

<Tr2>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	V_{GS} = 0V	-	480	-	pF
Output capacitance	C_{oss}	V_{DS} = -15V	-	85	-	
Reverse transfer capacitance	C_{rss}	f = 1MHz	-	65	-	
Turn - on delay time	$t_{d(on)}$ *5	V_{DD} ≃ -15V, V_{GS} = -10V	-	8.0	-	ns
Rise time	t_r *5	I_D = -2.25A	-	12	-	
Turn - off delay time	$t_{d(off)}$ *5	R_L = 6.7Ω	-	40	-	
Fall time	t_f *5	R_G = 10Ω	-	20	-	

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●Gate charge characteristics (T_a = 25°C)

<Tr1>

Parameter	Symbol	Conditions		Values			Unit
				Min.	Typ.	Max.	
Total gate charge	Q_g *5	V_{DD} ≃ 15V I_D = 7A	V_{GS} = 10V	-	7.2	-	nC
			V_{GS} = 4.5V	-	3.7	-	
Gate - Source charge	Q_{gs} *5			-	1.4	-	
Gate - Drain charge	Q_{gd} *5			-	1.3	-	

<Tr2>

Parameter	Symbol	Conditions		Values			Unit
				Min.	Typ.	Max.	
Total gate charge	Q_g *5	V_{DD} ≃ -15V I_D = -5.5A	V_{GS} = -10V	-	10	-	nC
			V_{GS} = -4.5V	-	5.2	-	
Gate - Source charge	Q_{gs} *5			-	1.6	-	
Gate - Drain charge	Q_{gd} *5			-	1.9	-	

●Body diode electrical characteristics (Source-Drain) (T_a = 25°C)

<Tr1>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Body diode continuous forward current	I_S	T_a = 25°C	-	-	1.0	A
Body diode pulse current	I_{SP} *2		-	-	18	
Forward voltage	V_{SD} *5	V_{GS} = 0V, I_S = 1A	-	-	1.2	V

<Tr2>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Body diode continuous forward current	I_S	T_a = 25°C	-	-	-1.0	A
Body diode pulse current	I_{SP} *2		-	-	-18	
Forward voltage	V_{SD} *5	V_{GS} = 0V, I_S = -1A	-	-	-1.2	V

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●Electrical characteristic curves <Tr1>

Fig.1 Power Dissipation Derating Curve

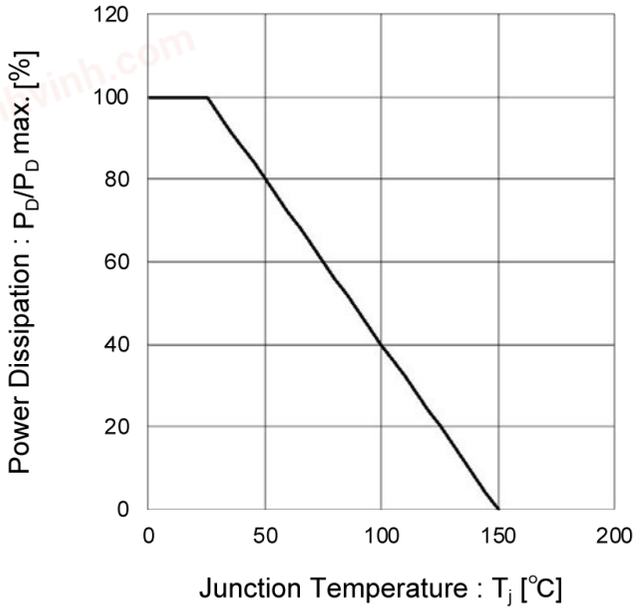


Fig.2 Maximum Safe Operating Area

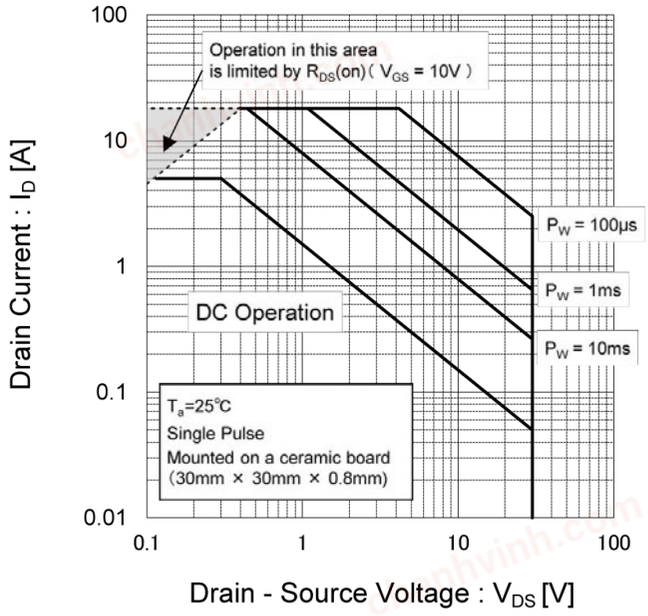


Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

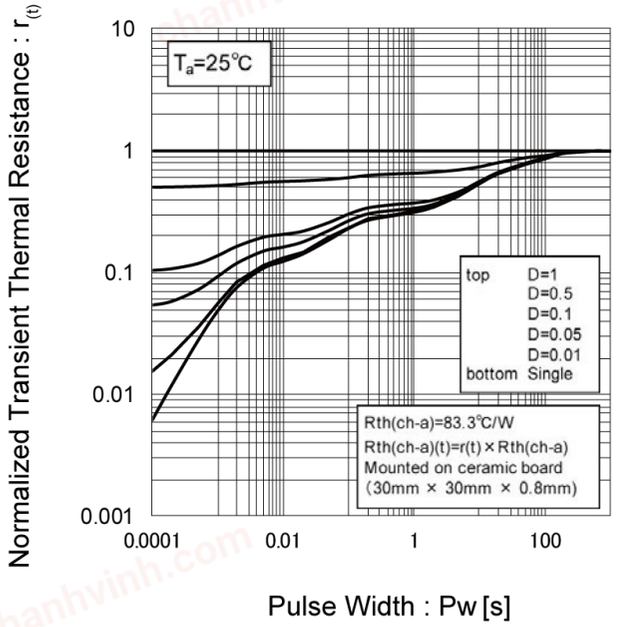
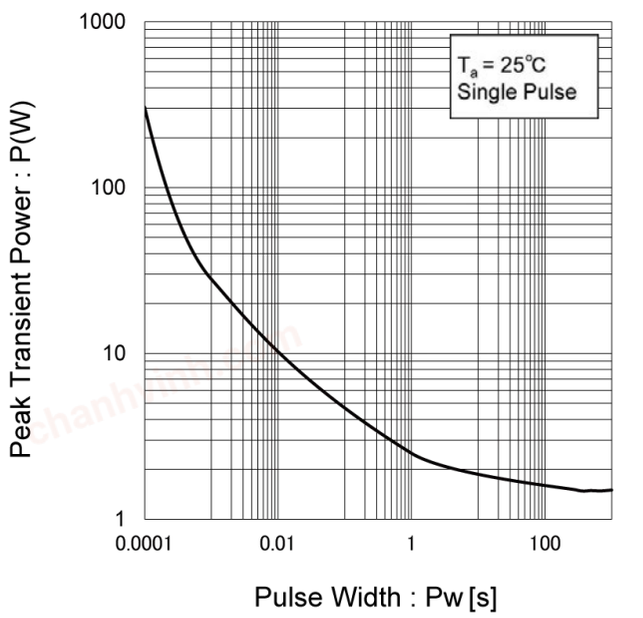


Fig.4 Single Pulse Maximum Power dissipation



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●Electrical characteristic curves <Tr1>

Fig.5 Typical Output Characteristics(I)

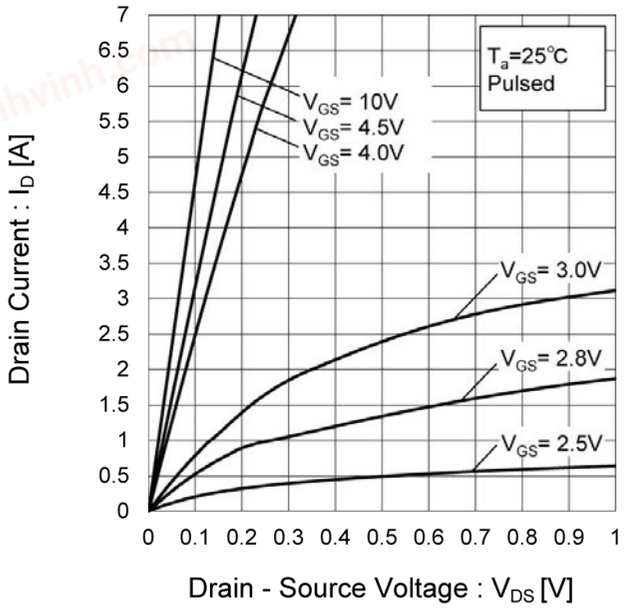


Fig.6 Typical Output Characteristics(II)

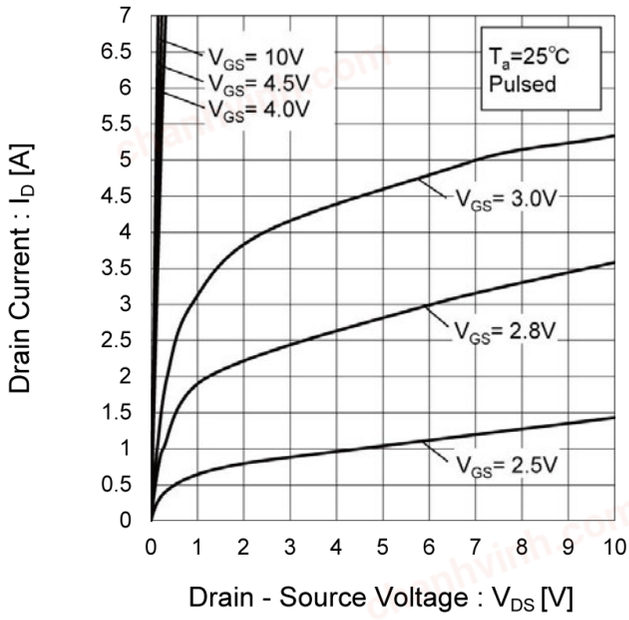
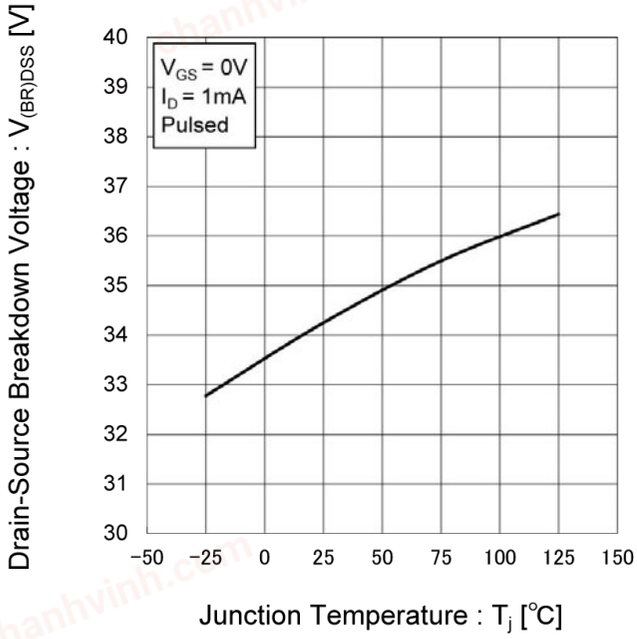


Fig.7 Breakdown Voltage vs. Junction Temperature



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●Electrical characteristic curves <Tr1>

Fig.8 Typical Transfer Characteristics

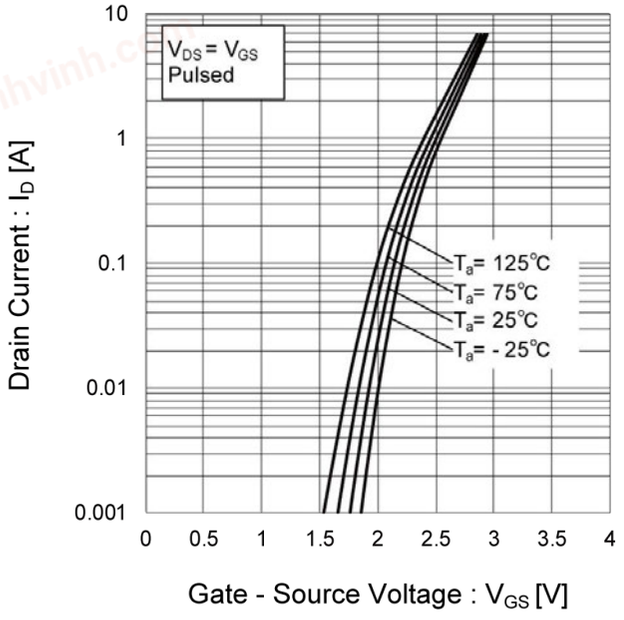


Fig.9 Gate Threshold Voltage vs. Junction Temperature

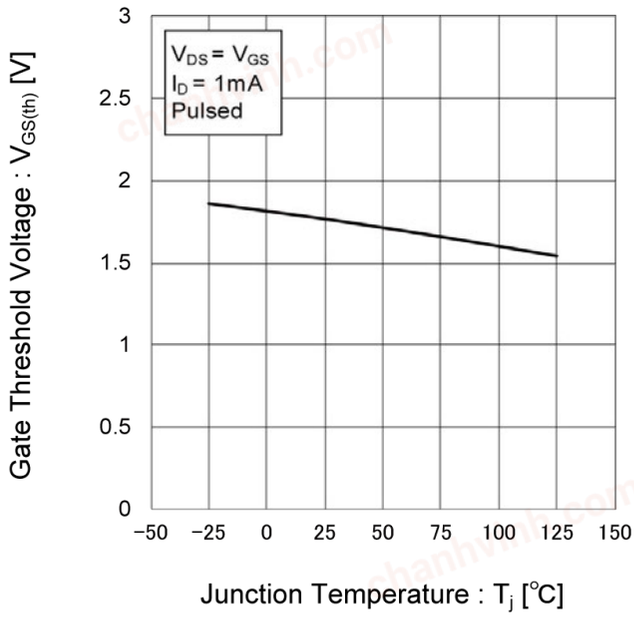
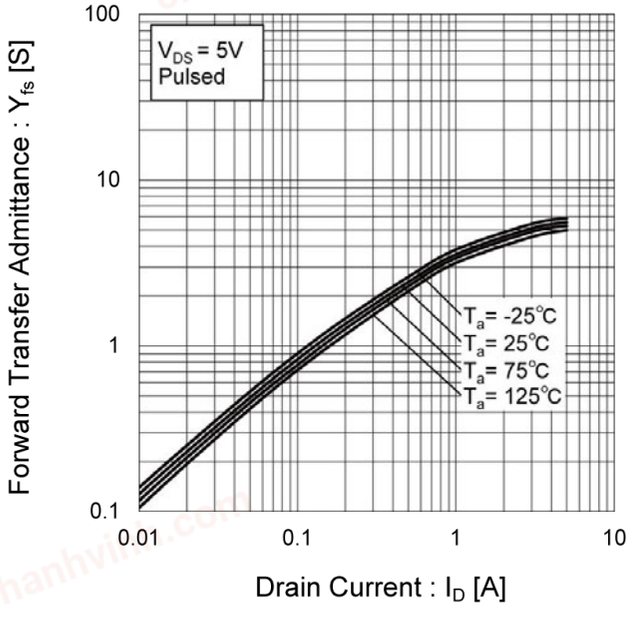


Fig.10 Tranceconductance vs. Drain Current



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●Electrical characteristic curves <Tr1>

Fig.11 Drain Current Derating Curve

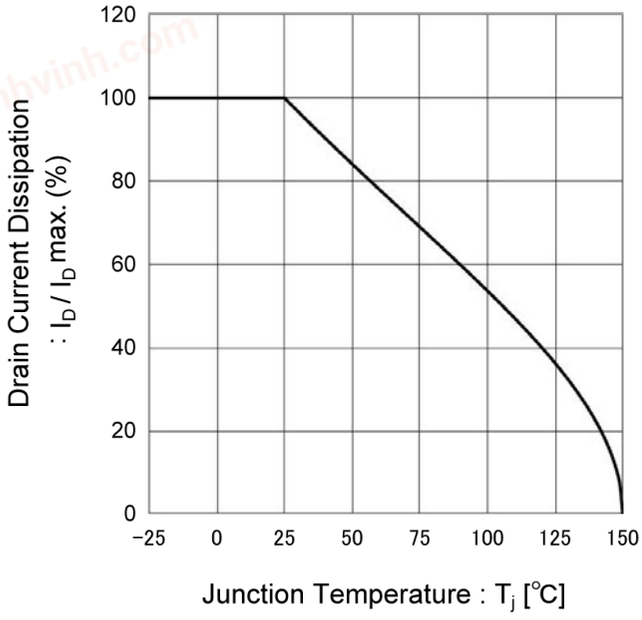


Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage

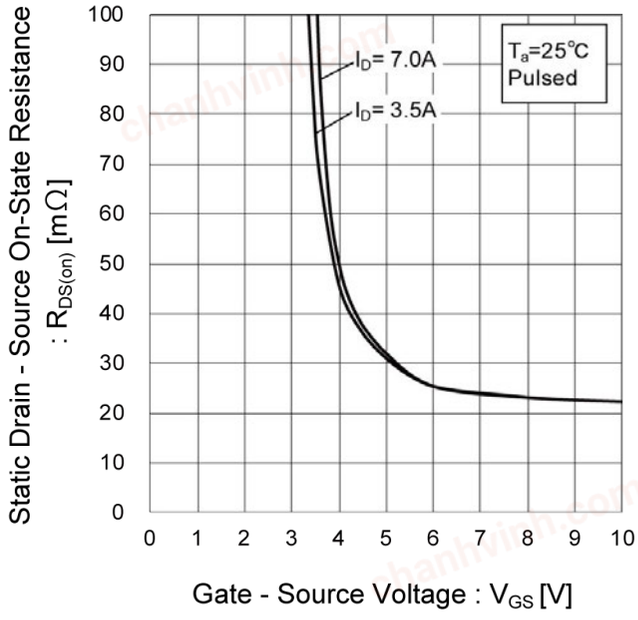
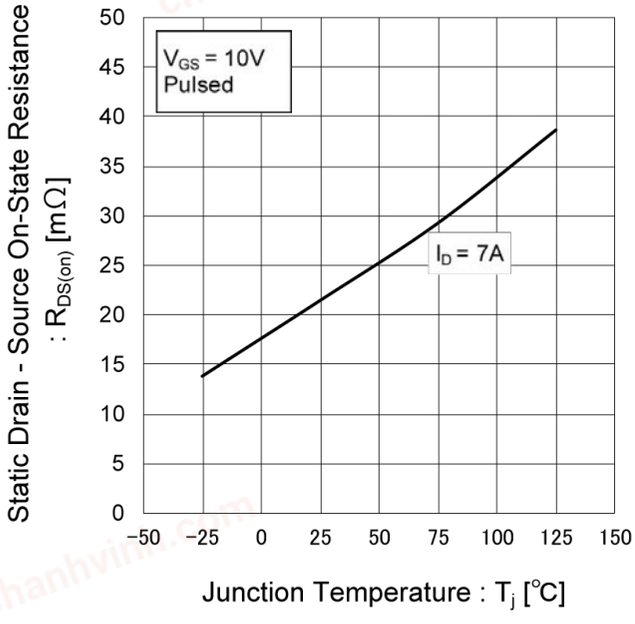


Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature



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●Electrical characteristic curves <Tr1>

Fig.14 Static Drain - Source On - State Resistance vs. Drain Current(I)

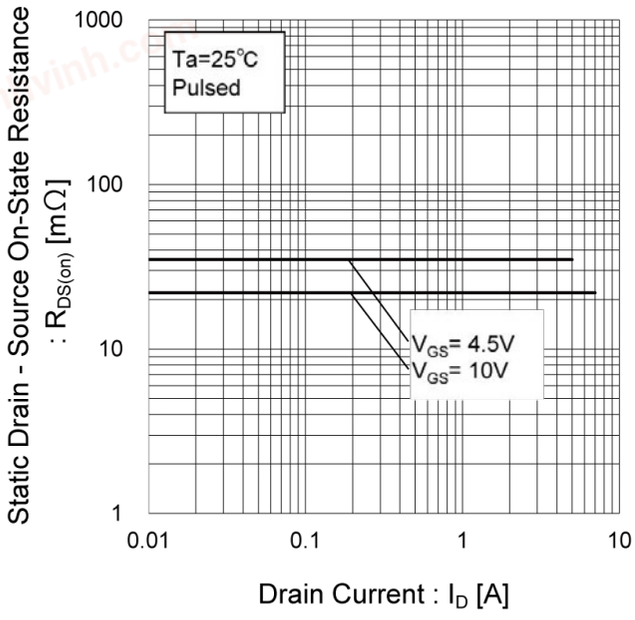


Fig.15 Static Drain - Source On - State Resistance vs. Drain Current(II)

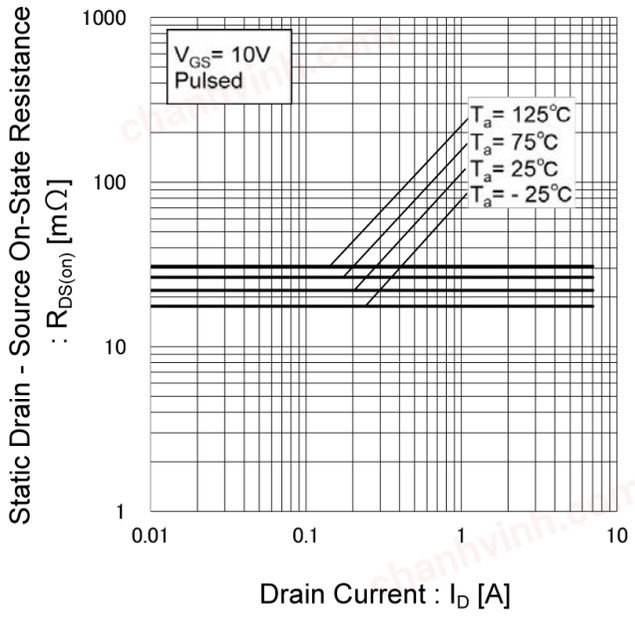
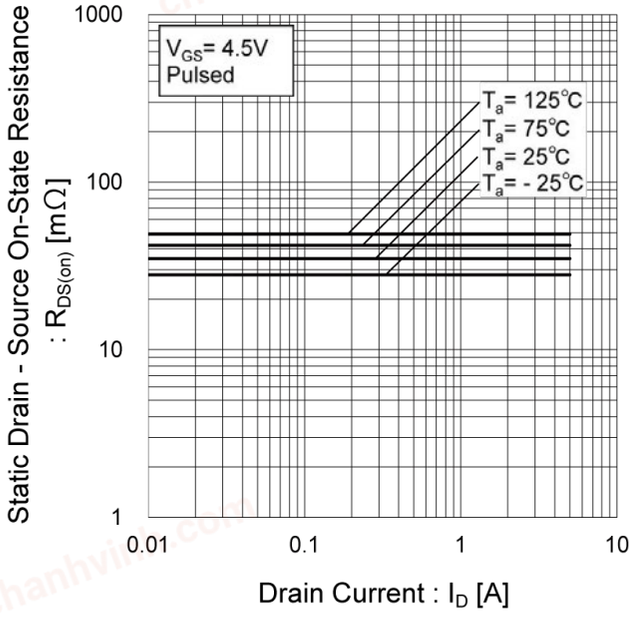


Fig.16 Static Drain - Source On - State Resistance vs. Drain Current(III)



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●Electrical characteristic curves <Tr1>

Fig.17 Typical Capacitance vs. Drain - Source Voltage

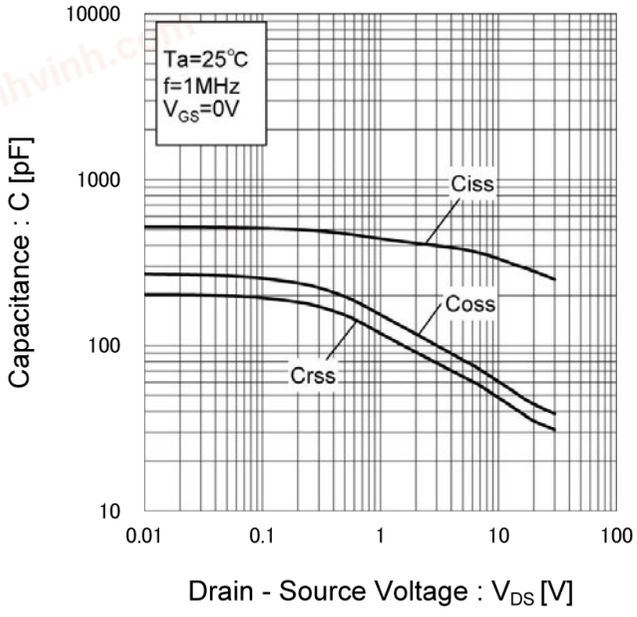


Fig.18 Switching Characteristics

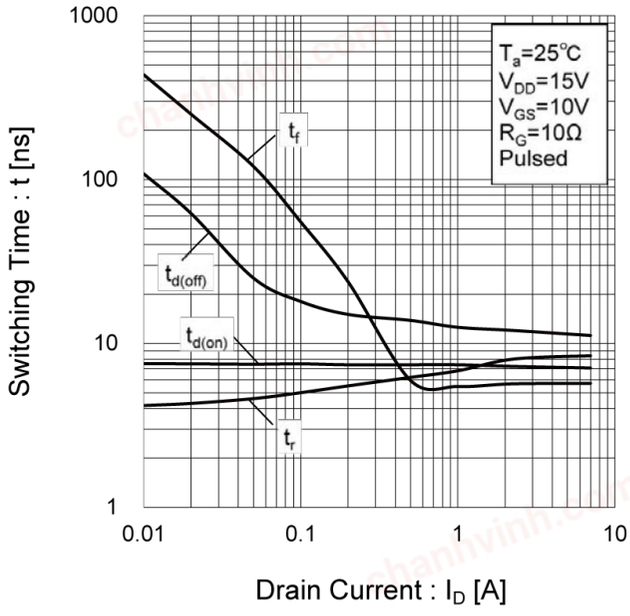


Fig.19 Dynamic Input Characteristics

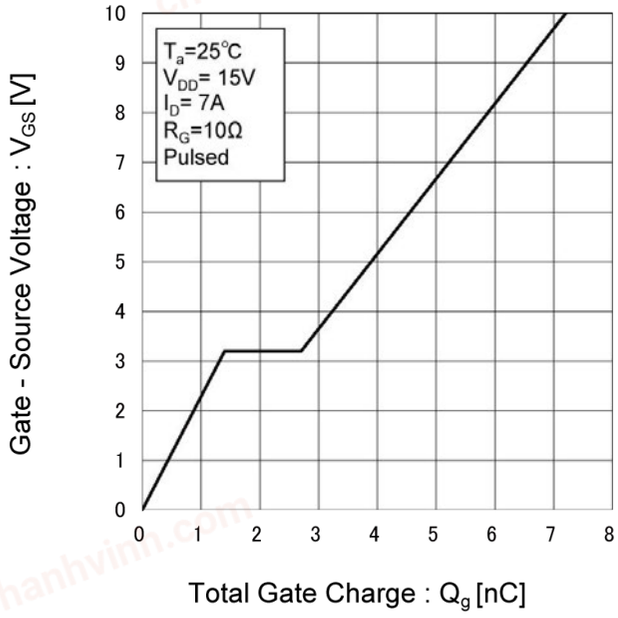
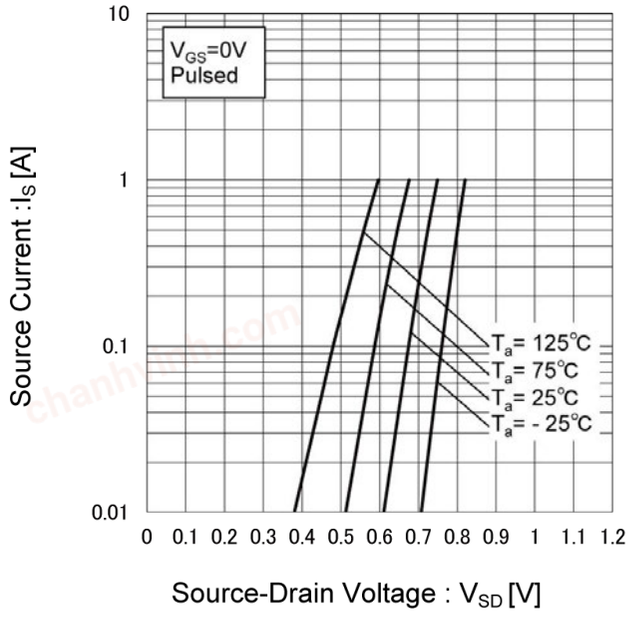


Fig.20 Source Current vs. Source Drain Voltage



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●Electrical characteristic curves <Tr2>

Fig.1 Power Dissipation Derating Curve

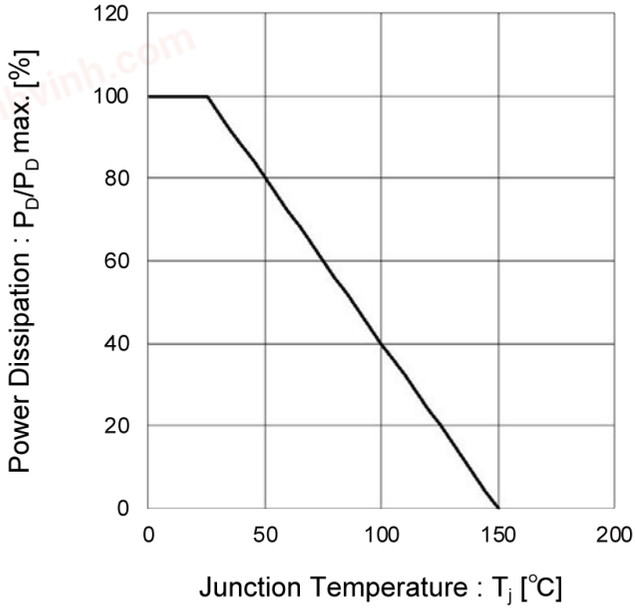


Fig.2 Maximum Safe Operating Area

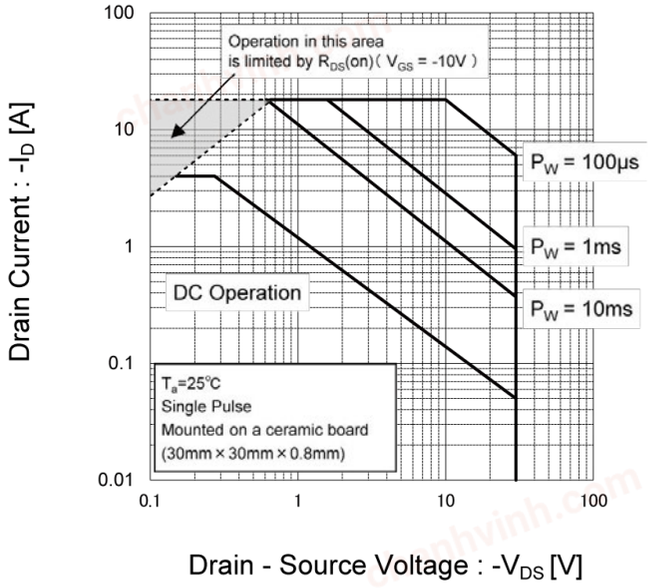


Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

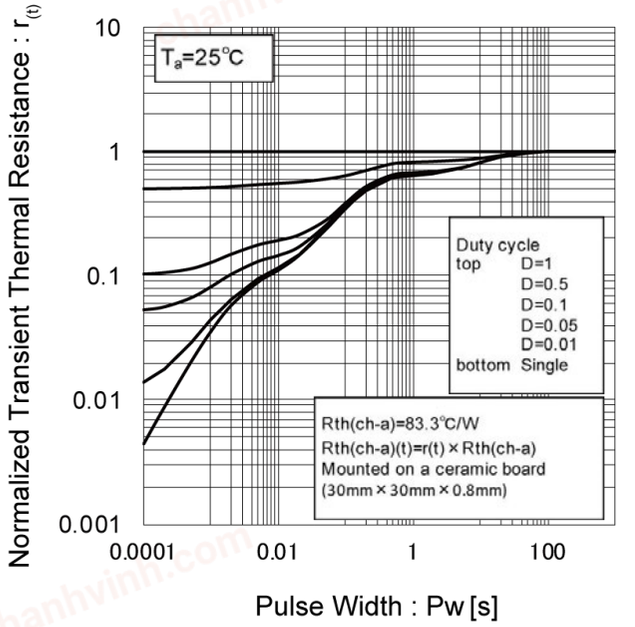
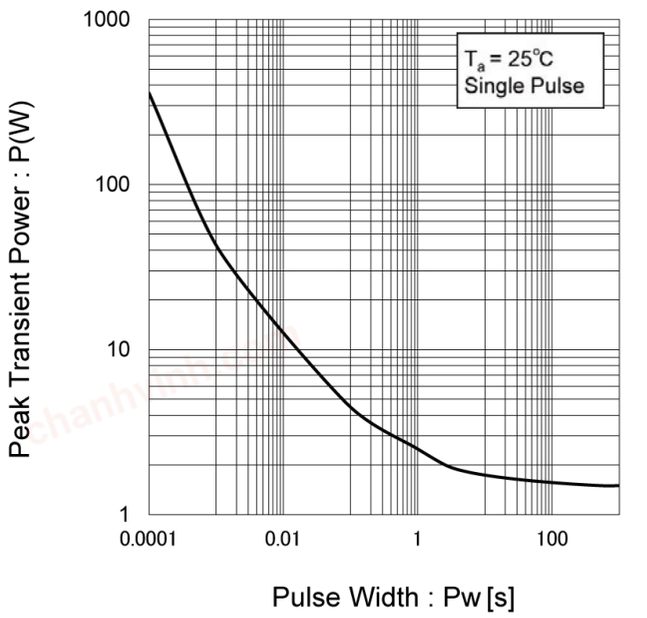


Fig.4 Single Pulse Maximum Power dissipation



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●Electrical characteristic curves <Tr2>

Fig.5 Typical Output Characteristics(I)

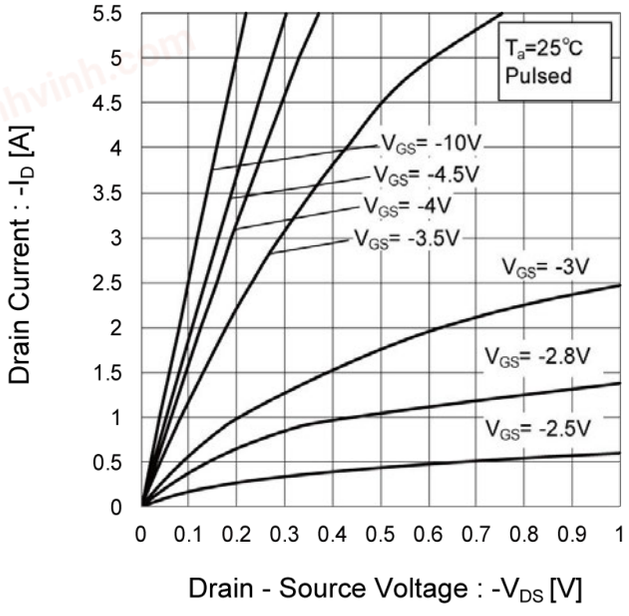


Fig.6 Typical Output Characteristics(II)

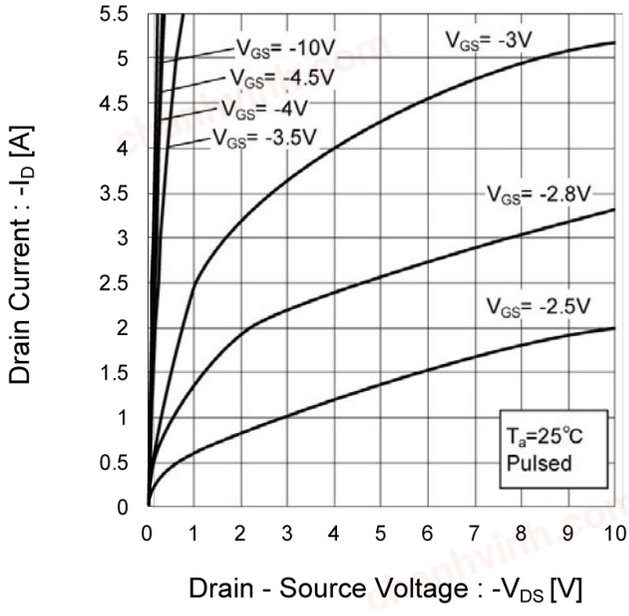
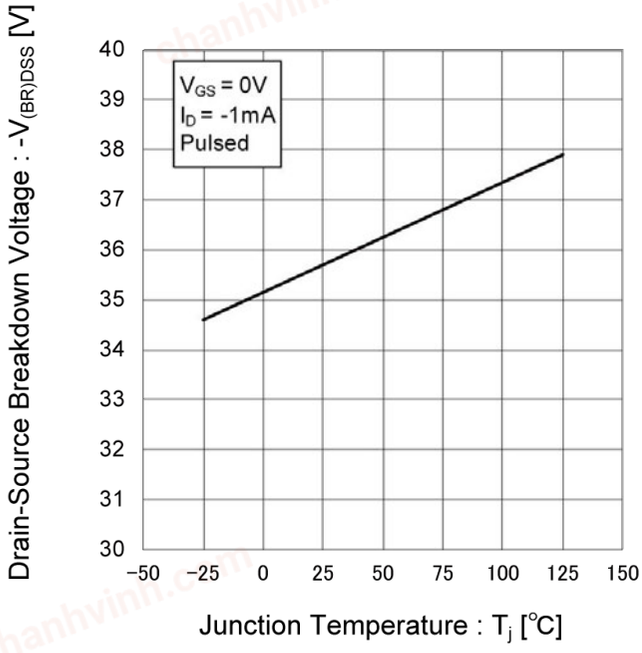


Fig.7 Breakdown Voltage vs. Junction Temperature



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●Electrical characteristic curves <Tr2>

Fig.8 Typical Transfer Characteristics

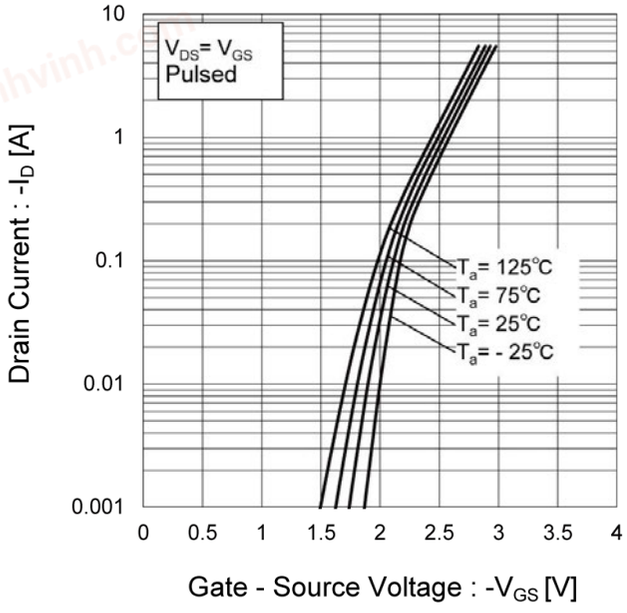


Fig.9 Gate Threshold Voltage vs. Junction Temperature

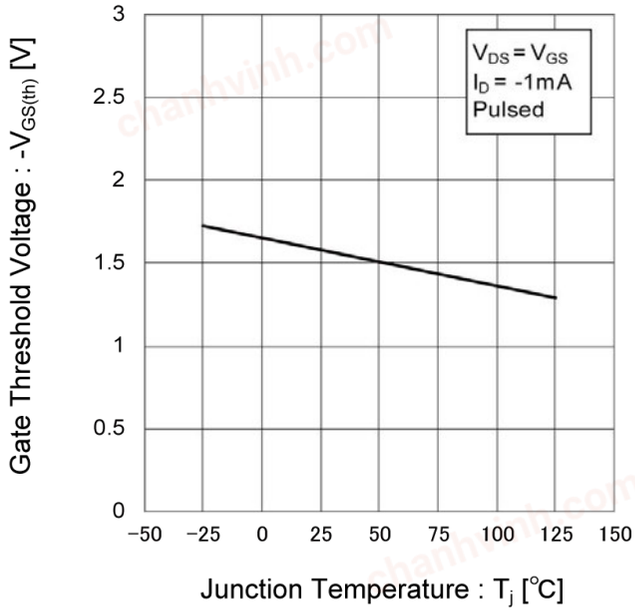
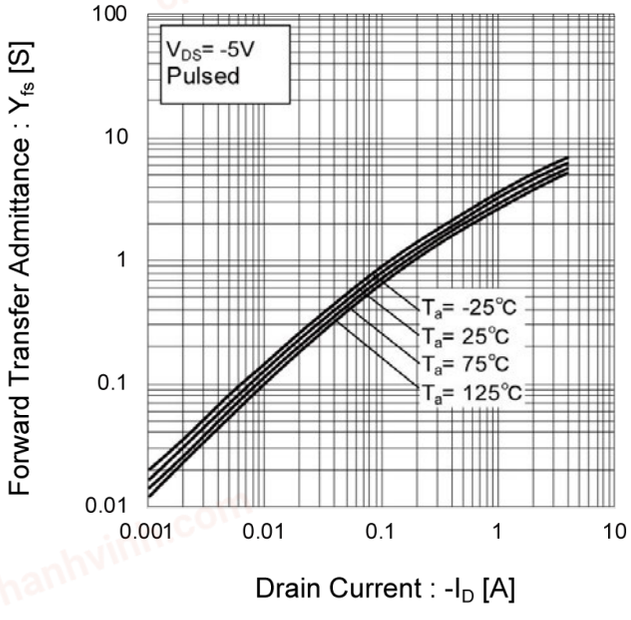


Fig.10 Tranceconductance vs. Drain Current



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●Electrical characteristic curves <Tr2>

Fig.11 Drain Current Derating Curve

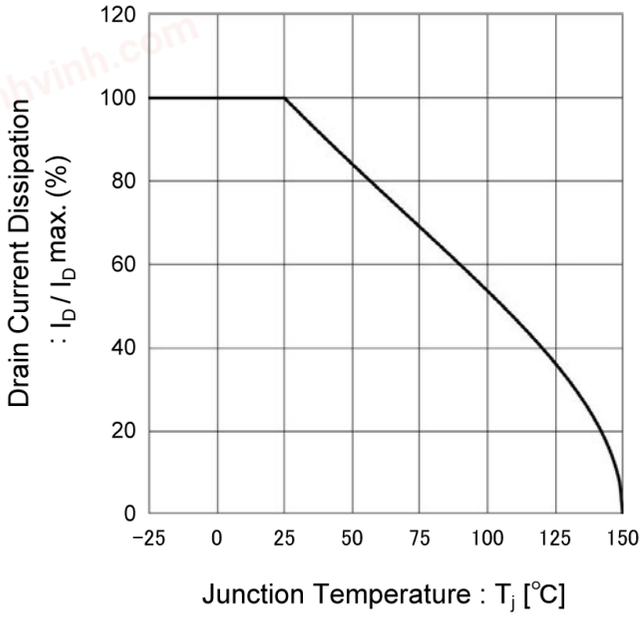


Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage

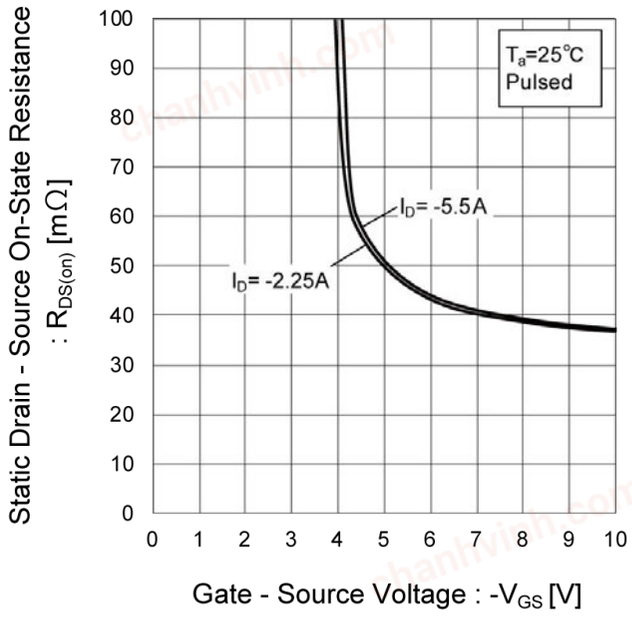
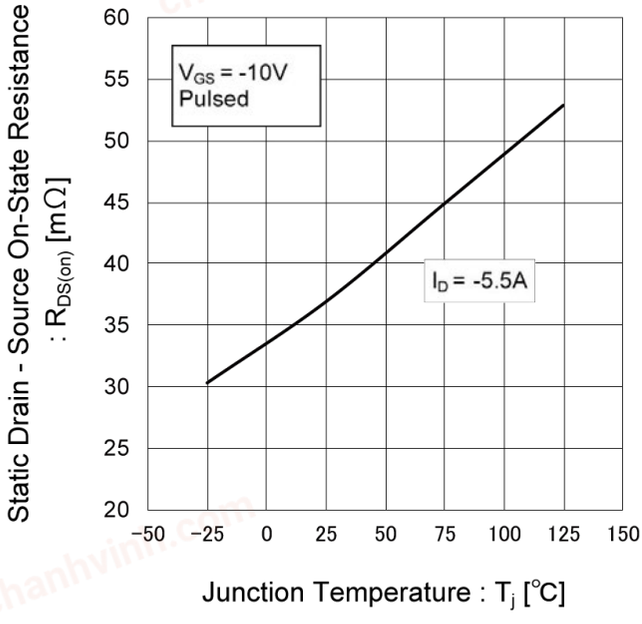


Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature



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●Electrical characteristic curves <Tr2>

Fig.14 Static Drain - Source On - State Resistance vs. Drain Current(I)

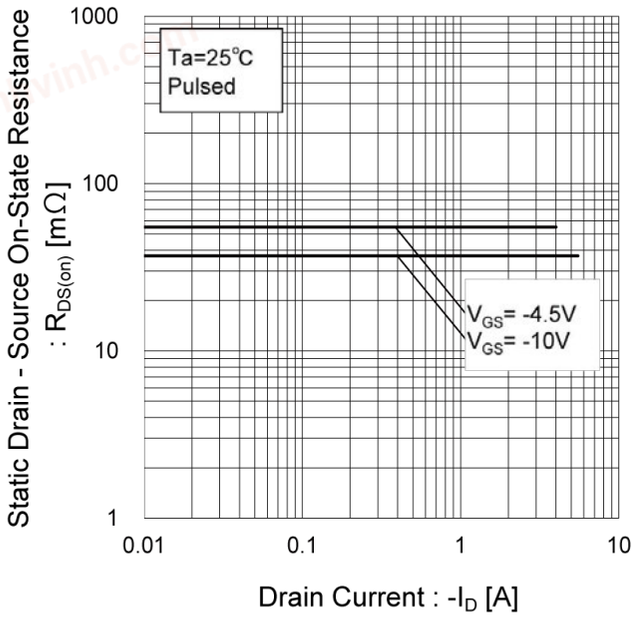


Fig.15 Static Drain - Source On - State Resistance vs. Drain Current(II)

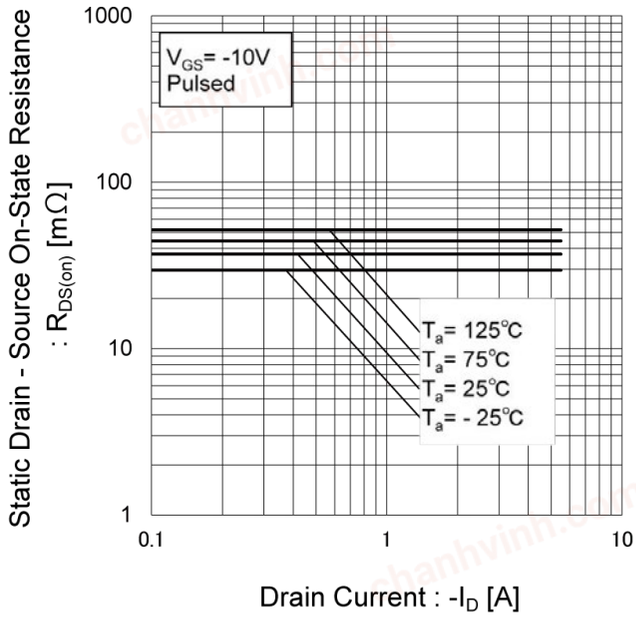
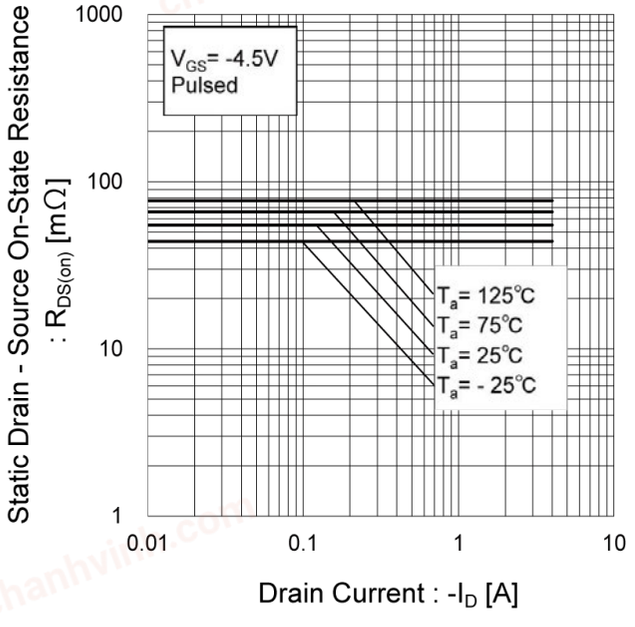


Fig.16 Static Drain - Source On - State Resistance vs. Drain Current(III)



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●Electrical characteristic curves <Tr2>

Fig.17 Typical Capacitance vs. Drain - Source Voltage

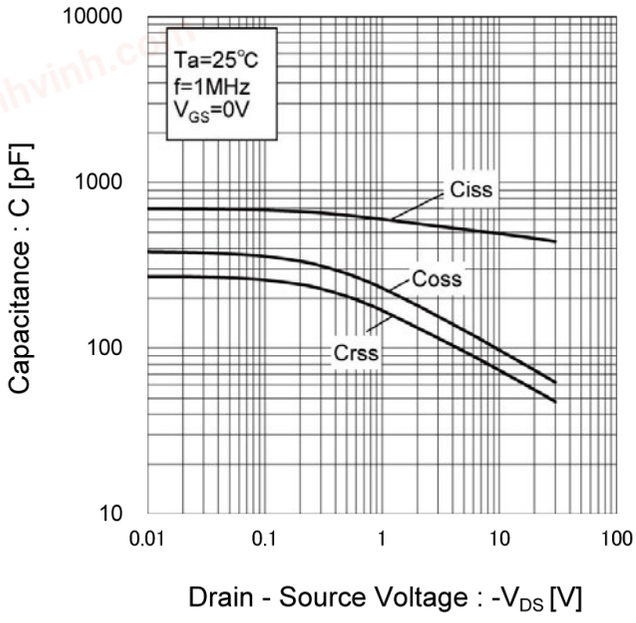


Fig.18 Switching Characteristics

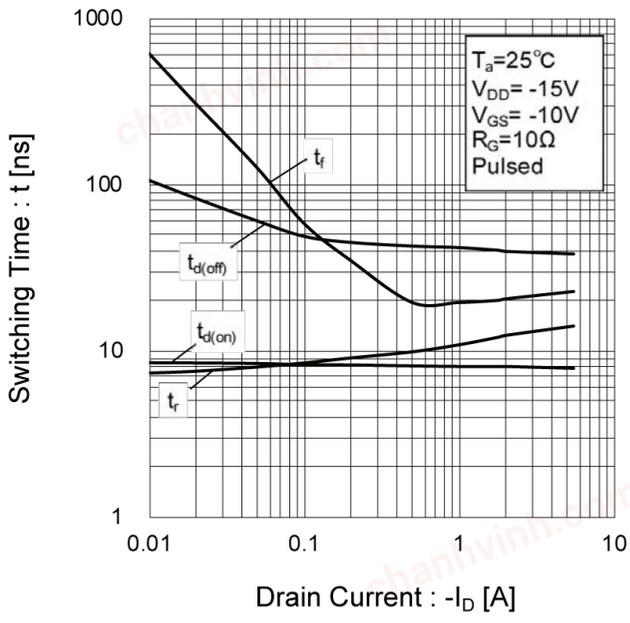


Fig.19 Dynamic Input Characteristics

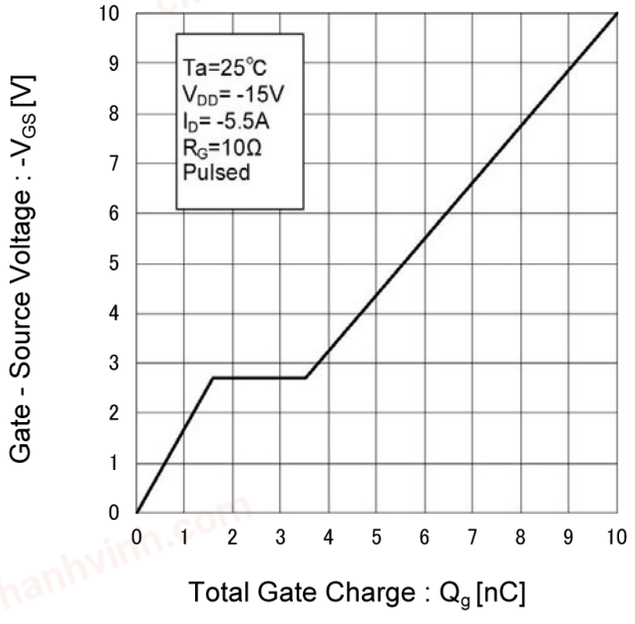
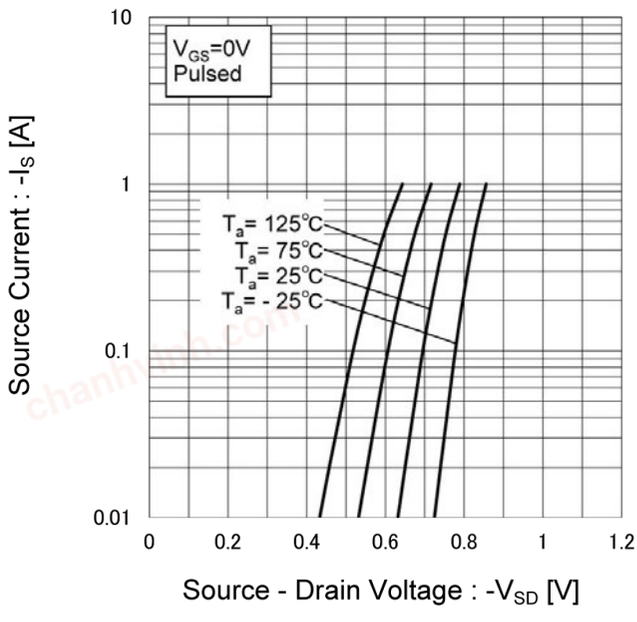


Fig.20 Source Current vs. Source Drain Voltage



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●Measurement circuits <Tr1>

Fig.1-1 Switching Time Measurement Circuit

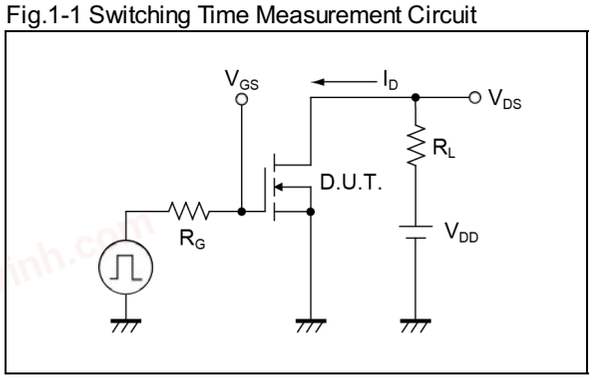


Fig.1-2 Switching Waveforms

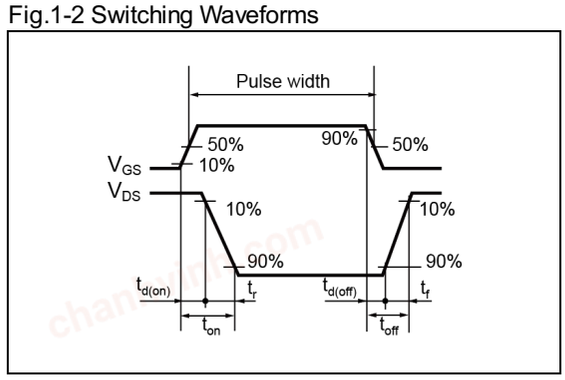


Fig.2-1 Gate Charge Measurement Circuit

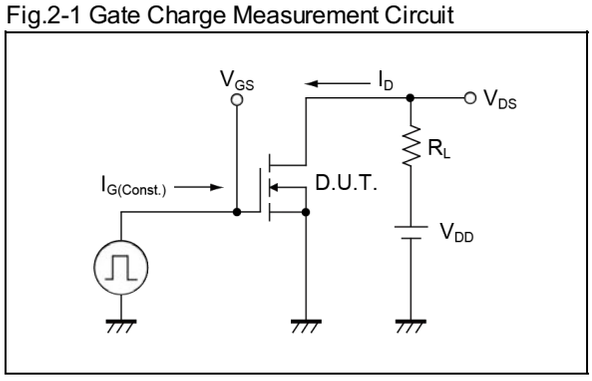


Fig.2-2 Gate Charge Waveform

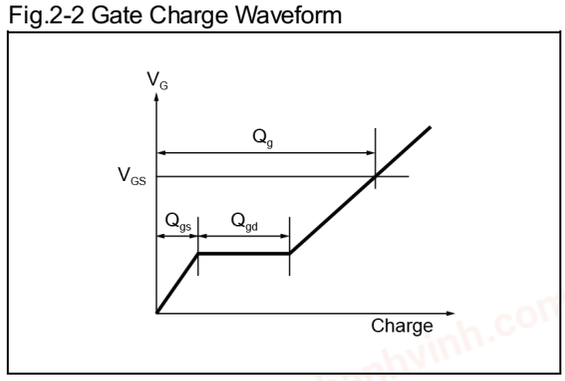


Fig.3-1 Avalanche Measurement Circuit

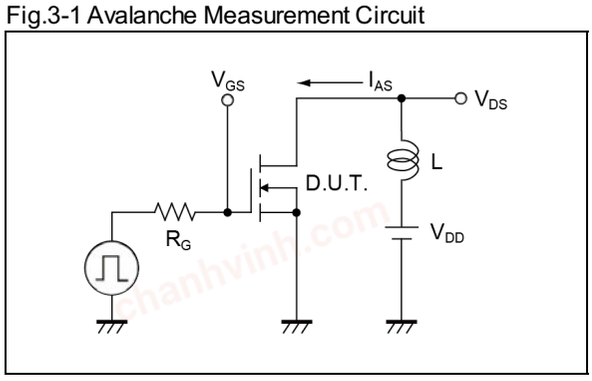
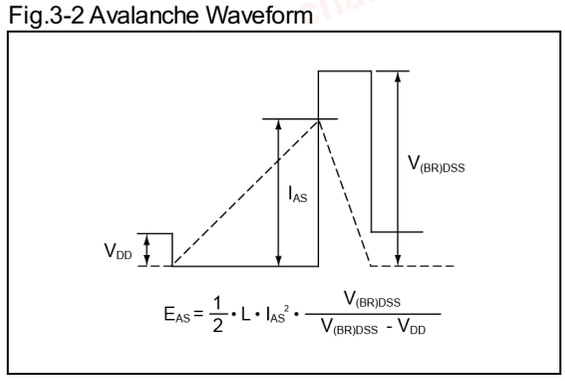


Fig.3-2 Avalanche Waveform



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●Measurement circuits <Tr2>

Fig.4-1 Switching Time Measurement Circuit

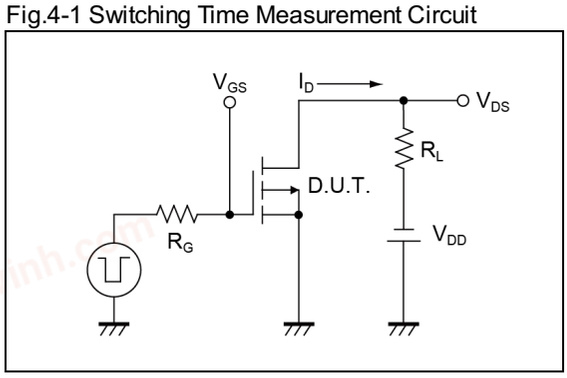


Fig.4-2 Switching Waveforms

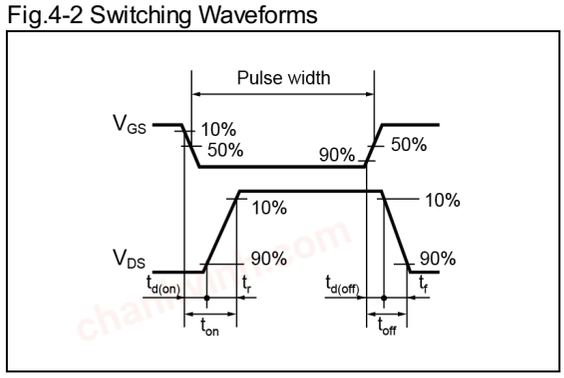


Fig.5-1 Gate Charge Measurement Circuit

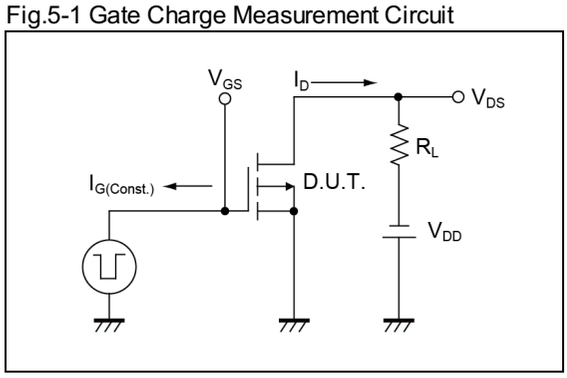


Fig.5-2 Gate Charge Waveform

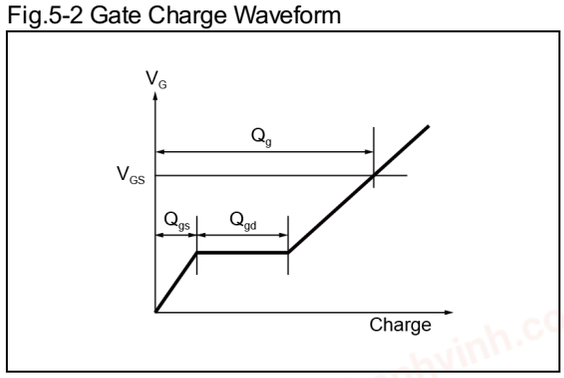


Fig.6-1 Avalanche Measurement Circuit

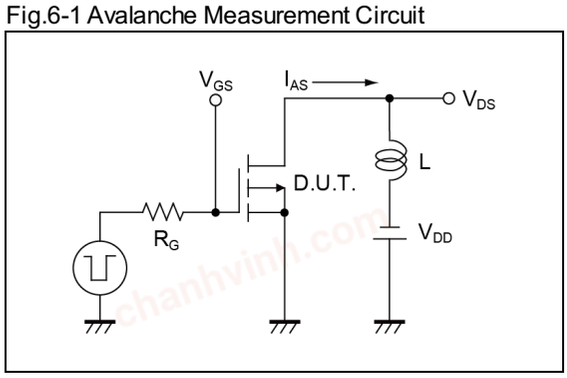
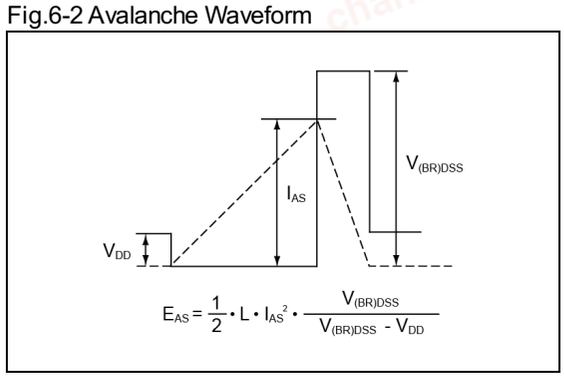


Fig.6-2 Avalanche Waveform



●Notice

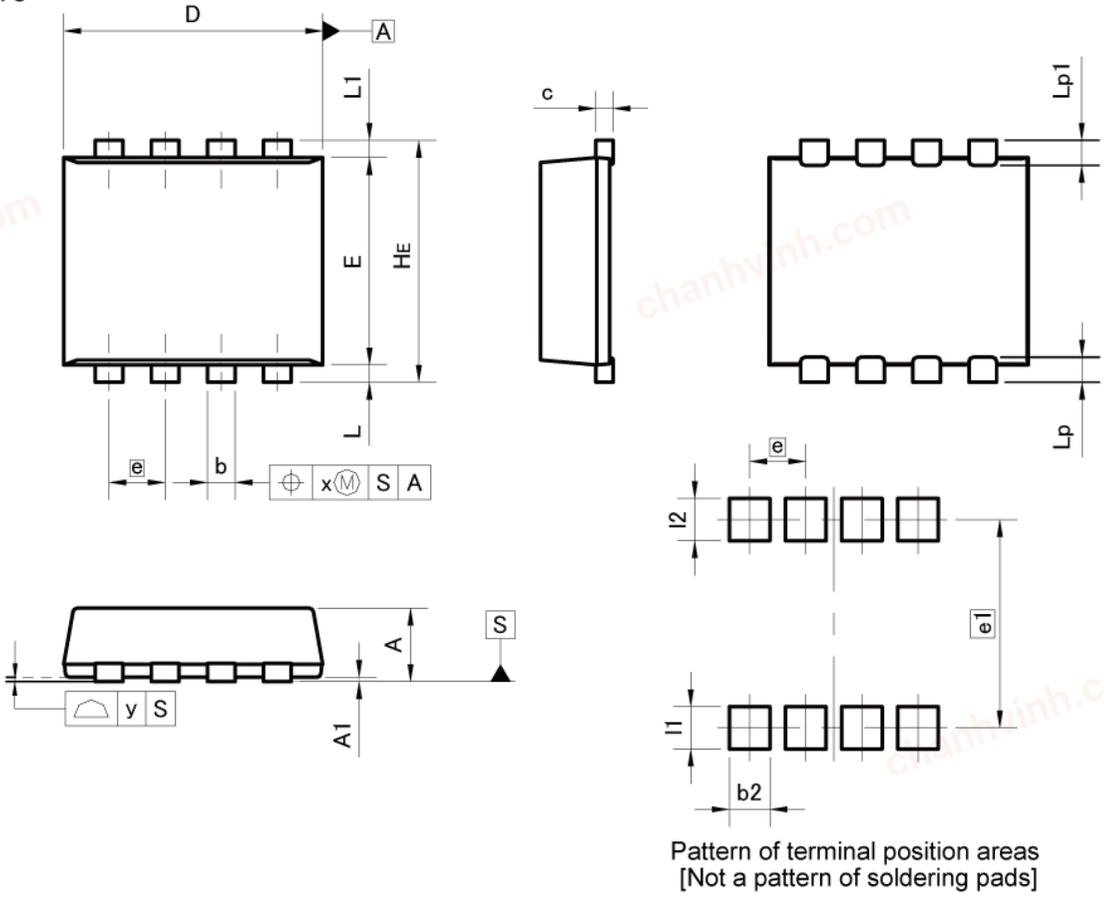
This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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●Dimensions

TSMT8



Pattern of terminal position areas
[Not a pattern of soldering pads]

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.75	0.85	0.030	0.033
A1	0.00	0.05	0.000	0.002
b	0.27	0.37	0.011	0.015
c	0.12	0.22	0.005	0.009
D	2.90	3.10	0.114	0.122
E	2.30	2.50	0.091	0.098
e	0.65		0.026	
HE	2.70	2.90	0.106	0.114
L	0.10	0.30	0.004	0.012
L1	0.10	0.30	0.004	0.012
Lp	0.19	0.39	0.007	0.015
Lp1	0.19	0.39	0.007	0.015
x	–	0.10	–	0.004
y	–	0.10	–	0.004

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
b2	–	0.47	–	0.019
e1	2.41		0.095	
l1	–	0.49	–	0.019
l2	–	0.49	–	0.019

Dimension in mm/inches

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