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Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

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ROHM GROUP
LAPIS TECHNOLOGY

FEDL62Q2500-04
Issue Date: Mar 26, 2024

ML62Q2500 Group

16-bit micro controller

GENERAL DESCRIPTION

ML62Q2500 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory(Flash memory), data memory(RAM), data Flash (Erase unit:128byte, Write unit:1byte) and rich peripheral functions such as the multiplier/divider, CRC generator, Clock generator, Timer, General Purpose Ports, UART, Synchronous serial port, I2C bus interface unit(Master, Slave), Voltage Level Supervisor(VLS), Successive approximation type 12bit A/D converter, Safety function (IEC60730/60335 Class B) and so on.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP (In-System Programming) function supports the Flash programming in production line.

- Applications

  Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc)

  Note:
  This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems.
  Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equipment, power transmission systems, core systems for financial terminals and various safety control devices.

- Product list

  The ML62Q2500 Group has products as show in the Table1 with multiple package and memory size combinations.

Table 1 Product List

Program memory	Data memory (RAM)	Data Flash	32pin TQFP32 WQFN32	40pin WQFN40	48pin TQFP48 WQFN48
128Kbyte	8Kbyte	4Kbyte	ML62Q2504	ML62Q2524	ML62Q2534
64Kbyte			ML62Q2502	ML62Q2522	ML62Q2532

Please see the last 2 pages “Notes for product usage” and “Notes” in this document on use with this product.

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FEATURES

- CPU
  - 16-bit RISC CPU : nX-U16/100 (A35 core)
  - Instruction system : 16-bit length instructions
  - Instruction set : Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Built-in On-chip debug function (connect to the Lapis Technolofy on-chip debug emulator)
  - Minimum instruction execution time : 1 count of system clock
    Approximately 30.5 µs/62.5ns/41.6ns (at 32.768 kHz/16 MHz/24MHz system clock)

- Coprocessor for multiplication and division
  - Signed or Unsigned is selectable

Parameter	Expression	Operation time [cycle]
Multiplication	16bit × 16bit	4
Division	32bit ÷ 16bit	8
	32bit ÷ 32bit	16
Multiply-accumulate (non-saturating, non-saturating)	16bit × 16bit + 32bit	4

- Operating voltage and temperature
  - Operating voltage : V_{DD} = 1.8 to 5.5 V
  - Operating temperature : -40 °C to +105 °C

- Flash memory

Parameter	Program memory area	Data Flash memory area
Erase/Write count	100 cycles	10,000 cycles
Write unit	32bit(4byte)	8bit(1byte)
Erase unit	16Kbyte/1Kbyte	all area/128byte
Erase/Write temperature	0 °C to +40 °C	-40 °C to +85 °C

  - Background Operation (CPU can work while erasing and rewriting to the Data Flash memory area.)
  - The built-in on-chip debug function and ISP (In-System Programming) function enable Flash programming

This product uses Super Flash® technology licensed from Silicon Storage Technology, Inc.
Super Flash® is a registered trademark of Silicon Storage Technology, Inc.

- Data RAM area
  - Rewrite unit: 8bit/16bit (1byte/2byte)
  - Parity check function is available (interrupt or reset is generatable at Parity error)

- Clock generation circuit
  - Low-speed clock (LSCLK)
    Internal low-speed RC oscillation (RC32K) : Approx. 32.768 kHz
    External low-speed clock input (EXT32K) : Approx. 32.768 kHz
    External low-speed crystal oscillation (XT32K) : Approx. 32.768 kHz,
    Selectable 4 mode (Tough, Normal, Low power mode, and Ultra low power mode)
  - High-speed clock (HSCLK)
    PLL oscillation: selectable 3 oscillation frequency (24MHz ,16MHz and 1MHz) by code option
  - Built-in dedicated clock generator (RC1K: Approx. 1.024kHz) for Watch Dog Timer (WDT)
  - High-speed time base clock (HTBCLK)
    Generates a clock with a period of 2 to 8 times that of HSCLK as a peripheral clock.

- Reset
  - System Resets by reset input pin, Power-On Reset, voltage level supervisor (VLS), WDT overflow, WDT invalid clear, RAM parity error, and PC error (unused ROM area access (instruction access))
  - Software reset by BRK instruction (reset CPU only)
  - Reset the peripherals individually/collectively by software

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- Power management
  - Optimal power management with various standby modes
    - STOP/STOP-D mode(All clocks are stopped), HALT-D mode(clocks for System and part of the periferal block are stopped), HALT/HALT-H mode(clocks for System are stopped)
    - HALT-D mode is suitable for long term standby, HALT-H mode is suitable for short term Intermittent operation standby
  - Indivisual clock input controll to the peripheral blocks by software
  - High-speed clock frequency(HSCLK) is configurable (1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of PLL clock, Max 7steps)
  - Clock gear: High-speed system clock frequency is changeable dynamically (1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of HSCLK, Max 6steps)

- Interrupt controller
  - Non-maskable interrupt source : 1 (Internal sources: WDT)
  - Maskable interrupt sources : 34 (included the external interrupt 8 sources)
  - Four step interrupt levels
  - External interrupt ports (EXI) : 8 (selectable from Max.24 pins) with sampling filter and edge(rise, fall, both) selection.

- General-purpose ports (GPIO)
  - I/O port : Max. 40 (Including pins for shared functions)
  - Input port: 3 (Including one pin for shared on-chip debug and two pins for shared low speed crystal oscillation)
  - Carrier frequency output function (for IR communication)

- Watchdog timer (WDT) : 1 channel
  - Overflow period : 8selectable (7.8, 15.6, 31.3, 62.5, 125, 500, 2000, 8000 ms)
  - Selectable window function (enable or disable):
    configurable clear enable period (50% or 75% of overflow period) with invalid clear
    When disable, Interrupts the first overflow and resets the second overflow
    When enable, reset occurs for the first overflow
  - Selectable WDT operation : select Enable or Disable by code option
  - Selectable operation in HALT/HALT-H mode and HALT-D mode(Continue counting/Stop counting)
  - WDT counter operation monitoring function (Readable WDT counter)

- Low-speed Time base counter(LTBC) : 2 channels
  - Generate 8 frequency (128, 64, 32, 16, 8, 4, 2, 1 Hz) internal pulse signals by dividing the Low-speed clock (LSCLK)
  - 4 interrupts are generatable from 8 different frequencys internal pulse signals
  - One of internal pulse signals selected to interrupt can be output from general purpose port (TBCO)

- Functional timer : 2 channels
  - Various modes (Continuous, One shot, capture, PWM with the same period and different duties, and complementary PWM output with the dead time)
  - Event trigger (external pin, 16bit timer, functional timer, LTBC, RC1K)
  - Selectable counter clock from various sources (divided by 1 to 8 of LSCLK, HSCLK, HTBCLK, and external clock)

- 16-bit General timers : 6 channels
  - Timer output (toggled by overflow)
  - Selectable counter clock from various sources (divided by 1 to 8 of LSCLK, HSCLK, HTBCLK, LTBC, RC1K, and external clock)
  - Timer X is shared with waiting for the stability of low-speed crystal oscillation

- Synchronous Serial Port : 2 channels (with FIFO: 1channel, without FIFO: 1channel)
  - FIFO: 4steps for each transmitting and receiving
  - Selectable from Master and Slave
  - Selectable from LSB first or MSB first
  - Selectable 8-bit length or 16-bit length

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- UART (Full-duplex communication mode): 3 channels
  - Selectable from 5 to 8bit length, parity or no parity, odd parity or even parity, 1 stop bit or 2 stop bits, Positive logic or Negative logic, LSB first or MSB first
  - Sampling filter for receiving data and start bit
  - Built-in baud rate generator (HSCLK@16MHz: 300bps to 2Mbps, LSCLK: up to 4800bps)

- I^2C bus : 2 channels
  - Select from Master mode or Slave mode: 1channel. Master mode only: 1channel
  - Standard mode (100 kbps), fast mode (400 kbps) and 1Mbps mode(1Mbps)
  - 7bit address format
  - Master mode: Handshake (Clock synchronization), 10bit slave address format is supported
  - Slave mode: Clock stretch function,

- Successive approximation type 12bit A/D converter (SA-ADC) : input 14 channels
  - Conversion time: Min. 1.375µs / ch (When the V_{DD} is higher than 2.7V and the conversion clock is 16MHz)
  - Reference voltages are selectable from VDD pin input voltage or External reference voltage (VREF pin)
  - dedicated result register for each channel
  - Continuous conversion, Trigger start, Interrupt determining by upper limit or lower limit threshold of conversion result

- Voltage Level Supervisor (VLS) : 1 channel
  - Threshold voltage: selectable from 15 level (from 1.85V to 4.00V)
  - Functional Voltage level detection reset (VLS reset) or Functional Voltage level detection interrupt (VLS0 interrupt) is generatable
  - Equipped with single mode / with sampling filter / low consumption operation

- CRC (Cyclic Redundancy Check) generator
  - Generation equation: $X^{16}+X^{12}+X^5+1$
  - Selectable from LSB first or MSB first
  - Built-in Automatic program memory CRC calculation mode in HALT mode

- Safety Function
  - Automatic switching to the internal low-speed RC oscillation in case the low-speed crystal oscillation stopped
  - RAM/SFR guard
  - Automatic program memory CRC calculation
  - RAM parity error detection
  - ROM unused area access reset (instruction access)
  - Clock mutual monitoring, WDT counter monitoring
  - SA-ADC test
  - Communication loop back test (UART, Synchronous serial port, I^2C bus(master))
  - GPIO test

- Shipping package

Package	Body size (including lead) [mm × mm]	Pin pitch [mm]	Packing form and Product name	
			Tray	Tape & Reel
32 pin plastic TQFP	7.0 × 7.0 (9.0 × 9.0)	0.80	ML62Q2502-xxxTBZWAX ML62Q2504-xxxTBZWAX	ML62Q2502-xxxTBZWBX ML62Q2504-xxxTBZWBX
48 pin plastic TQFP	7.0 × 7.0 (9.0 × 9.0)	0.50	ML62Q2532-xxxTBZWAX ML62Q2534-xxxTBZWAX	ML62Q2532-xxxTBZWBX ML62Q2534-xxxTBZWBX
32 pin plastic WQFN	5.0 × 5.0 (-)	0.50	ML62Q2502-xxxGDZW5AX ML62Q2504-xxxGDZW5AX	ML62Q2502-xxxGDZW5BX ML62Q2504-xxxGDZW5BX
40 pin plastic WQFN	6.0 × 6.0 (-)	0.50	ML62Q2522-xxxGDZW5AX ML62Q2524-xxxGDZW5AX	ML62Q2522-xxxGDZW5BX ML62Q2524-xxxGDZW5BX
48 pin plastic WQFN	7.0 × 7.0 (-)	0.50	ML62Q2532-xxxGDZW5AX ML62Q2534-xxxGDZW5AX	ML62Q2532-xxxGDZW5BX ML62Q2534-xxxGDZW5BX

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How To Read The Part Number

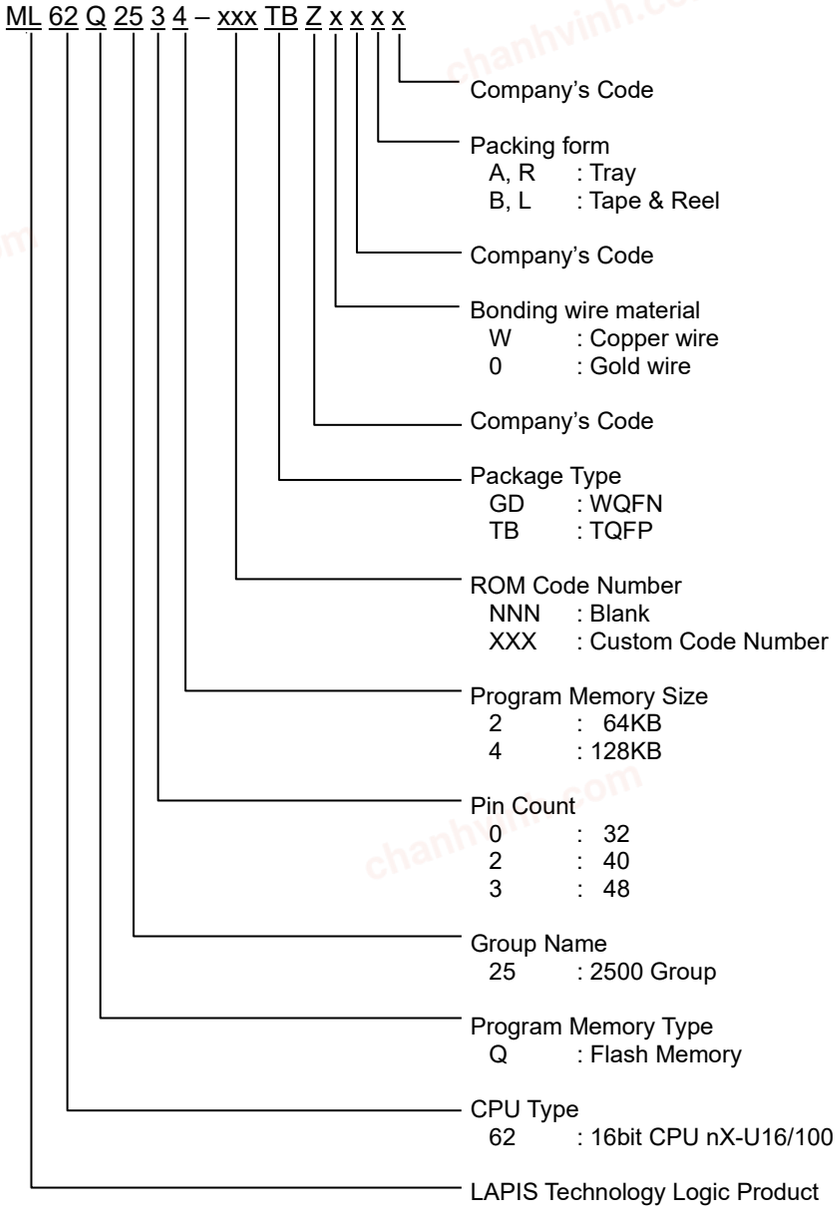

Figure 1 Part Number

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Main Function List

Table 2 Main Function List

Part number	Pin							Interrupt			Timer					Communication					Analog	
	Total pin	Power pin	Reset Input pin	Debug Input port	General purpose Input portpin *1	General purpose I/O port pin (LED drive is supported)	External interrupt pin	External interrupt source	Non maskable interrupt source	Internal maskable interrupt source	16bit Timer [ch]	16bit Functional Timer [ch]	16bit Functional Timer [Port]	Watchdog Timer [ch]	Time base counter [ch]	Synchronous serial (without FIFO) [ch]	Synchronous serial (with FIFO) [ch]	Full-duplex UART [ch]	I²C bus interface (Master only) [ch]	I²C bus unit (Master/Slave) [ch]	12bit Successive type A/D converter [ch]	Voltage Level Supervisor [ch]
ML62Q2502	32	3	1	1	3	24	16	8	1	26	6	2	4	1	2	1	1	3	1	1	14	1
ML62Q2504																						
ML62Q2522	40					32	19															
ML62Q2524																						
ML62Q2532	48					40	24															
ML62Q2534																						

*1: Shared with pins for crystal oscillation and debug input.

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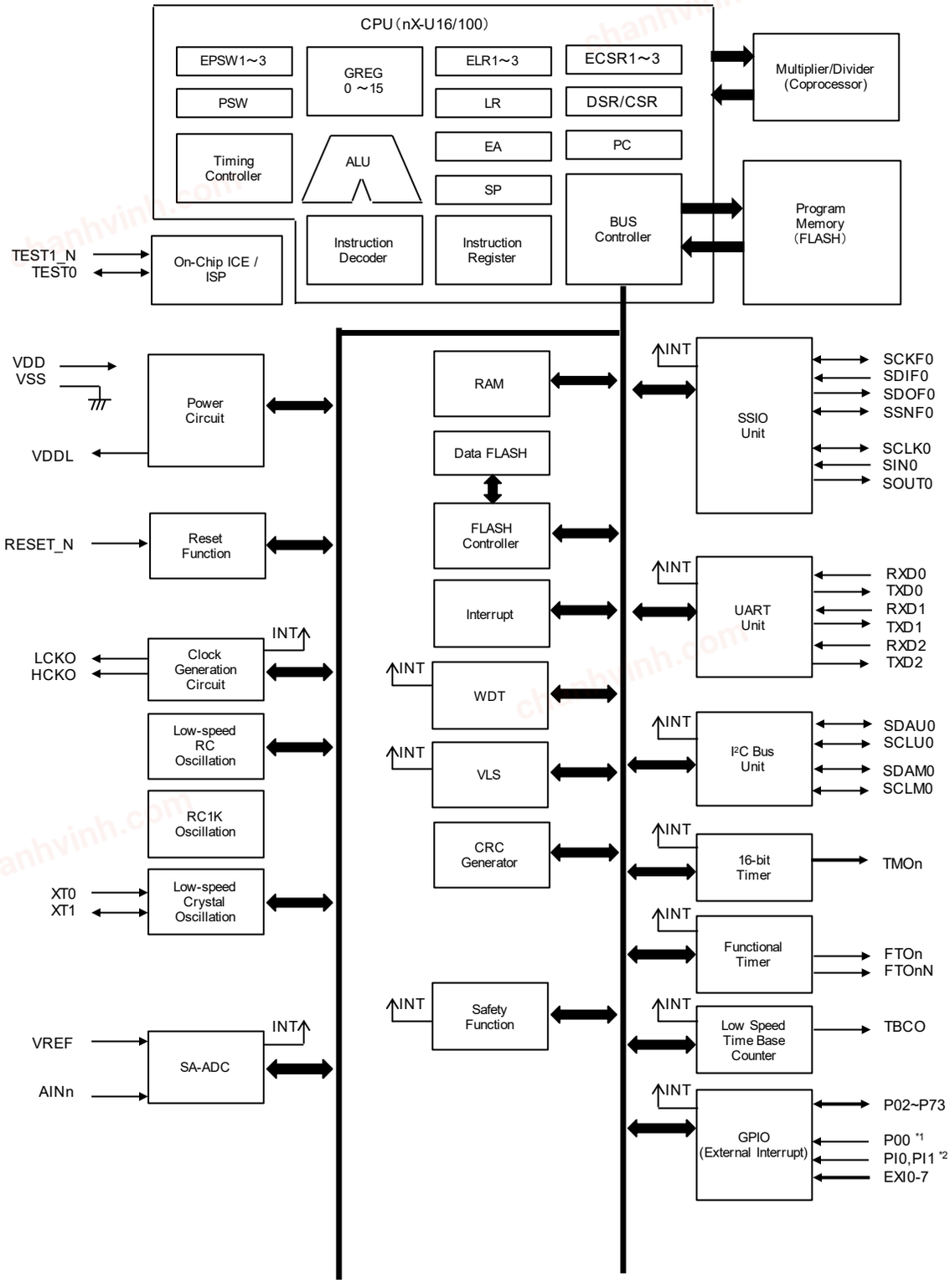
BLOCK DIAGRAM



*1 : Not available as the input port when connecting to the on-chip debug emulator.
*2 : Not available as the input port when connecting to the crystal resonator.

Figure 2 Block Diagram

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PIN CONFIGURATION

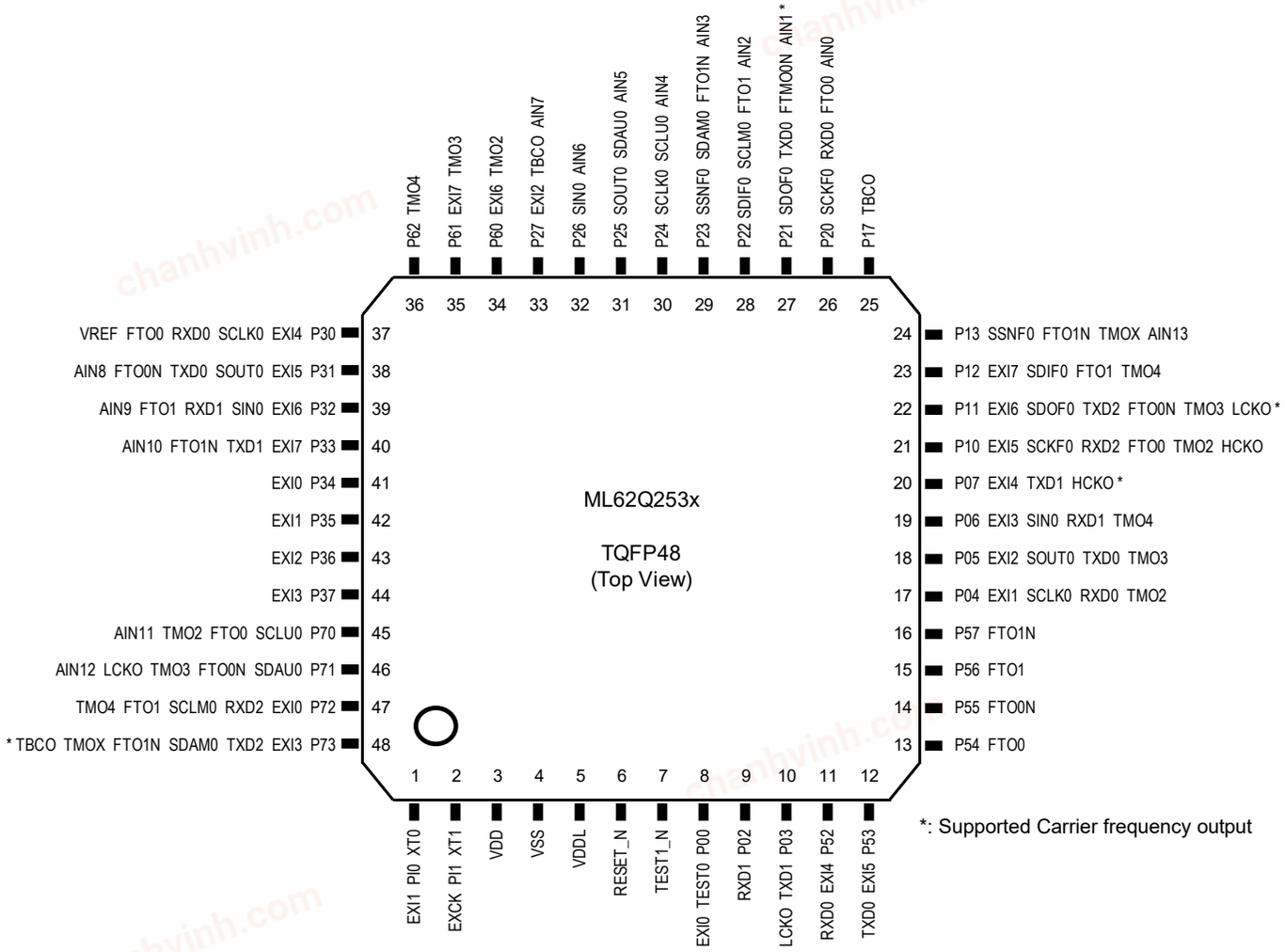

Fig.3-1 48 pin TQFP

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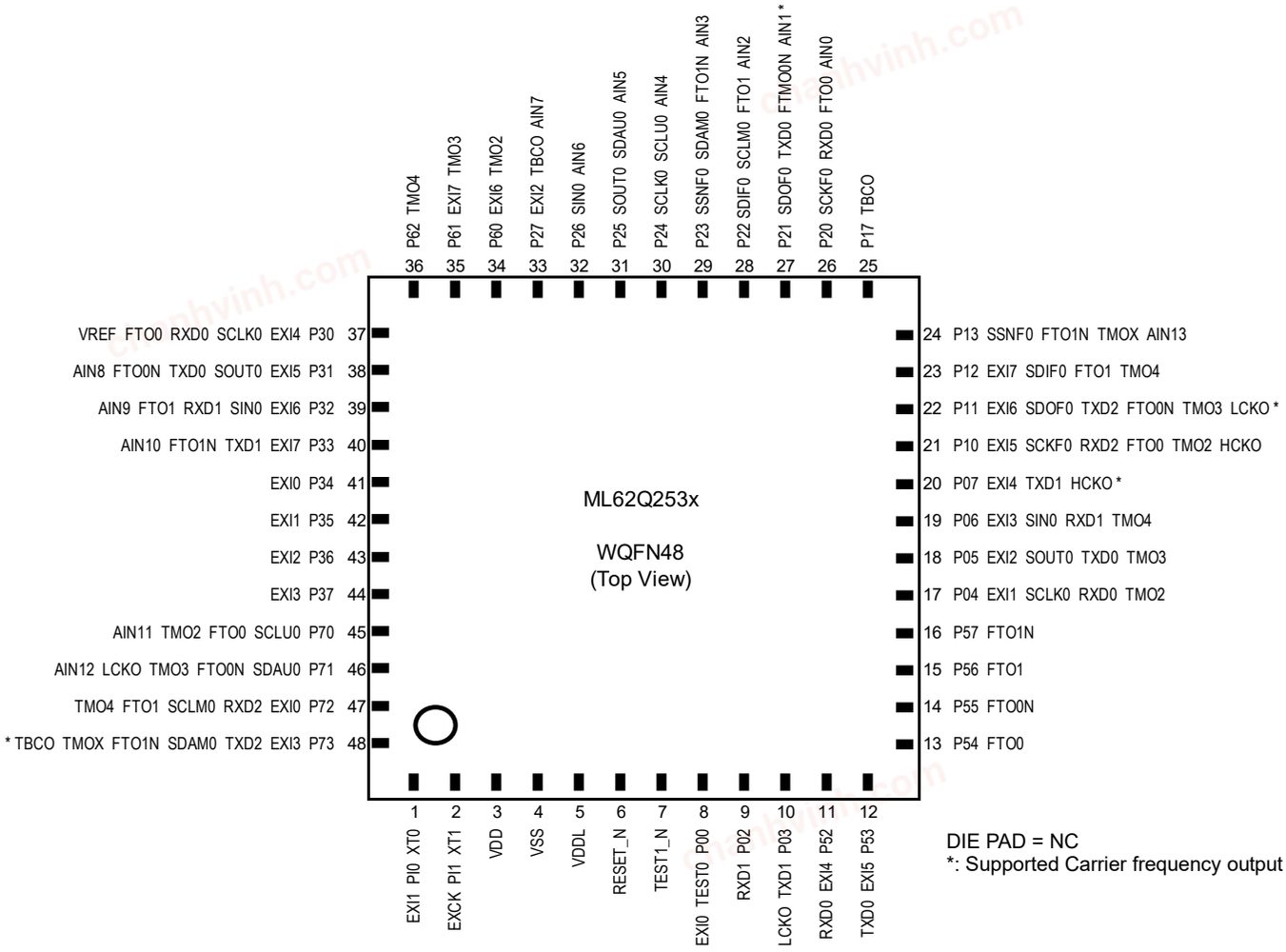

Fig.3-2 48 pin WQFN

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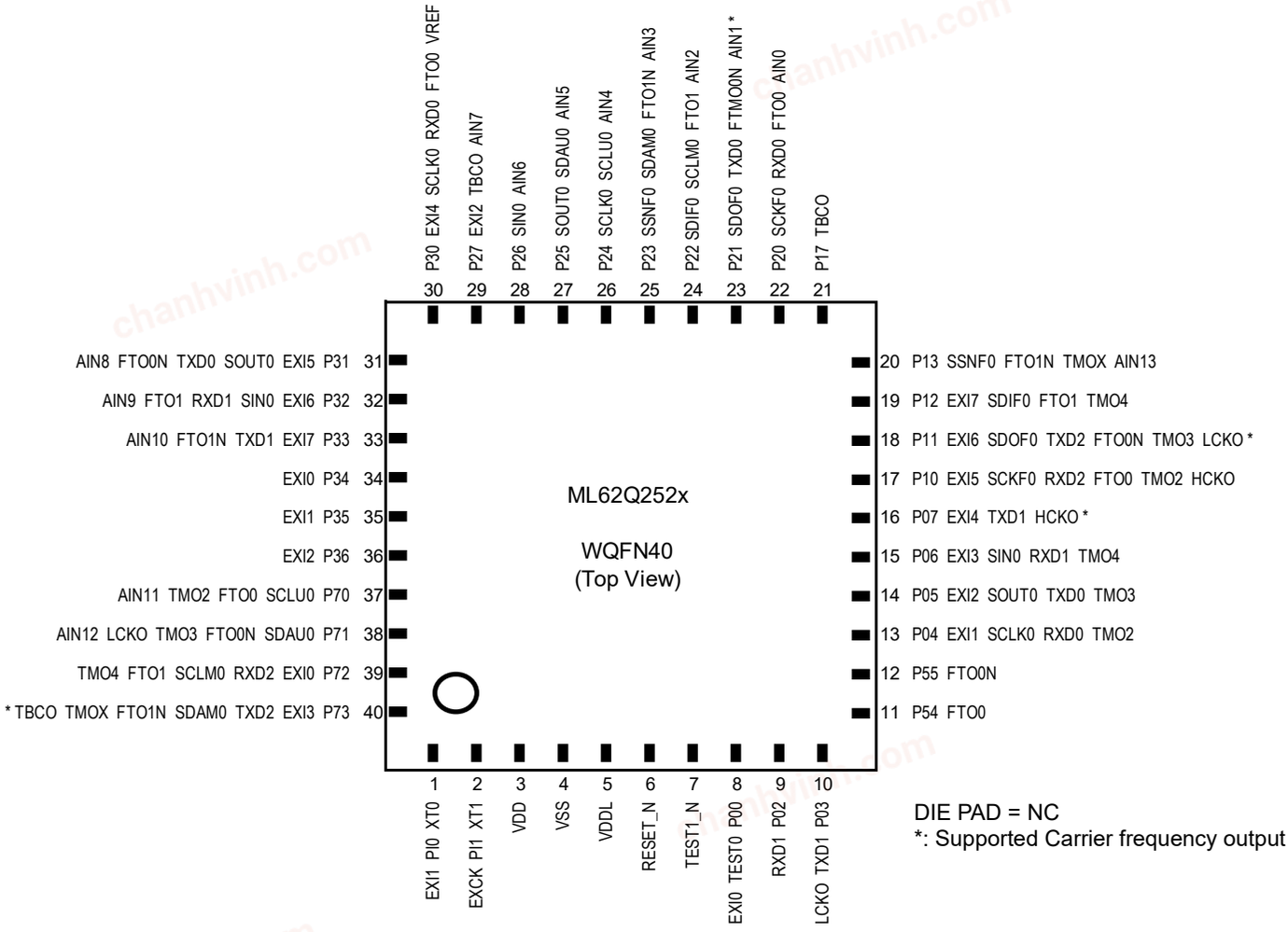

DIE PAD = NC
*: Supported Carrier frequency output

Fig.3-3 40 pin WQFN

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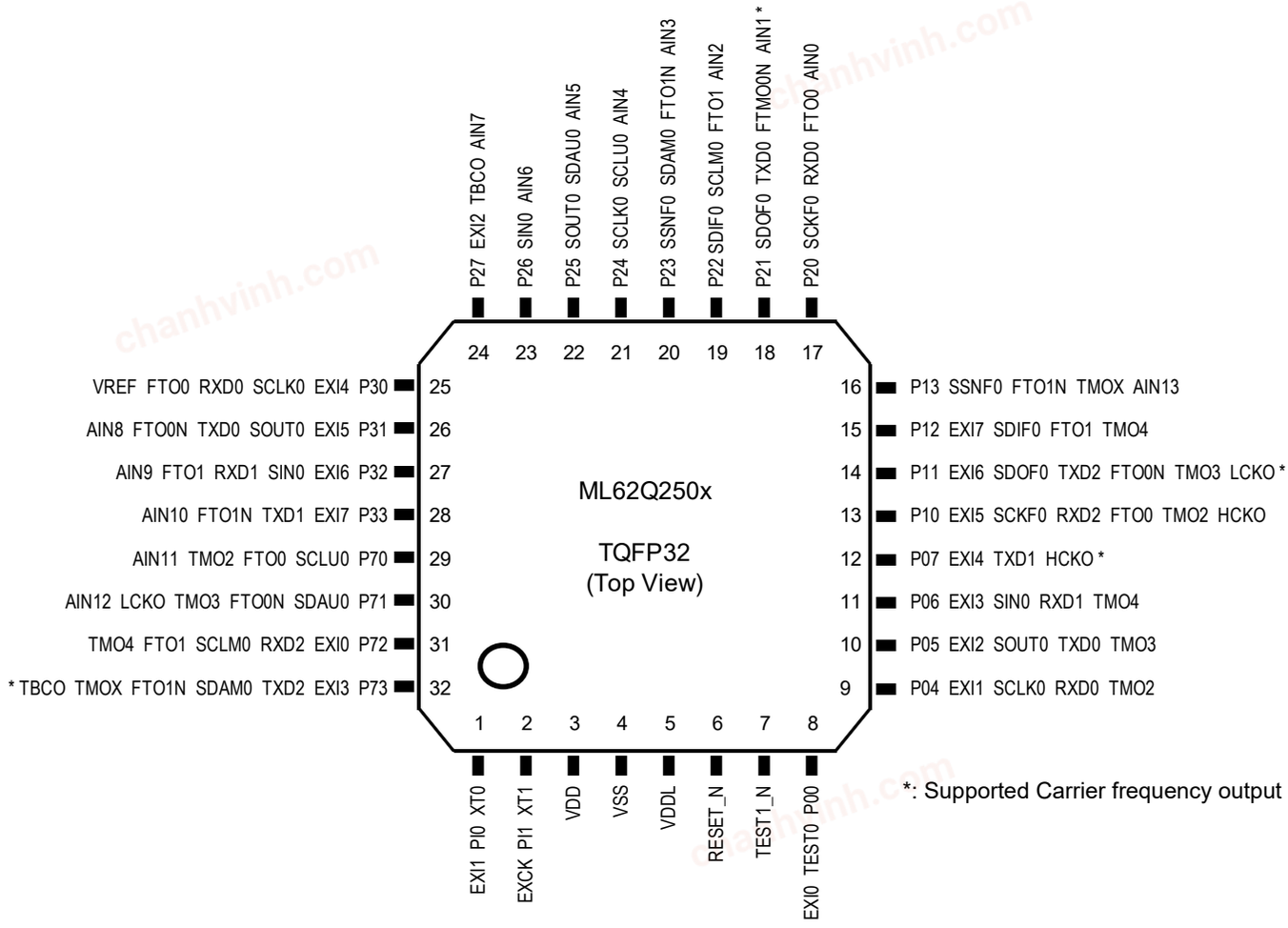

Fig.3-4 32 pin TQFP

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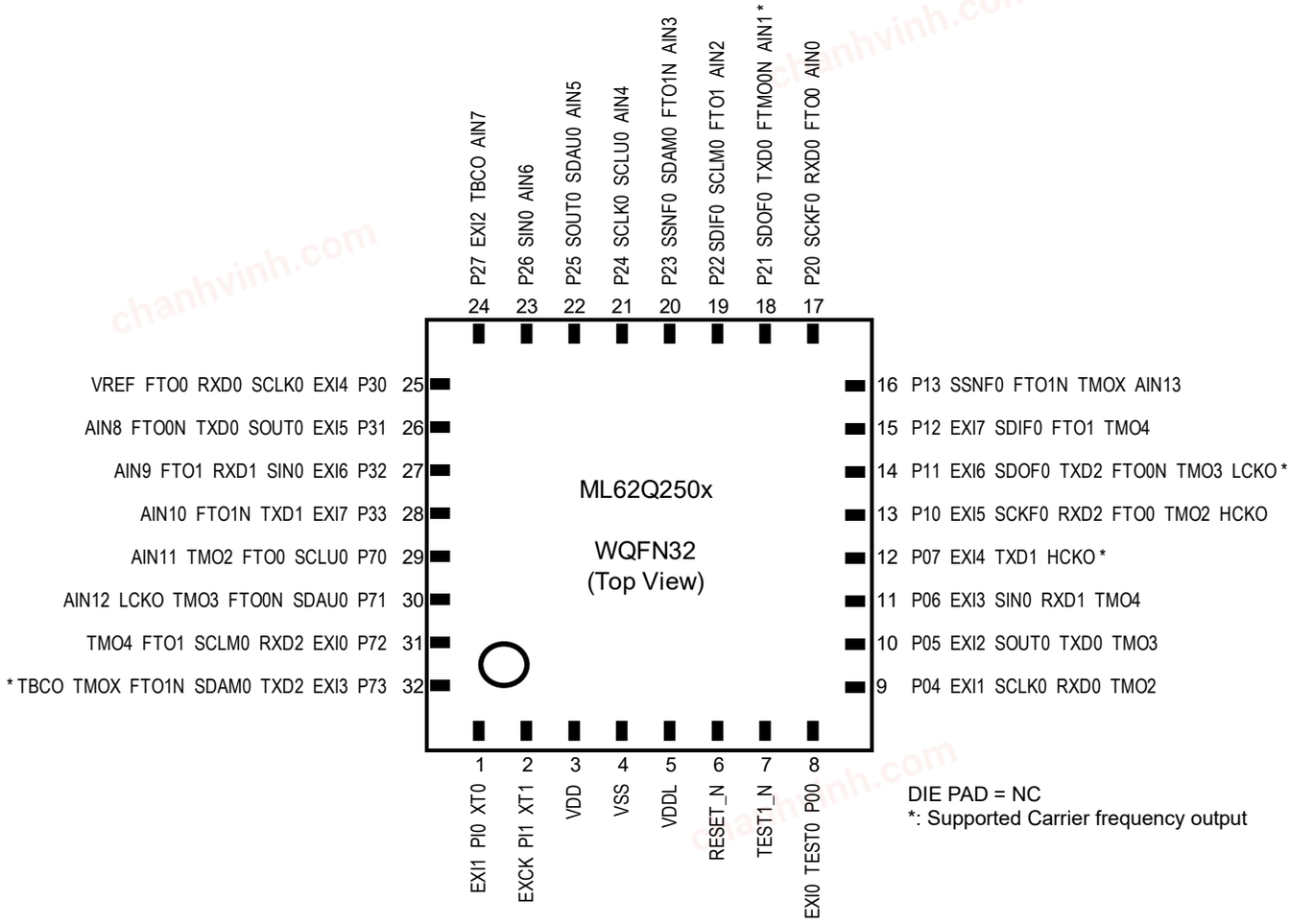

Fig.3-5 32 pin WQFN

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PIN LIST

Table 3 Pin List

Pin No.			Pin name	Career frequency output	1st func.	1st func.	2nd func.	3rd func.	4th func.	5th func.	6th func.	7th func.
ML62Q250x	ML62Q252x	ML62Q253x			GPI/EXI	ADC	SSIO*/**	UART	I2C*	FTM**	Timer	CLKOUT/ LTBC**
1	1	1	XT0	-	PI0/EXI1	-	-	-	-	-	-	-
2	2	2	XT1	-	PI1	-	-	-	-	-	-	-
3	3	3	VDD	-	-	-	-	-	-	-	-	-
4	4	4	VSS	-	-	-	-	-	-	-	-	-
5	5	5	VDDL	-	-	-	-	-	-	-	-	-
6	6	6	RESET_N	-	-	-	-	-	-	-	-	-
7	7	7	TEST1_N	-	-	-	-	-	-	-	-	-
8	8	8	P00/TEST0	-	EXI0	-	-	-	-	-	-	-
-	9	9	P02	-	-	-	-	RXD1	-	-	-	-
-	10	10	P03	-	-	-	-	TXD1	-	-	-	LCKO
9	13	17	P04	-	EXI1	-	SCLK0-0	RXD0	-	-	TMO2	-
10	14	18	P05	-	EXI2	-	SOUT0-0	TXD0	-	-	TMO3	-
11	15	19	P06	-	EXI3	-	SIN0-0	RXD1	-	-	TMO4	-
12	16	20	P07	●	EXI4	-	-	TXD1	-	-	-	HCKO
13	17	21	P10	-	EXI5	-	SCKF0-0	RXD2	-	FTO0	TMO2	HCKO
14	18	22	P11	●	EXI6	-	SDOF0-0	TXD2	-	FTO0N	TMO3	LCKO
15	19	23	P12	-	EXI7	-	SDIF0-0	-	-	FTO1	TMO4	-
16	20	24	P13	-	-	AIN13	SSNF0-0	-	-	FTO1N	TMOX	-
-	21	25	P17	-	-	-	-	-	-	-	-	TBCO
17	22	26	P20	-	-	AIN0	SCKF0-1	RXD0	-	FTO0	-	-
18	23	27	P21	●	-	AIN1	SDOF0-1	TXD0	-	FTO0N	-	-
19	24	28	P22	-	-	AIN2	SDIF0-1	-	SCLM0-0	FTO1	-	-
20	25	29	P23	-	-	AIN3	SSNF0-1	-	SDAM0-0	FTO1N	-	-
21	26	30	P24	-	-	AIN4	SCLK0-1	-	SCLU0-0	-	-	-
22	27	31	P25	-	-	AIN5	SOUT0-1	-	SDAU0-0	-	-	-
23	28	32	P26	-	-	AIN6	SIN0-1	-	-	-	-	-
24	29	33	P27	-	EXI2	AIN7	-	-	-	-	-	TBCO
25	30	37	P30	-	EXI4	VREF	SCLK0-2	RXD0	-	FTO0	-	-
26	31	38	P31	-	EXI5	AIN8	SOUT0-2	TXD0	-	FTO0N	-	-
27	32	39	P32	-	EXI6	AIN9	SIN0-2	RXD1	-	FTO1	-	-
28	33	40	P33	-	EXI7	AIN10	-	TXD1	-	FTO1N	-	-
-	34	41	P34	-	EXI0	-	-	-	-	-	-	-
-	35	42	P35	-	EXI1	-	-	-	-	-	-	-
-	36	43	P36	-	EXI2	-	-	-	-	-	-	-
-	-	44	P37	-	EXI3	-	-	-	-	-	-	-
-	-	11	P52	-	EXI4	-	-	RXD0	-	-	-	-
-	-	12	P53	-	EXI5	-	-	TXD0	-	-	-	-
-	11	13	P54	-	-	-	-	-	-	FTO0	-	-
-	12	14	P55	-	-	-	-	-	-	FTO0N	-	-
-	-	15	P56	-	-	-	-	-	-	FTO1	-	-
-	-	16	P57	-	-	-	-	-	-	FTO1N	-	-
-	-	34	P60	-	EXI6	-	-	-	-	-	TMO2	-
-	-	35	P61	-	EXI7	-	-	-	-	-	TMO3	-
-	-	36	P62	-	-	-	-	-	-	-	TMO4	-
29	37	45	P70	-	-	AIN11	-	-	SCLU0-1	FTO0	TMO2	-
30	38	46	P71	-	-	AIN12	-	-	SDAU0-1	FTO0N	TMO3	LCKO
31	39	47	P72	-	EXI0	-	-	RXD2	SCLM0-1	FTO1	TMO4	-
32	40	48	P73	●	EXI3	-	-	TXD2	SDAM0-1	FTO1N	TMOX	TBCO
DIE	DIE	DIE	NC	-	-	-	-	-	-	-	-	-

*: The SSIO and I2C use with a combination of the same suffix pins.
**: Assign each function; SCLK0/SCKF0/FTOn/FTOnN/HCKO, to only one LSI pin each.

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PIN DESCRIPTION

"I/O" Field in the below table define the pin type ("-" : power supply pin, "I" : Input pin, "O" : Out put pin, "I/O" bi-directional pin)

Table 4 Pin Description

Function	Functional pin name	LSI pin name	I/O	Description
Power	-	VSS	-	Negative power supply pin (-) Define this terminal potential as V_{SS}
	-	VDD	-	Positive power supply pin (+). Connect a capacitor C_V (more than 1µF) between this pin and VSS. Define this terminal potential as V_{DD}.
	-	VDDL	-	Power supply for internal logic (internal regulator's output). Connect a capacitor C_L (1µF) between this pin and VSS.
Debug ISP	TEST0	P00/ TEST0	I/O	Input/output for testing This pin which is shared with P00 is used as on-chip debug interface and ISP function and is initialized as pull-up input mode by the system reset.
	TEST1_N	TEST1_N	I	Input for testing This pin is used as on-chip debug interface and ISP function and is initialized as pull-up input mode by the system reset.
Reset	RESET_N	RESET_N	I	Reset input. Appling this pin "L" level shifts MCU to system reset mode. Appling this pin "H" level shifts MCU to program running mode. No pull-up resistor is built-in.
General input port (GPI)	PI0, PI1	XT0, XT1	I	General purpose input. - High-impedance (initial value) - Input without Pull-up
	P00	P00/ TEST0	I	General purpose input. - Input with Pull-up (initial value) - Input without Pull-up Not available as general inputs when using the on-chip debug interface or ISP function.
General port (GPIO)	P02 ~ P07	P02 ~ P07	I/O	General purpose input/output - High-impedance (initial value) - Input with Pull-up - Input without Pull-up - CMOS output - N channel (N-ch) open drain output
	P10 ~ P17	P10 ~ P17		
	P20 ~ P27	P20 ~ P27		
	P30 ~ P37	P30 ~ P37		
	P52 ~ P57	P52 ~ P57		
	P60 ~ P62	P60 ~ P62		
	P70 ~ P73	P70 ~ P73		
Clock Input	XT0	XT0	I	Connect a Low speed(32.768kHz) crystal resonator and connect capacitors between the pin and VSS. When inputting a square wave clock, input from XT1 pin
	XT1	XT1	I/O	
Clock Output (7th func.)	HCKO	P07 P10	O	High-speed clock output.
	LCKO	P03 P11 P71		Low-speed clock output.
	TBCO	P17 P27 P73		Low-speed time base counter output.
Career frequency output	-	P07 P11 P21 P73	O	Career frequency output
External Interrupt (1st func.)	EXI0	P00 P72 P34	I	External Maskable Interrupt 0 Input
	EXI1	P04 XT0 P35		External Maskable Interrupt 1 Input
	EXI2	P05 P27 P36		External Maskable Interrupt 2 Input
	EXI3	P06 P73 P37		External Maskable Interrupt 3 Input
	EXI4	P07 P30 P52		External Maskable Interrupt 4 Input
	EXI5	P10 P31 P53		External Maskable Interrupt 5 Input
	EXI6	P11 P32 P60		External Maskable Interrupt 6 Input
	EXI7	P12 P33 P61		External Maskable Interrupt 7 Input

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Function	Functional pin name	LSI pin name	I/O	Description
16bit General Timer (6th func.)	TMO2	P04 P10 P60 P70	O	16bit General Timer 2 output
	TMO3	P05 P11 P61 P71		16bit General Timer 3 output
	TMO4	P06 P12 P62 P72		16bit General Timer 4 output
	TMOX	P13 P73		16bit General Timer X output

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Function	Functional pin name	LSI pin name	I/O	Description
Functional Timer (5th func.)	FTO0	P10 P20 P30 P54 P70	O	Functional Timer0 P output
	FTO0N	P11 P21 P31 P55 P71		Functional Timer0 N output
	FTO1	P12 P22 P32 P56 P72		Functional Timer1 P output
	FTO1N	P13 P23 P33 P57 P73		Functional Timer1 N output
I2C Bus (4th func.)	SCLU0	P24 P70	I/O	I2C Unit0 Clock input/output
	SDAU0	P25 P71		I2C Unit0 Data input/output
	SCLM0	P22 P72		I2C Master0 Clock input/output
	SDAM0	P23 P73		I2C Master0 Data input/output
UART (3rd func.)	RXD0	P04 P20 P30 P52	I	UART0 received data input
	TXD0	P05 P21 P31 P53	O	UART0 transmission data output
	RXD1	P02 P06 P32	I	UART1 received data input
	TXD1	P03 P07 P33	O	UART1 transmission data output
	RXD2	P10 P72	I	UART2 received data input
	TXD2	P11 P73	O	UART2 transmission data output
Synchronous Serial Port (2nd func.)	SCKF0	P10 P20	I/O	Synchronous serial0 (with FIFO) clock input/output
	SDIF0	P12 P22	I	Synchronous serial0 (with FIFO) data input
	SDOF0	P11 P21	O	Synchronous serial0 (with FIFO) data output
	SSNF0	P13 P23	I/O	Synchronous serial0 (with FIFO) slave select input/output
	SCLK1	P04 P24 P30	I/O	Synchronous serial0 clock input/output
	SIN1	P06 P26 P32	I	Synchronous serial0 data input
	SOUT1	P05 P25 P31	O	Synchronous serial0 data output
Successive approximation type A/D converter (SA-ADC) (1st func.)	VREF	P30	I	SA-ADC external reference voltage input Define the potential of reference voltage for SA-ADC as V_{REF}
	AIN0~AIN13	P13 P27-P20 P33-P31 P71-P70	I	SA-ADC channel 0 to 13 analog input

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TERMINATION OF UNUSED PINS

Table 5 shows the processing of unused pins.

Table 5 Termination of unused pins

Pin	pin termination
NC	Open
RESET_N	Connect to V_{DD}
TEST1_N	Connect to V_{DD}
P00/TEST0	Open with the initial condition of pulled-up input mode
XT0, XT1	Open the pins with the initial condition of High impedance (input/output invalid) mode.
P02 ~ P07 P10 ~ P17 P20 ~ P27 P30 ~ P37 P52 ~ P57 P60 ~ P62 P70 ~ P73	

[Note]

- **Terminate unused input pins according to the table 5 in order to avoid unexpected through-current in the pins.**

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V_{DD}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}			-0.3 to +2.0	
Input voltage	V_{IN}			-0.3 to V_{DD}+0.3*1	
Output voltage1	V_{OUT1}			-0.3 to V_{DD}+0.3*1	
"H" level output current	I_{OUTH}	Ta = +25°C	1pin	-40*2	mA
			Total	-180*2	
"L" level output current	I_{OUTL}		1pin	+40	
			Total	+180	
Power dissipation	PD	Ta = +25°C		1	W
Storage temperature	T_{STG}	-		-55 to +150*3	°C

*1: 6.5V or lower
*2: The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*3: Please observe a storage conditions shown in the document "Board Mounting (soldering)" about the storage conditions until implementation.

[Note]

- **Stresses above the absolute maximum ratings listed in the above table may cause permanent damage to the device.**
  These are stress ratings only and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambient)	Ta	-	-40 to +105	°C
Operating temperature (Chip-Junction)	Tj	-	-40 to +115	
Operating voltage 1	V_{DD}	-	1.8 to 5.5	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.8 to 5.5V	30k to 25M	Hz
VDDL pin external capacitance	C_L	-	1.0 ±30%	µF

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Thermal characteristics

The maximum chip-junction temperature, T_{jmax}, is estimated using the following equation.

$T_{j\,max} = T_{a\,max} + P_{D\,max} \times \theta_{ja}$
$T_{a\,max}$: maximum ambient temperature
$P_{D\,max}$: LSI maximum power dissipation
θ_{ja} : Package junction to ambient thermal resistance

Design a Mounting board by considering heat radiation such as power dissipation and ambient temperature to satisfy the recommended conditions.

The following table shows the each package's thermal resistance for thermal design reference estimated by simulation based on the PCB (printed circuit board) conditions define as a below.

Parameter	Symbol	Package type	Value		Unit
			L1	L2	
Thermal resistance	θ_{ja}	WQFN32	50.6	43.5	°C/W
		TQFP32	67.6	61.8	
		WQFN40	32.8	28.9	
		WQFN48	31.1	27.4	
		TQFP48	60.2	56.9	

PCB conditions:

PCB name	L1	L2	Unit
PCB size (L / W / T)	114.3 / 76.2 / 1.6	114.3 / 76.2 / 1.6	mm
Number of layers	1	2	layer
Wiring density	60% (top layer)	60% (top and bottom layer)	-
Wind condition	No wind (0m/s)		-

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Current Consumption

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Condition		Rating				Unit	Measuring circuit
	Operating mode	Status of clocks *1	Min.	Typ.*2	Max.			
					Tj≤+95°C	Tj≤ +115°C		
IDD0	STOP-D	All clocks are stopped.	-	0.33	25	55	μA	1
IDD1	STOP	All clocks are stopped.	-	0.4	30	70		
IDD2-0R	HALT-D	RC32K is oscillating. XT32K/PLL are stopped.	-	0.6	28	60		
IDD2-0X	HALT-D	XT32K is oscillating in LP mode, without noise-filter. RC32K/PLL are stopped.	-	1.0	30	65		
IDD2-1R	HALT (High speed oscillation off)	RC32K is oscillating. XT32K/PLL are stopped.	-	0.9	30	70		
IDD3	CPU running in wait-mode SYSCLK=32.768kHz	RC32K is oscillating. XT32K/PLL are stopped.	-	10	45	75		
IDD4-H1	CPU running in wait-mode SYSCLK=1MHz	PLL is oscillating as PLL1M mode. HSCLK = 1MHz	-	0.22	0.33	0.35	mA	
IDD4-H16		PLL is oscillating as PLL16M mode. HSCLK = 1MHz	-	0.32	0.48	0.5		
IDD5-H16	CPU running in wait-mode SYSCLK=16MHz	PLL is oscillating as PLL16M mode. HSCLK = 16MHz	-	2.4	3.24	3.3		
IDD5-H24	CPU running in wait-mode SYSCLK=24MHz	PLL is oscillating as PLL24M mode. HSCLK = 24MHz	-	3.5	4.4	4.5		

*1: LTBC0(ch0) and WDT is operating except IDD0/1, and all clock supply to peripheral circuits are stopped by block control.. LSCLK1 is stopped. The code option VLMD is "1".
*2: On the condition of VDD=3.0V, Ta=+25°C

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Low speed Crystal Oscillation

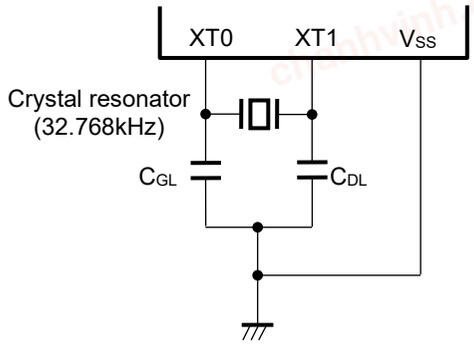
(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Crystal oscillation frequency *1 *2	f_{XTL}	-	-	32.768	-	kHz
Crystal oscillation start time	T_{XTL}	-	-	-	2	s

*1: The oscillation frequency is determined by the oscillation circuit, crystal resonator, and the external capacitance (CGL/CDL). As those parameters changes depending the crystal resonator, The matching evaluation using the actual PCB is required. Ask crystal resonator manufacture the matching evaluation to confirm the oscillation characteristics.

*2: In order to obtain the expected oscillation characteristics, it is necessary to design a PCB that considers the material and wiring pattern of the circuit board, as well as the wiring capacitance and parasitic capacitance of quartz crystals and terminals, etc. See below as reference for a PCB design.
- Keep the wiring layout for configuring the external circuit as short as possible.
- In order to shorten the wiring to the crystal unit and the crystal oscillator external capacitance as much as possible, place the crystal unit and the crystal oscillator external capacitance in close proximity to the MCU.
- Ensure no signal line flowing big current runs near the oscillation circuit.
- Ensure no signal line runs under and near the oscillation circuit.
- Make ground of external capacitance the same as MCU ground V_{SS} pin and connect them to the ground that has low variation of current and voltage.
- The quality of oscillation characteristics might be lost depending on operating environment due to moisture absorption of PCB and condensation of PCB surface, recommended to have measures such as covering the oscillation circuit with resin.

Example of external circuit for Low speed Crystal Oscillation



External Clock Input

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXCK}	-	Typ. -1.0%	32.768	Typ. +1.0%	kHz
Input pulse width	t_{EXCKW}	-	14.5	-	-	µs

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On-chip Oscillator

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
RC32K frequency	f_{RCL1}	Ta= -40 to +85°C except HALT-D mode		Typ. -1.5%	32.768	Typ. +1.5%	kHz	1
		Ta= -40 to +105°C except HALT-D mode		Typ. -2.0%		Typ. +2.0%		
	f_{RCL2}	HALT-D mode		Typ. -10%		Typ. +10%		
PLL oscillation frequency	f_{PLL1}	PLL 24MHz mode	Ta= -40 to +85°C with RC32K	Typ. -1.5%	24.002560	Typ. +1.5%	MHz	
			Ta= -40 to +105°C with RC32K	Typ. -2.0%		Typ. +2.0%		
		PLL 16MHz mode	Ta= -40 to +85°C with RC32K	Typ. -1.5%	16.007168	Typ. +1.5%		
			Ta= -40 to +105°C with RC32K	Typ. -2.0%		Typ. +2.0%		
		PLL 1MHz mode	Ta= -40 to +85°C with RC32K	Typ. -1.5%	0.999424	Typ. +1.5%		
			Ta= -40 to +105°C with RC32K	Typ. -2.0%		Typ. +2.0%		
PLL oscillation stabilization time	T_{PLL}	-		-	-	2	ms	
		wake-up from HALT-H VLMD=0 no temperature variation between before/after HALT-H		-	-	300	µs	
RC1K frequency (for WDT)	f_{RC1K}	Ta= -20 to +85°C		Typ. -15%	1.024	Typ. +15%	kHz	
		Ta= -40 to +105°C		Typ. -25%		Typ. +25%		

*: The frequency is the factory default specification. It may vary depending on the board mounting.

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Input / Output pin 1

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage1 "H"/"L" level (all input/output port)	VOH1	IOH1=-10mA V_{DD}≥4.5V	V_{DD} -1.5	-	-	V	2
		IOH1=-1mA V_{DD}≥1.8V	V_{DD} -0.5	-	-		
	VOL1	IOL1=+10mA V_{DD}≥4.5V	-	-	1.5		
		IOL1=+1mA V_{DD}≥1.8V	-	-	0.5		
Output voltage2 "L" level (all input/output port except P00/TEST0)	VOL2	When N-ch open drain output mode is selected: IOL2=+15mA V_{DD}≥4.5V	-	-	0.7		
		When N-ch open drain output mode is selected: IOL2=+8mA V_{DD}≥3.0V	-	-	0.5		
		When N-ch open drain output mode is selected: IOL2=+3mA V_{DD}≥2.0V	-	-	0.4		
		When N-ch open drain output mode is selected: IOL2=+2mA V_{DD}≥1.8V	-	-	0.4		

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Input current1 (RESET_N)	IIH1	VIH1=V_{DD}	-	-	1	μA	4
	IIL1	VIL1=V_{SS}	-1[*1]	-	-		
Input current2 (P00/TEST0/ TEST1_N)	IIL2	VIL2=V_{SS} (pull-up mode) [*2]	-1500[*1]	-300[*1]	-20[*1]		
	V/IIL2	VIL2=V_{SS} (pull-up mode) [*2]	3.7	10	80	kΩ	
	IIH2Z	VIH2=V_{DD} (High impedance mode)	-	-	1	μA	
	IIL2Z	VIL2=V_{SS} (High impedance mode)	-1[*1]	-	-		
Input current3 (all input port except RESET_N, TEST1N, P00/TEST0, input/output port)	IIL3	VIL1=V_{SS} (pull-up mode) [*2]	-250[*1]	-30[*1]	-2[*1]		
	V/IIL3	VIL1= V_{SS} (pull-up mode) [*2]	22	100	800	kΩ	
	IIH3Z	VIH1=V_{DD} (High impedance mode)	-	-	1	μA	
	IIL3Z	VIL1=V_{SS} (High impedance mode)	-1[*1]	-	-		
Input current4 (PI0, PI1)	IIH4	VIH1=V_{DD}	-	-	1		
	IIL4	VIL1=V_{SS}	-1[*1]	-	-		
Input voltage1 (all input port, input/output port)	VIH1	-	0.7 × V_{DD}	-	V_{DD}	V	5
	VIL1	-	0	-	0.3 × V_{DD}		
Pin capacitance (all input port, input/output port)	CPIN	f = 10kHz Ta = 25°C	-	-	10	pF	-

*1: The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value. For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*2: Measurement conditions: Typ: V_{DD} = 3.0V, Max: V_{DD} = 1.8V, Min: V_{DD} = 5.5V

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Input / Output pin 2

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
"H" level output current1 *6	IOH1	1pin	V_{DD}≥4.5V	-10*3*5	-	-	mA	3
			V_{DD}≥1.8V	-1*3*5	-	-		
"H" level output total current1 *1*4	IOH3	Total of group A or B ** (duty ≤ 50%)	V_{DD}≥4.5V	-90*5	-	-		
			V_{DD}≥1.8V	-20*5	-	-		
		All pin total (duty ≤ 50%)	V_{DD}≥4.5V	-180*5	-	-		
			V_{DD}≥1.8V	-40*5	-	-		
"L" level output current1 *6	IOL1	1pin (CMOS output mode)	V_{DD}≥4.5V	-	-	10*3		
			V_{DD}≥1.8V	-	-	1*3		
"L" level output current2 *6	IOL2	1pin (N-ch open drain output mode)	V_{DD}≥4.5V	-	-	15*3		
			V_{DD}≥3.0V	-	-	8*3		
			V_{DD}≥2.0V	-	-	3*3		
			V_{DD}≥1.8V	-	-	2*3		
"L" level output total current *2*4	IOL3	Total of group A or B ** (N-ch open drain output mode, duty≤50%)	V_{DD}≥4.5V	-	-	90		
			V_{DD}≥3.0V	-	-	40		
			V_{DD}≥2.0V	-	-	15		
			V_{DD}≥1.8V	-	-	10		
		All pin total (N-ch open drain output mode, duty≤50%)	V_{DD}≥4.5V	-	-	180		
			V_{DD}≥1.8V	-	-	20		
Output leak (all input/output port)	IOOH	VOH=V_{DD} (High impedance mode)		-	-	+1	μA	
	IOOL	VOL=V_{SS} (High impedance mode)		-1*5	-	-		

** : Group A is "P02 to P07, P10 to P17 and P52 to P57", group B is "P20 to P27, P30 to P37, P60 to P62 and P70 to P73".

*1: Tolerable current what can flow out from VDD pin to the output pin
*2: Tolerable current what can flow in from the output pin to VSS pin
*3: The total output current need to be within the rated range of IOH3 and IOL3.
*4: The total current is on the condition of Duty≤50% (same applies to IOH1).
When the duty ＞50% the total current is calculated by following formula.
Total current = IOL3 x 50/n (When the duty is n%)
<For an example> When IOL3=100mA and n=80%,
Total current = IOL3 x 50/80 = 62.5mA
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.
*5: The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*6: These values are satisfied with VOH1, VOL1 and VOL2.

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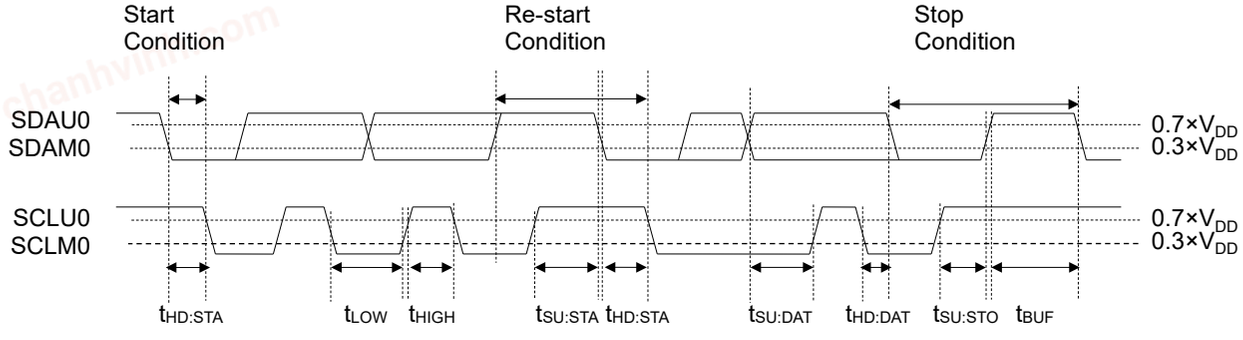
I²C Bus Interface

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Rating									Unit
		Standard Mode			Fast Mode			1Mbps Mode			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Voltage	V_{DD}	1.8	-	5.5	1.8	-	5.5	2.7	-	5.5	V
SCL clock frequency	f_{SCL}	0	-	100	0	-	400	0	-	1000	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	4.0	-	-	0.6	-	-	0.26	-	-	μs
SCL "L" level time	t_{LOW}	4.7	-	-	1.3	-	-	0.5	-	-	
SCL "H" level time	t_{HIGH}	4.0	-	-	0.6	-	-	0.26	-	-	
SCL setup time (restart condition)	$t_{SU:STA}$	4.7	-	-	0.6	-	-	0.26	-	-	
SDA hold time	$t_{HD:DAT}$	0	-	-	0	-	-	0	-	-	
SDA setup time	$t_{SU:DAT}$	0.25	-	-	0.1	-	-	0.1	-	-	
SDA setup time (stop condition)	$t_{SU:STO}$	4.0	-	-	0.6	-	-	0.26	-	-	
Bus-free time	t_{BUF}	4.7	-	-	1.3	-	-	0.5	-	-	

When using the I²C as the master, configure the I²C master 0 mode register(I2M0MOD) and I²C bus 0 mode register (master side, I2U0MOD) so that meet these specifications.



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Synchronous Serial Port

Slave mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle	t_{SCYC}	-	1*1	-	-	μs
SCLK input pulse width	t_{SW}	-	t_{SCYC} x 0.4	-	-	
SOUT output delay time	t_{SD}	V_{DD}≥2.4V	-	-	100	
		V_{DD}≥1.8V	-	-	200	
SIN input setup time	t_{SS}	-	80	-	-	
SIN input hold time	t_{SH}	-	50	-	-	

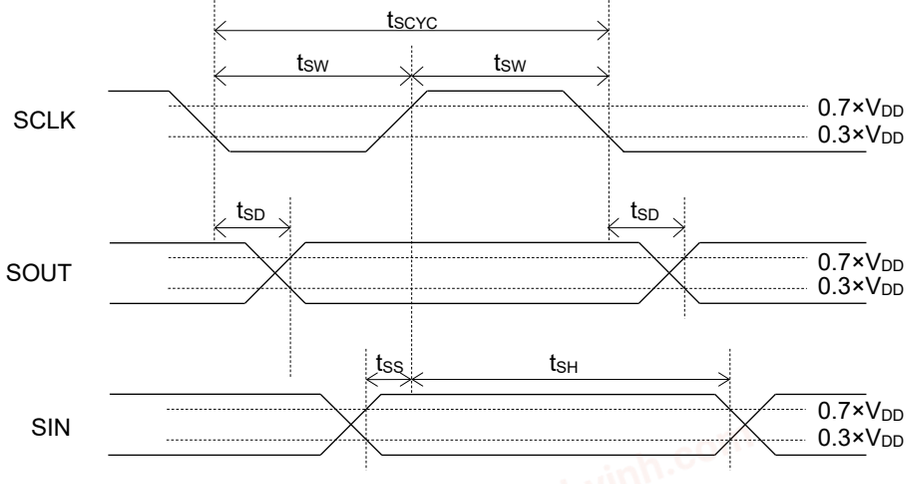
*1: Need input cycles of SYSCLK x 4 or longer

Master mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK output cycle	t_{SCYC}	V_{DD}≥2.4V	250	SCLK*2	-	ns
		V_{DD}≥1.8V	500	SCLK*2	-	
SCLK output pulse width	t_{SW}	-	t_{SCYC}×0.4	t_{SCYC}×0.5	t_{SCYC}×0.6	
SOUT output delay time	t_{SD}	V_{DD}≥2.4V	-	-	100	
		V_{DD}≥1.8V	-	-	160	
SIN input setup time	t_{SS}	V_{DD}≥2.4V	120	-	-	
		V_{DD}≥1.8V	180	-	-	
SIN input hold time	t_{SH}	V_{DD}≥2.4V	80	-	-	
		V_{DD}≥1.8V	100	-	-	

*2: Clock cycle selected by bit12 to 8(S0CK4 to 0) of the serial port 0 mode register (SIO0MOD)



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Synchronous Serial Port with FIFO

Slave mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCKF input cycle	t_{SCYC}	-	1*1	-	-	µs
SCKF input pulse width	t_{SW}	-	t_{SCYC} x 0.4	-	-	
SDOF output delay time	t_{SD}	V_{DD}≥2.4V	-	-	100	ns
		V_{DD}≥1.8V	-	-	200	
SDIF input setup time	t_{SS}	-	80	-	-	
SDIF input hold time	t_{SH}	-	50	-	-	

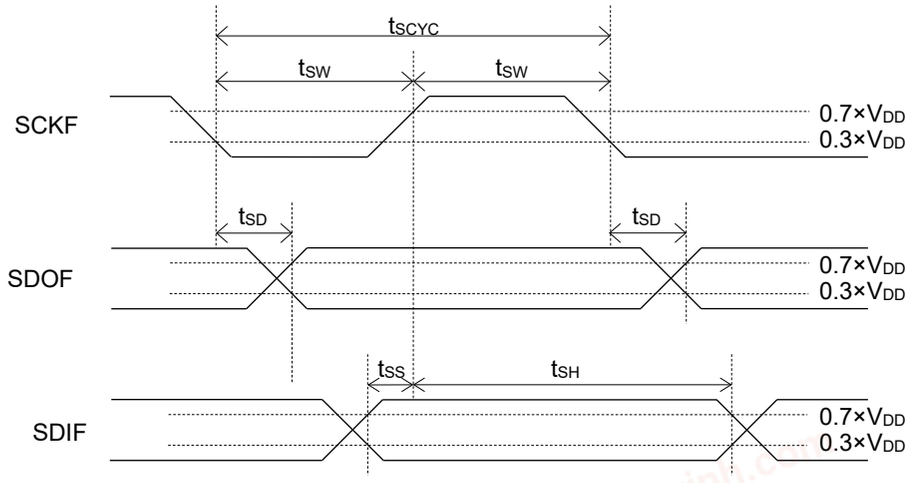
*1: Need input cycles of SYSCLK x 4 or longer

Master mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCKF output cycle	t_{SCYC}	V_{DD}≥2.4V	250	SCLK*2	-	ns
		V_{DD}≥1.8V	500	SCLK*2	-	
SCKF output pulse width	t_{SW}	-	t_{SCYC}×0.4	t_{SCYC}×0.5	t_{SCYC}×0.6	
SDOF output delay time	t_{SD}	V_{DD}≥2.4V	-	-	100	
		V_{DD}≥1.8V	-	-	160	
SDIF input setup time	t_{SS}	V_{DD}≥2.4V	120	-	-	
		V_{DD}≥1.8V	180	-	-	
SDIF input hold time	t_{SH}	V_{DD}≥2.4V	80	-	-	
		V_{DD}≥1.8V	100	-	-	

*2: Clock cycle selected by bit9 to 0(SF0BR9 to 0) of the SIOF0 baud rate register (SF0BRR)



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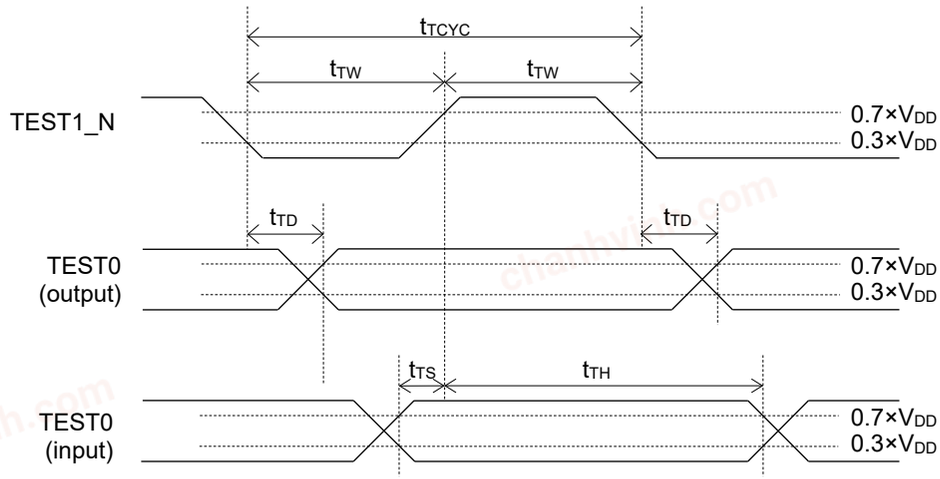
ISP interface

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
TEST1_N clock input cycle	t_{TCYC}	-	400	-	660	ns
TEST1_N input pulse width	t_{TW}	-	t_{TCYC} x 0.4	-	-	
TEST0 output delay time	t_{TD}	V_{DD}≥2.7V	-	-	80	
		V_{DD}≥1.8V	-	-	200	
TEST0 input setup time	t_{TS}	-	80	-	-	
TEST0 input hold time	t_{TH}	-	50	-	-	



EXI0~7 Timer Clock Input

(VDD=1.8 to 5.5V, VSS =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXI}	-	-	-	3	MHz
Input pulse width	t_{WEXI}	-	135	-	-	ns

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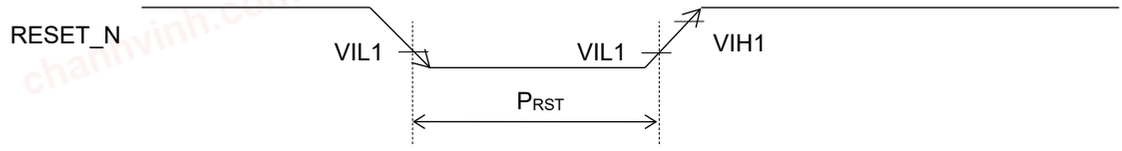
Reset

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Reset pulse width*1	P_{RST}	-	10	-	-	µs	1



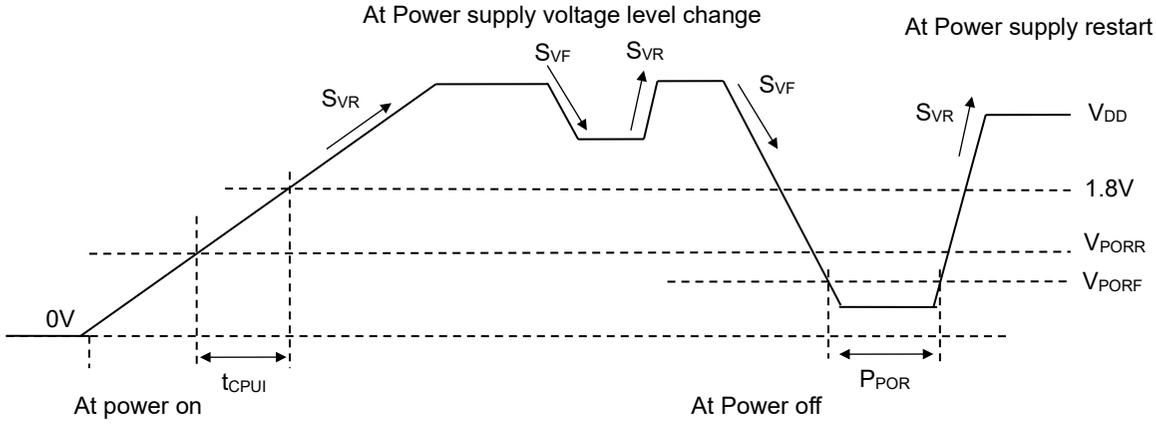
[Note]

- **RESET_N input shorter pulse than the Reset pulse width (P_{RST}) valid time should be avoided. The shorter pulse input may cause unexpected behavior.**

Slope of Power supply and Power On Reset

(V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Power supply voltage rising inclination	S_{VR}	-	-	-	60	V/ms	1
Power supply voltage falling inclination	S_{VF}	-	-	-	2		
Power on reset detection voltage	V_{PORR}	At Power up (rising)	1.50	1.63	1.80	V	
	V_{PORF}	At Power down (falling)	1.35	1.60	1.75		
Power on reset minimum pulse width	P_{POR}	-	500	-	-	µs	
CPU operation start time (from the release of reset to the CPU starts to run)	t_{CPUI}	-	13	21	35	ms	-



[Note]

- **If a pulse shorter than the Power on reset minimum pulse width is asserted to V_{DD}, it may cause the MCU malfunction. Apply prevent measurement such as bypass capacitors or external reset input, and so on.**
- **Set V_{DD} to 1.8V or higher before starting CPU operation.**

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VLS

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating						Unit	Measuring circuit
			Falling			Rising				
			V_{VLSF}			V_{VLSR}				
		VLS0LV[*1]	Min.	Typ.	Max.	Min.	Typ.	Max.		
VLS threshold voltage	V_{VLSR} V_{VLSF}	0H	3.83	3.99	4.15	3.84	4.05	4.26	V	1
		1H	3.53	3.68	3.83	3.55	3.74	3.93		
		2H	2.92	3.05	3.18	2.94	3.10	3.26		
		3H	2.84	2.96	3.08	2.85	3.01	3.17		
		4H	2.72	2.84	2.96	2.74	2.89	3.04		
		5H	2.65	2.76	2.87	2.66	2.80	2.94		
		6H	2.55	2.66	2.77	2.56	2.70	2.84		
		7H	2.43	2.54	2.65	2.45	2.58	2.71		
		8H	2.35	2.45	2.55	2.36	2.49	2.62		
		9H	2.25	2.35	2.45	2.27	2.39	2.51		
		AH	2.15	2.24	2.33	2.16	2.28	2.40		
		BH	2.07	2.16	2.25	2.08	2.19	2.30		
		CH	1.96	2.05	2.14	1.98	2.09	2.20		
		DH	1.87	1.95	2.03	1.89	1.99	2.09		
		EH	1.77	1.85	1.93	1.78	1.88	1.98		

[*1]: Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS current consumption	I_{VLS}	-	-	10	-	nA	1

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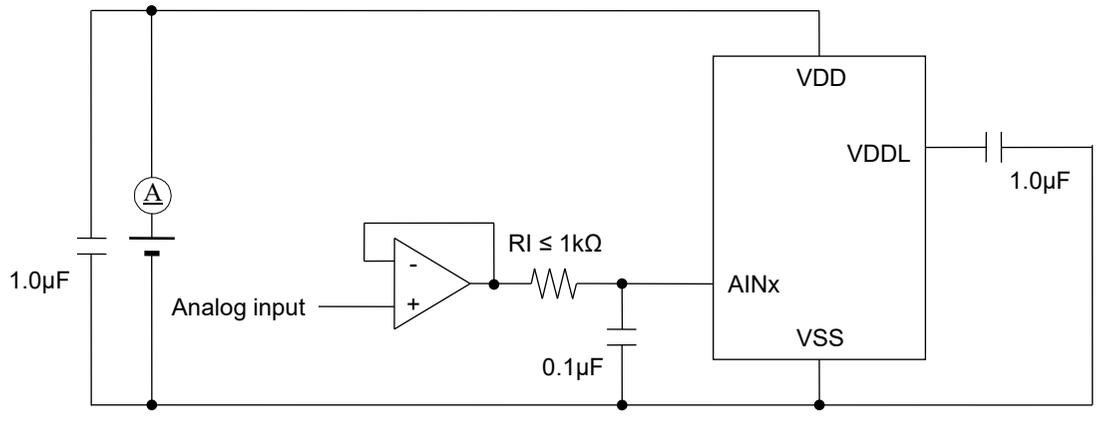
Successive Approximation Type A/D Converter

(V_{DD}=2.1 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit
Resolution	n_{AD}	-		-	-	12	bit
Conversion clock	f_{ADCLK}	nominal value, V_{DD} ≥ 2.7V, V_{REF} ≥ 2.7V		32.768	-	16000	kHz
		nominal value, V_{DD} ≥ 2.4V, V_{REF} ≥ 2.4V		32.768	-	8000	
		nominal value, V_{DD} ≥ 2.1V, V_{REF} ≥ 2.1V		32.768	-	1000	
Conversion time	t_{CONV}	f_{ADCLK} = 16MHz		1.375	-	-	µs
		f_{ADCLK} = 32.768kHz		-	518.799	-	
SA-ADC reference potential	V_{REF}	V_{DD} ≥ V_{REF}		2.1	-	V_{DD}	V
Overall error	-	4.5V ≤ V_{REF} ≤ 5.5V		-6	-	+6	LSB
Integral non-linearity error	INL_{AD}	f_{ADCLK} = 16MHz	2.7V ≤ V_{REF}	-4	-	+4	LSB
		f_{ADCLK} = 8MHz	2.4V ≤ V_{REF}	-7	-	+7	
		f_{ADCLK} = 1MHz	2.1V ≤ V_{REF}	-8	-	+8	
Differential non-linearity error	DNL_{AD}	f_{ADCLK} = 16MHz	2.7V ≤ V_{REF}	-3	-	+3	
		f_{ADCLK} = 8MHz	2.4V ≤ V_{REF}	-5	-	+5	
		f_{ADCLK} = 1MHz	2.1V ≤ V_{REF}	-7	-	+7	
Zero-scale error	ZSE	f_{ADCLK} = 16MHz		-8	-	+8	
		f_{ADCLK} = 8MHz		-8	-	+8	
		f_{ADCLK} = 1MHz		-10	-	+10	
Full-scale error	FSE	f_{ADCLK} = 16MHz		-8	-	+8	
		f_{ADCLK} = 8MHz		-8	-	+8	
		f_{ADCLK} = 1MHz		-10	-	+10	



The current flows during the SA-ADC sampling as it takes charging. Make the output impedance of the analog signal source 1kΩ or smaller. Also, putting 0.1µF capacitor on the ADC input pin is recommended for noise reduction.

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Flash Memory

(V_{SS}= 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +85	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		+1.8 to +5.5	V
Maximum rewrite count	CEPD	Data Flash		10000	times
	CEPP	Program Flash		100	
Erasing unit	-	Block erasing	Program Flash	16K	Byte
			Data Flash	all area	
	-	Sector erasing	Program Flash	1K	Byte
			Data Flash	128	
Erasing time (Max.)	-	Block erasing / Sector erasing		50	ms
Writing unit	-	Program Flash		4	Byte
		Data Flash		1	
Writing time (Max.)	-	Program Flash		80	µs
	-	Data Flash		40	
Data retention period	YDR	rewriting count 100 times		15	years

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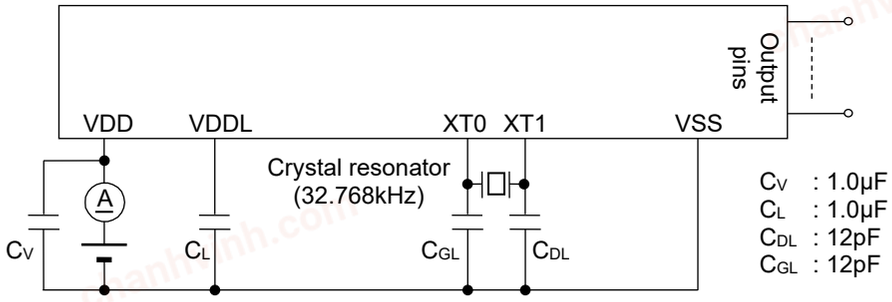
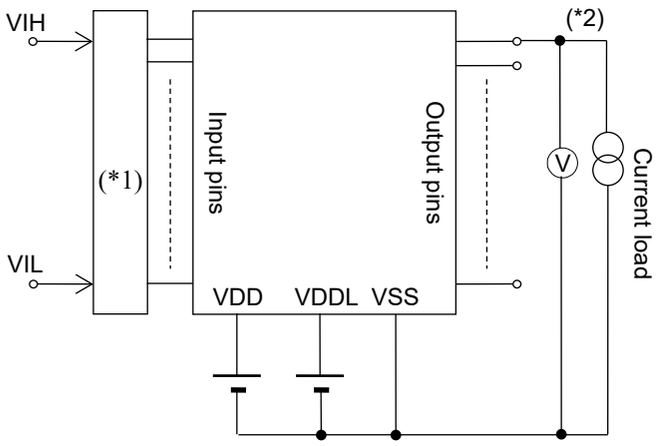
Measuring circuit

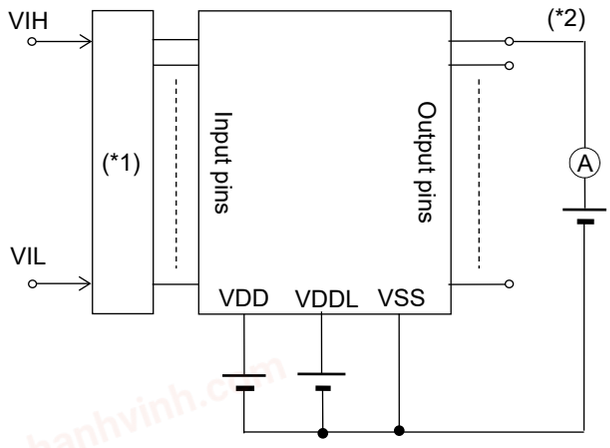
Measuring circuit 1



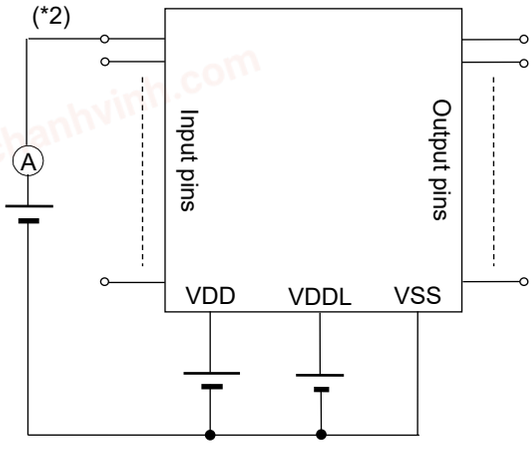
Measuring circuit 2



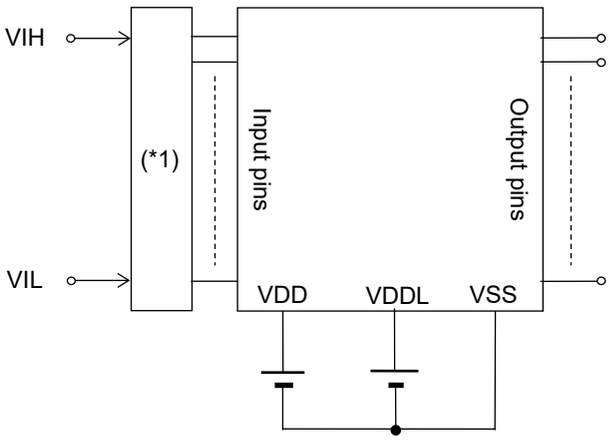
Measuring circuit 3



Measuring circuit 4



Measuring circuit 5



(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

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Characteristics graphs

These Graphs on the following pages are references for designing an application.

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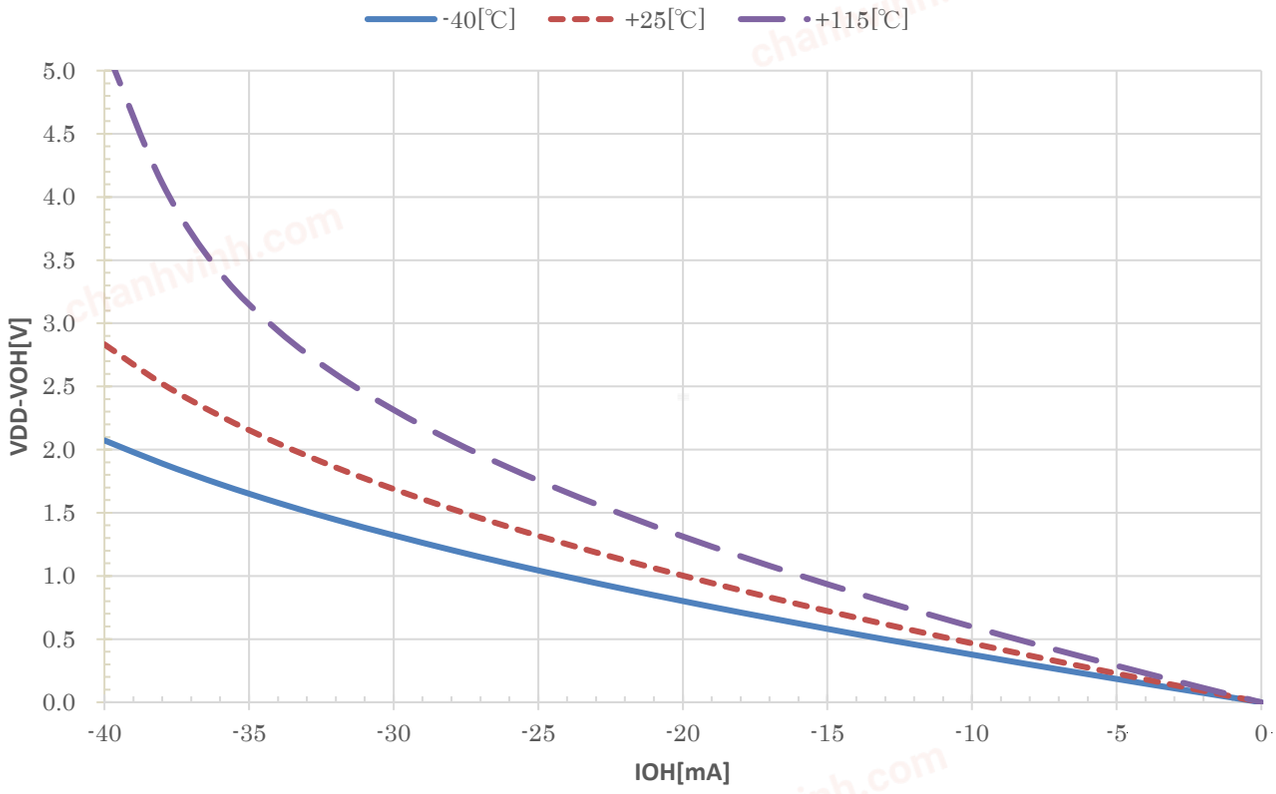
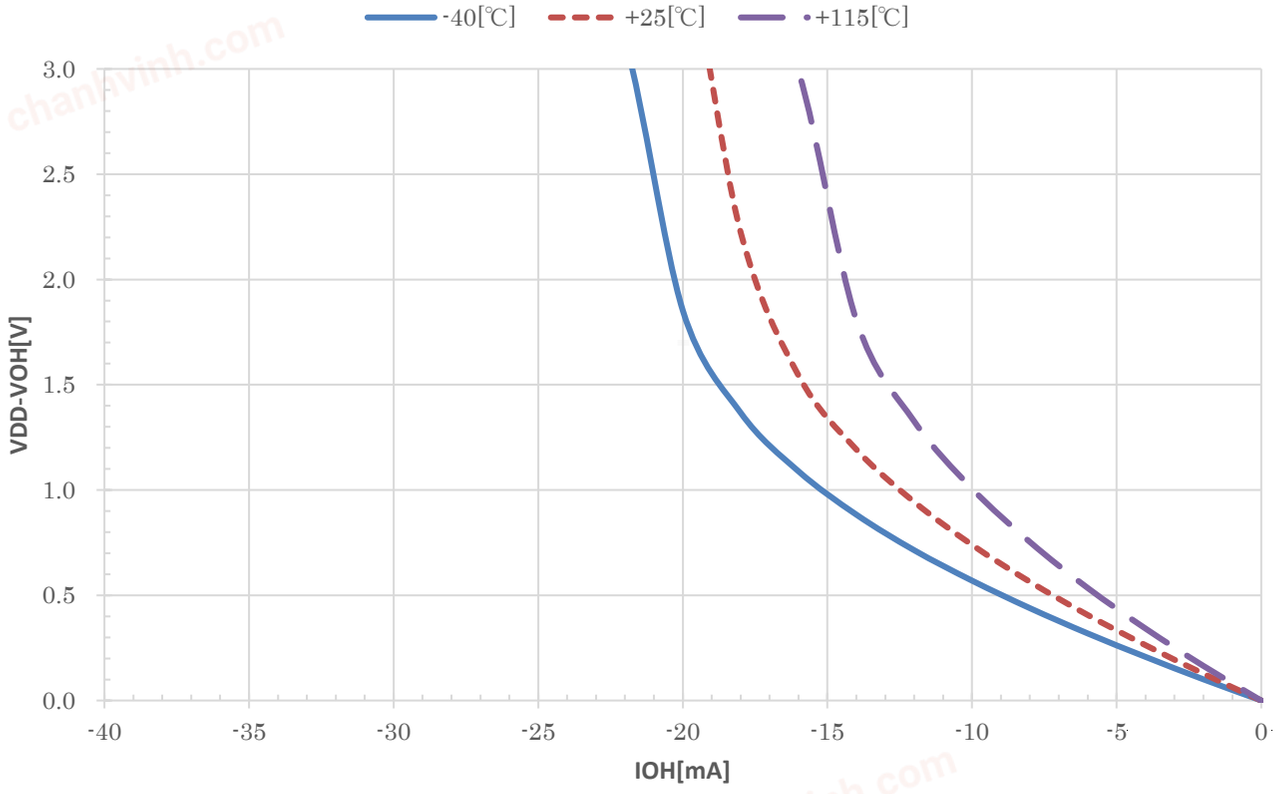
– VDD-VOH1 vs IOH (VDD=5V TYP.)



– VDD-VOH1 vs IOH (VDD=3V TYP.)



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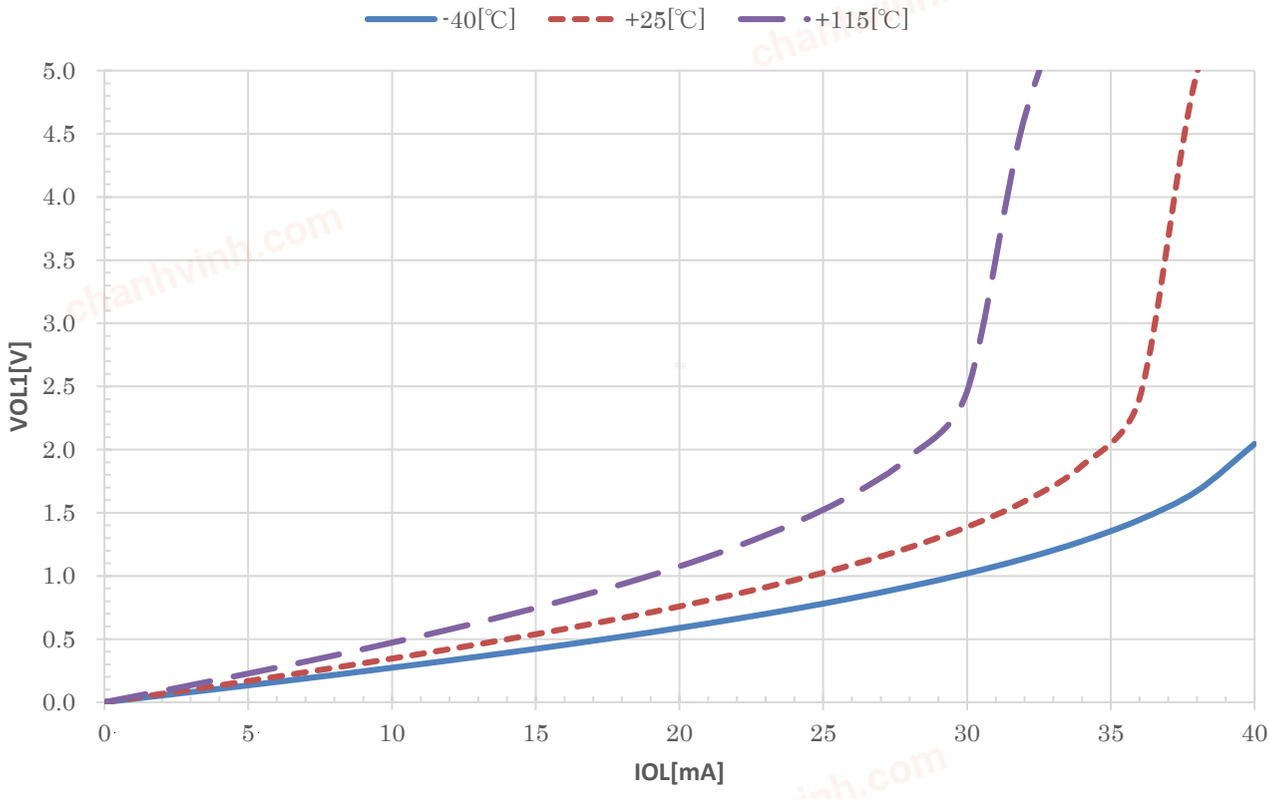
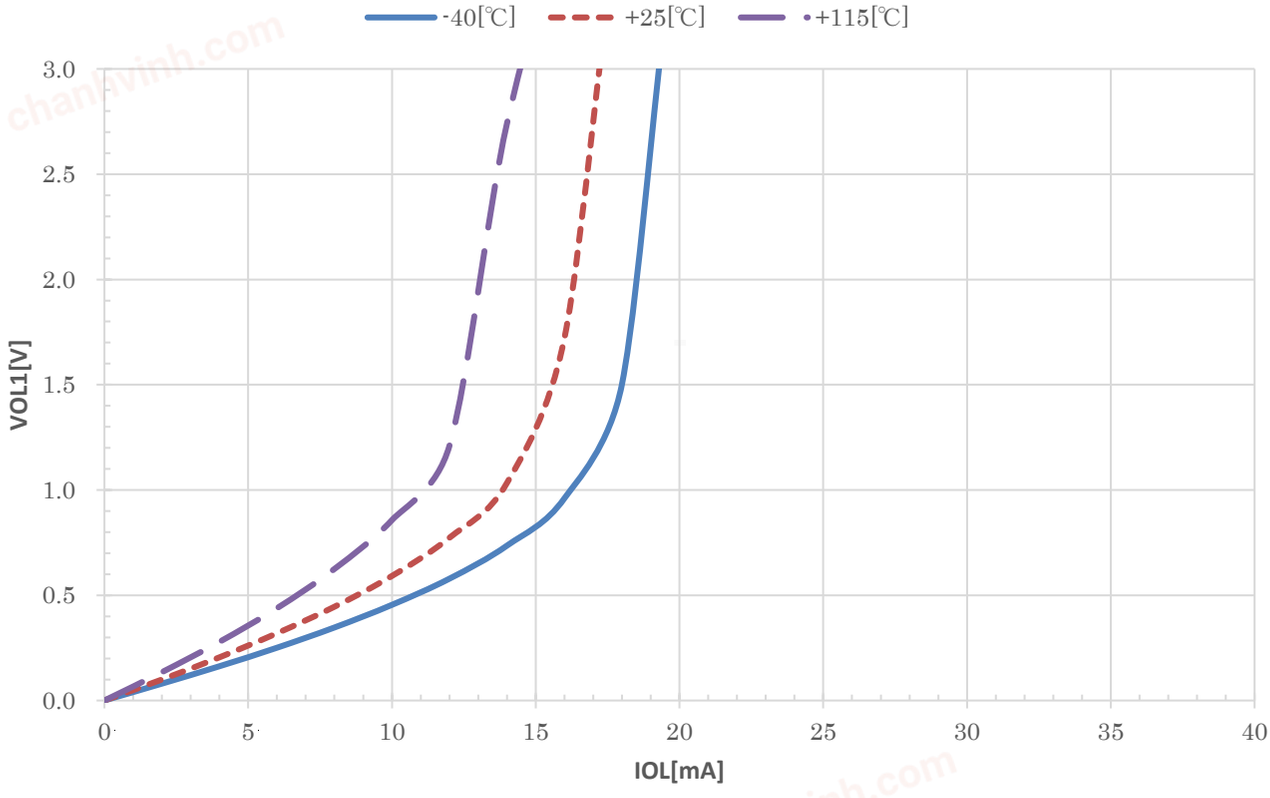
– VOL1 vs IOL (VDD=5V TYP.)



– VOL1 vs IOL (VDD=3V TYP.)



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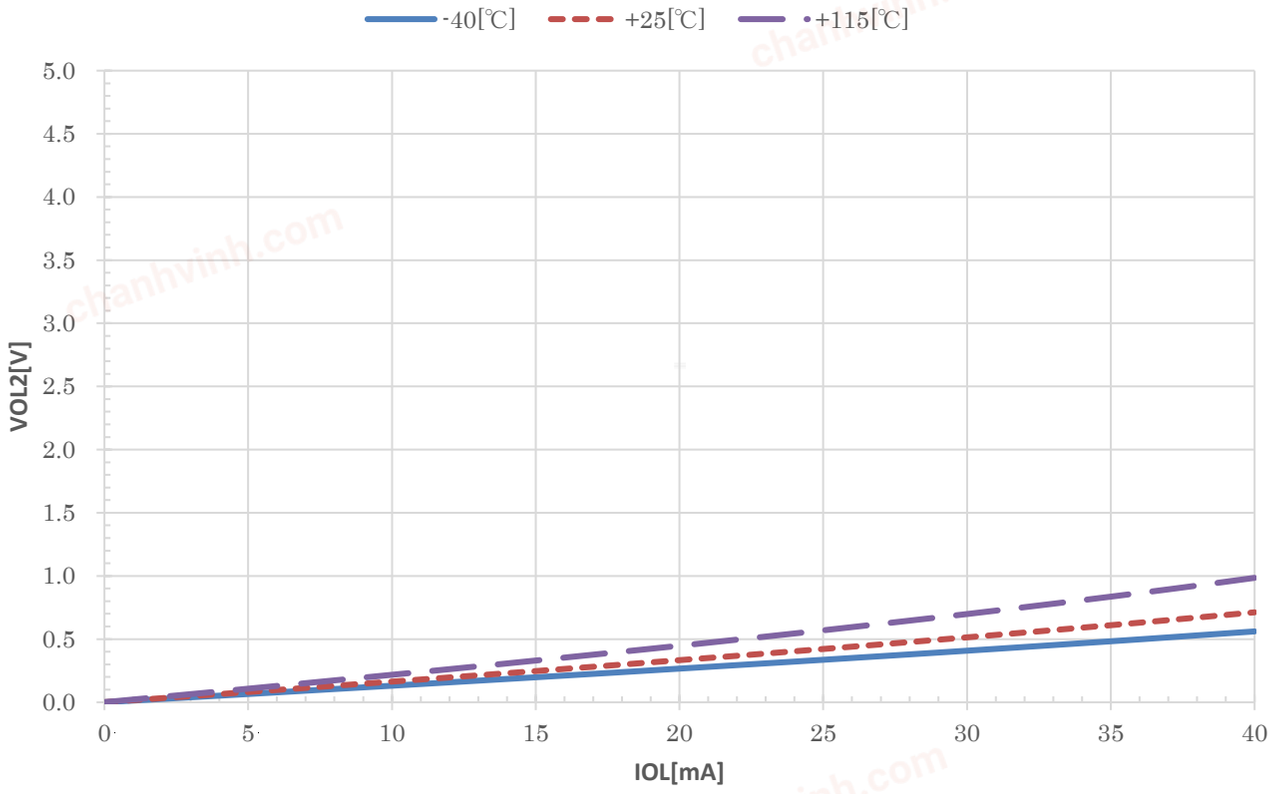
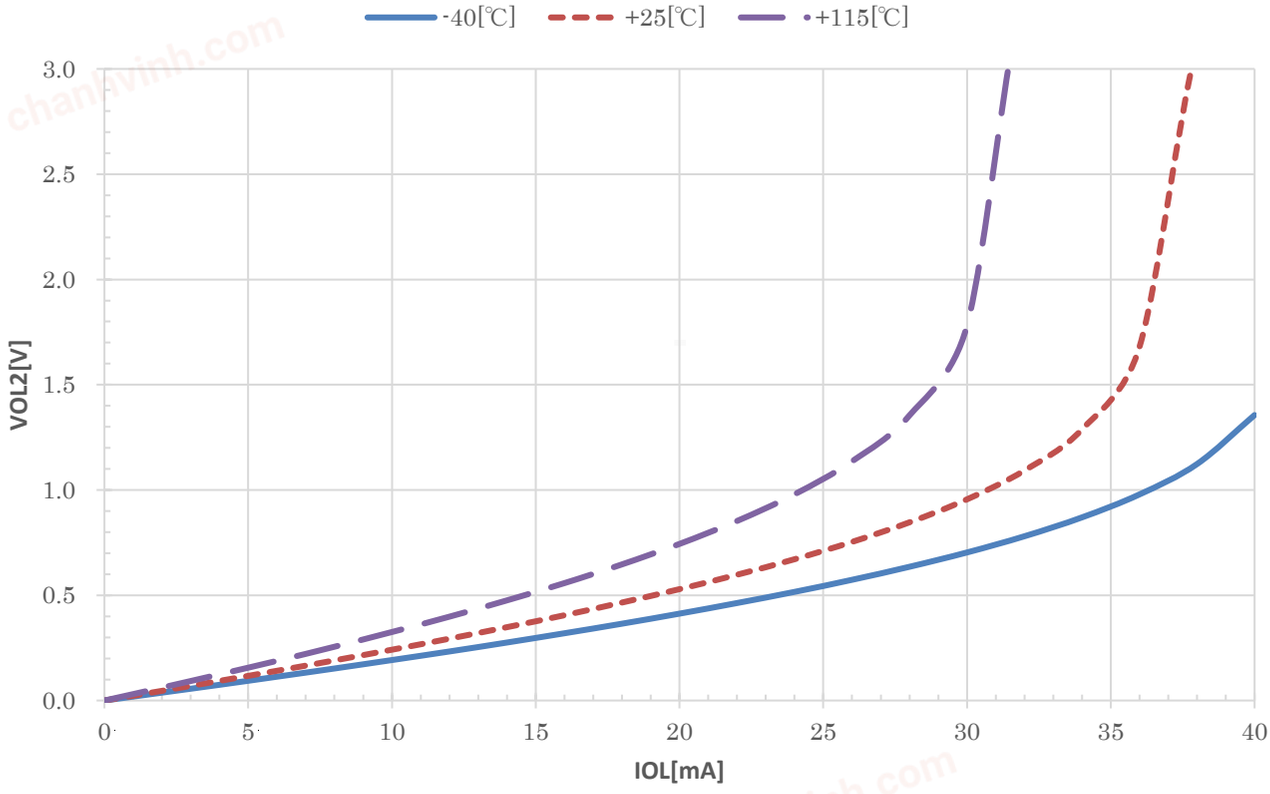
– VOL2 vs IOL (VDD=5V TYP.)



– VOL2 vs IOL (VDD=3V TYP.)



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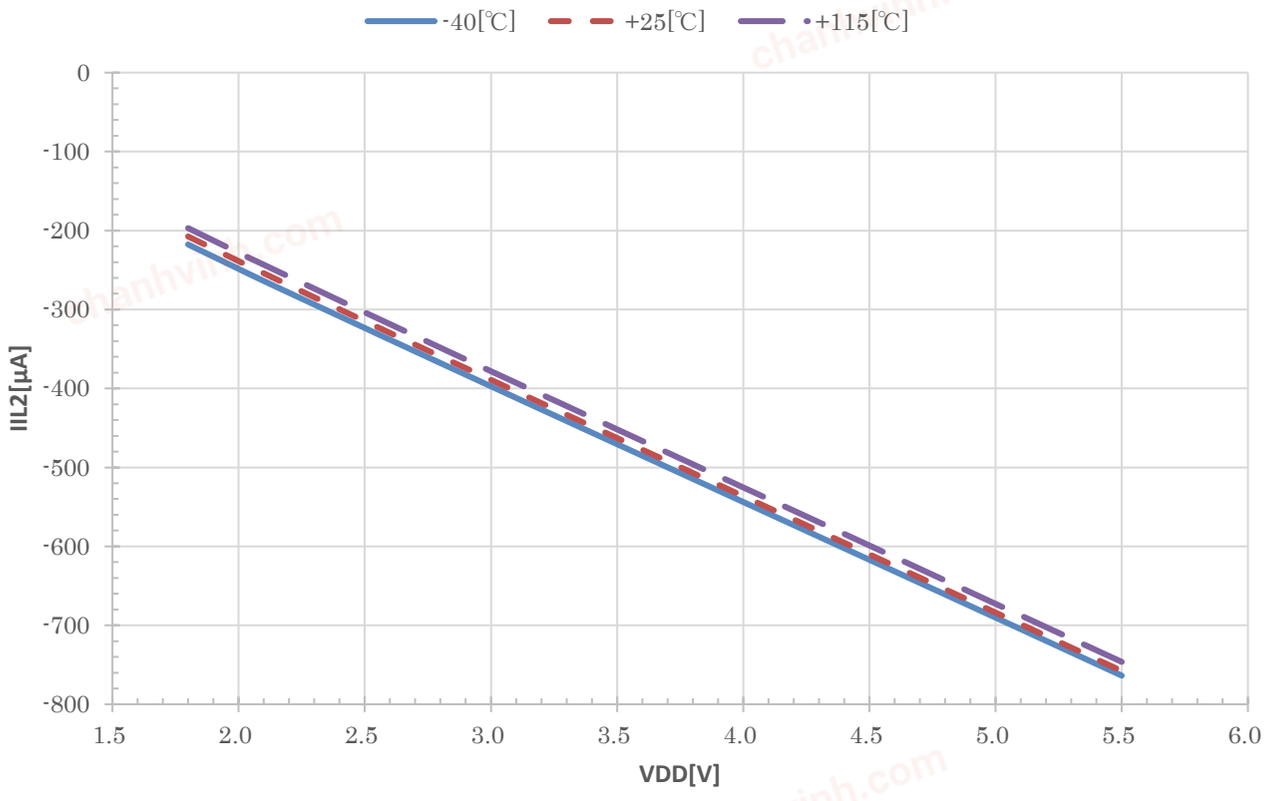
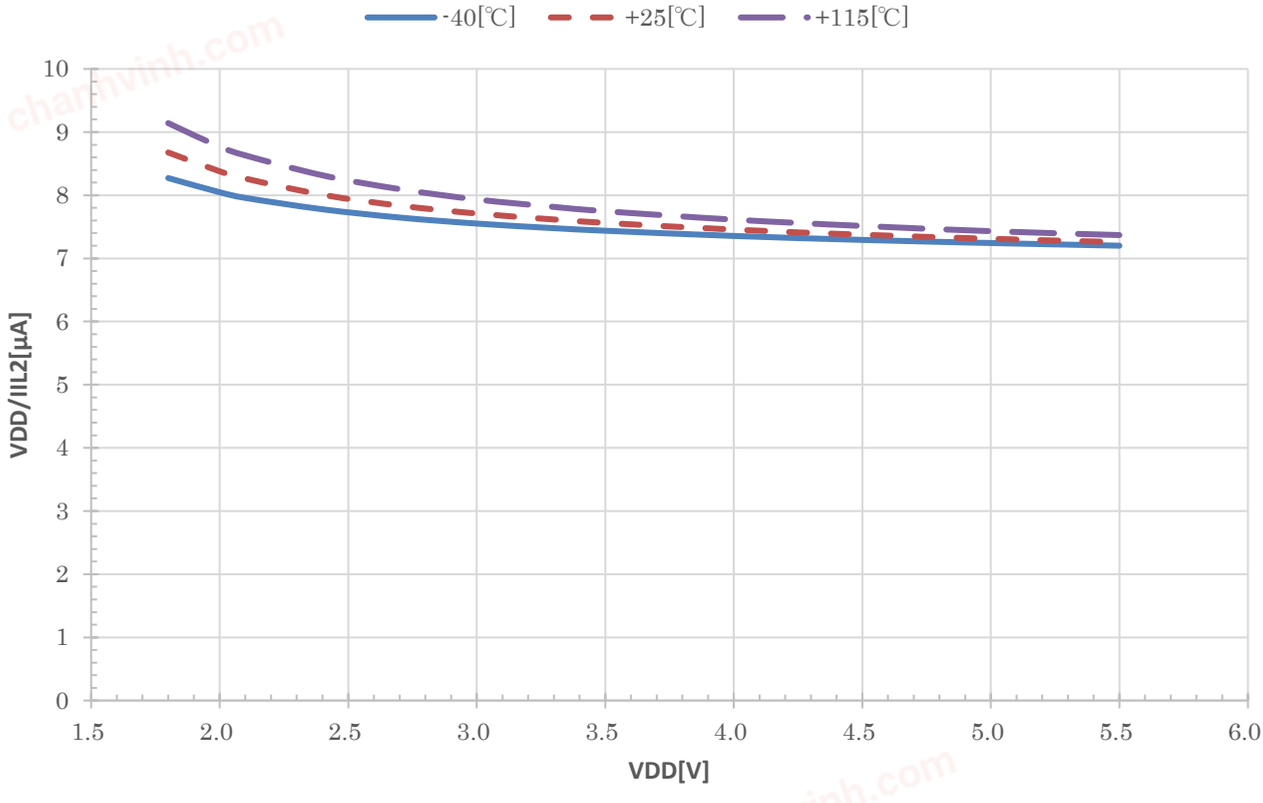
– IIL2 vs VDD (TYP. VIL=VSS)



– VDD/IIL2 vs VDD (TYP. VIL=VSS)



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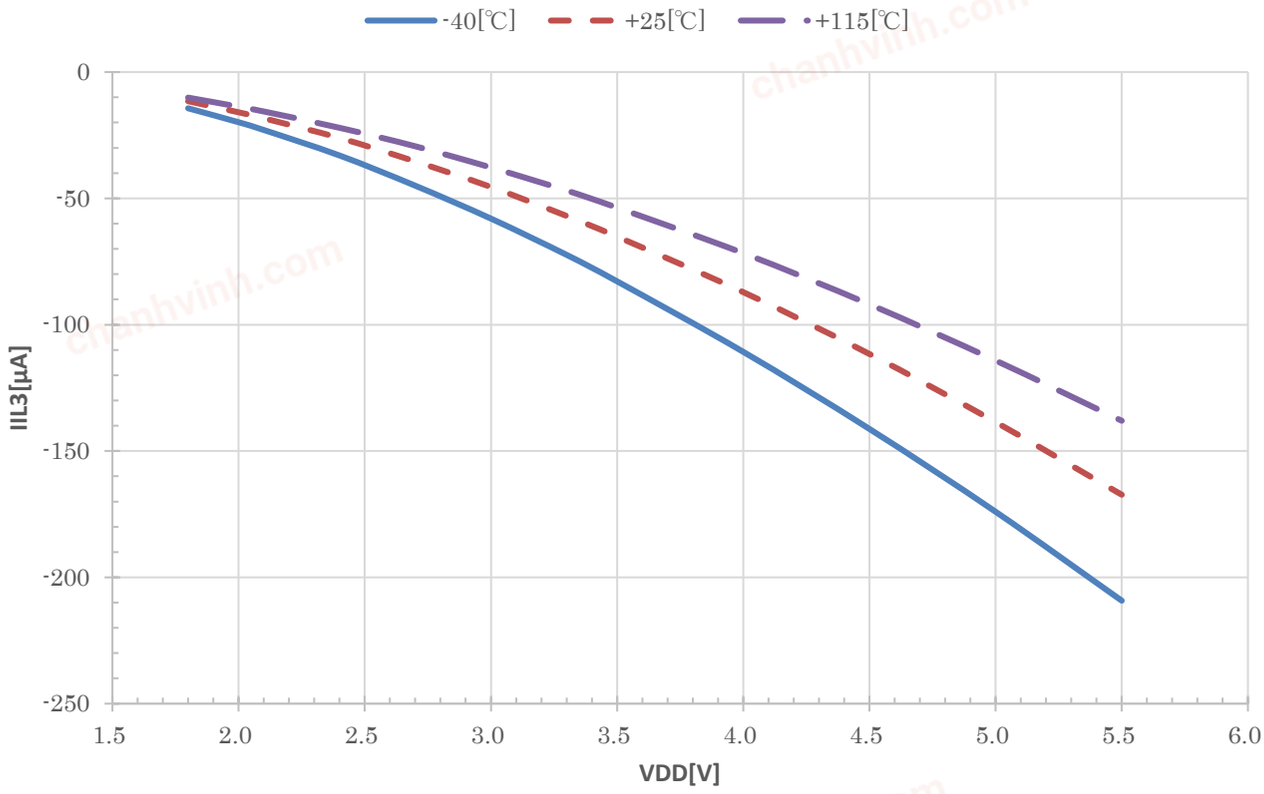
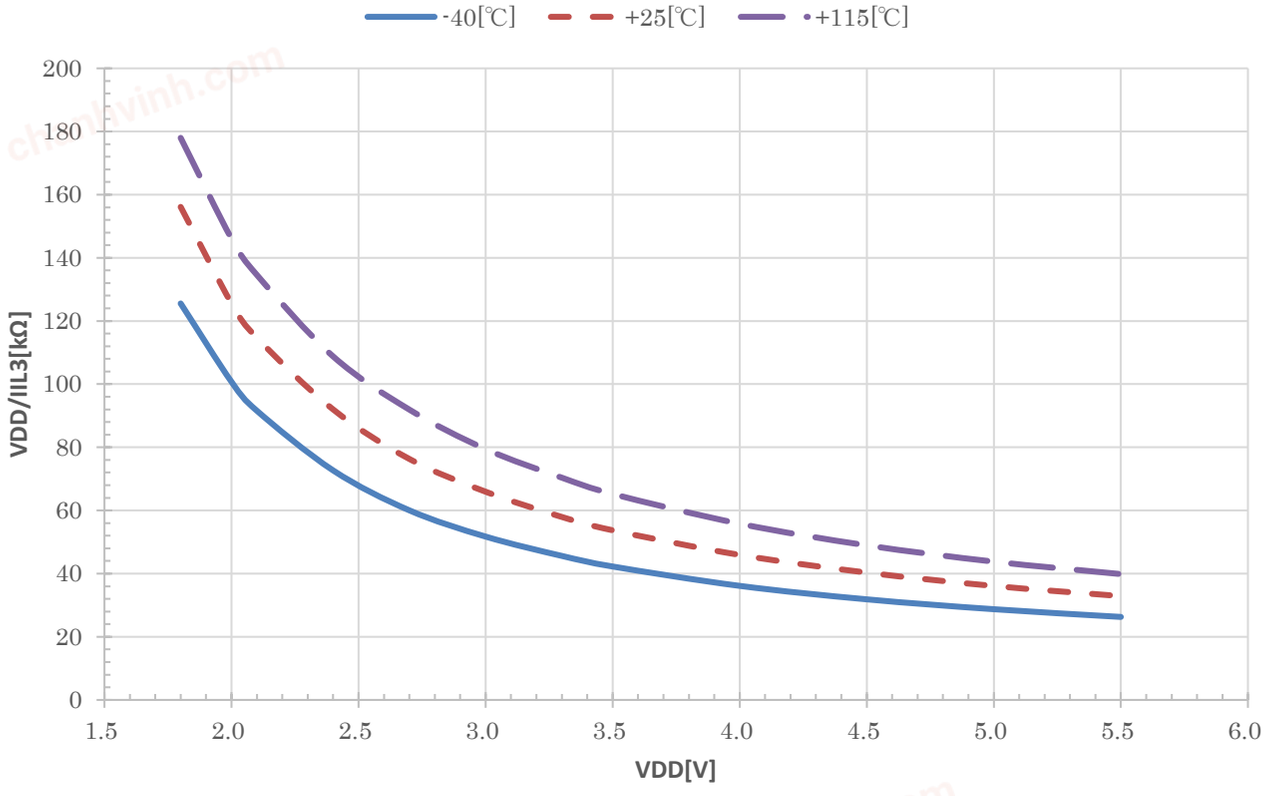
– IIL3 vs VDD (TYP. VIL=VSS)



– VDD vs VDD/IIL3 (TYP. VIL=VSS)



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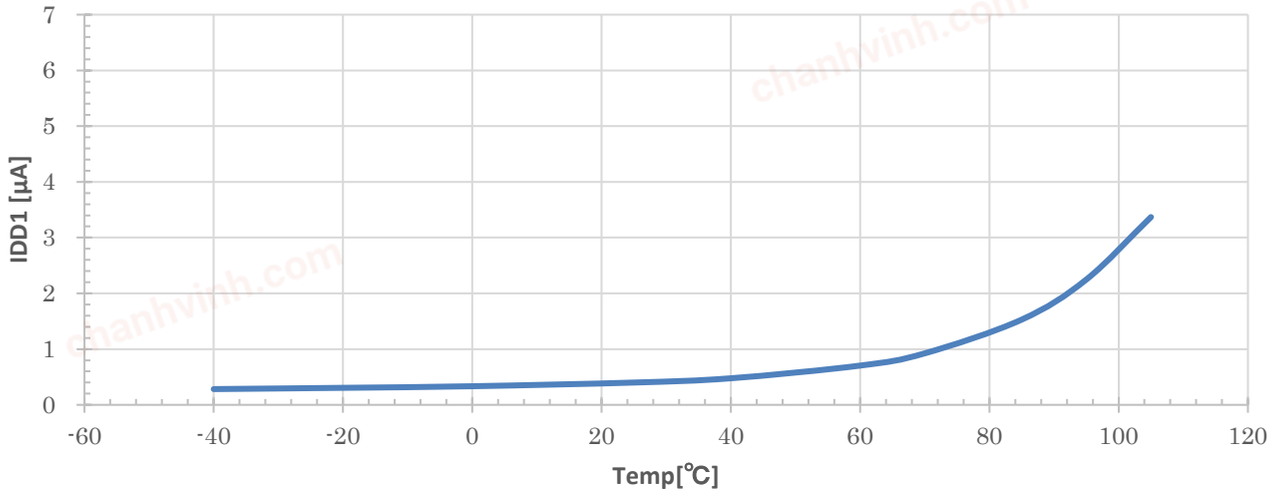
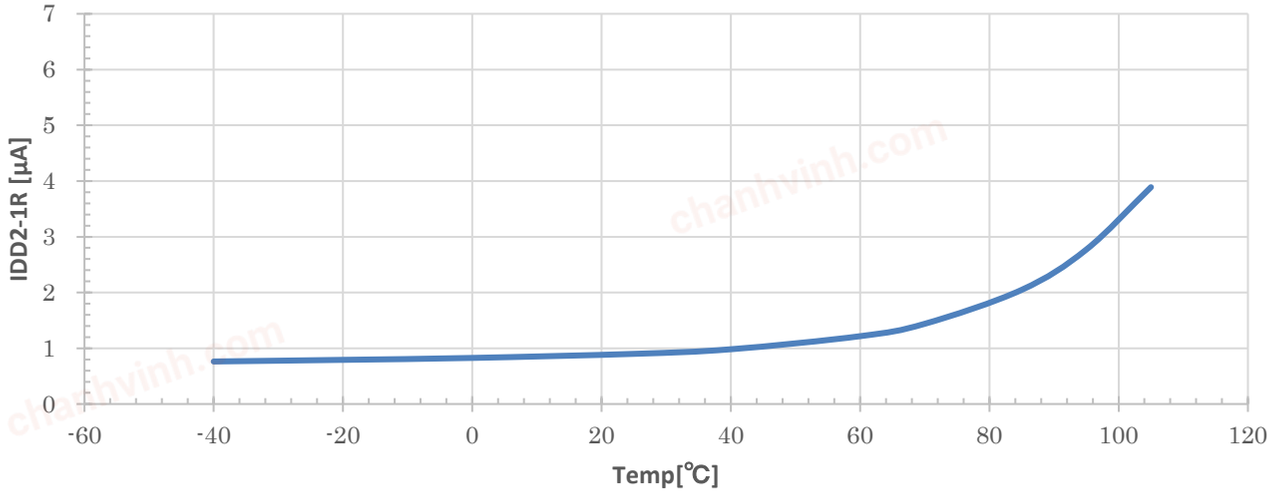
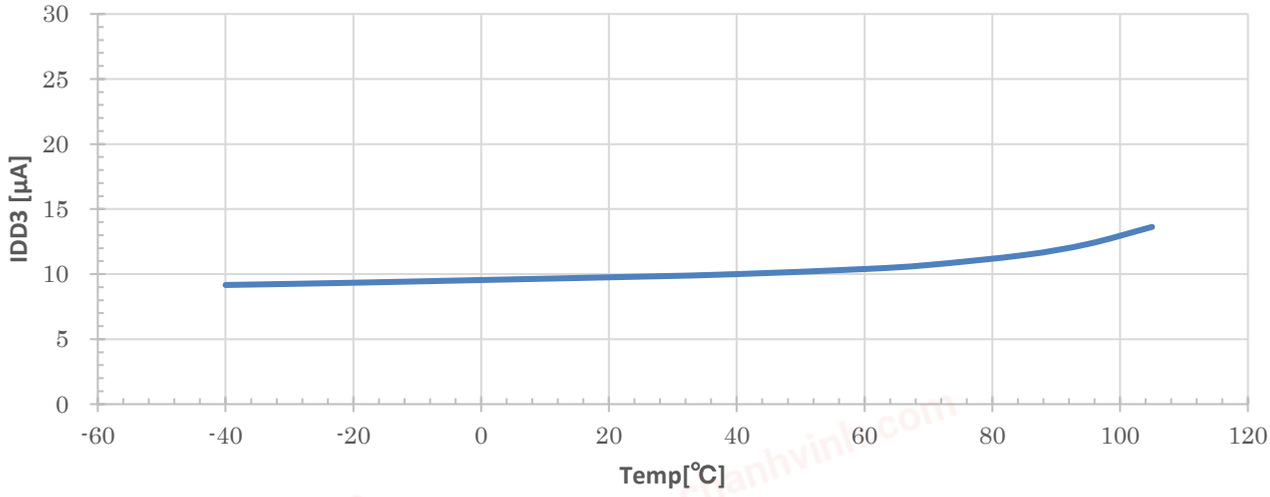
– IDD1 vs Temp (V_{DD}=3.0V)



– IDD2-1R vs Temp (V_{DD}=3.0V)



– IDD3 vs Temp (V_{DD}=3.0V)



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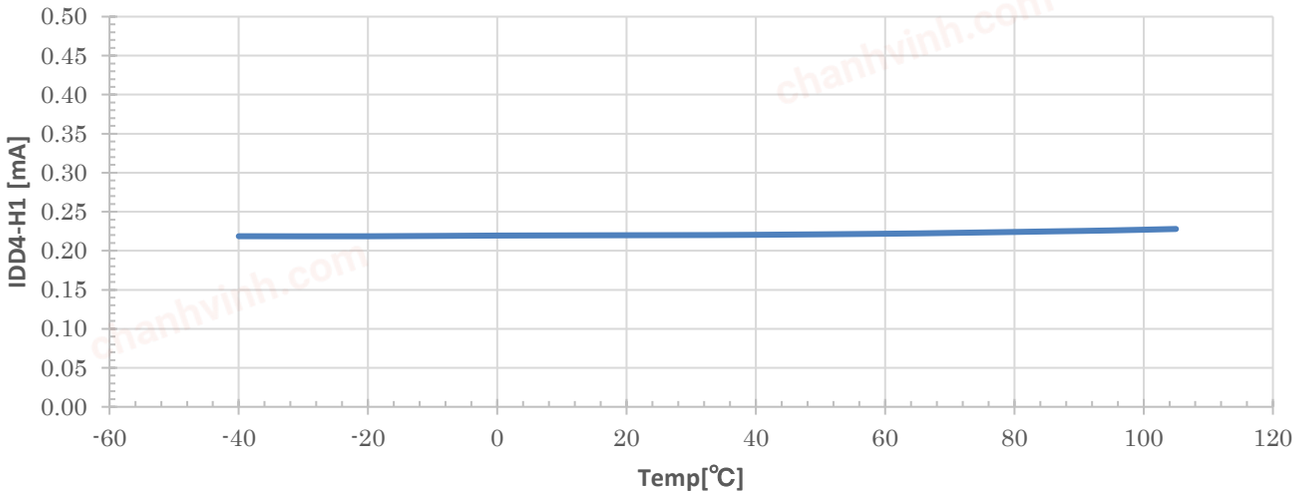
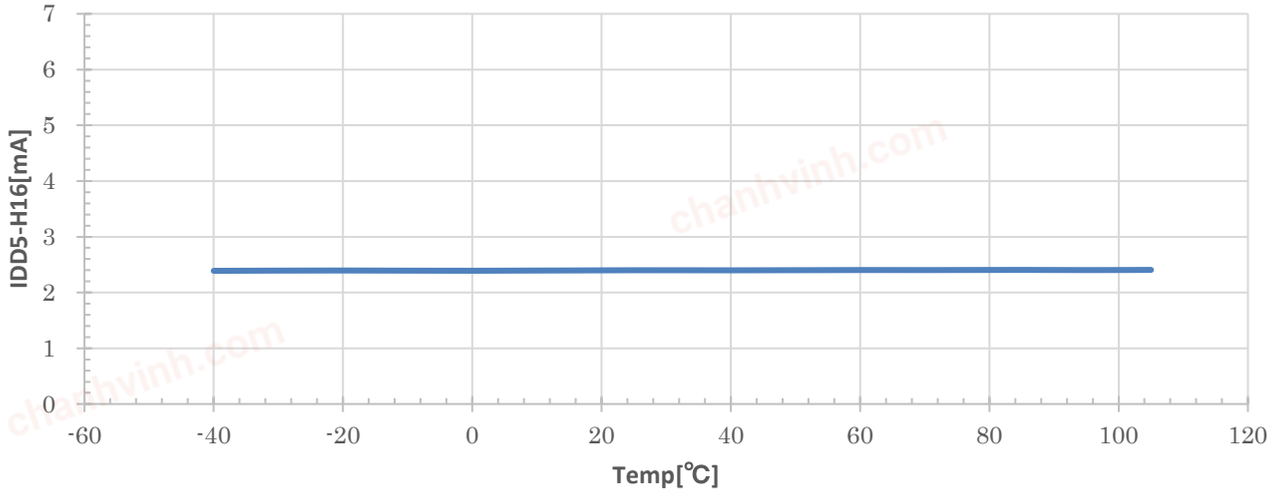
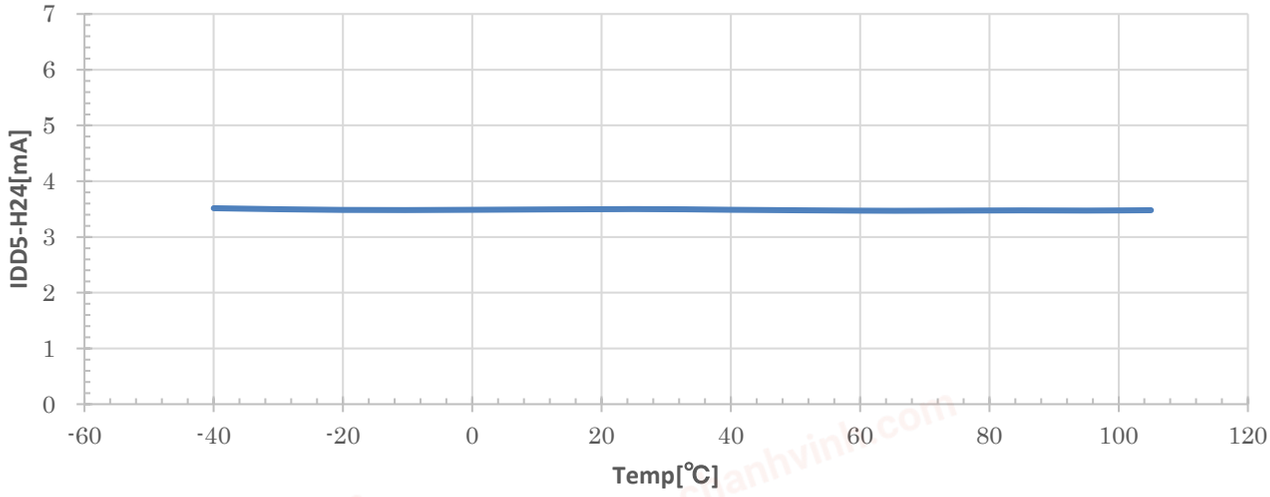
– IDD4-H1 vs Temp (V_{DD}=3.0V)



– IDD5-H16 vs Temp (V_{DD}=3.0V)



– IDD5-H24 vs Temp (V_{DD}=3.0V)



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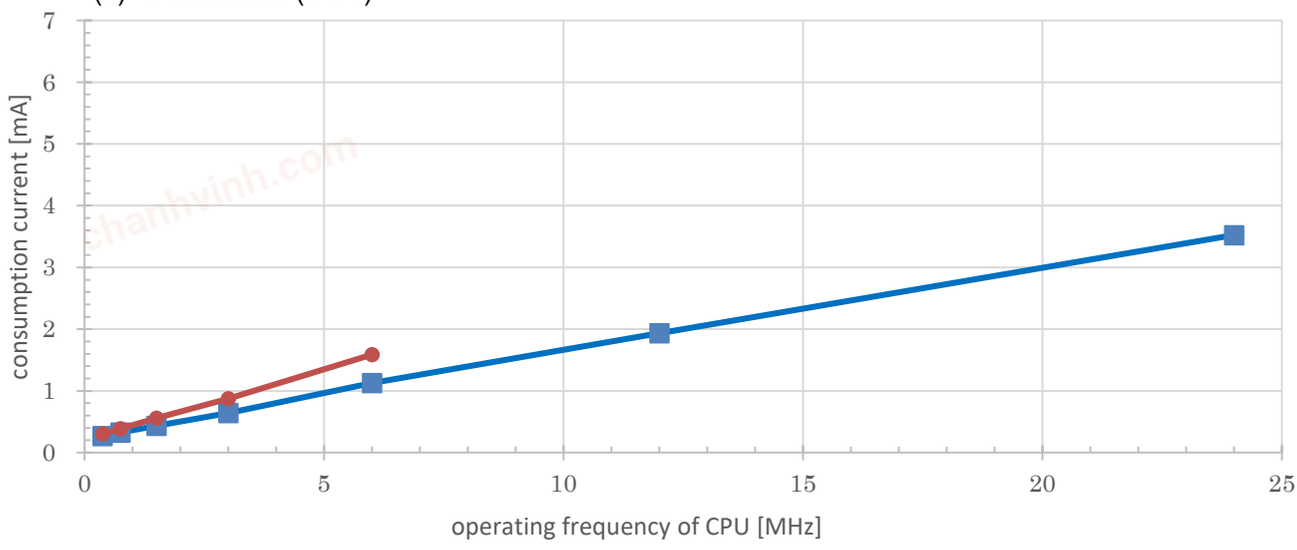
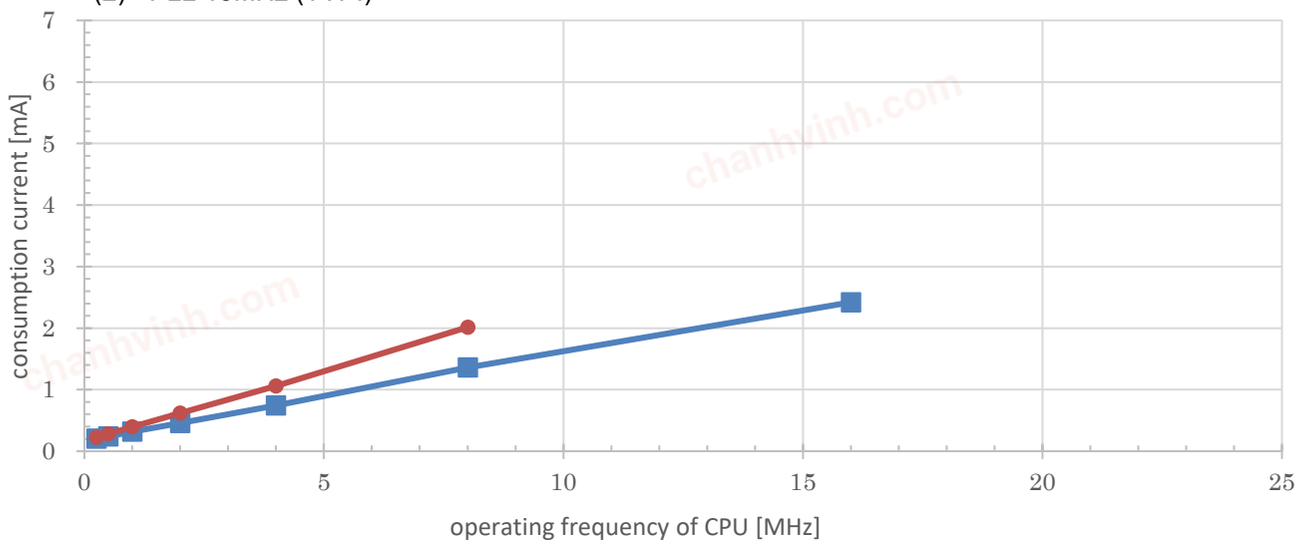
– Current consumption vs operating frequency of CPU
(VDD=3.0V, temp=+25°C, Stop the clock supply to peripherals.)

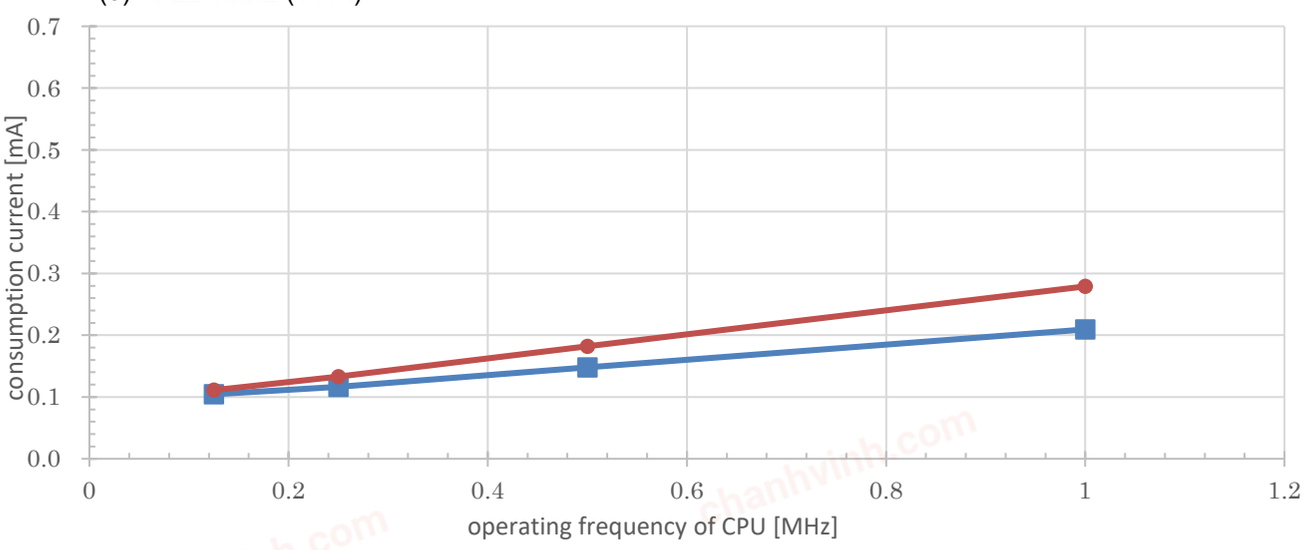
(1) PLL 24MHz (TYP.)



(2) PLL 16MHz (TYP.)



(3) PLL 1MHz (TYP.)



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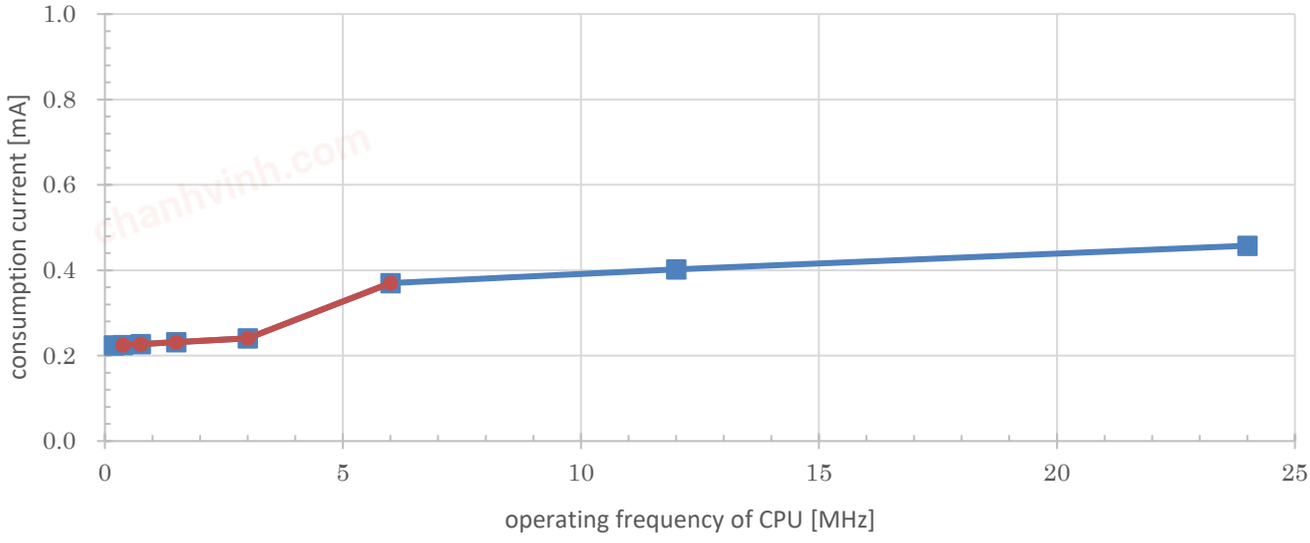
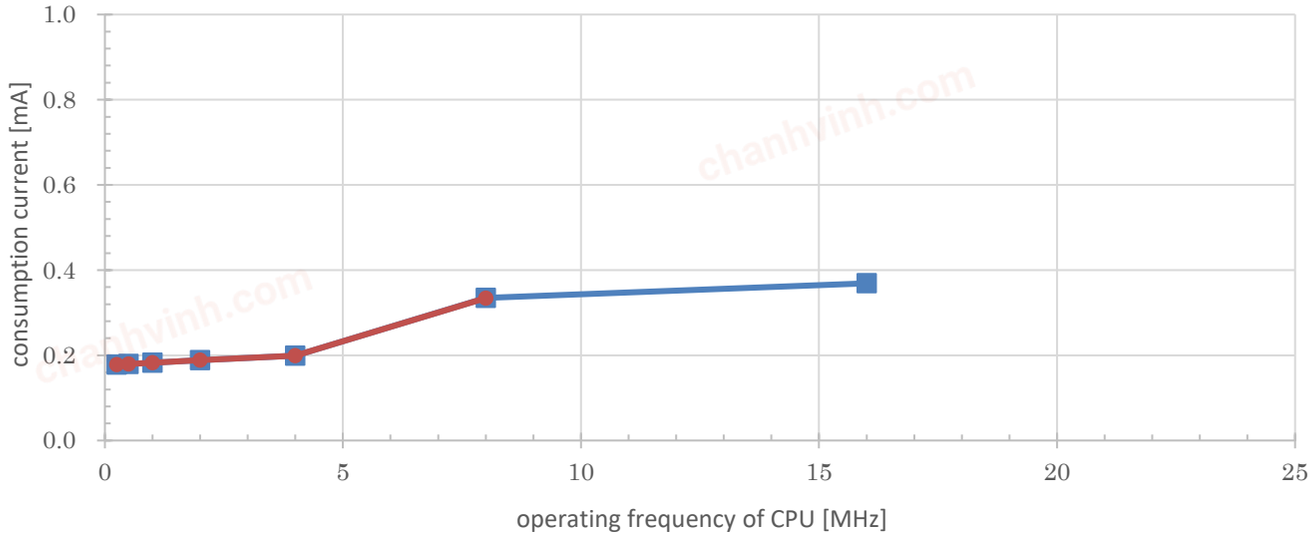
– Current consumption of halt vs operating frequency of CPU
(VDD=3.0V, temp=+25°C, Stop the clock supply to peripherals.)

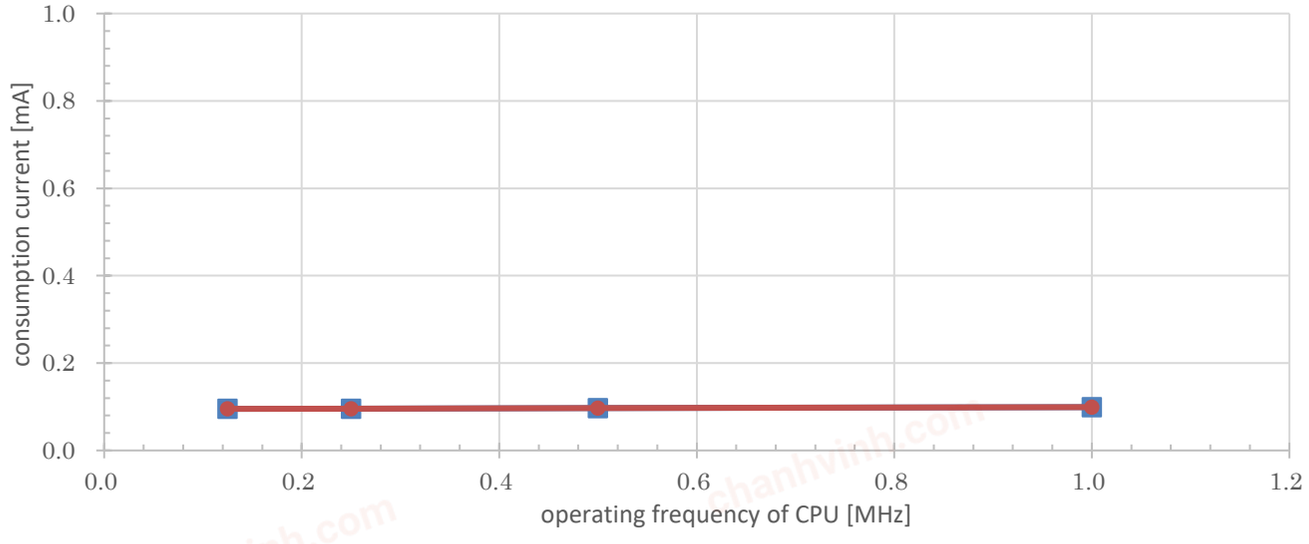
(1) PLL 24MHz (TYP.)



(2) PLL 16MHz (TYP.)



(3) PLL 1MHz (TYP.)



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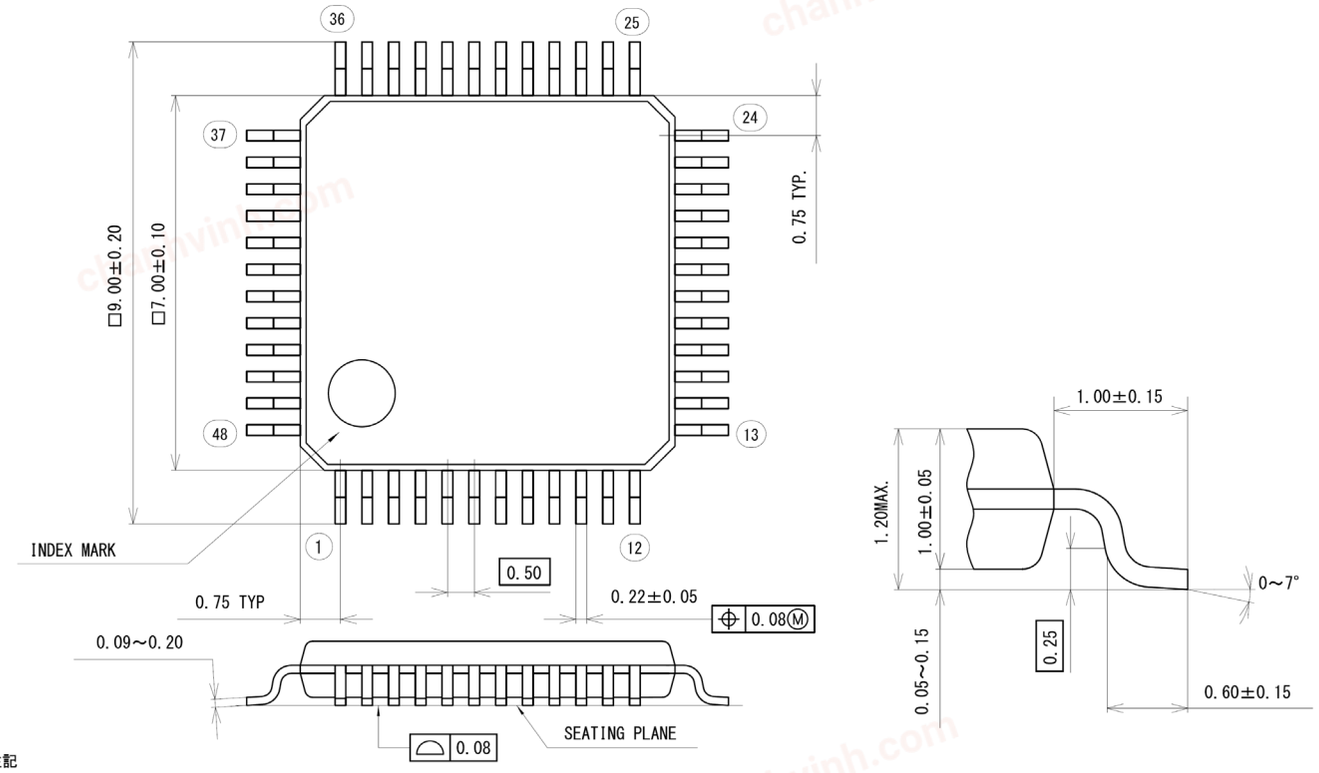
PACKAGE DIMENSIONS

48pin TQFP Package



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
   又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
   パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69142
LEAD FINISH	Sn 100%	REVISION	4
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.13TYP	REVISED	Oct/12/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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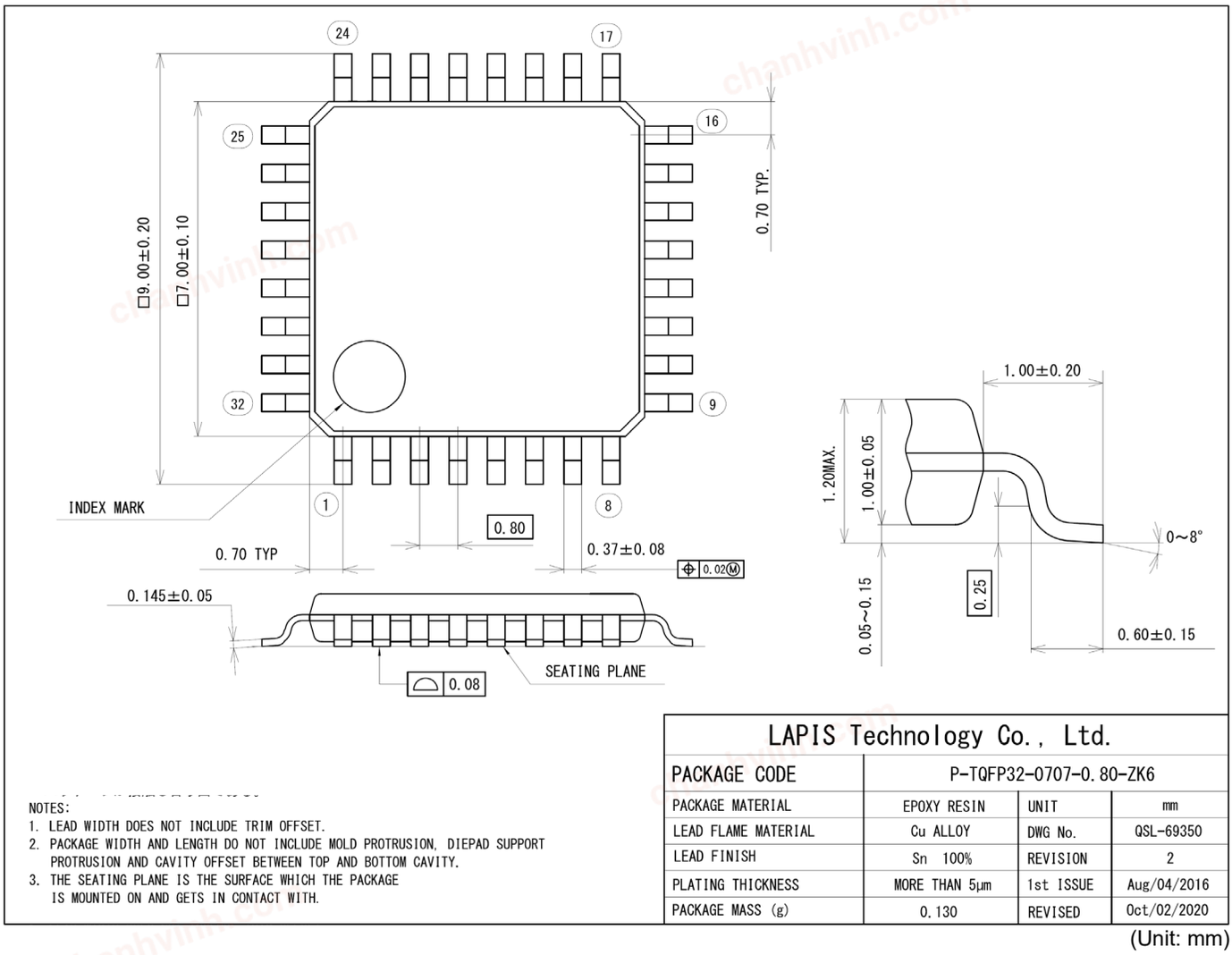
32pin TQFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP32-0707-0.80-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69350
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Aug/04/2016
PACKAGE MASS (g)	0.130	REVISED	Oct/02/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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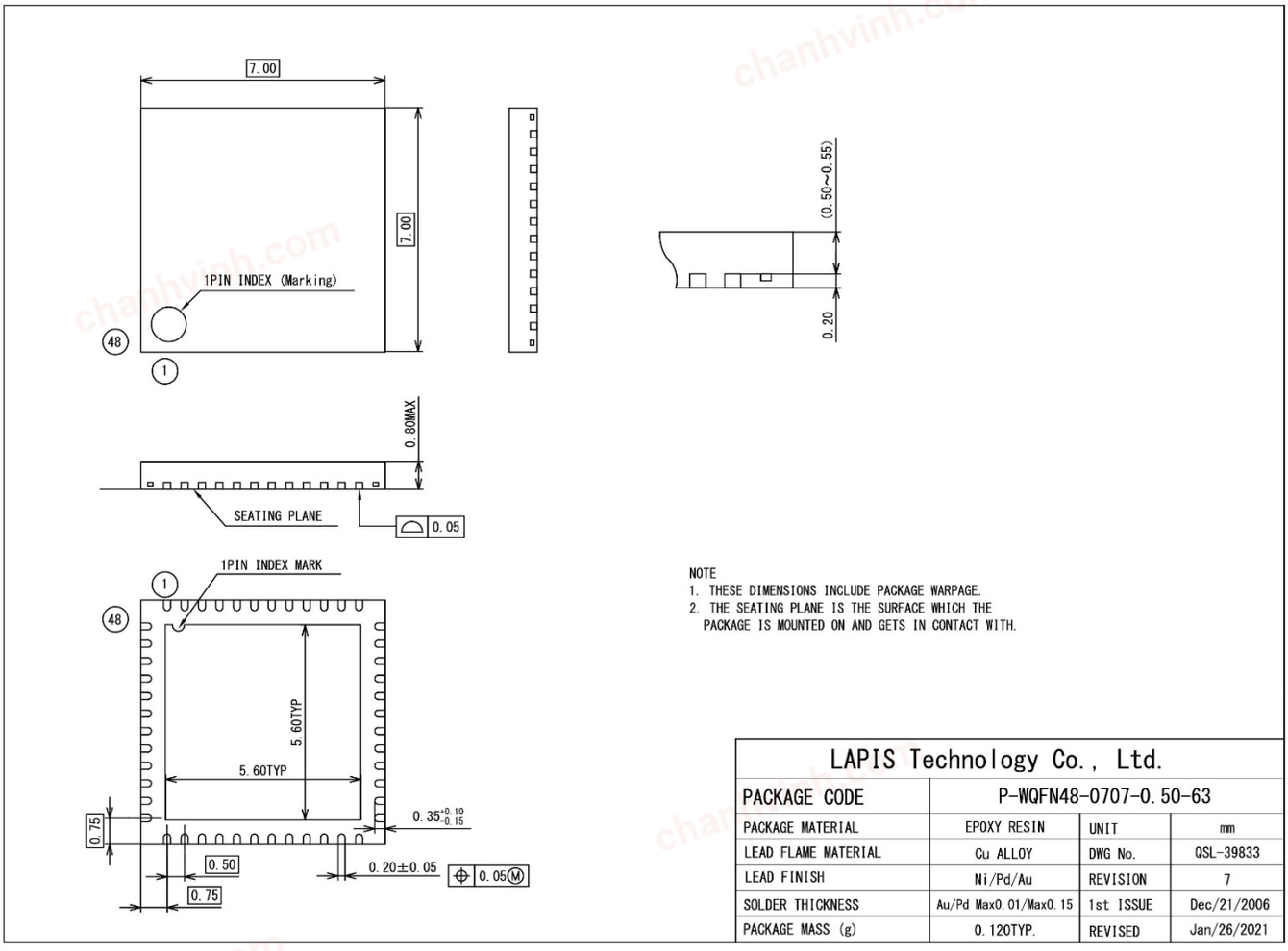
48pin WQFN Package



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN48-0707-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-39833
LEAD FINISH	Ni/Pd/Au	REVISION	7
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Dec/21/2006
PACKAGE MASS (g)	0.120TYP.	REVISED	Jan/26/2021

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

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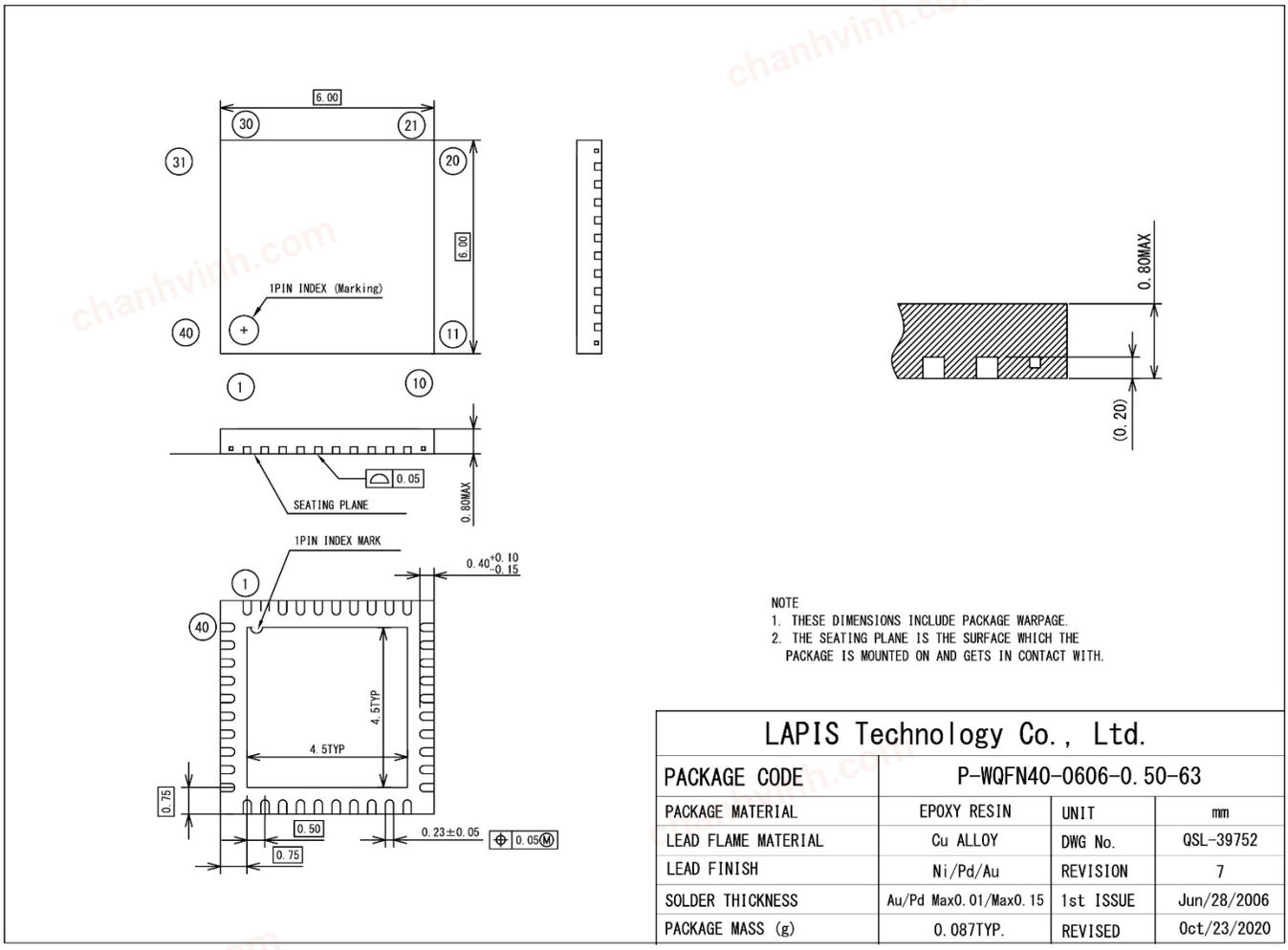
40pin WQFN Package



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN40-0606-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-39752
LEAD FINISH	Ni/Pd/Au	REVISION	7
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Jun/28/2006
PACKAGE MASS (g)	0.087TYP.	REVISED	Oct/23/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

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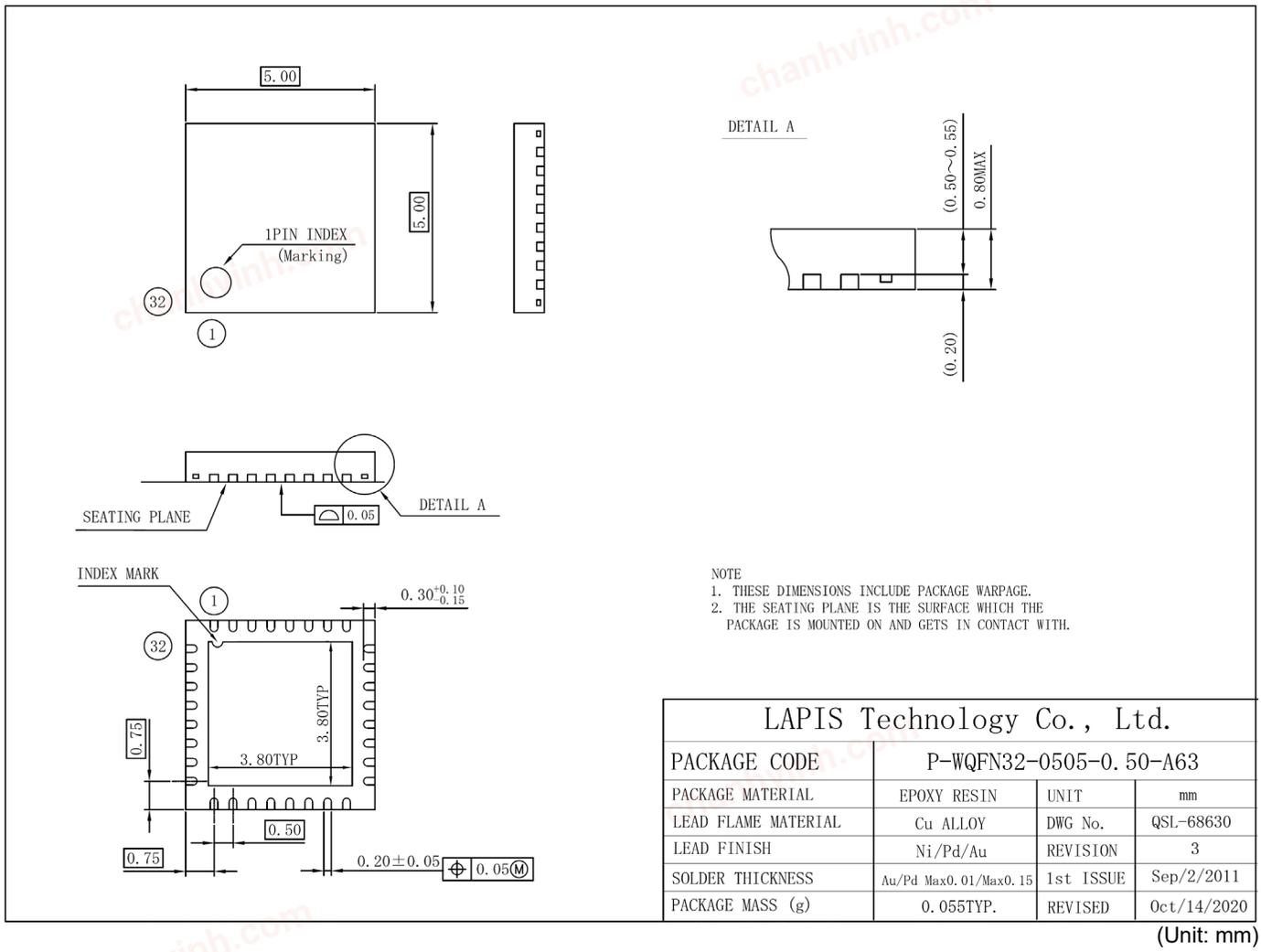
32pin WQFN Package



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN32-0505-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68630
LEAD FINISH	Ni/Pd/Au	REVISION	3
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/2/2011
PACKAGE MASS (g)	0.055TYP.	REVISED	Oct/14/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL62Q2500-01	Oct. 20, 2022	-	-	1st Edition
FEDL62Q2500-02	Nov.9, 2022	-	-	Corrected typo, corrected appearance
FEDL62Q2500-03	Feb.2, 2023	19	19	Corrected typo, HSCLK condition of IDD4-H16
		19	19	New addition of Tj≤+95°C specification of IDD3, IDD4-H1, IDD4-H16, IDD5-H16 and IDD5-H24
FEDL62Q2500-04	Mar.26, 2024	1	1	Updated Shipping package table
		4	4	Corrected UART baud rates
		4	4	Updated Shipping package table
		5	5	Updated “How To Read The Part Number”
		-	34 to 43	Added “Characteristics graphs”
		40	51	Revised the Note

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Notes for product usage

Notes on this page are applicable to the all LAPIS Technology microcontroller products.
For individual notes on each LAPIS Technology microcontroller product, refer to [Note] in the chapters of each user's manual.
The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS
   Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON
   At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.
   On LAPIS Technology microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.
   Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY
   If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCT
   Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.
   When replacing from other product to LAPIS Technology microcontroller products, please evaluate enough the apparatus/system which implemented LAPIS Technology microcontroller products.

5. USE ENVIRONMENT
   When using LAPIS Technology microcontroller products in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

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Notes

1) When using LAPIS Technology Products, refer to the latest product information and ensure that usage conditions (absolute maximum ratings*1, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures.
*1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

2) The Products specified in this document are not designed to be radiation tolerant.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

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