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FEDL62Q2045-02
Issue Date: May 24, 2024

ML62Q2033/2035/2043/2045

16-bit micro controller

GENERAL DESCRIPTION

ML62Q2033/2035/2043/2045 are high performance CMOS 16-bit microcontrollers equipped with an 16-bit CPU nX-U16/100 and integrated with program memory (Flash memory), data memory (RAM), data Flash (Erase unit:128byte, Write unit:1byte) and rich peripheral functions such as the multiplier/divider, Clock generator, PWM generator, Timer, General Purpose Ports, UART, I2C bus interface unit(Master, Slave), Successive approximation type 12bit A/D converter, 8bit D/A converter, PGA (Programable Gain Amp) and so on.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP (In-System Programming) function supports the Flash programming in production line.

- Applications

  Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc)

  Note:
  This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems.
  Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equipment, power transmission systems, core systems for financial terminals and various safety control devices.

- Product list

  Table1 shows the conbination of ML62Q2033/2035/2043/2045 memory variations and package type.

Table 1 Product List

Program memory	Data memory (RAM)	Data Flash	20pin TSSOP20	24pin WQFN24
32Kbyte	2Kbyte	4Kbyte	ML62Q2035	ML62Q2045
16Kbyte			ML62Q2033	ML62Q2043

Please see the last 2 pages “Notes for product usage” and “Notes” in this document on use with this product.

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FEATURES

- CPU
  - 16-bit RISC CPU : nX-U16/100 (A35 core)
  - Instruction system : 16-bit length instructions
  - Instruction set : Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack, manipulations, arithmetic shift, and so on
  - Built-in On-chip debug function (connect to the ROHM on-chip debug emulator)
  - Minimum instruction execution time : 1 count of system clock
    Approximately 30.5µs/62.5ns (at 32.768kHz/16MHz system clock)

- Coprocessor for multiplication and division
  - Signed or Unsigned is selectable

Parameter	Expression	Operation time [cycle]
Multiplication	16bit × 16bit	4
Division	32bit ÷ 16bit	8
	32bit ÷ 32bit	16
Multiply-accumulate (non-saturating, non-saturating)	16bit × 16bit + 32bit	4

- Operating voltage and temperature
  - Operating voltage : V_{DD} = 4.5 to 5.5V
  - Operating temperature : -40°C to +105°C

- Flash memory

Parameter	Program memory area	Data Flash memory area
Erase/Write count	100cycles	10,000cycles
Write unit	16bit (2byte)	8bit (1byte)
Erase unit	16Kbyte/1Kbyte	all area/128byte
Erase/Write temperature (Ta)	0°C to +40°C	-40°C to +85°C

  - Background Operation (CPU can work while erasing and rewriting to the Data Flash memory area.)
  - The built-in on-chip debug function and ISP (In-System Programming) function enable Flash programming

    This product uses Super Flash® technology licensed from Silicon Storage Technology, Inc.
    Super Flash® is a registered trademark of Silicon Storage Technology, Inc.

- Data RAM area
  - Rewrite unit: 8bit/16bit (1byte/2byte)
  - Parity check function is available (interrupt or reset is generatable at Parity error)

- Clock generation circuit
  - Low-speed clock (LSCLK0)
    Internal low-speed RC oscillation (RC32K) : Approx. 32.768kHz
  - High-speed source clock (HSOCLK) : Available for PWM generation circuit clock
    PLL oscillation : 64MHz
  - High-speed system clock (HSCLK) : 16MHz, generated by dividing HSOCLK

- Reset
  - System Resets by reset input pin, Power-On Reset, Low Level Detector (LLD) reset, Watchdog timer (WDT) overflow, WDT invalid clear, RAM parity error reset, and Progran Counter error reset (instruction access to unused ROM area)
  - Software reset by BRK instruction (reset CPU only)
  - Reset the peripherals individually/collectively by software

- Power management
  - Two stand-by mode.
    - STOP mode (All clocks are stopped)
    - HALT mode (clocks for System are stopped)
  - Individual clock input control to the peripheral blocks by software
  - Clock gear: High-speed system clock frequency is changeable dynamically (1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of HSCLK)

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- Interrupt controller
  - Non-maskable interrupt source : 1 (Internal sources: WDT)
  - Maskable interrupt sources : 22 (included the external interrupt 4 sources)
  - Four step interrupt levels
  - External interrupt ports（EXI） : 4 (selectable from Max.8 pins) with sampling filter and edge(rise, fall, both) selection.

- General-purpose ports (GPIO)
  - I/O port : Max. 20 (Including pins for shared functions)
  - Carrier frequency output function (for IR communication)

- Watchdog timer (WDT) : 1 channel
  - Overflow period : 8selectable (7.8, 15.6, 31.3, 62.5, 125, 500, 2000, 8000ms)
  - Selectable window function (enable or disable): configurable clear enable period (50% or 75% of overflow period) with invalid clear. When disable, interrupts the first overflow and resets the second overflow. When enable, reset occurs for the first overflow.
  - Selectable WDT operation : select Enable or Disable by code option
  - Selectable operation during HALT mode (Continue counting/Stop counting)
  - WDT counter operation monitoring function (Readable WDT counter)

- Operational timer : 6 channels
  - Various modes (Continuous, One shot, capture, and PWM mode)
  - Event trigger (external terminal, 16bit timer, operational timer, comparator) input is available
  - Selectable counter clock from various sources (LSCLK0, HSCLK(16MHz), HSOCLK(64MHz), divided by 1 to 8 of external pin input)
  - Logic AND output with several channel output (Operational timer output, comparator output, and external pin input) is available

- 16-bit General timers : 1 channel
  - Selectable counter clock from various sources (LSCLK, HSCLK (16MHz), and external clock divided by 1 to 8)

- UART (Half-duplex/Full-duplex communication mode): 2 channels
  Selectable from 5 to 8bit length, parity or no parity, odd parity or even parity, 1 stop bit or 2 stop bits, Positive logic or Negative logic, LSB first or MSB first
  - Sampling filter for receiving data and start bit
  - Built-in baud rate generator (HSCLK@16MHz: 300bps to 2Mbps, LSCLK: up to 2400bps)

- I^2C bus : 1 channel
  - Select from Master mode or Slave mode: 1channel. Master mode only: 1channel
  - Standard mode (100kbps), fast mode (400kbps) and 1Mbps mode (1Mbps)
  - 7bit address format
  - Master mode: Handshake (Clock synchronization), 10bit Master address format is supported
  - Slave mode: Clock stretch function,

- Successive approximation type 12bit A/D converter (SA-ADC) : input 5 channels
  - Conversion time: Min. 1.375μs / ch (When the conversion clock frequency is 16MHz)
  - Reference voltages (V_{ADCREF}) are selectable from VDD pin input voltage or Internal reference voltage (V_{ADCREF}, Approx. 2.5V)
  - Dedicated result register for each channel
  - Interrupt by Continuous conversion and Trigger start

- Programable-Gain-Amp (PGA) : 1 channel
  - Amplification factor : 4/ 8/16/ 32
  - Voltage input pin is selectable (AIN0/ AIN1/ AIN2/ AIN3)

- Analog comparator (CMP) : 3 channels
  - Selectable interrupt from the comparator output (rising edge or falling edge) and sampling
  - Selectable reference voltage ($V_{CMPREFn\ n=0\ to\ 2}$) from external pin input, internal reference voltage (0.8V) ($V_{CMPREFI}$), and D/A converter

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- D/A converter (DAC) : 2 channels
  - Resolution : 8 bit
  - Output impedance : 10kΩ (Typ.)
  - R-2R ladder type
  - Reference voltages (V_{DACREF}) are selectable from VDD pin input voltage or Internal reference voltage (0.8V) (V_{DACREF})

- Low Level Detector (LLD) : 1 channel
  - Reset generating
  - Sampling filter
  - Low power operation

- Safety Function
  - RAM/SFR guard
  - RAM parity error detection
  - ROM unused area access reset (instruction access)
  - WDT counter monitoring
  - SA-ADC test
  - Communication loop back test (UART, I^2C bus(master))
  - GPIO test

- Shipping package

Package	Body size (including lead) [mm × mm]	Pin pitch [mm]	Packing form and Product name	
			Tray	Tape & Reel
20 pin plastic TSSOP	6.5 × 4.4 (6.5 × 6.4)	0.65	ML62Q2033-xxxTDZWARZ ML62Q2035-xxxTDZWARZ	ML62Q2033-xxxTDZWATZ ML62Q2035-xxxTDZWATZ
24 pin plastic WQFN	4.0 × 4.0 (-)	0.50	ML62Q2043-xxxGDZW5AY ML62Q2045-xxxGDZW5AY	ML62Q2043-xxxGDZW5BY ML62Q2045-xxxGDZW5BY

xxx: ROM code number, (NNN: ROM code is blank)

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How To Read The Part Number

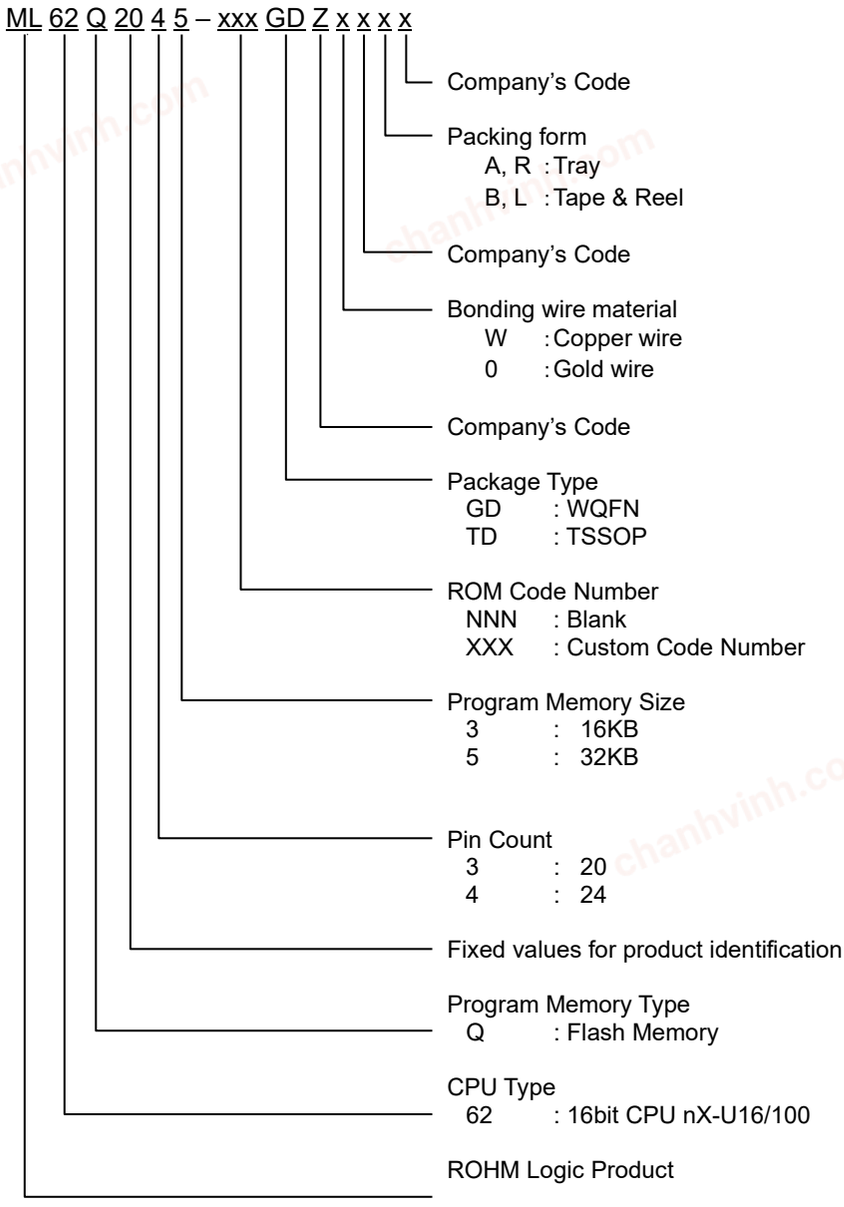


Figure 1 Part Number

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Main Function List

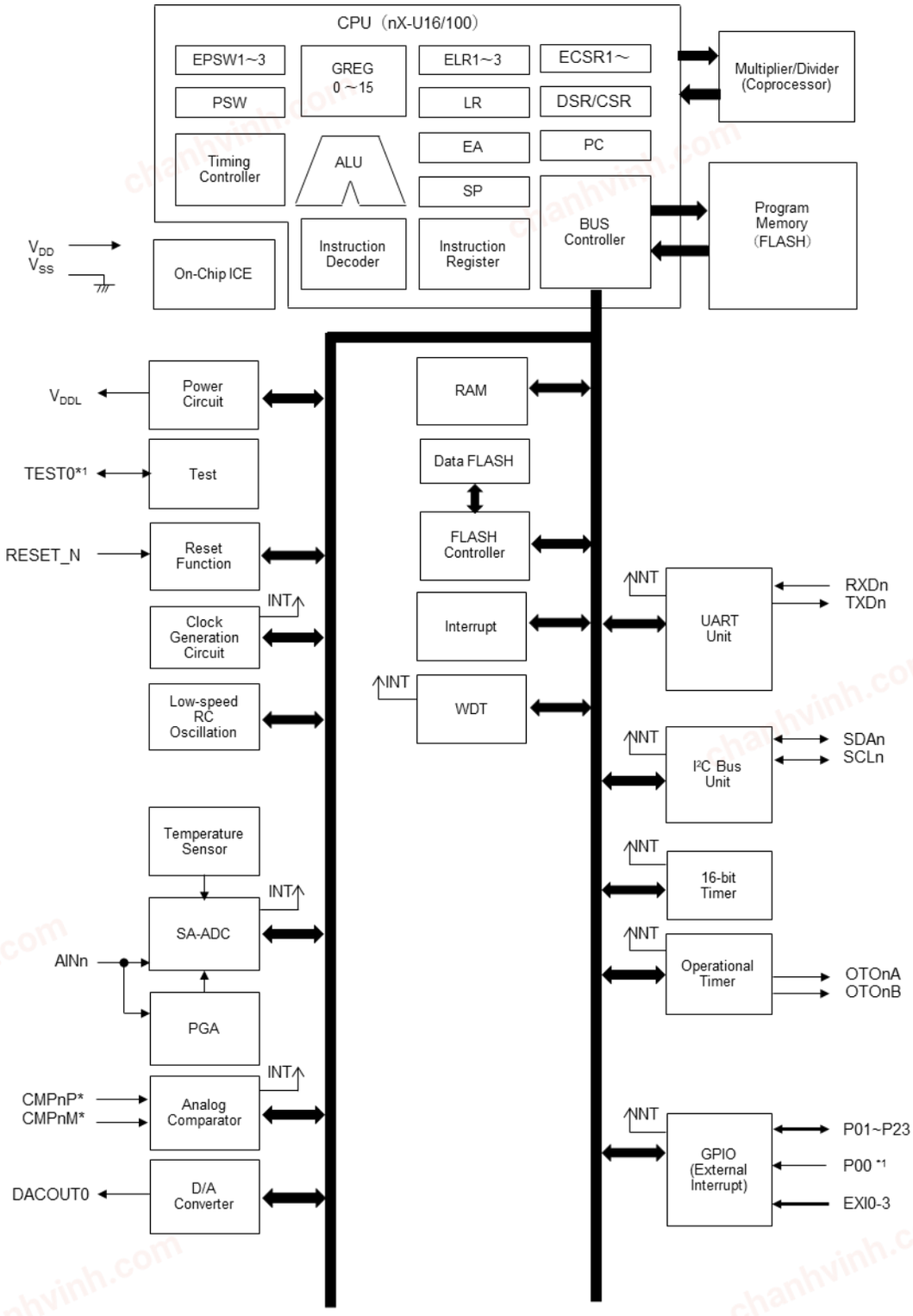
Table 2 Main Function List

Part number	Pin						Interrupt			Timer				Communication		Analog			
	Total pin	Power pin	Reset Input pin	General purpose I/O pin*1	General purpose I/O pin (LED drive is supported)	External interrupt pin	External interrupt source	Non maskable interrupt source	Internal maskable interrupt source	16bit Timer [ch]	16bit oprational Timer [ch]	16bit operational Timer [Port]	Watchdog Timer [ch]	UART [ch]	I²C bus unit (Master / Slave) [ch]	12bit Successive type A/D converter [ch]	Analog Comparator [ch]	D/A converter [dh]	PGA [ch]
ML62Q2033	20	3	1	1	15	8	4	1	18	1	6	10	1	2	1	5	3	2	1
ML62Q2035																			
ML62Q2043	24				19							13							
ML62Q2045																			

*1: Shared with pins debug input.

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BLOCK DIAGRAM

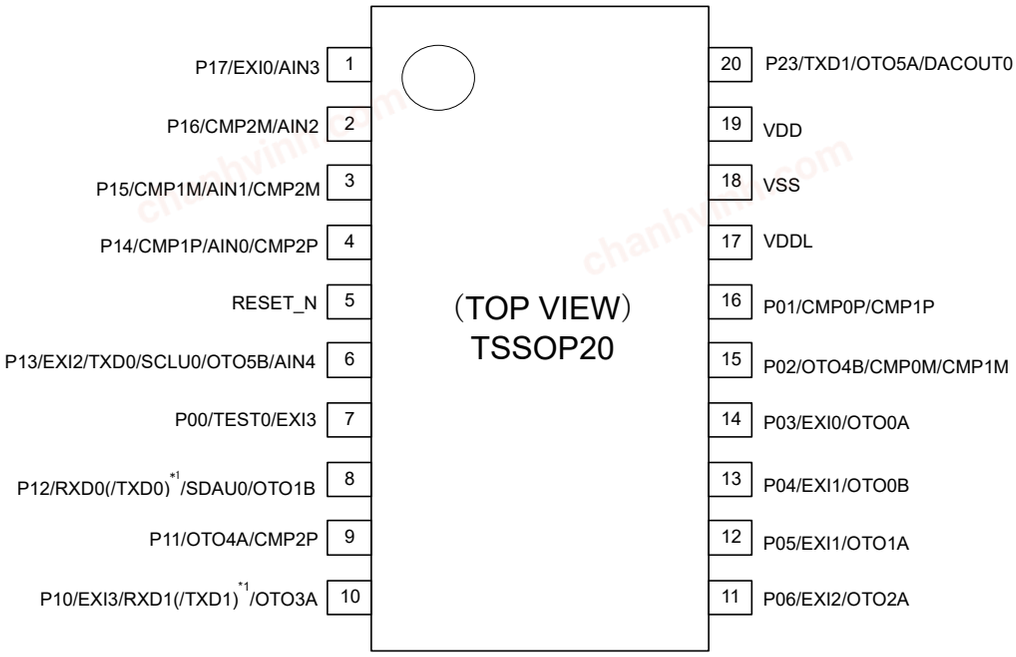


*1 : Not available as the input port when connecting to the on-chip debug emulator.

Figure 2 Block Diagram

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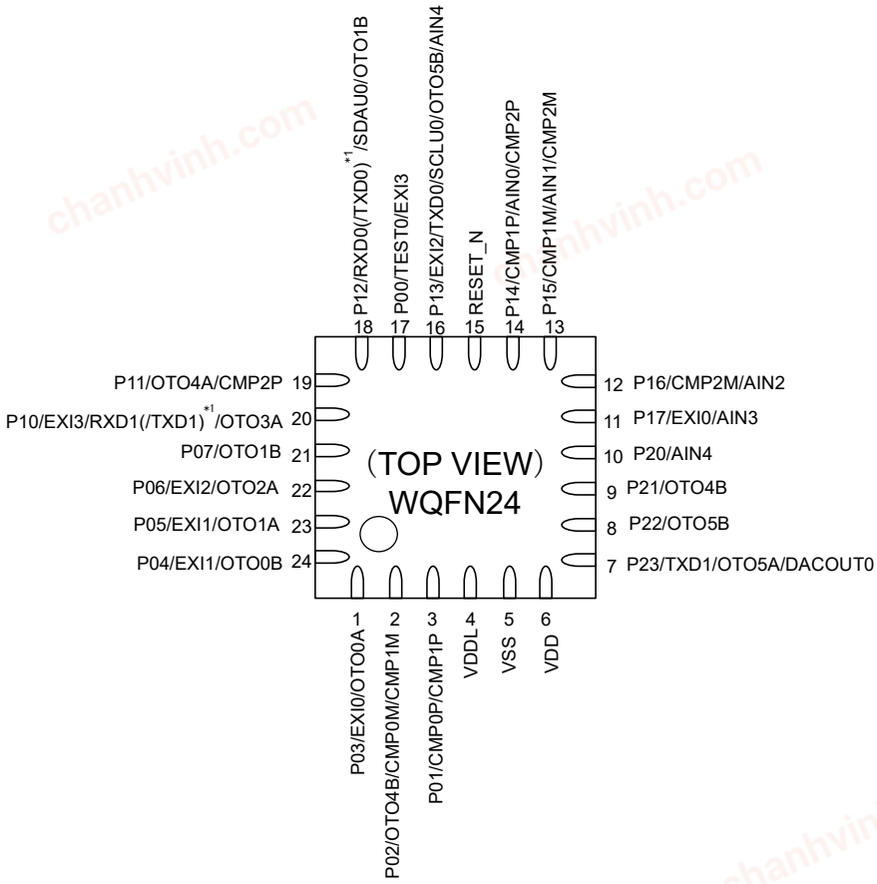
PIN CONFIGURATION



*1 : RXDn pin is shareable with TXDn pin by SFR setting

Fig.3-1 20 pin TSSOP

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DIE PAD = NC

*1 : RXDn pin is shareable with TXDn pin by SFR setting

Fig.3-2 24 pin WQFN

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PIN LIST

Table 3 Pin List

Pin No.		Pin name	1st function	2nd function	3rd function	4th function	5th function	6th function	7th function	8th function
ML62Q203x	ML62Q204x		GPI/ EXI	UART*	I²C	OTM	CMP/DAC	ADC	CMP	CMP/ADC
19	6	VDD	-	-	-	-	-	-	-	-
18	5	VSS	-	-	-	-	-	-	-	-
17	4	VDDL	-	-	-	-	-	-	-	-
16	3	P01	-	-	-	-	CMP0P	-	CMP0P/ CMP1P	CMP0P
15	2	P02	-	-	-	OTO4B	CMP0M	-	CMP0M/ CMP1M	CMP0M
14	1	P03	EXI0	-	-	OTO0A	-	-	-	-
13	24	P04	EXI1	-	-	OTO0B	-	-	-	-
12	23	P05	EXI1	-	-	OTO1A	-	-	-	-
11	22	P06	EXI2	-	-	OTO2A	-	-	-	-
-	21	P07	-	-	-	OTO1B	-	-	-	-
10	20	P10	EXI3	RXD1*1 (/TXD1)*2	-	OTO3A	-	-	-	-
9	19	P11	-	-	-	OTO4A	CMP2P	-	CMP2P	CMP2P
8	18	P12	-	RXD0*1 (/TXD0)*2	SDAU0	OTO1B	-	-	-	-
7	17	P00/TEST0	EXI3	-	-	-	-	-	-	-
6	16	P13	EXI2	TXD0*1	SCLU0	OTO5B	-	AIN4	-	-
5	15	RESET_N	-	-	-	-	-	-	-	-
4	14	P14	-	-	-	-	CMP1P	AIN0	CMP1P/ CMP2P	AIN0 /CMP1P
3	13	P15	-	-	-	-	CMP1M	AIN1	CMP1M/ CMP2M	AIN1 /CMP1M
2	12	P16	-	-	-	-	CMP2M	AIN2	CMP2M	AIN2 /CMP2M
1	11	P17	EXI0	-	-	-	-	AIN3	-	-
-	10	P20	-	-	-	-	-	AIN4	-	-
-	9	P21	-	-	-	OTO4B	-	-	-	-
-	8	P22	-	-	-	OTO5B	-	-	-	-
20	7	P23	-	TXD1*1	-	OTO5A	DACOUT0	-	-	-
DIE	DIE	NC	-	-	-	-	-	-	-	-

*1 : The UARTpin use with a combination of the same suffix pins

*2 : RXDn pin is shareable with TXDn pin by SFR setting

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PIN DESCRIPTION

"I/O" Field in the below table define the pin type ("-" : power supply pin, "I" : Input pin, "O" : Out put pin, "I/O" bi-directional pin)

Table 4 Pin Description

Function	Functional pin name	LSI pin name	I/O	Description
Power	-	VSS	-	Negative power supply pin (-) Define this terminal potential as V_{SS}.
	-	VDD	-	Positive power supply pin (+). Connect a capacitor C_V (more than 1µF) between this pin and VSS. Define this terminal potential as V_{DD}
	-	VDDL	-	Power supply for internal logic (internal regulator's output). Connect a capacitor C_L (1µF) between this pin and VSS.
Debug ISP	TEST0	P00/ TEST0	I/O	Input/output for testing This pin which is shared with P00 is used as on-chip debug interface and ISP function and is initialized as pull-up input mode by the system reset.
Reset	RESET_N	RESET_N	I	Reset input. Appling this pin "L" level shifts MCU to system reset mode. Appling this pin "H" level shifts MCU to program running mode. No pull-up resistor is built-in.
General input port (GPI)	P00	P00/ TEST0	I/O	General purpose input. - Input with Pull-up (initial value) - Input without Pull-up Not available as general inputs when using the on-chip debug interface or ISP function.
General port (GPIO)	P01 to P07	P01 to P07	I/O	General purpose input/output - High-impedance (initial value) - Input with Pull-up - Input without Pull-up - CMOS output - N channel (N-ch) open drain output - P channel (P-ch) open drain output
	P10 to P17	P10 to P17		
	P20 to P23	P20 to P23		
Career frequency output	-	P13 P23	O	Career frequency output
External Interrupt (1st function)	EXI0	P03 P17	I	External Maskable Interrupt 0 input
	EXI1	P04 P05		External Maskable Interrupt 1 input
	EXI2	P06 P13		External Maskable Interrupt 2 input
	EXI3	P00 P10		External Maskable Interrupt 3 input
Operational Timer (4th function)	OTO0A	P03	O	Operational Timer 0 A output
	OTO0B	P04		Operational Timer 0 B output
	OTO1A	P05		Operational Timer 1 A output
	OTO1B	P07 P12		Operational Timer 1 B output
	OTO2A	P06		Operational Timer 2 A output
	OTO3A	P10		Operational Timer 3 A output
	OTO4A	P11		Operational Timer 4 A output
	OTO4B	P02 P21		Operational Timer 4 B output
	OTO5A	P23		Operational Timer 5 A output
	OTO5B	P13 P22		Operational Timer 5 B output
I²C Bus (3rd function)	SCLU0	P13	I/O	I²C Unit0 Clock input/output
	SDAU0	P12		I²C Unit0 Data input/output

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Function	Functional pin name	LSI pin name	I/O	Description
UART (2nd function)	RXD0	P12	I	UART0 received data input
	TXD0	P13	O	UART0 transmission data output
	RXD1	P10	I	UART1 received data input
	TXD1	P23	O	UART1 transmission data output
Successive approximation type A/D converter (SA-ADC) (6/8th function)	AIN0 to AIN4	P14 P15 P16 P17 P13 P20	I	SA-ADC channel 0 to 4 analog input
D/A converter (5th function)	DACOUT0	P23	O	D/A converter 0 output (select by SFR)
Analog comparator (5/7/8th function)	CMP0P	P01	I	Analog comparator 0 Noninverting input
	CMP0M	P02		Analog comparator 0 Inverting input
	CMP1P	P01 P14		Analog comparator 1 Noninverting input
	CMP1M	P02 P15		Analog comparator 1 Inverting input
	CMP2P	P11 P14		Analog comparator 2 Noninverting input
	CMP2M	P15 P16		Analog comparator 2 Inverting input

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TERMINATION OF UNUSED PINS

Table 5 shows the processing of unused pins.

Table 5 Termination of unused pins

Pin	pin termination
RESET_N	Connect to VDD
P00/TEST0	Open with the initial condition of pulled-up input mode
P01 to P07 P10 to P17 P20 to P23	Open the pins with the initial condition of Hi-impedance (input/output invalid) mode.

[Note]

- **Terminate unused input pins according to the table 5 in order to avoid unexpected through-current in the pins.**

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V_{DD}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}			-0.3 to +2.0	
Input voltage	V_{IN}			-0.3 to V_{DD}+0.3*1	
Output voltage1	V_{OUT1}			-0.3 to V_{DD}+0.3*1	
"H" level output current	I_{OUTH}	Ta = +25°C	1pin	-40*2	mA
			Total	-150*2	
"L" level output current	I_{OUTL}		1pin	+40	
			Total	+150	
Power dissipation	PD	Ta = +25°C		1	W
Storage temperature	T_{STG}	-		-55 to +150*3	°C

*1: 6.5V or lower
*2: The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*3: Please observe a storage conditions shown in the document "Board Mounting (soldering)" about the storage conditions until implementation.

[Note]
Stresses above the absolute maximum ratings listed in the above table may cause permanent damage to the device.
These are stress ratings only and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambient)	Ta	-	-40 to +105	°C
Operating temperature (Chip-Junction)	Tj	-	-40 to +115	
Operating voltage 1	V_{DD}	-	4.5 to 5.5	V
Operating frequency (CPU)	f_{OP}	V_{DD} =4.5 to 5.5V	30k to 16M	Hz
VDDL pin external capacitance	C_L	-	1.0 ±30%	µF

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Thermal characteristics

The maximum chip-junction temperature, T_{jmax}, is estimated using the following equation.

$T_{j\,max} = T_{a\,max} + P_{D\,max} \times \theta_{ja}$
$T_{a\,max}$: maximum ambient temperature
$P_{D\,max}$: LSI maximum power dissipation
θ_{ja} : Package junction to ambient thermal resistance

Design a Mounting board by considering heat radiation such as power dissipation and ambient temperature to satisfy the recommended conditions.

The following table shows the each package's thermal resistance for thermal design reference estimated by simulation based on the PCB (printed circuit board) conditions define as a below.

Parameter	Symbol	Package type	PCB condition		Unit
			L1	L2	
Thermal resistance	θja	TSSOP20	72.32	68.83	°C/W
		WQFN24	38.86	34.81	

PCB conditions:

PCB name	L1	L2	Unit
PCB size (L / W / T)	114.3 / 76.2 / 1.6	114.3 / 76.2 / 1.6	mm
Number of layers	1	2	layer
Wiring density	60% (top layer)	60% (top and bottom layer)	-
Wind condition	Windlessness (0m/s)		-

The thermal resistance of WQFN is the simulated value when the exposed die pad part (100%) is soldered with the board.

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Current Consumption

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Condition		Rating				Unit	Measuring circuit
	Operating mode	circuit state *1	Min.	Typ.*2	Max.			
					Tj≤+95°C	Tj≤+115°C		
IDD1	STOP	All clocks are stopped.	-	80	120	130	μA	1
IDD2-1R	HALT (Hi-speed oscillation off)	RC32K is oscillating. PLL is stopped.	-	90	140	150		
IDD3	CPU running in SYSCLK=32.768kHz	RC32K is oscillating. PLL is stopped.	-	100	160			
IDD5-H16	CPU running in wait-mode SYSCLK=16MHz	PLL is oscillating as PLL16M mode. HSCLK = 16MHz	-	3.3	4.2		mA	

*1: WDT is operating except IDD1, and all clocks peripheral circuits are stopped by block control.
*2: On the condition of V_{DD}=5.0V, Ta=+25°C

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On-chip Oscillator

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
RC32K frequency	f_{RCL1}	Ta= -20 to +85°C	Typ. -1.5%	32.768	Typ. +1.5%	kHz	1
		Ta= -40 to +105°C	Typ. -2.0%		Typ. +2.0%		
PLL oscillation frequency	f_{PLL1}	Ta= -20 to +85°C with RC32K	Typ. -1.5%	64	Typ. +1.5%	MHz	
		Ta= -40 to +105°C with RC32K	Typ. -2.0%		Typ. +2.0%		
PLL oscillation stabilization time	T_{PLL}	-	-	-	2	ms	

*: The frequency is the factory default specification. It may vary depending on the board mounting.

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Input / Output pin 1

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage1 "H"/"L" level (all input/output port)	VOH1	IOH1=-10mA		V_{DD} -1.5	-	-	V	2
		IOH1=-4mA		V_{DD} -0.5	-	-		
	VOL1	IOL1=+10mA		-	-	1.5		
		IOL1=+4mA		-	-	0.5		
Output voltage2 "L" level (all input/output port except TEST0)	VOL2	When N-ch open drain output mode is selected	IOL2=+15mA	-	-	0.7		
			IOL2=+8mA	-	-	0.5		
			IOL2=+3mA	-	-	0.4		
Output voltage2 "H" level (all input/output port except TEST0)	VOH2	When P-ch open drain output mode is selected	IOL2=-10mA	V_{DD} -1.5	-	-		
			IOL2=-4mA	V_{DD} -0.5	-	-		

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Input current1 (RESET_N)	IIH1	VIH1=V_{DD}	-	-	1	µA	4
	IIL1	VIL1=V_{SS}	-1*1	-	-		
Input current2 (P00/TEST0)	IIL2	VIL2=V_{SS} (pull-up mode) *2	-1500*1	-1000*1	-300*1		
	V/IIL2	VIL2=V_{SS} (pull-up mode) *2	3.7	5.0	15	kΩ	
	IIH2Z	VIH2=V_{DD} (High impedance mode)	-	-	1	µA	
	IIL2Z	VIL2=V_{SS} (High impedance mode)	-1*1	-	-		
Input current3 (all input port except RESET_N, P00/TEST0, input/output port)	IIL3	VIL1=V_{SS} (pull-up mode) *2	-250*1	-125*1	-30*1		
	V/IIL3	VIL1= V_{SS} (pull-up mode) *2	22	40	150	kΩ	
	IIH3Z	VIH1=V_{DD} (High impedance mode)	-	-	1	µA	
	IIL3Z	VIL1=V_{SS} (High impedance mode)	-1*1	-	-		
Input voltage1 (all input port, input/output port)	VIH1	-	0.7 × V_{DD}	-	V_{DD}	V	5
	VIL1	-	0	-	0.3 × V_{DD}		
Pin capacitance (RESET_N, all input port, input/output port)	CPIN	f=10kHz Ta=25°C	-	-	10	pF	-

*1: The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value. For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*2: Measurement conditions: Typ: VDD = 5.0V, Max: VDD = 4.5V, Min: VDD = 5.5V

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Input / Output pin 2

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
"H" level output current1 *6	IOH1	1pin	-	-10*3*5	-	-	mA	3
"H" level output total current1 *1*4	IOH3	Total of group A or B ** (duty ≤ 50%)	Ta=-40 to 85 °C	-25*5	-	-		
			Ta=-40 to 105 °C	-12*5	-	-		
		All pin total (duty ≤ 50%)	Ta=-40 to 85 °C	-50*5	-	-		
			Ta=-40 to 105 °C	-24*5	-	-		
"L" level output current1 *6	IOL1	1pin (CMOS output mode)	-	-	-	10*3		
"L" level output current2 *6	IOL2	1pin (N-ch open drain output mode)	-	-	-	15*3		
"L" level output total current *2*4	IOL3	Total of group A or B ** (N-ch open drain output mode, duty≤50%)	Ta=-40 to 85°C	-	-	25		
			Ta=-40 to105°C	-	-	15		
		All pin total (N-ch open drain output mode, duty≤50%)	Ta=-40 to 85°C	-	-	50		
			Ta=-40 to 105°C	-	-	30		
Output leak (all input/output port)	IOOH	VOH=V_{DD} (High impedance mode)		-	-	+1	μA	
	IOOL	VOL=V_{SS} (High impedance mode)		-1*5	-	-		

** : Group A is "P00 to P07 and P10 to P12", group B is "P13 to P17 and P20 to P23".

*1: Sink-out current from VDD to the output pin, which can guarantee the device operation.
*2: Sink-in current from the output pin to VSS, which can guarantee the device operation.
*3: Do not exceed total current.
*4: The total current is on the condition of Duty≤50% (same applies to IOH1).
When the duty>50% the total current is calculated by following formula.
Total current = IOL3 x 50/n (When the duty is n%)
<For an example> When IOL3=100mA and n=80%,
Total current = IOL3 x 50/80 = 62.5mA
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.
*5: The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*6: These values are satisfied with VOH1, VOL1 and VOL2.

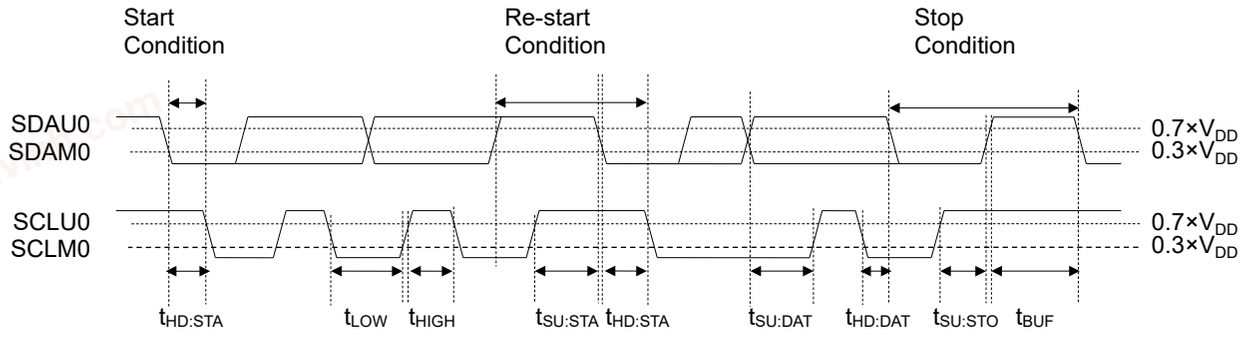
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I²C Bus Interface

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Rating									Unit
		Standard Mode			Fast Mode			1Mbps Mode			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Voltage	V_{DD}	4.5	-	5.5	4.5	-	5.5	4.5	-	5.5	V
SCL clock frequency	f_{SCL}	0	-	100	0	-	400	0	-	1000	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	4.0	-	-	0.6	-	-	0.26	-	-	µs
SCL "L" level time	t_{LOW}	4.7	-	-	1.3	-	-	0.5	-	-	
SCL "H" level time	t_{HIGH}	4.0	-	-	0.6	-	-	0.26	-	-	
SCL setup time (restart condition)	$t_{SU:STA}$	4.7	-	-	0.6	-	-	0.26	-	-	
SDA hold time	$t_{HD:DAT}$	0	-	-	0	-	-	0	-	-	
SDA setup time	$t_{SU:DAT}$	0.25	-	-	0.1	-	-	0.1	-	-	
SDA setup time (stop condition)	$t_{SU:STO}$	4.0	-	-	0.6	-	-	0.26	-	-	
Bus-free time	t_{BUF}	4.7	-	-	1.3	-	-	0.5	-	-	

When using the I²C as the master, configure the I²C master 0 mode register(I2M0MOD) and I²C bus 0 mode register (master side, I2U0MOD) so that meet these specifications.



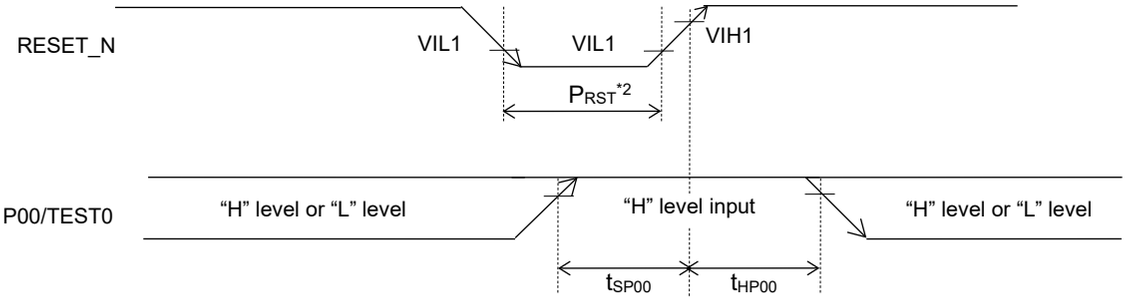
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Reset

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Reset pulse width*1	P_{RST}	-	2	-	-	ms	1
P00“H” level setup time	t_{SP00}	-	1	-	-		
P00“H” level hold time*1	t_{HP00}	-	1	-	-		

*1: except ISP mode. Refer to the User's manual “25.4 In-System Programing Function” for the timing in ISP mode.



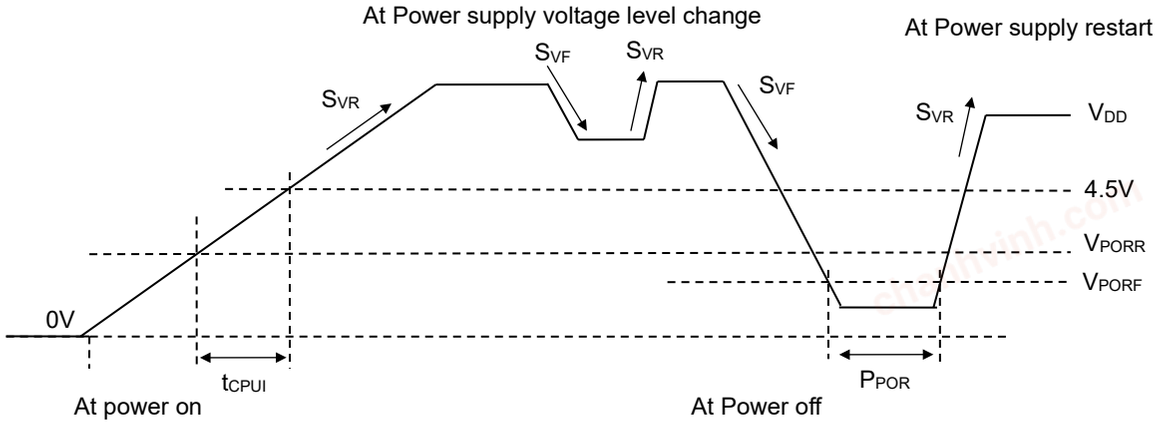
*2: V_{DD}=4.5V or over at power on.

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Slope of Power supply and Power On Reset

(V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter Symbol	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Power supply voltage rising inclination	S_{VR}	-	-	-	60	V/ms	1
Power supply voltage falling inclination	S_{VF}	-	-	-	2		
Power on reset detection voltage	V_{PORR}	At Power up (rising)	3.70	4.10	4.50	V	
	V_{PORF}	At Power down (falling)	3.60	4.00	4.40		
Power on reset minimum pulse width	P_{POR}	-	200	-	-	µs	
CPU operation start time (from the release of reset to the CPU starts to run)	t_{CPUI}	-	11.5	16.5	-	ms	-



[Note]

- **If a pulse shorter than the Power on reset minimum pulse width is asserted to V_{DD}, it may cause the MCU malfunction. Apply prevent measurement such as bypass capacitors or external reset input, and so on.**
- **Set V_{DD} to 4.5V or higher before starting CPU operation.**

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LLD characteristics

(V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
LLD Low voltage detection level	V_{LLD}	-	4.08	4.25	4.42	V	1
LLD current consumption	I_{LLD}	-	-	10	-	nA	1

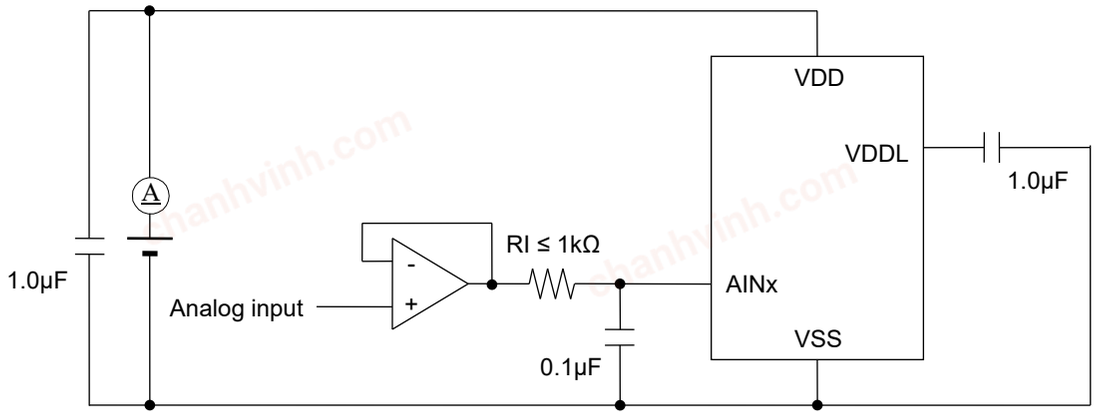
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Successive Approximation Type A/D Converter

(V_{DD}=4.5 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n_{AD}	-	-	-	12	bit
Conversion clock	f_{ADCLK}	nominal value	32.768	-	16000	kHz
Conversion time	t_{CONV}	f_{ADCLK} = 16MHz	1.375	-	-	µs
		f_{ADCLK} = 32.768kHz	-	518.799	-	
		At temperature conversion (f_{ADCLK} = 4MHz)	10.5	-	-	
		PGA is used (f_{ADCLK} = 16MHz)	8	-	-	
Overall error	-	4.5V ≤ V_{REF} ≤ 5.5V	-6	-	+6	LSB
Integral non-linearity error	INL_{AD}	f_{ADCLK} = 16MHz	-4	-	+4	
		f_{ADCLK} = 8MHz	-7	-	+7	
		f_{ADCLK} ≤ 4MHz	-8	-	+8	
		Reference voltage = Internal reference voltage (f_{ADCLK} ≤ 8MHz)	-	±64	-	
		Reference voltage = Internal reference voltage (f_{ADCLK} ≤ 4MHz)	-30	-	+30	
Differential non-linearity error	DNL_{AD}	f_{ADCLK} = 16MHz	-3	-	+3	
		f_{ADCLK} = 8MHz	-5	-	+5	
		f_{ADCLK} ≤ 4MHz	-7	-	+7	
		Reference voltage = Internal reference voltage (f_{ADCLK} ≤ 8MHz)	-	±63	-	
		Reference voltage = Internal reference voltage (f_{ADCLK} ≤ 4MHz)	-29	-	+29	
Zero-scale error	ZSE	f_{ADCLK} = 16MHz	-8	-	+8	
		f_{ADCLK} = 8MHz	-8	-	+8	
		f_{ADCLK} ≤ 4MHz	-10	-	+10	
		Reference voltage = Internal reference voltage	-80	-	+80	
Full-scale error	FSE	f_{ADCLK} = 16MHz	-8	-	+8	
		f_{ADCLK} = 8MHz	-8	-	+8	
		f_{ADCLK} ≤ 4MHz	-10	-	+10	
		Reference voltage = Internal reference voltage	-80	-	+80	
Internal reference voltage	$V_{ADCREFI}$	-	2.45	2.5	2.55	V
Temperature conversion slope	-	f_{ADCLK} = 4MHz	-10	-	-8	LSB/°C

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The current flows during the ADC sampling as it takes charging. Make the output impedance of the analog signal source 1kΩ or smaller. Also, putting 0.1μF capacitor on the ADC input pin is recommended for noise reduction.

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Analog comparator

(V_{DD}=4.5 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Comparator in-phase Input voltage range	V_{CMR}	-	0.1	-	V_{DD} -0.1	V	1
Comparator Input offset	V_{CMOF}	Ta=+25°C, V_{DD}=5.0V	-	±5	-	mV	
Comparator reference voltage	V_{CMREFI}	-	0.75	0.8	0.85	V	
Comparator Hysteresis	V_{CHYS}	-	-	15	-	mV	
Comparator Operation delay time	V_{CTS}	Hysteresis mode OFF (Input amplitude ±100mV)	-	-	100	ns	
		Hysteresis mode ON (Input amplitude ±100mV)	-	120	-		

D/A Converter

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n_{DA}	-	-	-	8	bit
Conversion cycle	tc	-	10	-	-	µs
Integral non-linearity error	INL_{DA}	RL=4MΩ	-2	-	2	LSB
Differential non-linearity error	DNL_{DA}	RL=4MΩ	-1	-	1	
Output impedance	Ro	-	5	10	15	kΩ
Full-scale error	FSE	V_{REF}=V_{DD}	V_{DD} -0.025	V_{DD}	V_{DD} +0.025	V
		V_{REF}=internal 0.8V reference voltage	0.725	0.8	0.875	
DAC internal reference voltage	$V_{DACREFI}$	-	0.75	0.8	0.85	

Programable Gain Amp

(V_{DD}=4.5 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Gain deviation*1	-	Gain=4	-0.7	-	+0.7	%
		Gain=8	-1.0	-	+1.0	
		Gain=16	-1.5	-	+1.5	
		Gain=32	-2.0	-	+2.0	
Input offset	$V_{INPGAOS}$	Ta=+25 °C, V_{DD}=5.0V	-	±5	-	mV
Input voltage range	V_{INPGA}	-	0.0	-	V_{DD}/Gain	V
Output voltage range	V_{OUTPGA}	-	0.0	-	V_{DD}-0.5	
Slew rate	V_{PGASR}	Gain=4, 8	2.5	-	-	V/µs
		Gain=16, 32	1.4	-	-	

*1 : V_{INPGA}=0.1*V_{DD}/Gain to 0.9*V_{DD}/Gain

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Flash Memory

(V_{SS}= 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +85	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		+4.5 to +5.5	V
Maximum rewrite count	CEPD	Data Flash		10000	times
	CEPP	Program Flash		100	
Erasing unit	-	Block erasing	Program Flash	16K	Byte
			Data Flash	all area	
	-	Sector erasing	Program Flash	1K	
			Data Flash	128	
Erasing time (Max.)	-	Block erasing / Sector erasing		50	ms
Writing unit	-	Program Flash		4	Byte
		Data Flash		1	
Writing time (Max.)	-	Program Flash		80	µs
	-	Data Flash		40	
Data retention period	YDR	rewriting count 100 times		15	years

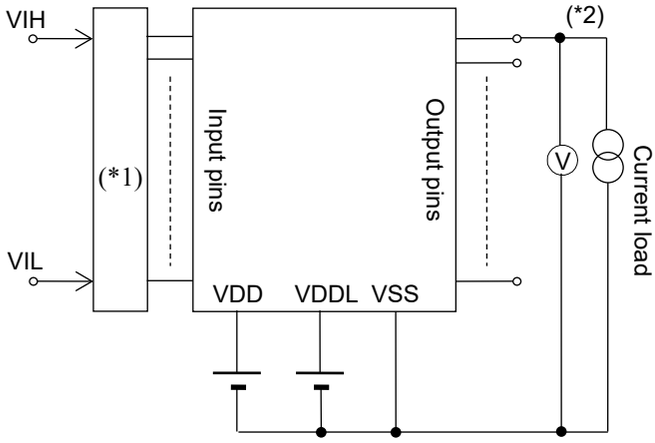
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Measuring circuit

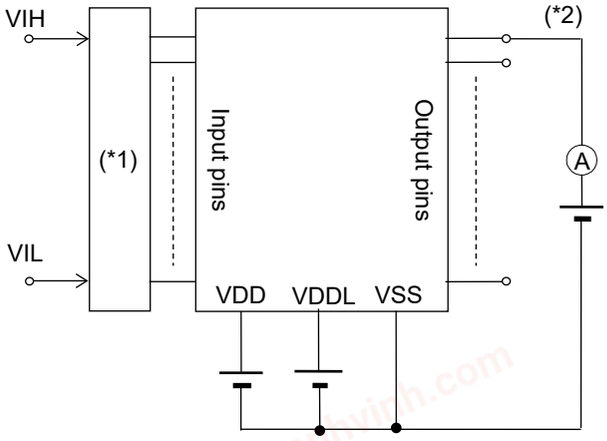
Measuring circuit 1



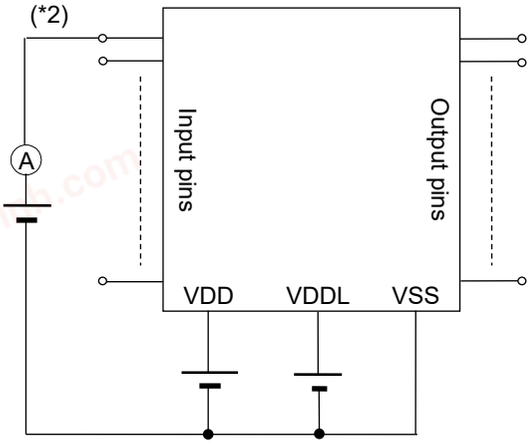
Measuring circuit 2



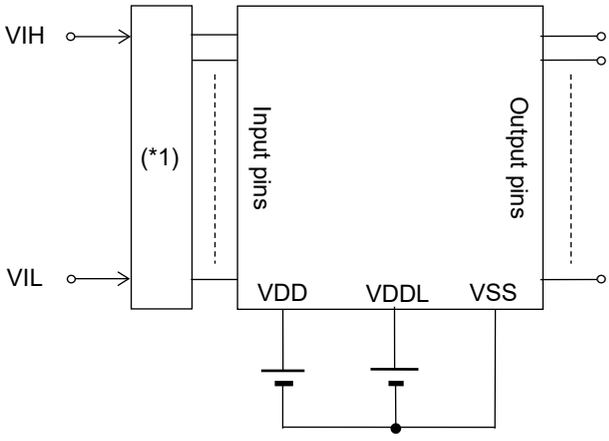
Measuring circuit 3



Measuring circuit 4



Measuring circuit 5

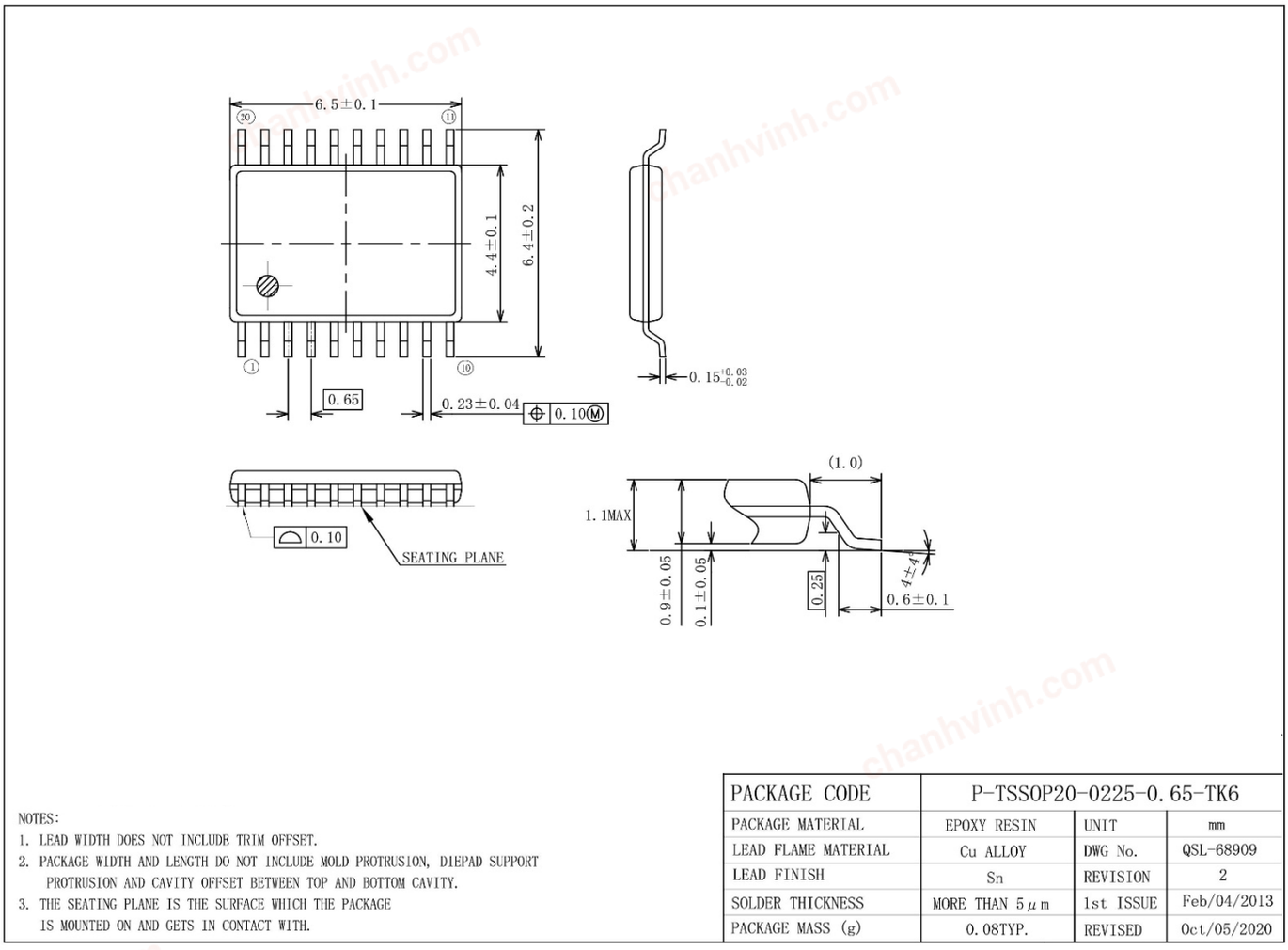


(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

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PACKAGE DIMENSIONS

20pin TSSOP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

PACKAGE CODE	P-TSSOP20-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68909
LEAD FINISH	Sn	REVISION	2
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Feb/04/2013
PACKAGE MASS (g)	0.08TYP.	REVISED	Oct/05/2020

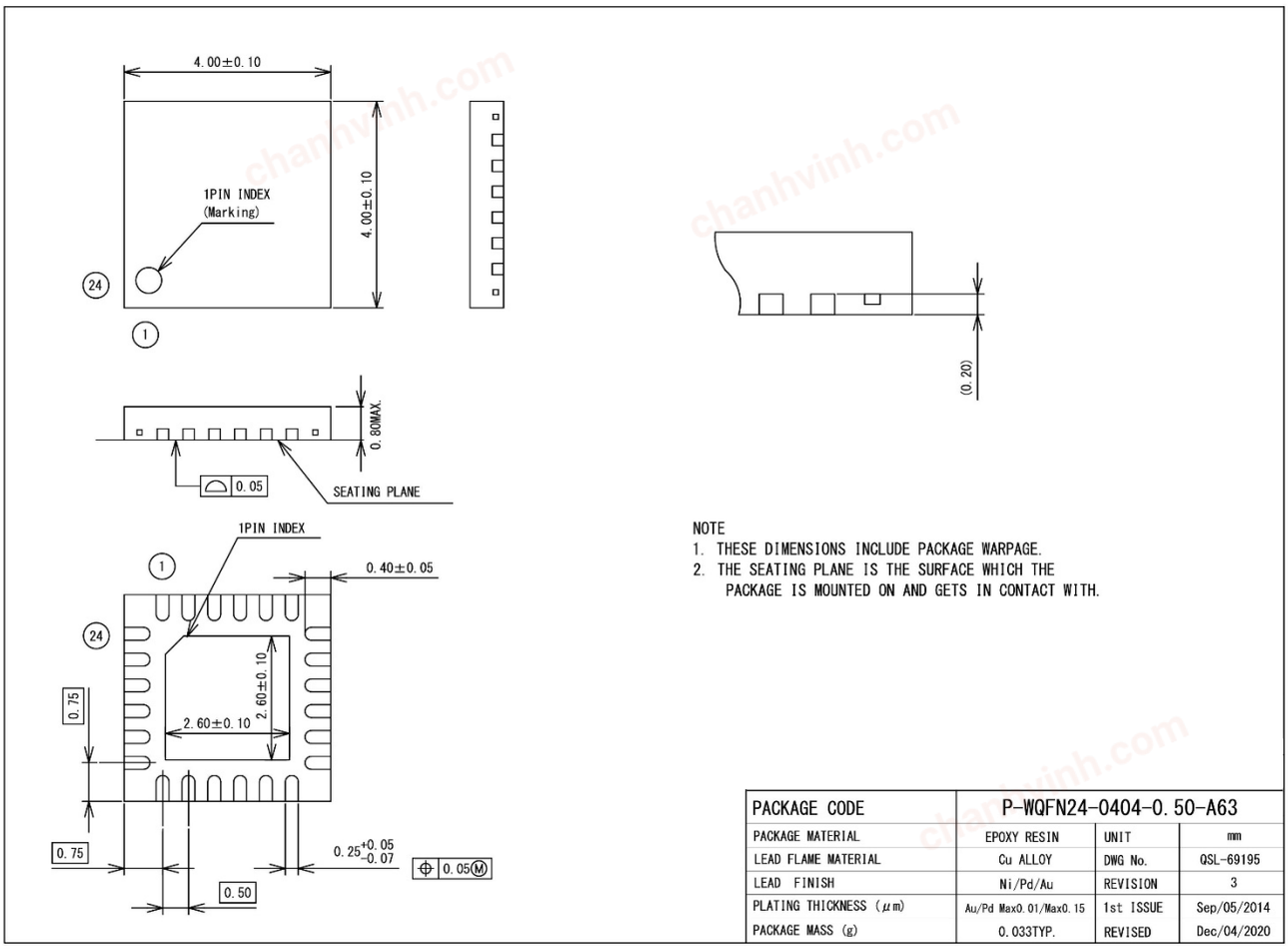
(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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24pin WQFN Package



PACKAGE CODE	P-WQFN24-0404-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69195
LEAD FINISH	Ni/Pd/Au	REVISION	3
PLATING THICKNESS (μm)	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/05/2014
PACKAGE MASS (g)	0.033TYP.	REVISED	Dec/04/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL62Q2000-01	Apr 1, 2024	-	-	1st Edition
FEDL62Q2045-02	May 24, 2024	-	-	Change the document name from FEDL62Q2000 to FEDL62Q2045
		22	22	Correction of incorrect CPU startup start time

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Notes for product usage

Notes on this page are applicable to the all ROHM microcontroller products.
For individual notes on each RHOM microcontroller product, refer to [Note]
in the chapters of each user's manual.
The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS
   Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON
   At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.
   On ROHM microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.
   Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY
   If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCT
   Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.
   When replacing from other product to ROHM microcontroller products, please evaluate enough the apparatus/system which implemented ROHM microcontroller products.

5. USE ENVIRONMENT
   When using ROHM microcontroller products in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

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Notice

Precaution on using ROHM Products

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   *1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

2) The Products specified in this document are not designed to be radiation tolerant.

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