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Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology" and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

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ML5243

5-Series Cell Li-ion Rechargeable Battery Protection IC

■ General Description

The ML5243 is a protection IC for the 5-cell Li-ion rechargeable battery pack. It detects individual cell overvoltage/undervoltage and the pack overcurrent/over-temperature, and its output signal indicates charge/discharge enable. And it has open-wire detection function of battery connection wire.

■ Features

- 3 to 5 cell high-precision overvoltage and undervoltage detection function
  Voltage detecting function for individual cells

Overvoltage detection threshold	4.225 V,	Detection accuracy: ±25 mV (0 to 60°C)
2nd overvoltage detection threshold	4.325V,	Detection accuracy: ±35 mV (0 to 60°C)
Undervoltage detection threshold	2.0 V,	Detection accuracy: ±50 mV (0 to 60°C)

- Overcurrent detection function

Discharge overcurrent detection threshold	70 mV,	Detection accuracy: ±15 mV (0 to 60°C)
Charge overcurrent detection threshold	-30 mV,	Detection accuracy: ±15 mV (0 to 60°C)
Short circuit detection threshold	300 mV,	Detection accuracy: ±20 mV (0 to 60°C)

- Temperature detection function : With external NTC (10 kΩ, B=3435) and 4.7 kΩ resistor
  Discharge inhibition temperature: detection 70 °C or higher, release 65 °C or lower
  Charge inhibition temperature : detection -5 °C or lower/50°C or higher, release 0 °C or higher/45°C or lower
- Detection delay timer built-in
  Overvoltage/undervoltage detection delay time : 2sec
  2nd overvoltage detection delay time : 8sec
  Open-wire detection delay time : 3.6sec
  TEST MODE reduces each detection delay time as 0.1sec by controlling the TEST pin input.
- Three type of charge/discharge enable signal output/
  Selected from CMOS / Nch open drain / Pch open drain (high voltage tolerant output)
- Detection voltages and detection delay times are modified by product code.
- Low current consumption (-40 to 85°C)

Normal operation state	: 4.5 µA (typ.),	10 µA (max)
Power-down state	: 0.1 µA (typ.),	1.0 µA (max)

- Supply voltage : +5 V to +25 V
- Operating temperature : -40°C to +85°C
- Package : 20-pin TSSOP

■ Application

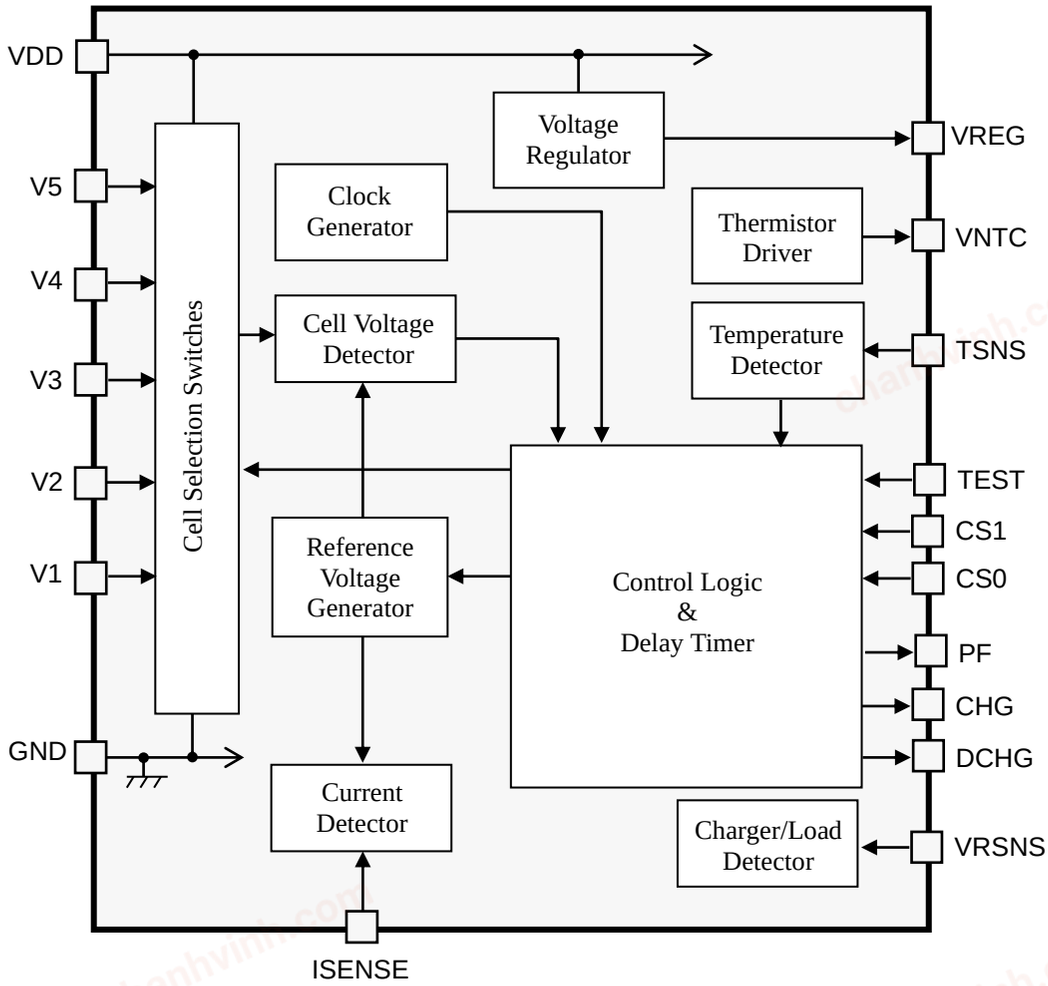
・Power tools and Garden tools
・Cordless Cleaner

■ Part number

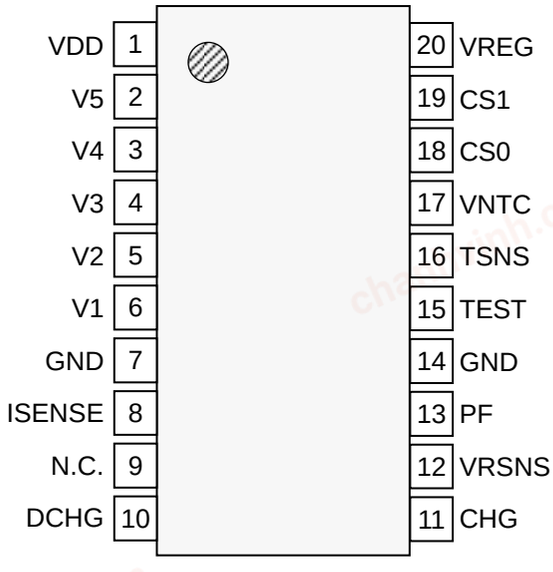
ML5243-xxxTD (xxx: code number)
The detection voltage, etc., depends on the code number.
The parameters for the 001 code are listed in this data sheet.
Please refer to the code list for codes other than 001.

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■ Block Diagram



■ Pin Configuration (top view)



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■ Pin Description

Pin No.	Pin name	I/O	Description
1	VDD	—	Power supply input pin. Connect an external CR filter for noise rejection.
2	V5	I	Battery cell 5 high voltage input pin.
3	V4	I	Battery cell 5 low voltage input and Battery cell 4 high voltage input pin.
4	V3	I	Battery cell 4 low voltage input and Battery cell 3 high voltage input pin.
5	V2	I	Battery cell 3 low voltage input and Battery cell 2 high voltage input pin.
6	V1	I	Battery cell 2 low voltage input and Battery cell 1 high voltage input pin.
7	GND	I	Ground pin.
8	ISENSE	I	Current sense resistor input pin. Connect a resistor of the resistance value corresponding to the detecting current between this pin and the GND pin. Should be tied to GND if not used.
9	N.C.		No connected. Connect to GND or Leave it electrically unconnected.
10	DCHG	O	Discharge enable pin. Output type is selected from CMOS / NMOS open drain / PMOS open drain. And its asserted level is selected from “L” level/”H” level.
11	CHG	O	Charge enable pin. Output type is selected from CMOS / NMOS open drain / PMOS open drain. And its asserted level is selected from “L” level/”H” level.
12	VRSNS	IO	Load/charger connection detecting input pin. Load or charger presence is decided by this input level.
13	PF	O	2nd overvoltage alarm output. Output type is selected from CMOS / NMOS open drain / PMOS open drain. And its asserted level is selected from “L” level/”H” level.
14	GND	—	Ground pin.
15	TEST	I	Detection delay time reduced test input pin. Every detection delay time is reduced by setting the voltage of this pin as VREG pin level. Internal 10kΩ pull-down resistor is connected.
16	TSNS	I	Input pin for high/low temperature charge/discharge inhibition detection. Connect a thermistor between this pin and GND. Should be tied to the VNTC pin through 10kΩ resistor if not used.
17	VNTC	O	Thermistor power supply. Should be connected to TSNS through a 4.7 kΩ resistor. If not used, this 4.7 kΩ resistor should be connected.
18,19	CS0,CS1	IO	Pins to specify battery cell number. Either the VREG or the GND level should be applied. CS1 / CS0 / Number of connected Battery cells GND / GND / 5 cell GND / VREG / 4 cell VREG / GND / VREG / 3 cell
20	VREG	O	Built-in 3.3 V regulator output pin. Should be tied to GND through a 1 μF or larger capacitor. Do not use this pin as power supply for an external circuit.

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■ Absolute Maximum Ratings

GND=0V, Ta=25°C

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Applied to VDD pin	-0.3 to +50	V
Input voltage	V_{IN1}	Applied to V1 to V5 pins	-0.3 to V_{DD}+0.3	V
	V_{IN2}	Applied to VRSNS pin	V_{DD}-50 to V_{DD}+0.3	V
	V_{IN3}	Applied to CS0, CS1, ISENSE, TSNS pins	-0.3 to V_{REG}+0.3	V
	V_{IN5}	Applied to TEST pin	-0.3 to +4.8	V
Output voltage	V_{OUT1}	Applied to DCHG, CHG, PF pins, if output type is CMOS. Applied to PF pin if output type is PMOS open drain	-0.3 to V_{DD}+0.3	V
	V_{OUT2}	Applied to DCHG, CHG, PF pins, if output type is NMOS open drain.	-0.3 to +50	
	V_{OUT3}	Applied to DCHG, CHG pins, if output type is PMOS open drain.	V_{DD}-50 to V_{DD}+0.3	V
	V_{OUT4}	Applied to VREG pin	-0.3 to +4.8	V
	V_{OUT5}	Applied to VNTC pin.	-0.3 to V_{REG}+0.3	V
Power dissipation	P_D	—	1.0	W
Short-circuit output current	I_{OS}	Applied to DCHG, CHG, PF, VNTC pins	10	mA
Storage temperature	T_{STG}	—	-55 to +150	°C

■ Recommended Operating Conditions

(GND= 0 V)

Item	Symbol	Condition	Range	Unit
Supply voltage	V_{DD}	Applied to VDD pin	5 to 25	V
Operational temperature	T_{OP}	—	-40 to +85	°C

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■ Electrical Characteristics

● DC Characteristics

V_{DD}=5 V to 25 V, GND=0 V, Ta=-40 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital "H" input voltage (Note 1)	V_{IH}	—	V_{REG}×0.8	—	V_{REG}	V
Digital "L" input voltage (Note 1)	V_{IL}	—	0	—	V_{REG}×0.2	V
Digital "H" input current (Note 2)	I_{IH}	V_{IH} = V_{REG}	—	—	2	µA
Digital "L" input current (Note 1)	I_{IL}	V_{IL} = GND	–2	—	—	µA
Digital "H" input current (Note 3)	I_{IHT}	V_{IH} = 3V	150	300	600	µA
Cell monitoring pin V5 to V1 Input current	I_{INVC1}	normal operation mode,	–0.5	0.1	0.5	µA
	I_{INVC2}	power-down mode	–0.5	0.0	0.5	µA
"L" output voltage (Note 4)	V_{OL}	I_{OL} = 100 µA	0	—	0.2	V
"H" output voltage (Note 4)	V_{OH}	I_{OH}=-100 µA	V_{DD} -0.2	—	V_{DD}	V
Pch open-drain output leakage current (Note 4)	I_{LKP}	V_O =0 V to V_{DD}	2	—	2	µA
Nch open-drain output leakage current (Note 4)	I_{LKN}	Vo = 0 V to V_{DD}	2	—	2	µA
VREG pin output voltage	V_{REG}	With no load	3.0	3.3	3.7	V
VNTC pin output voltage	V_{NTC}	With 14.7 kΩ resistor connection	2.2	2.4	2.6	V
VRSNS pin pull-up resistor	R_{VRU}	Charge overcurrent detected, Power-down mode	0.2	0.5	1.5	MΩ
VRSNS pin pull-down resistor	R_{VRD}	Discharge overcurrent detected, Short circuit detected	1	3	10	MΩ
VRSNS pin input leakage current	I_{LKVR}	Normal mode	-2	—	2	µA
TSNS pin input current	I_{INTS}	V_{NSTS}=0 V to V_{REG}	–1	—	1	µA
ISENSE pin input current	I_{INIS}	V_{ISENSE}= -0.1 V to 1 V	–1	—	1	µA

Note 1: Applied to CS0, CS1, and TEST pins.
Note 2: Applied to CS0, CS1 pins.
Note 3: Applied to TEST pin.
Note 4: Applied to DCHG, CHG, PF pins.

● Supply Current Characteristics

V_{DD}= 5 to 25 V, GND=0 V, Ta=-40 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in normal operation mode	I_{DD}	No output load (Note1)	—	4.5	10	µA
Current consumption in power-down mode	I_{DDS}	No output load	—	0.1	1.0	µA

(Note1) 4.7kΩ resistor is connected between VNTC and TSNS pins, and 10kΩ resistor is connected between TSNS and GND pins.

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- Code 001: Detection/Release Threshold Characteristics (Ta = 0 to 60 °C)

V_{DD}=18 V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	4.200	4.225	4.250	V
Overvoltage release threshold	V_{OVR}	—	3.975	4.025	4.075	V
2nd Overvoltage detection threshold	V_{SOV}	—	4.290	4.325	4.360	V
2nd Overvoltage release threshold	V_{SOVR}	—	4.225	4.275	4.325	V
Undervoltage detection threshold	V_{UV}	—	1.95	2.00	2.05	V
Undervoltage release threshold	V_{UVR}	—	2.95	3.00	3.05	V
Open-wire detection/release threshold	V_{OW}		0.5	0.6	0.7	V
Discharge overcurrent detection threshold	V_{OCU}	—	55	70	85	mV
Charge overcurrent detection threshold	V_{OCO}	—	-45	-30	-15	mV
Short circuit detection threshold	V_{SHRT}	—	280	300	320	mV
High temperature charge inhibition detection TSNS pin threshold	V_{CHD}	—	1.07	1.12	1.17	V
High temperature charge inhibition Release TSNS pin threshold	V_{CHR}	—	1.15	1.22	1.29	V
High temperature discharge inhibition detection TSNS pin threshold	V_{DHD}	—	0.72	0.77	0.82	V
High temperature discharge inhibition release TSNS pin threshold	V_{DHR}	—	0.80	0.85	0.90	V
Low temperature charge inhibition detection TSNS pin threshold	V_{CCD}	—	2.08	2.13	2.18	V
Low temperature charge inhibition release TSNS pin threshold	V_{CCR}	—	1.99	2.06	2.13	V
Charger connection detection VRSNS pin threshold	V_{PC}	Power-up from power-down mode	V_{DD} x 0.35	V_{DD} x0.5	V_{DD} x 0.65	V
Charger removal detection VRSNS pin threshold	V_{PLU}	Charge overcurrent detection	0	0.2	0.4	V
	V_{PLD}	Power-down mode	V_{DD} x 0.65	V_{DD} x 0.75	V_{DD} x 0.85	V
Load removal detection VRSNS pin threshold	V_{RL}	Discharge overcurrent detection, short circuit detection	1.0	1.2	1.4	V
VREG drop detection threshold	V_{UREG}	—	2.1	2.4	2.7	V
VREG drop release threshold	V_{RREG}	—	2.3	2.6	2.9	V

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- Code001: Detection Delay and Monitor Cycle Characteristics (Ta = 0 to 60 °C)

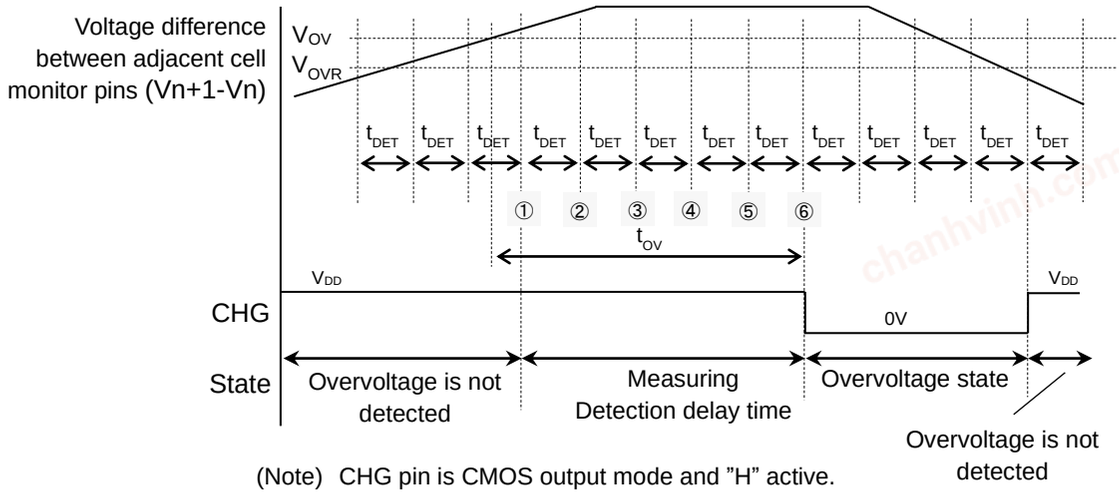
V_{DD}=18 V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage monitor cycle	t_{DET}	—	300	400	500	ms
Overvoltage detection delay	t_{OV}	—	5 × t_{DET}	—	6 × t_{DET}	ms
2nd Overvoltage detection delay	t_{SOV}	—	20 × t_{DET}	—	21 × t_{DET}	ms
Undervoltage detection delay	t_{UV}	—	5 × t_{DET}	—	6 × t_{DET}	ms
Open-wire detection/release delay	t_{OW}	—	9 × t_{DET}	—	10 × t_{DET}	ms
Discharge overcurrent detection delay	t_{OCU}	—	250	500	750	ms
Charge overcurrent detection delay	t_{OCO}	—	50	100	150	ms
Short circuit detection delay	t_{SHRT}	—	0.2	0.5	1.0	ms
Temperature monitor cycle	t_{PT}	—	300	400	500	ms
Temperature measurement time	t_{TM}	—	1.9	3.9	5.5	ms
Temperature detection/release delay	t_{TDR}	—	1 × t_{PT}	—	2 × t_{PT}	ms
Load removal detection delay	t_{ORL}	Discharge overcurrent state, short circuit state	50	100	150	ms
Charger removal detection delay	t_{OCHG}	Charge overcurrent state	50	100	150	ms
Cell voltage monitor cycle for test mode	t_{DETT}	TEST pin = “H”, Ta=25°C	75	100	125	ms
Overvoltage detection delay for test mode	t_{OVT}	TEST pin = “H”, Ta=25°C	0	—	1 × t_{DETT}	ms
2nd Overvoltage detection delay for test mode	t_{SOVT}	T TEST pin = “H”, Ta=25°C	0	—	1 × t_{DETT}	ms
Undervoltage detection delay for test mode	t_{UVT}	TEST pin = “H”, Ta=25°C	0	—	1 × t_{DETT}	ms
Open-wire detection/release delay for test mode	t_{OWT}	TEST pin = “H”, Ta=25°C	0	—	1 × t_{DETT}	ms
Temperature monitor cycle for test mode	t_{PTT}	TEST pin = “H”, Ta=25°C	75	100	125	ms
Temperature detection/release delay for test mode	t_{TDRT}	TEST pin = “H”, Ta=25°C	0	—	1 × t_{PTT}	ms

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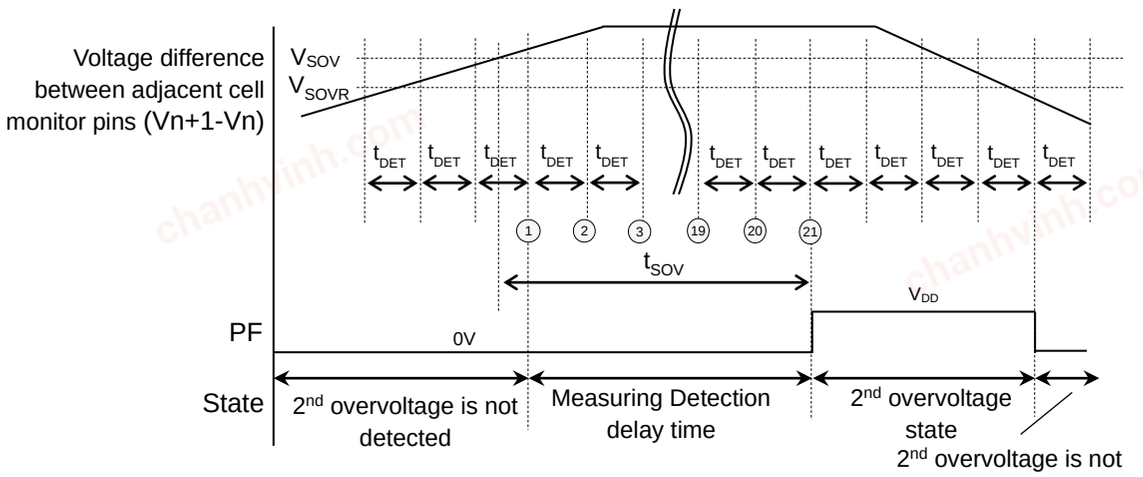
■ Timing Diagrams

- Overvoltage Detection and Recovery



(Note) CHG pin is CMOS output mode and "H" active.

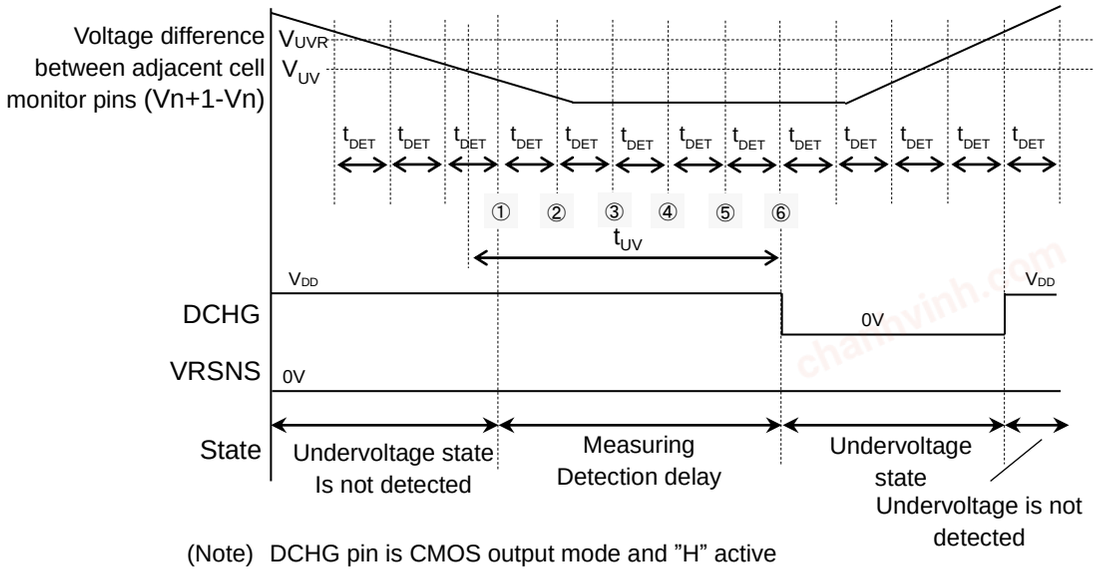
- 2nd Overvoltage Detection and Recovery



(Note) PF pin is CMOS output mode and "H" active.

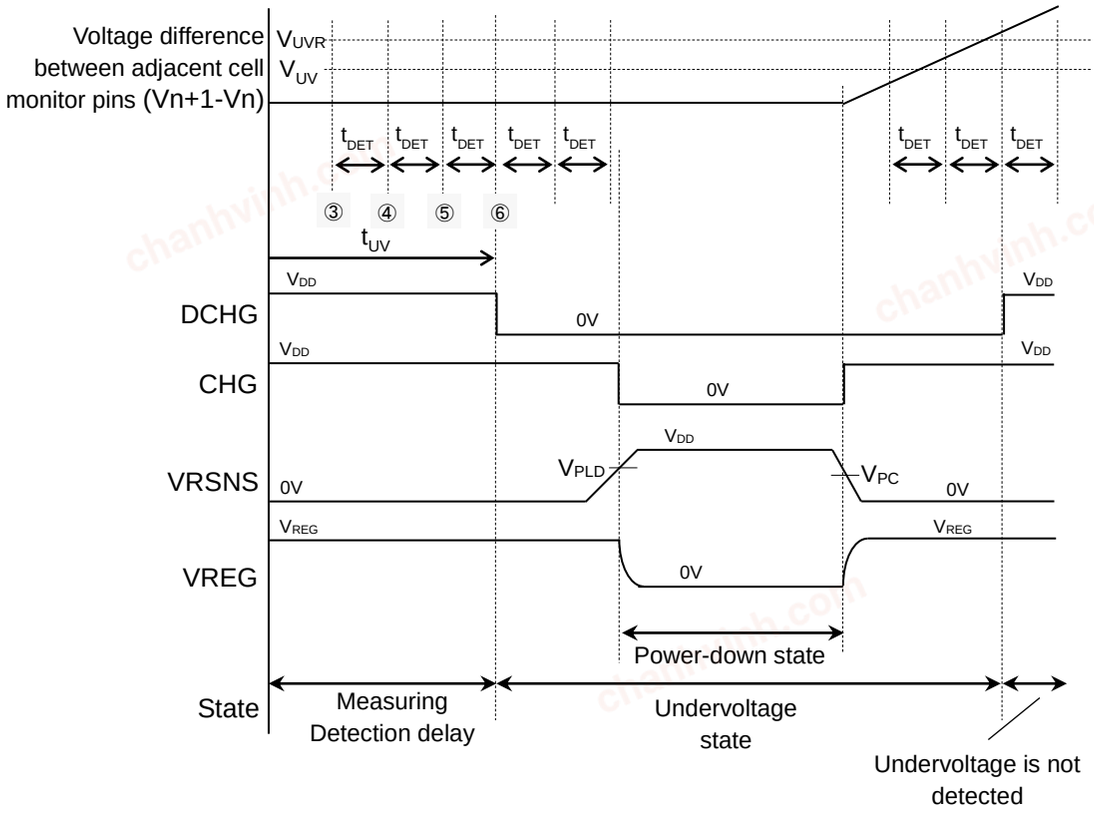
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- Undervoltage Detection and Recovery



(Note) DCHG pin is CMOS output mode and "H" active

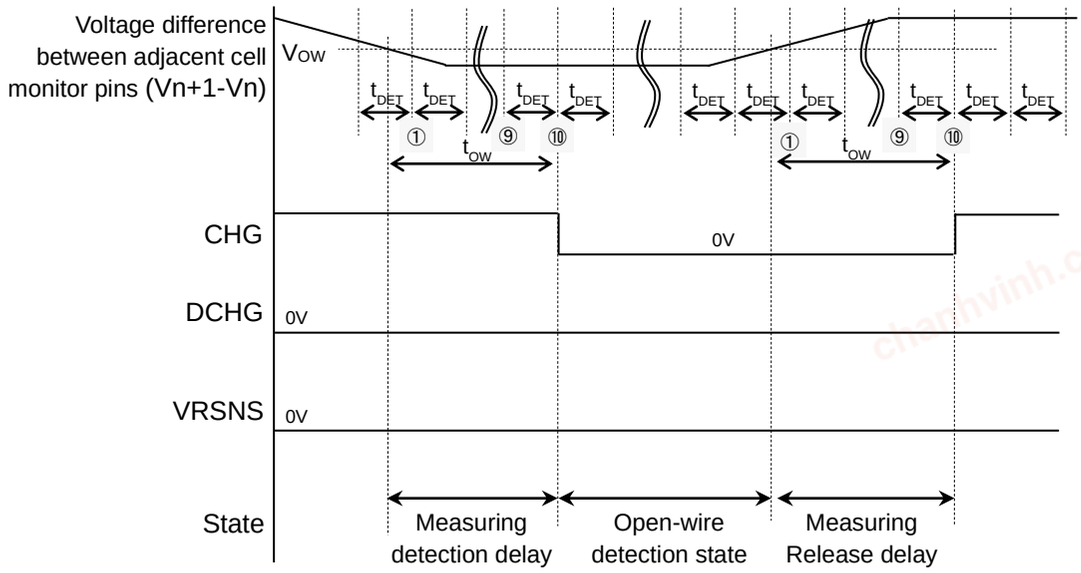
- Power-down after Undervoltage detection and Power-up



(Note) DCHG and CHG pins are CMOS output mode and "H" active

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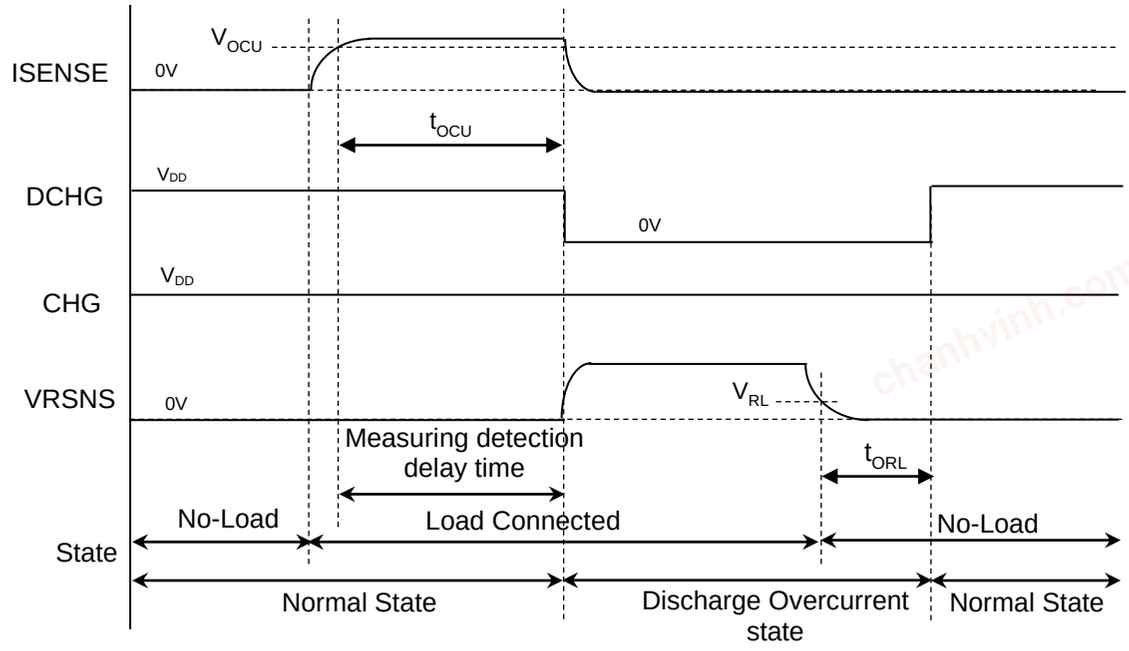
- Open-wire detection and recovery



(Note) DCHG and CHG pin are CMOS output mode and ”H” active.
The status is assumed to be undervoltge state.

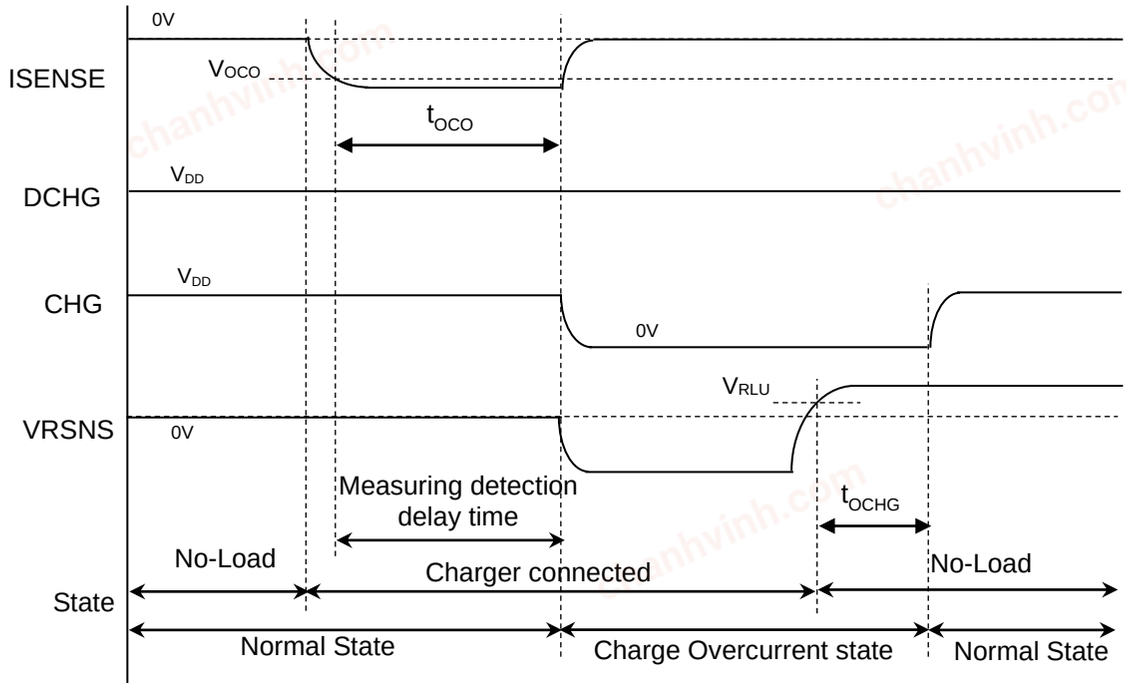
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- Discharge Over-current Detection and Recovery from it with Load Removal



(Note) DCHG and CHG pins are CMOS output mode and "H" active

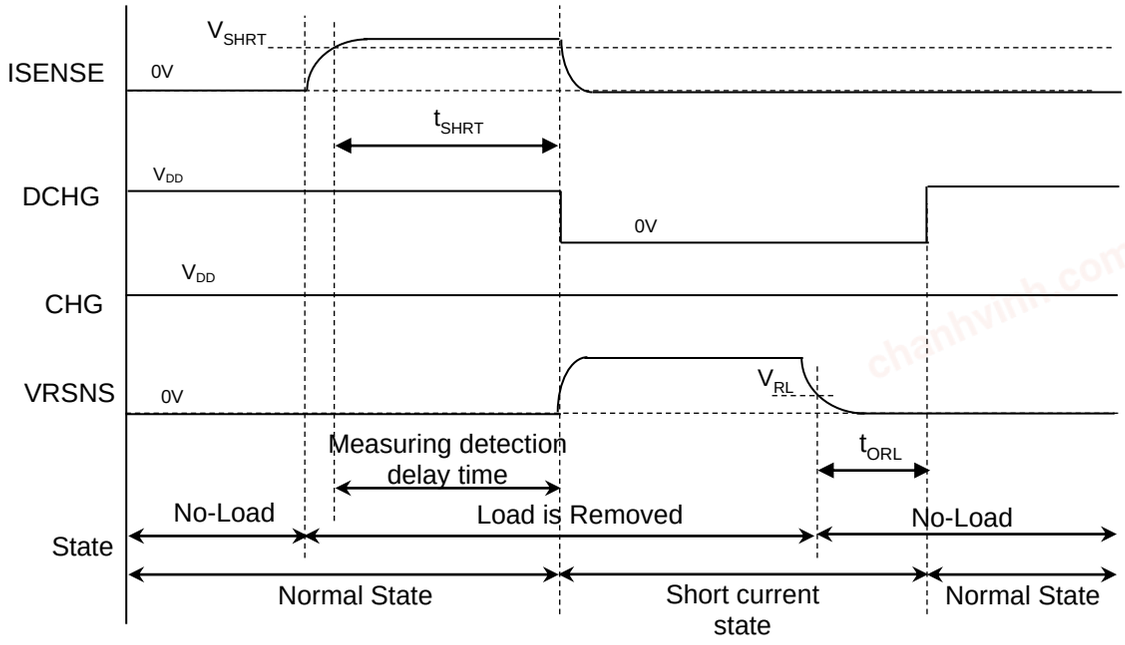
- Charge Over-current Detection and Recovery from it with Charger Removal



(Note) DCHG and CHG pins are CMOS output mode and "H" active

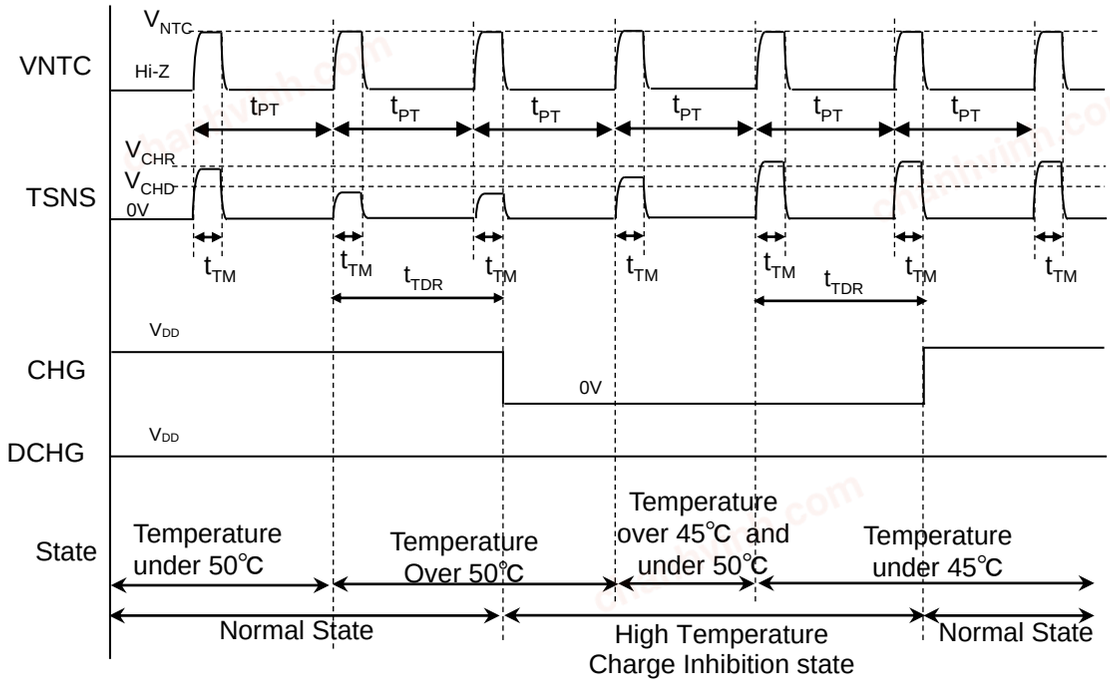
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- Short Circuit detection and Recovery from it with Load Removal



(Note) DCHG and CHG pins are CMOS output mode and "H" active

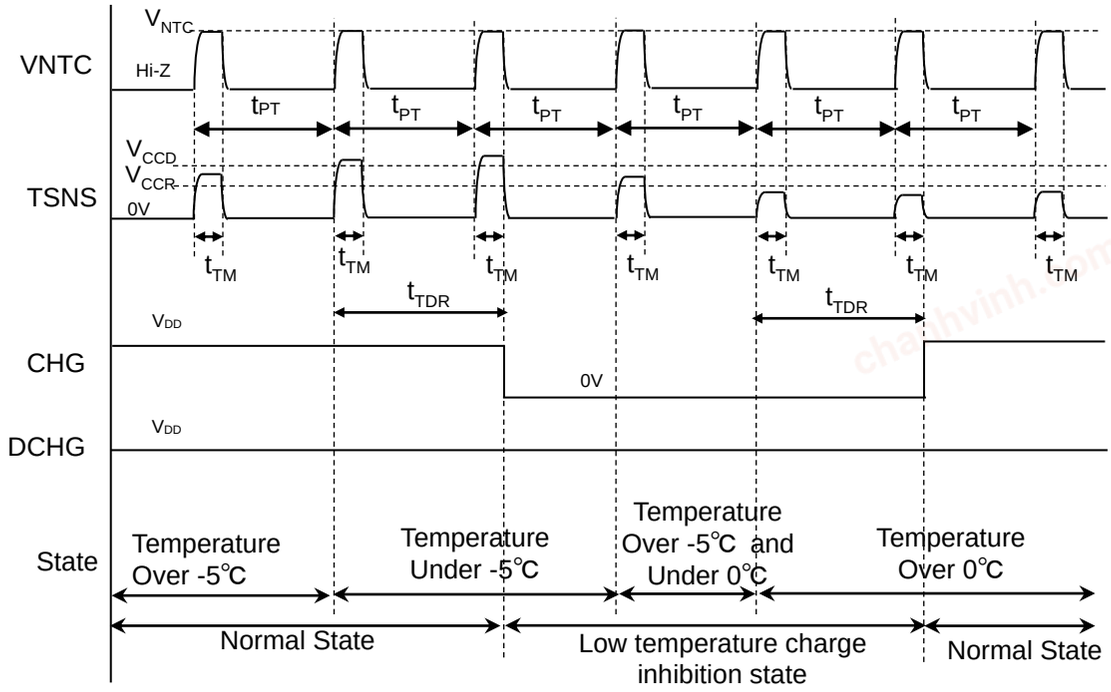
- High temperature Charge inhinition detection and Recovery



(Note) DCHG and CHG pins are CMOS output mode and "H" active

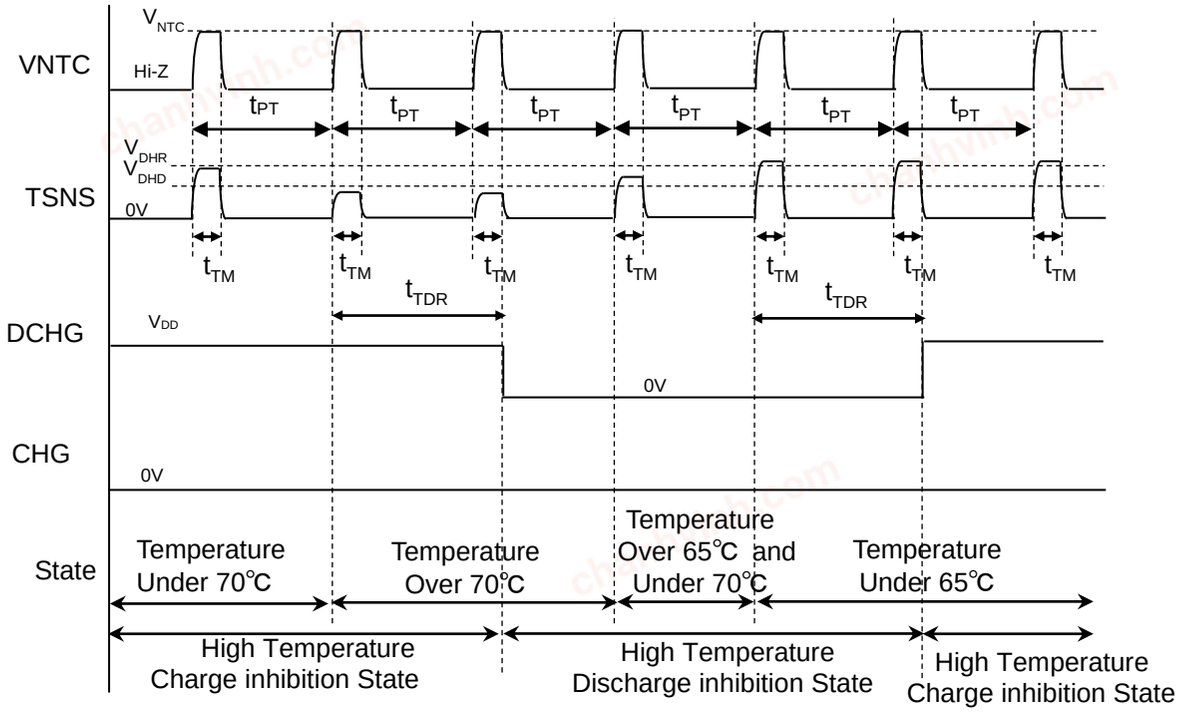
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- Low Temperature Charge Inhibition Detection and Recovery



(Note) DCHG and CHG pins are CMOS output mode and "H" active

- High Temperature Discharge Inhibition and Recovery



(Note) DCHG and CHG pins are CMOS output mode and "H" active

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■ Functional Description

● States of ML5243

The ML5243 has the following twelve states which depend on individual cell voltages and the input levels of the ISENSE and TSNS pins.

1. Initial state
2. Normal state
3. Overvoltage state
4. 2nd Overvoltage state
5. Undervoltage state (including power-down mode)
6. Open-wire state
7. Discharge overcurrent state
8. Charge overcurrent state
9. Short circuit state
10. High temperature charge inhibition state
11. Low temperature charge inhibition state
12. High temperature discharge inhibition state

Each state is described below.

1. Initial State

The initial state refers to the period while the battery cells are being connected to the ML5243 and connection of all the battery cells specified by the CS0 and CS1 pins is completed, before transitioning to the normal state.

In the initial state, when the VREG pin voltage is below the VREG drop detection threshold V_{UREG}, the DCHG pin output is discharge inhibited state and the CHG pin output is charge permitted state.

When the VREG pin level reaches or exceeds the VREG drop release threshold V_{RREG}, individual cell voltage monitoring takes place. If all the battery cells specified by the CS0 and CS1 pins reach or exceed the undervoltage release threshold V_{UVR}, the system transitions to the normal state. Overvoltage, overcurrent and temperature detection is also performed in parallel.

2. Normal State

The normal state refers to the period where all the battery cell voltages do not reach or exceed the overvoltage/undervoltage detection threshold, the ISENSE pin voltage is below the overcurrent detection threshold, and the TSNS pin voltage is below the high temperature detection threshold or above the low temperature detection threshold. In the normal state, both the DCHG and CHG pin outputs are set as both charge and discharge is permitted.

Individual cell voltages are monitored every 0.4 second for performing overvoltage/undervoltage detection, while the pack temperature is also monitored using an external thermistor every 0.4 second. The ISENSE pin voltage is always monitored to detect overcurrent in parallel.

3. Overvoltage State

When any one or more battery cell voltages reach or exceed the overvoltage detection threshold V_{OV} for longer than the overvoltage detection delay time $t_{OV,}$ the system enters the overvoltage state. If the ML5243 detects that voltage of all cell is below the overvoltage detection threshold V_{OV} for consecutive two times, detection delay time counting is cleared.

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In the overvoltage state, the CHG pin output is set to charge disabled, while the DCHG pin output maintains the value in the previous state.

Battery cell voltages decrease gradually by self-discharge or by a connected light load. When all of them reach or decrease below the overvoltage detection release threshold V_{OVR}, the system recovers from the overvoltage state.

4. 2nd overvoltage state

When more than one battery cell voltage reaches or exceeds the 2nd overvoltage detection threshold V_{SOV} , and when it past longer than the 2nd overvoltage detection delay time t_{SOV} since the ML5243 has detected it, the system enters the 2nd overvoltage state. If the ML5243 detects that voltage of all cell is below the 2nd overvoltage detection threshold V_{SOV} for consecutive two times, detection delay time counting is cleared.

In the 2nd overvoltage state, the PF pin output is set to 2nd overcharge detected state, while the DCHG pin output maintains the value in the previous state.

Battery cell voltages decrease gradually by self-discharge or a connected light load. When all of them reach or decrease below the 2nd overvoltage detection release threshold V_{SOVR}, the system recovers from the 2nd overvoltage state.

5. Undervoltage State

When more than one battery cell voltage reaches or decreases below the undervoltage detection threshold V_{UV}, and when it past longer than the undervoltage detection delay time t_{UV} since the ML5243 has detected it, the system enters the undervoltage state. If the ML5243 detects that voltage of all cell is above the undervoltage detection threshold V_{UV} for consecutive two times, detection delay time counting is cleared.

In the undervoltage state, the DCHG pin output is set to discharge disabled, while the CHG pin output maintains the value in the previous state.

In the undervoltage state, a 500 kΩ pull-up resistor is connected between the VRSNS pin and VDD. When the VRSNS pin voltage increases and reaches or exceeds the charger removal detection VRSNS threshold V_{PLD}, the system enters power-down mode to reduce current consumption.

In the undervoltage state, if the 2nd overvoltage is already detected, the ML5243 status doesn't be changed to power-down and VRSNS pin pull-up resistor is not connected.

If the VRSNS pin voltage reaches or decreases below the charger detection voltage V_{PC}, the system wakes up all the circuits to resume monitoring individual battery cell voltages.

If the system was in the overvoltage, undervoltage, high temperature or any overcurrent state before entering power-down mode, these error flags are cleared during power-down. After wake-up, if these errors are detected again for longer than the specified detection delay time, the system reenters the corresponding error state.

Battery cell voltages increase gradually while charging, and if all cell voltages reach or exceed the undervoltage detection release threshold V_{UVR}, the system recovers from the undervoltage state.

6. Open-wire state

When more than one battery cell voltage reaches or decreases below the open-wire detection threshold Vo_V, and when it past longer than the open-wire detection delay time to_V since the ML5243 has detected it, the system enters the open-wire state. If the ML5243 detects that voltage of all cell exceeds the open-wire detection threshold V_{OW} for once, the detection delay time counting is cleared.

In the open-wire state, CHG pin output is set to charge disabled. Because open-wire detection threshold V_{OW} is lower than undervoltage detection threshold V_{UV}, and undervoltage detection delay time t_{UV} is shorter than open-wire detection delay time t_{OW}, in the open-wire state the status is also in the undervoltage state, and DCHG pin output is set to discharge disabled.

When every cell voltage reaches or exceeds the open-wire detection threshold V_{OW}, and when it past longer than the open-wire detection delay time t_{OW} since the ML5243 has detected it, the system

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recovers from the open-wire state and CHG pin output is set to charge enabled. If the ML5243 detects that voltage of more than one cell voltage reaches or decrease below the open-wire detection threshold V_{OW} for once, the release delay time counting is cleared.

7. Discharge Overcurrent State

When the load is connected and ISENSE pin voltage reaches or exceeds the discharge overcurrent detection threshold V_{OCU} for longer than the discharge overcurrent detection delay time t_{OCU}, the system enters the discharge overcurrent state, regardless of the individual battery cell voltages. In the discharge overcurrent state, the DCHG pin output is set to discharge inhibiting state.

In the discharge overcurrent state, the VRSNS pin is pulled-down to GND with a 3 MΩ resistor and a backflow prevention diode.

The system recovers from the discharge overcurrent state when the VRSNS pin level reaches or decrease below the load removal detection threshold V_{RL} for longer than the load removal detection delay time t_{ORL} .

8. Charge Overcurrent State

When the charger is connected and ISENSE pin voltage reaches or exceeds the charge overcurrent detection threshold V_{OCO} for longer than the charge overcurrent detection delay time t_{OCO}, the system enters the charge overcurrent state, regardless of the individual battery cell voltages. In the charge overcurrent state the CHG pin output is set to charge inhibiting state, while the DCHG pin output maintains the value in the previous state.

In the charge overcurrent state, a 500 kΩ pull-up resistor is connected between the VRSNS pin and VDD pin. The system recovers from the charge overcurrent state when the VRSNS pin voltage reaches or exceeds the charger removal detection threshold V_{PLU} for longer than the charger removal detection delay time t_{OCHG}.

9. Short Circuit State

When the pack is overloaded and the ISENSE pin voltage reaches or exceeds the short circuit detection threshold V_{SHRT} for longer than the short circuit detection delay time $t_{SHRT,}$ the system enters the short circuit state, regardless of the battery cell voltages.

In the short circuit state, a 3 MΩ pull-down resistor is connected between the VRSNS pin and the GND pin through a backflow prevention diode.

The system recovers from the short circuit state when the VRSNS pin level reaches or decreases below the load removal detection threshold V_{RL} for longer than the load removal detection delay time t_{ORL}.

10. High Temperature Charge inhibition State

Pack temperature is monitored using an external thermistor every 0.4 seconds regardless of the battery cell voltages and current measuring. When the TSNS pin voltage reaches or decrease below the high temperature charge inhibition detection threshold V_{CHD} for longer than the temperature detection/release delay time t_{TDR} the system enters the high temperature charge inhibition state. In this state, the CHG pin output is in the charge inhibition state.

If the TSNS pin voltage reaches or exceeds the high temperature charge inhibition release TSNS pin threshold V_{CHR} for longer than the temperature detection/release delay time $t_{TDR,}$ the system recovers from the high temperature charge inhibition state and the CHG pin output is in the charge enable state.

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11. Low Temperature Charge Inhibition State

Pack temperature is monitored using an external thermistor every 0.4 seconds regardless of the battery cell voltages and current measuring. When the TSNS pin voltage reaches or exceeds the low temperature charge inhibition detection threshold V_{CCD} for longer than the temperature detection/release delay time t_{TDR} the system enters the low temperature charge inhibition state. In this state, the CHG pin output is in the charge inhibition state.

If the TSNS pin voltage reaches or decrease below the low temperature charge inhibition release TSTN pin threshold V_{CCR} for longer than the temperature detection/release delay time $t_{TDR,}$ the system recovers from the low temperature charge inhibition state and the CHG pin output is in the charge enable state.

12. High Temperature Discharge Inhibition State

Pack temperature is monitored using an external thermistor every 0.4 seconds regardless of the battery cell voltages and current measuring. When the TSNS pin voltage reaches or decrease below the high temperature discharge inhibition detection threshold V_{DHD} for longer than the temperature detection/release delay time t_{TDR} the system enters the high temperature discharge inhibition state. In this state, the DCHG pin output is in the discharge inhibition state.

If the TSNS pin voltage reaches or exceeds the high temperature discharge inhibition release TSNS pin threshold V_{DHR} for longer than the temperature detection/release delay time $t_{TDR,}$ the system recovers from the high temperature discharge inhibition state and the DCHG pin output is in the discharge enable state.

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- Selecting the Number of Battery Cells

Cell count is selectable from predefined 3 values using the CS0 and CS1 pins.
Its configuration is given in the table below.

CS1	CS0	Battery cell number	Unused Vn pins
GND	GND	5 cell	None
GND	VREG	4 cell	V1
VREG	GND	3 cell	V1, V2
VREG	VREG		V1, V2

- Code001: output pin status of each state

The table below shows the output pin status of each state.

	CHG	DCHG	PF	VRSNS	VREG
Initial state	"H"	"L"	"L"	"Hi-Z"	3.3V
Normal state	"H"	"H"	"L"	"Hi-Z"	3.3V
Overvoltage state	"Hi-Z"	"H"	"L"	"Hi-Z"	3.3V
2nd Overvoltage state	"Hi-Z"	"H"	"H"	"Hi-Z"	3.3V
Undervoltage state	"H"	"L"	"L"	500kΩpull-up	3.3V
Power down state	"Hi-Z"	"L"	"L"	500kΩpull-up	0V
Open-wire state	"Hi-Z"	"L"	"L"	500kΩpull-up	3.3V
Discharge overcurrent state	"Hi-Z"	"L"	"L"	3MΩpull-down	3.3V
Charge overcurrent state	"Hi-Z"	"H"	"L"	500kΩpull-up	3.3V
Short circuit state	"Hi-Z"	"L"	"L"	3MΩpull-down	3.3V
High temperature charge inhibit state	"Hi-Z"	"H"	"L"	"Hi-Z"	3.3V
High temperature discharge inhibit state	"H"	"L"	"L"	"Hi-Z"	3.3V
Low temperature charge inhibit state	"Hi-Z"	"H"	"L"	"Hi-Z"	3.3V

- Power-on/Power-off Sequence

Battery cells can be connected in any order, but it is recommend that the GND and VDD pins are connected first, and then connection continues from lower to higher voltage cells. There are no restrictions on the power supply voltage rise time at power-on, and power-off sequence or power supply voltage fall time at power-off.

After power-on, the system usually transitions to the normal state. However, it may transition to the undervoltage state due to chattering at power-on or other reasons. If it has transitioned to the undervoltage state and moved to power-down mode, apply the charger connection detection threshold V_{PC} or lower level to the VRSNS pin to power it up again.

In the battery connection, if it takes long time to set all the battery cells, the ML5243 might detect overvoltage/2nd overvoltage/undervoltage.

- Handling VDD Pin and V1 to V5 Pins

Since the VDD pin is the power supply input, put a noise elimination RC filter in front of the VDD input for stabilization. If the drive current requirement on the CHG, DCHG and PF pins is large, the resistor value of this noise filter should be adjusted so that the voltage drop across the resistor is smaller than 1 V.

The V1 to V5 pins are the monitor pins for individual cell voltages. Put a noise elimination RC filter in front of each battery cell to prevent false detection. On a system with less than 5 battery cells, unused Vn pins should be tied to GND.

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- Handling VREG Pin

The VREG pin is the power source of the built-in regulator which supplies power to the internal modules. Connect a 1 µF or larger capacitor between this pin and GND for stabilization. Do not use it as a power supply for external circuits since the supply current of the built-in regulator is limited.

- Unused Pin Treatment

The following table shows how to handle unused pins.

Unused pins	Recommended treatment
Vn	Connected to GND
VNTC	Tied to the TSNS pin with a 4.7kΩ resistor
TSNS	Tied to the GND with a 10kΩ resistor
VRSNS	Tied to the GND
ISENSE	Tied to the GND
CHG	Open
DCHG	Open
PF	Open

- Reducing each detection delay time

By setting the TEST pin as VREG level, cell voltage monitoring cycle and temperature monitoring cycle is reduced to 100ms(typ) and each detection delay time is reduced down to 1 monitoring cycle minimum.

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- Setting the CHG, DCHG and PF pin output level

CHG pin output level is shown.

	CHG pin output level (“H” active output)		
	CMOS	N-ch open drain	P-ch open drain
Initial state	“H” level	“Hi-Z” level	“H” level
Normal state	“H” level	“Hi-Z” level	“H” level
Overvoltage state	“L” level	“L” level	“Hi-Z” level
2nd Overvoltage state	“L” level	“L” level	“Hi-Z” level
Undervoltage state	“H” level	“Hi-Z” level	“H” level
Power down state	“L” level	“L” level	“Hi-Z” level
Open-wire state	“L” level	“L” level	“Hi-Z” level
Discharge overcurrent state	“H” level	“Hi-Z” level	“H” or “Hi-Z” level
Charge overcurrent state	“L” level	“L” level	“H” level
Short circuit state	“H” level	“Hi-Z” level	“H” or “Hi-Z” level
High temperature charge inhibit state	“L” level	“L” level	“H” level
High temperature discharge inhibit state	“L” level	“L” level	“H” level
low temperature charge inhibit state	“L” level	“L” level	“H” level

	CHG pin output level (“L” active output)		
	CMOS	N-ch open drain	P-ch open drain
Initial state	“L” level	“L” level	“Hi-Z” level
Normal state	“L” level	“L” level	“Hi-Z” level
Overvoltage state	“H” level	“Hi-Z” level	“H” level
2nd Overvoltage state	“H” level	“Hi-Z” level	“H” level
Undervoltage state	“L” level	“L” level	“Hi-Z” level
Power down state	“H” level	“Hi-Z” level	“H” level
Open-wire state	“H” level	“Hi-Z” level	“H” level
Discharge overcurrent state	“L” level	“L” level	“Hi-Z” level
Charge overcurrent state	“H” level	“Hi-Z” level	“H” level
Short circuit state	“L” level	“L” level	“Hi-Z” level
High temperature charge inhibit state	“H” level	“Hi-Z” level	“H” level
High temperature discharge inhibit state	“H” level	“Hi-Z” level	“H” level
Low temperature charge inhibit state	“H” level	“Hi-Z” level	“H” level

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DCHG pin output level is shown.

	DCHG pin output level (“H” active output)		
	CMOS	N-ch open drain	P-ch open drain
Initial state	“L” level	“L” level	“Hi-Z” level
Normal state	“H” level	“Hi-Z” level	“H” level
Overvoltage state	“H” level	“Hi-Z” level	“H” level
2nd Overvoltage state	“H” level	“Hi-Z” level	“H” level
Undervoltage state	“L” level	“L” level	“Hi-Z” level
Power down state	“L” level	“L” level	“Hi-Z” level
Open-wire state	“L” level	“L” level	“Hi-Z” level
Discharge overcurrent state	“L” level	“L” level	“Hi-Z” level
Charge overcurrent state	“H” level	“Hi-Z” level	“H” level
Short circuit state	“L” level	“L” level	“Hi-Z” level
High temperature charge inhibit state	“H” level	“Hi-Z” level	“H” level
High temperature discharge inhibit state	“L” level	“L” level	“Hi-Z” level
Low temperature charge inhibit state	“H” level	“Hi-Z” level	“H” level

	DCHG pin output level (“L” active output)		
	CMOS	N-ch open drain	P-ch open drain
Initial state	“H” level	“Hi-Z” level	“H” level
Normal state	“L” level	“L” level	“Hi-Z” level
Overvoltage state	“L” level	“L” level	“Hi-Z” level
2nd Overvoltage state	“L” level	“L” level	“Hi-Z” level
Undervoltage state	“H” level	“Hi-Z” level	“H” level
Power down state	“H” level	“Hi-Z” level	“H” level
Open-wire state	“H” level	“Hi-Z” level	“H” level
Discharge overcurrent state	“H” level	“Hi-Z” level	“H” level
Charge overcurrent state	“L” level	“L” level	“Hi-Z” level
Short circuit state	“H” level	“Hi-Z” level	“H” level
High temperature charge inhibit state	“L” level	“L” level	“Hi-Z” level
High temperature discharge inhibit state	“H” level	“Hi-Z” level	“H” level
Low temperature charge inhibit state	“L” level	“L” level	“Hi-Z” level

PF pin output level is shown.

	PF pin output level (“H” active output)		
	CMOS	N-ch open drain	P-ch open drain
2nd Overvoltage state	“H” level	“Hi-Z” level	“H” level
other state	“L” level	“L” level	“Hi-Z” level

	PF pin output level (“L” active output)		
	CMOS	N-ch open drain	P-ch open drain
2nd Overvoltage state	“L” level	“L” level	“Hi-Z” level
other state	“H” level	“Hi-Z” level	“H” level

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- Redefinition of Detection/Release Threshold Range and Step (product code)

  The detection/release thresholds can be redefined as shown in the following table.
  Since some combinations are unavailable, contact us for details.

Detecting voltage	Symbol	Threshold range	Threshold step
Overvoltage detection threshold	V_{OV}	3.65 V to 4.35 V	25 mV
Overvoltage release threshold	V_{OVR}	3.5 V to 4.25 V	25 mV
2nd Overvoltage detection threshold	V_{SOV}	3.85 V to 4.45 V	25 mV
2nd Overvoltage release threshold	V_{SOVR}	3.7 V to 4.35 V	25 mV
Undervoltage detection threshold	V_{UV}	1.5 V to 3.0 V	100 mV
Undervoltage release threshold	V_{UVN}	2.3 V to 3.5 V	100 mV
Charge overcurrent detection threshold	V_{OCO}	-30 mV to -100 mV	10 mV
Discharge overcurrent detection threshold	V_{OCU}	50 mV to 300 mV	50 mV
Short circuit detection threshold	V_{SHRT}	100 mV to 500 mV	100 mV
High temperature Discharge inhibition detection threshold	V_{DHD}	0.6 V to 1.2 V	10 mV
High temperature Charge inhibition detection threshold	V_{CHD}	0.7 V to 1.3 V	10 mV
Low temperature Charge inhibition detection threshold	V_{CCD}	2.0 V to 2.2 V	10 mV

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- Redefinition of Detection Delay Time of Overvoltage/2nd overvoltage/undervoltage detection

The detection delay times can be redefined as shown in the following table.

Detection delay time	Settable time(cycles for detection)							Unit
Overvoltage/undervoltage detection delay time	1 to 2	3 to 4	5 to 6	7 to 8	9 to 10	11 to 12	13 to 14	cycle
2nd overvoltage detection delay time	5 to 6	10 to 11	20 to 21	30 to 31	40 to 41	—	—	cycle
Open-wire detection/release delay time	1 to 2	3 to 4	5 to 6	7 to 8	9 to 10	11 to 12	13 to 14	cycle

Detection delay time	Settable time (detection cycle=400ms)							Unit
Overvoltage/undervoltage detection delay time	0.4 to 0.8	1.2 to 1.6	2.0 to 2.4	2.8 to 3.2	3.6 to 4.0	4.4 to 4.8	5.2 to 5.6	sec
2nd overvoltage detection delay time	2.0 to 2.4	4.0 to 4.4	8.0 to 8.4	12 to 12.4	16 to 16.4	—	—	sec
Open-wire detection/release delay time	0.4 to 0.8	1.2 to 1.6	20.0 to 2.4	2.8 to 3.2	3.6 to 4.0	4.4 to 4.8	5.2 to 5.6	sec

Temperature detection delay time and release delay time are not resettable.

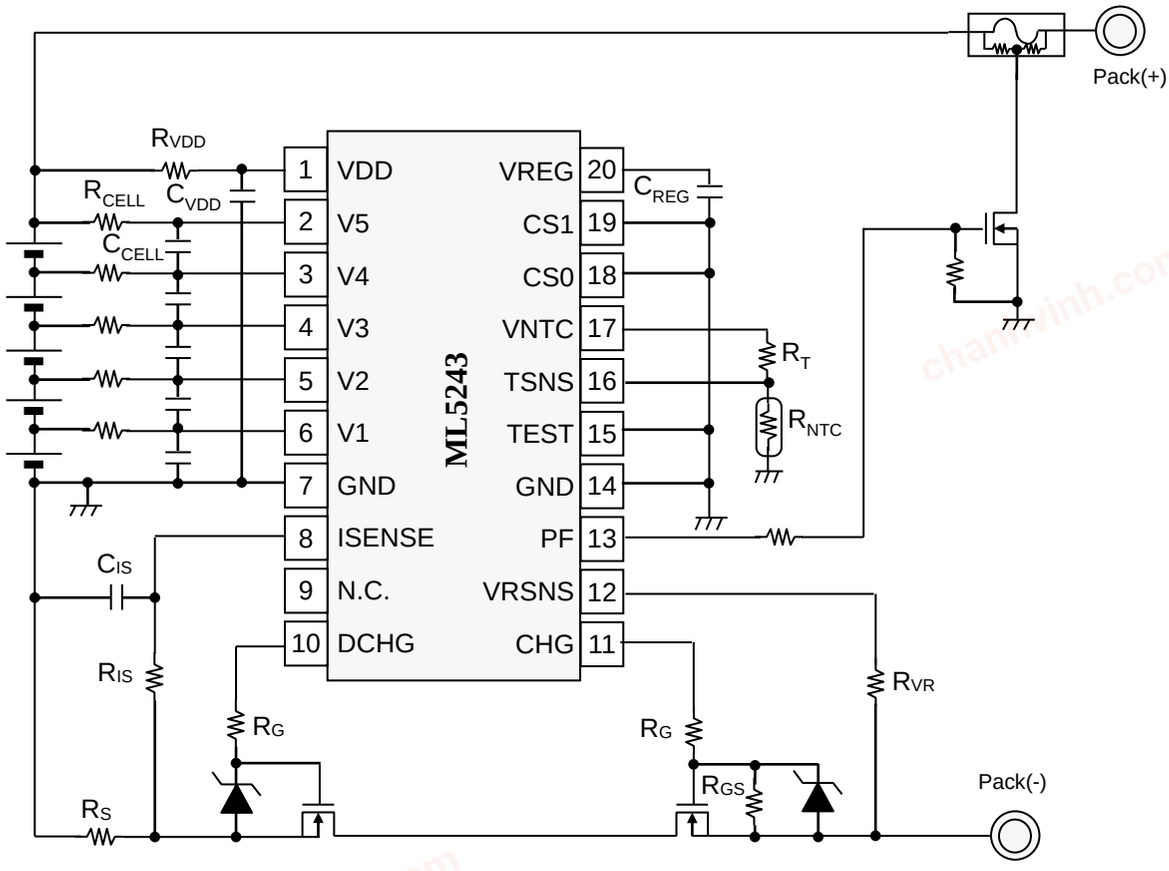
- Redefinition of Overcurrent detection delay time

The detection delay times can be redefined as shown in the following table.

Detection delay time	symbol	Settable time(ms)						
Discharge overcurrent detection delay time	t_{OCU}	25	50	100	200	300	400	500
Charge overcurrent detection delay time	t_{OCO}	25	50	100	200	300	400	500
Short circuit detection delay time	t_{SHRT}	0.1	0.2	0.3	0.4	0.5	—	—

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■ Application Circuit Example 1 (5-cell system)



■Recommended Values for External Components

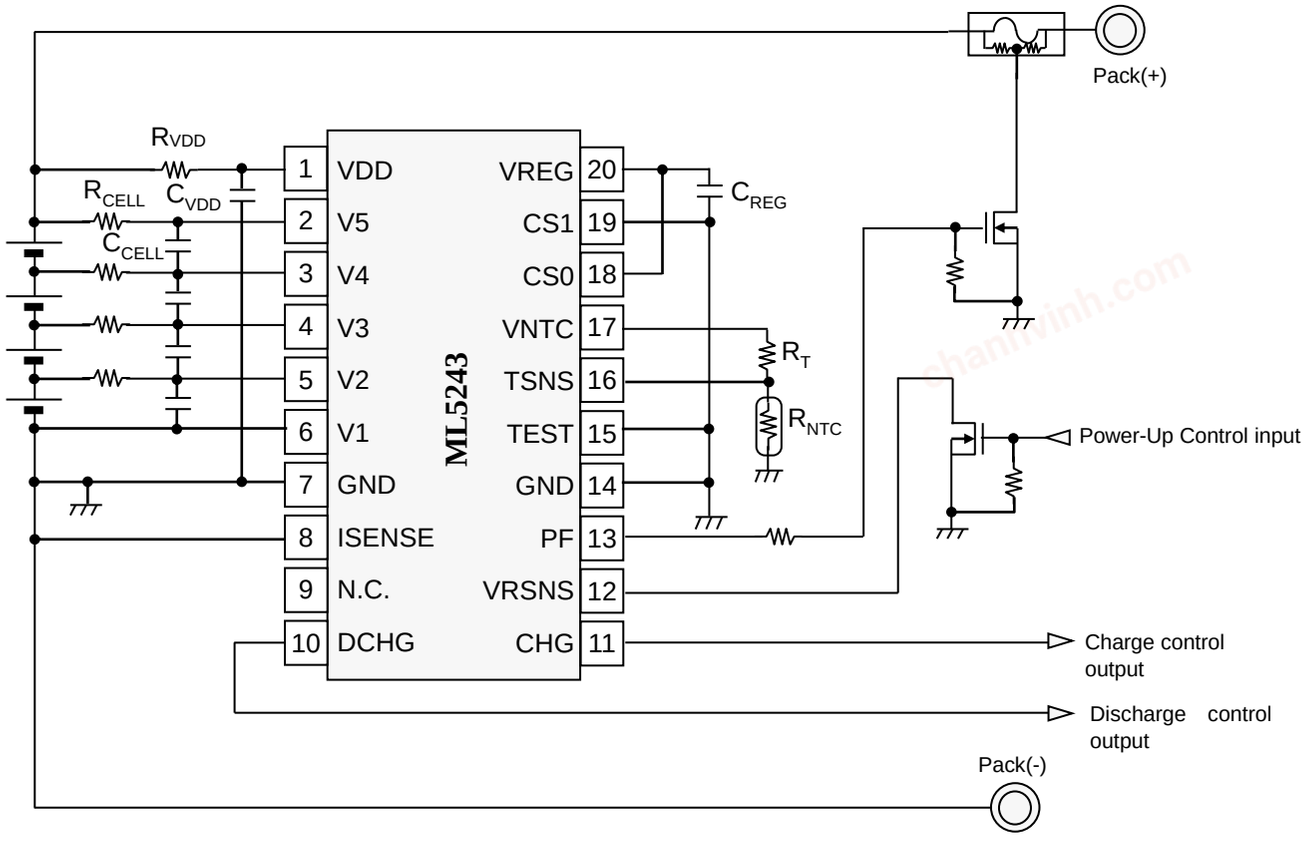
Component	Recommended value
R_{VDD}	1.5kΩ
C_{VDD}	2.2 µF
R_{CEL}	1 kΩ to 10 kΩ
C_{CEL}	0.1 µF or more
C_{REG}	1 µF
R_S	1 mΩ
R_{IS}	1 kΩ

Component	Recommended value
C_{IS}	0.01 µF
R_T	4.7 kΩ
R_{NTC}	10 kΩ, B3435
R_G	10 kΩ
R_{GS}	1 MΩ
R_{VR}	1 kΩ

(Note) This circuit example and the recommended values of external components are not always warranted. Evaluation on customer's application is required and select circuit and parts depend on customer's application.

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■ Application Circuit Example 2 (4-cell system, overcurrent is not implemented)



■Recommended Values for External Components

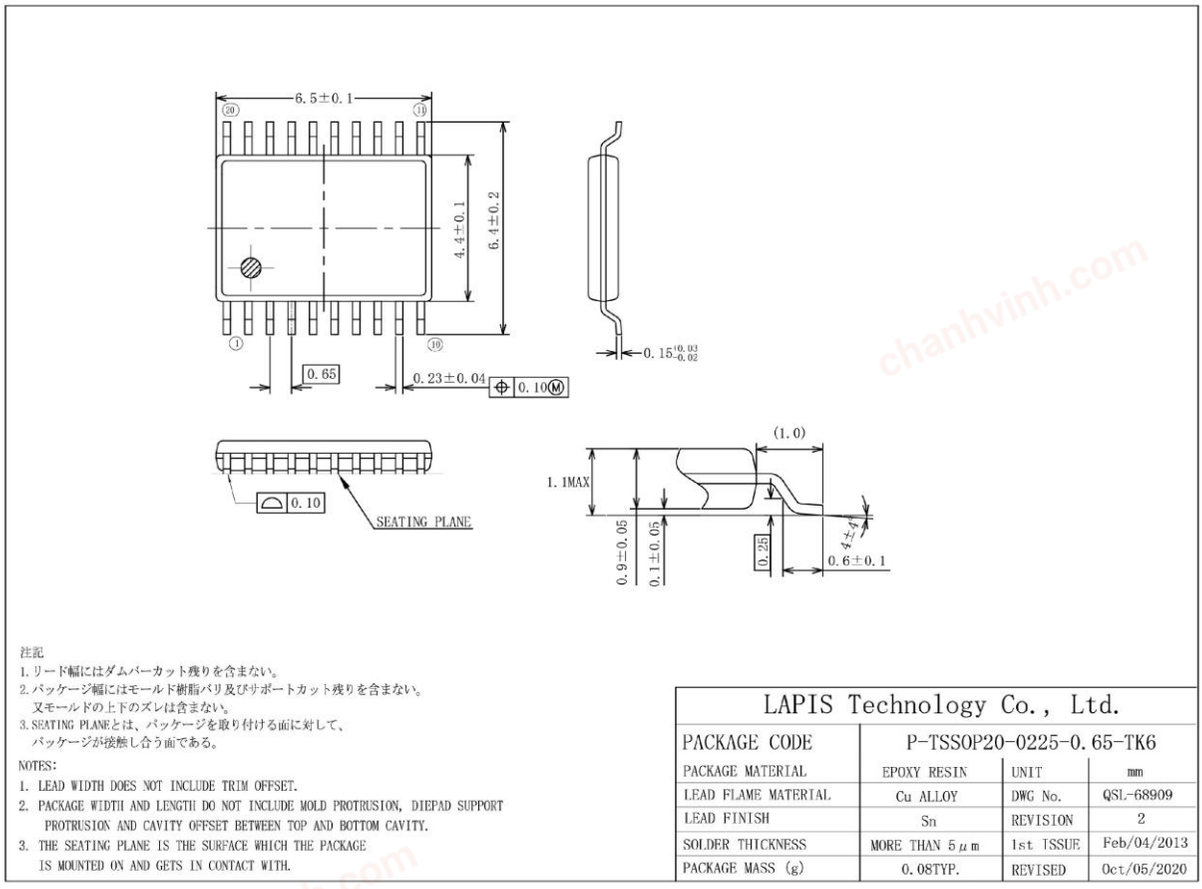
Component	Recommended value
R_{VDD}	1.5kΩ
C_{VDD}	2.2 µF
R_{CEL}	1 kΩ to 10 kΩ
C_{CEL}	0.1 µF or larger
C_{REG}	1 µF

Component	Recommended value
R_T	4.7 kΩ
R_{NTC}	10 kΩ, B3435

(Note) This circuit example and the recommended values of external components are not always warranted. Evaluation on customer's application is required and select circuit and parts depend on customer's application.

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■ Package Dimensions



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

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PACKAGE CODE	P-TSSOP20-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68909
LEAD FINISH	Sn	REVISION	2
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Feb/04/2013
PACKAGE MASS (g)	0.08TYP.	REVISED	Oct/05/2020

Caution regarding surface mount type packages

Surface mount type packages are susceptible to heat applied in solder reflow and moisture absorbed during storage. Please contact your local ROHM sales representative for recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

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■ Revision History

Document No.	Issue date	Page		Revision description
		Before revision	After revision	
FEDL5243-01	8, March. 2019	-	-	First edition.
FEDL5243-02	19, June. 2019	15	15	overvoltage is corrected to undervoltage
		25	25	R_T=1kΩ is corrected to 4.7kΩ
FEDL5243-03	2, August. 2019	18	18	CHG pin status in Open-wire state, mistype is corrected, “L” to “Hi-Z”.
		23	23	Open-wire detection/release delay time, mistype is corrected “2 to 4 ” to “3 to 4 cycles”.
FEDL5243-04	1, Dec. 2020	-	-	Changed Company name
		28	28	Changed “Notes”
FEDL5243-05	Jan. 9, 2024	1	1	Add Application Part number
		28	28	Add Notes

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Notes

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