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Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

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ML5232

Overvoltage Protector for 14-Series Cell Li-ion Rechargeable Batteries

■ General Description

The ML5232 is an overvoltage protection IC for 14-series-cell Li-ion rechargeable battery packs. It asserts the "L" level on the N-channel open drain alarm output and the "H" level on the CMOS alarm output if overvoltage condition is detected on any single cell.

■ Features

- 14-series-cell high-precision overvoltage detection
  Individual cell monitoring performed
  Fewer cells supported by shorting cell inputs.
  Overvoltage detection threshold/accuracy : 4.35 V ±20 mV (max)
  Overvoltage release threshold/accuracy : 3.90 V ±30 mV (max)
- Integrated detection delay timer
  Overvoltage detection delay : 2 sec
  Overvoltage release delay : 0.2 sec
  Overvoltage detection and release delays are reduced to 0.1 sec in the customer test mode
- Dual overvoltage alarm outputs
  Both the OVN pin (N-channel open-drain) and the OV pin (CMOS) are available for overvoltage alarm output
- Externally-controlled overvoltage alarm
  OVN and OV alarms enabled by the CTRL pin input
- Variety of overvoltage thresholds and detection delays can be redefined and supplied as code products
- Low current consumption
  Normal operation state : 2.5 µA (typ), 8µA (max)
  Overvoltage state : 4.5 µA (typ), 15µA (max)
- Supply voltage : +7 V to +80 V
- Operating temperature : -40 °C to +105 °C
- Package : 20-pin TSSOP

■ Application

- Power tools and Garden tools
- Cordless Cleaner
- E-Bike and Electric assisted bicycle
- Uninterruptible Power Supplies (UPS)
- Energy Storage Systems (ESS)

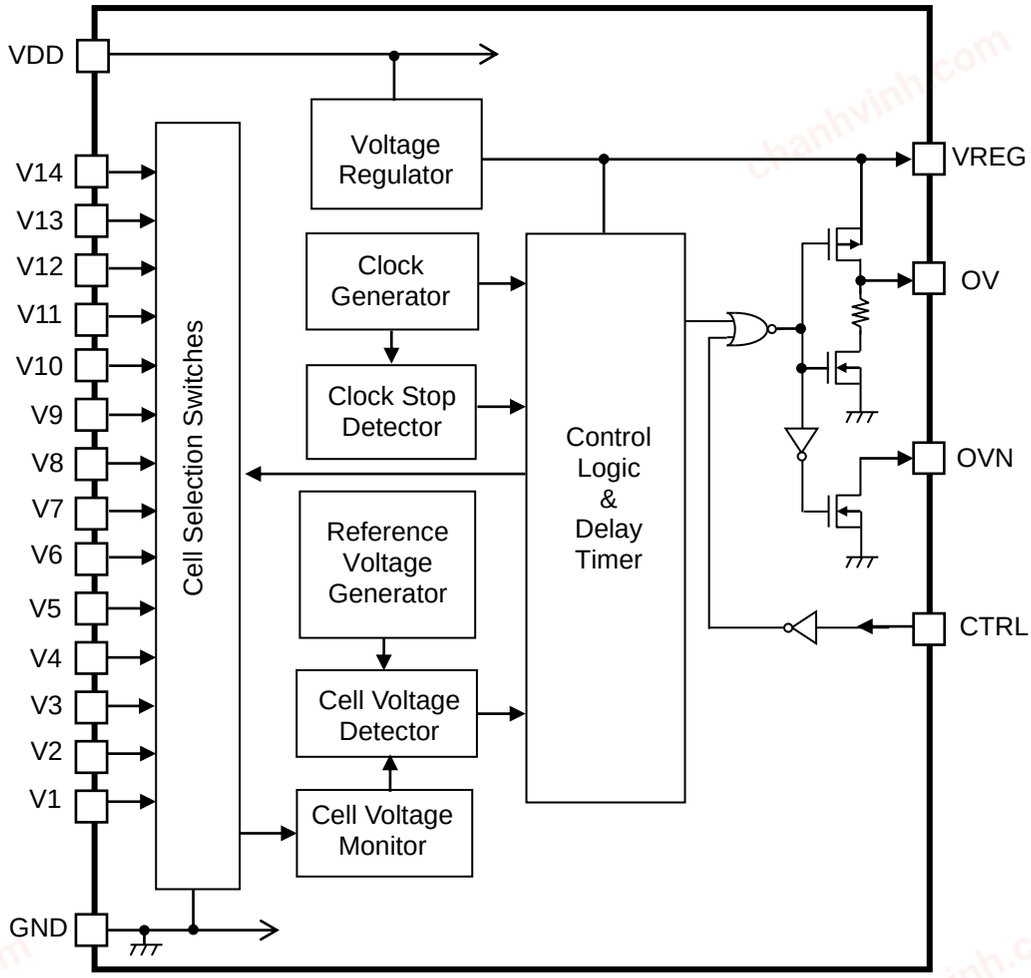
■ Part number

ML5232-001TD

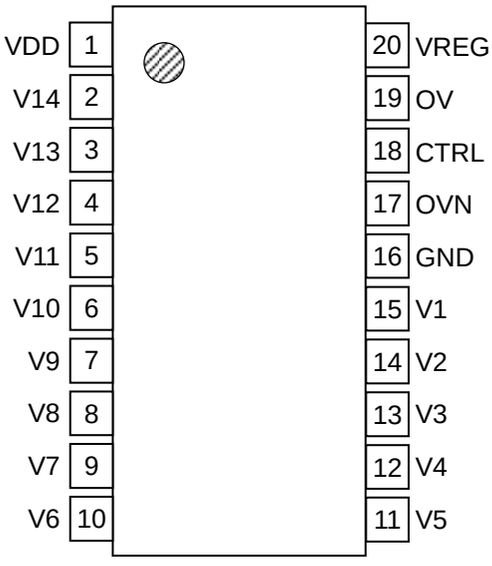
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■ Block Diagram



■ Pin Configuration (Top View)



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■ Pin Description

Pin No.	Pin name	I/O	Description
1	VDD	—	Power supply pin. Configure an external CR noise filter.
2	V14	I	Cell 14 positive input pin.
3	V13	I	Cell 14 negative input and Cell 13 positive input pin.
4	V12	I	Cell 13 negative input and Cell 12 positive input pin.
5	V11	I	Cell 12 negative input and Cell 11 positive input pin.
6	V10	I	Cell 11 negative input and Cell 10 positive input pin.
7	V9	I	Cell 10 negative input and Cell 9 positive input pin.
8	V8	I	Cell 9 negative input and Cell 8 positive input pin.
9	V7	I	Cell 8 negative input and Cell 7 positive input pin.
10	V6	I	Cell 7 negative input and Cell 6 positive input pin.
11	V5	I	Cell 6 negative input and Cell 5 positive input pin.
12	V4	I	Cell 5 negative input and Cell 4 positive input pin.
13	V3	I	Cell 4 negative input and Cell 3 positive input pin.
14	V2	I	Cell 3 negative input and Cell 2 positive input pin.
15	V1	I	Cell 2 negative input and Cell 1 positive input pin.
16	GND	—	Ground pin.
17	OVN	O	High voltage N-channel open drain output for overvoltage alarm. Hi-Z output in normal state and "L" level output in the overvoltage state.
18	CTRL	I	High voltage CMOS input for controlling OVN and OV status. Assert "L" level to emulate the overvoltage state. Tied to "H" level (VDD level) in the normal state.
19	OV	O	Regular voltage CMOS output for overvoltage alarm, internally pulled down with a 25 kΩ resistor. “L” level output in normal state and "H" level (VREG level) output in the overvoltage state.
20	VREG	O	Integrated 4.3 V regulator output. Tied to GND through a 0.1 μF or larger capacitor. Do not supply power to external circuits.

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■ Absolute Maximum Ratings

GND= 0 V, Ta = 25 °C

Item	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	Applied to VDD pin	-0.3 to +86.5	V
Input voltage	V_{IN1}	Applied to V14 to V1 pins	-0.3 to V_{DD}+0.6	V
	V_{IN2}	Applied to CTRL pin	-0.3 to +86.5	V
Output voltage	V_{OUT1}	Applied to OVN pin	-0.3 to +86.5	V
	V_{OUT2}	Applied to OV pin	-0.3 to V_{REG}+0.3	V
	V_{OUT3}	Applied to VREG pin	-0.3 to +6.5	V
Power dissipation	P_D	—	1.0	W
Short-circuit output current	I_{OS}	Applied to OV, OVN, and VREG pins	10	mA
Storage temperature	T_{STG}	—	-55 to +150	°C

■ Recommended Operating Conditions

GND= 0 V

Item	Symbol	Conditions	Range	Unit
Supply voltage	V_{DD}	Applied to VDD pin	7 to 80	V
Operating temperature	T_{OP}	—	-40 to +105	°C

■ Electrical Characteristics

● DC Characteristics

V_{DD}=7 V to 80 V, GND=0 V, Ta=-40 to +105 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CTRL pin "H" input voltage	V_{IH}	—	0.8×V_{DD}	—	V_{DD}	V
CTRL pin "L" input voltage	V_{IL}	—	0	—	0.2×V_{DD}	V
CTRL pin "H" input current	I_{IH}	V_{IH} = V_{DD}	—	—	5	µA
CTRL pin "L" input current	I_{IL}	V_{IL} = GND	–5	—	—	µA
Cell monitor pins V14 to V1 input current	I_{INVC}	Average current during normal operation	–0.1	0.1	3	µA
OVN pin "L" output voltage	V_{OL}	I_{OL} = 100 µA	—	—	0.2	V
OVN pin output leakage current	I_{OLK}	V_{OUT}= 0 V to 80 V	–5	—	5	µA
OV pin "H" output voltage	V_{OH}	I_{OH} = -100 µA	V_{REG}-0.2	—	V_{REG}	V
OV pin pull-down resistance	R_{PD}	V_{OL}=1V	10	25	40	kΩ
VREG pin output voltage	V_{REG}	VDD=7V to 64V With a 0.5mA or less load current	3.8	4.3	4.8	V

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- Supply Current Characteristics

V_{DD}= 7 V to 64 V, GND=0 V, Ta=-40 to +105 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption not in overvoltage state	I_{DD1}	No output load Ta = -40 to 60°C	—	2.5	6	µA
	I_{DD1T}	No output load		2.5	8	µA
Current consumption in overvoltage state	I_{DD2}	No output load	—	4.5	15	µA

- Detection Threshold Characteristics (Ta = 25 °C)

V_{DD}=56 V, GND=0 V, Ta=+25 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Overvoltage threshold	V_{OV}	—	4.33	4.35	4.37	V
Overvoltage release threshold	V_{OVR}	—	3.87	3.90	3.93	V
V14 pin activation threshold	V_{CON}	V14-to-V13 voltage	1.5	2.0	2.5	V

- Detection Threshold Characteristics (Ta = 0 to 60 °C)

V_{DD}=56 V, GND=0 V, Ta=0 to 60 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Overvoltage threshold	V_{OV}	—	4.325	4.350	4.375	V
Overvoltage release threshold	V_{OVR}	—	3.85	3.90	3.95	V
Low VREG threshold	V_{UREG}	—	3.0	3.4	3.8	V
VREG recovery threshold	V_{RREG}	—	3.4	3.8	4.2	V

- Detection Threshold Characteristics (Ta = 105 °C)

V_{DD}=56 V, GND=0 V, Ta=105 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Overvoltage threshold	V_{OV}	—	4.30	4.35	4.40	V
Overvoltage release threshold	V_{OVR}	—	3.8	3.9	4.0	V

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● Detection Delay Time Characteristics (Ta = 25 °C)

V_{DD}=56 V, GND=0 V, Ta=+25 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Overvoltage detection delay time (Note)	t_{OV}	—	1.7	2.0	2.4	sec
Overvoltage release delay time (Note)	t_{OVR}	—	0.16	0.2	0.24	sec
Cell voltage monitor cycle	t_{DET1}	During normal state	320	400	480	ms
	t_{DET2}	During overvoltage state	80	100	120	ms
Overvoltage detection delay in quick test mode (Note)	t_{OVT}	—	80	100	120	ms
Overvoltage release delay in quick test mode (Note)	t_{OVRT}	—	80	100	120	ms
Quick test mode transition time	t_{TST}	—	15	25	35	ms

(Note) The actual overvoltage detection and release delays may include the time lag incorporated by the cell voltage monitor cycle.

● Detection Delay Time Characteristics (Ta = 0 to 60 °C)

V_{DD}=56 V, GND=0 V, Ta=0 to 60 °C

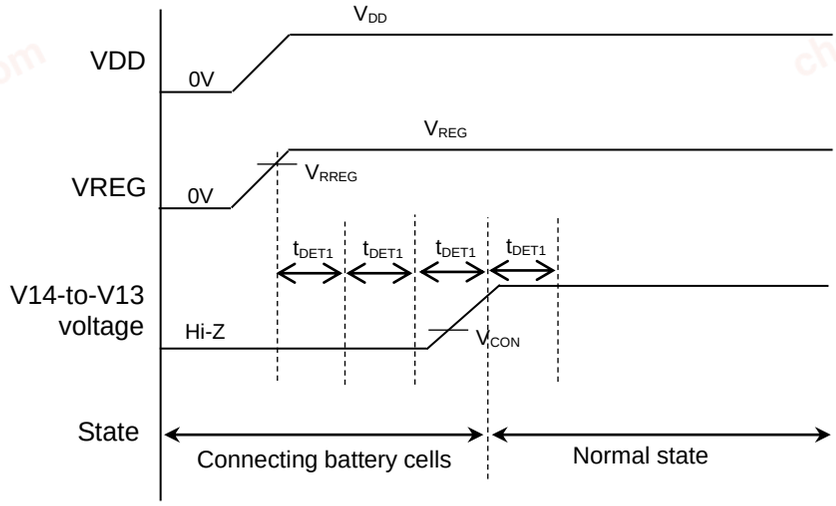
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Overvoltage detection delay (Note)	t_{OV}	—	1.6	2.0	2.5	sec
Overvoltage release delay (Note)	t_{OVR}	—	0.14	0.2	0.26	sec
Cell voltage monitor cycle	t_{DET1}	During normal state	300	400	500	ms
	t_{DET2}	During overvoltage state	75	100	125	ms

(Note) The actual overvoltage detection and release delays may include the time lag incorporated by the cell voltage monitor cycle.

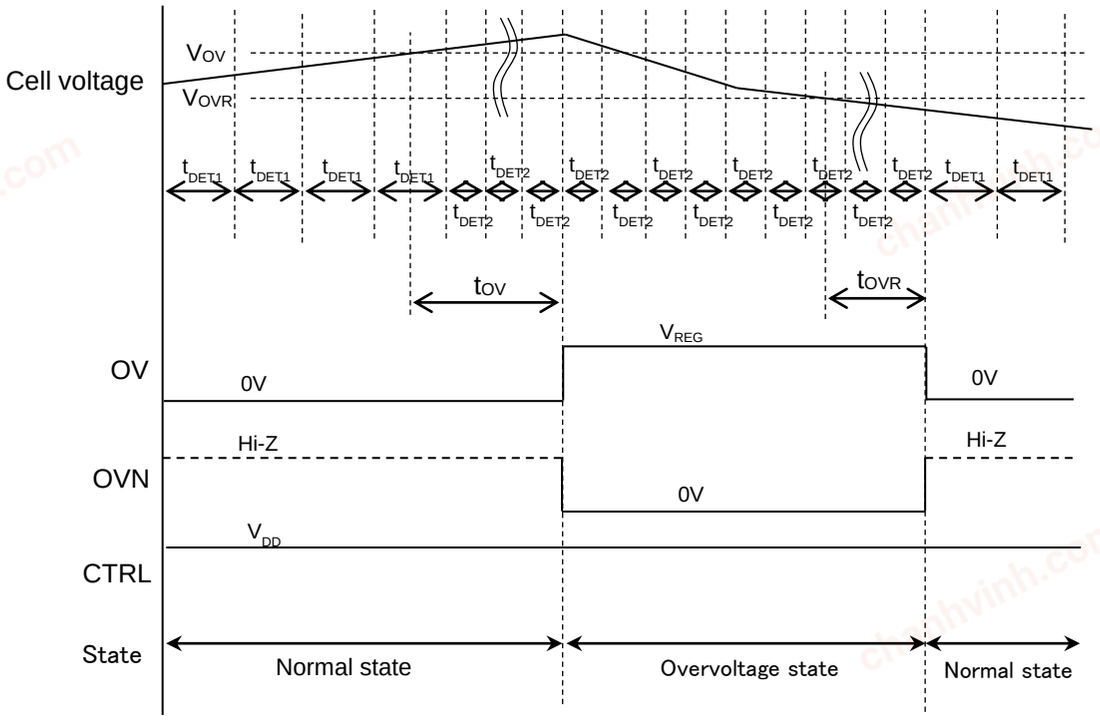
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■ Timing Diagrams

● During Battery Cell Connection

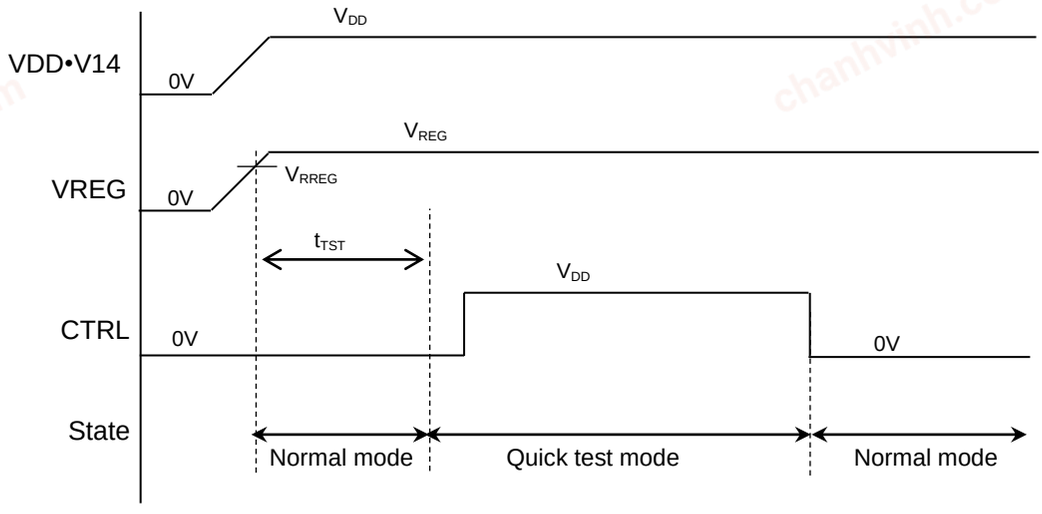


● Overvoltage Detection and Release



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- Transition to and Return from Quick Test Mode



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■ Functional Description

● Selecting Cell Count in the Battery Pack

If the serial cell count is fewer than 14, Vn pins from V1 to upward are not used. All unused pins should be tied to GND.

● OV and OVN state control with CTRL Pin

The “L” level input on the CTRL pin emulates the overvoltage state.
The following table shows the OV and OVN pin output states depending on the CTRL level.

CTRL pin input	OV pin output	OVN pin output	Remarks
"L" level	"H" level (4.3 V)	"L" level (0 V)	Overvoltage state
"H" level	"L" level (25 kΩ pull-down)	"Hi-Z" level	Normal state

● Handling VDD and V1 to V14 Pins

Since the VDD pin is power supply input, configure a noise elimination RC filter circuit in front of the VDD input for stabilization.
The V1 to V14 pins are the monitor pins for individual cell voltages. Configure a noise elimination RC filter circuit in front of each cell voltage input to prevent a false detection. All unused Vn pins should be tied to GND in battery packs with fewer than 14 cells.

● Handling VREG Pin

The VREG pin is the output pin of the internal regulator and also sources power to internal circuits. Connect a 0.1 µF or larger capacitor between this pin and GND for stabilization. Do not source power to external circuits since its current supply capacity is limited.

● Unused Pins Treatment

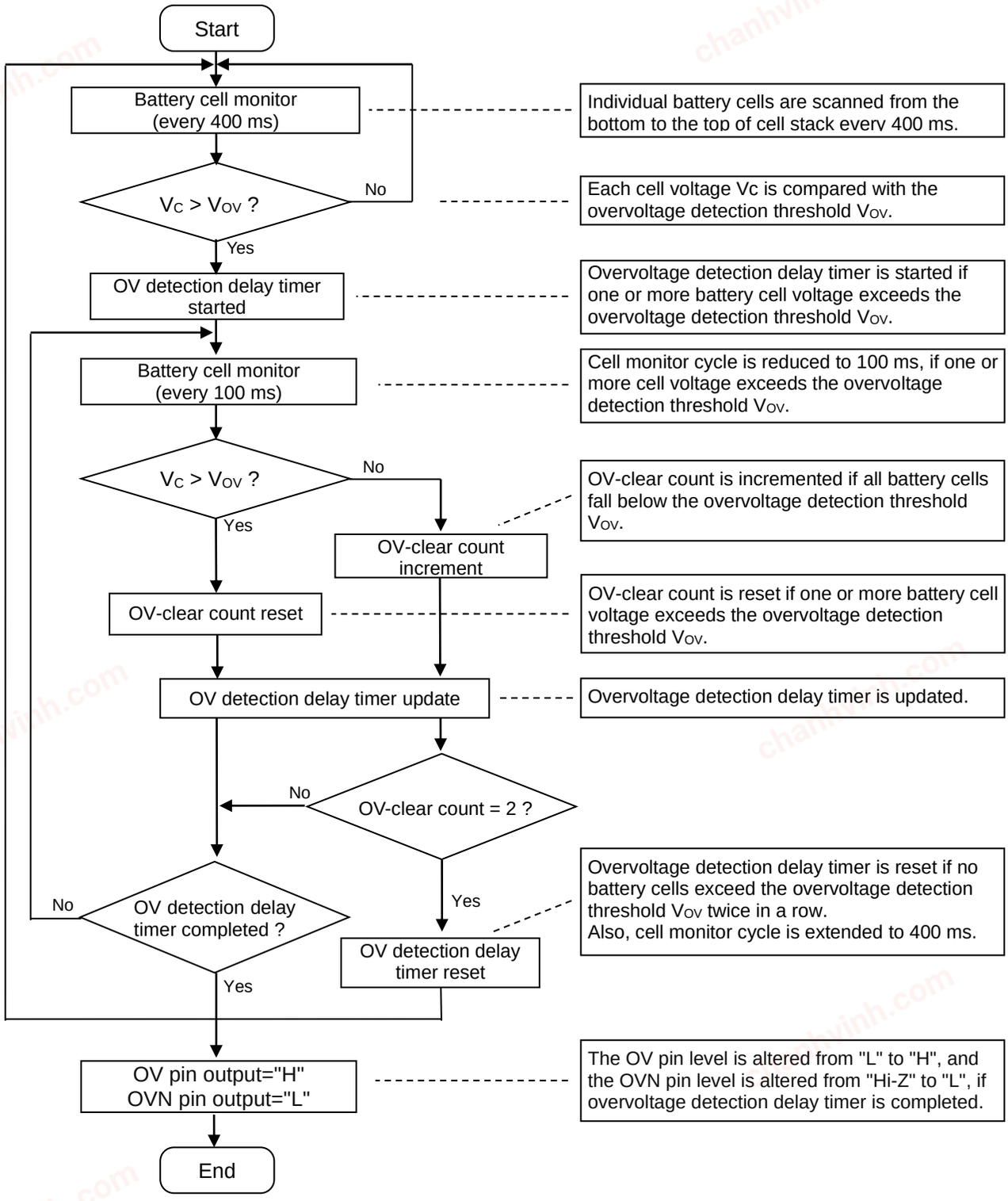
Unused pins should be handled according to the following table.

Unused pins	Recommended treatment
Vn	Connected to GND
CTRL	Connected to VDD
OV	Open
OVN	Open

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- Overvoltage Detection Flow

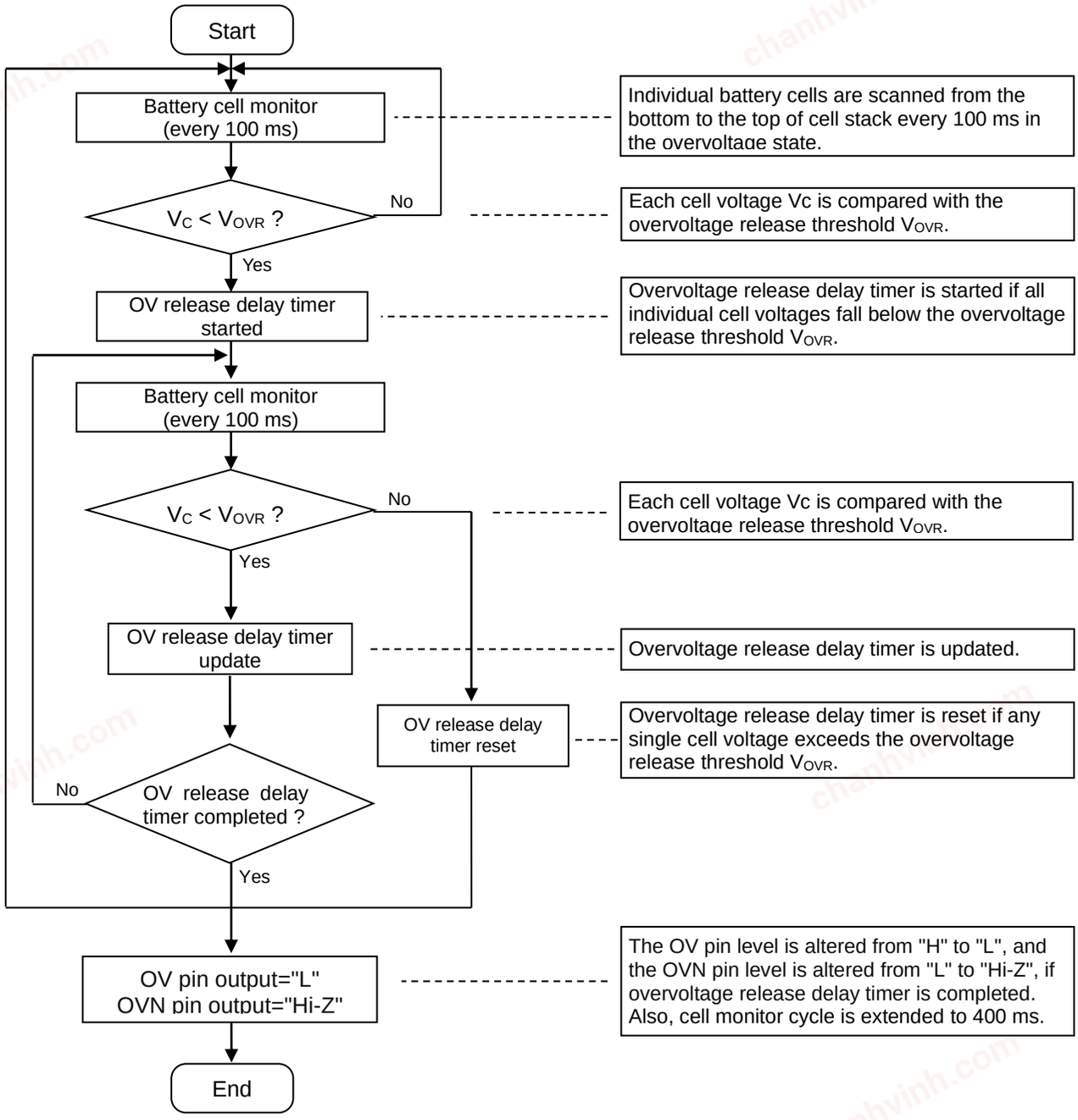
Below is the operation flow chart at overvoltage detection.
Normal state (not in overvoltage state) is assumed initially.



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- Overvoltage Release Flow

Below is the operation flow chart at overvoltage release.
Overvoltage state is assumed initially.



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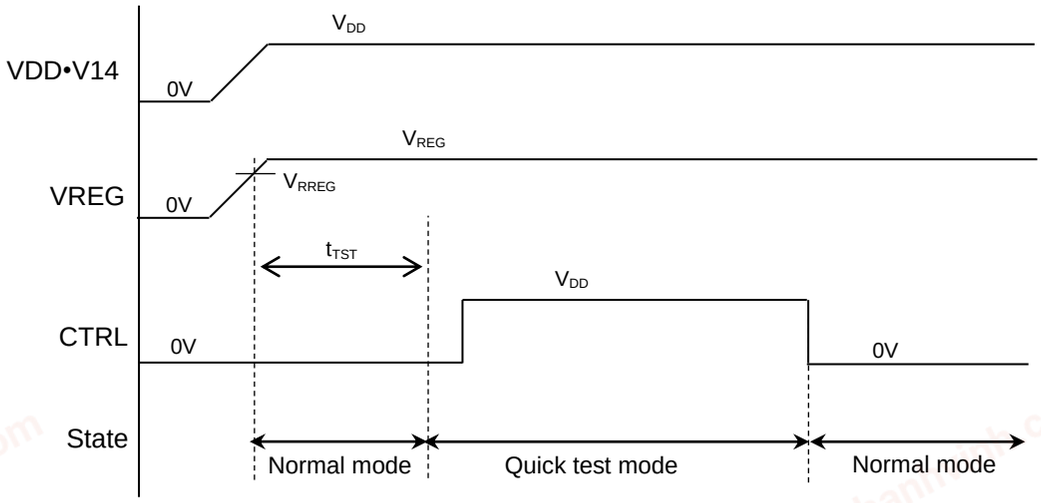
- V14-to-V13 Level Check

The voltage between the V14 and V13 pins is analyzed to avoid false overvoltage alarm during battery cell assembly. Individual cell voltage monitoring is performed every 400 ms, when the VREG output voltage exceeds the VREG recovery threshold V_{RREG}.

If the V14-to-V13 level is below the V14 activation threshold V_{CON}, overvoltage detection is overridden, ignoring all overvoltage conditions. When the V14-to-V13 level exceeds the V14 activation threshold V_{CON}, overvoltage alarm is triggered normally.

- Reduced Cell Monitoring Cycle and Overvoltage Detection/Release Delays

The quick test mode is provided in which cell monitor cycle, overvoltage detection delay, and overvoltage release delay are reduced to 100 ms (typ).
To enter the quick test mode, assert "L" on the CTRL pin while power is turned on and keep it for longer than the quick test mode transition time t_{TST} after the VREG output level has reached the VREG recovery threshold V_{RREG}. To exit the quick test mode, assert “H” on the CTRL pin and then pull it to "L".
The quick test mode can significantly reduce the production test time for the assembled modules.



- Power-on/Power-off Sequence

Battery cells can be connected in any order, but the recommended connection sequence is to start with the GND and VDD pins, followed by Vn pins from the bottom to the top of the cell stack.
If cell connection is not completed within overvoltage detection delay t_{OV}, the overvoltage state may be detected. To avoid such false detection, overvoltage detection is performed only after the V14-to-V13 level reaches the V14 active threshold V_{CON}. Therefore the V14 pin should be connected in the last step of pack assembly. Likewise, if the V14 pin stems from the VDD pin via a resistor, the highest battery cell (the V14 and VDD pins) should be connected at the end.
There are no restrictions on the power supply voltage rise time at power-on, power-off sequence, and power supply voltage fall time at power-off.

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Overvoltage Detection and Release Threshold Options

Overvoltage detection and release thresholds can be defined according to the range and step specified in the following table. Some combinations are unavailable due to conflicts. Contact us for details.

Detecting voltage	Range	Step voltage
Overvoltage detection threshold	4.0 V to 4.4 V	25 mV
Overvoltage release threshold	3.6 V to 4.0 V	100 mV

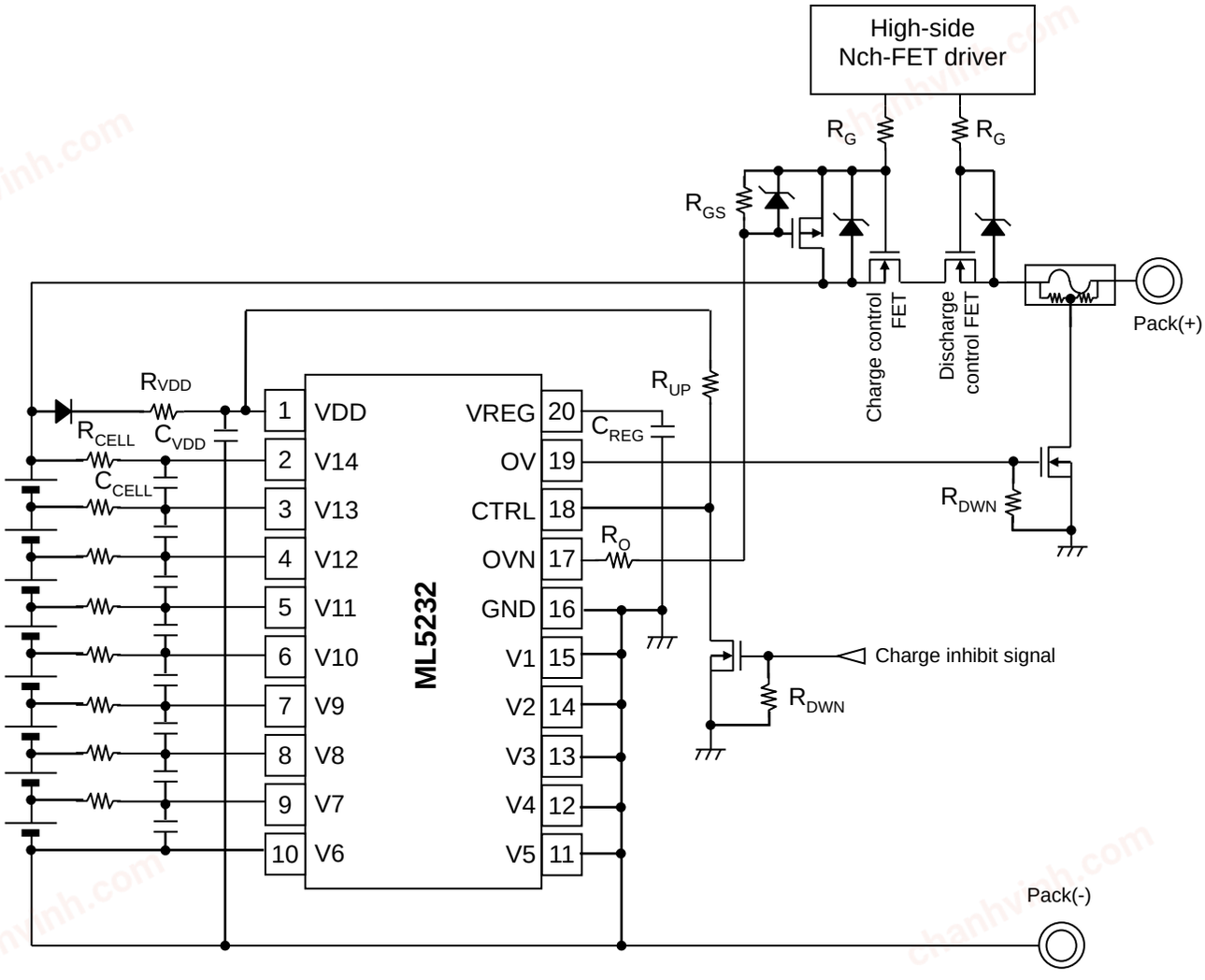
Overvoltage Detection and Release Delay Options

Overvoltage detection and release delays can be selected from the values in the following table.

Delay time	Configurable delay					Unit
Overvoltage detection delay	1	2	3	4	5	sec
Overvoltage release delay	0.2	0.4	0.6	0.8	1	sec

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■ Application Circuit Example (8-cell system)



■ Recommended Values for External Components

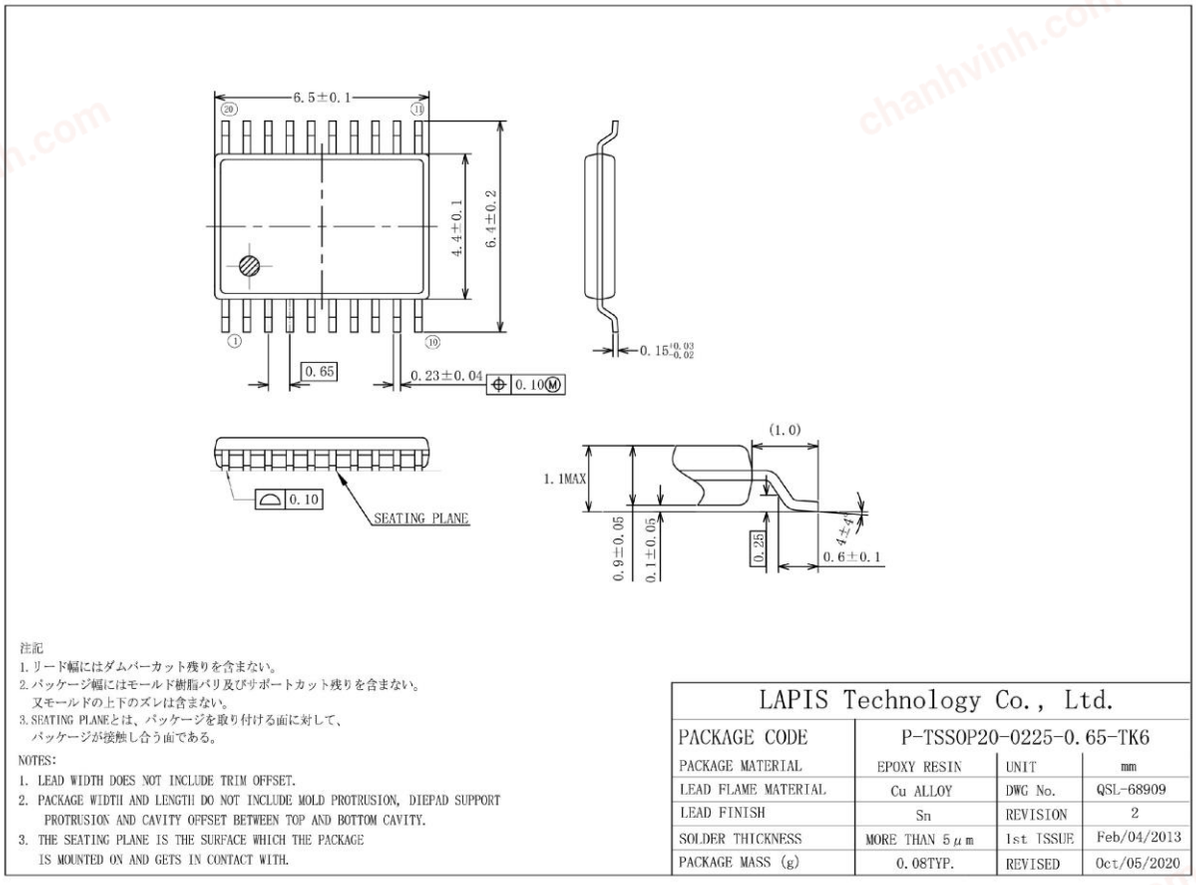
Component	Recommended value
R_{VDD}	1 kΩ to 2 kΩ
C_{VDD}	0.1 µF or more
R_{CEL}	1 kΩ to 10 kΩ
C_{CEL}	0.1 µF or more
C_{REG}	0.1 µF or more

Component	Recommended value
R_O	1 MΩ
R_{UP} ,R_{DWN}	100 kΩ
R_{GS}	1 MΩ
R_G	1 kΩ

(Note) The circuit examples and recommended values of external parts provided here do not guarantee the device performance under all conditions. Full and detailed evaluations are suggested on your actual applications before deciding your circuits and part constants.

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■ Package Dimensions



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

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PACKAGE CODE	P-TSSOP20-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68909
LEAD FINISH	Sn	REVISION	2
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Feb/04/2013
PACKAGE MASS (g)	0.08TYP.	REVISED	Oct/05/2020

Caution regarding surface mount type packages

Surface mount type packages are susceptible to applied heat in solder reflow or moisture absorption during storage. Please contact your local ROHM sales representative for the recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

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■ Revision History

Document No.	Issue date	Page		Revision description
		Before revision	After revision	
FEDL5232-01	Sep 6, 2016	-	-	1st edition issued
FEDL5232-02	Dec. 1, 2020	-	-	Changed Company name
		17	17	Changed “Notes”
FEDL5232-03	Jan. 9, 2024	1	1	Add Application Part number, Delete notes
		17	17	Add Notes

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https://www.lapis-tech.com/en/

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