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Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology" and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

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ML5206

5 series Cell Li-ion Rechargeable Battery Protection IC with cell balancing function

■ General Description

The ML5206 is a protection IC with cell balancing funcion for the 3- to 5-cell Li-ion rechargeable battery pack. It detects individual cell overvoltage and battery cell open-wire, and alerts by alarm output signal. And cell balancing function is built in and it is automatically executed.

■ Features

- 3 to 5 cell high precision overvoltage detection function
  - Overvoltage detection threshold V_{OV} : 4.0V to 4.4V (5mV step), error: ±25mV (0°C to 60°C)
  - Overvoltage release threshold V_{OVR} : VOV - 0 to 200mV (10mV step)
    error: ±25mV to 35mV (0°C to 60°C)
  - Overvoltage detection delay time : 0sec to 5.6 sec(typ)

- Open-wire detection function
  - Open-wire detection threshold : 0.6V(typ)
  - Open-wire detection sink current : 100nA(typ)
  - Open-wire detection delay time : 0sec to 5.6sec(typ)

- Cell balancing function
  - Cell balancing detection threshold V_{CB} : 4.0V to 4.4V (5mV step), error: ±25mV (0°C to 60°C)
  - Cell balancing relase threshold V_{CBR} : VCB - 0 to 200mV (10mV step),
    error: ±25mV ot 35mV (0°C to 60°C)
  - Cell balancing current : 40mA(typ)
  - Cell balancing detection delay time : 0sec to 5.6sec(typ)

- 3 types of alarm output
  Selected from CMOS / Nch open drain / Pch open drain

- Setting number of connected battery cells : defined with part-number
  5 cells = ML5206-001, 4 cells =ML5206-001A, 3 cells=ML5206-001B

- Low current consumption
  1μA(typ), 2μA(max) (0°C to 60°C)

- Power supply voltage : +5V to +25V

- Operating temperature : -20°C to +85°C

- Package : 8 pin VSSOP

■ Application

・Power tools and Garden tools
・Cordless Cleaner

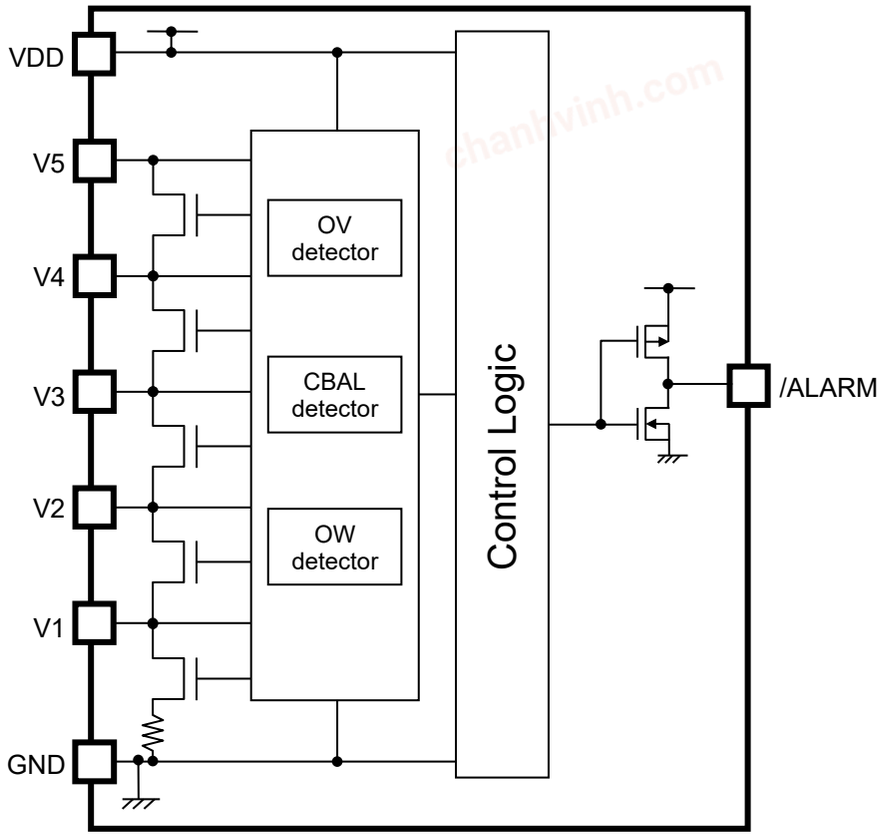
■ Part number

ML5206-001MB 5 cells, Nch open drain output
ML5206-001BMB 3 cells, Nch open drain output
The detection voltage, etc., is the same for both 5 cells and 3 cells.

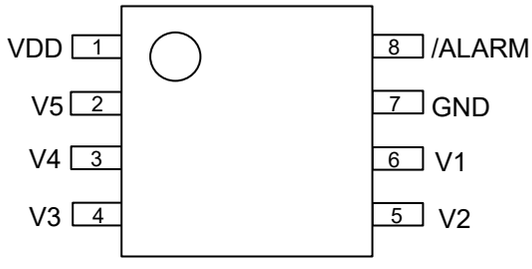
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■ Block Diagram



■ Pin Configuration (top view)



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■ Pin Description

Pin No.	Pin	I/O	Description
1	VDD	—	Power supply input pin.
2	V5	I	Battery cell 5 high voltage input pin
3	V4	I	Battery cell 5 low voltage input and Battery cell 4 high voltage input pin.
4	V3	I	Battery cell 4 low voltage input and Battery cell 3 high voltage input pin.
5	V2	I	Battery cell 3 low voltage input and Battery cell 2 high voltage input pin. Should be connected to GND for the 3 cell series connected battery pack application.
6	V1	I	Battery cell 2 low voltage input and Battery cell 1 high voltage input pin. Should be connected to GND for the 3 or 4 cell series connected battery pack application.
7	GND	—	Ground pin.
8	/ALARM	O	Alarm signal output pin. ・If CMOS output : Output level is ”L” level(GND level) if overvoltage/ open-wire is detected, else ”H” level (VDD power supply level). Its reversed setting is possible. ・If Nch open drain output : Output level is ”L” level(GND level) if overvoltage/ open-wire is detected, else ”Hi-Z” level. Its reversed setting is possible. ・If Pch open drain output： Output level is ”H”level (VDD power supply level) if overvoltage/open-wire is detected, else ”Hi-Z” level. Its reversed setting is possible.

■ Absolute Maximum Ratings

（GND= 0 V, Ta = 25 °C）

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Applied to VDD pin	−0.3 to +33	V
Input Voltage	V_{IN}	Applied to V5 to V1 pins Vn+1 –Vn pin voltage defference (note1) V1 – GND pin voltage difference	−0.3 to +6.5	V
	V_{IN2}	Applied to between V2-V1 pins. When cell balancing switch between V2-V1 pins is OFF.	−0.3 to +7.5	V
	V_{IN5}	Applied to V5 pin	−0.3 to + VDD + 6.5	V
Output Voltage	V_{OUT1}	Applied to /ALARM pin (CMOS, Pch open-drain)	−0.3 to V_{DD}+0.3	V
	V_{OUT2}	Applied to /ALARM pin (Nch open-drain)	−0.3 to +32	V
Cell balancing current	I_{CB}	Per every cellbalancing switch	100	mA
Short-circuit output current	I_{OS}	Applied to /ALARM pin	10	mA
Power dissipation	P_D	Mounted on the JEDEC 4-layer board	730	mW
Storage temperature	T_{STG}	—	−55 to +150	°C

(note 1) When connecting or disconnecting battery cells, the voltage difference between V_{n+1} - V_n pins might exceed this ratings and the LSI will be destructed.

■ Recommended Operating Conditions

（GND= 0 V）

Item	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	5 to 25	V
Operating temperature	T_{OP}	—	-20 to +85	°C

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■ Electrical Characteristics

● DC Characteristics

V_{DD}=5 to 25V, GND=0 V, Ta=-20 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V5 to V1 pins Open-wire detection sink current	I_{VCL}	Each cell voltage = 3.6V Ta=0 to 60°C	30	100	300	nA
/ALARM pin "H" output voltage	I_{OHA}	I_{OH}=-100µA	V_{DD}-0.2	—	V_{DD}	V
/ALARM pin "L" output voltage	V_{OLA}	I_{OL}=100µA	0	—	0.2	V
/ALARM pin Output leakage current	I_{OLKA}	Output state is Hi-Z	-2	—	2	µA
V5 to V2 pins Cell balance Switch ON resistance	R_{BL1}	Internal balance FET Vn+1 – Vn = 0.3V V_{DD} – V2 ≧ 6V V_{DD}=9V to 25V	3	6	12	Ω
V1 pin Cell balance Switch ON resistance	R_{BL2}	Internal balance FET V1=2.1V V_{DD}=9V to 25V	38	57	91	Ω

● Supply Current Characteristics

V_{DD}=5 to 25V, GND=0 V, Ta=-20 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}	Each cell voltage=3.6V No output load Ta=0 to 60°C	—	1	2	µA
	I_{DDT}	Each cell voltage=3.6V No output load Ta=-20 to 85°C	—	1	3	µA

(Note) VDD pin current consumption. V5 to V1 pin input current, /ALARM pin output current is not included.

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● Detection Threshold Chracteristics（Ta=0 to 60°C）

V_{DD}=18V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	V_{OV} -25mV	V_{OV}	V_{OV} +25mV	V
Overvoltage release threshold	V_{OVR}	V_{OV}-V_{OVR}≦50mV	V_{OVR} -25m	V_{OVR}	V_{OVR} +25m	V
		V_{OV}-V_{OVR}＞50mV	V_{OVR} -35m	V_{OVR}	V_{OVR} +35m	V
Cell balancing detection threshold	V_{CB}	—	V_{CB} -25mV	V_{CB}	V_{CB} +25mV	V
Cell balancing release threshold	V_{CBR}	V_{CB}-V_{CBR}≦50mV	V_{CBR} -25m	V_{CBR}	V_{CBR} +25m	V
		V_{B}-V_{CBR}＞50mV	V_{CBR} -35m	V_{CBR}	V_{CBR} +25m	V
Open-wire detection / release threshold	V_{OW}	—	0.5	0.6	0.7	V
Quick test mode transition VDD-V5 pin voltage difference	V_{TSTT}	Ta=25°C	10	—	—	V
Quick test mode release VDD-V5 pin voltage difference	V_{TSTR}	Ta=25°C	0	—	3	V

● Detection delay time characteristtics（Ta=0 to 60°C）

V_{DD}=18V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage monitoring cycle	t_{DET}	—	300	400	500	ms
Cell voltage monitoring term	t_{MON}	—	37	50	63	ms
Cell balancing term	T_{BAL}	—	262	350	438	ms
Overvoltage detection delay time setting range	t_{OV}	Defined with detection cycle	0	—	14	cycle
Cell balancing detection delay time setting range	t_{CB}	Defined with detection cycle	0	—	14	cycle
Open-wire detection/release delay time setting range	t_{OW}	Defined with detection cycle	0	—	14	cycle
Quick test mode Cell voltage monitoring cycle	t_{DETT}	Ta=25°C	75	100	125	ms
Quick test mode Cell balancing term	t_{BALT}	Ta=25°C	37	50	63	ms
Quick test mode Overvoltage detection delay time, Cell balancing detection delay time, open-wire detection/release delay time	t_{DLYT}	Defined with detection cycle	—	—	1	cycle

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● Code-001: Setting Parameters

V_{DD}=18V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	4.275	4.300	4.325	V
Overvoltage release threshold	V_{OVR}	—	4.165	4.200	4.235	V
Cell balancing detection threshold	V_{CB}	—	4.075	4.100	4.125	V
Cell balancing release threshold	V_{CBR}	—	4.075	4.100	4.125	V
Overvoltage detection delay time	t_{OV}	Defined with detection cycle	3	—	4	cycle
Cell balancing detection delay time	t_{CB}	Defined with detection cycle	1	—	2	cycle
Open-wire detection/release delay time	t_{OW}	Defined with detection cycle	1	—	2	cycle

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■ Functional Description

● Selecting the number of battery cells

Number of battery cells is determined by part number.
5-cells=ML5206-001, 4-cells=ML5206-001A, 3-cells=ML5206-001B

● /ALARM output pin

/ALARM pin output status for overvoltage/open-wire detected state.

	/ALARM pin output status		
	CMOS	Nch open drain (Code 001)	Pch open drain
Overvoltage/open-wire detected state	“L” level	“L” level	“H” level
Undetected state	“H” level	“Hi-Z” level	“Hi-Z” level

(note 1) /ALARM pin output status for detected state and undetected state can be reversed.

● Handling VDD pin and V1 to V5 pins

Since the VDD pin is the power supply input, put a noise elimination RC filter in front of the VDD input for stabilization. The resistor value of this noise filter should be adjusted so that the voltage drop across the resistor is smaller than 0.3 V.

The V1 to V5 pins are the monitor pins for individual cell voltages. Put a noise elimination RC filter in front of each battery cell to prevent false detection.

● Unused pin Treatment

The following table shows how to handle unused pins

Unused pins	Recommended treatment
V1 , V2	Connected to GND pin

● Power-on/Power-off sequence

Battery cells can be connected in any order, but it is recommend that the lowest voltage cell is connected first, and then connection continues from lower to higher voltage cells, and the highest voltage cell is connected last. There are no restrictions on the power supply voltage rise time at power-on, and power-off sequence or power supply voltage fall time at power-off.

It may transition to the open-wire or overvoltage detection state if it takes long time to connect all cells.

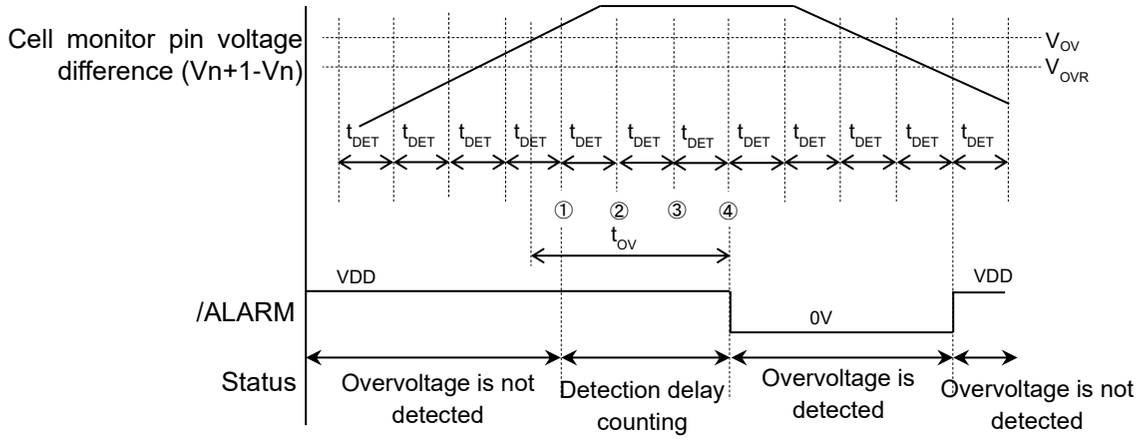
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● Overvoltage detection function (In case if the overvoltage detection delay time = 3 detection cycles)

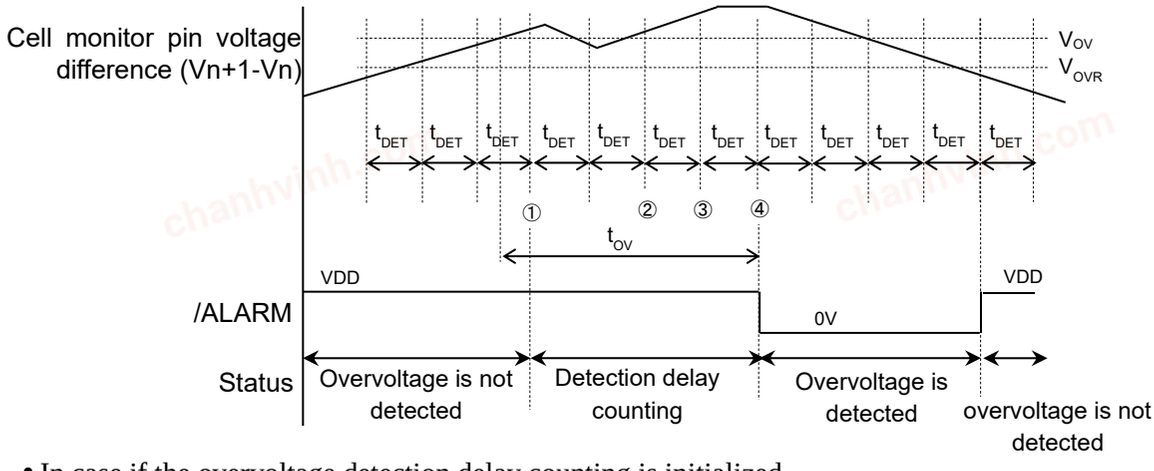
After power-on, cell voltage monitoring is started with cell voltage monitoring cycle of t_{DET} =400ms(typ). When any one or more battery cell voltages reach or exceed the overvoltage detection threshold V_{OV} for series four times, it detects overvoltage state. And if /ALARM pin output type is CMOS output, /ALARM pin output changes from "H" level to "L" level.

If the state in which cell voltage of all cell is lower than overvoltage detection threshold V_{OV} is detected once, detection delay time is not initialized. But if it is detected for series two times, detection delay time counting is initialized.

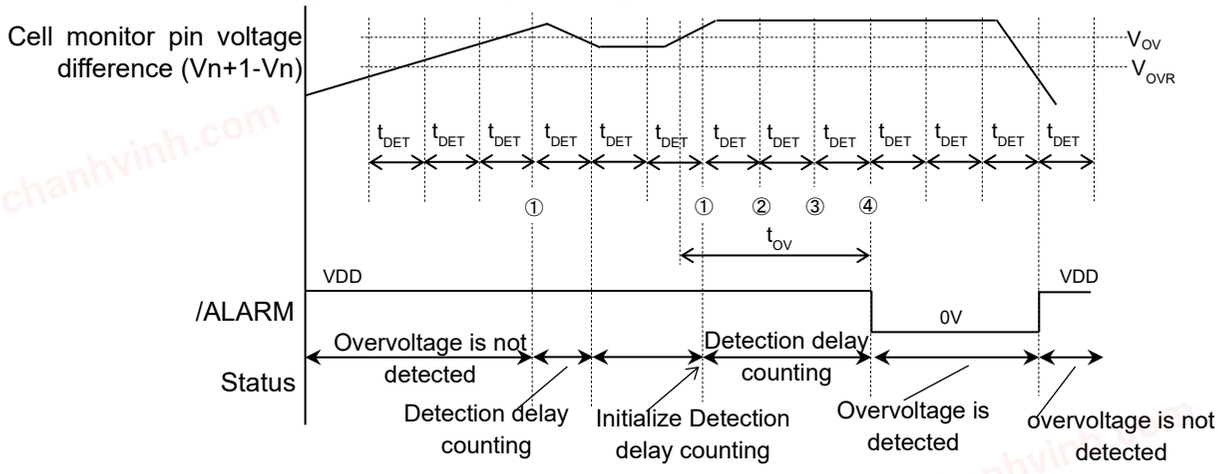
After the overvoltage detection, if the cell voltage of all cell is lower than overvoltage release threshold V_{OVR}, and if /ALARM pin output type is CMOS output, /ALARM pin output changes from "L" level to "H" level.



• In case if the overvoltage detection delay counting is not initialized



• In case if the overvoltage detection delay counting is initialized



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● Cell balancing function (In case if the cell balancing detection delay time = 1 detection cycle)

After power-on, cell voltage monitoring is started with cell voltage monitoring cycle of t_{DET}=400ms(typ).

When a cell voltage reach or exceed the cell balancing detection threshold V_{CB} for series two times, the cell balancing switch of the cell is turned on. Not more than one cell balancing switches are turned on in the same time, but only one cell balancing switche is turned on in the order of V1 to V5.

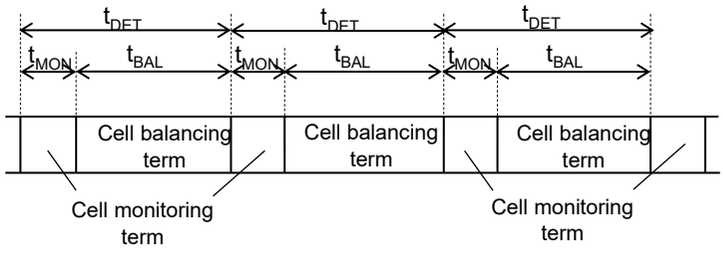
When a cell voltage of the cell reach or below the cell balancing detection threshold V_{CB} for one time, the detection delay time counting is initialized.

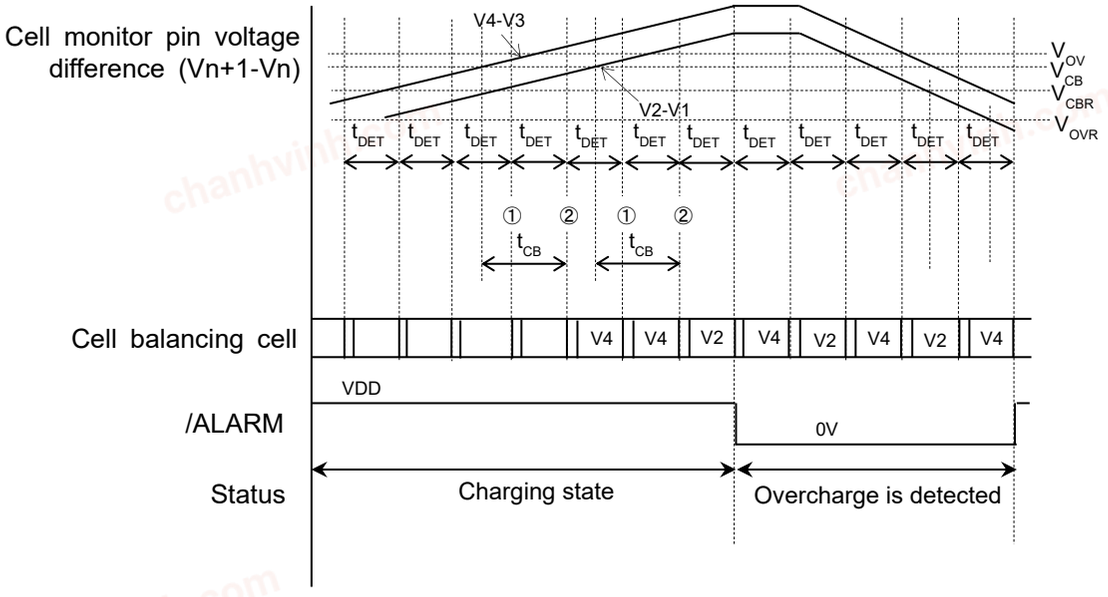
For monitoring the cell voltage, in the cell monitoring term t_{MON}=50ms(typ), cell balancing switch is automatically turned-off. The cell balancing switch is turned on during the call balancing term t_{BAL}=350ms(typ).

If the cell voltage of which cell balancing switch is turned-on is decrease below cell balance release voltage V_{CBR}, cell balancing switch is turned off.

This cell balancing is operated independently each other.

If the connected cells is less then five, the cell balancing term is as much as the connected cells.

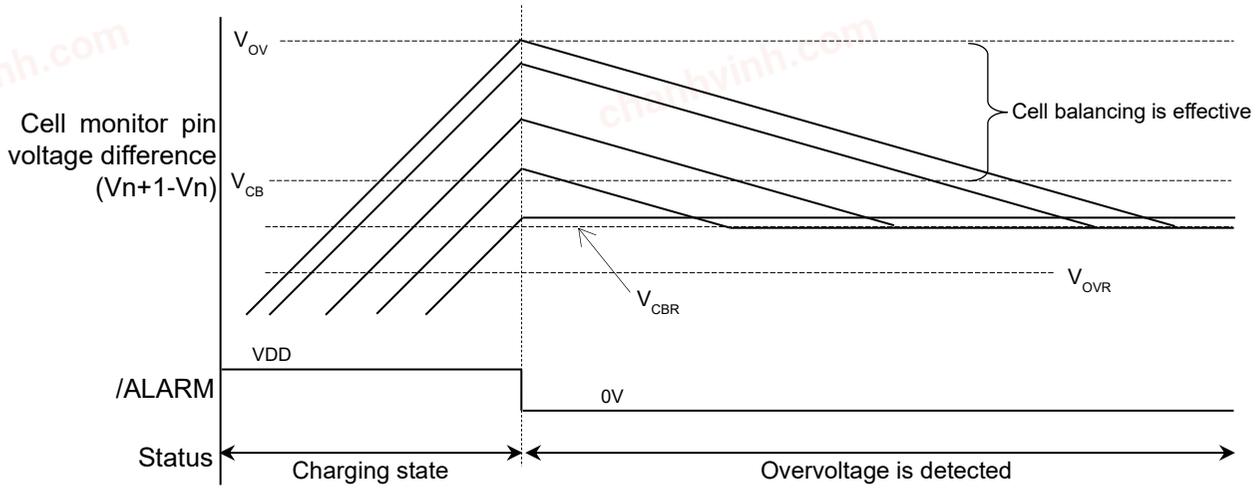




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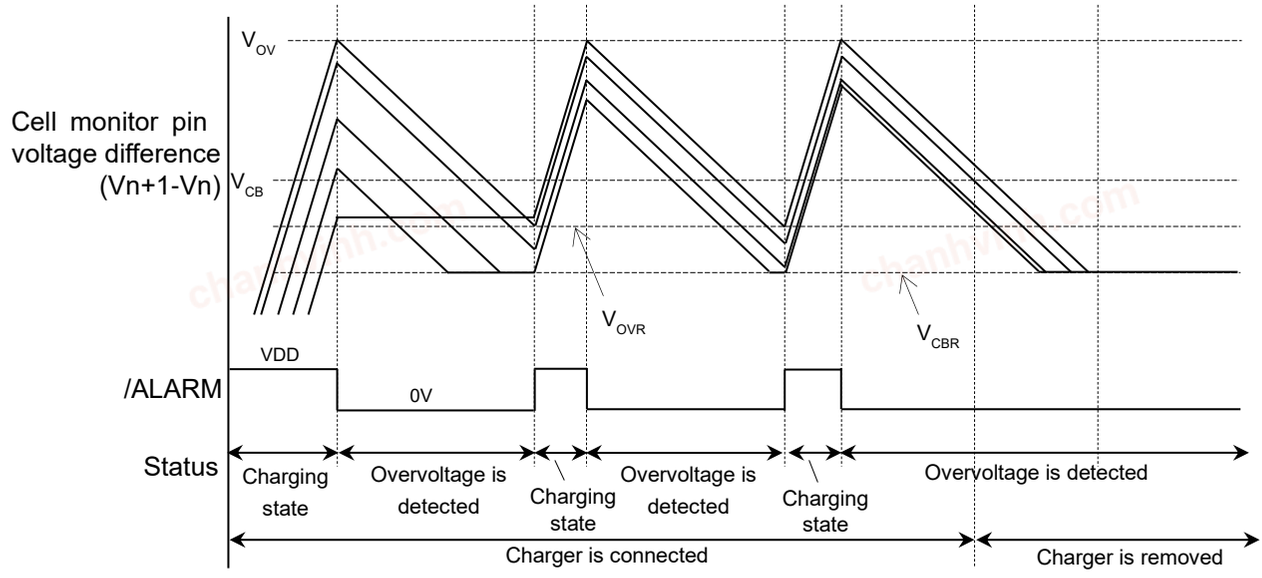
Cell balancing operation is shown below.

• In case if the cell balancing release threshold V_{CBR} > overvoltage release threshold V_{OVR}



Cell balancing is executed at cells whose voltage is between over voltage detection threshold V_{OV} and cell balancing detection threshold V_{CB}.

• In case if the overvoltage release threshold V_{OVR} > cell balancing release threshold V_{CBR}



When the charger is connected, charging and discharging by cell balancing is repeated. When the charger is removed, the cell monitor voltage difference (Vn+1-Vn) will settle in cell balancing release threshold V_{CBR}.

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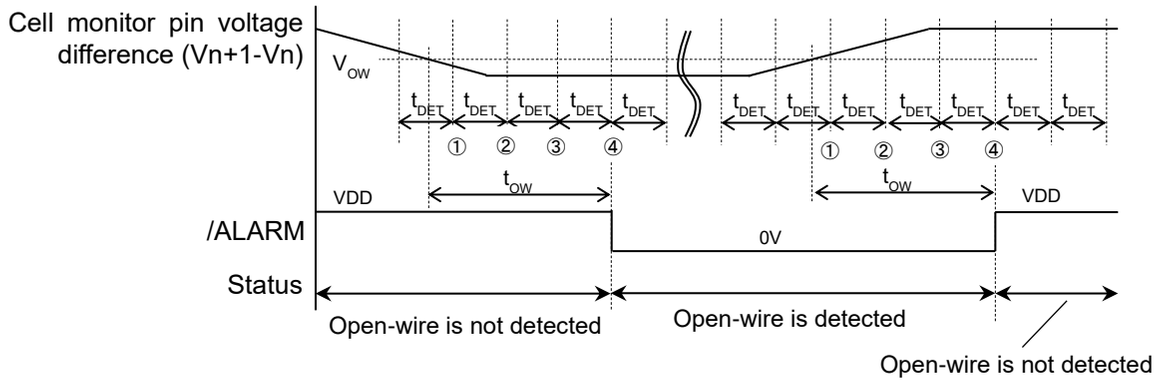
● Open-wire detection function (In case if the open-wire detection delay time = 3 detection cycles)

After power-on, cell voltage monitoring is started with cell voltage monitoring cycle of t_{DET}=400ms(typ). When any one or more battery cell voltages reach or below the open-wire detection threshold V_{OW} for series four times. It detects open-weire state. And if /ALARM output type is CMOS output, /ALARM pin output changes from “H” level to “L” level.

If the state in which voltage of all cell is higher than open-wire detection threshold V_{OW} is detected for once, detection delay time counting is initialized.

After the open-wire detection, if the state in which cell voltage of all cell is higher than open-wire detection threshold V_{OW} is detected for series four times, and if /ALARM output type is CMOS output, /ALARM pin output changes from “L” level to “H” level.

If the state in which cell voltage of one or more cell is lower than open-wire detection threshold V_{OW} is detected for once, detection delay time counting is initialized.



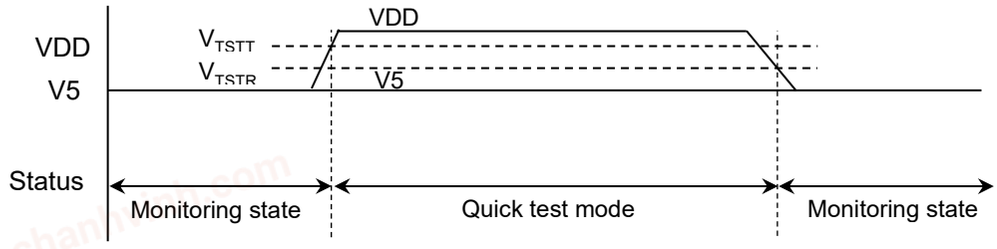
● Quick test mode

In the Quick test mode, cell voltage monitoring cycle is 100ms(typ), cell balancing term is 50ms(typ), overvoltage/cell balancng detection delay time and open-wire detection/release delay time are set shorter than one detection cycle..

If the voltage of VDD pin is more than 10V higher than V5 pin, the state changes into this quick test mode.

For recovering from quick test mode to normal mode, set the difference voltage of V5 and VDD pin lower than 3V”.

This test mode can decrease the test time after board mounting.



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● Redefinition of overvoltage / release voltage, cell balancing detection / release voltage Setting Range and Step

The threshold for Overvoltage detection, Overvoltage Release voltage, Cell Balancing Threshold, and Cell Balancing Release voltage are ROM code selectable per this table. Since some combinations are unavailable, contact us for details.

Detection voltage	Setting range	Step voltage
Overvoltage detection threshold V_{OV}	4.0V to 4.4V	5mV
Overvoltage release threshold V_{OVR}	V_{OV}−(0 to 200mV)	10mV
Cell balancing detection threshold V_{CB}	4.0V to 4.4V	5mV
Cell balancing release threshold V_{CBR}	V_{CB}−(0 to 200mV)	10mV

● Redefinition of overvoltage / cell balancing Detection Delay time and open-wire Detection/Relase Delay Time Range

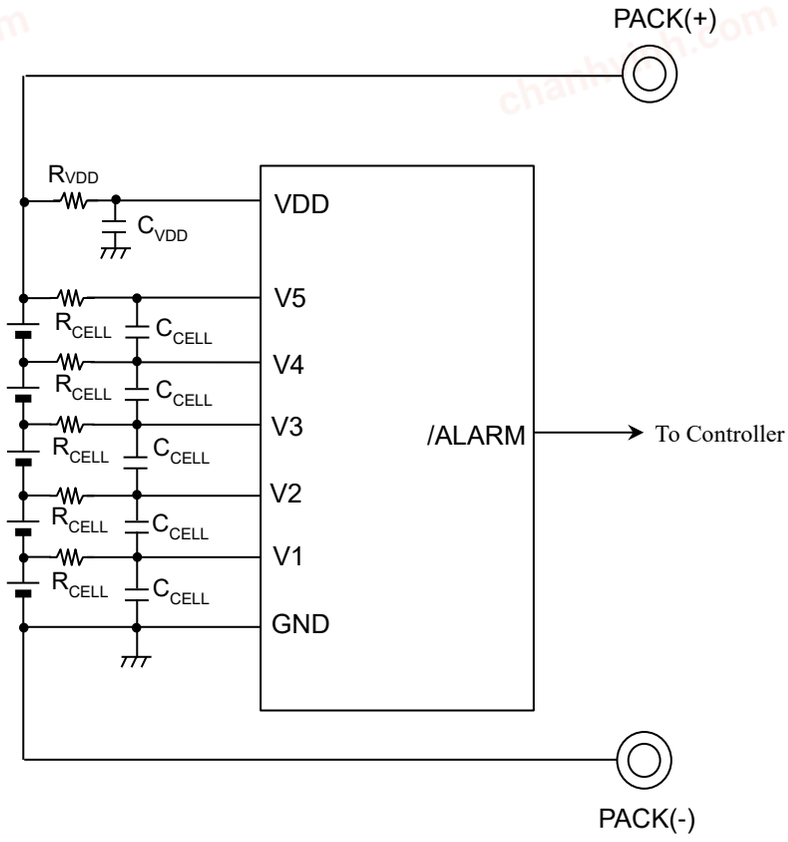
The overvoltage detection delay time and open-wire detection/release delay time are ROM code selectable per these tables.

Delay time	Settable time (detection cycle)														Unit
Overvoltage detection delay time	0 to 1	1 to 2	2 to 3	3 to 4	4 T0 5	5 to 6	6 to 7	7 to 8	8 to 9	9 to 10	10 to 11	12 to 13	13 to 14	14 to 15	cycle
cell balancing detection delay time	0 to 1	1 to 2	2 to 3	3 to 4	4 T0 5	5 to 6	6 to 7	7 to 8	8 to 9	9 to 10	10 to 11	12 to 13	13 to 14	14 to 15	cycle
Open-wire detection/relase delay time	0 to 1	1 to 2	2 to 3	3 to 4	4 T0 5	5 to 6	6 to 7	7 to 8	8 to 9	9 to 10	10 to 11	12 to 13	13 to 14	14 to 15	cycle

Delay time	Settable time (monitoring cycle=400ms)														Unit
Overvoltage detection delay time	0 to 0.4	0.4 to 0.8	0.8 to 1.2	1.2 to 1.6	1.6 to 2.0	2.0 to 2.4	2.4 to 2.8	2.8 to 3.0	3.2 to 3.6	3.6 to 4.0	4.0 to 4.4	4.4 to 4.8	4.8 to 5.2	5.2 to 5.6	sec
cell balancing detection delay time	0 to 0.4	0.4 to 0.8	0.8 to 1.2	1.2 to 1.6	1.6 to 2.0	2.0 to 2.4	2.4 to 2.8	2.8 to 3.0	3.2 to 3.6	3.6 to 4.0	4.0 to 4.4	4.4 to 4.8	4.8 to 5.2	5.2 to 5.6	sec
Open-wire detection/relase delay time	0 to 0.4	0.4 to 0.8	0.8 to 1.2	1.2 to 1.6	1.6 to 2.0	2.0 to 2.4	2.4 to 2.8	2.8 to 3.0	3.2 to 3.6	3.6 to 4.0	4.0 to 4.4	4.4 to 4.8	4.8 to 5.2	5.2 to 5.6	sec

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■ Application Circuit Example (5-cell system)

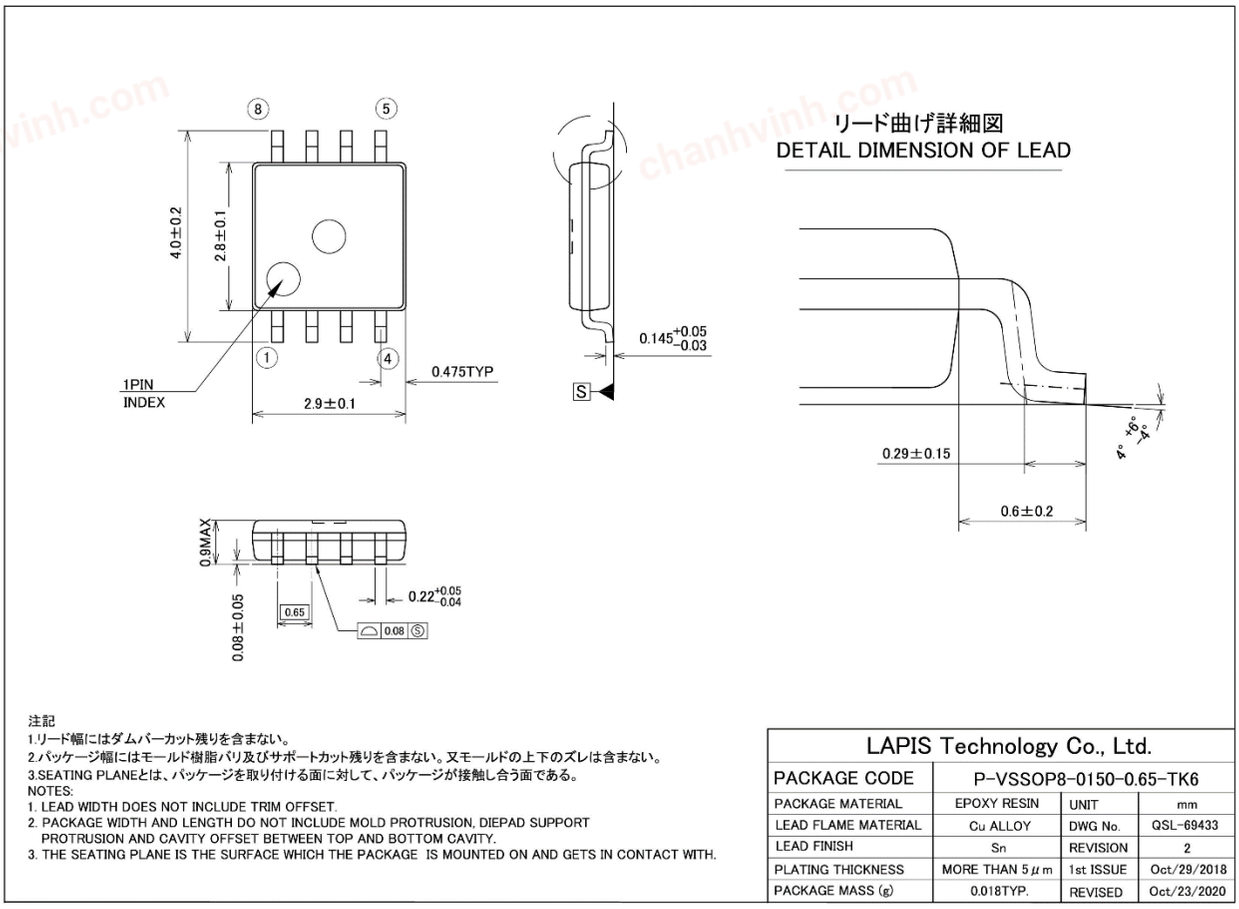


■ Recommended values for External Components

Component	Recommended Value
R_{VDD}	1kΩ
C_{VDD}	4.7µF
R_{CELL}	51Ω
C_{CELL}	0.1µF

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■ Package Dimensions



注記
1.リード幅にはダムバーカット残りを含まない。
2.パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。又モールドの上下のズレは含まない。
3.SEATING PLANEとは、パッケージを取り付ける面に対して、パッケージが接触し合う面である。
NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-VSSOP8-0150-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69433
LEAD FINISH	Sn	REVISION	2
PLATING THICKNESS	MORE THAN 5 μm	1st ISSUE	Oct/29/2018
PACKAGE MASS (g)	0.018TYP.	REVISED	Oct/23/2020

Caution regarding surface mount type packages

Surface mount type packages are susceptible to heat applied in solder reflow and moisture absorbed during storage. Please contact your local ROHM sales representative for recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

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■ Revision History

Document No.	Issue date	Page		Revision Description
		Before rvision	After revision	
FEDL5206-01	2020.11.27	—	—	First edition
FEDL5206-02	Jan. 9, 2024	1	1	Add Application Part number
		16	16	Add Notes

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Notes

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   *1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

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