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Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

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ROHM GROUP
LAPIS TECHNOLOGY

FEDL5205-03

January 9, 2024

ML5205

5 seris cell Li-ion Rechargeable Battery Protection IC

■ General Description

The ML5205 is a protection IC for the 3- to 5-cell Li-ion rechargeable battery pack. It detects individual cell overvoltage and battery cell open-wire, and alerts by alarm output signal.

■ Features

- 3 to 5 cell high precision overvoltage detection function
  Overvoltage detection threshold : 4.0V to 4.4V(5mV step), accuracy:±25mV (0 °C to 60 °C)
  Overvoltage release threshold : 3.8V to 4.2V(10mV step), accuracy:±50mV (0 °C to 60 °C)
  Overvoltage detection delay time : 0 sec to 5.6 sec(typ)

- Open-wire detection function
  Open-wire detection threshold : 0.6V(typ)
  Open-wire detection sink current : ±0.8μA(typ)
  Open-wire detection delay time : 0 sec to 5.6 sec(typ)

- Three types of alarm output
  Selected from CMOS / Nch open drain / Pch open drain

- Number of connected battery cells detection function
  By connecting batteries in order from the top and unused pins are connected to VDD, number of connected cells (3 to 5 cells) is automatically detected.

- Low current consumption : 3μA(typ), 5μA(max) (0℃ to 60℃)

- Power supply voltage : +5V to +25V

- Operating temperature : -20℃ to +85℃

- Package : 8 pin VSSOP

■ Application

・Power tools and Garden tools
・Cordless Cleaner

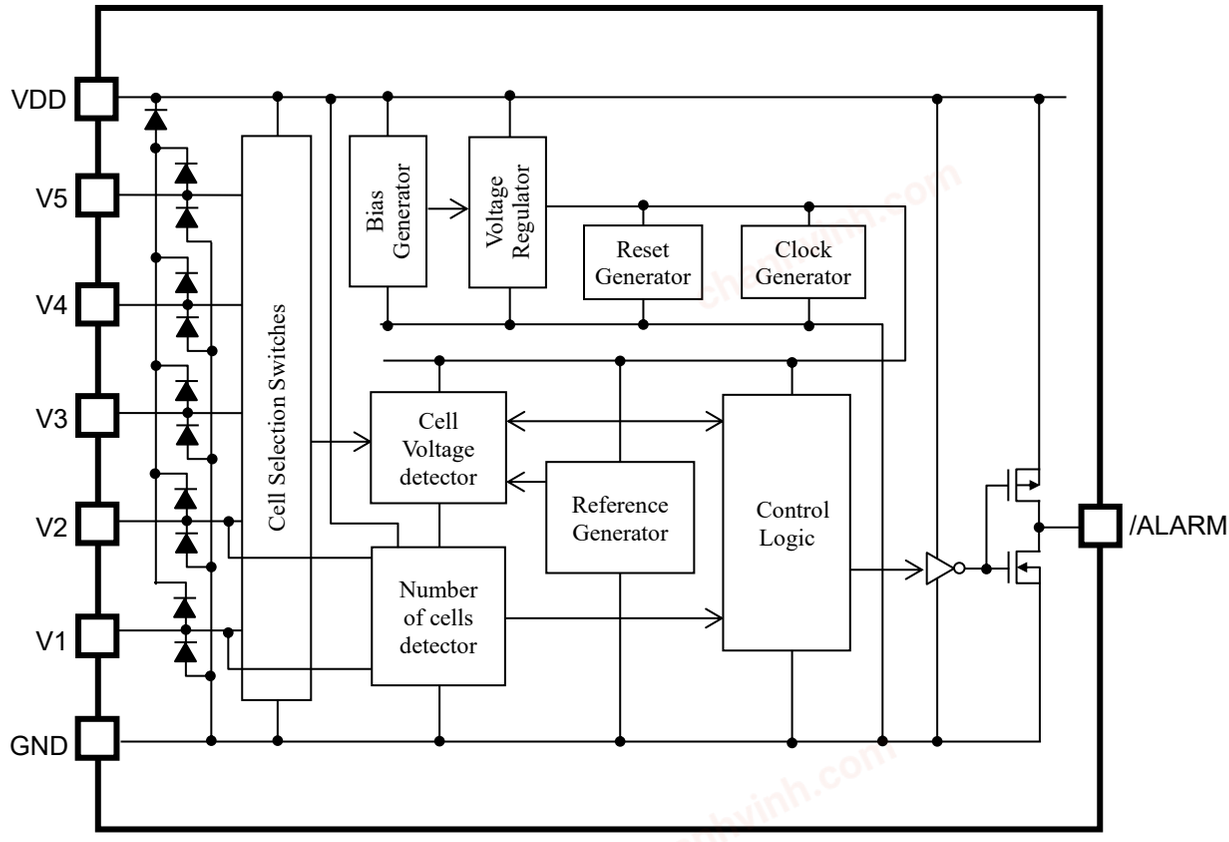
■ Part number

ML5205-001MB Nch open drain output

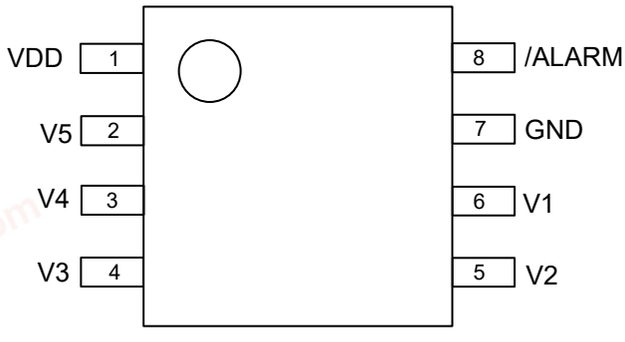
ROHM SEMICONDUCTOR

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■ Block Diagram



■ Pin Configuration (top view)



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■ Pin Description

Pin No	Pin	I/O	Description
1	VDD	—	Power supply input pin
2	V5	I	Battery cell 5 high voltage input pin
3	V4	I	Battery cell 5 low voltage input pin and Battery cell 4 high voltage input pin
4	V3	I	Battery cell 4 low voltage input pin and Battery cell 3 high voltage input pin
5	V2	I	Battery cell 3 low voltage input pin and Battery cell 2 high voltage input pin Should be connected to positive terminal of the highest battery cell for the 3 cell series connected battery pack application
6	V1	I	Battery cell 2 low voltage input pin and Battery cell 1 high voltage input pin Should be connected to positive terminal of the highest battery cell for the 3 or 4 cell series connected battery pack application
7	GND	—	Ground pin
8	/ALARM	O	Alarm signal output pin. ・If CMOS output : Output level is “L“ level(GND level) if overvoltage/ open-wire is detected, else “H“ level (VDD power supply level). The reverse is selectable. ・If Nch open drain output : Output level is “L“ level(GND level) if overvoltage/ open-wire is detected, else “Hi-Z“ level. The reverse is selectable. ・If Pch open drain output: Output level is “H“level (VDD power supply level) if overvoltage/open-wire is detected, else “Hi-Z“ level. The reverse is selectable.

■ Absolute Maximum Ratings

(GND= 0 V, Ta = 25 ℃)

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Applied to VDD pin	−0.3 to +32	V
Input Voltage	V_{IN}	Applied to V5 to V1 pins	−0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT1}	Applied to /ALARM pin(CMOS, Pch open drain)	−0.3 to V_{DD}+0.3	V
	V_{OUT2}	Applied to /ALARM pin(Nch open drain)	−0.3 to +32	V
Short-circuit output current	I_{OS}	Applied to /ALARM pin	10	mA
Power dissipation	P_D	−	730	mW
Storage temperature	T_{STG}	−	-55 to +150	℃

■ Recommended Operating Conditions

(GND= 0 V)

Item	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	−	5 to 25	V
Operating temperature	T_{OP}	−	−20 to +85	℃

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■ Electrical Characteristics

● DC Characteristics

V_{DD}=5 to 25V, GND=0 V, Ta=-20 to +85℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V1, V2 pins input current	I_{VC12}	Each cell voltage= 3.6V Ta=25℃	−1.0	−0.8	−0.6	µA
V3, V4 pins input current	I_{VC34}	Each cell voltage= 3.6V Ta=25℃	0.6	0.8	1.0	µA
V5 pin input current	I_{VC5}	Cell voltage= 3.6V	-0.3	—	0.3	µA
/ALARM pin “H” output voltage	V_{OHA}	I_{OH}= -100µA	V_{DD}−0.2	—	V_{DD}	V
/ALARM pin “L” output voltage	V_{OLA}	I_{OL}=500µA V_{DD}=8 to 25V	0	—	0.5	V
/ALARM pin output leakage current	I_{OLKA}	Output state is Hi-Z	−2	—	2	µA
V1,V2 pin “H” input voltage	V_{IH}	3cell, 4cell configuration	V_{DD}−0.3	—	V_{DD}	V
V1,V2 pin “L” input voltage	V_{IL}	4cell, 5cell configuration	0	—	V_{DD}−3	V

● Supply Current Characteristics

V_{DD}=5 to 25V, GND=0 V, Ta=-20 to +85℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in normal operation	I_{DD}	Each cell voltage=3.6V No output load Ta=0 to 60℃	—	3	5	µA
	I_{DDT}	Each cell voltage=3.6V No output load Ta=-20 to 85℃	—	3	7	µA

(Note) VDD pin current consumption. V5 to V1 pin input current and /ALARM pin output current is not included.

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● Detection Threshold Characteristics (Ta=0 to 60℃)

V_{DD}=18V, GND=0 V, Ta=0 to 60℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	V_{OV}-25m	V_{OV}	V_{OV}+25m	V
Overvoltage release threshold	V_{OVR}	—	V_{OVR}-50m	V_{OVR}	V_{OVR}+50m	V
Open-wire detection / release threshold	V_{OW}	—	0.5	0.6	0.7	V
Quick test mode transition VDD-V5 pin voltage difference	V_{TSTT}	Ta=25℃	10	—	—	V
Quick test mode release VDD-V5 pin voltage difference	V_{TSTR}	Ta=25℃	0	—	3	V

● Detection delay time Characteristics (Ta=0 to 60℃)

V_{DD}=18V, GND=0 V, Ta=0 to 60℃

Item	Symbol	Condition	Min.	Typ.	Max.	単位
Cell voltage monitoring cycle	t_{DET}	—	300	400	500	ms
Overvoltage detection delay time setting range	t_{OV}	Defined with detection cycle	0	—	14	Cycle
Open-wire detection / release delay time	t_{OW}	Defined with detection cycle	0	—	14	Cycle
Quick test mode cell voltage monitoring cycle	t_{DETT}	Ta=25℃	75	100	125	ms
Quick test mode overvoltage detection delay time, Open-wire detection / release delay time	t_{DOVW}	Defined with detection cycle time.	—	—	1	Cycle

● Code 001: Setting Parameters

V_{DD}=18V, GND=0V, Ta=0 to 60℃

Items	Symbols	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	4.175	4.200	4.225	V
Overvoltage release threshold	V_{OVR}	—	4.10	4.15	4.20	V
Overvoltage detection delay time	t_{OV}	Defined with detection cycle	2	—	3	cycle
Open-wire detection / release delay time	t_{OW}	Defined with detection cycle	2	—	3	cycle

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■ Functional Description

● Selecting the number of battery cells

By connecting batteries in order from the top and unused pins are connected to VDD, number of connected cells (3 to 5 cells) is automatically detected.

Connected cells	V5 pin	V4 pin	V3 pin	V2 pin	V1 pin
3 cells	Cell	Cell	Cell	VDD	VDD
4 cells	Cell	Cell	Cell	Cell	VDD
5 cells	Cell	Cell	Cell	Cell	Cell

● /ALARM output pin

/ALARM pin output status for overvoltage/open-wire detected state.

	/ALARM pin output		
	CMOS	Nch open drain (code 001)	Pch open drain
Overvoltage/open-wire detected state	“L” level	“L” level	“H” level
Undetected state	“H” level	“Hi-Z”	“Hi-Z”

(Note) The /ALARM pin output for detected state and undetected state is selectable the reverse.

● Handling VDD pin and V1 to V5 pins

Since the VDD pin is the power supply input, put a noise elimination RC filter in front of the VDD input for stabilization. The resistor value of this noise filter should be adjusted so that the voltage drop across the resistor is smaller than 0.3 V.

The V1 to V5 pins are the monitor pins for individual cell voltages. Put a noise elimination RC filter in front of each battery cell to prevent false detection.

● Power-on / Power-off sequence

Battery cells can be connected in any order, but it is recommend that the lowest voltage cell is connected first, and then connection continues from lower to higher voltage cells, and the highest voltage cell is connected last. There are no restrictions on the power supply voltage rise time at power-on, and power-off sequence or power supply voltage fall time at power-off.

It may transition to the open-wire detection or overvoltage detection state if it takes long time to connect all cells.

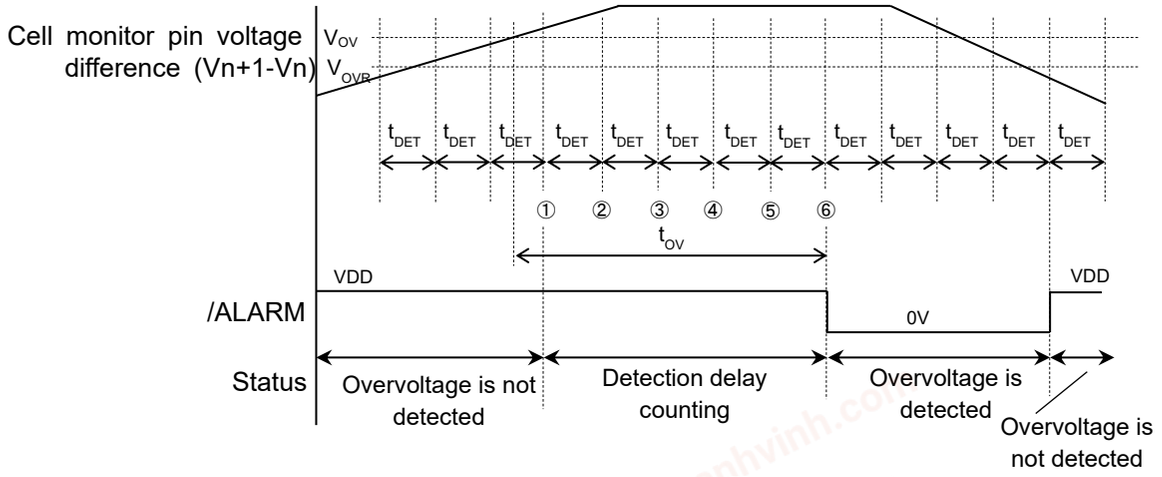
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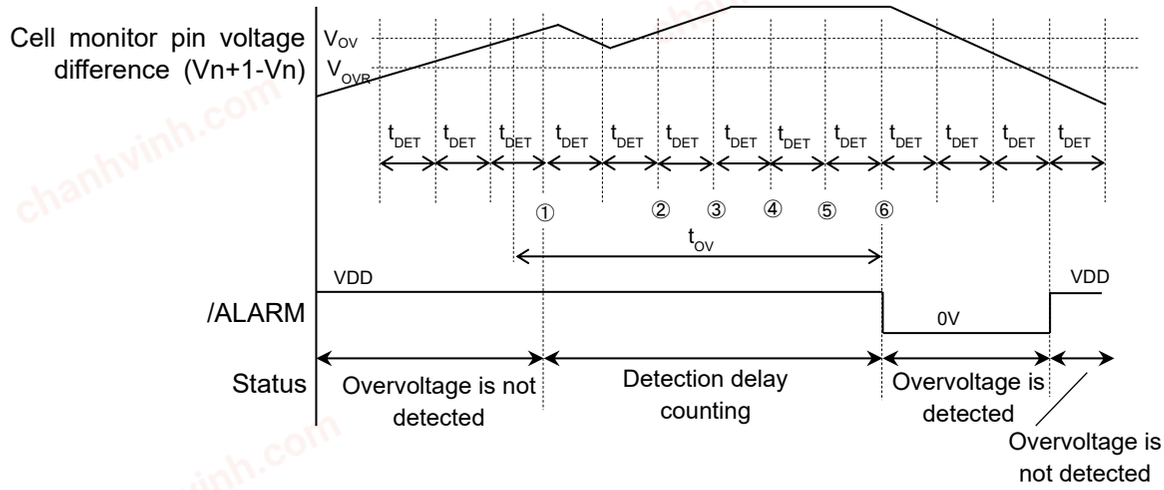
● Overvoltage detection function (if the overvoltage detection delay time =5 detection cycles)

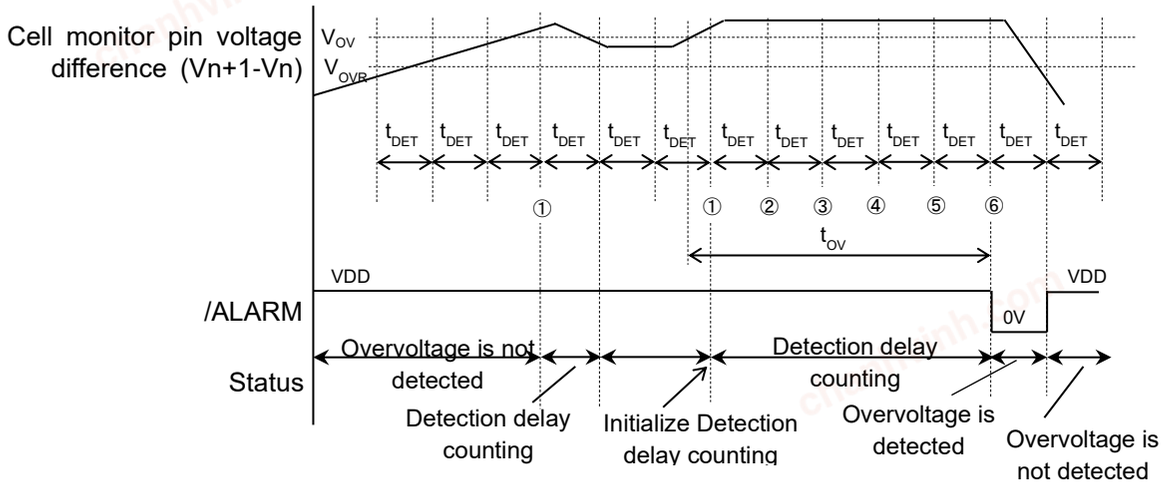
After power-on, voltage monitoring is started with cycle of cell voltage monitoring cycle t_{DET} 400ms(typ) . When any one or more battery cell voltages reach or exceed the overvoltage detection threshold V_{OV} for series six times, it detects overvoltage state. And in case of CMOS output, /ALARM pin output changes from "H" level to "L" level.

If the state in which cell voltage of all cell is lower than overvoltage detection threshold V_{OV} is detected only one time, detection delay time counting is not initialized, but if detected for series two times, detection delay time counting is initialized.

After the overvoltage detection, if the cell voltage of all cell is lower than overvoltage release threshold V_{OVR} , and in case of CMOS output, /ALARM pin output changes from "L" level to "H" level.







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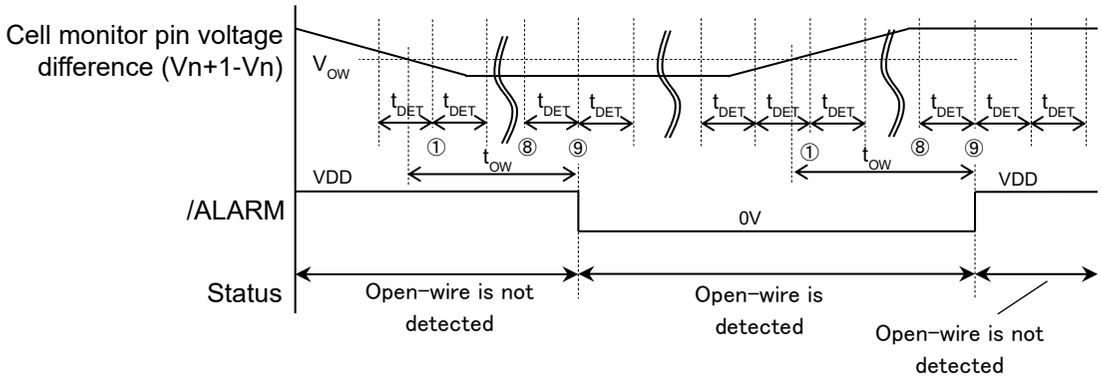
● Open-wire detection function(if the open-wire detection delay time =8 detection cycles)

After power-on, voltage monitoring is started with cycle of cell voltage monitoring cycle t_{DET} 400ms(typ).

When any one or more battery cell voltages reach or below the open-wire detection threshold V_{OW} for series nine times, it detects open-wire. And in case of CMOS output, /ALARM pin output changes from "H" to "L" level

If the state in which cell voltage of all cell is higher than open-wire detection threshold V_{OW} is detected one time, detection delay counting is initialized.

After the open-wire detection, if the state in which cell voltage of all cell is higher than open-wire detection threshold V_{OW} is detected for series nine times, and in case of CMOS output, /ALARM pin output changes from "L" level to "H" level. If the state in which cell voltage of one or more cell is lower than open-wire detection threshold V_{OW} for once, detection time counting is initialized.



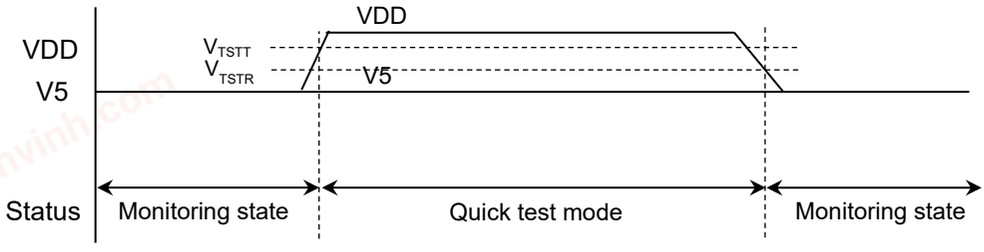
● Quick test mode

In the Quick test mode, overvoltage/open wire detection cycle time is set 100ms(typ), overvoltage detection delay time and 0V battery detection delay time are set equal or shorter than one detection cycle.

If the voltage of VDD pin is more than 10V higher than V5 pin, the state change into this quick test mode.

For recovering from quick test mode to normal mode, set the voltage of VDD pin lower than "the voltage of V5 + 3V".

This test mode can decrease the test time after board mounting.



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● Definition of overvoltage detection/release threshold voltage range and step

The overvoltage detection/release thresholds can be defined as shown in the following table. Since some combinations are unavailable, contact us for detail.

Detection threshold	Setting range	Step voltage
Overvoltage detection threshold V_{OV}	4.0V to 4.4V	5mV
Overvoltage release threshold V_{OVR}	V_{OV} – (0 to 200mV)	10mV

● Definition of overvoltage detection delay time and open-wire detection/release delay time range

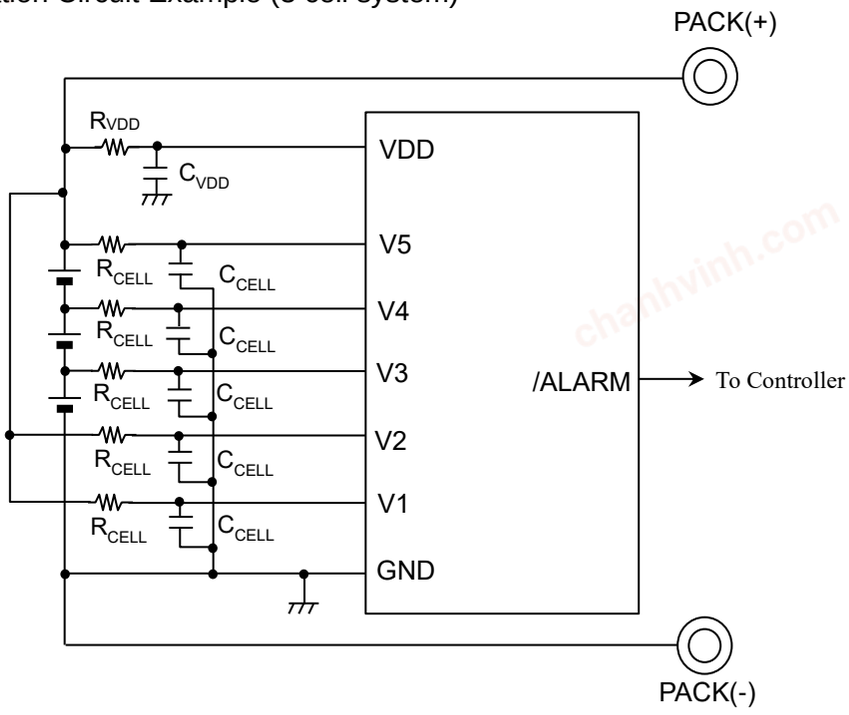
The overvoltage detection delay time and open-wire detection delay time can be defined as shown in the following table.

Delay time	Settable time (detection cycle time))														Unit
Overvoltage detection delay time	0 to 1	1 to 2	2 to 3	3 to 4	4 to 5	5 to 6	6 to 7	7 to 8	8 to 9	9 to 10	10 to 11	11 to 12	12 to 13	13 to 14	Cycle
Open-wire detection/release delay time	0 to 1	1 to 2	2 to 3	3 to 4	4 to 5	5 to 6	6 to 7	7 to 8	8 to 9	9 to 10	10 to 11	11 to 12	12 to 13	13 to 14	Cycle

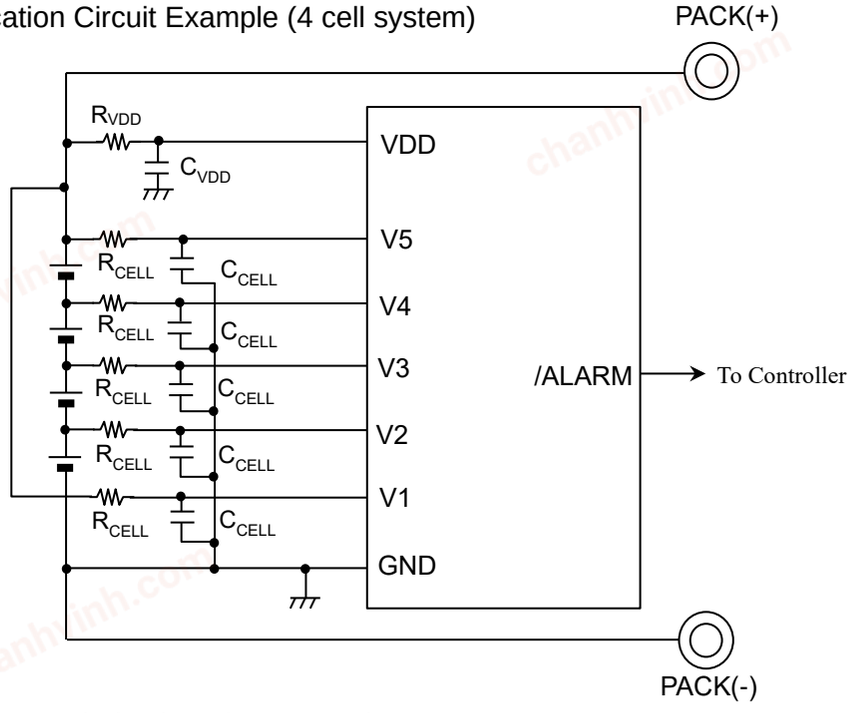
Delay time	Settable time(detection cycle =400ms)														Unit
Overvoltage detection delay time	0 to 0.4	0.4 to 0.8	0.8 to 1.2	1.2 to 1.6	1.6 to 2.0	2.0 to 2.4	2.4 to 2.8	2.8 to 3.2	3.0 to 3.6	3.6 to 4.0	4.0 to 4.4	4.4 to 4.8	4.8 to 5.2	5.2 to 5.6	sec
Open-wire detection/release delay time	0 to 0.4	0.4 to 0.8	0.8 to 1.2	1.2 to 1.6	1.6 to 2.0	2.0 to 2.4	2.4 to 2.8	2.8 to 3.2	3.0 to 3.6	3.6 to 4.0	4.0 to 4.4	4.4 to 4.8	4.8 to 5.2	5.2 to 5.6	sec

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■ Application Circuit Example (3 cell system)



■ Application Circuit Example (4 cell system)

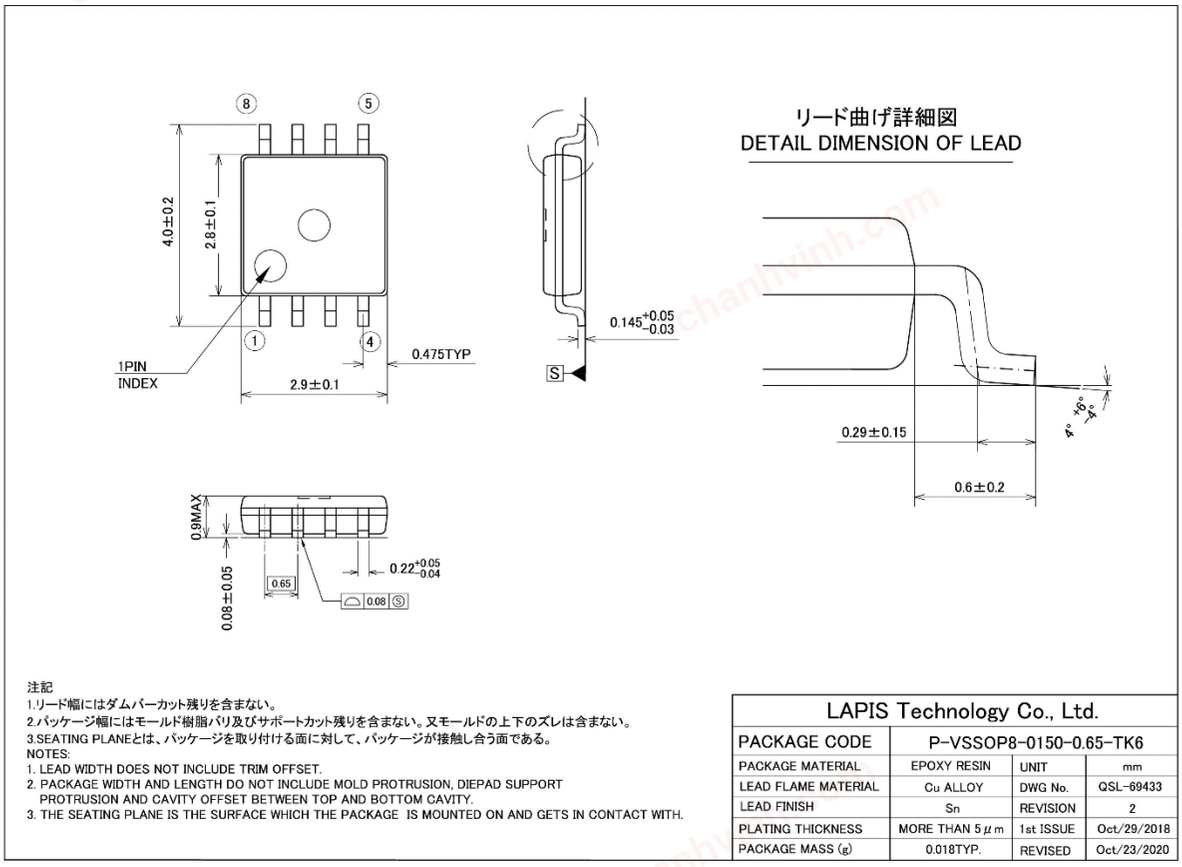


■ Recommended values for External Components

Component	Recommended Value
R_{VDD}	1kΩ
C_{VDD}	4.7μF
R_{CELL}	330Ω
C_{CELL}	0.22μF

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■ Package Dimensions



注記
1.リード幅にはダムバーカット残りを含まない。
2.パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。又モールドの上下のズレは含まない。
3.SEATING PLANEとは、パッケージを取り付ける面に対して、パッケージが接触し合う面である。
NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-VSSOP8-0150-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69433
LEAD FINISH	Sn	REVISION	2
PLATING THICKNESS	MORE THAN 5 μm	1st ISSUE	Oct/29/2018
PACKAGE MASS (g)	0.018TYP.	REVISED	Oct/23/2020

Caution regarding surface mount type packages

Surface mount type packages are susceptible to heat applied in solder reflow and moisture absorbed during storage. Please contact your local ROHM sales representative for recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment

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■ Revision History

Document No.	Issued date	Page		Revision Description
		Before revision	After revision	
FEDL5205-01	2021.03.23	—	—	Frist edition issued
FEDL5205-02	2021.07.27	2	2	Change Block Diagram
FEDL5205-03	Jan. 9, 2024	1	1	Add Application Part number
		13	13	Add Notes

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LAPIS Technology Co.,Ltd.
2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
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