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TECHNICAL NOTE

Voltage Detector IC series

Low Voltage Standard CMOS Voltage Detector IC Series

BU48□□G/F/FVE，BU49□□G/F/FVE series

●General Description

ROHM standard CMOS reset IC series is a high-accuracy low current consumption reset IC series.
The lineup was established with two output types (Nch open drain and CMOS output) and detection voltage range from 0.9V to 4.8V in increments of 0.1V, so that the series may be selected according to the application at hand.

●Features

1) Detection voltage from 0.9V to 4.8V in 0.1V increments
2) Highly accurate detection voltage: ±1.0%
3) Ultra-low current consumption
4) Nch open drain output (BU48□□G/F/FVE)and CMOS output（BU49□□G/F/FVE）
5) Small surface package : SSOP5(BU48□□G，BU49□□G)
: SOP4(BU48□□F，BU49□□F)
: VSOF5(BU48□□FVE，BU49□□FVE)

●Applications

All electronics devices that use microcontrollers and logic circuits.

●Selection Guide

Part Number : BU4□ □ □ □

① ② ③

Number	Specification	Details
①	Output Circuit Type	2 : Open drain output 3 : CMOS output
②	Detection voltage	Example) V_{DET} : Represented as 0.1V steps in the range from 0.9V to 4.8V (Displayed as 0.9 in the case of 0.9V)
③	Package	G : SSOP5（SMP5C2） F : SOP4 FVE : VSOF5（EMP5）

●Lineup

Making	Detection voltage	Part Number	Making	Detection voltage	Part Number	Making	Detection voltage	Part Number	Making	Detection voltage	Part Number
ZR	4.8V	BU4848	YV	2.8V	BU4828	1H	4.8V	BU4948	0M	2.8V	BU4928
ZQ	4.7V	BU4847	YU	2.7V	BU4827	1G	4.7V	BU4947	0L	2.7V	BU4927
ZP	4.6V	BU4846	YT	2.6V	BU4826	1F	4.6V	BU4946	0K	2.6V	BU4926
ZN	4.5V	BU4845	YS	2.5V	BU4825	1E	4.5V	BU4945	0J	2.5V	BU4925
ZM	4.4V	BU4844	YR	2.4V	BU4824	1D	4.4V	BU4944	0H	2.4V	BU4924
ZL	4.3V	BU4843	YQ	2.3V	BU4823	1C	4.3V	BU4943	0G	2.3V	BU4923
ZK	4.2V	BU4842	YP	2.2V	BU4822	1B	4.2V	BU4942	0F	2.2V	BU4922
ZJ	4.1V	BU4841	YN	2.1V	BU4821	1A	4.1V	BU4941	0E	2.1V	BU4921
ZH	4.0V	BU4840	YM	2.0V	BU4820	0Z	4.0V	BU4940	0D	2.0V	BU4920
ZG	3.9V	BU4839	YL	1.9V	BU4819	0Y	3.9V	BU4939	0C	1.9V	BU4919
ZF	3.8V	BU4838	YK	1.8V	BU4818	0X	3.8V	BU4938	0B	1.8V	BU4918
ZE	3.7V	BU4837	YJ	1.7V	BU4817	0W	3.7V	BU4937	0A	1.7V	BU4917
ZD	3.6V	BU4836	YH	1.6V	BU4816	0V	3.6V	BU4936	ZZ	1.6V	BU4916
ZC	3.5V	BU4835	YG	1.5V	BU4815	0U	3.5V	BU4935	ZY	1.5V	BU4915
ZB	3.4V	BU4834	YF	1.4V	BU4814	0T	3.4V	BU4934	ZX	1.4V	BU4914
ZA	3.3V	BU4833	YE	1.3V	BU4813	0S	3.3V	BU4933	ZW	1.3V	BU4913
YZ	3.2V	BU4832	YD	1.2V	BU4812	0R	3.2V	BU4932	ZV	1.2V	BU4912
YY	3.1V	BU4831	YC	1.1V	BU4811	0Q	3.1V	BU4931	ZU	1.1V	BU4911
YX	3.0V	BU4830	YB	1.0V	BU4810	0P	3.0V	BU4930	ZT	1.0V	BU4910
YW	2.9V	BU4829	YA	0.9V	BU4809	0N	2.9V	BU4929	ZS	0.9V	BU4909

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●ABSOLUTE MAXIMUM RATINGS(Ta=25℃)

Parameter		Symbol	Limits	Unit
Power Supply Voltage		VDD-GND	-0.3 ~ +7	V
Output Voltage	Nch Open Drain Output	VOUT	GND-0.3 ~ +7	V
	CMOS Output		GND-0.3 ~ VDD+0.3	
Power Dissipation	SSOP5 ＊1 ＊4	Pd	540	mW
	SOP4 ＊2 ＊4		400	
	VSOF5 ＊3 ＊4		210	
Operating Temperature		Topr	-40 ~ +125	℃
Ambient Storage Temperature		Tstg	-55 ~ +125	℃

＊1 When used at temperatures higher than Ta=25℃,the power is reduced by 5.4mW per 1℃ above 25℃
＊2 When used at temperatures higher than Ta=25℃,the power is reduced by 4.0mW per 1℃ above 25℃
＊3 When used at temperatures higher than Ta=25℃,the power is reduced by 2.1mW per 1℃ above 25℃
＊4 When a ROHM standard circuit board（70mm×70mm×1.6mm，glass epoxy board）is mounted.

●ELECTRICAL CHARACTERISTICS (Unless specified otherwise, Ta=-25℃~+125℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Detection Voltage	VDET	VDET(T)×0.99	VDET (T)	VDET(T)×1.01	V	VDD=H→L,RL=470kΩ ＊1
Detection Voltage	VDET/ΔT	–	±30	–	ppm/℃	Ta=-40℃～+125℃ (Designed Guarantee)
Hysteresis Voltage	ΔVDET	VDET×0.03	VDET×0.05	VDET×0.07	V	VDET≧1.1V,RL=470kΩ,VDD=L→H→L
Circuit Current when ON	IDD1	–	0.40	1.75	μA	VDD=VDET-0.2V,VDET=4.3～4.8V
Circuit Current when OFF	IDD2	–	0.55	2.28	μA	VDD=VDET+2.0V,VDET=4.3～4.8V
Operating Voltage Range	VOPL	0.7	–	–	V	VOL≦0.4V,Ta=25～125℃
“L” Output Current (Nch)	IOL	3.6	6.5	–	mA	VDS=0.5V,VDD=2.4V,VDET=2.7～4.8V
“H” Output Current (Pch)	IOH	2.0	4.0	–	mA	VDS=0.5V,VDD=6.0V,VDET=4.0～4.8V

＊1 Guarantee on Ta=25℃
Note）RL is unnecessary for CMOS output.
Note）Regarding the operating limit voltage
The VOUT output is unsettled when VDD is less than this voltage. It will be Open, High or Low.
Note）Hysteresis Voltage =（Reset Release Voltage）-（Reset Detection Voltage）[V]
VDET（T）: Set Value of Detection voltage（0.9V～4.8V，0.1Vstep）
Designed Guarantee. (Outgoing inspection is not done an all products.)

●Block Diagram

BU48□□G/F/FVE

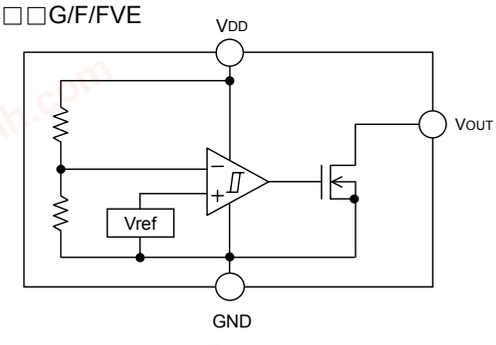


Fig.1

BU49□□G/F/FVE

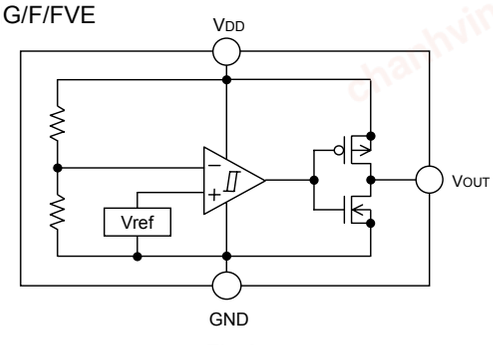


Fig.2

TOP VIEW



SSOP5

PIN No.	Symbol	Function
1	VOUT	Reset output
2	VDD	Power supply voltage
3	GND	GND
4	N.C.	Unconnected terminal
5	N.C.	Unconnected terminal

TOP VIEW



SOP4

PIN No.	Symbol	Function
1	VOUT	Reset output
2	VDD	Power supply voltage
3	N.C.	Unconnected terminal
4	GND	GND

TOP VIEW



VSOF5

PIN No.	Symbol	Function
1	VOUT	Reset output
2	SUB	Substrate＊
3	N.C.	Unconnected terminal
4	VDD	Power supply voltage
5	GND	GND

＊Connect the substrate to VDD

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●Reference Data (unless specified otherwise, Ta=25℃)

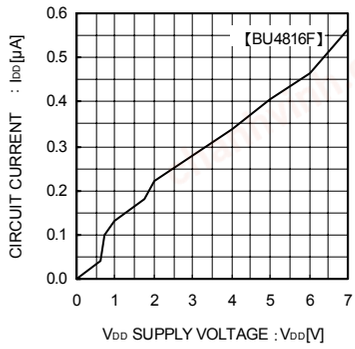


Fig.3 Circuit Current

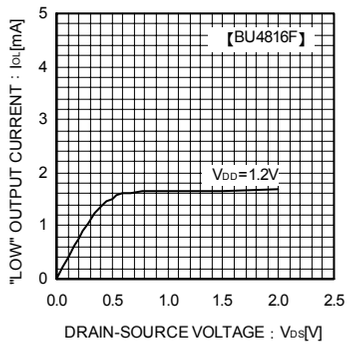


Fig.4 “LOW” Output Current

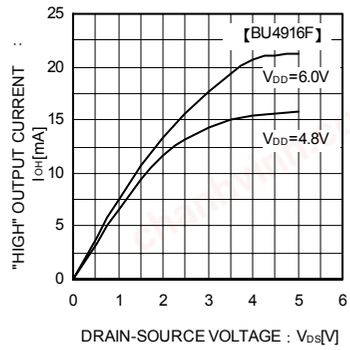


Fig.5 “High” Output Current

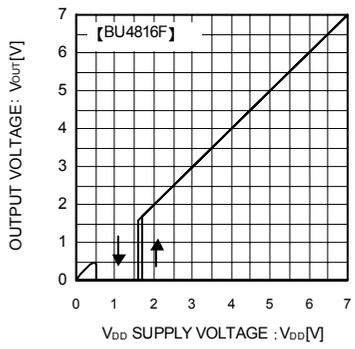


Fig.6 I/O Characteristics

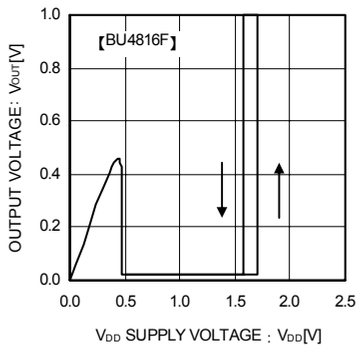


Fig.7 Operating Limit Voltage

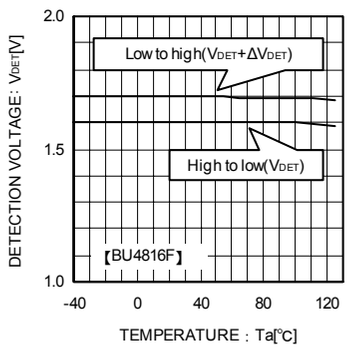


Fig.8 Detecting Voltage
Release Voltage

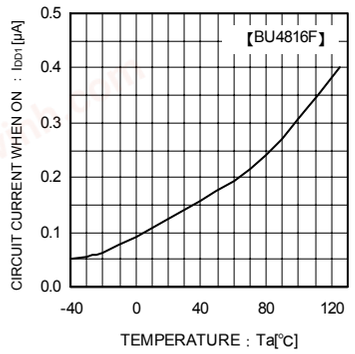


Fig.9 Circuit Current when ON

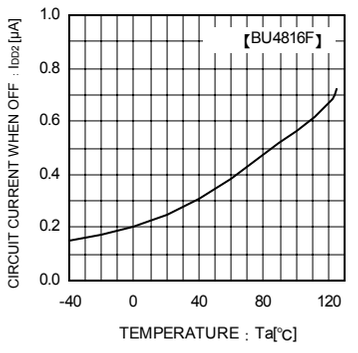


Fig.10 Circuit Current when OFF

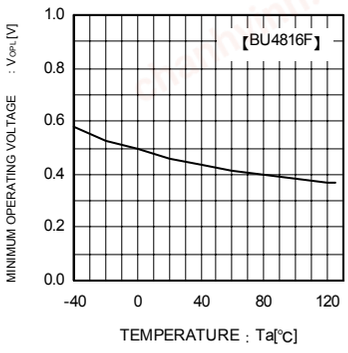


Fig.11 Operating Limit Voltage

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●Reference Data

Examples of Output rising value（TPLH）and Output falling value（TPHL）

Part Number	TPLH[μs]	TPHL[μs]
BU4845G/F/FVE	23.3	275.9
BU4945G/F/FVE	3.5	354.3
	VDD=4.3V→5.1V	VDD=5.1V→4.3V

※This data is for reference only.

This figure will vary with the application, so please confirm actual operation conditions before use.

●Explanation of Operation

For both the open drain type（Fig.12）and the CMOS output type（Fig.13）, the detection and release voltages are used as threshold voltages. When the voltage applied to the VDD pins reaches the applicable threshold voltage, the Vout terminal voltage switches from either “High” to “Low” or from “Low” to “High”. Because the BU48□□G/F/FVE series uses an open drain output type, it is possible to connect a pull-up resistor to VDD or another power supply [The output “High” voltage (VOUT) in this case becomes VDD or the voltage of the other power supply].

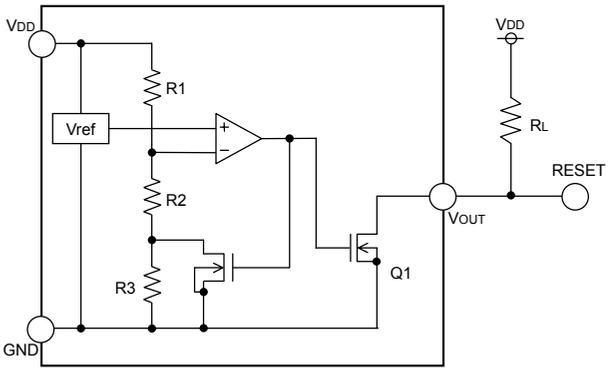


Fig.12（BU48□□ type internal block diagram）

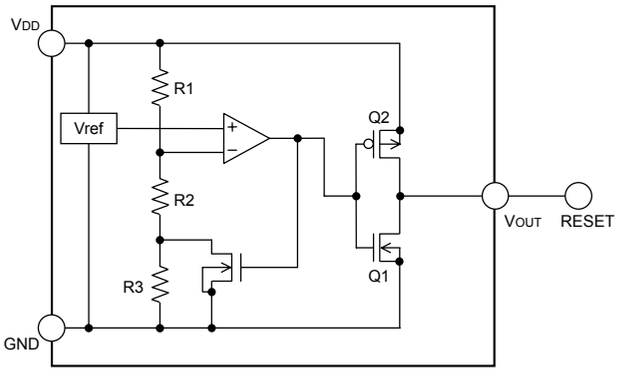


Fig.13（BU49□□ type internal block diagram）

●Timing Waveforms

Example:The following shows the relationship between the input voltage VDD, the CT Terminal Voltage VCT and the output voltage VOUT when the input power supply voltage VDD is made to sweep up and sweep down (The circuits are those in Figures 12 and 13).

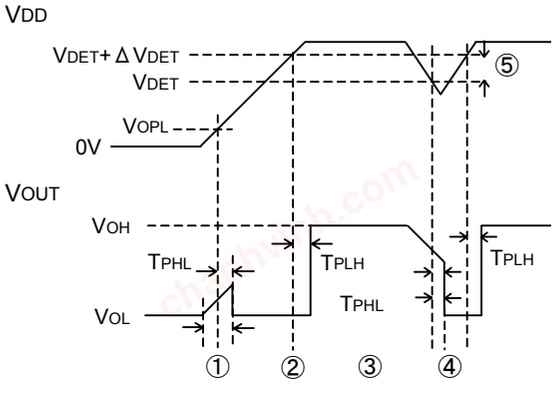


Fig.14

① When the power supply is turned on, the output is unsettled from after over the operating limit voltage (VOPL) until TPHL. There fore it is possible that the reset signal is not outputted when the rise time of VDD is faster than TPHL.

② When VDD is greater than VOPL but less than the reset release voltage (VDET + VDET), output (VOUT) voltages will switch to L.

③ If VDD exceeds the reset release voltage (VDET + VDET), then VOUT switches from L to H (with a delay of TPLH).

④ If VDD drops below the detection voltage (VDET) when the power supply is powered down or when there is a power supply fluctuation, VOUT switches to L (with a delay of TPHL).

⑤ The potential deference between the detection voltage and the release voltage is known as the hysteresis width (VDET). The system is designed such that the output does not flip-flop with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

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●Circuit Applications

1) Examples of a common power supply detection reset circuit

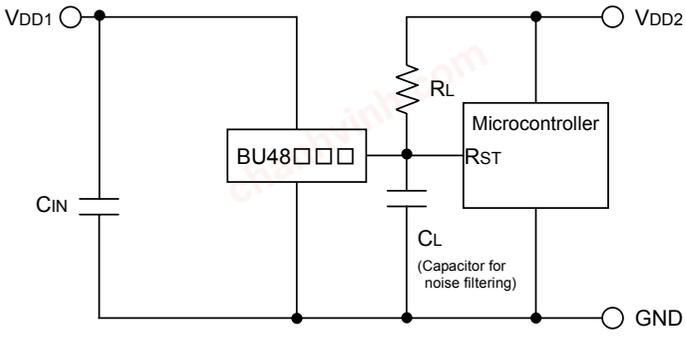


Fig.15 Open collector Output type

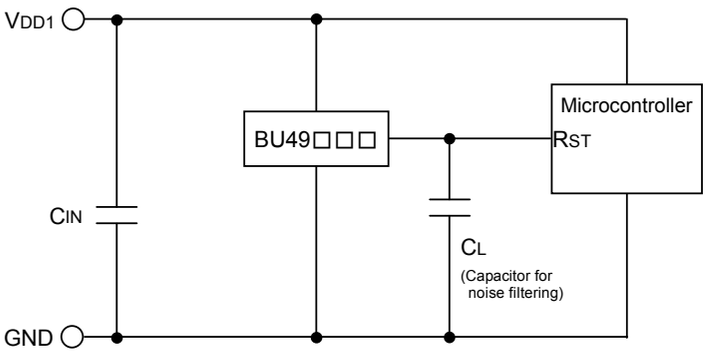


Fig.16 CMOS Output type

Application examples of BU48□□G/F/FVE series (Open Drain output type) and BU49□□G/F/FVE series (CMOS output type) are shown below.

CASE1:The power supply of the microcontroller ($V_{DD}2$) differs from the power supply of the reset detection ($V_{DD}1$).
Use the Open Drain Output Type (BU48□□G/FVE) attached a load resistance (R_L) between the output and $V_{DD}2$. (As shown Figure 15)

CASE2:The power supply of the microcontroller ($V_{DD}1$) is same as the power supply of the reset detection ($V_{DD}1$).
Use CMOS output type (BU43□□G/FVE) or Open Drain Output Type (BU48□□G/FVE) attached a load resistance (R_L) between the output and $V_{DD}1$.
(As shown Figure 16)

When a capacitance CL for noise filtering or setting the output delay time is connected to the Vout pin (the reset signal input terminal of the microcontroller), please take into account the waveform of the rise and fall of the output voltage (Vout).

2) Examples of the power supply with resistor dividers

In applications where the power supply input terminal (VDD) of an IC with resistor dividers, it is possible that a through-current will momentarily flow into the circuit when the output logic switches, resulting in malfunctions (such as output oscillatory state).
(Through-current is a current that momentarily flows from the power supply (VDD) to ground (GND) when the output level switches from “High” to “Low” or vice versa.)
Consider the use of BD48□□ when the power supply input it with resistor dividers.

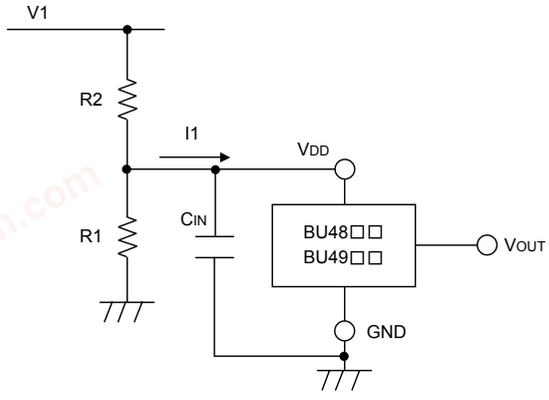


Fig.17

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● Operation Notes

1. Absolute maximum range
   Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed. We cannot be defined the failure mode, such as short mode or open mode. Therefore a physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2. GND potential
   GND terminal should be a lowest voltage potential every state.
   Please make sure all pins that are over ground even if include transient feature.

3. Electrical Characteristics
   Be sure to check the electrical characteristics, that are one the tentative specification will be changed by temperature, supply voltage, and external circuit.

4. Bypass Capacitor for Noise Rejection
   Please put into the to reject noise between V_{DD} pin and GND with 1uF over and between V_{OUT} pin and GND with 1000pF. If extremely big capacitor is used, transient response might be late. Please confirm sufficiently for the point.

5. Short Circuit between Terminal and Soldering
   Don't short-circuit between Output pin and V_{DD} pin, Output pin and GND pin, or V_{DD} pin and GND pin. When soldering the IC on circuit board please is unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

6. Electromagnetic Field
   Mal-function may happen when the device is used in the strong electromagnetic field.

7. The V_{DD} line inpedance might cause oscillation because of the detection current.

8. A V_{DD} -GND capacitor (as close connection as possible) should be used in high V_{DD} line impedance condition.

9. Lower than the mininum input voltage makes the V_{OUT} high impedance, and it must be V_{DD} in pull up (V_{DD}) condition.

10. Recommended value of RL Resistar is over 10kΩ (VDET＝1.5V～4.8V),
    over 100kΩ (VDET＝0.9～1.4V).

11. This IC has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If 10MΩ leakage is assumed between the CT terminal and the GND terminal, 1MΩ connection between the CT terminal and the V_{DD} terminal would be recommended. Also, if the leakage is assumed between the V_{OUT} terminal and the GND terminal, the pull up resistor should be less than 1/10 of the assumed leak resistance.

12. External parameters
    For R_L, the recommended range is 10kΩ～1MΩ. There are many factors (board layout, etc) that can affect characteristics. Please verify and confirm using practical applications.

13. Power on reset operation
    Please note that the power on reset output varies with the Vcc rise up time. Please verify the actual operation.

14. Precautions for board inspection
    Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC.Therefore, be certain to use proper discharge procedure before each process of the test operation.
    To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handing, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

15. When the power supply, is turned on because of incertain cases, momentary Rash-current flow into the IC at the logic unsettled, the couple capacitance, GND pattern of width and leading line must be considered.

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●Part Number Selection

B	U	4					–	T	R

BU48：Standard CMOS reset IC
Open drain type
BU49：Standard CMOS reset IC
CMOS Output type

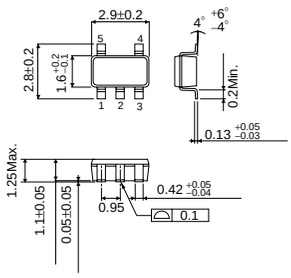
Reset voltage examples
09：0.9V
〃 (0.1Vstep)
48：4.8V

Package
G ：SSOP5
F ：SOP4
FVE：VSOF5

Taping
Embossed taping

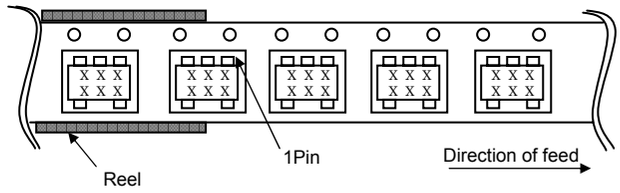
SSOP5

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<Tape and Reel information> SSOP5

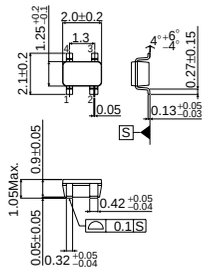
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

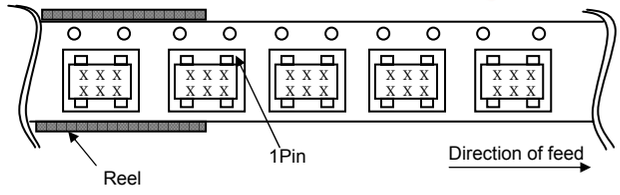
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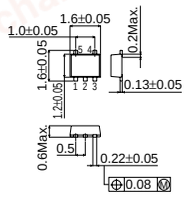
Tape	Embossed carrier tape
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※When you order , please order in times the amount of package quantity.

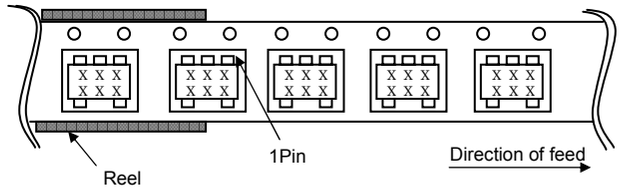
VSOF5

<Dimension> (Unit：mm)



<Tape and Reel information> VSOF5

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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