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Technical Note

High Reliability Serial EEPROMs

High Reliability Series EEPROMs Microwire BUS

BR93L□□-W Series, BR93A□□-WM Series, BR93H□□-WC Series

No.11001EFT03

ROHM's series of serial EEPROMs represent the highest level of reliability on the market. A double cell structure provides a failsafe method of data reliability, while a double reset function prevents data miswriting. In addition, gold pads and gold wires are used for internal connections, pushing the boundaries of reliability to the limit.
BR93L□□-W Series are assort 1Kbit～16Kbit. BR93A□□-WM Series are possible to operate at 105℃ and are assorted with 1K～16Kbit. BR93H□□-WC Series are possible to operate at 125℃, are assorted with 2K～16Kbit.

Contents

BR93L□□-W Series

BR93L46-W, BR93L56-W, BR93L66-W, BR93L76-W, BR93L86-W

BR93A□□-WM Series

BR93A46-WM, BR93A56-WM, BR93A66-WM, BR93A76-WM, BR93A86-WM

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BR93H□□-WC Series

BR93H56-WC, BR93H66-WC, BR93H76-WC, BR93H86-WC

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Serial EEPROM Series

High Reliability Series EEPROMs Microwire BUS

BR93L□□-W Series, 93A□□-WM Series

●Description

BR93L□□-W Series, BR93A□□-WM Series are serial EEPROM of serial 3-line interface method

●Features

1) 3-line communications of chip select, serial clock, serial data input / output (the case where input and output are shared)
2) Actions available at high speed 2MHz clock(2.5~5.5V)
3) Speed write available (write time 5ms max.)
4) Same package and pin layout from 1Kbit to 16Kbit
5) 1.8~5.5V (BR93L□□-W Series), 2.5～5.5V(BR93A□□-WM Series) single power source action
6) Highly reliable connection by Au pad and Au wire
7) Address auto increment function at read action
8) Write mistake prevention function
   Write prohibition at power on
   Write prohibition by command code
   Write mistake prevention function at low voltage
9) Program cycle auto delete and auto end function
10) Program condition display by READY / BUSY
11) Low current consumption
   At write action (at 5V) : 1.2mA (Typ.)
   At read action (at 5V) : 0.3mA (Typ.)
   At standby action (at 5V) : 0.1μA (Typ.)(CMOS input)
12) TTL compatible(input / output s)
13) Compact package SOP8/SOP-J8/SSOP-B8/TSSOP-B8/MSOP8/TSSOP-B8J*1
14) Data retention for 40 years
15) Data rewrite up to 1,000,000 times
16) Data at shipment all addresses FFFFh

*1 Only SOP8, SOP-J8, MSOP8 for BR93A□□-WM

●BR93L, BR93A Series

Capacity	Bit format	Type	Power source voltage	SOP8		SOP-J8		SSOP-B8		TSSOP-B8		MSOP8	TSSOP-B8J
Package type				F	RF	FJ	RFJ	FV	RFV	FVT	RFVT	RFVM	RFVJ
1Kbit	64×16	BR93L46-W	1.8～5.5V	●	●	●	●	●	●	●	●	●	●
2Kbit	128×16	BR93L56-W	1.8～5.5V	●	●	●	●	●	●	●	●	●	●
4Kbit	256×16	BR93L66-W	1.8～5.5V	●	●	●	●	●	●	●	●	●	●
8Kbit	512×16	BR93L76-W	1.8～5.5V	●	●	●	●		●		●	●	●
16Kbit	1K×16	BR93L86-W	1.8～5.5V	●	●	●	●		●		●	●	●
1Kbit	64×16	BR93A46-WM	2.5～5.5V	●	●	●	●						
2Kbit	128×16	BR93A56-WM	2.5～5.5V	●	●	●	●					●	
4Kbit	256×16	BR93A66-WM	2.5～5.5V	●	●	●	●					●	
8Kbit	512×16	BR93A76-WM	2.5～5.5V	●	●	●	●						
16Kbit	1K×16	BR93A86-WM	2.5～5.5V	●	●	●	●					●	

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●Absolute Maximum Ratings(Ta=25℃,BR93L□□-W)

Parameter	Symbol	Limits	Unit
Impressed voltage	VCC	-0.3～+6.5	V
Permissible dissipation	Pd	450 (SOP8) *1	mW
		450 (SOP-J8) *2	
		300 (SSOP-B8) *3	
		330 (TSSOP-B8) *4	
		310 (MSOP8) *5	
		310 (TSSOP-B8J) *6	
Storage temperature range	Tstg	-65～+125	℃
Action temperature range	Topr	-40～+85	℃
Terminal voltage	-	-0.3～VCC+0.3	V

* When using at Ta=25℃ or higher, 4.5mW(*1,*2), 3.0mW(*3) 3.3mW(*4), 3.1mW(*5, 6), to be reduced per 1℃.

●Absolute Maximum Ratings (Ta=25℃,BR93A□□-WM)

Parameter	Symbol	Limits	Unit
Impressed voltage	VCC	-0.3～+6.5	V
Permissible dissipation	Pd	450 (SOP8) *1	mW
		450 (SOP-J8) *2	
		310 (MSOP8) *3	
Storage temperature range	Tstg	-65～+125	℃
Action temperature range	Topr	-40～+105	℃
Terminal voltage	-	-0.3～VCC+0.3	V

* When using at Ta=25℃ or higher, 4.5mW(*1,*2), 3.1 mW(*3) to be reduced per 1℃.

●Memory cell characteristics (VCC=1.8～5.5V,BR93L□□-W)

Parameter	Limit			Unit	Condition
	Min.	Typ.	Max.		
Number of data rewrite times *1	1,000,000	-	-	Times	Ta=25℃
Data hold years *1	40	-	-	Years	Ta=25℃

○Shipment data all address FFFFh
*1 Not 100% TESTED

●Memory cell characteristics (VCC=2.5～5.5V,BR93A□□-WM)

Parameter	Limit			Unit	Condition
	Min.	Typ.	Max.		
Number of data rewrite times *1	1,000,000			Times	Ta≦25℃
	100,000				Ta≦105℃
Data hold years *1	40	-	-	Years	Ta≦25℃
	10	-	-		Ta≦50℃

○Shipment data all address FFFFh
*1 Not 100% TESTED

●Recommended action conditions (BR93L□□-W)

Parameter	Symbol	Limits	Unit
Power source voltage	VCC	1.8～5.5	V
Input voltage	VIN	0～VCC	

●Recommended action conditions (BR93A□□-WM)

Parameter	Symbol	Limits	Unit
Power source voltage	VCC	2.5～5.5	V
Input voltage	VIN	0～VCC	

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●Electrical characteristics

(Unless otherwise specified, VCC=2.5～5.5V, Ta=-40～+85℃, BR93L□□-W, Ta=-40～+105℃, BR93A□□-WM)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
“L” input voltage 1	V_{IL1}	-0.3	-	+0.8	V	4.0V≦VCC≦5.5V
“L” input voltage 2	V_{IL2}	-0.3	-	0.2 x VCC	V	VCC≦4.0V
“H” input voltage 1	V_{IH1}	2.0	-	VCC+0.3	V	4.0V≦VCC≦5.5V
“H” input voltage 2	V_{IH2}	0.7 x VCC	-	VCC+0.3	V	VCC≦4.0V
“L” output voltage 1	V_{OL1}	0	-	0.4	V	I_{OL}=2.1mA, 4.0V≦VCC≦5.5V
“L” output voltage 2	V_{OL2}	0	-	0.2	V	I_{OL}=100μA
“H” output voltage 1	V_{OH1}	2.4	-	VCC	V	I_{OH}=-0.4mA, 4.0V≦VCC≦5.5V
“H” output voltage 2	V_{OH2}	VCC-0.2	-	VCC	V	I_{OH}=-100μA
Input leak current	I_{LI}	-1	-	+1	μA	V_{IN}=0V～VCC
Output leak current	I_{LO}	-1	-	+1	μA	V_{OUT}=0V～VCC, CS=0V
Current consumption at action	I_{CC1}	-	-	3.0	mA	f_{SK}=2MHz, $t_{E/W}$=5ms (WRITE)
	I_{CC2}	-	-	1.5	mA	f_{SK}=2MHz (READ)
	I_{CC3}	-	-	4.5	mA	f_{SK}=2MHz, $t_{E/W}$=5ms (WRAL, ERAL)
Standby current	I_{SB}	-	-	2	μA	CS=0V, DO=OPEN

◎Radiation resistance design is not made.

(Unless otherwise specified, VCC=1.8～2.5V, Ta=-40～+85℃, BR93L□□-W)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
“L” input voltage	V_{IL}	-0.3	-	0.2 x VCC	V	
“H” input voltage	V_{IH}	0.7 x VCC	-	VCC+0.3	V	
“L” output voltage	V_{OL}	0	-	0.2	V	I_{OL}=100μA
“H” output voltage	V_{OH}	VCC-0.2	-	VCC	V	I_{OH}=-100μA
Input leak current	I_{LI}	-1	-	+1	μA	V_{IN}=0V～VCC
Output leak current	I_{LO}	-1	-	+1	μA	V_{OUT}=0V～VCC, CS=0V
Current consumption at action	I_{CC1}	-	-	1.5	mA	f_{SK}=500kHz, $t_{E/W}$=5ms (WRITE)
	I_{CC2}	-	-	0.5	mA	f_{SK}=500kHz (READ)
	I_{CC3}	-	-	2	mA	f_{SK}=500kHz, $t_{E/W}$=5ms (WRAL, ERAL)
Standby current	I_{SB}	-	-	2	μA	CS=0V, DO=OPEN

◎Radiation resistance design is not made.

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●Action timing characteristics

(BR93L□□-W, Ta=-40～+85℃, VCC=2.5～5.5V, BR93A□□-WM, Ta=-40～+105℃, VCC=2.5～5.5V)

Parameter	Symbol	2.5V≦VCC≦5.5V			Unit
		Min.	Typ.	Max.	
SK frequency	f_{SK}	-	-	2	MHz
SK “H” time	t_{SKH}	230	-	-	ns
SK “L” time	t_{SKL}	230	-	-	ns
CS “L” time	t_{CS}	200	-	-	ns
CS setup time	t_{CSS}	50	-	-	ns
DI setup time	t_{DIS}	100	-	-	ns
CS hold time	t_{CSH}	0	-	-	ns
DI hold time	t_{DIH}	100	-	-	ns
Data “1” output delay time	t_{PD1}	-	-	200	ns
Data “0” output delay time	t_{PD0}	-	-	200	ns
Time from CS to output establishment	t_{SV}	-	-	150	ns
Time from CS to High-Z	t_{DF}	-	-	150	ns
Write cycle time	$t_{E/W}$	-	-	5	ms

(BR93L□□-W, Ta=-40～+85℃, VCC=1.8～2.5V)

Parameter	Symbol	1.8V≦VCC≦2.5V			Unit
		Min.	Typ.	Max.	
SK frequency	f_{SK}	-	-	500	kHz
SK “H” time	t_{SKH}	0.8	-	-	us
SK “L” time	t_{SKL}	0.8	-	-	us
CS “L” time	t_{CS}	1	-	-	us
CS setup time	t_{CSS}	200	-	-	ns
DI setup time	t_{DIS}	100	-	-	ns
CS hold time	t_{CSH}	0	-	-	ns
DI hold time	t_{DIH}	100	-	-	ns
Data “1” output delay time	t_{PD1}	-	-	0.7	us
Data “0” output delay time	t_{PD0}	-	-	0.7	us
Time from CS to output establishment	t_{SV}	-	-	0.7	us
Time from CS to High-Z	t_{DF}	-	-	200	ns
Write cycle time	$t_{E/W}$	-	-	5	ms

●Sync data input / output timing

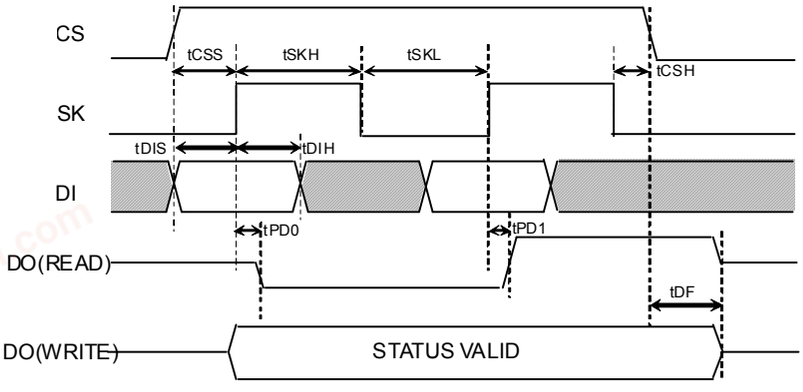


Fig.1 Sync data input / output timing

○Data is taken by DI sync with the rise of SK.
○At read action, data is output from DO in sync with the rise of SK.
○The status signal at write (READY / BUSY) is output after tCS from the fall of CS after write command input, at the area DO where CS is “H”, and valid until the next command start bit is input. And, while CS is “L”, DO becomes High-Z.
○After completion of each mode execution, set CS “L” once for internal circuit reset, and execute the following action mode.

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●BR93L□□-W Characteristic data (The following characteristic data are Typ. values.)

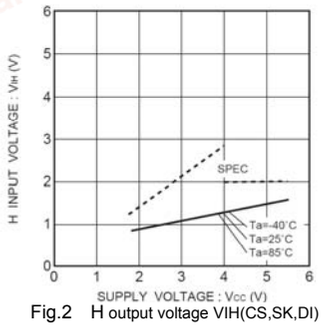


Fig.2 H output voltage VIH(CS,SK,DI)

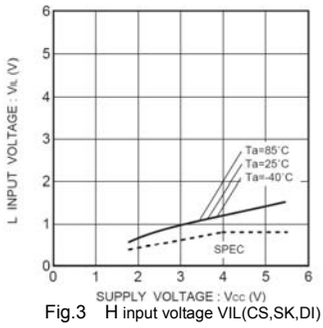


Fig.3 H input voltage VIL(CS,SK,DI)

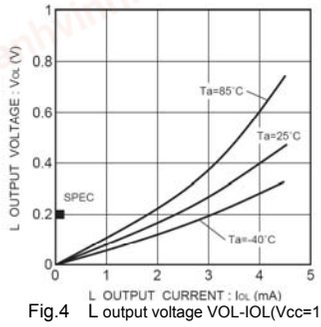


Fig.4 L output voltage VOL-IOL(Vcc=1.8V)

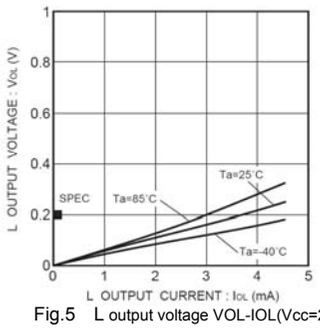


Fig.5 L output voltage VOL-IOL(Vcc=2.5V)

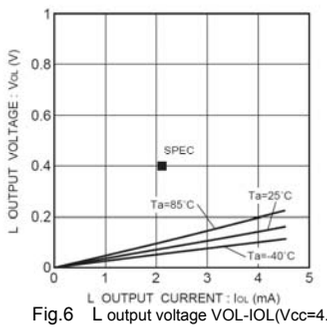


Fig.6 L output voltage VOL-IOL(Vcc=4.0V)

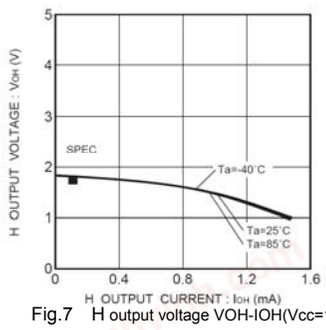


Fig.7 H output voltage VOH-IOH(Vcc=1.8V)

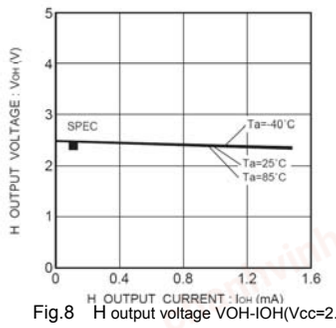


Fig.8 H output voltage VOH-IOH(Vcc=2.5V)

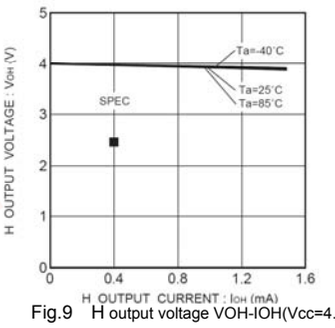


Fig.9 H output voltage VOH-IOH(Vcc=4.0V)

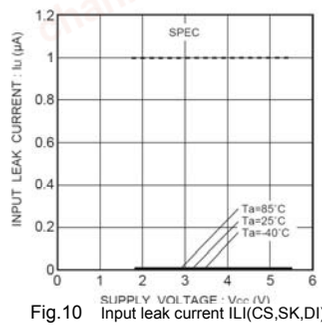


Fig.10 Input leak current ILI(CS,SK,DI)

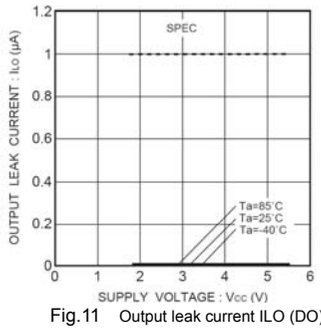


Fig.11 Output leak current ILO (DO)

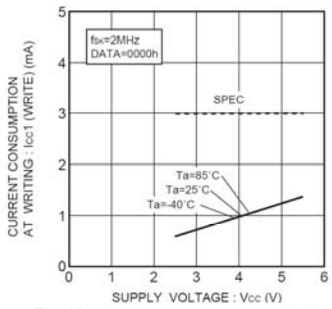


Fig.12 Current consumption at WRITE action ICC1 (WRITE, fSK=2MHz)

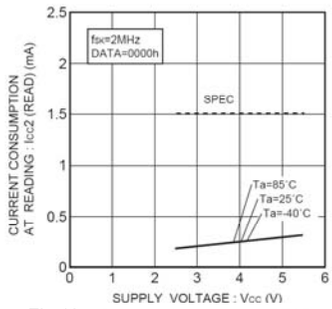


Fig.13 Consumption current at READ action ICC2 (READ, fSK=2MHz)

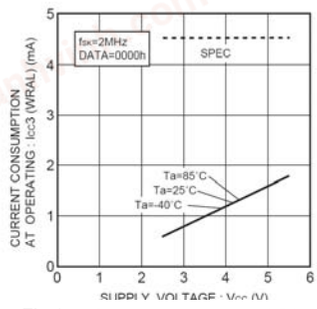


Fig.14 Consumption current at WRAL action ICC3 (WRAL, fSK=2MHz)

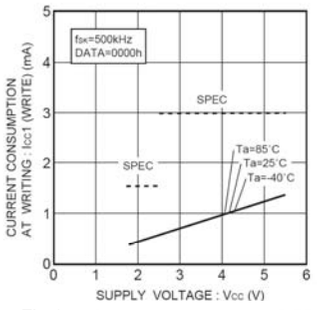


Fig.15 Current consumption at WRITE action ICC1 (WRITE, fSK=500kHz)

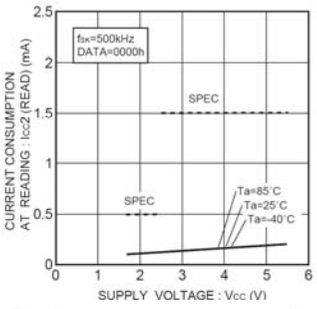


Fig.16 Consumption current at READ action ICC2 (READ, fSK=500kHz)

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●BR93L□□-W Characteristic data (The following characteristic data are Typ. values.)

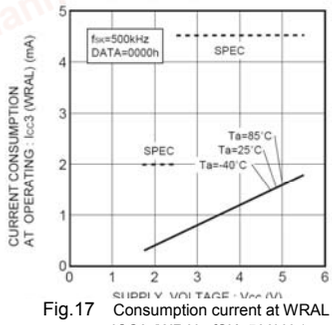


Fig.17 Consumption current at WRAL action ICC3 (WRAL, fSK=500kHz)

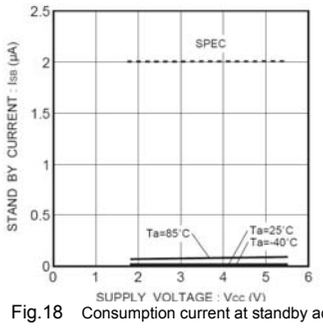


Fig.18 Consumption current at standby action ISB

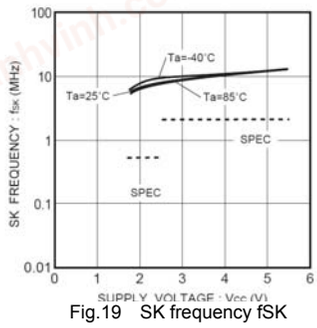


Fig.19 SK frequency fSK

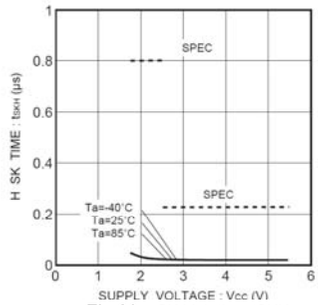


Fig.20 SK high time tSKH

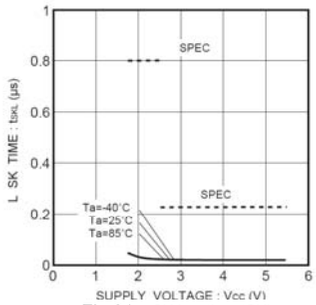


Fig.21 SK low time tSKL

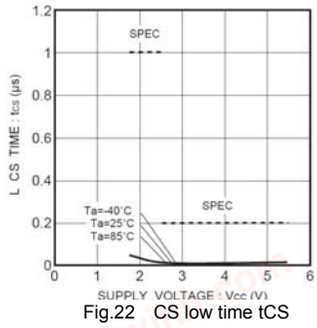


Fig.22 CS low time tCS

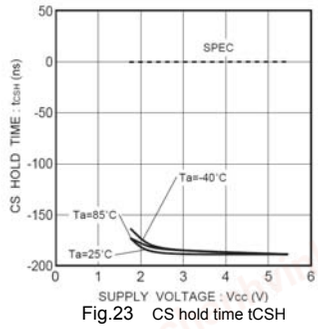


Fig.23 CS hold time tCSH

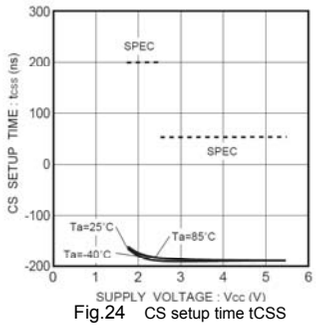


Fig.24 CS setup time tCSS

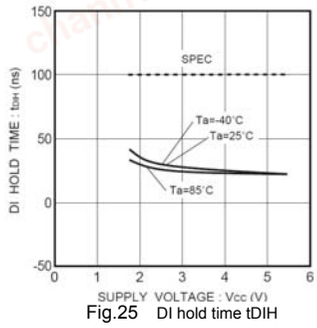


Fig.25 DI hold time tDIH

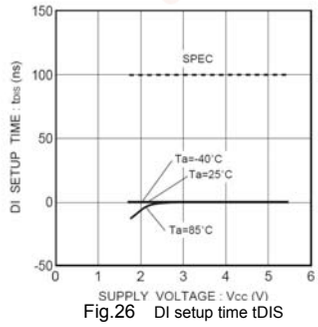


Fig.26 DI setup time tDIS

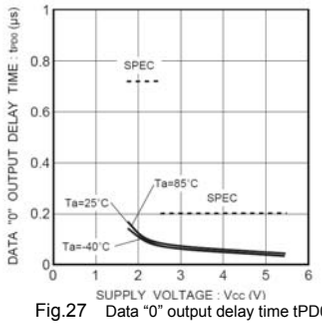


Fig.27 Data “0” output delay time tPD0

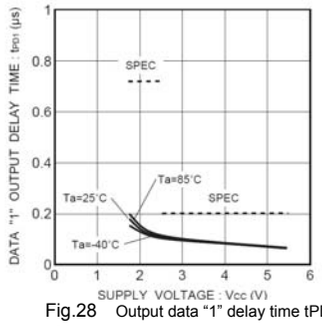


Fig.28 Output data “1” delay time tPD1

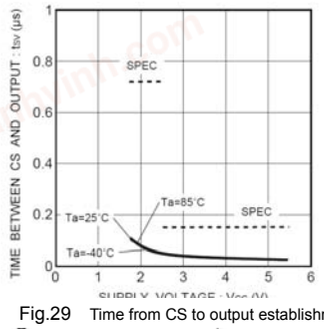


Fig.29 Time from CS to output establishment tSV

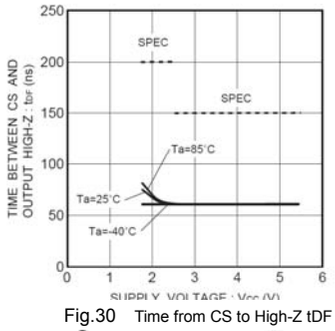


Fig.30 Time from CS to High-Z tDF

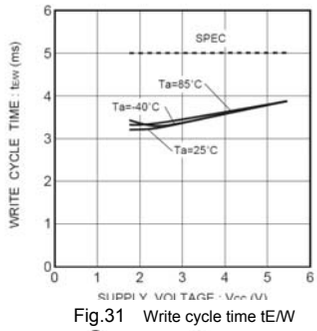


Fig.31 Write cycle time tE/W

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●BR93A□□-WM Characteristic data (The following characteristic data are Typ. values.)

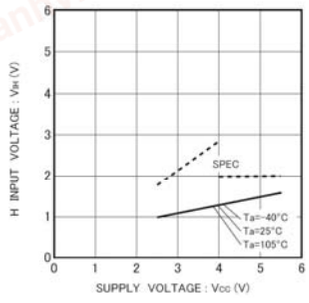


Fig.32 H output voltage VIH(CS,SK,DI)

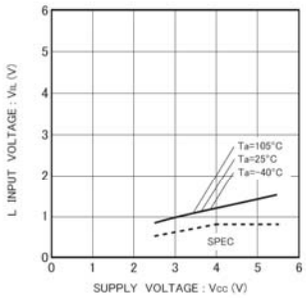


Fig.33 H input voltage VIL(CS,SK,DI)

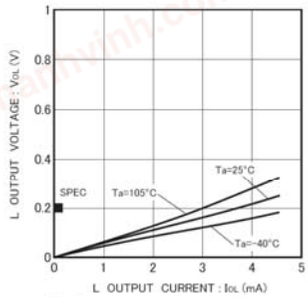


Fig.34 L output voltage VOL-IOL(Vcc=2.5V)

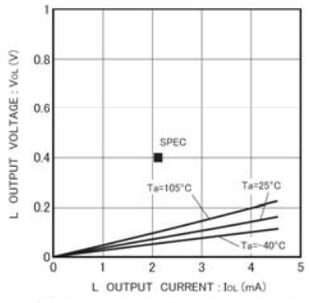


Fig.35 L output voltage VOL-IOL(Vcc=4.0V)

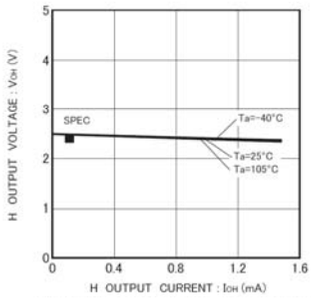


Fig.36 H output voltage VOH-IOH(Vcc=2.5V)

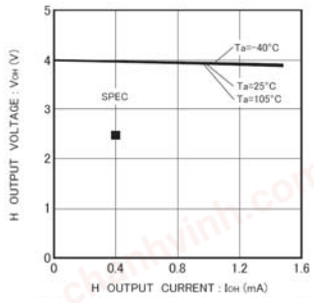


Fig.37 H output voltage VOH-IOH(Vcc=4.0V)

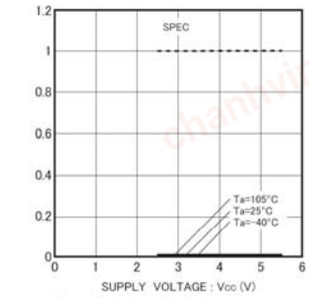


Fig.38 Input leak current ILI(CS,SK,DI)

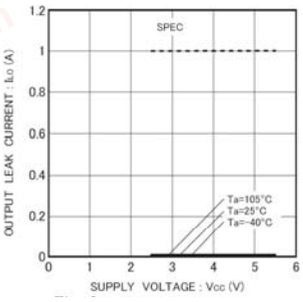


Fig.39 Output leak current ILO(DO)

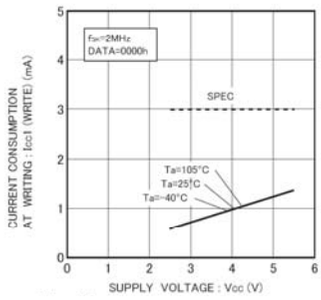


Fig.40 Current consumption at WRITE action Icc1(WRITE, fSK=2MHz)

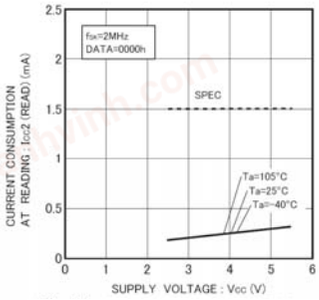


Fig.41 Consumption current at READ action Icc2(READ, fSK=2MHz)

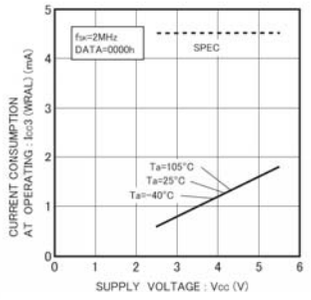


Fig.42 Consumption current at WRAL action Icc3(WRAL, fSK=2MHz)

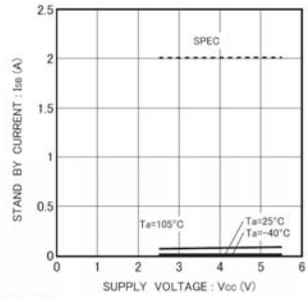


Fig.43 Consumption current at standby action ISB

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●BR93A□□-WM Characteristic data (The following characteristic data are Typ. values.)

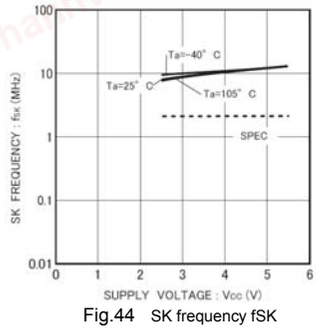


Fig.44 SK frequency fSK

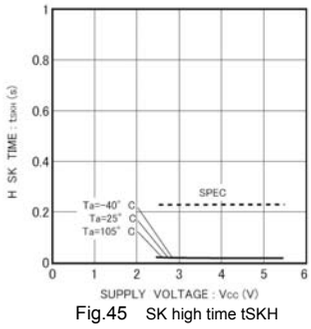


Fig.45 SK high time tSKH

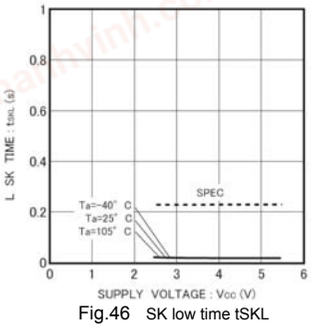


Fig.46 SK low time tSKL

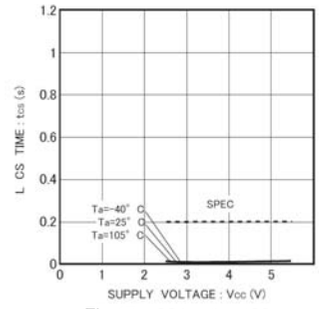


Fig.47 CS low time tCS

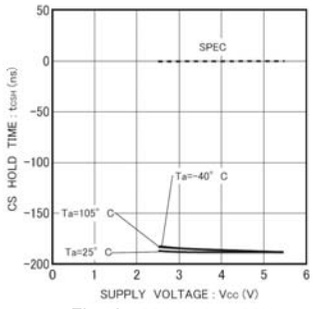


Fig.48 CS hold time tCSH

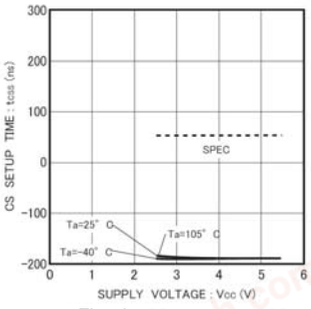


Fig.49 CS setup time tCSS

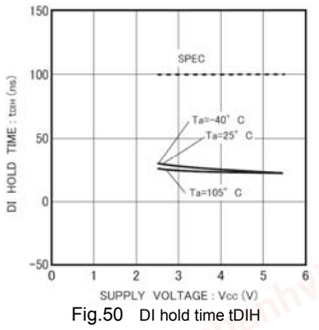


Fig.50 DI hold time tDIH

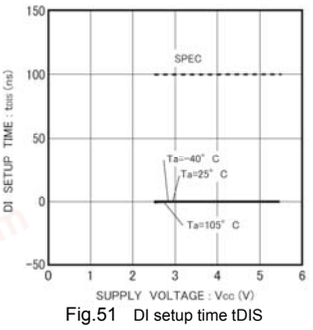


Fig.51 DI setup time tDIS

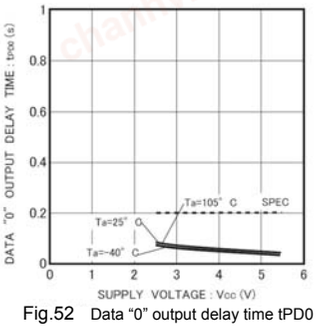


Fig.52 Data "0" output delay time tPD0

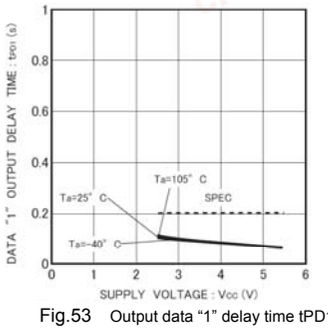


Fig.53 Output data "1" delay time tPD1

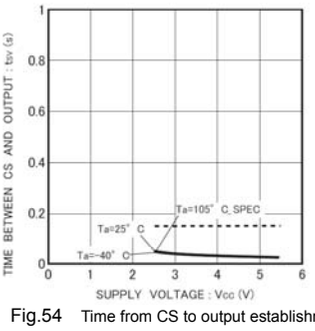


Fig.54 Time from CS to output establishment tSV

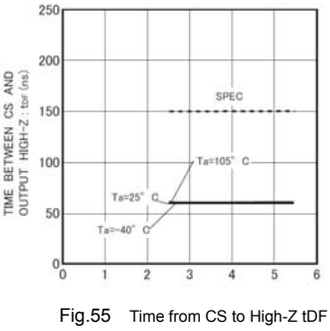


Fig.55 Time from CS to High-Z tDF

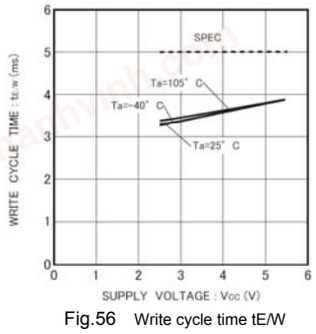


Fig.56 Write cycle time tE/W

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●Block diagram

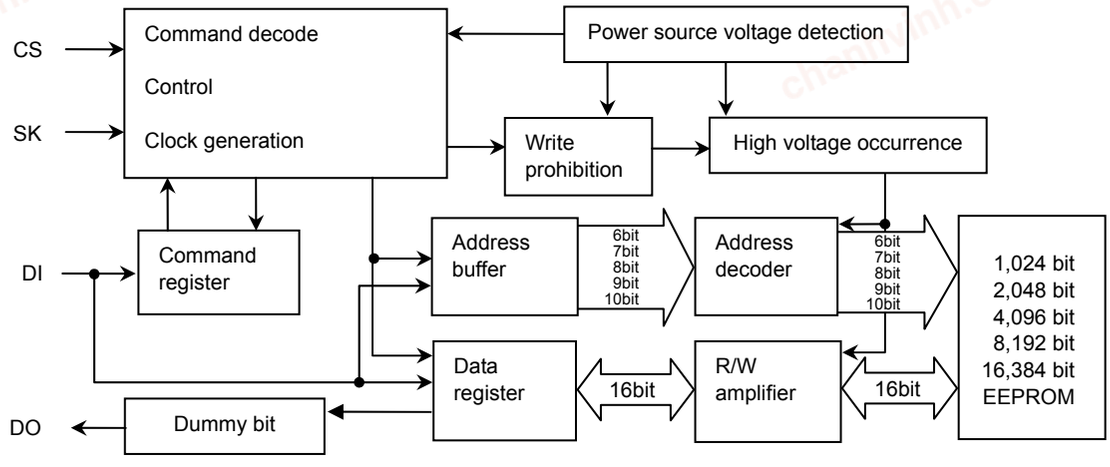
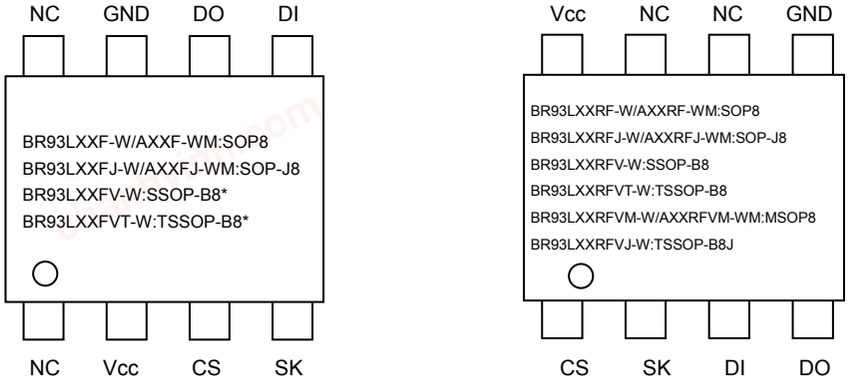


Fig.57 Block diagram

●Pin assignment and function



*BR93L46/56/66-W

Fig.58 Pin assignment diagram

Pin name	I / O	Function
VCC	-	Power source
GND	-	All input / output reference voltage, 0V
CS	Input	Chip select input
SK	Input	Serial clock input
DI	Input	Start bit, ope code, address, and serial data input
DO	Output	Serial data output, READY / $\overline{\text{BUSY}}$ internal condition display output
NC	-	Non connected terminal, Vcc, GND or OPEN

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●Description of operations

Communications of the Microwire Bus are carried out by SK (serial clock), DI (serial data input),DO (serial data output) ,and CS (chip select) for device selection.

When to connect one EEPROM to a microcontroller, connect it as shown in Fig.59(a) or Fig.59(b). When to use the input and output common I/O port of the microcontroller, connect DI and DO via a resistor as shown in Fig.59(b) (Refer to pages 17/35.), and connection by 3 lines is available.

In the case of plural connections, refer to Fig. 59 (c).

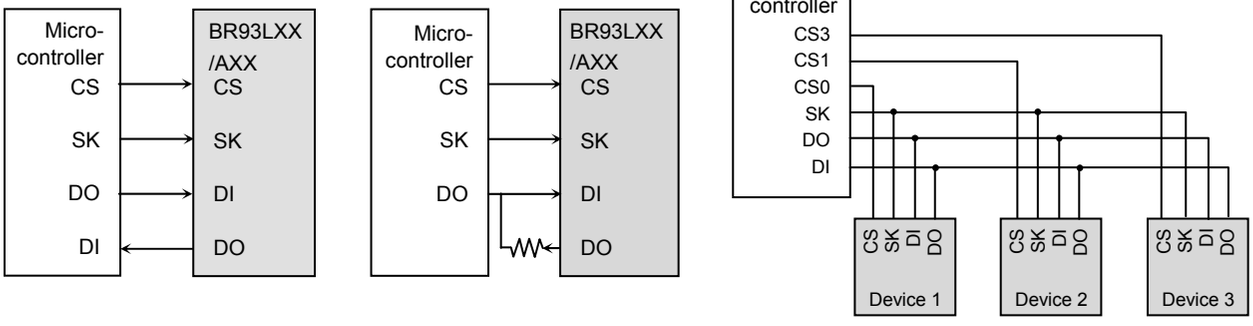


Fig.59-(a) Connection by 4 lines

Fig.59-(b) Connection by 3 lines

Fig.59-(c) Connection example of plural devices

Fig.59 Connection method with microcontroller

Communications of the Microwire Bus are started by the first “1” input after the rise of CS. This input is called a start bit. After input of the start bit, input ope code, address and data. Address and data are input all in MSB first manners.

“0” input after the rise of CS to the start bit input is all ignored. Therefore, when there is limitation in the bit width of PIO of the microcontroller, input “0” before the start bit input, to control the bit width.

●Command mode

Command	Start bit	Ope code	Address			Data
			BR93L46-W BR93A46-WM	BR93L56/66-W BR93A56/66-WM	BR93L76/86-W BR93A76/86-WM	
Read (READ) *1	1	10	A5,A4,A3,A2,A1,A0	A7,A6,A5,A4,A3,A2,A1,A0	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15~D0(READ DATA)
Write enable (WEN)	1	00	1 1 ****	1 1 ******	1 1 ********	
Write (WRITE) *2	1	01	A5,A4,A3,A2,A1,A0	A7,A6,A5,A4,A3,A2,A1,A0	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15~D0(WRITE DATA)
Write all (WRAL) *2	1	00	0 1 ****	0 1 ******	0 1 ********	D15~D0(WRITE DATA)
Write disable (WDS)	1	00	0 0 ****	0 0 ******	0 0 ********	
Erase (ERASE)	1	11	A5,A4,A3,A2,A1,A0	A7,A6,A5,A4,A3,A2,A1,A0	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	
Chip erase (ERAL)	1	00	1 0 ****	1 0 ******	1 0 ********	

・ Input the address and the data in MSB first manners.
・ As for *, input either VIH or VIL.

A7 of BR93L56-W/A56-WM becomes Don't Care.
A9 of BR93L76-W/A76-WM becomes Don't Care.

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The start bit means the first “1” input after the rise of CS.

*1 As for read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are sequentially output continuously. (Auto increment function)

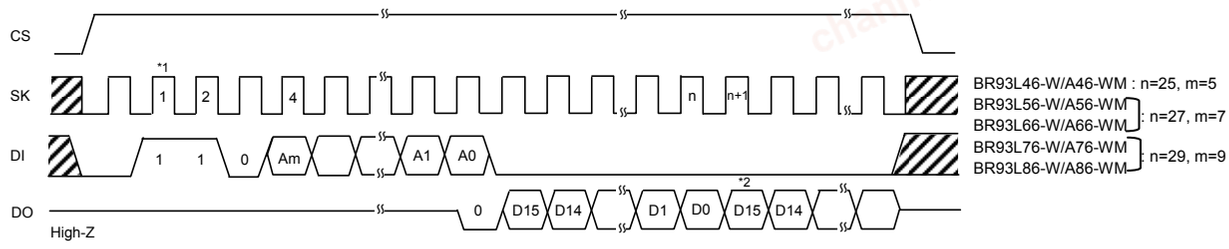
*2 When the read and the write all commands are executed, data written in the selected memory cell is automatically deleted, and input data is written.

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●Timing chart

1) Read cycle (READ)



*1 Start bit
When data “1” is input for the first time after the rise of CS, this is recognized as a start bit. And when “1” is input after plural “0” are input, it is recognized as a start bit, and the following operation is started. This is common to all the commands to described hereafter.

Fig. 60 Read cycle

○When the read command is recognized, input address data (16bit) is output to serial. And at that moment, at taking A0, in sync with the rise of SK, “0” (dummy bit) is output. And, the following data is output in sync with the rise of SK.
This IC has an address auto increment function valid only at read command. This is the function where after the above read execution, by continuously inputting SK clock, the above address data is read sequentially. And, during the auto increment, keep CS at “H”.

2) Write cycle (WRITE)

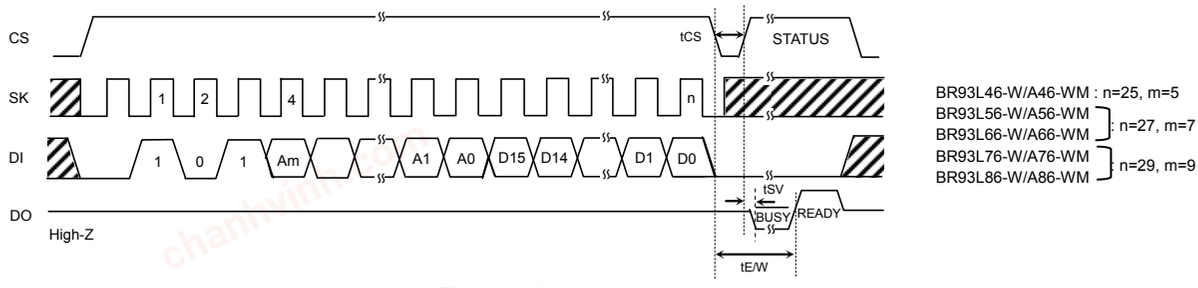


Fig.61 Write cycle

○In this command, input 16bit data (D15~D0) are written to designated addresses (Am~A0). The actual write starts by the fall of CS of D0 taken SK clock.
When STATUS is not detected, (CS=”L” fixed) Max. 5ms in conformity with tE/W, and when STATUS is detected (CS=”H”), all commands are not accepted for areas where “L” ($\overline{\text{BUSY}}$) is output from D0, therefore, do not input any command.

3) Write all cycyle (WRAL)

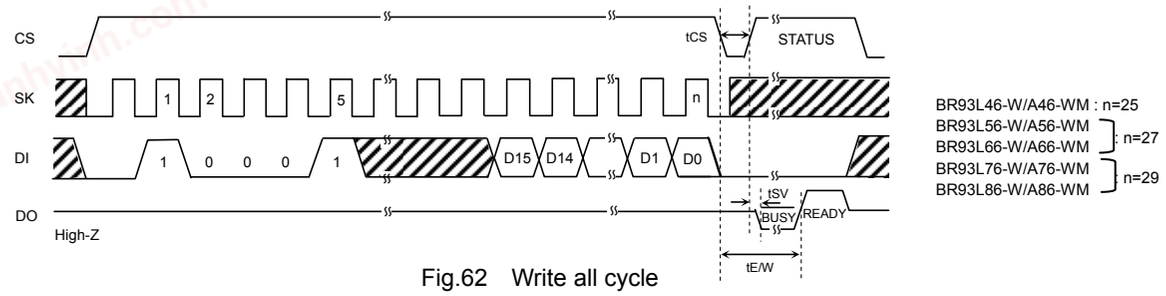


Fig.62 Write all cycle

○In this command, input 16bit data is written simultaneously to all adresses. Data is not written continuously per one word but is written in bulk, the write time is only Max. 5ms in conformity with tE/W.

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4) Write enable (WEN) / disable (WDS) cycle

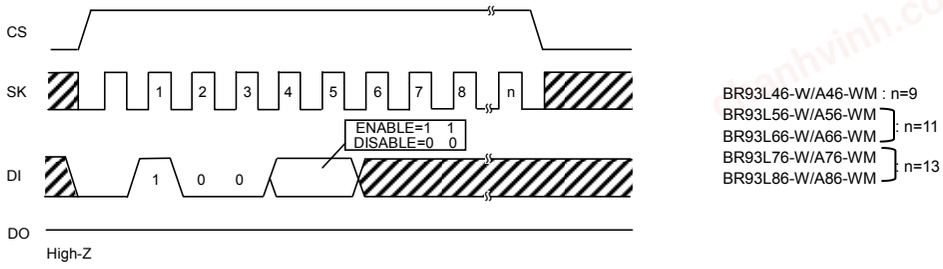


Fig.63 Write enable (WEN) / disable (WDS) cycle

○ At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid unitl the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / diable command. Input to SK after 6 clocks of this command is available by either “H” or “L”, but be sure to input it.

○ When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is canceled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by mistake, write is started. To prevent such a mistake, it is recommended to execute the write disable command after completion of write.

5) Erase cycle timing (ERASE)

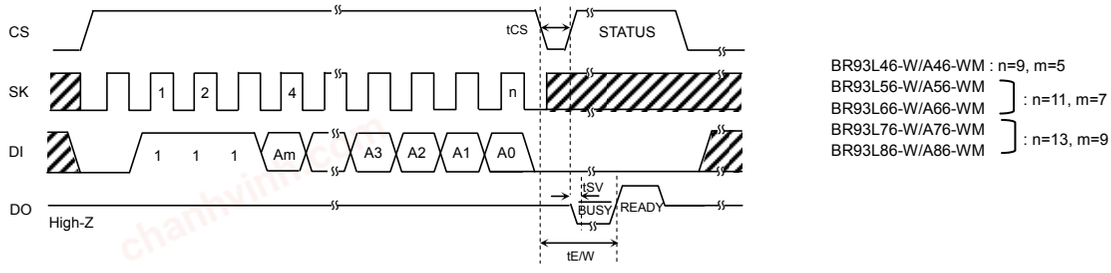


Fig.64 Erase cycle timing

○In this command, data of the designated address is made into “1”. The data of the designated address becomes “FFFFh”.
Actual ERASE starts at the fall of CS after the fall of A0 taken SK clock.
In ERASE, status can be detected in the same manner as in WRITE command.

6) Chip erase cycle timing (ERAL)

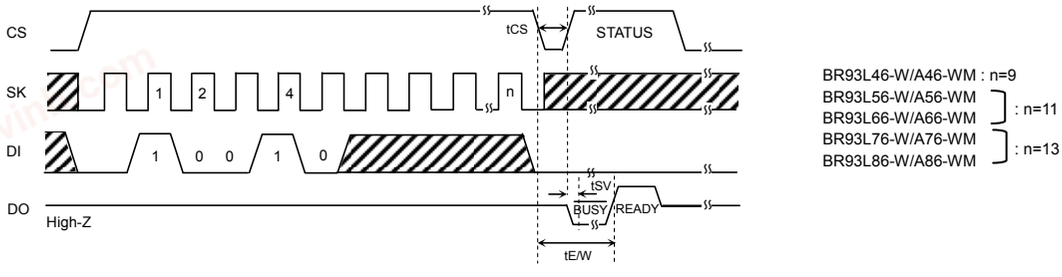


Fig.65 Chip erase cycle timing

○In this command, data of all addresses is erased. Data of all addresses becomes ”FFFFh”.
Actual ERASE starts at the fall of CS after the falll of the n-th clock from the start bit input.
In ERAL, status can be detected in the same manner as in WRITE command.

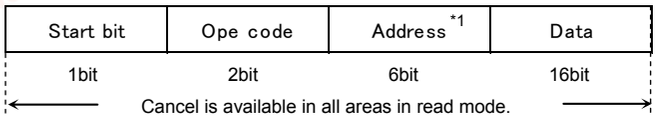
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●Application

1) Method to cancel each command

○READ



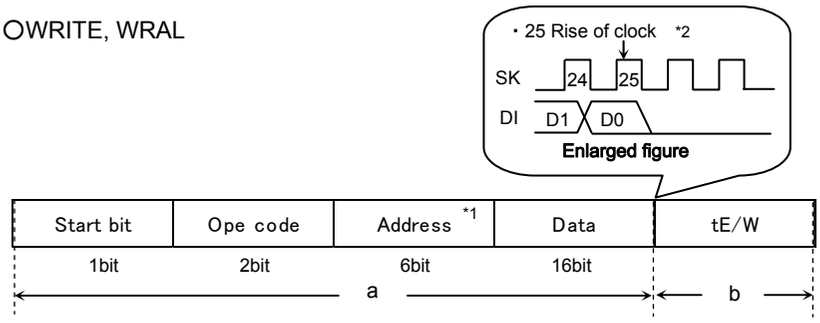
(In the case of BR93L46-W/A46-WM)

・Method to cancel : cancel by CS="L"

＊1 Address is 8 bits in BR93L56-W/A56-WM, BR93L-66W/A66-WM
Address is 10 bits in BR93L76-W/A76-WM, BR93L86-W/A86-WM

Fig.66 READ cancel available timing

○WRITE, WRAL

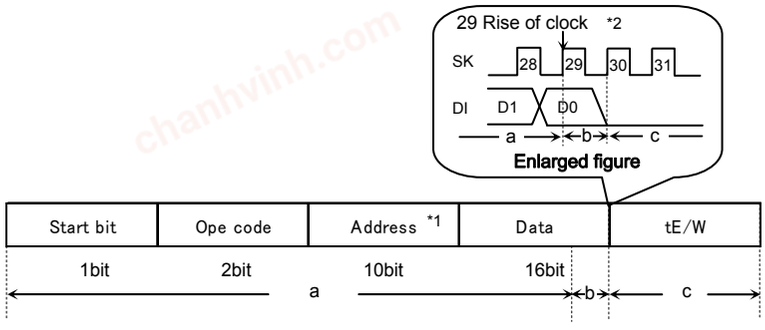


(In the case of BR93L46-W/A46-WM)

a : From start bit to 25 clock rise*2
Cancel by CS="L"

b : 25 clock rise and after*2
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.
And when SK clock is input continuously, cancellation is not available.

*1 Address is 8 bits in BR93L56-W/A56-WM, BR93L66-W/A66-WM
Address is 10 bits in BR93L76-W/A76-WM BR93L86-W/A86-WM
*2 27 clocks in BR93L56-W/A56-WM, BR93L66-W/A66-WM
29 clocks in BR93L76-W/A76-WM BR93L86-W/A86-WM



(In the case of BR93L86-W/A86-WM)

a : From start bit to 29 clock rise
Cancel by CS="L"

b : 29 clock rise and after
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.

c : 30 clock rise and after
Cancel by CS="L"
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is output continuously is not available.

Note 1) If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.

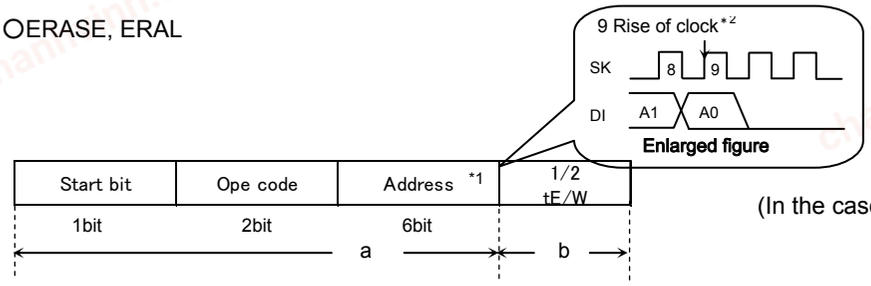
Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable, therefore, it is recommended to fail in SK="L" area.
As for SK rise, recommend timing of tCSS/tCSH or higher.

Fig.67 WRITE, WRAL cancel available timing

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○ERASE, ERAL



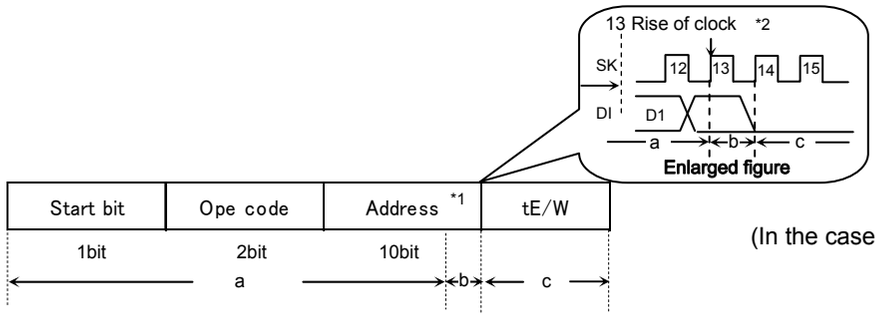
(In the case of BR93L46-W/A46-WM)

a : From start bit to 9 clock rise*2
Cancel by CS="L"

b : 9 clock rise and after*2
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.
And when SK clock is input continuously, cancellation is not available.

＊1 Address is 8 bits in BR93L56-W/A56-WM, BR93L66-W/A66-WM
Address is 10 bits in BR93L76-W/A76-WM

＊2 11 clocks in BR93L56-W/A56-WM, BR93L66-W/A66-WM
13 clocks in BR93L76-W/A76-WM



(In the case of BR93L86-W/A86-WM)

a : From start bit to 13 clock rise
Cancel by CS="L"

b : 13 clock rise and after
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.

c : 14 clock rise and after
Cancel by CS="L"
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is output continuously is not available.

Note 1) If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.

Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable, therefore, it is recommended to fail in SK="L" area.
As for SK rise, recommend timing of tCSS/tCSH or higher.

Fig.68 ERASE, ERAL cancel available timing

2) At standby

○Standby current

When CS is "L", SK input is "L", DI input is "H", and even with middle electric potential, current does not increase.

○Timing

As shown in Fig.69, when SK at standby is "H", if CS is started, DI status may be read at the rise edge.
At standby and at power ON/OFF, when to start CS, set SK input or DI input to "L" status. (Refer to Fig.70)

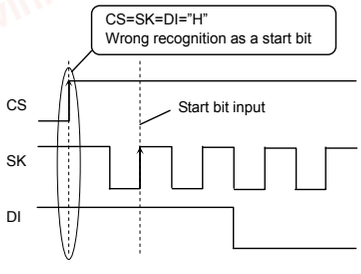


Fig.69 Wrong action timing

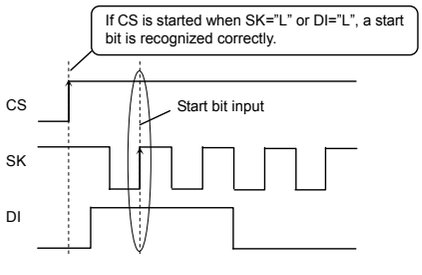


Fig.70 Normal action timing

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3) Equivalent circuit

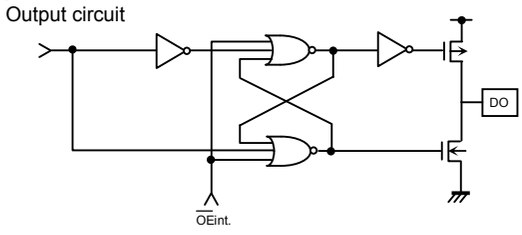


Fig.71 Output circuit (DO)

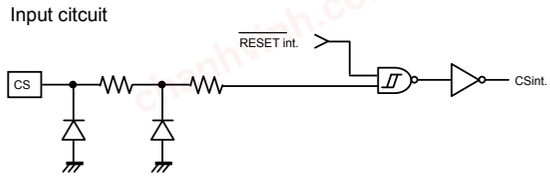


Fig.72 Input circuit (CS)

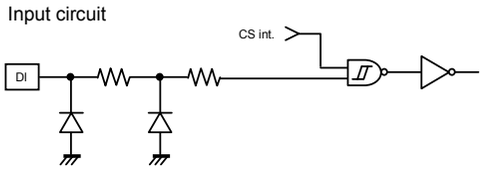


Fig.73 Input circuit (DI)

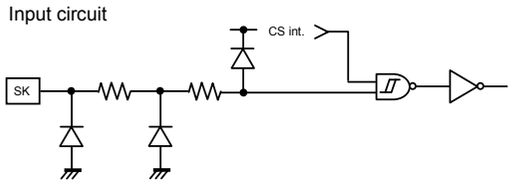


Fig.74 Input circuit (SK)

4) I/O peripheral circuit

4-1) Pull down CS.

By making CS="L" at power ON/OFF, mistake in operation and mistake write are prevented.

○Pull down resistance Rpd of CS pin

To prevent mistake in operation and mistake write at power ON/OFF, CS pull down resistance is necessary. Select an appropriate value to this resistance value from microcontroller VOH, IOH, and VIL characteristics of this IC.

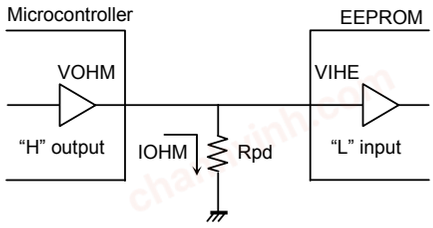


Fig.75 CS pull down resistance

$$Rpd \geqq \frac{VOHM}{IOHM} \quad \cdots ①$$

$$VOHM \geqq VIHE \quad \cdots ②$$

Example) When V_{CC} =5V, VIHE=2V, VOHM=2.4V, IOHM=2mA, from the equation ①,

$$Rpd \geqq \frac{2.4}{2 \times 10^{-3}}$$

$$\therefore \quad Rpd \geqq 1.2\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, VOHM becomes 2.4V or higher, and VIHE (=2.0V), the equation ② is also satisfied.

- VIHE : EEPROM VIH specifications
- VOHM : Microcontroller VOH specifications
- IOHM : Microcontroller IOH specifications

4-2) DO is available in both pull up and pull down.

Do output become "High-Z" in other READY / BUSY output timing than after data output at read command and write command. When malfunction occurs at "High-Z" input of the microcontroller port connected to DO, it is necessary to pull down and pull up DO. When there is no influence upon the microcontroller actions, DO may be OPEN.

If DO is OPEN, and at timing to output status READY, at timing of CS="H", SK="H", DI="H", EEPROM recognizes this as a start bit, resets READY output, and DO="High-Z", therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

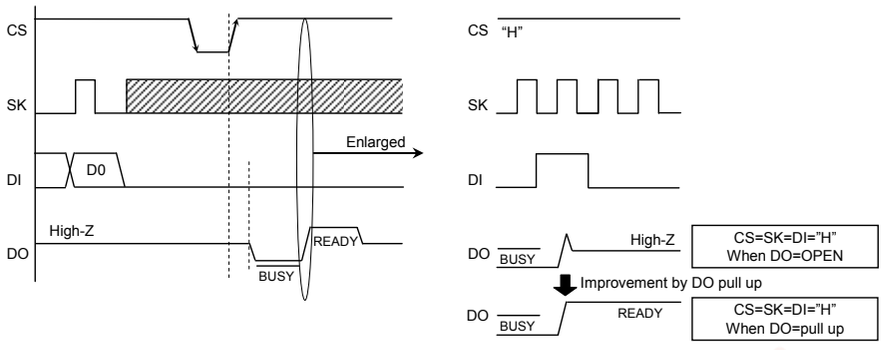


Fig.76 READY output timing at DO=OPEN

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○Pull up resistance Rpu and pull down resistance Rpd of DO pin

As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller VIH, VIL, and VOH, IOH, VOL, IOL characteristics of this IC.

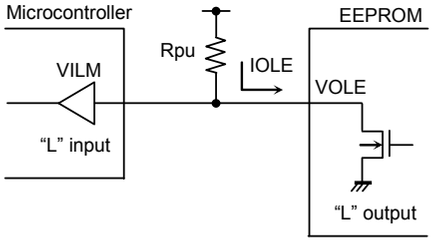


Fig.77 DO pull up resistance

$$Rpu \geqq \frac{Vcc-VOLE}{IOLE} \quad \cdot\cdot\cdot ③$$

$$VOLE \leqq VILM \quad \cdot\cdot\cdot ④$$

Example) When V_{CC} =5V, VOLE=0.4V, IOLE=2.1mA, VILM=0.8V, from the equation ③,

$$Rpu \geqq \frac{5-0.4}{2.1\times10^{-3}}$$

$$\therefore \quad Rpu \geqq 2.2\ [k\Omega]$$

With the value of Rpu to satisfy the above equation, VOLE becomes 0.4V or below, and with VILM(=0.8V), the equation ④ is also satisfied.

- VOLE : EEPROM VOL specifications
- IOLE : EEPROM IOL specifications
- VILM : Microcontroller VIL specifications

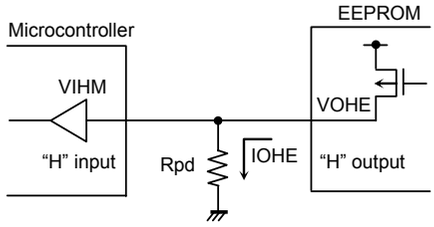


Fig.78 DO pull down resistance

$$Rpd \geqq \frac{VOHE}{IOHE} \quad \cdot\cdot\cdot ⑤$$

$$VOHE \geqq VIHM \quad \cdot\cdot\cdot ⑥$$

Example) When V_{CC} =5V, VOHE=Vcc−0.2V, IOHE=0.1mA, VIHM=Vcc×0.7V from the equation ⑤,

$$Rpd \geqq \frac{5-0.2}{0.1\times10^{-3}}$$

$$\therefore \quad Rpd \geqq 48\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, VOHE becomes 2.4V or below, and with VIHM (=3.5V), the equation ⑥ is also satisfied.

- VOHE : EEPROM VOH specifications
- IOHE : EEPROM IOH specifications
- VIHM : Microcontroller VIH specifications

5) READY / $\overline{BUSY}$ status display (DO terminal)

(common to BR93L46-W/A46-WM,BR93L56-W/A56-WM, BR93L66-W/A66-WM, BR93L76-W/A76-WM, BR93L86-W/A86-WM)

This display outputs the internal status signal. When CS is started after tCS (Min.200ns) from CS fall after write command input, "H" or "L" is output.

R/$\overline{B}$ display＝"L" ($\overline{BUSY}$) = write under execution

(DO status) After the timer circuit in the IC works and creates the period of tE/W, this time circuit completes automatically. And write to the memory cell is made in the period of tE/W, and during this period, other command is not accepted.

R/$\overline{B}$ display = "H" (READY) = command wait status

(DO status) Even after tE/W (max.5ms) from write of the memory cell, the following command is accepted. Therefore, CS="H" in the period of tE/W, and when input is in SK, DI, malfunction may occur, therefore, DI="L" in the area CS="H". (Especially, in the case of shared input port, attention is required.)

*Do not input any command while status signal is output. Command input in $\overline{BUSY}$ area is cancelled, but command input in READY area is accepted. Therefore, status READY output is cancelled, and malfunction and mistake write may be made.

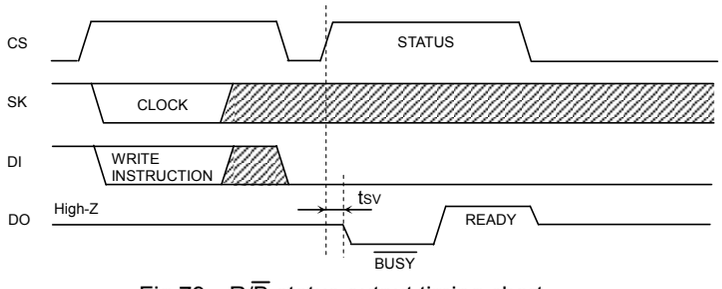


Fig.79 R/$\overline{B}$ status output timing chart

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6) When to directly connect DI and DO

This IC has independent input terminal DI and output terminal DO, and separate signals are handled on timing chart, meanwhile, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by 1 control line.

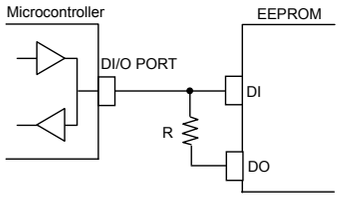


Fig.80 DI, DO control line common connection

○Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input.

Drive from the microcontroller DI/O output to DI input on I/O timing, and signal output from DO output occur at the same time in the following points.

(1) 1 clock cycle to take in A0 address data at read command

Dummy bit "0" is output to DO terminal.

→When address data A0 = "1" input, through current route occurs.

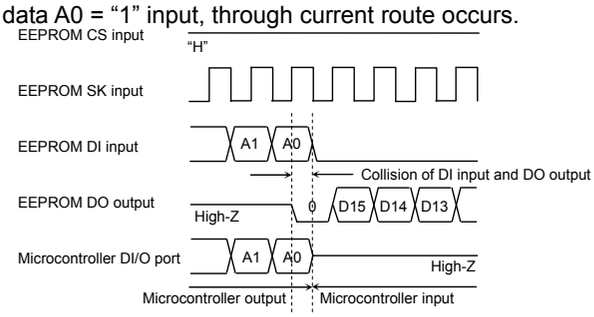


Fig.81 Collision timing at read data output at DI, DO direct connection

(2) Timing of CS = "H" after write command. DO terminal in $\overline{\text{READY}}$ / BUSY function output.

When the next start bit input is recognized, "HIGH-Z" gets in.

→Especially, at command input after write, when CS input is started with microcontroller DI/O output "L", READY output "H" is output from DO terminal, and through current route occurs.

Feedback input at timing of these (1) and (2) does not cause disorder in basic operations, if resistance R is inserted.

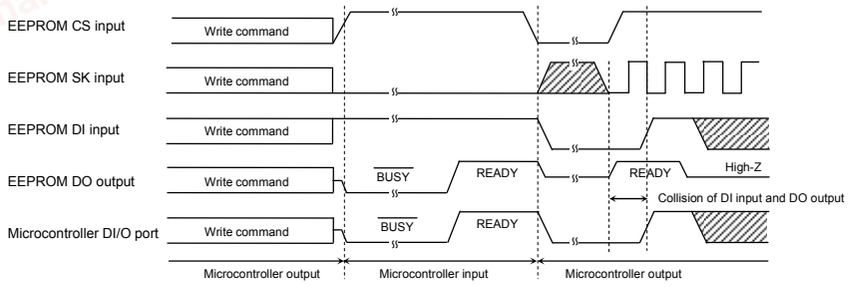


Fig.82 Collision timing at DI, DO direct connection

Note) As for the case (2), attention must be paid to the following.

When status READY is output, DO and DI are shared, DI="H" and the microcontroller DI/O="High-Z" or the microcontroller DI/O="H",if SK clock is input, DO output is input to DI and is recognized as a start bit, and malfunction may occur. As a method to avoid malfunction, at status READY output, set SK="L", or start CS within 4 clocks after "H" of READY signal is output.

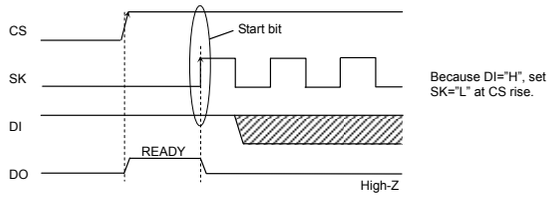


Fig.83 Start bit input timing at DI, DO direct connection

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○Selection of resistance value R

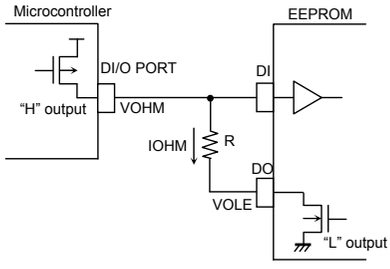
The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level VIH/VIL even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

(1) Address data A0 = "1" input, dummy bit "0" output timing

(When microcontroller DI/O output is "H", EEPROM DO outputs "L", and "H" is input to DI)

・Make the through current to EEPROM 10mA or below.

・See to it that the level VIH of EEPROM should satisfy the following.



Conditions

$$VOHM \geqq VIHE$$

$$VOHM \geqq IOHM \times R + VOLE$$

At this moment, if VOLE=0V,

$$VOHM \geqq IOHM \times R$$

$$\therefore \quad R \geqq \frac{VOHM}{IOHM} \quad \cdots ⑦$$

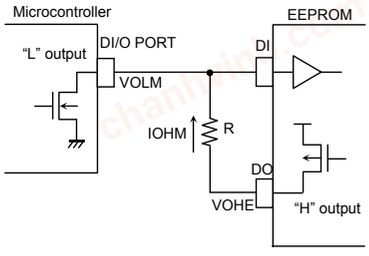
・VIHE : EEPROM VIH specifications
・VOLE : EEPROM VOL specifications
・VOHM : Microcontroller VOH specifications
・IOHM : Microcontroller IOH specifications

Fig.84 Circuit at DI, DO direct connection (Microcontroller DI/O "H" output, EEPROM "L" output)

(2) DO status READY output timing

(When the microcontroller DI/O is "L", EEPROM DO output "H", and "L" is input to DI)

・Set the EEPROM input level VIL so as to satisfy the following.



Conditions

$$VOLM \geqq VILE$$

$$VOLM \geqq VOHE - IOLM \times R$$

As this moment, VOHE=Vcc

$$VOLM \geqq Vcc - IOLM \times R$$

$$\therefore \quad \frac{Vcc - VOLM}{IOLM} \quad \cdots ⑧$$

・VILE : EEPROM VIL specifications
・VOHE : EEPROM VOH specifications
・VOLM : Microcontroller VOL specifications
・IOLM : Microcontroller IOL specifications

Example) When Vcc=5V, VOHM=5V, IOHM=0.4mA, VOLM=5V, IOLM=0.4mA,

From the equation ⑦,

$$R \geqq \frac{VOHM}{IOHM}$$

$$R \geqq \frac{5}{0.4 \times 10^{-3}}$$

$$\therefore \quad R \geqq 12.5\ [k\Omega] \quad \cdots ⑨$$

From the equation⑧,

$$R \geqq \frac{Vcc - VOLM}{IOLM}$$

$$R \geqq \frac{5 - 0.4}{2.1 \times 10^{-3}}$$

$$\therefore \quad R \geqq 2.2\ [k\Omega] \quad \cdots ⑩$$

Therefore, from the equations ⑨ and ⑩,

$$\therefore \quad R \geqq 12.5\ [k\Omega]$$

Fig.85 Circuit at DI, DO direct connection (Microcontroller DI/O "L" output, EEPROM "H" output)

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7) Notes on power ON/OFF

・At power ON/OFF, set CS “L”.

When CS is “H”, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CS “L”. (When CS is in “L” status, all inputs are cancelled.) And at power decline, owing to power line capacity and so forth, low power status may continue long. At this case too, owing to the same reason, malfunction, mistake write may occur, therefore, at power OFF too, set CS “L”.

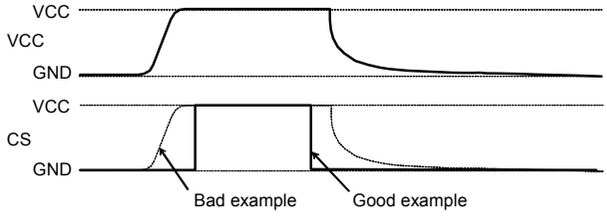


Fig.86 Timing at power ON/OFF

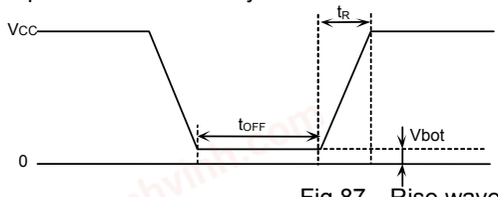
（Bad example）CS pin is pulled up to Vcc.
In this case, CS becomes “H” (active status), and EEPROM may have malfunction, mistake write owing to noise and the likes.
Even when CS input is High-Z, the status becomes like this case, which please note.

（Good example）It is “L” at power ON/OFF.
Set 10ms or higher to recharge at power OFF.
When power is turned on without observing this condition, IC internal circuit may not be reset, which please note.

○POR citcuit

This IC has a POR (Power On Reset) circuit as a mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is “H” at power ON/OFF, it may become write enable status owing to noises and the likes. For secure actions, observe the follwing conditions.

1. Set CS=”L”
2. Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit action.



Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Fig.87 Rise waveform diagram

○LVCC circuit

LVCC (VCC-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ.=1.2V) or below, it prevent data rewrite.

8) Noise countermeasures

○VCC noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC VCC and GND, At that moment, attach it as close to IC as possible.And, it is also recommended to attach a bypass capacitor between board VCC and GND.

○SK noise

When the rise time (tR) of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement.To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (tR) of SK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

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●Note ofn use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our IC.

(3) Absolute Maximum Ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, IC may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to IC.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(5) Heat design
In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging
When to package IC onto a board, pay sufficient attention to IC direction and displacement. Wrong packaging may destruct IC. And in the case of shortcircuit between IC terminals and terminals and power source, terminal and GND owing to foreign matter, IC may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently

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Serial EEPROM Series

High Reliability Series EEPROMs Microwire BUS

BR93H□□-WC Series

●Description

BR93H□□-WC Series is a serial EEPROM of serial 3-line interface method.

●Features

1) Withstands electrostatic voltage 8kV, (twice more than other series)（HBM method typ.）
2) Wide action range -40℃～+125℃（-40℃～+85℃, -40℃～+105℃ in other series）
3) Conforming to Microwire BUS
4) Highly reliable connection by Au pad and Au wire
5) Address auto increment function at read action
6) Write mistake prevention function
   - Write prohibition at power on
   - Write prohibition by command code
   - Write mistake prevention circuit at low voltage
7) Program cycle auto delete and auto end function
8) Program condition display by READY / BUSY
9) Low current consumption
   - At write action (at 5V) : 0.6mA (Typ.)
   - At read action (at 5V) : 0.6mA (Typ.)
   - At standby action (at 5V) : 0.1μA (Typ.)(CMOS input)
10) Built-in noise filter CS, SK, DI terminals
11) Compact package SOP8/SOP-J8
12) High reliability by ROHM original Double-Cell structure
13) High reliability ultrafine CMOS process
14) Easily connectable with serial port BR93H series
15) Data retention for 40 years
16) Data rewrite up to 1,000,000 times
17) Data at shipment all address FFFFh

●BR93H Series

Capacity	Bit format	Type	Power source voltage	SOP8		SOP-J8	
Package type				F	RF	FJ	RFJ
2Kbit	128×16	BR93H56-WC	2.7～5.5V		●		●
4Kbit	256×16	BR93H66-WC	2.7～5.5V		●		●
8Kbit	512×16	BR93H76-WC	2.7～5.5V		●		●
16Kbit	1K×16	BR93H86-WC	2.7～5.5V		●		●

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●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Impressed voltage	VCC	-0.3～+6.5	V
Permissible dissipation	Pd	560 (SOP8) *1	mW
		560 (SOP-J8) *2	
Storage temperature range	Tstg	-65～+150	℃
Action temperature range	Topr	-40～+125	℃
Terminal voltage	-	-0.3～VCC+0.3	V

*When using at Ta=25℃ or higher, 4.5mW(*1,*2), to be reduced per 1℃.

●Memory cell characteristics (VCC=2.7～5.5V)

Parameter	Limit			Limit	Limit
	Min.	Typ.	Max.		
Number of data rewrite times *1	1,000,000	-	-	Times	Ta≦85℃
	500,000	-	-	Times	Ta≦105℃
	300,000	-	-	Times	Ta≦125℃
Data hold years	40	-	-	Years	Ta≦25℃
	20	-	-	Years	Ta≦85℃

*1 Not 100% TESTED

●Recommended action conditions

Parameter	Symbol	Limits	Unit
Power source voltage	VCC	2.7～5.5	V
Input voltage	VIN	0～VCC	

●Electrical characteristics (Unless otherwise specified, Ta=-40～+125℃, VCC=2.7～5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
“L” input voltage	VIL	-0.3	-	0.3xVCC	V	
“H” input voltage	VIH	0.7xVCC	-	VCC+0.3	V	
“L” output voltage 1	VOL1	0	-	0.4	V	IOL=2.1mA, 4.0V≦VCC≦5.5V
“L” output voltage 2	VOL2	0	-	0.2	V	IOL=100μA
“H” output voltage 1	VOH1	2.4	-	VCC	V	IOH=-0.4mA, 4.0V≦VCC≦5.5V
“H” output voltage 2	VOH2	VCC-0.2	-	VCC	V	IOH=-100μA
Input leak current	ILI	-10	-	10	μA	VIN=0V～VCC
Output leak current	ILO	-10	-	10	μA	VOUT=0V～VCC, CS=0V
Current consumption at action	ICC1	-	-	3.0	mA	fSK=1.25MHz, tE/W=10ms (WRITE)
	ICC2	-	-	1.5	mA	fSK=1.25MHz (READ)
	ICC3	-	-	4.5	mA	fSK=1.25MHz, tE/W=10ms (WRAL)
Standby current	ISB	-	0.1	10	μA	CS=0V, DO=OPEN

◎Radiation resistance design is not made.

●Action timing characteristics (Unless otherwise specified, Ta=-40～+125℃, VCC=2.7～5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SK frequency	fSK	-	-	1.25	MHz
SK “H” time	tSKH	250	-	-	ns
SK “L” time	tSKL	250	-	-	ns
CS “L” time	tCS	200	-	-	ns
CS setup time	tCSS	200	-	-	ns
DI setup time	tDIS	100	-	-	ns
CS hold time	tCSH	0	-	-	ns
DI hold time	tDIH	100	-	-	ns
Data “1” output delay time	tPD1	-	-	300	ns
Data “0” output delay time	tPD0	-	-	300	ns
Time from CS to output establishment	tSV	-	-	200	ns
Time from CS to High-Z	tDF	-	-	200	ns
Write cycle time	tE/W	-	7	10	ms

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●Sync data input / output timing

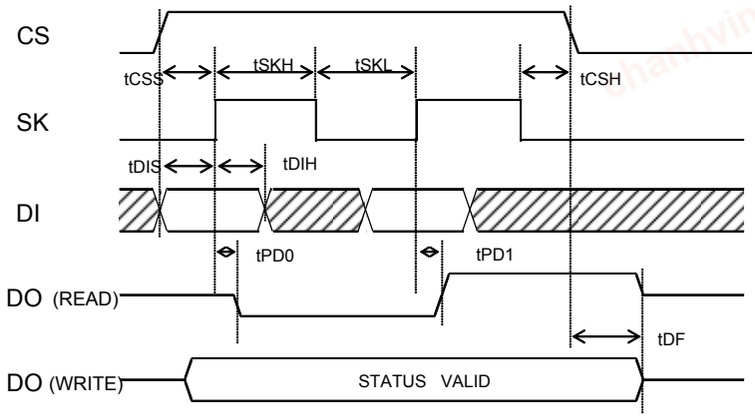


Fig.1 Sync data input / output timing diagram

○Data is taken by DI sync with the rise of SK.
○At read action, data is output from DO in sync with the rise of SK.
○The status signal at write (READY / $\overline{\text{BUSY}}$) is output after tCS from the fall of CS after write command input, at the area DO where CS is “H”, and valid until the next command start bit is input. And, white CS is “L”, DO becomes High-Z.
○After completion of each mode execution, set CS “L” once for internal circuit reset, and execute the following action mode.

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●BR93H□□-WC Characteristic data

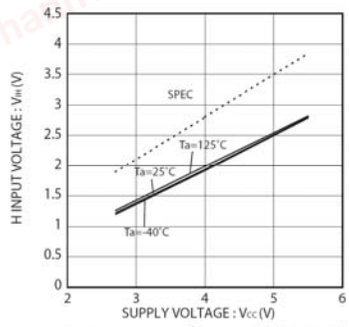


Fig.2 H input voltage VIH (CS,SK,DI)

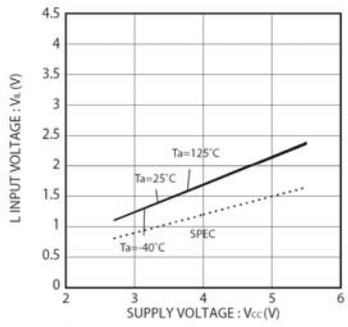


Fig.3 L input voltage VIL (CS,SK,DI)

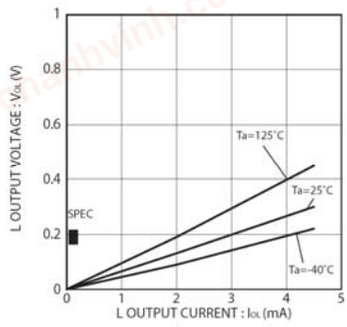


Fig.4 L output voltage VOL-IOL (VCC=2.7V)

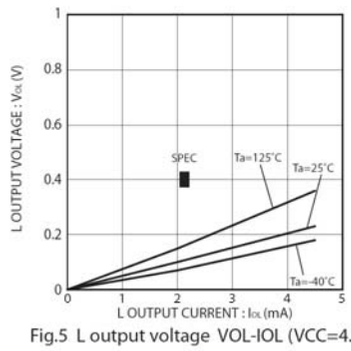


Fig.5 L output voltage VOL-IOL (VCC=4.0V)

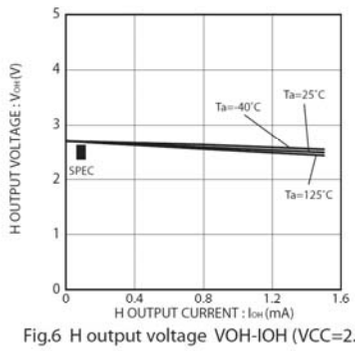


Fig.6 H output voltage VOH-IOH (VCC=2.7V)

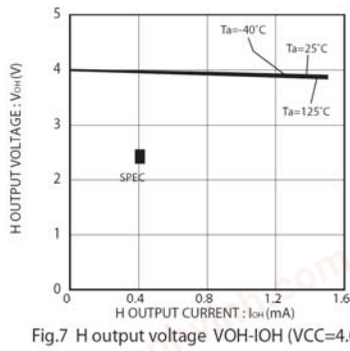


Fig.7 H output voltage VOH-IOH (VCC=4.0V)

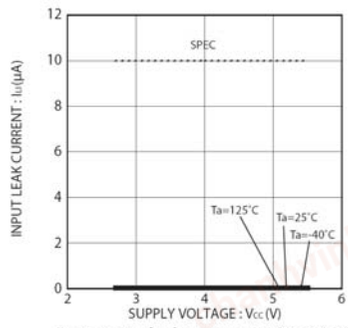


Fig.8 Input leak current ILI (CS,SK,DI)

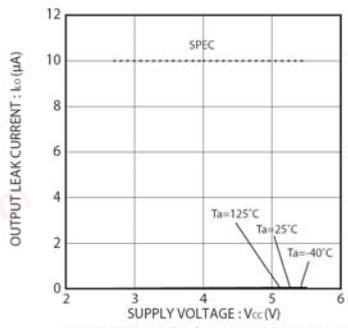


Fig.9 Output leak current ILO (DO)

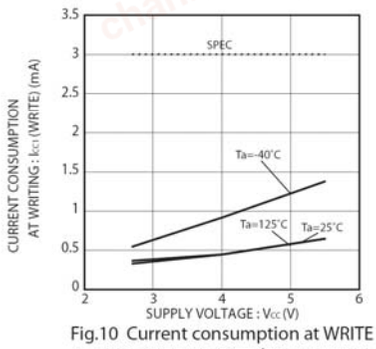


Fig.10 Current consumption at WRITE operation ICC1 (WRITE,fSK=1.25MHz)

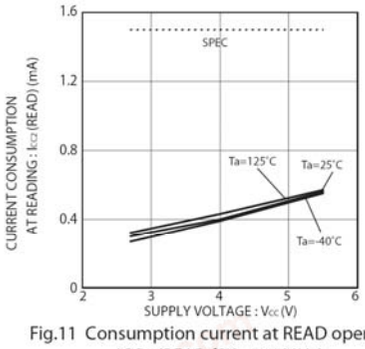


Fig.11 Consumption current at READ operation ICC2 (READ,fSK=1.25MHz)

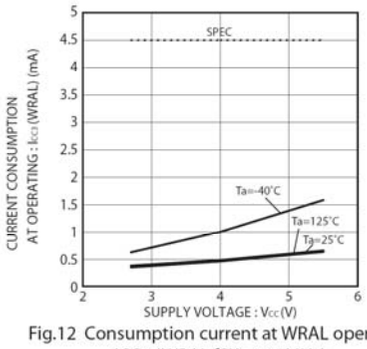


Fig.12 Consumption current at WRAL operation ICC3 (WRAL,fSK=1.25MHz)

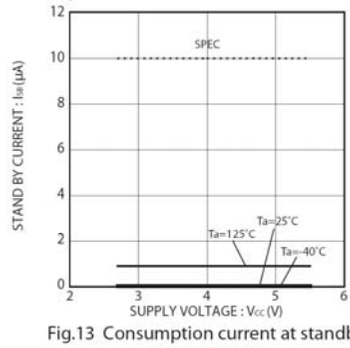


Fig.13 Consumption current at standby operation ISB

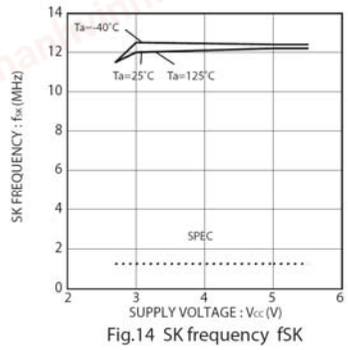


Fig.14 SK frequency fSK

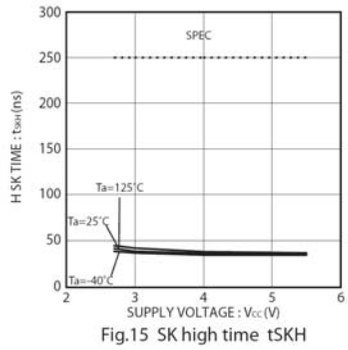


Fig.15 SK high time tSKH

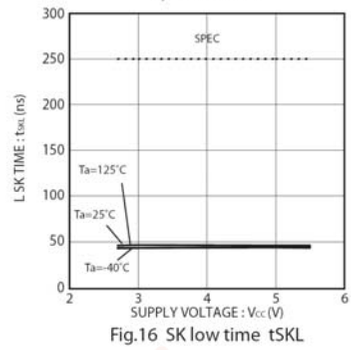


Fig.16 SK low time tSKL

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●BR93H□□-WC Characteristic data

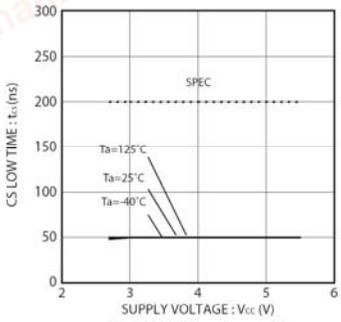


Fig.17 CS low time tCS

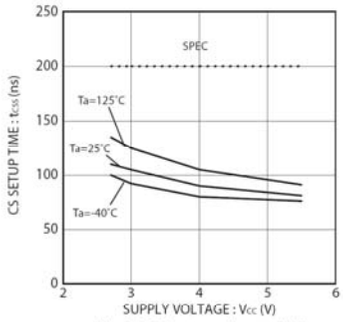


Fig.18 CS setup time tCSS

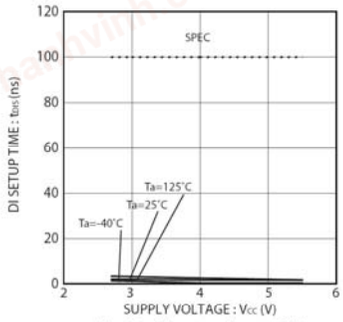


Fig.19 DI setup time tDIS

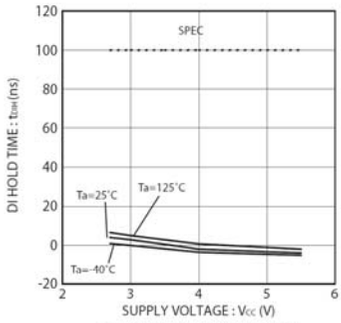


Fig.20 DI hold time tDIH

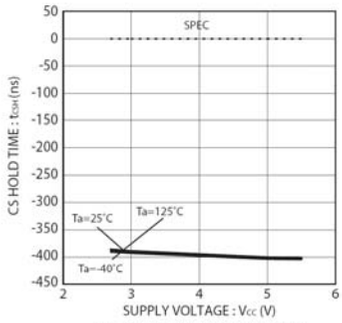


Fig.21 CS hold time tCSH

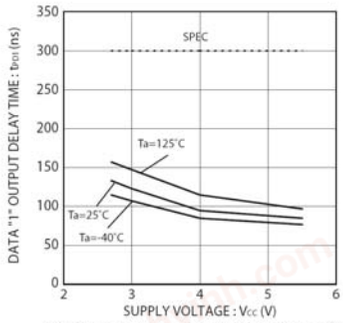


Fig.22 Data "1" output delay time tPD1

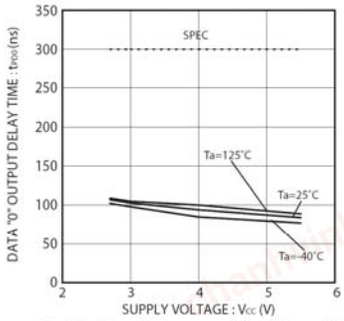


Fig.23 Data "0" output delay time tPD0

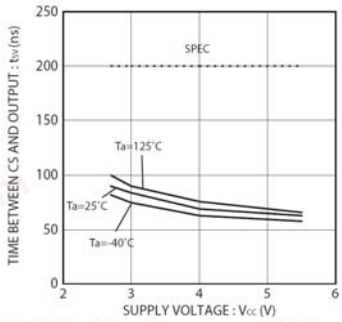


Fig.24 Time from CS to output establishment tSV

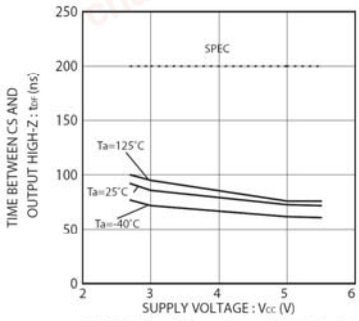


Fig.25 Time from CS to High-Z tDF

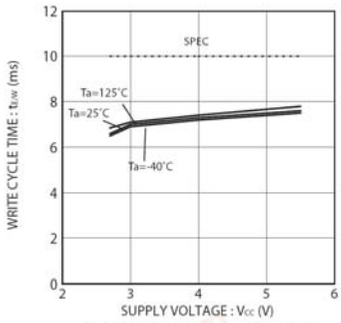


Fig.26 Write cycle time tE/W

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●Block diagram

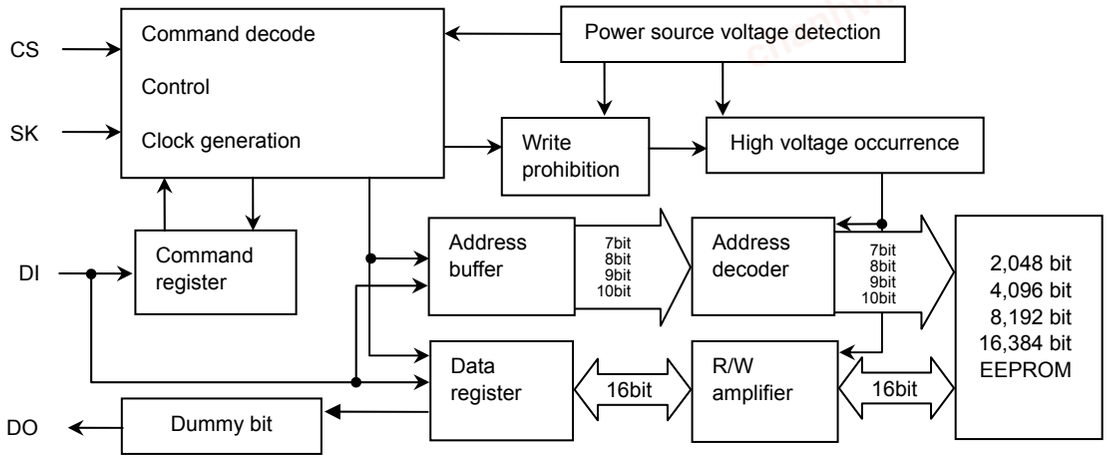


Fig. 27 Block diagram

●Pin assignment and function

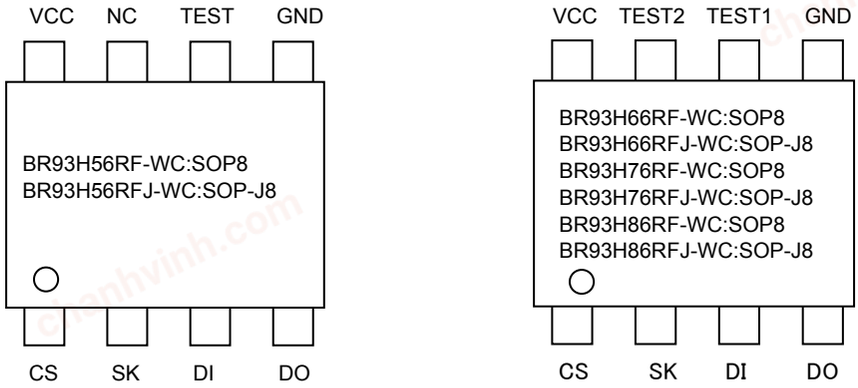


Fig.28 Pin assignment diagram

Pin name	I / O	Function
Vcc	-	Power source
GND	-	All input / output reference voltage, 0V
CS	Input	Chip select input
SK	Input	Serial clock input
DI	Input	Start bit, ope code, address, and serial data input
DO	Output	Serial data output, READY / $\overline{\text{BUSY}}$ internal condition display output
NC	-	Non connected terminal, Vcc, GND or OPEN
TEST1	-	TEST terminal, GND or OPEN
TEST2	-	TEST terminal, Vcc, GND or OPEN
TEST	-	TEST terminal, GND or OPEN

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●Description of operations

Communications of the Microwire Bus are carried out by SK (serial clock), DI (serial data input),DO (serial data output) ,and CS (chip select) for device selection.
When to connect one EEPROM to a microcontroller, connect it as shown in Fig.29-(a) or Fig.29-(b). When to use the input and output common I/O port of the microcontroller, connect DI and DO via a resistor as shown in Fig.29-(b) (Refer to pages 31/35.), and connection by 3 lines is available.
In the case of plural connections, refer to Fig. 29-(c).

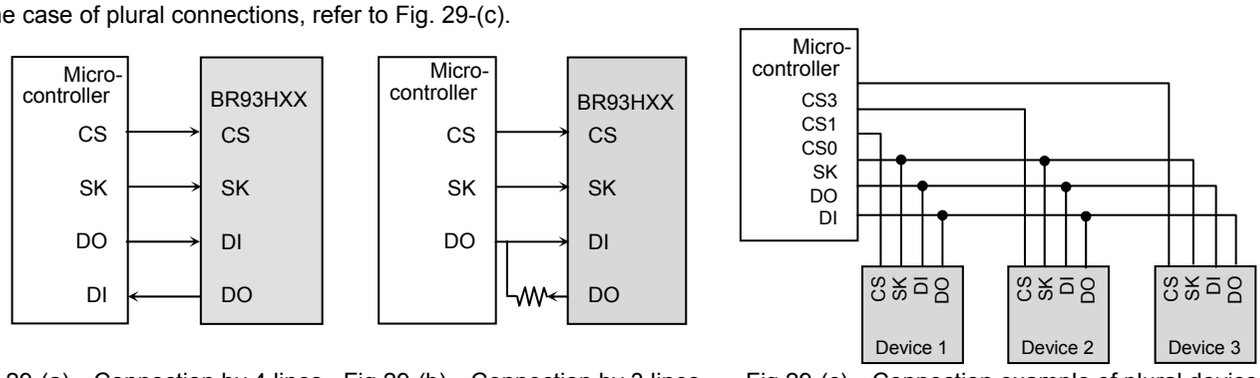


Fig.29-(a) Connection by 4 lines Fig.29-(b) Connection by 3 lines Fig.29-(c) Connection example of plural devices

Fig.29 Connection method with microcontroller

Communications of the Microwire Bus are started by the first “1” input after the rise of CS. This input is called a start bit. After input of the start bit, input ope code, address and data. Address and data are input all in MSB first manners.
“0” input after the rise of CS to the start bit input is all ignored. Therefore, when there is limitation in the bit width of PIO of the microcontroller, input “0” before the start bit input, to control the bit width.

●Command mode

Command		Start bit	Ope code	Address		Data
				BR93H56/66-WC	BR93H76/86-WC	
Read (READ)	*1	1	10	A7,A6,A5,A4,A3,A2,A1,A0	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15~D0(READ DATA)
Write enable (WEN)		1	00	1 1 ******	1 1 ********	
Write (WRITE)	*2	1	01	A7,A6,A5,A4,A3,A2,A1,A0	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15~D0(WRITE DATA)
Write all (WRAL)	*2,3	1	00	0 1 ***** B0	0 1 ***** B2,B1,B0	D15~D0(WRITE DATA)
Write disable (WDS)		1	00	0 0 ******	0 0 ********	

・ Input the address and the data in MSB first manners.
・ As for *, input either VIH or VIL.

A7 and B0 of BR93H56-WC becomes Don't Care.
A9 and B2 of BR93H76-WC becomes Don't Care.

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The start bit means the first “1” input after the rise of CS.

*1 As for read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are sequentially output continuously. (Auto increment function)
*2 When the read and the write all commands are executed, data written in the selected memory cell is automatically deleted, and input data is written.
*3 For the write all command, data written in memory cell of the areas designated by B2, B1, and B0, are automatically deleted, and input data is written in bulk.

●Write all area

B2	B1	B0	Write area
0	0	0	000h～07Fh
0	0	1	080h～0FFh
0	1	0	100h～17Fh
0	1	1	180h～1FFh
1	0	0	200h～27Fh
1	0	1	280h～2FFh
1	1	0	300h～37Fh
1	1	1	380h～3FFh

Designation of B2, B1, and B0

H56	*	*	*
H66	*	*	B0
H76	*	B1	B0
H86	B2	B1	B0

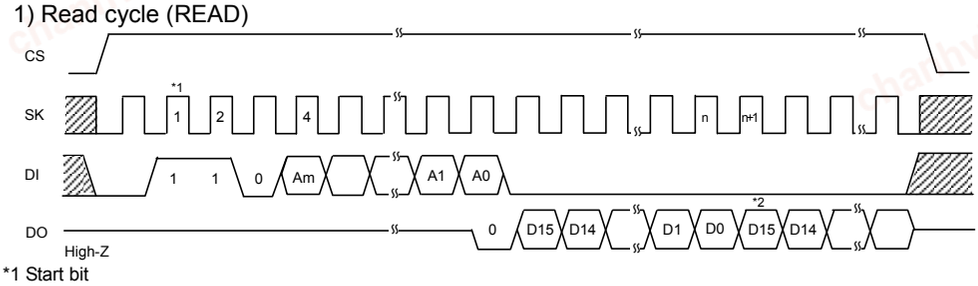
・The write all command is written in bulk in 2Kbit unit.
The write area can be selected up to 3bit. Confirm the settings and write areas of the above B2, B1, and B0.

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●Timing chart

1) Read cycle (READ)



BR93H56/66-WC : n=27, m=7
BR93H76/86-WC : n=29, m=9

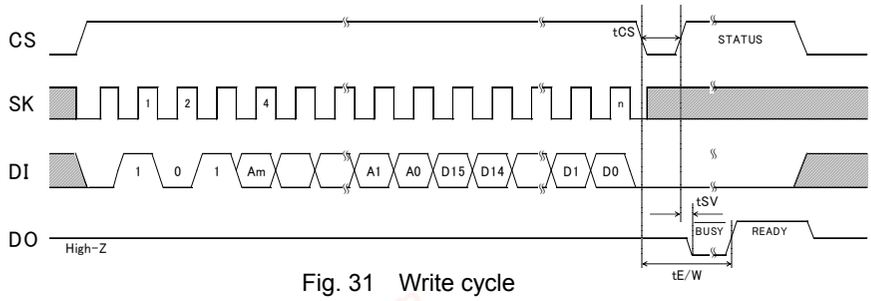
*2 The following address data output (auto increment function)

*1 Start bit
When data "1" is input for the first time after the rise of CS, this is recognized as a start bit. And when "1" is input after plural "0" are input, it is recognized as a start bit, and the following operation is started. This is common to all the commands to described hereafter.

Fig. 30 Read cycle

○When the read command is recognized, input address data (16bit) is output to serial. And at that moment, at taking A0, in sync with the rise of SK, "0" (dummy bit) is output. And, the following data is output in sync with the rise of SK.
This IC has address auto increment function valid only at read command. This is the function where after the above read execution, by continuously inputting SK clock, the above address data is read sequentially. And, during the auto increment, keep CS at "H".

2) Write cycle (WRITE)

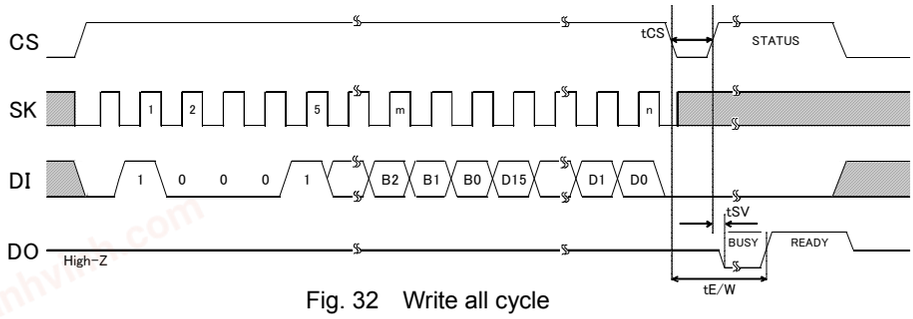


BR93H56/66-WC : n=27, m=7
BR93H76/86-WC : n=29, m=9

Fig. 31 Write cycle

○In this command, input 16bit data (D15~D0) are written to designated addresses (Am~A0). The actual write starts by the fall of CS of D0 taken SK clock(n-th clock from the start bit input), to the rise of the (n+1)-th clock.
When STATUS is not detected, (CS="L" fixed) Max. 10ms in conformity with tE/W, and when STATUS is detected (CS="H"), all commands are not accepted for areas where "L" ($\overline{\text{BUSY}}$) is output from D0, therefore, do not input any command.
Write is not made even if CS is started after input of clock after (n+1)-th clocks.
Note) Take tSKH or more from the rise of the n-th clock to the fall of CS.

3) Write all cycyle (WRAL)



BR93H56/66-WC : n=27, m=9
BR93H76/86-WC : n=29, m=11

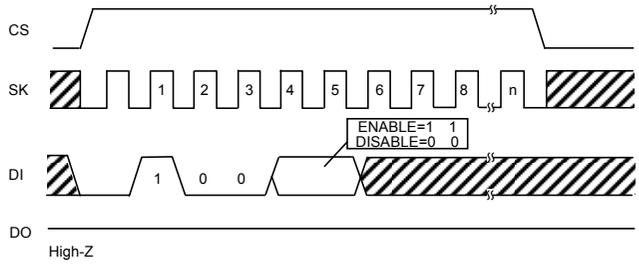
Fig. 32 Write all cycle

○In this command, input 16bit data is written simultaneously to designated block for 128 words. Data is writen in bulk at a write time of only Max. 10ms in conformity with tE/W. When writing data to all addresses, designate each block by B2, B1, and B0, and execute write. Write time is Max.10ms. The actual write starts by the fall of CS from the rise of D0 taken at SK clock (n-th clock from the start bit input), to the rise of the (n+1)-th clock. When CS is ended after clock input after the rise of the (n+1)-th clock, command is cancelled, and write is not completed.
Note)Take tSKH or more from the rise of the n-th clock to the fall of CS.

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4) Write enable (WEN) / disable (WDS) cycle



BR93H56/66-WC : n=11
BR93H76/86-WC : n=13

Fig. 33 Write enable (WEN) / disable (WDS) cycle

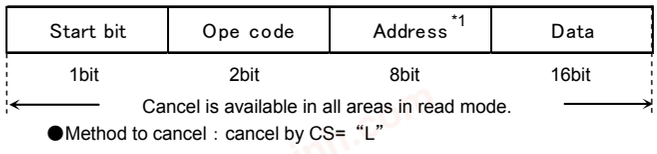
○At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid unitl the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / disable command. Input to SK after 6 clocks of this command is available by either “H” or “L”, but be sure to input it.

○When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is cancelled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by mistake, write is started. To prevent such a mistake, it is recommended to execute the write disable command after completion of write.

●Application

1) Method to cancel each command

○READ

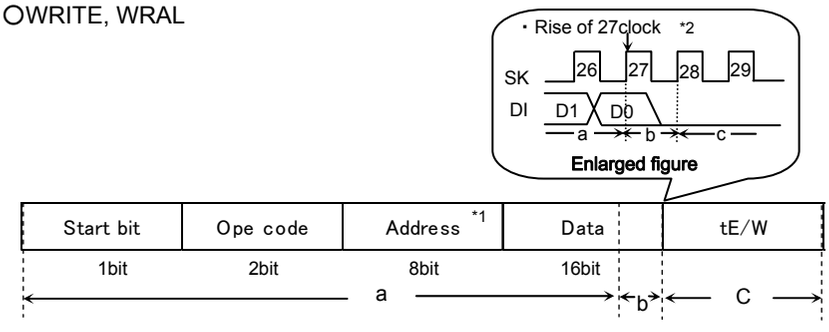


●Method to cancel : cancel by CS= “L”

*1 Address is 8 bits in BR93H56-WC, and BR93H66-WC.
Address is 10 bits in BR93H76-WC, and BR93H86-WC.

Fig.34 READ cancel available timing

○WRITE, WRAL



a : From start bit to 27 clock rise
Cancel by CS=“L”

b : 27 clock rise and after *2
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.

c : 28 clock rise and after *3
Cancel by CS=“L”
However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is input continuously, cancellation is not available.

*1 Address is 8 bits in BR93H56/66-WC
Address is 10 bits in BR93H76/86-WC
*2 27 clocks in BR93H56/66-WC
29 clocks in BR93H76/86-WC
*3 28 clocks in BR93H56/66-WC
30 clocks in BR93H76/86-WC

Note 1) If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.

Note 2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable, therefore, it is recommended to fail in SK=”L” area. As for SK rise, recommend timing of tCSS/tCSH or higher.

Fig.35 WRITE, WRAL cancel available timing

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2) Equivalent circuit

○Output circuit

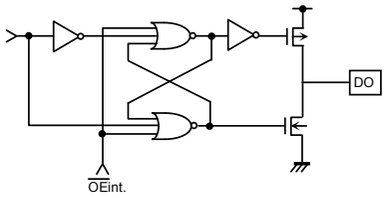


Fig.36 Output circuit (DO)

○Input circuit

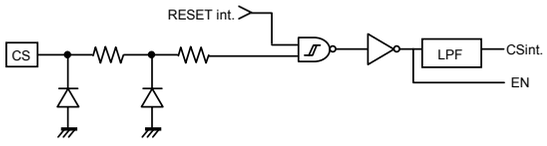


Fig.37 Input circuit (CS)

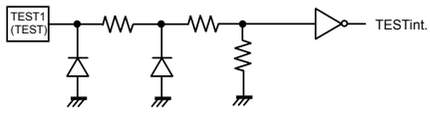


Fig.38 Input circuit (TEST1, TEST)

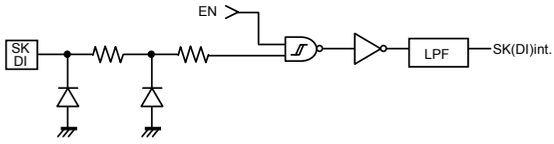


Fig.39 Input circuit (SK, DI)



Fig.40 Input circuit (TEST2)

3) I/O peripheral circuit

3-1) Pull down CS.

By making CS="L" at power ON/OFF, mistake in operation and mistake write are prevented.
Refer to the item 6) Notes at power ON/OFF in page 34/35.

○Pull down resistance Rpd of CS pin

To prevent mistake in operation and mistake write at power ON/OFF, CS pull down resistance is necessary.
Select an appropriate value to this resistance value from microcontroller VOH, IOH, and VIL characteristics of this IC.

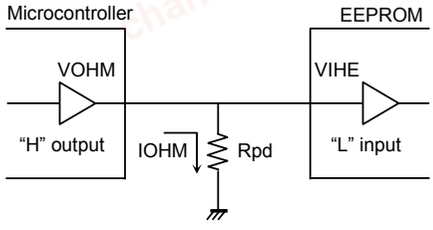


Fig.41 CS pull down resistance

$$Rpd \geqq \frac{VOHM}{IOHM} \quad \cdots ①$$

$$VOHM \geqq VIHE \quad \cdots ②$$

Example) When V_{CC} =5V, VIHE=2V, VOHM=2.4V, IOHM=2mA,
from the equation ①,

$$Rpd \geqq \frac{2.4}{2 \times 10^{-3}}$$

$$\therefore \quad Rpd \geqq 1.2\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, VOHM becomes 2.4V or higher, and VIHE (=2.0V), the equation ② is also satisfied.

- VIHE : EEPROM VIH specifications
- VOHM : Microcontroller VOH specifications
- IOHM :Microcontroller IOH specifications

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3-2) DO is available in both pull up and pull down.
Do output become “High-Z” in other READY / $\overline{\text{BUSY}}$ output timing than after data output at read command and write command. When malfunction occurs at “High-Z” input of the microcontroller port connected to DO, it is necessary to pull down and pull up DO. When there is no influence upon the microcontroller actions, DO may be OPEN. If DO is OPEN, and at timing to output status READY, at timing of CS=“H”, SK=“H”, DI=“H”, EEPROM recognizes thisas a start bit, resets READY output, and DO=”High-Z”, therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

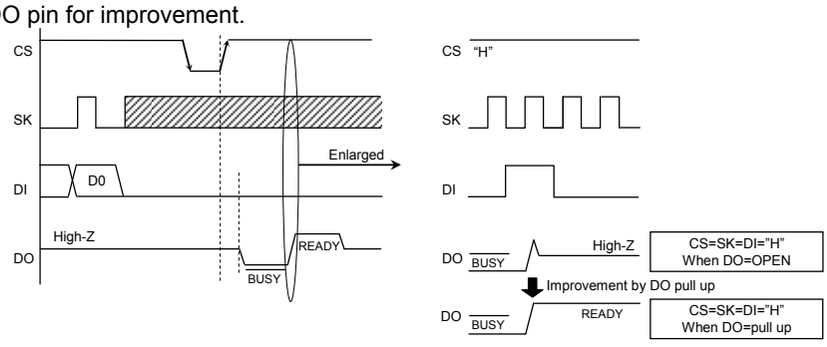
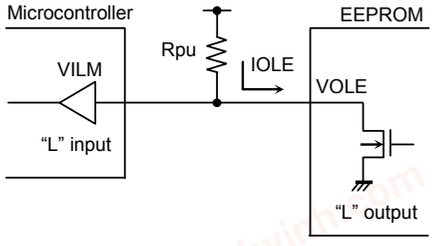


Fig.42 READY output timing at DO=OPEN

○Pull up resistance Rpu and pull down resistance Rpd of DO pin
As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller VIH, VIL, and VOH, IOH, VOL, IOL characteristics of this IC.



・VOLE
・IOLE
・VILM

Fig.43 DO pull up resistance

$$Rpu \geqq \frac{Vcc-VOLE}{IOLE} \quad \cdots ③$$

$$VOLE \leqq VILM \quad \cdots ④$$

Example) When V_{CC} =5V, VOLE=0.4V, IOLE=2.1mA, VILM=0.8V, from the equation ③,

$$Rpu \geqq \frac{5-0.4}{2.1\times10^{-3}}$$

$$\therefore \quad Rpu \geqq 2.2\ [k\Omega]$$

With the value of Rpu to satisfy the above equation, VOLE becomes 0.4V or below, and with VILM(=0.8V), the equation ④ is also satisfied.

・VOLE : EEPROM VOL specifications
・IOLE : EEPROM IOL specifications
・VILM : Microcontroller VIL specifications

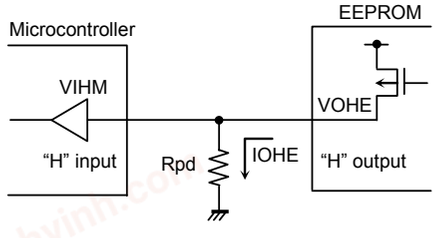


Fig.44 DO pull down resistance

$$Rpd \geqq \frac{VOHE}{IOHE} \quad \cdots ⑤$$

$$VOHE \geqq VIHM \quad \cdots ⑥$$

Example) When V_{CC} =5V, VOHE=Vcc−0.2V, IOHE=0.1mA, VIHM=Vcc×0.7V from the equation ⑤

$$Rpd \geqq \frac{5-0.2}{0.1\times10^{-3}}$$

$$\therefore \quad Rpd \geqq 48\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, VOHE becomes 2.4V or below, and with VIHM (=3.5V), the equation ⑥ is also satisfied.

・VOHE : EEPROM VOH specifications
・IOHE : EEPROM IOH specifications
・VIHM : Microcontroller VIH specifications

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○READY / $\overline{BUSY}$ status display (DO terminal)
(common to BR93H56-WC, BR93H66-WC, BR93H76-WC, BR93H86-WC)
This display outputs the internal status signal. When CS is started after tCS (Min.200ns) from CS fall after write command input, “H” or “L” output.

R/$\overline{B}$ display＝“L” ($\overline{BUSY}$) = write under execution
(DO status) After the timer circuit in the IC works and creates the period of tE/W, this time circuit completes automatically. And write to the memory cell is made in the period of tE/W, and during this period, other command is not accepted.

R/$\overline{B}$ display = “H” (READY) = command wait status
(DO status) Even after tE/W (max.10ms) from write of the memory cell, the following command is accepted. Therefore, CS=“H” in the period of tE/W, and when input is in SK, DI, malfunction may occur, therefore,

DI=“L” in the area
CS=“H”. (Especially, in the case of shared input port, attention is required.)

*Do not input any command while status signal is output. Command input in $\overline{BUSY}$ area is cancelled, but command input in READY area is accepted. Therefore, status READY output is cancelled, and malfunction and mistake write may be made.

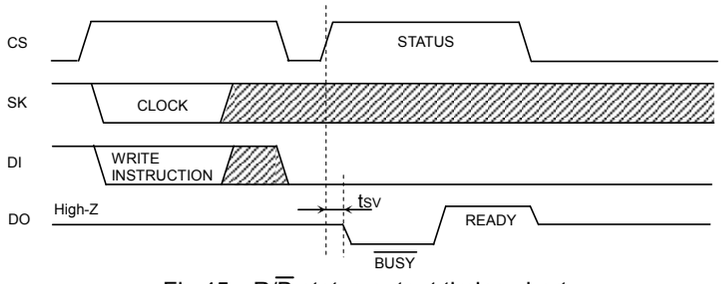


Fig.45 R/$\overline{B}$ status output timing chart

4) When to directly connect DI and DO
This IC has independent input terminal DI and output terminal DO, and separate signals are handled on timing chart, meanwhile, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by 1 control line.

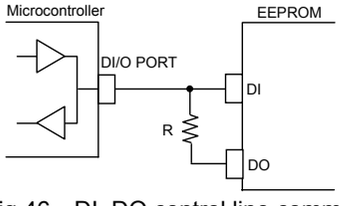


Fig.46 DI, DO control line common connection

○Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input.
Drive from the microcontroller DI/O output to DI input on I/O timing, and signal output from DO output occur at the same time in the following points.
4-1) 1 clock cycle to take in A0 address data at read command
Dummy bit “0” is output to DO terminal.
→When address data A0 = “1” input, through current route occurs.

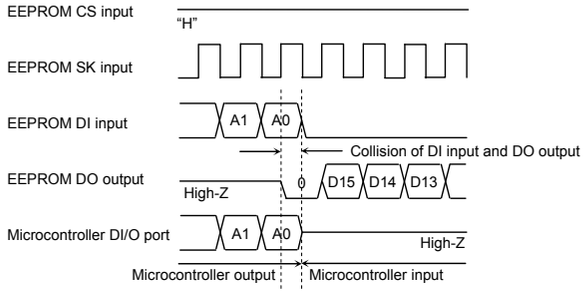


Fig.47 Collision timing at read data output at DI, DO direct connection

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4-2) Timing of CS = “H” after write command. DO terminal in READY / BUSY function output.
When the next start bit input is recognized, “HIGH-Z” gets in.
→Especially, at command input after write, when CS input is started with microcontroller DI/O output “L”, READY output “H” is output from DO terminal, and through current route occurs.

Feedback input at timing of these 4-1) and 4-2) does not cause disorder in basic operations, if resistance R is inserted.

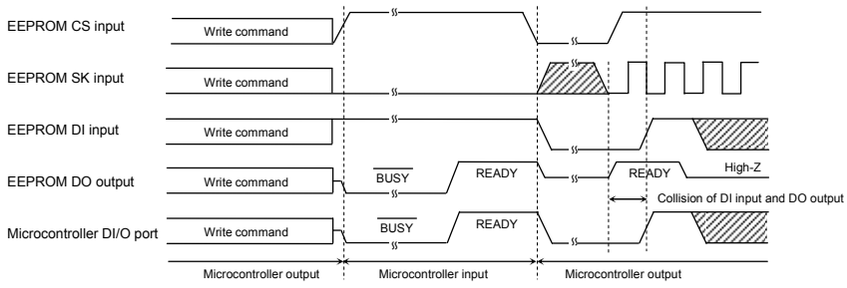
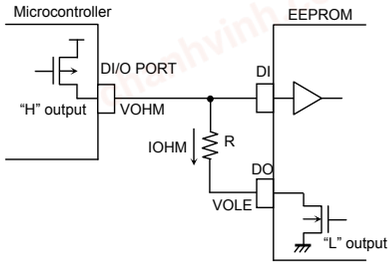


Fig.48 Collision timing at DI, DO direct connection

○Selection of resistance value R

The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level VIH/VIL, even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

4-3) Address data A0 = “1” input, dummy bit “0” output timing
(When microcontroller DI/O output is “H”, EEPROM DO outputs “L”, and “H” is input to DI)
・Make the through current to EEPROM 10mA or below.
・See to it that the input level VIH of EEPROM should satisfy the following.



Conditions

$$VOHM \leqq VIHE$$

$$VOHM \leqq IOHM \times R + VOLE$$

At this moment, if VOLE=0V,

$$VOHM \leqq IOHM \times R$$

$$\therefore \quad R \geqq \frac{VOHM}{IOHM} \quad \cdots ⑦$$

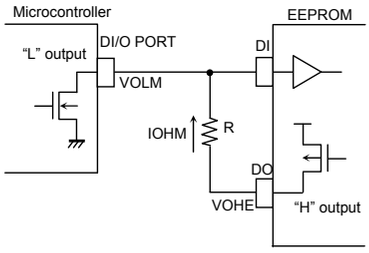
・VIHE : EEPROM VIH specifications
・VOLE : EEPROM VOL specifications
・VOHM : Microcontroller VOH specifications
・IOHM : Microcontroller IOH specifications

Fig.49 Circuit at DI, DO direct connection (Microcontroller DI/O “H” output, EEPROM “L” output)

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4-4) DO status READY output timing
(When the microcontroller DI/O is “L”, EEPROM DO outputs “H”, and “L” is input to DI)
・Set the EEPROM input level VIL so as to satisfy the following.



Conditions

$$VOLM \geqq VILE$$

$$VOLM \geqq VOHE - IOLM \times R$$

As this moment, if VOHE=Vcc,

$$VOLM \geqq Vcc - IOLM \times R$$

$$\therefore \quad R \geqq \frac{Vcc - VOLM}{IOLM} \quad \cdot\cdot\cdot ⑧$$

・VILE : EEPROM VIL specifications
・VOHE : EEPROM VOH specifications
・VOLM : Microcontroller VOL specifications
・IOLM : Microcontroller IOL specifications

Example) When Vcc=5V, VOHM=5V, IOHM=0.4mA, VOLM=5V, IOLM=0.4mA,

From the equation ⑦,

$$R \geqq \frac{VOHM}{IOHM}$$

$$R \geqq \frac{5}{0.4 \times 10^{-3}}$$

$$\therefore \quad R \geqq 12.5\ [k\Omega] \quad \cdot\cdot\cdot ⑨$$

From the equation ⑧,

$$R \geqq \frac{Vcc - VOLM}{IOLM}$$

$$R \geqq \frac{5 - 0.4}{2.1 \times 10^{-3}}$$

$$\therefore \quad R \geqq 2.2\ [k\Omega] \quad \cdot\cdot\cdot ⑩$$

Therefore, from the equations ⑨ and ⑩,

$$\therefore \quad R \geqq 12.5\ [k\Omega]$$

Fig.50 Circuit at DI, DO direct connection (Microcontroller DI/O “L” output, EEPROM “H” output)

5) Notes at test pin wrong input

There is no influence of external input upon TEST2 pin.
For TEST1 (TEST)pin, input must be GND or OPEN. If H level is input, the following may occur,

1. At WEN, WDS, READ command input
   There is no influence by TEST1 (TEST) pin.

2. WRITE, WRAL command input

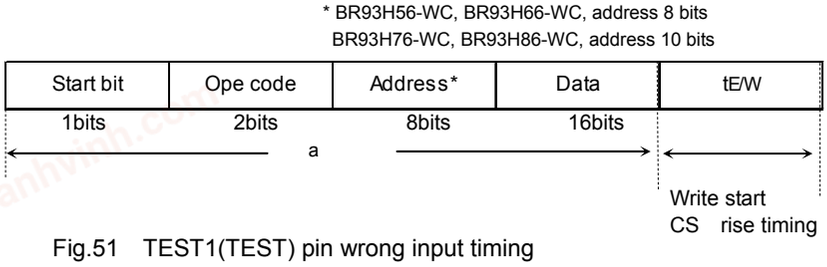


Fig.51 TEST1(TEST) pin wrong input timing

a : There is no influence by TEST1 (TEST) pin.

b : If H during write execution, it may not be written correctly. And H area remains $\overline{BUSY}$ and READY does not go back. Avoid noise input, and at use, be sure to connect it to GND terminal or set it OPEN.

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6) Notes on power ON/OFF

・At power ON/OFF, set CS “L”.

When CS is “H”, this IC gets in input accept status (active). At power ON, set CS “L” to prevent malfunction from noise. (When CS is in “L” status, all inputs are cancelled.) At power decline low power status may prevail. Therefore, at power OFF, set CS “L” to prevent malfunction from noise.

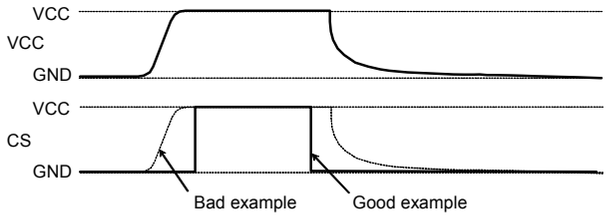


Fig.52 Timing at power ON/OFF

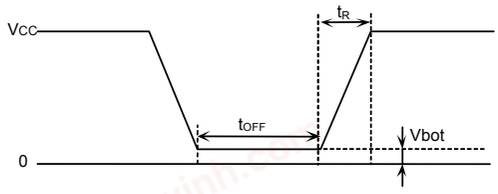
（Bad example）CS pin is pulled up to Vcc.
In this case, CS becomes “H” (active status), EEPROM may malfunction or have write error due to noises. This is true even when CS input is High-Z.

（Good example）It is “L” at power ON/OFF.
Set 10ms or higher to recharge at power OFF.
When power is turned on without observing this condition, IC internal circuit may not be reset.

○POR citcuit

This IC has a POR (Power On Reset) circuit as a mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is “H” at power ON/OFF, it may become write enable status owing to noises and the likes. For secure actions, observe the follwing conditions.

1. Set CS=”L”
2. Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit action.



Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Fig.53 Rise waveform diagram

○LVCC circuit

LVCC (VCC-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ.=1.9V) or below, it prevent data rewrite.

7) Noise countermeasures

○VCC noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC VCC and GND, At that moment, attach it as close to IC as possible.And, it is also recommended to attach a bypass capacitor between board VCC and GND.

○SK noise

When the rise time (tR) of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement.
To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (tR) of SK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

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●Cautions on use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our IC.

(3) Absolute Maximum Ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, IC may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to IC.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(5) Heat design
In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging
When to package IC onto a board, pay sufficient attention to IC direction and displacement. Wrong packaging may destruct IC. And in the case of shortcircuit between IC terminals and terminals and power source, terminal and GND owing to foreign matter, IC may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

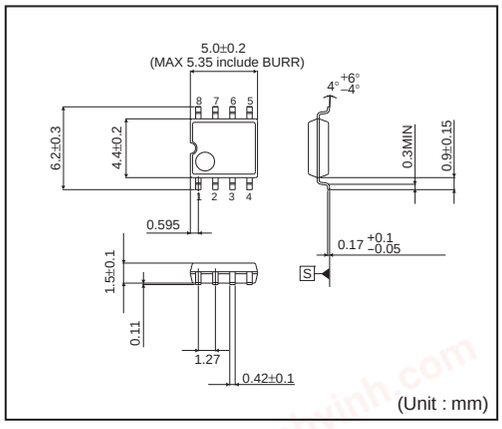
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B	R	9	3	L	4	6	F	J	-	W	E	2

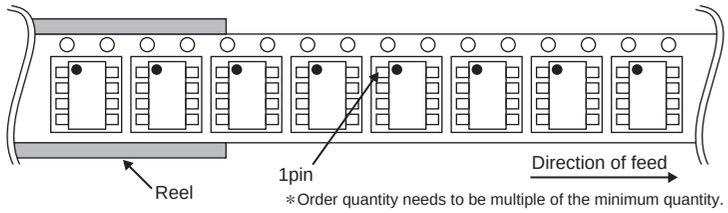
- ROHM Type name
- BUSType: 93 : Microwire
- Operating temperature: L:-40℃~+85℃, A:-40℃~+105℃, H:-40℃~+125℃
- Capacity: 46=1K, 56=2K, 66=4K, 76=8K, 86=16K
- Package type: F,RF :SOP8; FJ,RFJ :SOP-J8; FV,RFV : SSOP-B8; FVT,RFVT : TSSOP-B8; RFVJ : TSSOP-B8J; RFVM : MSOP8
- Double cell: L:W, A:WM, H:WC
- Package specifications: E2 : reel shape emboss taping, TR : reel shape emboss taping

SOP8



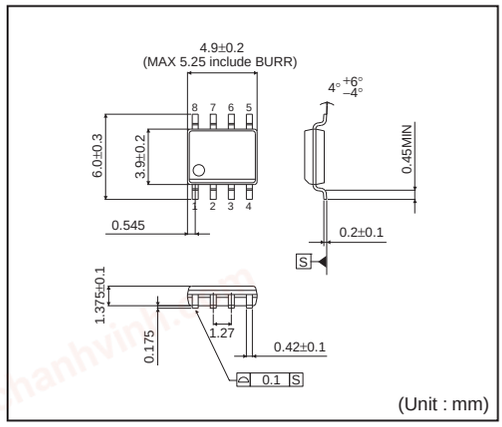
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



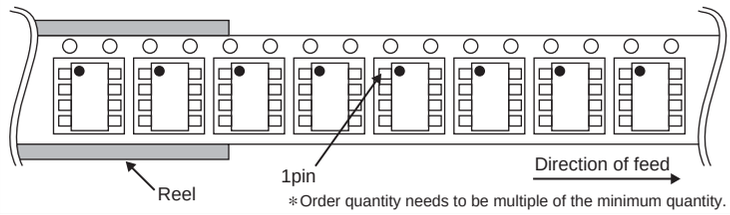
＊Order quantity needs to be multiple of the minimum quantity.

SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

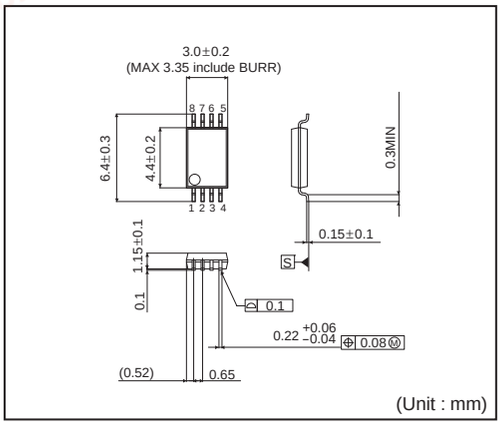


＊Order quantity needs to be multiple of the minimum quantity.

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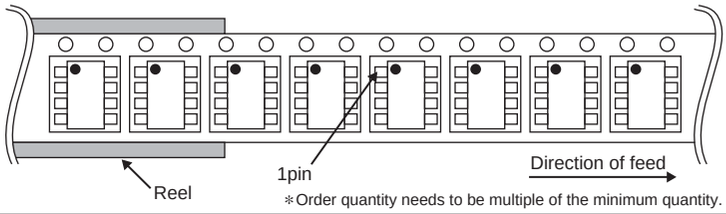
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SSOP-B8



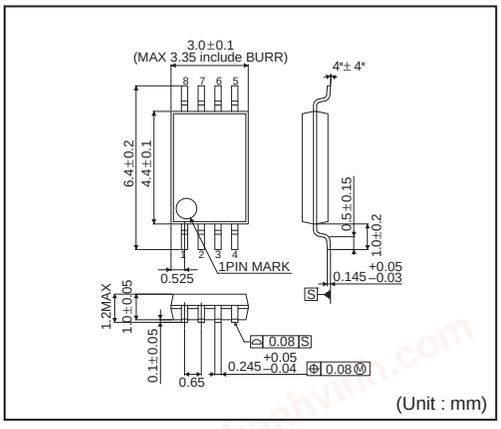
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



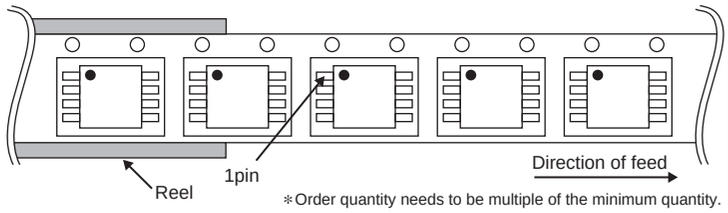
∗Order quantity needs to be multiple of the minimum quantity.

TSSOP-B8



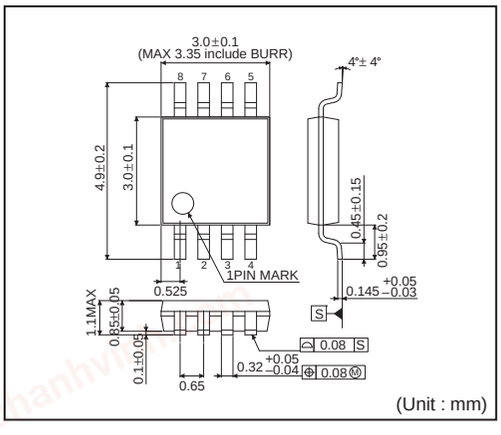
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



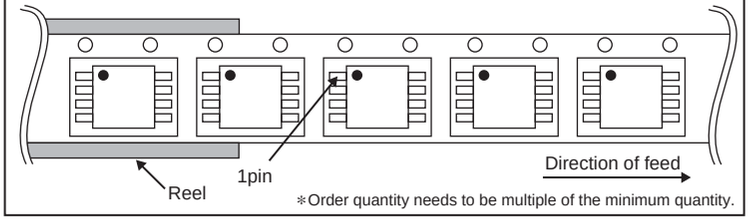
∗Order quantity needs to be multiple of the minimum quantity.

TSSOP-B8J



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

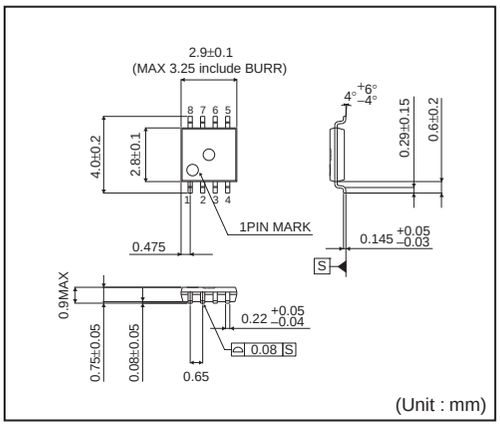


∗Order quantity needs to be multiple of the minimum quantity.

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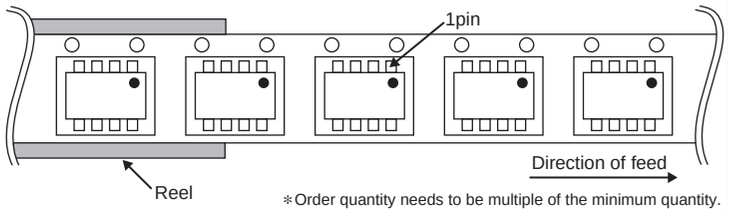
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MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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