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ROHM SEMICONDUCTOR

Technical Note

## High Reliability Serial EEPROMs

# I²C BUS
# BR24□□□□family

### BR24T□□□□Series

No.11001EAT21

Halogen Free ROHM Electronic Components | Pb Free ROHM Electronic Components | RoHS Directive Compliance

### ●Description

BR24T□□□-W series is a serial EEPROM of I²C BUS interface method

### ●Features

1) Completely conforming to the world standard I²C BUS.
   All controls available by 2 ports of serial clock (SCL) and serial data(SDA)
2) Other devices than EEPROM can be connected to the same port, saving microcontroller port
3) 1.7V～5.5V single power source action most suitable for battery use
4) 1.7V～5.5Vwide limit of action voltage, possible FAST MODE 400KHz action
5) Page write mode useful for initial value write at factory shipment
6) Auto erase and auto end function at data write
7) Low current consumption
8) Write mistake prevention function
   Write (write protect) function added
   Write mistake prevention function at low voltage
9) DIP-T8/SOP8/SOP-J8/SSOP-B8/TSSOP-B8/TSSOP-B8J/MSOP8/VSON008X2030 various packages
10) Data rewrite up to 1,000,000 times
11) Data kept for 40 years
12) Noise filter built in SCL / SDA terminal
13) Shipment data all address FFh

### ●BR24T series

| Capacity | Bit format | Type | Power source Voltage | DIP-T8 | SOP8 | SOP-J8 | SSOP-B8 | TSSOP-B8 | TSSOP-B8J | MSOP8 | VSON008 X2030 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1Kbit | 128×8 | BR24T01-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● | ● |
| 2Kbit | 256×8 | BR24T02-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● | ● |
| 4Kbit | 512×8 | BR24T04-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● | ● |
| 8Kbit | 1K×8 | BR24T08-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● | ● |
| 16Kbit | 2K×8 | BR24T16-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● | ● |
| 32Kbit | 4K×8 | BR24T32-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● | ● |
| 64Kbit | 8K×8 | BR24T64-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● | ● |
| 128Kbit | 16K×8 | BR24T128-W | 1.7～5.5V | ● | ● | ● | ● | ● | ● | ● | ● |
| 256Kbit | 32K×8 | BR24T256-W | 1.7～5.5V | ● | ● | ● | ● | ● | | | |
| 512Kbit | 64K×8 | BR24T512-W | 1.7～5.5V | ☆ | ☆ | ☆ | ☆ | ☆ | | | |
| 1024Kbit | 128K×8 | BR24T1M-W | 1.7～5.5V | ☆ | ☆ | ☆ | | | | | |

★:Developing


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## ●Absolute maximum ratings (Ta=25℃)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Impressed voltage | $V_{CC}$ | -0.3～+6.5 | V |
| Permissible dissipation | Pd | 450 (SOP8) *1 | mW |
| | | 450 (SOP-J8) *2 | |
| | | 300 (SSOP-B8) *3 | |
| | | 330 (TSSOP-B8) *4 | |
| | | 310 (TSSOP-B8J) *5 | |
| | | 310 (MSOP8) *6 | |
| | | 300 (VSON008X2030) *7 | |
| | | 800 (DIP-T8) *8 | |
| Storage temperature range | Tstg | −65～+150 | ℃ |
| Action temperature range | Topr | −40～+85 | ℃ |
| Terminal voltage | - | -0.3～Vcc+1.0 *9 | V |
| Junction temperature *10 | Tjmax | 150 | ℃ |

*1,*2 When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
*3,*7 When using at Ta=25℃ or higher 3.0mW to be reduced per 1℃.
*4 When using at Ta=25℃ or higher 3.3mW to be reduced per 1℃.
*5, *6 When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃.
*8 When using at Ta=25℃ or higher 8.1mW to be reduced per 1℃.
*9 The Max value of Terminal Voltage is not over 6.5V.
When the pulse width is 50ns or less, the Min value of
Terminal Voltage is not under -1.0V. (BR24T16/32/64/128/256/512/1M-W)
the Min value of Terminal Voltage is not under -0.8V. (BR24T01/02/04/08-W)
*10 Junction temperature at the storage condition.

## ●Memory cell characteristics (Ta=25℃, Vcc=1.7～5.5V)

| Parameter | Limits | | | Unit |
|---|---|---|---|---|
| | Min. | Typ. | Max | |
| Number of data rewrite times *1 | 1,000,000 | − | − | Times |
| Data hold years *1 | 40 | − | − | Years |

*1Not 100% TESTED

## ●Recommended operating conditions

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power source voltage | Vcc | 1.7～5.5 | V |
| Input voltage | $V_{IN}$ | 0～Vcc | |

## ●Electrical characteristics (Unless otherwise specified, Ta=−40～+85℃, VCC=1.7～5.5V)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| “H” input voltage 1 | $V_{IH1}$ | 0.7Vcc | − | Vcc+1.0 | V | |
| “L” input voltage 1 | $V_{IL1}$ | -0.3 *2 | − | 0.3Vcc | V | |
| “L” output voltage 1 | $V_{OL1}$ | − | − | 0.4 | V | $I_{OL}$=3.0mA, 2.5V≦Vcc≦5.5V (SDA) |
| “L” output voltage 2 | $V_{OL2}$ | − | − | 0.2 | V | $I_{OL}$=0.7mA, 1.7V≦Vcc＜2.5V (SDA) |
| Input leak current | $I_{LI}$ | −1 | − | 1 | μA | $V_{IN}$=0～Vcc |
| Output leak current | $I_{LO}$ | −1 | − | 1 | μA | $V_{OUT}$=0～Vcc (SDA) |
| Current consumption at action | $I_{CC1}$ | − | − | 2.0 | mA | Vcc=5.5V,$f_{SCL}$=400kHz, $t_{WR}$=5ms, Byte write, Page write BR24T01/02/04/08/16/32/64-W |
| | | − | − | 2.5 | | Vcc=5.5V,$f_{SCL}$=400kHz, $t_{WR}$=5ms, Byte write, Page write BR24T128/256-W |
| | | − | − | 4.5 | | Vcc=5.5V,$f_{SCL}$=400kHz, $t_{WR}$=5ms, Byte write, Page write BR24T512/1M-W |
| | $I_{CC2}$ | − | − | 0.5 | mA | Vcc=5.5V,$f_{SCL}$=400kHz Random read, current read, sequential read BR24T01/02/04/08/16/32/64/128/256-W |
| | | − | − | 2.0 | | Vcc=5.5V,$f_{SCL}$=400kHz Random read, current read, sequential read BR24T512/1M-W |
| Standby current | $I_{SB}$ | − | − | 2.0 | μA | Vcc=5.5V, SDA・SCL=Vcc A0,A1,A2=GND,WP=GND BR24T01/02/04/08/16/32/64/128/256-W |
| | | − | − | 3.0 | | Vcc=5.5V, SDA・SCL=Vcc A0, A1, A2=GND, WP=GND BR24T512/1M-W |

○ Radiation resistance design is not made.
*1 BR24T512/1M-W is a target value because it is developing.
*2 When the pulse width is 50ns or less, it is -1.0V. (BR24T16/32/64/128/256/512/1M-W)
When the pulse width is 50ns or less, it is -0.8V. (BR24T01/02/04/08-W)


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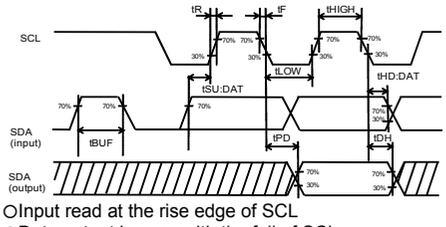
●**Action timing characteristics** (Unless otherwise specified, Ta=−40～+85℃, VCC=1.7～5.5V)

| Parameter | Symbol | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| SCL frequency | fSCL | − | − | 400 | kHz |
| Data clock “HIGH“ time | tHIGH | 0.6 | − | − | μs |
| Data clock “LOW“ time | tLOW | 1.2 | − | − | μs |
| SDA, SCL rise time *1 | tR | − | − | 1.0 | μs |
| SDA, SCL fall time *1 | tF | − | − | 1.0 | μs |
| Start condition hold time | tHD:STA | 0.6 | − | − | μs |
| Start condition setup time | tSU:STA | 0.6 | − | − | μs |
| Input data hold time | tHD:DAT | 0 | − | − | ns |
| Input data setup time | tSU:DAT | 100 | − | − | ns |
| Output data delay time | tPD | 0.1 | − | 0.9 | μs |
| Output data hold time | tDH | 0.1 | − | − | μs |
| Stop condition setup time | tSU:STO | 0.6 | − | − | μs |
| Bus release time before transfer start | tBUF | 1.2 | − | − | μs |
| Internal write cycle time | tWR | − | − | 5 | ms |
| Noise removal valid period (SDA, SCL terminal) | tI | − | − | 0.1 | μs |
| WP hold time | tHD:WP | 1.0 | − | − | μs |
| WP setup time | tSU:WP | 0.1 | − | − | μs |
| WP valid time | tHIGH:WP | 1.0 | − | − | μs |

*1 Not 100% TESTED.

Condition Input data level:VIL=0.2×Vcc VIH=0.8×Vcc
Input data timing refarence level: 0.3×Vcc/0.7×Vcc
Output data timing refarence level: 0.3×Vcc/0.7×Vcc
Rise/Fall time : ≦20ns

●**Sync data input / output timing**




○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Fig.1-(a) Sync data input / output timing

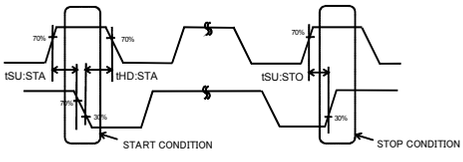



Fig.1-(b) Start-stop bit timing

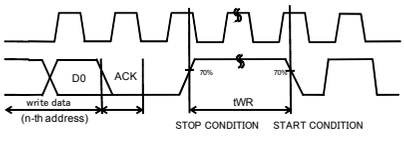



Fig.1-(c) Write cycle timing

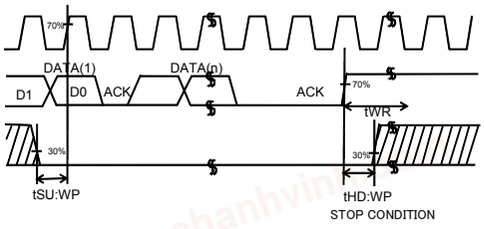



Fig.1-(d) WP timing at write execution

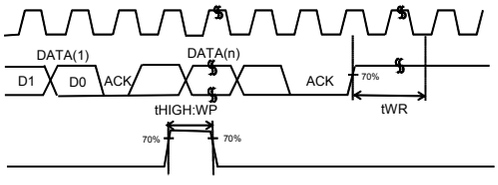


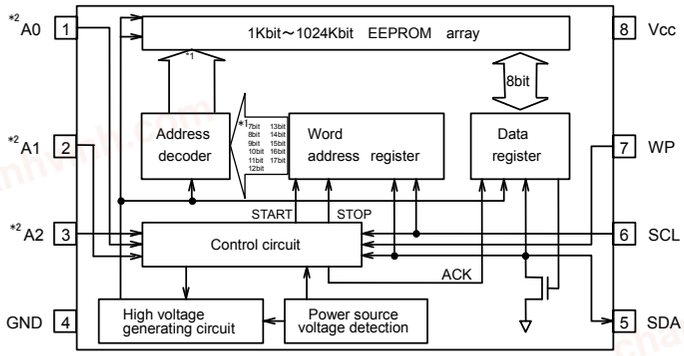

Fig.1-(e) WP timing at write cancel

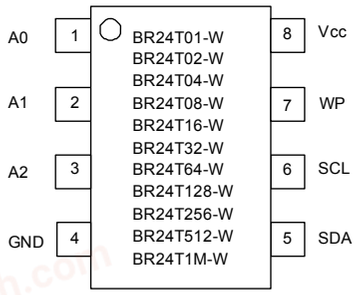

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## ●Block diagram




*1
7bit: BR24T01-W
8bit: BR24T02-W
9bit: BR24T04-W
10bit: BR24T08-W
11bit: BR24T16-W
12bit: BR24T32-W
13bit: BR24T64-W
14bit: BR24T128-W
15bit: BR24T256-W
16bit: BR24T512-W
17bit: BR24T1M-W

*2 A0= Don't use : BR24T04-W, BR24T1M-W
A0, A1=Don't use: BR24T08-W
A0, A1, A2=Don't use: BR24T16-W

Fig.2 Block diagram

## ●Pin assignment and description

| Terminal Name | Input/ Output | BR24T01-W | BR24T02-W | BR24T04-W | BR24T08-W | BR24T16-W | BR24T32/64/ 128/256/512-W | BR24T1M-W |
|---|---|---|---|---|---|---|---|---|
| A0 | Input | Slave address setting | | Don't use* | | | Slave address setting | Don't use* |
| A1 | Input | Slave address setting | | | Don't use* | | Slave address setting | |
| A2 | Input | Slave address setting | | | | Don't use* | Slave address setting | |
| GND | — | Reference voltage of all input / output, 0V | | | | | | |
| SDA | Input/ output | Serial data input serial data output | | | | | | |
| SCL | Input | Serial clock input | | | | | | |
| WP | Input | Write protect terminal | | | | | | |
| Vcc | — | Connect the power source. | | | | | | |

*Pins not used as device address may be set to any of 'H', 'L', and 'Hi-Z'.

## ●Characteristic data (The following values are Typ. ones.)

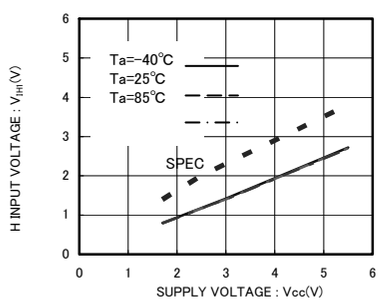



Fig.3 'H' input voltage $V_{IH1}$ (A0,A1,A2,SCL,SDA,WP)

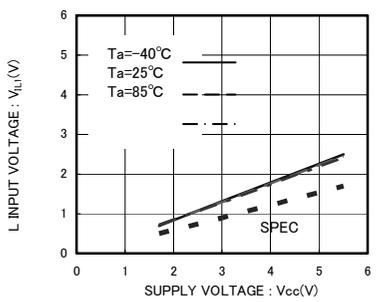



Fig.4 'L' input voltage $V_{IL1}$ (A0,A1,A2,SCL,SDA,WP)

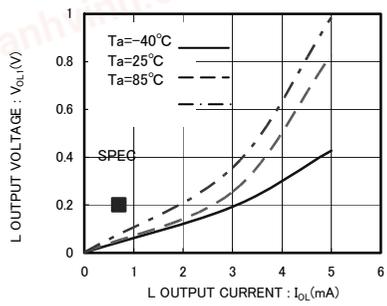



Fig.5 'L' output voltage $V_{OL1}$-$I_{OL}$(Vcc=1.7V)

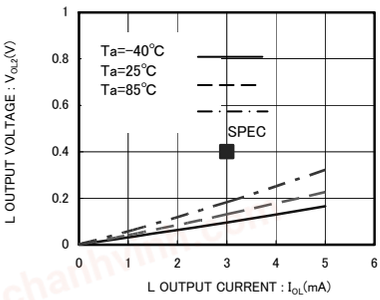



Fig.6 'L' output voltage $V_{OL2}$-$I_{OL}$(Vcc=2.5V)

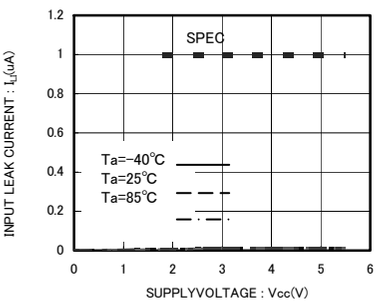



Fig.7 Input leak current $I_{LI}$ (A0,A1,A2,SCL,WP)

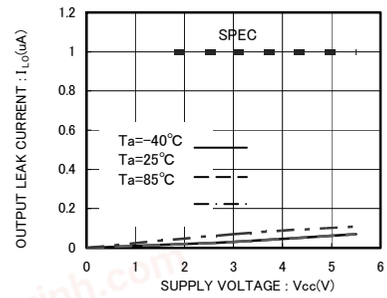



Fig.8 Output leak current $I_{LO}$(SDA)


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## ●Characteristic data (The following values are Typ. ones.)

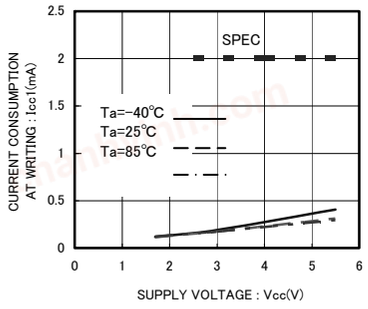



Fig.9 Current consumption at WRITE operation $I_{CC}1$
(fscl=400kHz BR24T01/02/04/08/16/32/64-W)

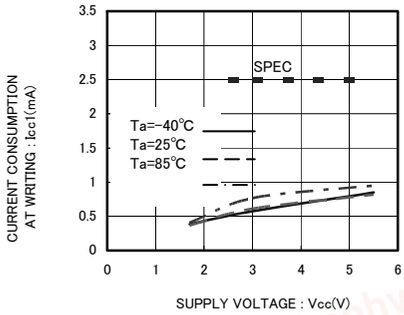



Fig.10 Current consumption at WRITE operation Icc1
(fscl=400kHz BR24T128/256-W)

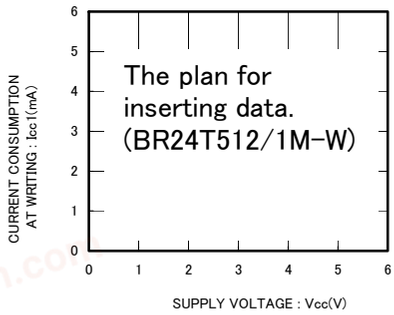



Fig.11 Current consumption at WRITE operation Icc1
(fscl=400kHz BR24T512/1M-W)

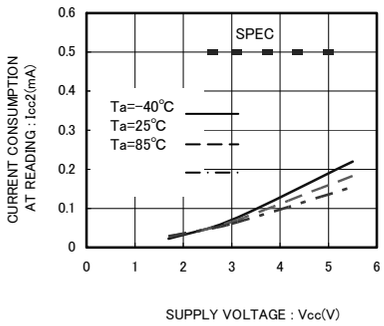



Fig.12 Current consumption at READ operation $I_{CC}2$
(fscl=400kHz BR24T01/02/04/08/16/32/64/128/256-W)

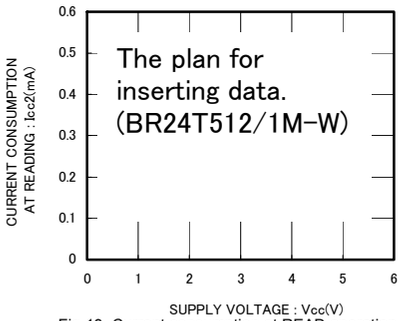



Fig.13 Current consumption at READ operation $I_{CC}2$
(fscl=400kHz BR24T512/1M-W)

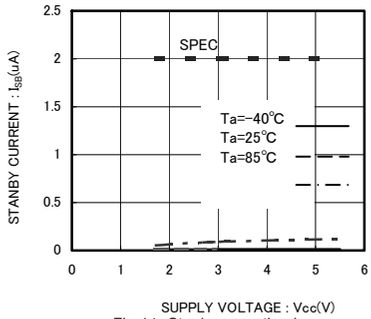



Fig.14 Stanby operation $I_{SB}$
(fscl=400kHz BR24T01/02/04/08/16/32/64/128/256-W)

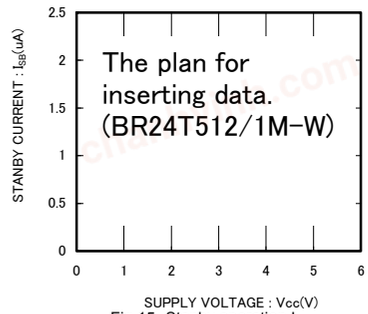



Fig.15 Stanby operation $I_{SB}$
(fscl=400kHz BR24T512/1M-W)

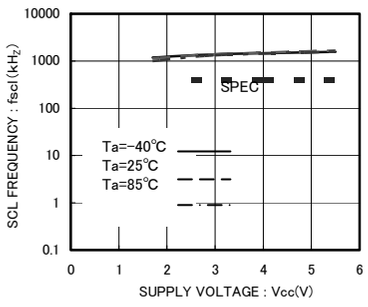



Fig.16 SCL frequency $f_{SCL}$

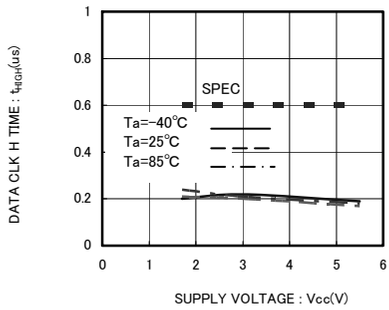



Fig.17 Data clock High Period $t_{HIGH}$

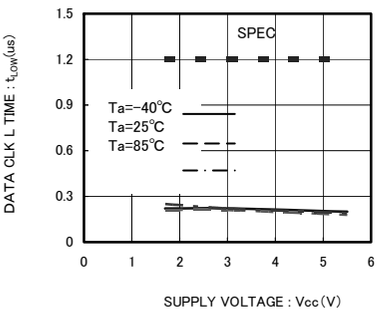



Fig.18 Data clock Low Period $t_{LOW}$

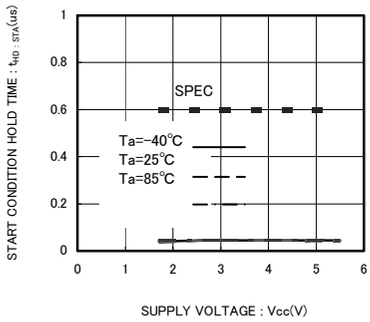



Fig.19 Start Condition Hold Time $t_{HD:STA}$

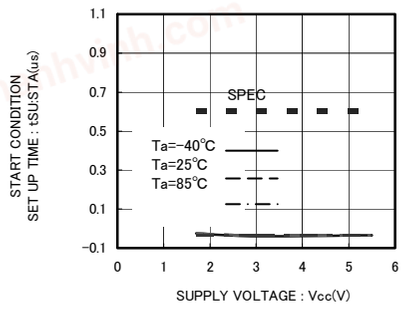



Fig.20 Start Condition Setup Time $t_{SU:STA}$

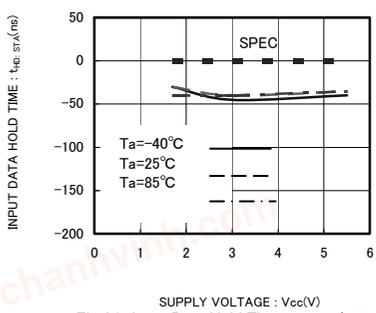



Fig.21 Input Data Hold Time $t_{HD:DAT}$(HIGH)

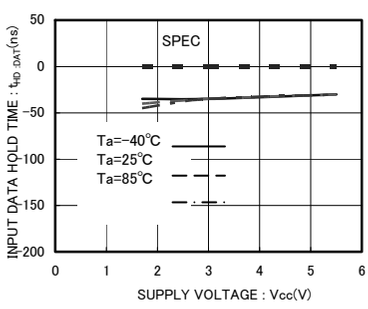



Fig.22 Input Data Hold Time $t_{HD:DAT}$(LOW)

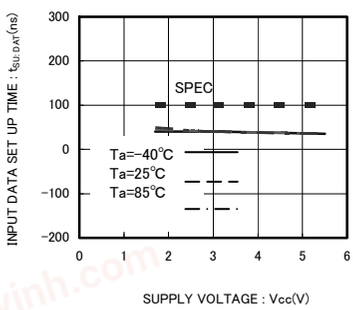



Fig.23 Input Data Setup Time $t_{SU:DAT}$(HIGH)


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## ●Characteristic data (The following values are Typ. ones.)

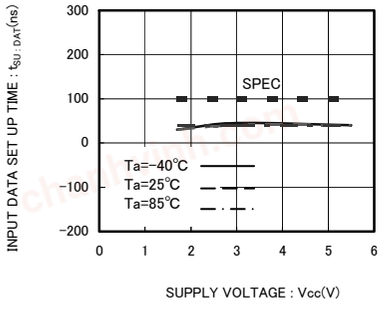



Fig.24 Input Data setup time $t_{SU\ :\ DAT}$(LOW)

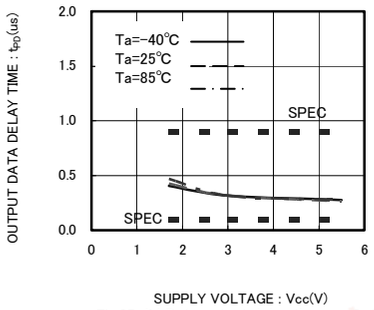



Fig.25 'L' Data output delay time $t_{PD}0$

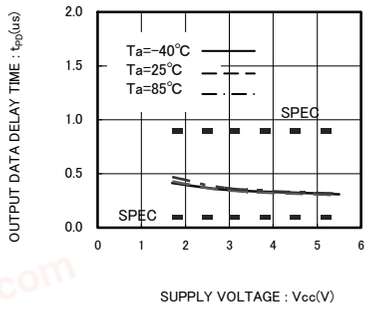



Fig.26 'H' Data output delay time $t_{PD}1$

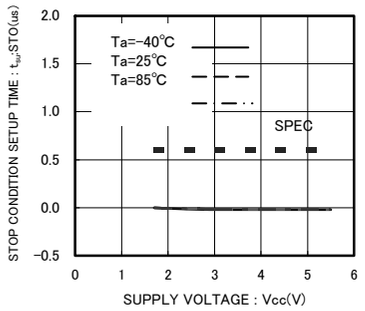



Fig.27 Stop condition setup time
$t_{SU}$:STO

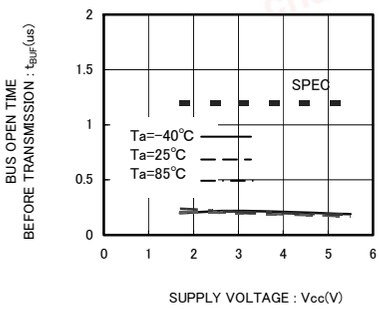



Fig.28 BUS open time before transmission $t_{BUF}$

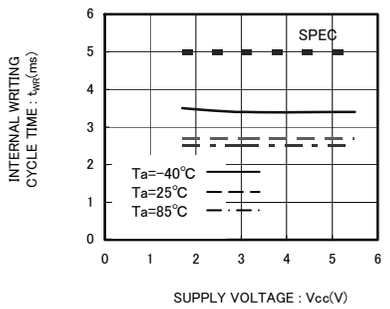



Fig.29 Internal writing cycle time $t_{WR}$

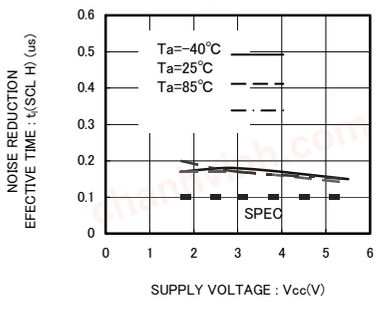



Fig.30 Noise reduction efection time $t_i$(SCL H)

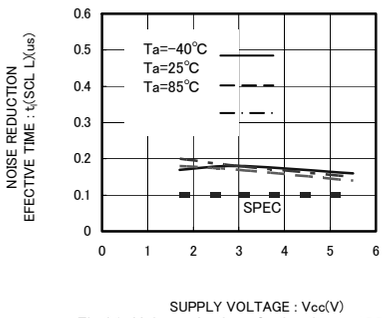



Fig.31 Noise reduction efective time $t_i$(SCL L)

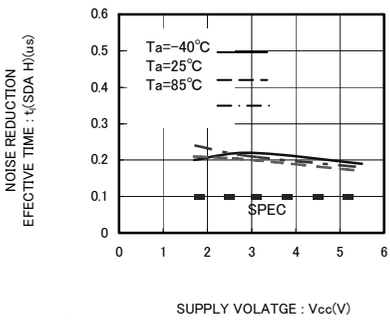



Fig.32 Noise resuction efecctive time $t_i$(SDA H)

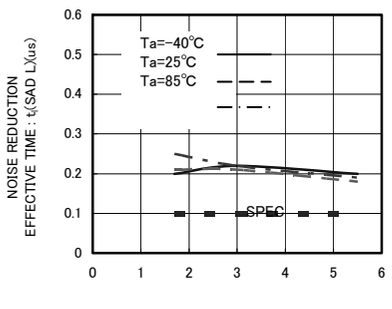



Fig.33 Noise reduction efective time $t_i$(SDA L)

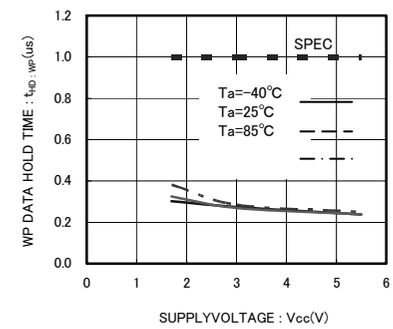



Fig.34 WP data hold time tHD:WP

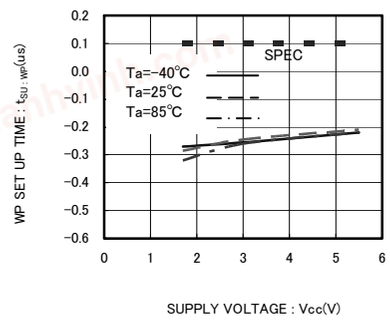



Fig.35 WP setup time $t_{SU\ :\ WP}$

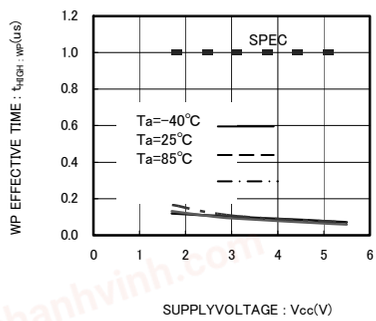



Fig.36 WP efective time $t_{HIGH\ :\ WP}$


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## ●I²C BUS communication

### ○I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).
Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by address peculiar to devices. EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

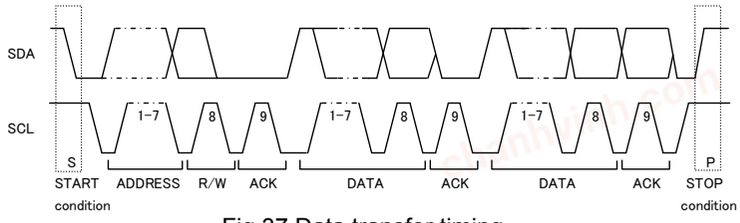



Fig.37 Data transfer timing

### ○Start condition (Start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this confdition is satisfied, any command is executed.

### ○Stop condition (stop bit recongnition)

- Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

### ○Acknowledge (ACK) signal

- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (µ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
- The device (this IC at slave address input of write command, read command, and µ-COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- Each write action outputs acknowledge signal (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
- Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (µ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop cindition (stop bit), and ends read action. And this IC gets in status.

### ○Device addressing

- Output slave address after start condition from master.
- The significant 4 bits of slave address are used for recognizing a device type.
  The device code of this IC is fixed to '1010'.
- Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
- The most insignificant bit (R/W --- READ / $\overline{\text{WRITE}}$ ) of slave address is used for designating write or read action, and is as shown below.

Setting R/$\overline{W}$ to 0 ------- write (setting 0 to word address setting of random read)
Setting R/$\overline{W}$ to 1 ------- read

| Type | Slave address | Maximum number of Connected buses |
|---|---|---|
| BR24T01-W,BR24T02-W | 1 0 1 0 A2 A1 A0 R/$\overline{W}$ | 8 |
| BR24T04-W | 1 0 1 0 A2 A1 P0 R/$\overline{W}$ | 4 |
| BR24T08-W | 1 0 1 0 A2 P1 P0 R/$\overline{W}$ | 2 |
| BR24T16-W | 1 0 1 0 P2 P1 P0 R/$\overline{W}$ | 1 |
| BR24T32-W,BR24T64-W,BR24T128-W, BR24T256-W,BR24T512-W | 1 0 1 0 A2 A1 A0 R/$\overline{W}$ | 8 |
| BR24T1M-W | 1 0 1 0 A2 A1 P0 R/$\overline{W}$ | 4 |

P0～P2 are page select bits.


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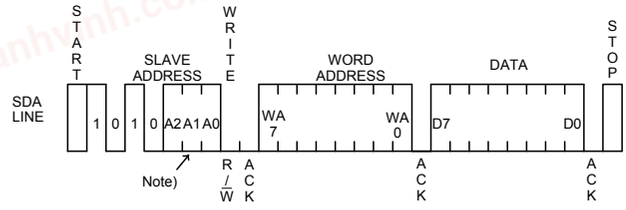
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## ●Write Command

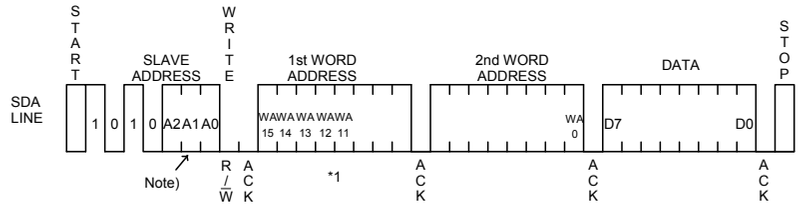
### ○Write cycle

・Arbitrary data is written to EEPROM. When to write only 1 byte, byte write is normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The maximum number of write bytes is specified per device of each capacity. Up to 256 arbitrary bytes can be written.(In the case of BR24T1M-W)



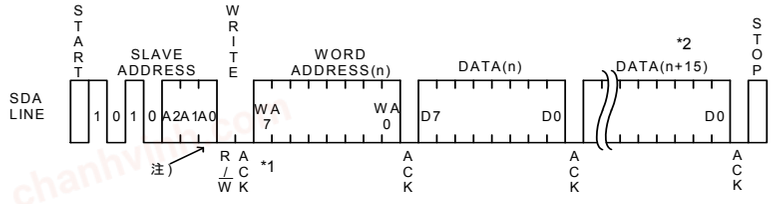

As for WA7, BR24T01-W becomes Don't care.

Fig.38 Byte write cycle (BR24T01/02/04/08/16-W)



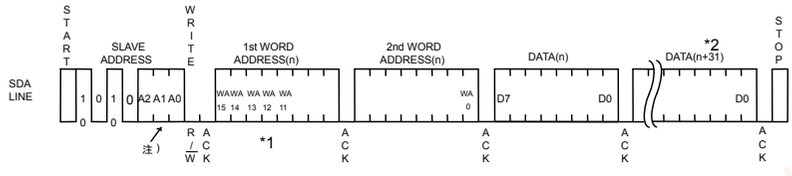

*1 As for WA12, BR24T32-W becomes Don't care.
As for WA13, BR24T32/64-W becomes Don't care.
As for WA14, BR24T32/64/128-W becomes Don't care.
As for WA15, BR24T32/64/128/256-W becomes Don't care.

Fig.39 Byte write cycle (BR24T32/64/128/256/512/1M-W)




*1 As for WA7, BR24T01-W becomes Don't care.
*2 As for BR24T01/02-W becomes (n+7)

Fig.40 Page write cycle (BR24T01/02/04/08/16-W)

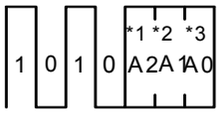



*1 As for WA12, BR24T32-W becomes Don't care.
As for WA13, BR24T32/64-W becomes Don't care.
As for WA14, BR24T32/64/128-W becomes Don't care.
As for WA15, BR24T32/64/128/256-W becomes Don't care.

*2 As for BR24T128/256-W becomes (n+63)
As for BR24T512-W becomes (n+127)
As for BR24T1M-W becomes (n+255)

Fig.41 Page write cycle (BR24T32/64/128/256/512/1M-W)

Note)




*1 In BR24T16-W, A2 becomes P2.
*2 In BR24T08/16-W, A1 becomes P1.
*3 In BR24T04/08/16/1M-W A0 becomes P0.

Fig.42 Difference of slave address of each type


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- During internal write execution, all input commands are ignored, therefore ACK is not sent back.
- Data is written to the address designated by word address (n-th address)
- By issuing stop bit after 8bit data input, write to memory cell inside starts.
- When internal write is started, command is not accepted for tWR (5ms at maximum).

- By page write cycle, the following can be written in bulk : Up to 8Byte (BR24T01-W, BR24T02-W)
  Up to 16Byte (BR24T04-W, BR24T08-W, BR24T16-W)
  Up to 32Byte (BR24T32-W, BR24T64-W)
  Up to 64Byte (BR24T128-W, BR24T256-W)
  Up to 128Byte (BR24T512-W)
  Up to 256Byte (BR24T1M-W)

  And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
  (Refer to "Internal address increment" of "Notes on page write cycle" in P10.)

- As for page write cycle of BR24T01-W and BR24T02-W, after the significant 4 bits (in the case of BR24T01-W) of word address, or the significant 5 bits (in the case of BR24T02-W) of word address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 3 bits is incremented internally, and data up to 8 bytes can be written.

- As for page write command of BR24T04-W, BR24T08-W and BR24T16-W, after page select bit 'P0'(in the case of BR24T04-W), after page select bit 'P0,P1'(in the case of BR24T08-W), after page select bit 'P0,P1,P2'(in the case of BR24T16-W) of slave address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 4 bits is incremented internally, and data up to 16 bytes can be written.

- As for page write cycle of BR24T32-W and BR24T64-W, after the significant 7 bits (in the case of BR24T32-W) of word address, or the significant 8 bits (in the case of BR24T64-W) of word address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 5 bits is incremented internally, and data up to 32 bytes can be written.

- As for page write cycle of BR24T128-W and BR24T256-W, after the significant 8 bits (in the case of BR24T128-W) of word address, or the significant 9 bits (in the case of BR24T256-W) of word address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 6 bits is incremented internally, and data up to 64 bytes can be written.

- As for page write cycle of BR24T512-W after the significant 9 bits of word address is designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 7 bits is incremented internally, and data up to 128 bytes can be written.

- As for page write cycle of BR24T1M-W after page select bit 'P0' and the significant 8 bit of word address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 8 bits is incremented internally, and data up to 256 bytes can be written.


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○Notes on page write cycle

List of numbers of page write

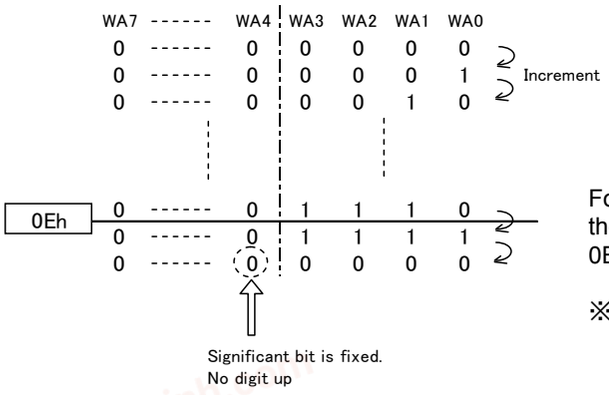
| Number of Pages | 8Byte | 16Byte | 32Byte | 64Byte | 128Byte | 256Byte |
|---|---|---|---|---|---|---|
| Product number | BR24T01-W<br>BR24T02-W | BR24T04-W<br>BR24T08-W<br>BR24T16-W | BR24T32-W<br>BR24T64-W | BR24T128-W<br>BR24T256-W | BR24T512-W | BR24T1M-W |

The above numbers are maximum bytes for respective types.
Any bytes below these can be written.

In the case BR24T256-W, 1 page=64bytes, but the page write cycle time is 5ms at maximum for 64byte bulk write.
It does not stand 5ms at maximum × 64byte=320ms(Max.)

○Internal address increment

Page write mode (in the case of BR24T16-W)




For example, when it is started from address 0Eh, therefore, increment is made as below,
0Eh→0Fh→00h→01h･･･ which please note.

※0Eh･･･0E in hexadecimal, therefore,
00001110 becomes a binary number.

○Write protect (WP) terminal

・Write protect (WP) function

When WP terminal is set Vcc (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.
In the case of use it as an ROM, it is recommended to connect it to pull up or Vcc.
At extremely low voltage at power ON / OFF, by setting the WP terminal 'H', mistake write can be prevented.


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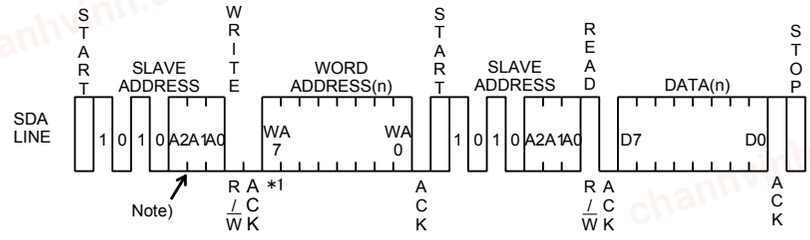
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## ●Read Command

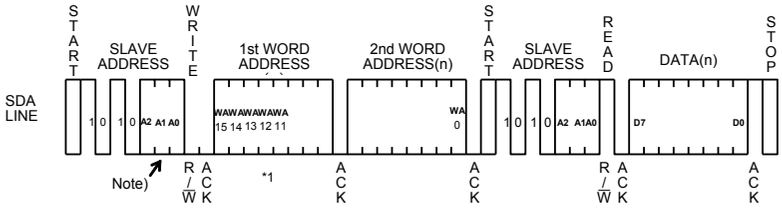
### ○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle. Random read cycle is a command to read data by designating address, and is used generally. Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.



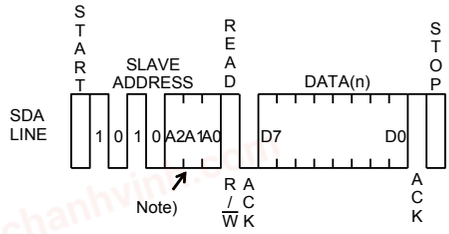

*1 As for WA7,BR24T01-W become Don't care.

Fig.43 Random read cycle (BR24T01/02/04/08/16-W)



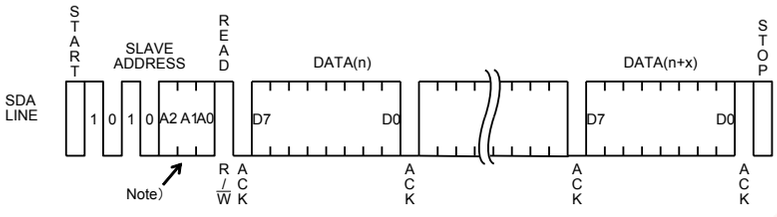

*1 As for WA12, BR24T32-W become Don't care.
As for WA13, BR24T32/64-W become Don't care.
As for WA14, BR24T32/64/128-W become Don't care.
As for WA15, BR24T32/64/128/256-W become Don't care.

Fig.44 Random read cycle (BR24T32/64/128/256/512/1M-W)




*1 As for WA7, BR24T01-W becomes Don't care.
*2 As for BR24T01/02-W becomes (n+7)

Fig.45 Current read cycle



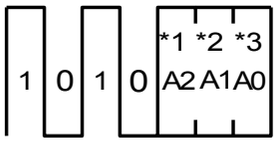

*1 As for WA12, BR24T32-W becomes Don't care.
As for WA13, BR24T32/64-W becomes Don't care.
As for WA14, BR24T32/64/128-W becomes Don't care.
As for WA15, BR24T32/64/128/256-W becomes Don't care.

*2 As for BR24T128/256-W becomes (n+63)
As for BR24T512-W becomes (n+127)
As for BR24T1M-W becomes (n+255)

Fig.46 Sequential read cycle (in the case of current read cycle)

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ-COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H' .
- When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
  Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

Note)




*1 In BR24T16-W, A2 becomes P2.
*2 In BR24T08/16-W, A1 becomes P1.
*3 In BR24T08/16/1M-W, A0 becomes P0.

Fig.47 Difference of slave address of each type


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## ●Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Fig.48-(a), Fig.48-(b), Fig.48-(c).) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

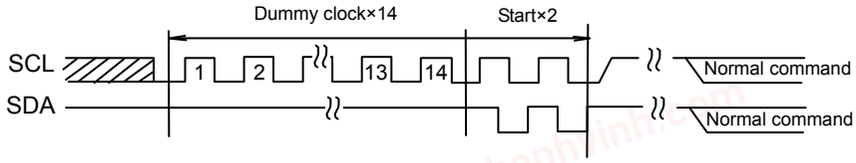



Fig.48-(a) The case of dummy clock +START+START+ command input

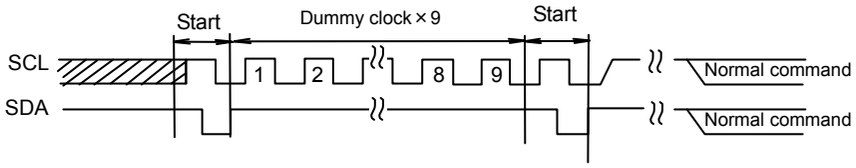



Fig.48-(b) The case of START +9 dummy clocks +START+ command input

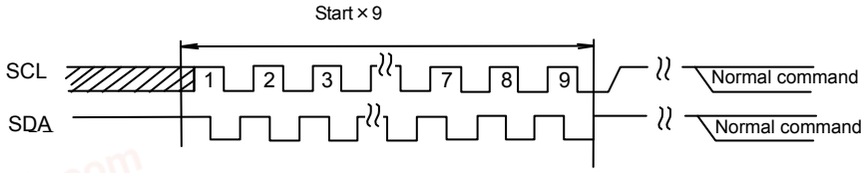



Fig.48-(c) START×9+ command input

※Start command from START input.

## ●Acknowledge polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.

When to write continuously, $R/\overline{W}$ = 0, when to carry out current read cycle after write, slave address $R/\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

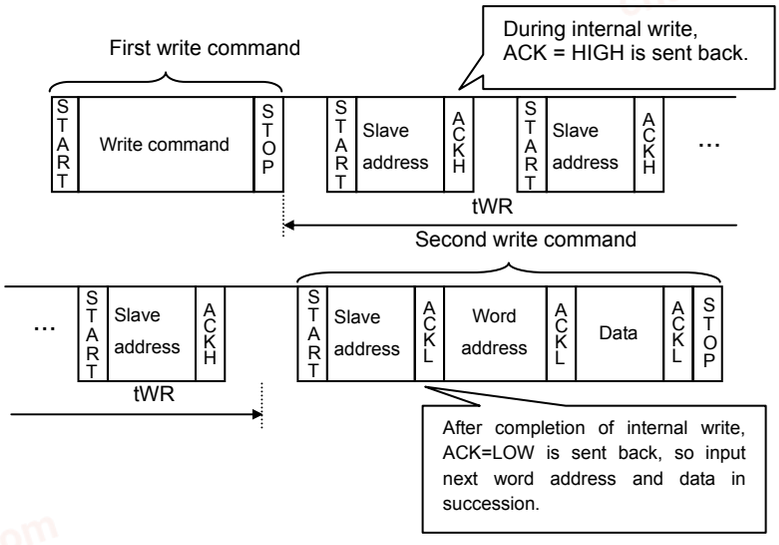



Fig.49 Case to continuously write by acknowledge polling


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**●WP valid timing (write cancel)**

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area.

WP input in this area becomes Don't care. The area from the rise of SCL to take in D0 to input the stop condition is cancel valid area. And, after execution of forced end by WP, standby status gets in.

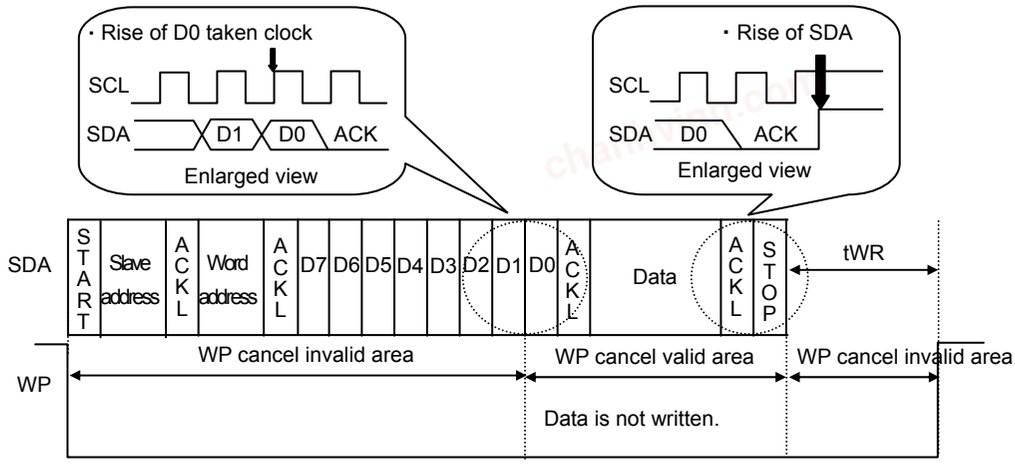



Fig.50 WP valid timing

**●Command cancel by start condition and stop condition**

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Fig.51) However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

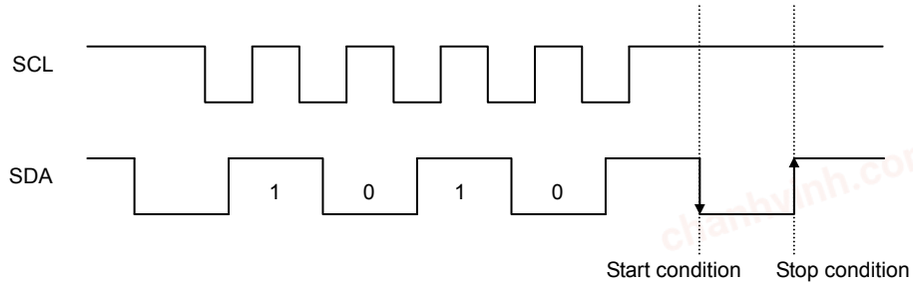



Fig.51 Case of cancel by start, stop condition during slave address input


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## ●I/O peripheral circuit

### ○Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value ($R_{PU}$), select an appropriate value to this resistance value from microcontroller $V_{IL}$, $I_L$, and $V_{OL}$-$I_{OL}$ characteristics of this IC. If $R_{PU}$ is large, action frequency is limited. The smaller the $R_{PU}$, the larger the consumption current at action.

### ○Maximum value of $R_{PU}$

The maximum value of $R_{PU}$ is determined by the following factors.

①SDA rise time to be determined by the capacitance (CBUS) of bus line of $R_{PU}$ and SDA should be tR or below.
And AC timing should be satisfied even when SDA rise time is late.

②The bus electric potential Ⓐ to be determined by input leak total ($I_L$) of device connected to bus at output of 'H' to SDA bus and $R_{PU}$ should sufficiently secure the input 'H' level ($V_{IH}$) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$V_{CC} - I_L R_{PU} - 0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leq \frac{0.8V_{CC} - V_{IH}}{I_L}$$

Ex.) VCC =3V IL=10μA VIH=0.7 VCC
from②

$$R_{PU} \leq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leq 300\ [k\Omega]$$

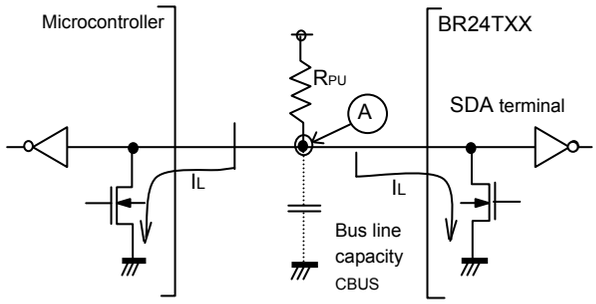



Fig.52 I/O circuit diagram

### ○ Minimum value of $R_{PU}$

The minimum value of $R_{PU}$ is determined by the following factors.
When IC outputs LOW, it should be satisfied that $V_{OLMAX}$=0.4V and $I_{OLMAX}$=3mA.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leq I_{OL}$$

$$\therefore \quad R_{PU} \geq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

②$V_{OLMAX}$= should secure the input 'L' level ($V_{IL}$) of microcontroller and EEPROM including recommended noise margin 0.1Vcc.

$V_{OLMAX} \leqq V_{IL} - 0.1\,V_{CC}$

Ex.) $V_{CC}$ =3V, $V_{OL}$=0.4V, $I_{OL}$=3mA, microcontroller, EEPROM $V_{IL}$=0.3Vcc

from① $R_{PU} \geq \frac{3 - 0.4}{3 \times 10^{-3}}$

$$\geq 867[\Omega]$$

And $V_{OL}$=0.4 [V]

$V_{IL}$=0.3×3
=0.9 [V]

Therefore, the condition ② is satisfied.

### ○Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ ~ several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.


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## ●Cautions on microcontroller connection

### ○Rs

In $I^2C$ BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used.

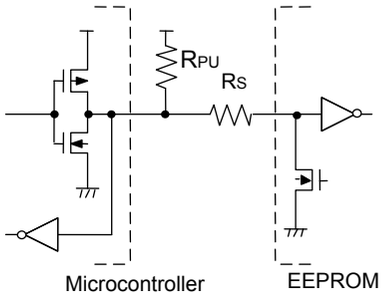



Fig.53 I/O circuit diagram

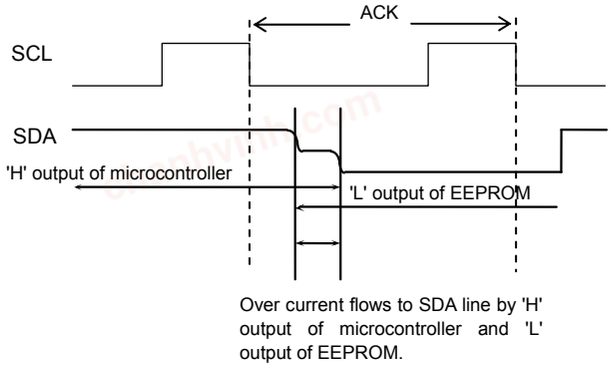



Fig.54 Input / output collision timing

### ○Maximum value of Rs

The maximum value of Rs is determined by the following relations.

①SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

②The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus sufficiently secure the input 'L' level ($V_{IL}$) of microcontroller including recommended noise margin 0.1Vcc.

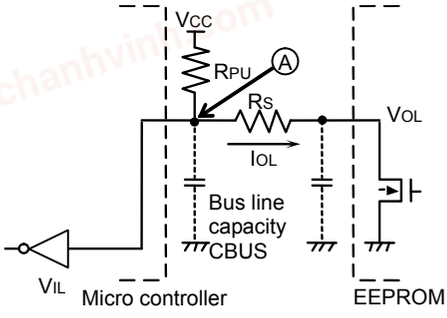



Fig.55 I/O Circuit Diagram

$$\frac{(V_{CC}-V_{OL})}{R_{PU}+R_S}+V_{OL}+0.1V_{CC}\le V_{IL}$$

$$\therefore\quad R_S\le\frac{(V_{CC}-V_{OL})}{1.1V_{CC}-V_{IL}}\times R_{PU}$$

Ex)$V_{CC}$=3V $V_{IL}$=0.3$V_{CC}$ $V_{OL}$=0.4V $R_{PU}$=20kΩ

$$R_S\le\frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3}\times20\times10^3$$

$$\le1.67[k\Omega]$$

### ○Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

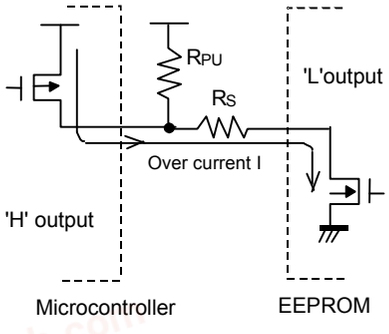



Fig.56 I/O circuit diagram

$$\frac{V_{CC}}{R_S}\le I$$

$$\therefore\quad R_S\ge\frac{V_{CC}}{I}$$

EX) $V_{CC}$=3V I=1mA

$$R_S\ge\frac{3}{10\times10^{-3}}$$

$$\ge300\ [\Omega]$$


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●**I²C BUS input / output circuit**

○Input (A0, A1, A2, SCL, WP)

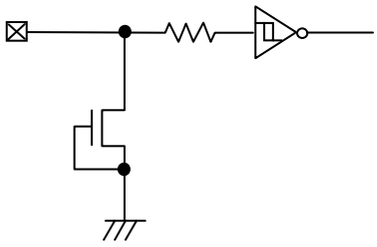


Fig.57 Input pin circuit diagram

○Input / output (SDA)

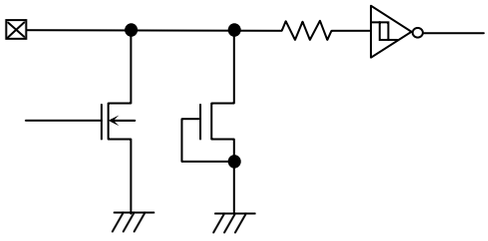


Fig.58 Input / output pin circuit diagram

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## ●Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of $t_R$, $t_{OFF}$, and Vbot for operating POR circuit.

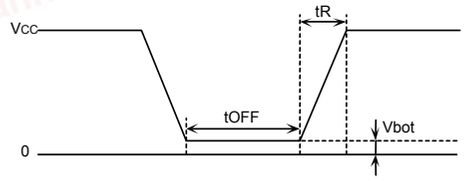



Fig.59 Rise waveform diagram

Recommended conditions of tR, tOFF,Vbot

| tR | tOFF | Vbot |
|---|---|---|
| 10ms or below | 10ms or larger | 0.3V or below |
| 100msor below | 10msor larger | 0.2V or below |

3. Set SDA and SCL so as not to become 'Hi-Z'.
When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

a) In the case when the above condition 1 cannot be observed. When SDA becomes 'L' at power on .
→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

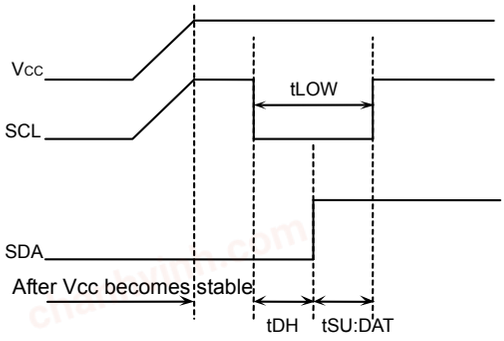



Fig.60 When SCL= 'H' and SDA= 'L'

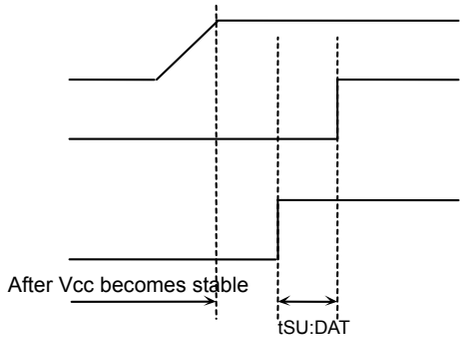



Fig.61 When SCL='L' and SDA='L'

b) In the case when the above condition 2 cannot be observed.
→After power source becomes stable, execute software reset(P12).
c) In the case when the above conditions 1 and 2 cannot be observed.
→Carry out a), and then carry out b).

## ●Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

## ●Vcc noise countermeasures

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board Vcc and GND.


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## ●Notes for use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Terminal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.


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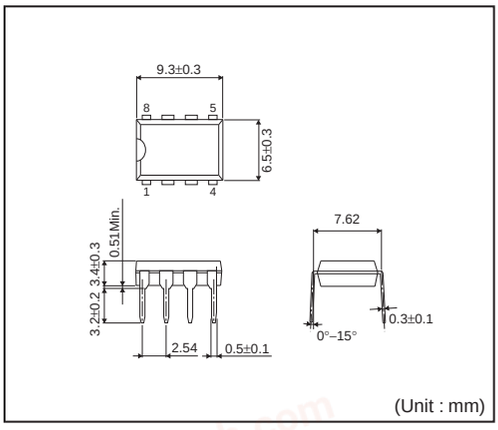
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## ●Order part number

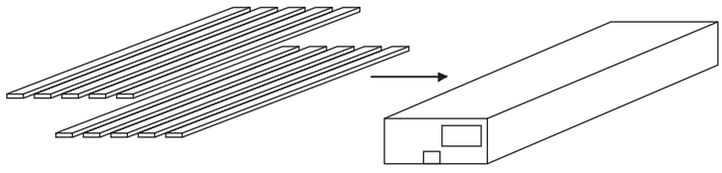
| B R | 2 4 | T | 1 2 8 | F V T | - | W | G | E 2 |
|---|---|---|---|---|---|---|---|---|
| Part No. | BUS type<br>24 : $I^2C$ | Operating temperature/ Power source Voltage<br>-40℃~+85℃<br>1.7V~5.5V | Capacity<br>01=1K 64=64K<br>02=2K 128=128K<br>04=4K 256=256K<br>08=8K 512=512K<br>16=16K 1M=1024K<br>32=32K | Package<br>Blank :DIP-T8<br>F :SOP8<br>FJ :SOP-J8<br>FV : SSOP-B8<br>FVT : TSSOP-B8<br>FVJ : TSSOP-B8J<br>FVM : MSOP8<br>NUX :VSON008X2030 | | Double Cell | Halogen Free | Packaging and forming specification<br>E2: Embossed tape and reel (SOP8, SOP8-J8, SSOP-B8, TSSOP-B8, TSSOP-B8J)<br>TR: Embossed tape and reel (MSOP8, VSON008X2030)<br>None: Tube (DIP-T8) |

### DIP-T8



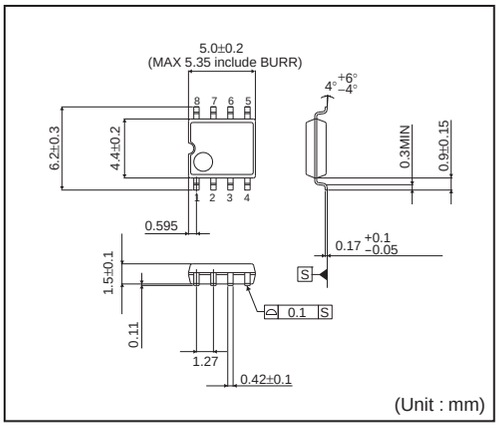

<Tape and Reel information>

| | |
|---|---|
| Container | Tube |
| Quantity | 2000pcs |
| Direction of feed | Direction of products is fixed in a container tube |



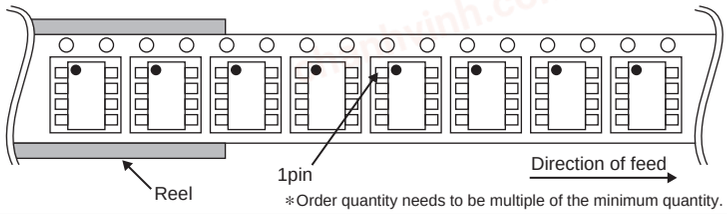
∗Order quantity needs to be multiple of the minimum quantity.

### SOP8



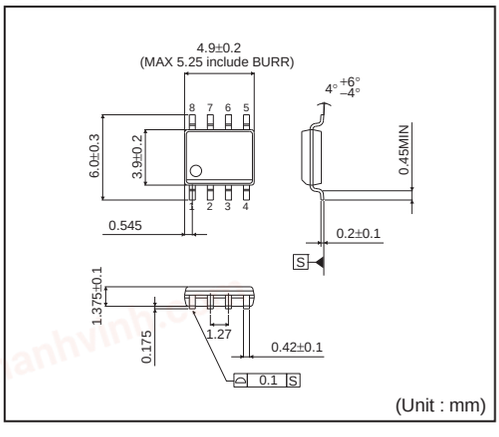

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



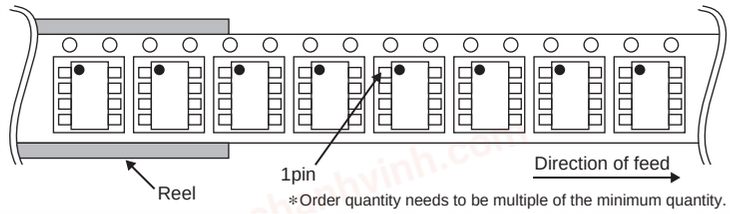

∗Order quantity needs to be multiple of the minimum quantity.

### SOP-J8




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



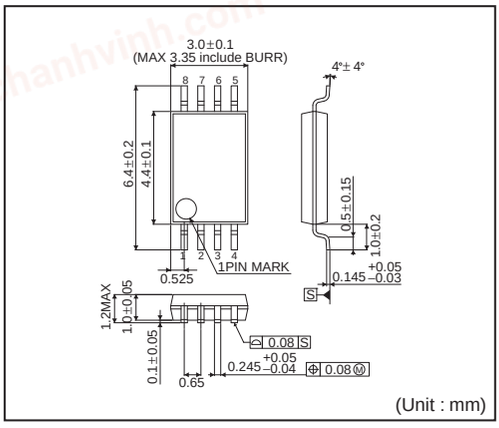

∗Order quantity needs to be multiple of the minimum quantity.


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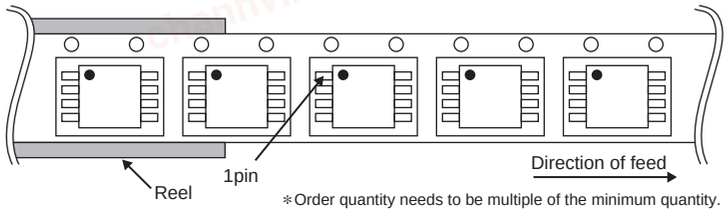


## TSSOP-B8



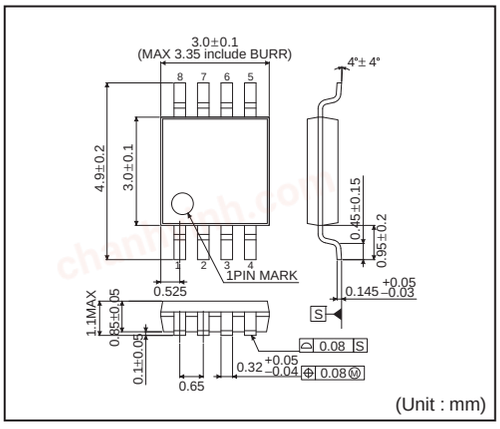

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



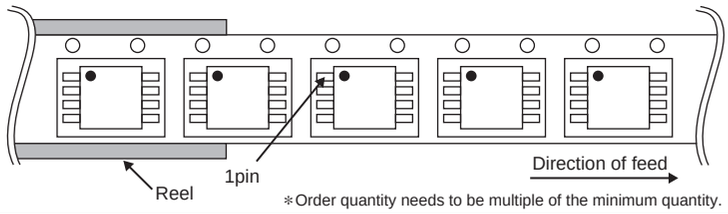

∗Order quantity needs to be multiple of the minimum quantity.

## TSSOP-B8J



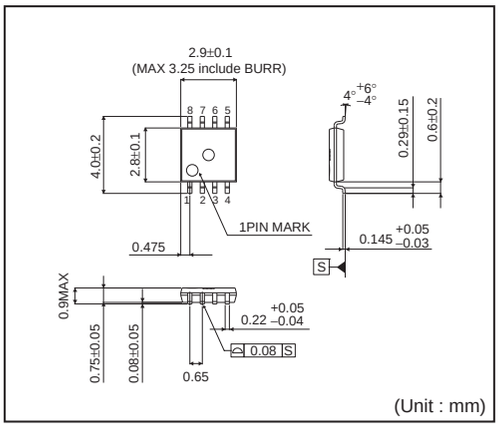

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



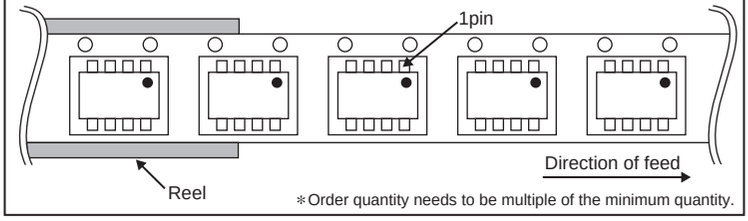

∗Order quantity needs to be multiple of the minimum quantity.

## MSOP8




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |



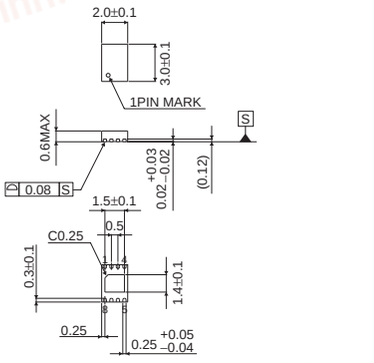

∗Order quantity needs to be multiple of the minimum quantity.


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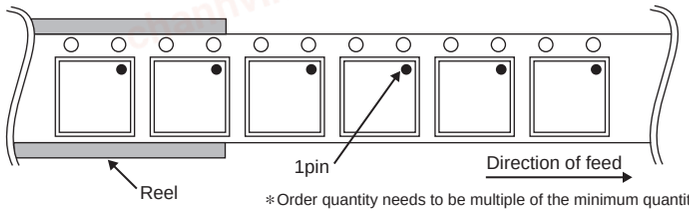
**VSON008X2030**




(Unit : mm)

<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 4000pcs |
| Direction of feed | TR<br>( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.


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