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ROHM SEMICONDUCTOR

Datasheet

AC/DC Converter IC

PWM Controller IC for AC/DC Converter

BM1P10CFJ

General Description

The PWM Controller for AC/DC power supplies provides an optimal system for all products that include an electrical outlet. It realizes the high flexibility in power supply design with external switching MOSFET and current detection resistor. This IC can make efficiency high because it has functions such as AC low voltage protection and X capacitor discharge and operates frequency reduction and burst operation at light load. In addition, this IC also has a built-in power save function and it reduces electric power at no load.
This IC has following various protection functions.

Features

- AC Low Voltage Protection Function (AC UVLO)
- X Capacitor Discharge Function
- VCC Pin Low Voltage Protection (VCC UVLO)
- PWM Type Current Mode Control
- Frequency Reduction Function
- Burst Operation at Light Load
- Switching Function of Operation Modes
- Power Save Function
  (Low Consumption Current at no load)
- Soft Start Function
- FB Pin Overload Protection Function (FB OLP)
- CS Pin Overload Protection Function (CS OLP)
- Switching Function of CS OLP Detection Voltage
- CS Pin Over Current Protection Function (CS OCP)
- CS Pin Leading Edge Blanking Function
- LA/ZT Pin Over Voltage Protection Function
  (ZT OVP)
- OUT Pin Gate Clamp Circuit

Key Specifications

- Operating Power Supply Voltage Range
  VCC Pin Voltage: 9.3 V to 55.0 V
  VH Pin Voltage: 650 V (Max)
- Current at Switching Operation 0.70 mA (Typ)
- Current at Burst Operation 0.35 mA (Typ)
- Current at Power Save Operation 0.11 mA (Typ)
- Switching Frequency 100 kHz (Typ)
- Operation Temperature Range -40 °C to +105 °C

Package

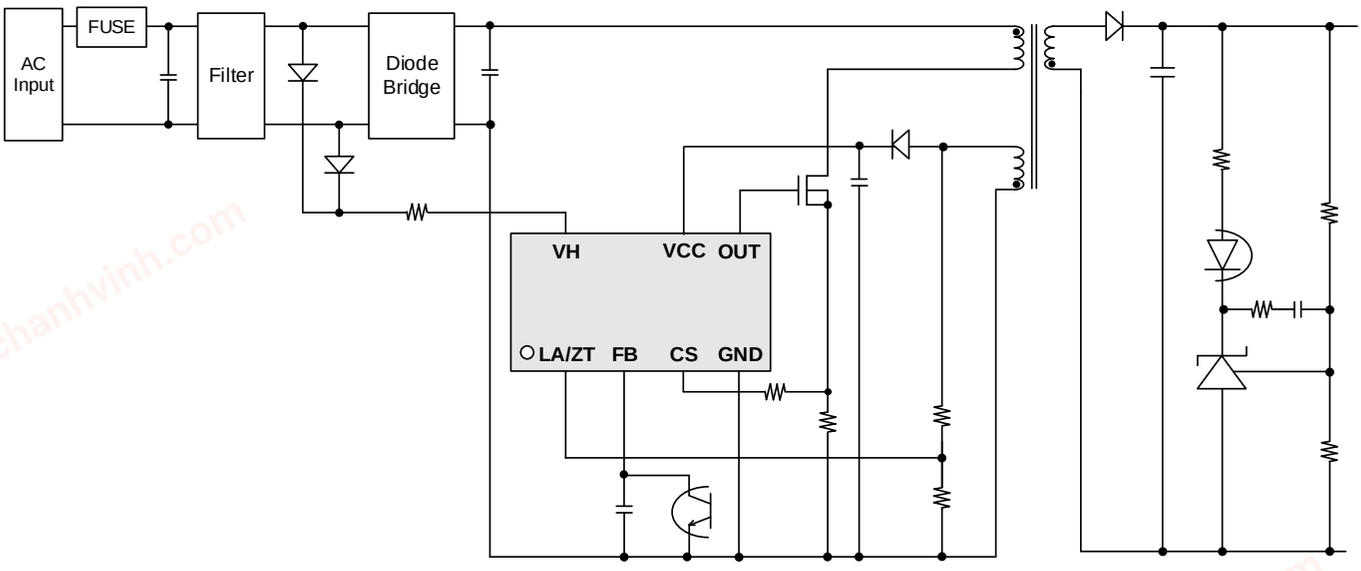
	W (Typ) x D (Typ) x H (Max)
SOP-J7S	4.9 mm x 6.0 mm x 1.65 mm
	Pitch: 1.27 mm (Typ)



Applications

OA Equipment, AC Adapters, Each Household Applications and Power Supplies for Motor

Typical Application Circuit

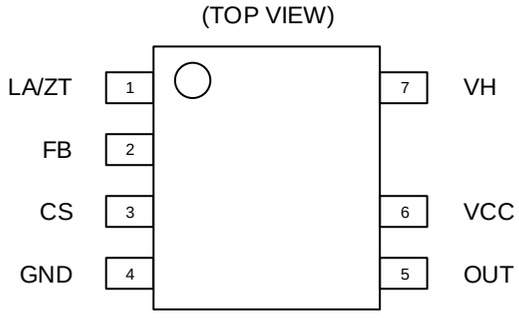


○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration



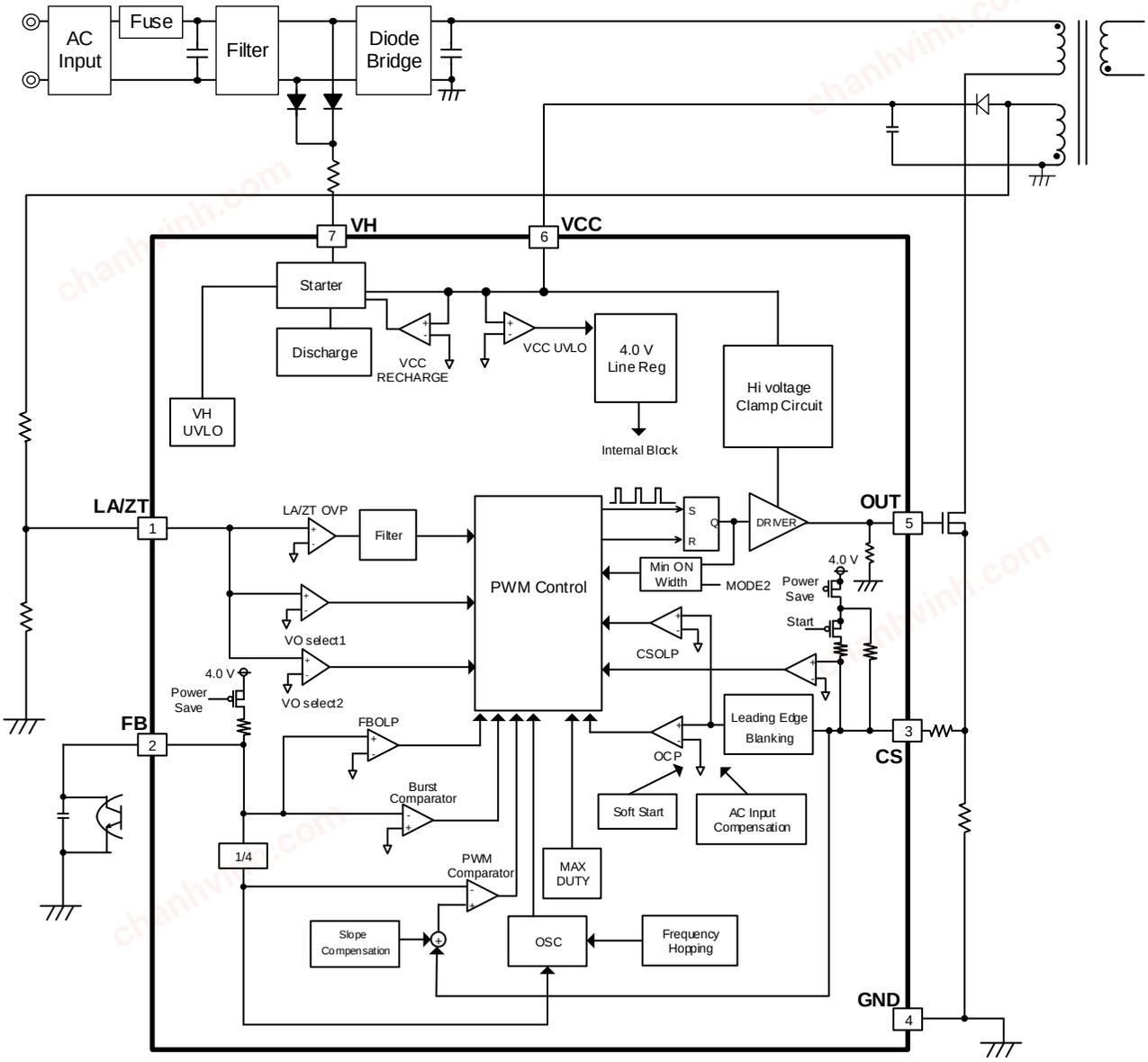
Pin Descriptions

Pin No.	Pin Name	Function
1	LA/ZT	Monitor auxiliary winding / Latch stop pin
2	FB	Feedback signal input pin
3	CS	Primary current detection pin
4	GND	GND pin
5	OUT	External MOSFET drive pin
6	VCC	Power supply input pin
7	VH	Startup power supply input / AC input voltage monitor pin

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Block Diagram



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Description of Blocks

1 Startup Circuit

This IC has a built-in startup circuit. When the AC input voltage is applied, the VH pin is also applied the voltage. Then the VCC pin voltage is charged by applied current to the VCC pin through the startup circuit. This charge is stopped after the VCC pin voltage rises and VCC UVLO is released.

2 AC UVLO (Under Voltage Lockout), X Capacitor Discharge Function

AC UVLO:

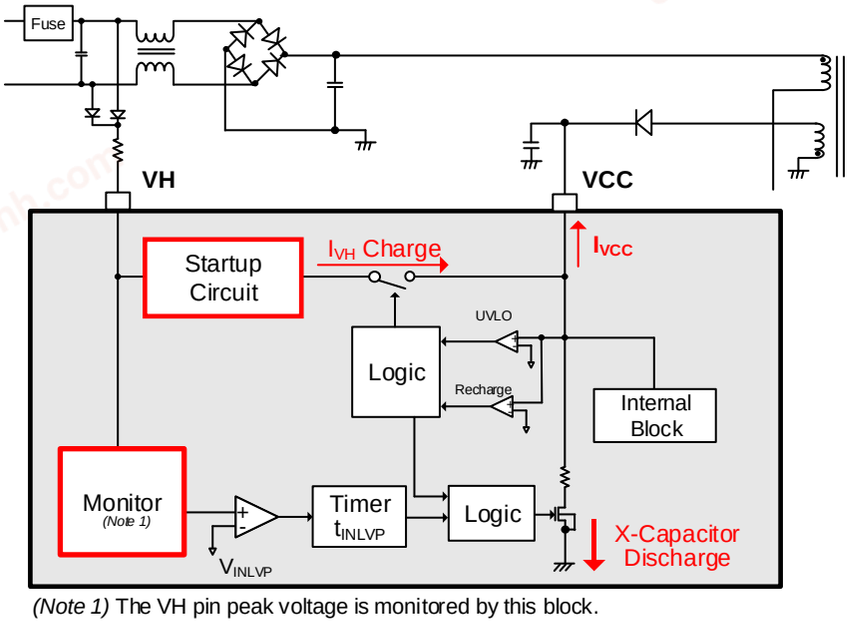
At startup, the voltage occurs at the VH pin when the AC input voltage is applied. The VCC pin waits the detection of AC input voltage remaining applied voltage until the VH pin peak voltage becomes more than V_{INLVP} because this IC charges the VCC pin through the startup circuit. During this term, the switching operation is not operated because AC UVLO operates.

When the VH pin peak voltage becomes more than V_{INLVP}, AC UVLO is released and the operation starts. After stop of supplying of the AC input voltage, the IC stops the switching operation when the status of the VH pin peak voltage ≤ V_{INLVP} continues for t_{INLVP}.

In addition, when there is no continuous up/down of voltage in the VH pin, it also stops the switching operation even though the VH pin peak voltage > V_{INLVP}.

X Capacitor Discharge Function:

When the status of the VH pin peak voltage ≤ V_{INLVP} continues for t_{INLVP} and the switching operation is stopped by AC UVLO, X capacitor discharge function starts to operate.



(Note 1) The VH pin peak voltage is monitored by this block.

Figure 1. Block Diagram of VH Pin and VCC Pin

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2 AC UVLO (Under Voltage Lockout), X Capacitor Discharge Function – continued

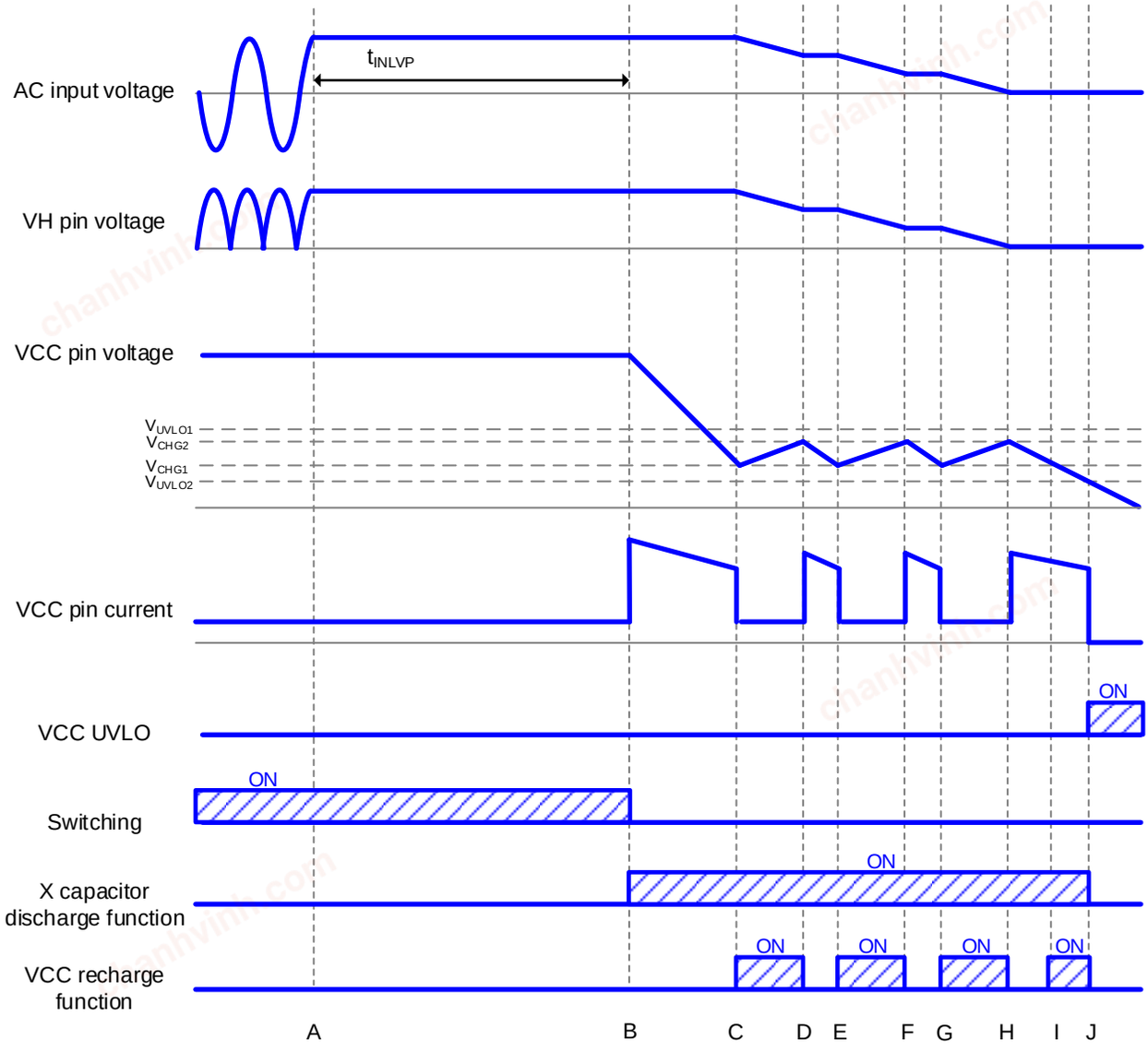


Figure 2. Timing Chart of X Capacitor Discharge Function

A: The AC input voltage is turned OFF, the voltage remains behind because X condenser is charged.
B: After t_{INLVP} from A, the switching operation stops. VCC capacitor is discharged because of the VCC pin voltage > V_{CHG1}.
C: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge operation starts.
D: When the VCC pin voltage becomes more than V_{CHG2}, the VCC recharge operation stops.
E: Same as C.
F: Same as D.
G: Same as C.
H: Same as D.
I: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge function operates. However, the current supply to the VCC pin decreases and the VCC pin voltage continues to drop because of the low VH pin voltage.
J: When the VCC pin voltage becomes less than V_{UVLO2}, VCC UVLO operates.

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Description of Blocks – continued

3 VCC Pin Protection Function

This IC has VCC UVLO and VCC recharge function at the VCC pin.
Use the ZT OVP connected from an auxiliary winding for over voltage protection in output because this IC does not have a built-in VCC OVP (Over Voltage Protection). After the latched stop, it is released when the VCC pin voltage becomes less than V_{LATCH}.

3.1 VCC UVLO (Under Voltage Lockout)

This is an auto recovery comparator with a voltage hysteresis. When the VCC pin voltage becomes less than V_{UVLO2}, the IC stops the operation. And when the VCC pin voltage becomes more than V_{UVLO1}, the operation is restarted.

3.2 VCC Recharge Function

If the VCC pin voltage drops to less than V_{CHG1} after once the VCC pin becomes more than V_{UVLO1} and the IC starts to operate, the VCC recharge function operates. At this time, the VCC pin is recharged from the VH pin through the startup circuit. When the VCC pin voltage becomes more than V_{CHG2}, this recharge is stopped.

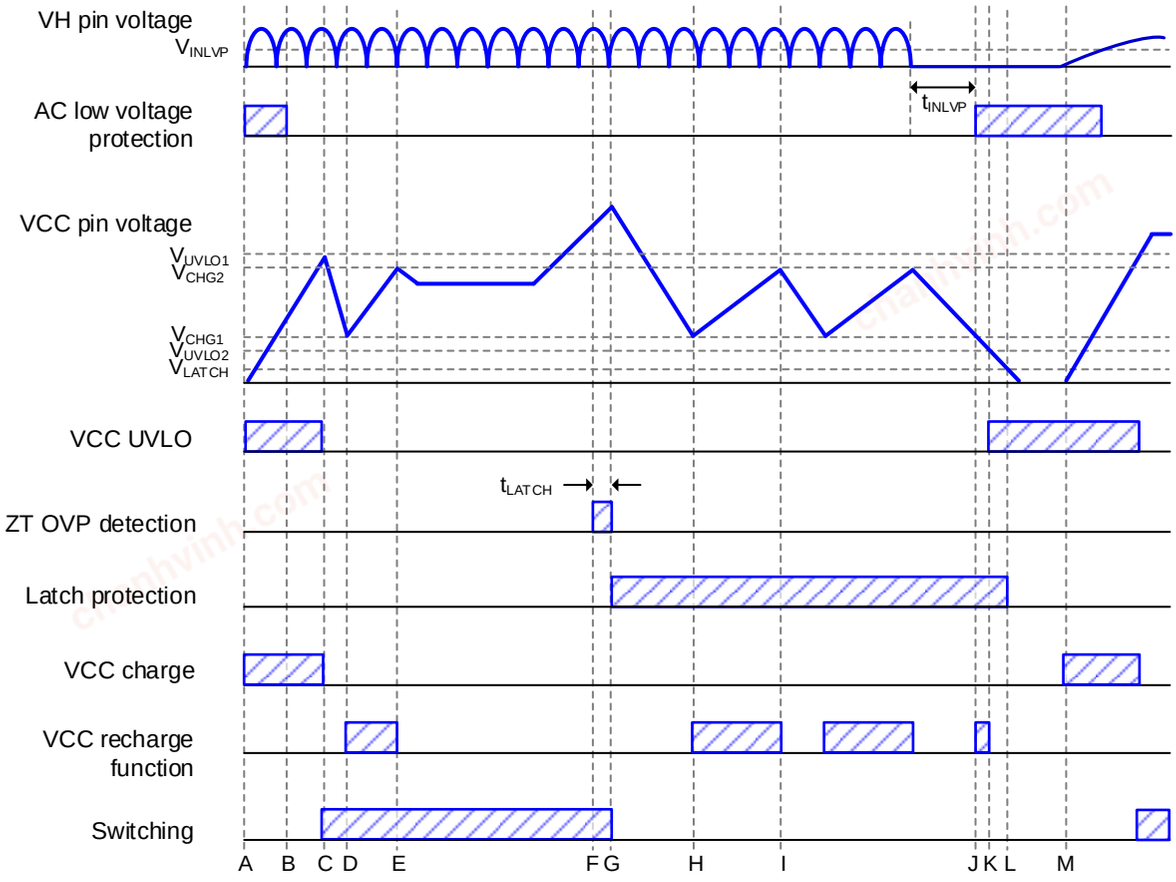


Figure 3. Timing Chart of VCC UVLO and VCC Recharge Function

A: The VH pin is applied voltage and the VCC pin voltage rises.
B: When the VH pin voltage becomes more than V_{INLVP}, AC UVLO is released.
C: When the VCC pin voltage becomes more than V_{UVLO1}, the switching operation starts.
D: When the VCC pin voltage becomes less than V_{CHG1}, the VCC pin is recharged from the VH pin by VCC recharge function.
E: When the VCC pin voltage becomes more than > V_{CHG2}, the VCC recharge function is stopped.
F: The output voltage rises and auxiliary winding voltage also does. At this moment, ZT OVP is detected.
G: When the detection of ZT OVP continues for t_{LATCH}, the switching operation is latched stop.
H: When the VCC pin voltage becomes less than V_{CHG1}, VCC recharge function operates.
I: When the VCC pin voltage becomes more than V_{CHG2}, VCC recharge function stops. By the operation of H and I, the VCC pin voltage is maintained constantly.
J: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge function operates. However, the current supply to the VCC pin decreases and the VCC pin voltage continues to drop because of the low VH pin voltage.
K: When the VCC pin voltage becomes less than V_{UVLO2}, VCC UVLO operates.
L: When the VCC pin voltage becomes less than V_{LATCH}, the latch protection is released.
M: The VH pin is applied voltage and the IC operation restarts.

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Description of Blocks – continued

4 DC/DC Driver Block

This IC performs a current mode PWM control and it has the following characteristics.

- The switching frequency operates in the range of f_{SW3} to f_{SW1} by an internal oscillator. It has a built-in frequency hopping function and the fluctuation cycle is at random. It makes the EMI low by swaying the switching frequency within ±6 %.
- This IC controls the ON width by detecting the peak current using the CS pin voltage correspond to the FB pin voltage. The CS pin voltage is restricted to $1/AV_{CS}$ of the FB pin voltage.
- Maximum duty is fixed at D_{MAX}.
- In the current mode control, a sub-harmonic oscillation may occur when the duty cycle exceeds 50 %. As a countermeasure, this IC has a built-in slope compensation circuit.
- It has a built-in burst mode and frequency reduction circuit to achieve lower power consumption at light load.
- The FB pin is pulled up to the internal power supply by R_{FB}.
- The FB pin voltage is changed by the secondary output voltage. This IC monitors this and changes a switching operation status.

4.1 Transition of Switching Frequency by FB Pin Voltage

This IC operates the burst operation when the FB pin voltage becomes less than V_{BST1} at light load.
At the peak load, the frequency rises to f_{SW1} accompanying with the increase of the FB pin voltage.

mode a:	Burst Operation	(The intermittent operation starts.)
mode b:	Fixed Frequency Operation 1	(It operates in f_{SW3})
mode c:	Frequency Reduction Operation 1	(It reduce the frequency.)
mode d:	Fixed Frequency Operation 2	(It operates in f_{SW2})
mode e:	Frequency Reduction Operation 2	(It reduce the frequency.)
mode f:	Fixed Frequency Operation 3	(It operates in f_{SW1})

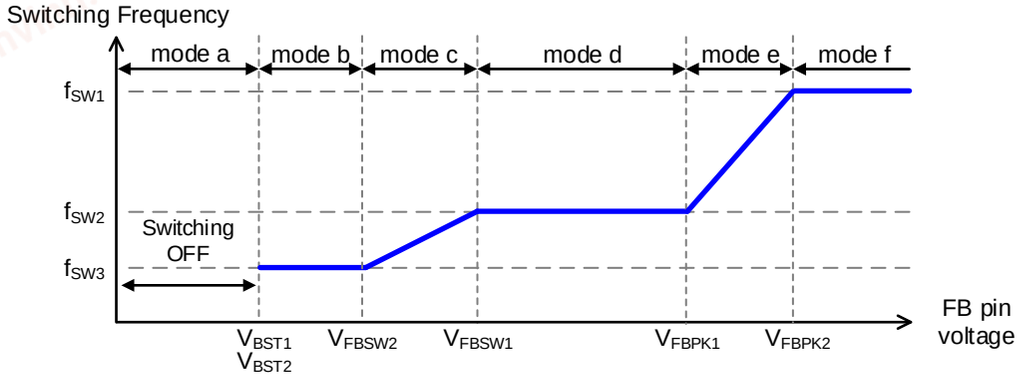


Figure 4. State Transition of Switching Frequency

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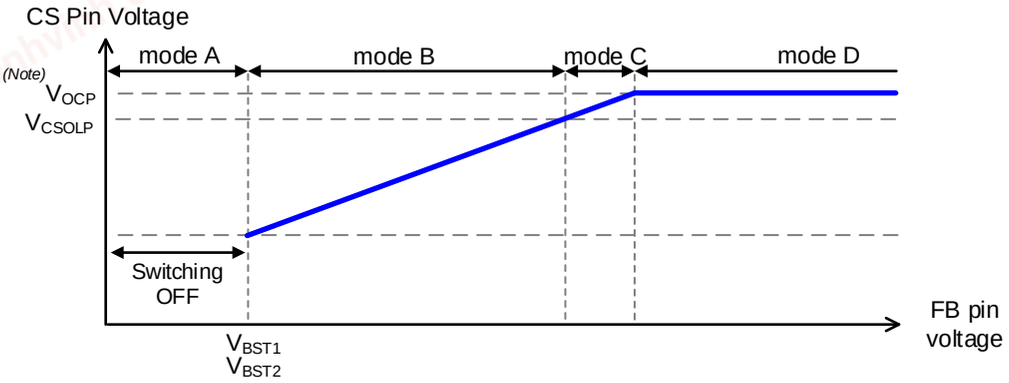
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4 DC/DC Driver Block – continued

4.2 Transition of CS Pin Voltage by FB Pin Voltage

This IC operates as shown below.

mode A: Burst Operation
mode B: Normal Load Operation (The CS pin voltage changes corresponding to the FB pin voltage.)
mode C: CS Overload Operation (Latched stop is operated by CS OLP when this status lasts for t_{CSOLP}.)
mode D: FB Overload Operation (The peak voltage is restricted to V_{OCP1}.
Latched stop is operated by FB OLP when this status lasts for t_{FBOLP}.)



(Note) V_{OCP} means V_{OCP1} to V_{OCP3} and this depends on AC voltage compensation function or operation modes.
V_{CSOLP} means V_{CSOLP1} to V_{CSOLP5} and this depends on Value of R_{CSS}.

Figure 5. State Transition of CS Pin Voltage by FB Pin Voltage

4.3 Switch Function of Operation Modes

This IC switches the operation modes by detecting the output voltage at the LA/ZT pin. It contributes to reduction of standby electric power by the three operation modes they correspond to normal, light and no load. At startup, this IC starts the operation from operation mode 1.

Table 1. Operation Modes

Operation Mode	Load Status	Range of LA/ZT pin high voltage
1	Normal Load	$>V_{ZT2}$
2	Light Load	V_{ZT1} to V_{ZT2}
3	No Load	$<V_{ZT1}$

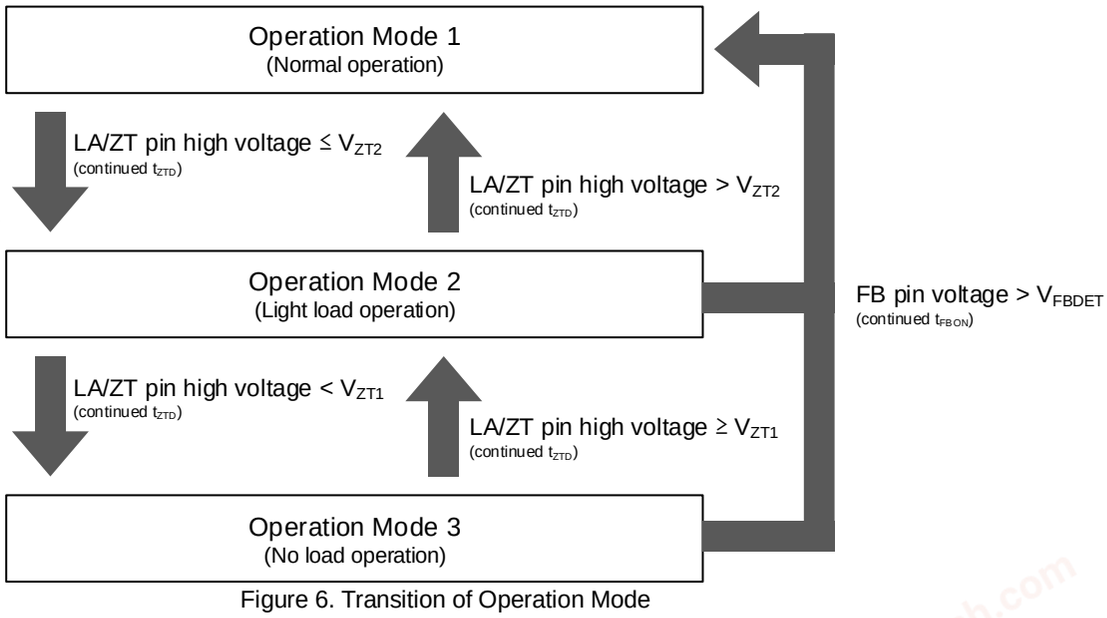


Figure 6. Transition of Operation Mode

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4.3 Switch Function of Operation Modes – continued

The operation modes are switched by detecting the LA/ZT pin voltage shown as Figure 6.
When the FB pin voltage > V_{FBDET} in operation mode 1, however, the operation modes are not switched even if the status of the LA/ZT pin voltage ≤ V_{ZT2} continues for t_{ZTD}.

In addition, when the status of the FB pin voltage > V_{FBDET} continues for t_{FBON} in operation mode 2 and 3, the IC interprets the load status is changed and the operation mode shifts to 1.

4.3.1 Setting of the LA/ZT Pin Voltage

V_{ZT1} is calculated by the formula below.
Set the LA/ZT pin voltage using the output voltage V_{OUT} by adjusting the resistor value of R_{ZT1} and R_{ZT2}.

$$Va = Nd \div Ns \times (V_{OUT} - Vf)$$
$$V_{ZT1} = R_{ZT2} \div (R_{ZT1} + R_{ZT2}) \times Va \quad [V]$$

Va is the voltage of auxiliary winding.
Ns is the number of wind in the secondary side.
Nd is the number of wind in the auxiliary winding.
Vf is the forward voltage of secondary diode.
R_{ZT1} is the upper resistor value of auxiliary winding.
R_{ZT2} is the lower resistor value of auxiliary winding.

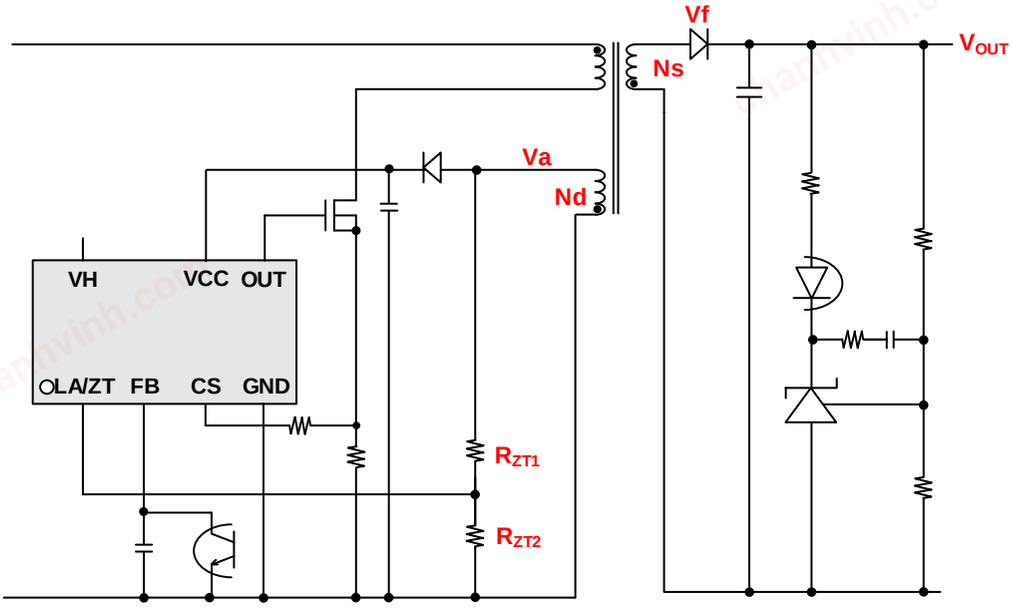


Figure 7. Items Positions Used in Setting Output Voltage

4.3.2 Setting of Operation Modes

Each operation mode works as shown the table below.
In operation mode 3, it is achieved to reduce the maximum electric power consumption by the increase of primary peak current and reduction of IC's current consumption.

Table 2. States of Each Operation Modes

	Operation Mode 1	Operation Mode 2	Operation Mode 3
Over Current Detected Voltage	V_{OCP1} to V_{OCP2}	V_{OCP1} to V_{OCP2}	V_{OCP3}
Current Consumption	Normal	Normal	Power Save
Voltage Gain (FB pin / CS pin)	AV_{CS}	AV_{CS}/Ka	AV_{CS}/Ka
Burst Operation	Normal	Normal	Power Save
Minimum ON Width	t_{MIN1}	t_{MIN2}	t_{MIN1}

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4.3 Switch Function of Operation Modes – continued

4.3.3 Burst Mode at Each Operation Mode

4.3.3.1 Operation Mode 1

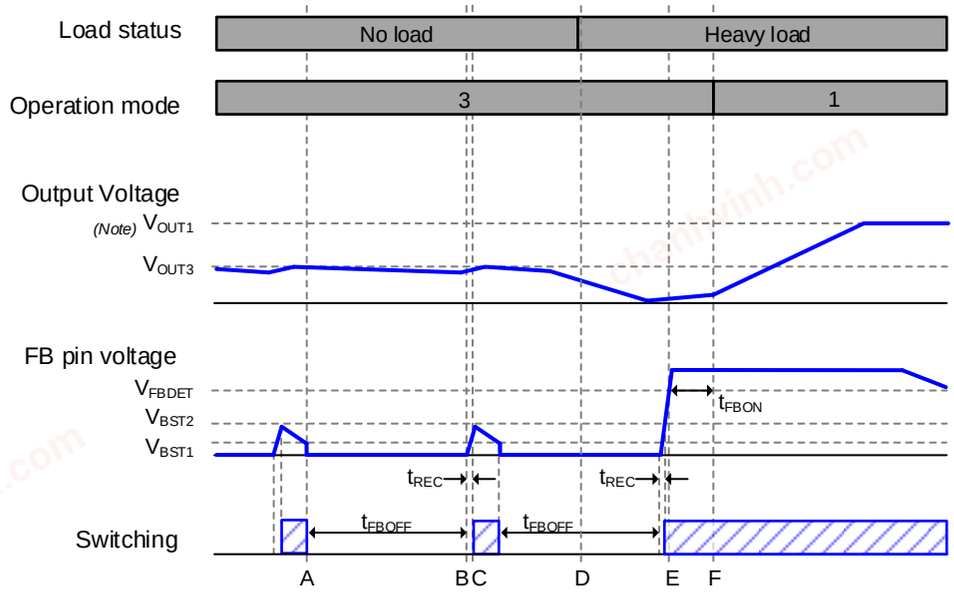
When the FB pin voltage becomes less than V_{BST1}, the switching operation stops. When the FB pin voltage becomes more than V_{BST2}, the switching operation restarts.

4.3.3.2 Operation Mode 2

The FB pin voltage becomes less than < V_{BST1}, the switching operation stops. When the FB pin voltage becomes more than V_{BST2}, the switching operation restarts.
In operation mode 2, the IC lowers the voltage gain and increases the primary peak current by 1.33 times. And the minimum ON width is switched to t_{MIN2}. These functions reduce the number of switching and burst frequency and cut down the switching loss.

4.3.3.3 Operation Mode 3

In operation mode 3, the IC lowers the voltage gain and increases the primary peak current by 1.33 times. These functions reduce the number of switching and burst frequency and cut down the switching loss.



(Note) V_{OUT1} and V_{OUT3} means the output voltage at Operation Mode 1 and Operation Mode 3.

Figure 8. In Case of Load Increase at Operation Mode 3

A: When the FB pin voltage becomes less than V_{BST1}, the switching operation is stopped. For t_{FBOFF} from this stop, the IC's current consumption is restricted to I_{SAVE} by the power save function.
B: After t_{FBOFF} from A, the timer of burst release recovery time starts to operate.
C: After t_{REC} from B, when the FB pin voltage become more than V_{BST2}, the switching operation restarts.
D: The setting of the output voltage is switched V_{OUT3} to V_{OUT1} in the secondary side.
E: After restarting the switching operation, when the FB pin voltage becomes more than V_{FBDET}, the operation mode switching detection timer 2 starts to work.
F: The status of the FB pin voltage > V_{FBDET} lasts more than t_{FBON}, the operation mode shifts to 1. (The timer is reset if the FB pin voltage becomes V_{FBDET} or less within t_{FBON}, and the switching operation stops again for t_{FBOFF} if the FB pin voltage becomes less than V_{BST1})

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4 DC/DC Driver Block – continued

4.4 Soft Start Function

At startup, this function controls the over current detection voltage in order to prevent any excessive voltage or current rising. This IC enables the soft start operation by changing the over current detection voltage with time.

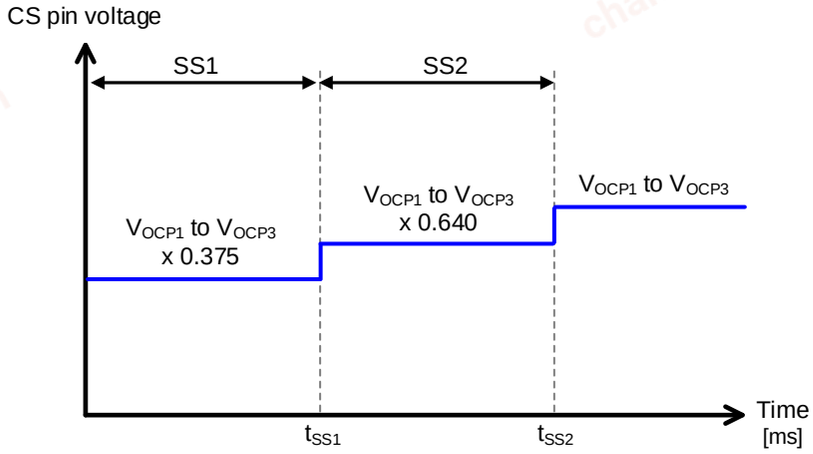
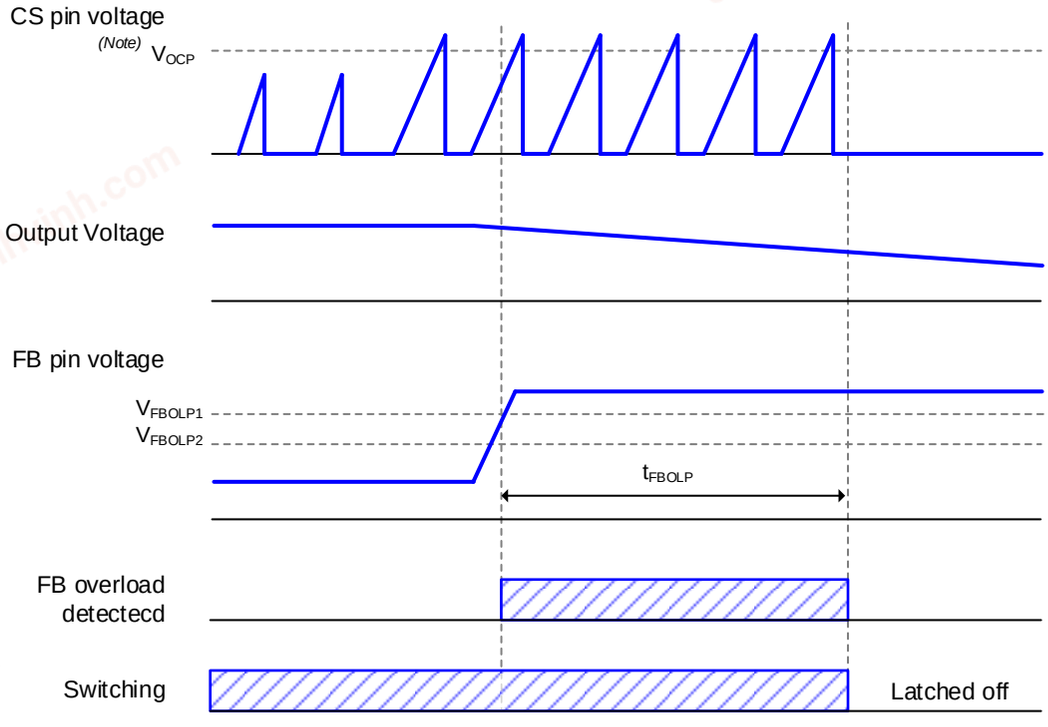


Figure 9. Soft Start Function

4.5 FB OLP (Overload Protection)

This IC is latched off when status that the FB pin voltage > V_{FBOLP1} lasts for t_{FBOLP}.
When the FB pin voltage becomes less than V_{FBOLP2}, the detection timer t_{FBOLP} is released.



(Note) V_{OCP} means V_{OCP1} to V_{OCP3} and this depends on AC voltage compensation function or operation modes.

Figure 10. FB Overload Protection Function

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4 DC/DC Driver Block – continued

4.6 CS Pin Protection Function

This IC has a built-in CS OLP and CS OCP in the CS pin.

Table 3. Operation Status of CS Pin Protection Functions

Function	Load Status at Operation to Protect	Detection Voltage	Operation to Protect
CS OLP	Over the rated load (Without lowing of the output voltage)	CS pin peak voltage > V_{CSOLP1} to V_{CSOLP5} (for t_{CSOLP}) (set by the external resistor at the CS pin)	IC is latched off
CS OCP	Over the peak load (Lowing the output voltage)	CS pin peak voltage > V_{OCP1} to V_{OCP3} (Changed by AC voltage compensation function at operation mode 1 and 2)	Turned off by pulse

4.6.1 CS OLP (Overload Protection)

This IC has a built-in overload protection function correspond to rated load.
When the status of the CS pin peak voltage > V_{CSOLP1} to V_{CSOLP5} lasts for t_{CSOLP}, this IC is latched off. It is not turned off by pulse per pulse. In addition, the overload detection voltage can be switched by the value of the external resistor R_{CSS} at the CS pin.

This IC monitors the voltage occurred in the CS pin after t_{SET} from the release of VCC UVLO and switches the V_{CSOLP1} to V_{CSOLP5} as shown in Table 4. For t_{SET}, the CS pin is pulled up by R_{CS2} in the internal reference voltage.

Table 4. Detection Voltage

Detection Voltage	R_{CSS} (kΩ)
V_{CSOLP1}	0.0 to 1.0
V_{CSOLP2}	2.0 to 2.4
V_{CSOLP3}	4.7 to 5.6
V_{CSOLP4}	10.0 to 12.0
V_{CSOLP5}	20.0 or above

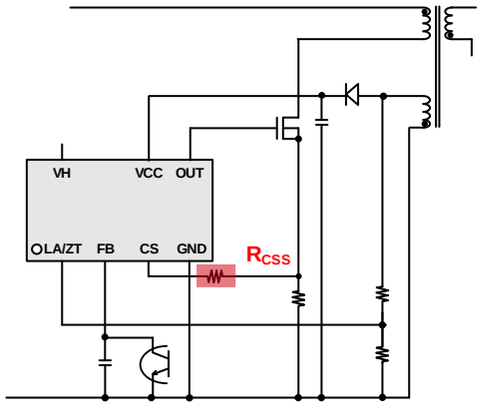
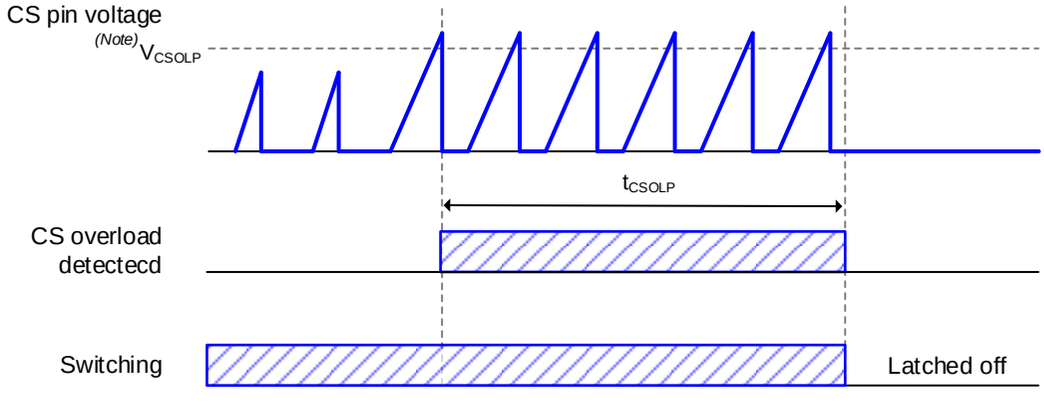


Figure 11. Position of R_{CSS}



(Note) V_{CSOLP} means V_{CSOLP1} to V_{CSOLP5} and this depends on Value of R_{CSS}.

Figure 12. CS Pin Overload Protection

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4.6 CS Pin Protection Function – continued

4.6.2 CS OCP (Over Current Protection)

This IC has a built-in over current protection function per switching cycles. This function stops the switching operation if the CS pin peak voltage becomes more than V_{OCP1} to V_{OCP3}. It also has a built-in AC voltage compensation function. This function compensates the dependent on AC voltage by making V_{OCP1} to V_{OCP3} increase with time. V_{OCP1} to V_{OCP3} is also changed by the operation modes.

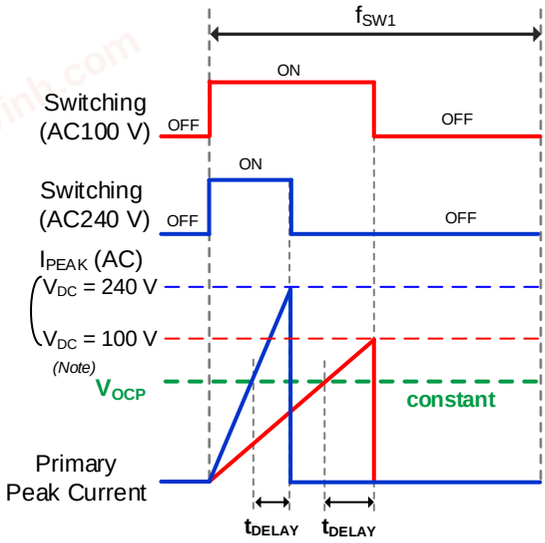


Figure 13. Without the Compensation Function

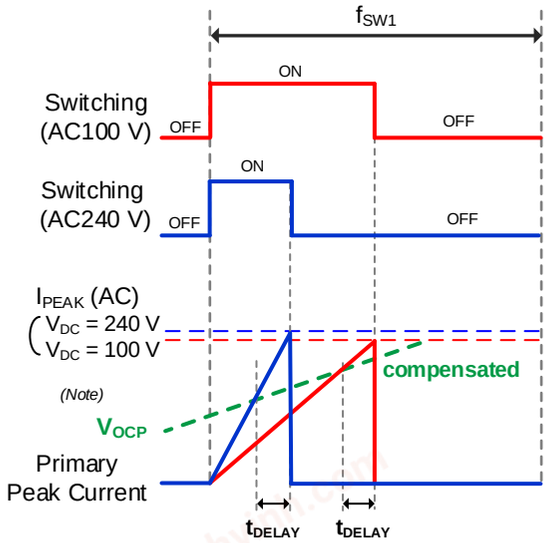


Figure 14. With the Compensation Function

(Note) V_{OCP} means V_{OCP1} to V_{OCP3} and this depends on AC voltage compensation function or operation modes.

4.6.2.1 AC Voltage Compensation Function

The dependent on AC voltage of primary peak current is compensated by changing the over current detection voltage of the CS pin with time. The primary peak current entering overload mode is calculated using the formula below.

$$I_{PEAK} = V_{OCP1} \div Rs + V_{DC} \div Lp \times t_{DELAY} \quad [A]$$

I_{PEAK} is the primary peak current.
V_{OCP1} is the over current detection voltage V_{OCP1}.
Rs is the current detection resistor.
V_{DC} is the input DC voltage.
Lp is the value of primary coil inductor.
t_{DELAY} is the delay time after the over current detection.

The over current detection voltage is set by t_{ON} in the range of V_{OCP1} to V_{OCP2}. Calculated the over current detection voltage with the approximation below.

$$V_{OCP} = -0.0104 \times {t_{ON}}^2 + 0.1032 \times t_{ON} + 0.36[V]$$

V_{OCP}: is the over current detection voltage set by t_{ON}
t_{ON} is the ON time.

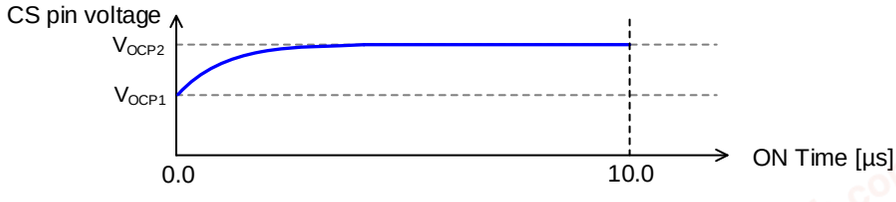


Figure 15. State Transition of Over Current Detection Voltage by Time

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4.6 CS Pin Protection Function – continued

4.6.3 Leading Edge Blanking Function

Normally, when the MOSFET for switching is turned ON, surge current is generated at each capacitor component and drive current and so on. At this time, detection errors may occur in the over current protection function because the CS pin voltage rises temporary. To prevent these errors, Leading Edge Blanking function is built in this IC. This function masks the CS pin voltage for t_{LEB} from the switch of the OUT pin voltage low to high.

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Description of Blocks – continued

5 ZT OVP (Over Voltage Protection)

The LA/ZT pin has two built-in latch type over voltage protection function which are the pulse detection and DC detection.

5.1 DC Detection

When the status that the LA/ZT pin voltage > V_{ZTL} lasts for more than t_{LATCH}, the switching operation is latched off.

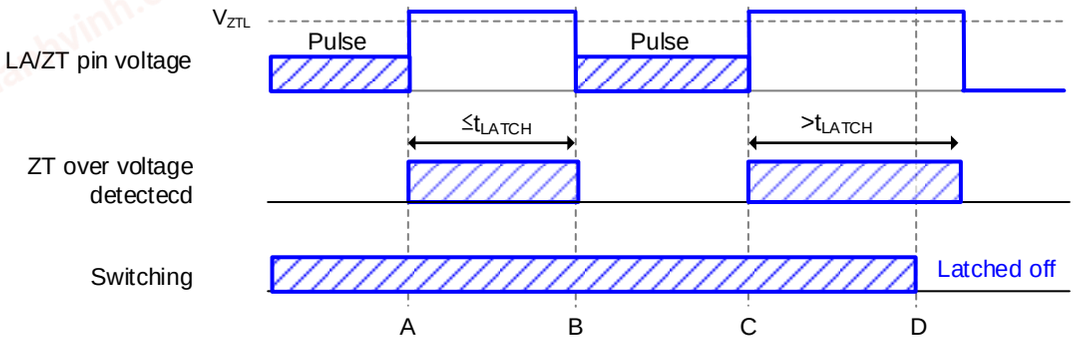


Figure 16. LA/ZT Pin Over Voltage Protection (DC Detection)

A: When the LA/ZT pin voltage becomes more than V_{ZTL}, ZT OVP detection timer t_{LATCH} starts to operate.
B: The timer is reset because the LA/ZT pin voltage becomes V_{ZTL} or less within t_{LATCH}.
C: When the LA/ZT pin voltage becomes more than V_{ZTL}, ZT OVP detection timer t_{LATCH} starts to operate.
D: When the status of the LA/ZT pin voltage > V_{ZTL} lasts for more than t_{LATCH}, the switching operation is latched off.

5.2 Pulse Detection

This IC is latched off when it passes from the three consecutive detections of the LA/ZT pin voltage pulse > V_{ZTL} for t_{LATCH}. The IC does not detect the LA/ZT pin voltage for this term because it has a built-in ZT OVP detection mask timer t_{ZTMK} corresponding the surge at the turn on of the LA/ZT pin voltage.

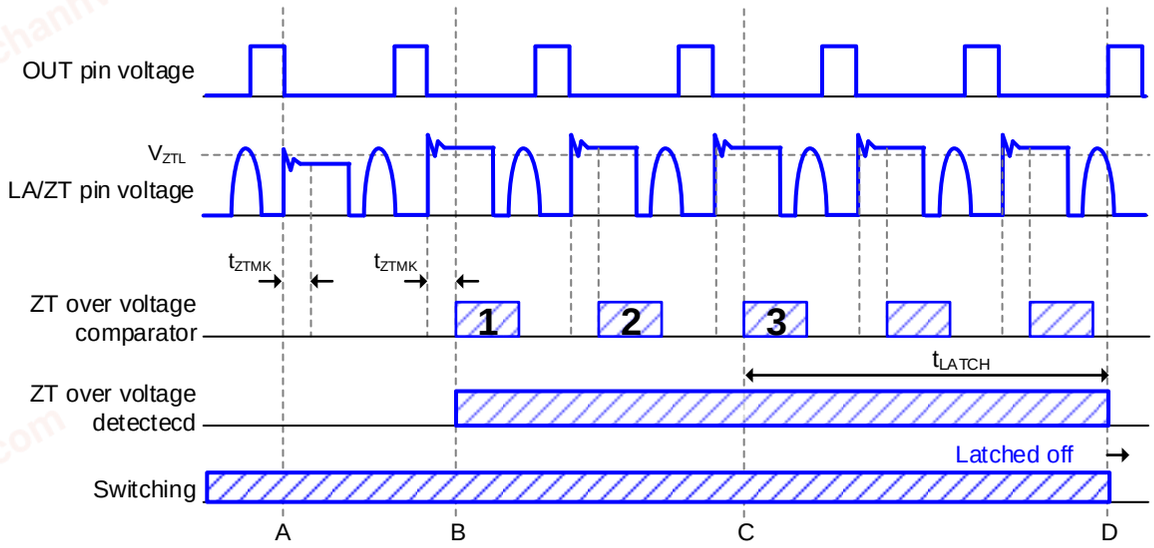


Figure 17. LA/ZT Pin Over Voltage Protection (Pulse Detection)

A: When the OUT pin is turned OFF, the LA/ZT pin becomes high voltage. The LA/ZT pin voltage becomes more than V_{ZTL} momentary, however, ZT OVP is not detected because it is within t_{ZTMK} from reaching high voltage.
B: When the LA/ZT pin voltage > V_{ZTL} is detected after t_{ZTMK} from reaching high voltage, ZT OVP is detected.
C: When the three consecutive voltage pulse of the LA/ZT pin voltage > V_{ZTL} is detected, ZT OVP detection timer t_{LATCH} starts to operate.
D: When it passes from C for t_{LATCH}, the switching operation is latched off.

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Description of Blocks – continued

6 OUT Pin Gate Clamp Circuit

The high level of the OUT pin is clamped to V_{OUTH} to prevent the gate voltage of external MOSFET from being damaged. The OUT pin is pulled down by R_{PDOUT} in the inside.

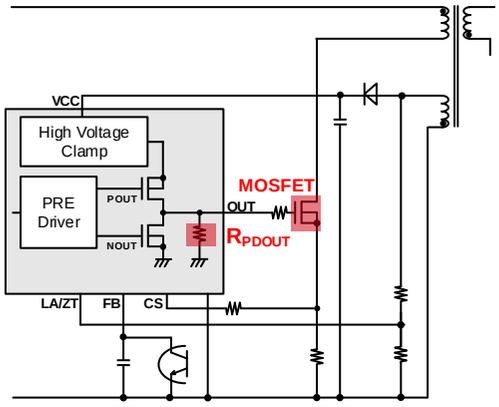


Figure 18. Positions of External MOSFET and R_{PDOUT}

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Description of Blocks – continued

7 Operation Mode of Protection Functions

The operation modes of each protection function are shown in Table 5

Table 5. Operation Modes of Protection Functions

	AC UVLO	VCC UVLO	FB OLP
Detection Conditions	VH pin peak voltage ≤ V_{INLVP}	VCC pin voltage < V_{UVLO2} (at voltage falling)	FB pin voltage > V_{FOLP1} (at voltage rising)
Release Conditions	VH pin peak voltage > V_{INLVP}	VCC pin voltage > V_{UVLO1} (at voltage rising)	VCC pin voltage < V_{LATCH}
Detection Timer (Reset Conditions)	t_{INLVP} (VH pin peak voltage > V_{INLVP})	–	t_{FBOLP} (FB pin voltage < V_{FOLP2})
Release Timer (Reset Conditions)	–	–	–
Auto Recovery or Latch	Auto Recovery	Auto Recovery	Latch

	CS OLP	ZT OVP
Detection Conditions	CS pin peak voltage > V_{CSOLP} (V_{CSOLP} is set by R_{CS})	ZT pin peak voltage > V_{ZTL}
Release Conditions	VCC pin voltage < V_{LATCH}	VCC pin voltage < V_{LATCH}
Detection Timer (Reset Conditions)	t_{CSOLP} (CS pin peak voltage ≤ V_{CSOLP})	t_{LATCH} (ZT pin peak voltage < V_{ZTL})
Release Timer (Reset Conditions)	–	–
Auto Recovery or Latch	Latch	Latch

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Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Condition
Maximum Applied Voltage 1	V_{MAX1}	to +6.5	V	LA/ZT pin *(Note 1)*
Maximum Applied Voltage 2	V_{MAX2}	-0.3 to +6.5	V	FB pin
Maximum Applied Voltage 3	V_{MAX3}	-0.3 to +6.5	V	CS pin
Maximum Applied Voltage 4	V_{MAX4}	-0.3 to +15	V	OUT pin
Maximum Applied Voltage 5	V_{MAX5}	-0.3 to +58	V	VCC pin
Maximum Applied Voltage 6	V_{MAX6}	-0.3 to +650	V	VH pin
LA/ZT Pin Maximum Source Current	I_{SZT1}	+1.0	mA	
LA/ZT Pin Maximum Sink Current	I_{SZT2}	-4.0	mA	
OUT Pin Maximum Source Current	I_{SOOUT}	0.20	A	
OUT Pin Maximum Sink Current	I_{SKOUT}	1.00	A	
Power Dissipation	Pd	0.68	W	*(Note 2)*
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) *Need to use the LA/ZT pin voltage within the range of LA/ZT Pin Maximum Source Current and LA/ZT Pin Maximum Sink Current.*

(Note 2) At mounted on a glass epoxy single layer PCB (114.3 mm x 76.2 mm x 1.57 mm). Derate by 5.4 mW/°C if the IC is used in the ambient temperature Ta 25 °C or above.

Thermal Dissipation

Make the thermal design so that the IC operates in the following conditions.
(Because the following temperature is guarantee value, it is necessary to consider margin.)

1. The ambient temperature Ta must be 105 °C or less.
2. The IC's loss must be the power dissipation Pd or less.

The thermal abatement characteristic is as follows.
(At mounting on a glass epoxy single layer PCB which size is 114.3 mm x 76.2 mm x 1.57 mm)

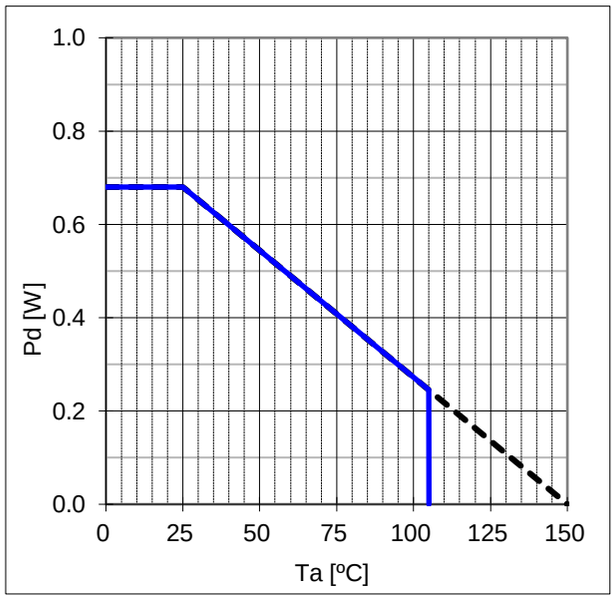


Figure 19. SOP-J7S Thermal Dissipation Characteristic

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Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
VCC Pin Power Supply Range	V_{CC}	9.3	-	55.0	V
VH Pin Power Supply Range	V_H	-	-	300 *(Note 2)*	V
VCC Pin Capacitor	C_{VCC}	4.7	-	-	µF
VH Pin Resistor	R_{VH}	-	-	2.0	kΩ
Operating Temperature	Topr	-40	-	+105	°C

(Note 2) The recommendation maximum operating voltage shows AC 300 V which is the input AC voltage in the application. Apply the input AC voltage which is full-wave-rectified to the VH pin.

Electrical Characteristics

(Unless otherwise noted, Ta = 25 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Circuit Current						
Current at Switching Operation	I_{ON1}	0.20	0.70	1.30	mA	FB pin voltage = 2.0 V
Current at Burst Operation	I_{ON2}	0.20	0.35	0.50	mA	FB pin voltage = 0.3 V
Current at Power Save Operation	I_{SAVE}	0.04	0.11	0.16	mA	Operation Mode 3
Current at Latched Stop	I_{LATCH}	0.10	0.22	0.35	mA	
Startup Circuit Block and VH Pin Protection Function						
Startup Current	I_{START1}	8.0	15.0	25.0	mA	V_{CC} = 10 V, V_H = 100 V
VH Pin OFF Current	I_{START2}	5	12	20	µA	V_H = 100 V
AC UVLO Detection Voltage	V_{INLVP}	83	99	115	V	
AC UVLO Stop Timer	t_{INLVP}	105	150	195	ms	
VCC Pin Protection Function						
VCC UVLO Release Voltage	V_{UVLO1}	12.50	13.50	14.50	V	At VCC pin voltage rising
VCC UVLO Detection Voltage	V_{UVLO2}	7.90	8.60	9.30	V	At VCC pin voltage falling
VCC UVLO Hysteresis	V_{UVLO3}	-	4.90	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
VCC Recharge Start Voltage	V_{CHG1}	8.60	9.30	10.00	V	
VCC Recharge Stop Voltage	V_{CHG2}	9.40	10.20	11.00	V	
Latch Release Voltage	V_{LATCH}	-	V_{UVLO2} – 1.0	-	V	VCC pin voltage

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Electrical Characteristics – continued
(Unless otherwise noted, Ta = 25 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DC/DC Driver Block						
Switching Frequency 1	f_{SW1}	111	130	149	kHz	
Switching Frequency 2	f_{SW2}	90	100	110	kHz	
Switching Frequency 3	f_{SW3}	18	28	38	kHz	
Voltage Gain (FB Pin / CS Pin)	AV_{CS}	-	4.0	-	V/V	Operation Mode 1
Voltage Gain Shift Factor	Ka	-	1.33	-	V/V	Operation Mode 2, 3
Maximum Duty	D_{MAX}	67	75	83	%	
FB Pin Burst Voltage 1	V_{BST1}	0.350	0.400	0.450	V	At the FB pin voltage falling
FB Pin Burst Voltage 2	V_{BST2}	-	0.450	-	V	At the FB pin voltage rising
Frequency Reduction Start FB Pin Voltage	V_{FBSW1}	1.15	1.35	1.55	V	
Frequency Reduction Stop FB Pin Voltage	V_{FBSW2}	0.95	1.15	1.35	V	
Peak Load Frequency Rising Start Voltage	V_{FBPK1}	2.8	3.0	3.2	V	
Peak Load Frequency Rising Stop Voltage	V_{FBPK2}	3.0	3.2	3.4	V	
CS Pin Leading Edge Blanking Time	t_{LEB}	-	0.300	-	µs	
CS Pin Pulled up Resistor 1	R_{CS1}	0.7	1.0	1.3	MΩ	At Normal Operation
CS Pin Pulled up Resistor 2	R_{CS2}	14	20	26	kΩ	At Startup
FB Pin Pulled up Resistor	R_{FB}	24	30	36	kΩ	
Minimum ON Width 1	t_{MIN1}	-	0.40	-	µs	Operation Mode 1, 3
Minimum ON Width 2	t_{MIN2}	1.5	2.0	2.5	µs	Operation Mode 2
DC/DC Driver Block (Switch Function of Operation Modes)						
Switching Operation Mode LA/ZT Pin Voltage 1	V_{ZT1}	0.60	0.70	0.80	V	
Switching Operation Mode LA/ZT Pin Voltage 2	V_{ZT2}	1.80	2.00	2.20	V	
Switching Operation Mode FB Pin Voltage	V_{FBDET}	0.64	0.70	0.76	V	
Switching Operation Mode Detection Timer 1	t_{ZTD}	3.15	4.50	5.85	ms	LA/ZT pin voltage
Switching Operation Mode Detection Timer 2	t_{FBON}	1.72	2.30	2.88	ms	FB pin voltage
Stop Timer at Burst Operation	t_{FBOFF}	8.0	10.0	12.0	ms	
Recovery Timer at Burst Operation Released	t_{REC}	50	100	200	µs	
DC/ DC Driver Block (Soft Start Function)						
Soft Start Time 1	t_{SS1}	0.66	1.10	1.54	ms	
Soft Start Time 2	t_{SS1}	2.76	4.60	6.40	ms	
DC/ DC Driver Block (FB Pin Overload Protection Function)						
FB OLP Detection Voltage	V_{FBOLP1}	3.20	3.40	3.60	V	
FB OLP Release Voltage	V_{FBOLP2}	3.00	3.20	3.40	V	
FB OLP Detection Timer	t_{FBOLP}	234	300	366	ms	

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Electrical Characteristics – continued
(Unless otherwise noted, Ta = 25 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
DC/ DC Driver Block (CS Pin Overload Protection Function)						
CS OLP Detection Voltage 1	V_{CSOLP1}	0.320	0.350	0.380	V	R_{CSS} = 0 to 1.0 kΩ
CS OLP Detection Voltage 2	V_{CSOLP2}	0.370	0.400	0.430	V	R_{CSS} = 2.0 to 2.4 kΩ
CS OLP Detection Voltage 3	V_{CSOLP3}	0.415	0.450	0.485	V	R_{CSS} = 4.7 to 5.6 kΩ
CS OLP Detection Voltage 4	V_{CSOLP4}	0.460	0.500	0.540	V	R_{CSS} = 10 to 12 kΩ
CS OLP Detection Voltage 5	V_{CSOLP5}	0.510	0.550	0.590	V	R_{CSS} = 20 kΩ or more
CS OLP Detection Timer	t_{CSOLP}	1063	1450	1836	ms	
CS OLP Detection Voltage Setting Time	t_{SET}	150	300	450	µs	
DC/ DC Driver Block (CS Pin Over Current Protection Function)						
CS OCP Detection Voltage 1	V_{OCP1}	0.330	0.350	0.370	V	t_{ON} = 0 µs (Operation Mode1, 2)
CS OCP Detection Voltage 2	V_{OCP2}	-	0.620	-	V	t_{ON} = 10 µs (Operation Mode 1, 2)
CS OCP Detection Voltage 3	V_{OCP3}	0.180	0.200	0.220	V	Operation Mode 3
LA/ZT Pin Protection Function Block						
ZT OVP Detection Voltage	V_{ZTL}	4.50	4.70	4.90	V	
ZT OVP Detection Timer	t_{LATCH}	75	150	250	µs	
ZT OVP Detection Mask Timer	t_{ZTMK}	-	0.40	-	µs	
OUT Pin Gate Clamp Circuit Block						
OUT Pin Clamp Voltage	V_{OUTH}	10.50	12.50	14.50	V	V_{CC} = 15 V
OUT Pin Nch MOS R_{ON}	R_{NOUT}	-	4.8	8.0	Ω	
OUT Pin Pulled down Resistor	R_{PDOUT}	70	100	130	kΩ	

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Typical Performance Curves
(Reference Data)

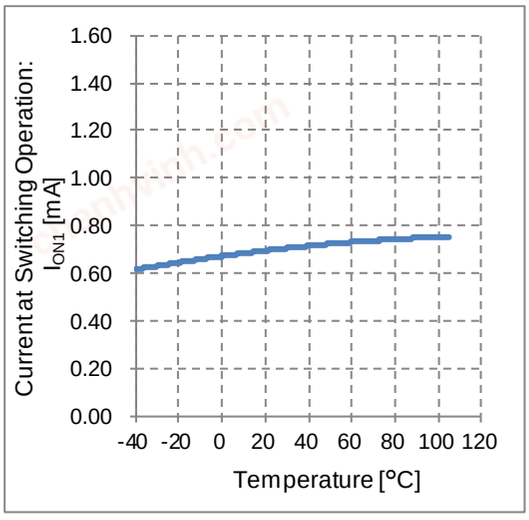


Figure 20. Current at Switching Operation vs Temperature

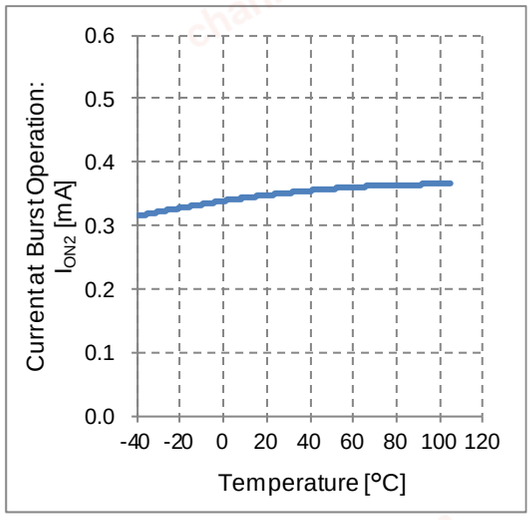


Figure 21. Current at Burst Operation vs Temperature

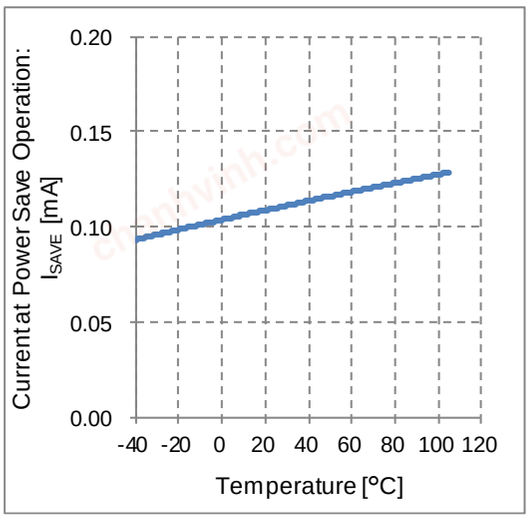


Figure 22. Current at Power Save Operation vs Temperature

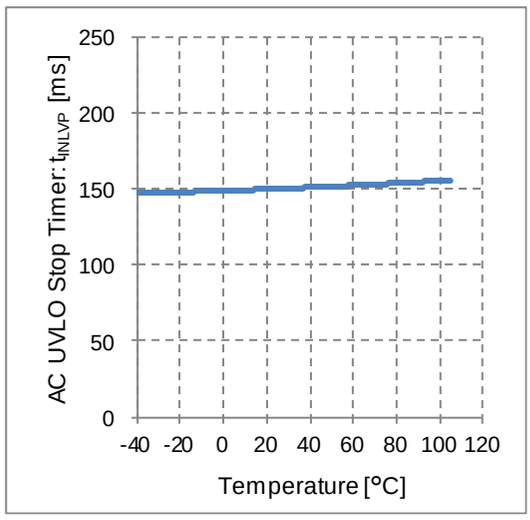


Figure 23. AC UVLO Stop Timer vs Temperature

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Typical Performance Curves – continued
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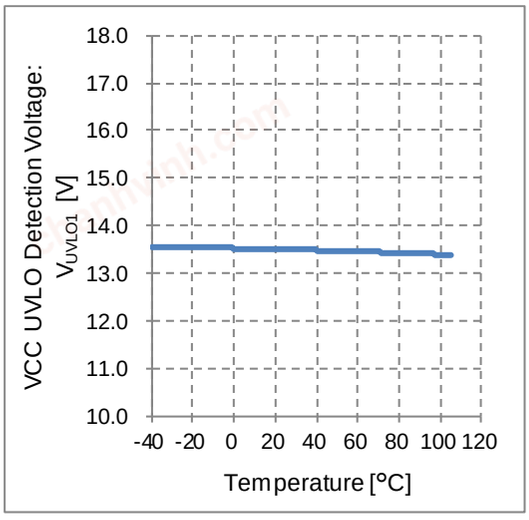


Figure 24. VCC UVLO Detection Voltage vs Temperature

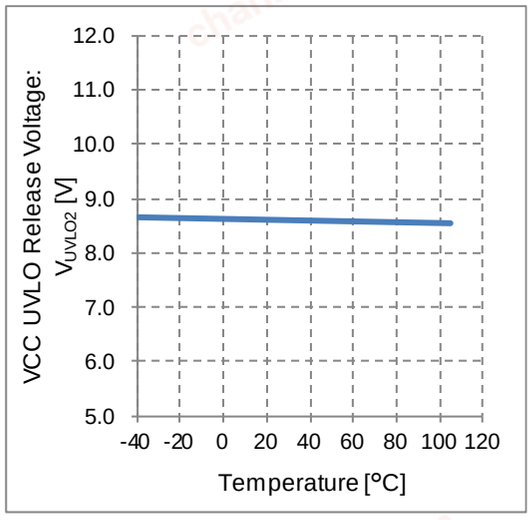


Figure 25. VCC UVLO Release Voltage vs Temperature

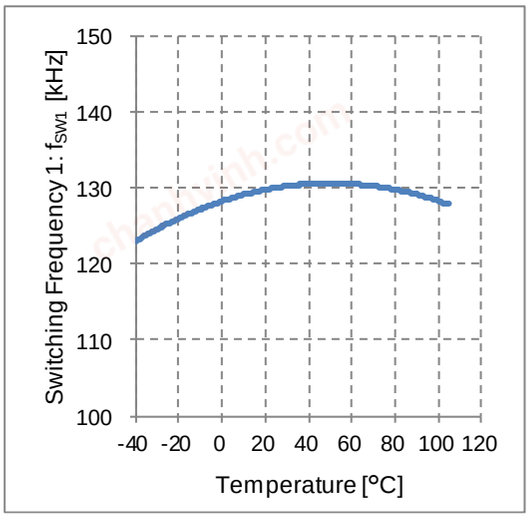


Figure 26. Switching Frequency 1 vs Temperature

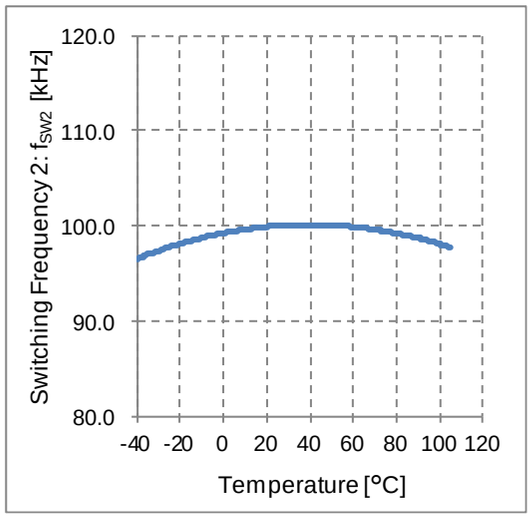


Figure 27. Switching Frequency 2 vs Temperature

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Typical Performance Curves – continued
(Reference Data)

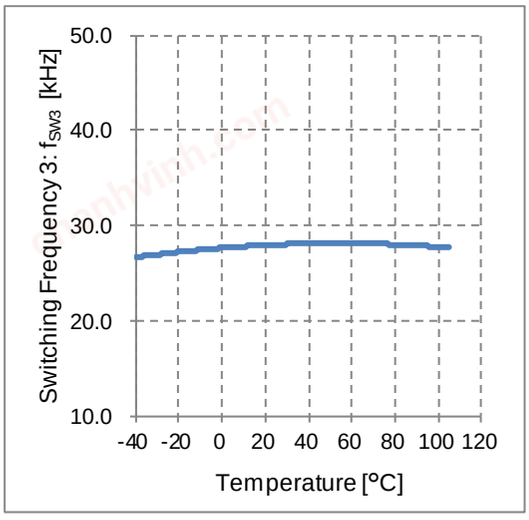


Figure 28. Switching Frequency 3 vs Temperature

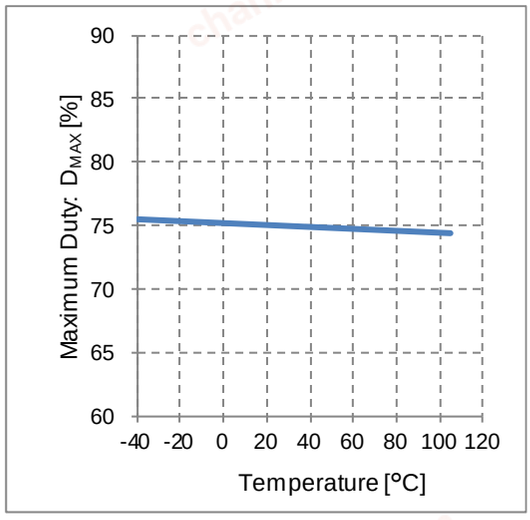


Figure 29. Maximum Duty vs Temperature

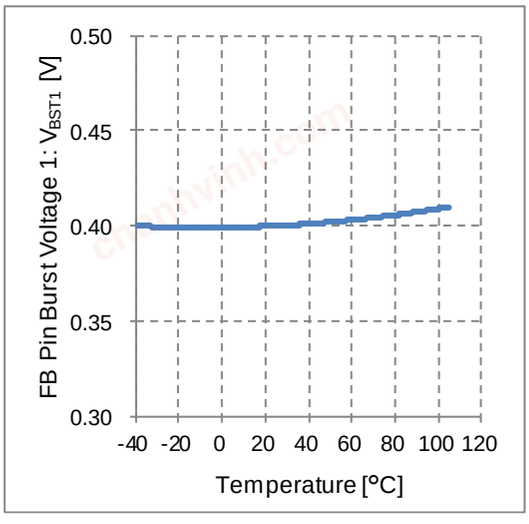


Figure 30. FB Pin Burst Voltage 1 vs Temperature

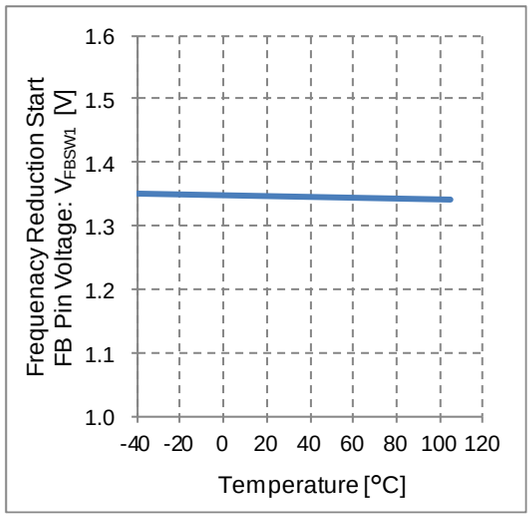


Figure 31. Frequency Reduction Start
FB Pin Voltage vs Temperature

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Typical Performance Curves – continued
(Reference Data)

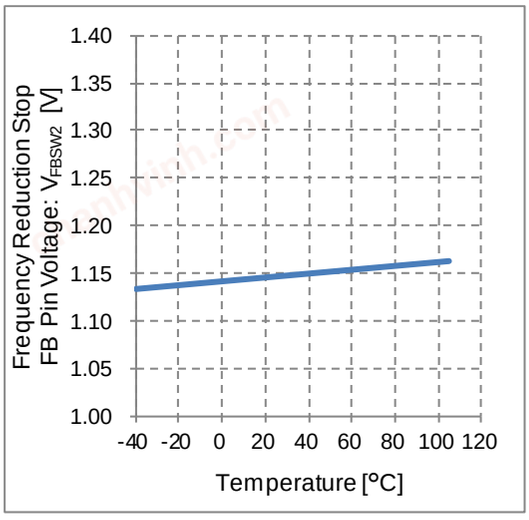


Figure 32. Frequency Reduction Stop FB Pin Voltage vs Temperature

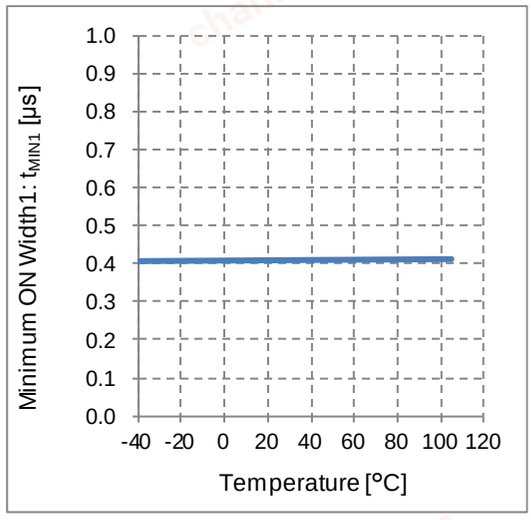


Figure 33. Minimum ON Width 1 vs Temperature

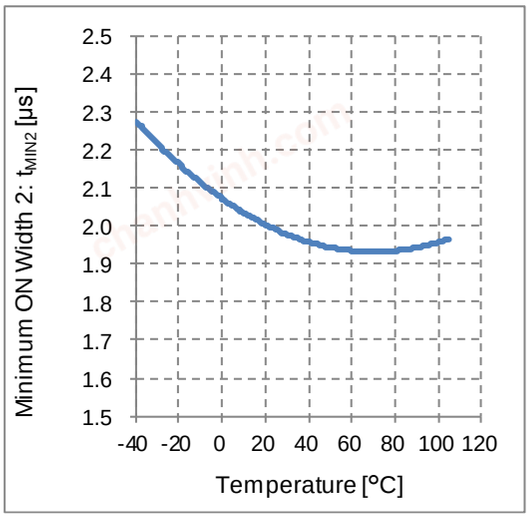


Figure 34. Minimum ON Width 2 vs Temperature

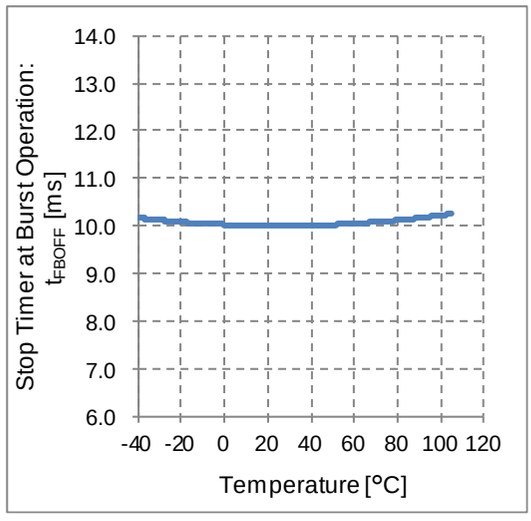


Figure 35. Stop Timer at Burst Operation vs Temperature

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Typical Performance Curves – continued
(Reference Data)

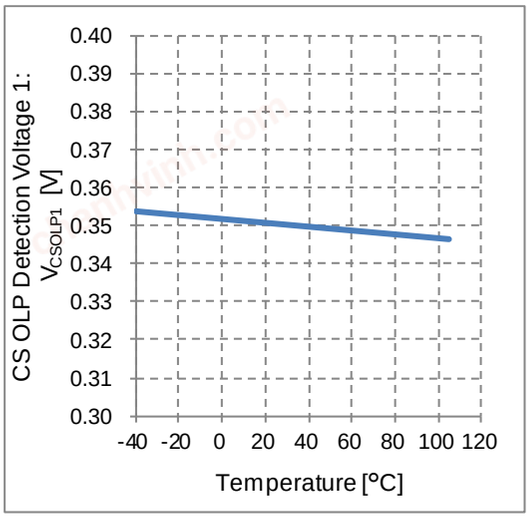


Figure 36. CS OLP Detection Voltage 1 vs Temperature

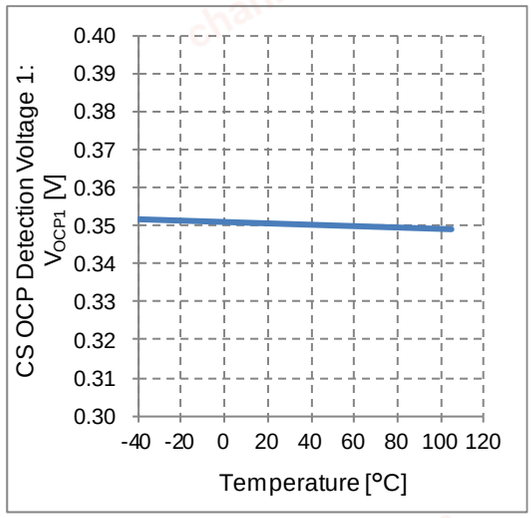


Figure 37. CS OCP Detection Voltage 1 vs Temperature

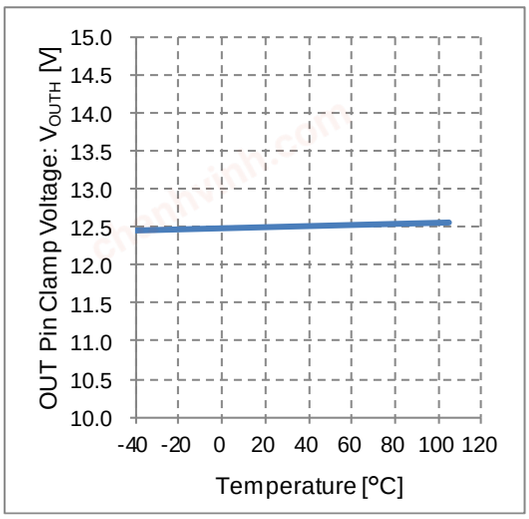
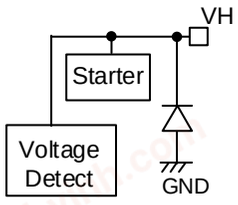
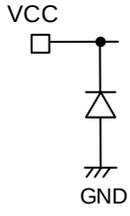
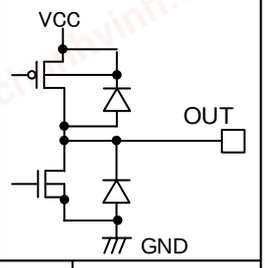
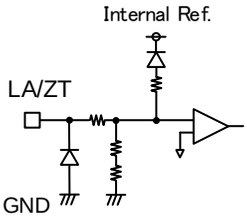
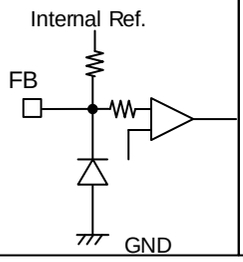
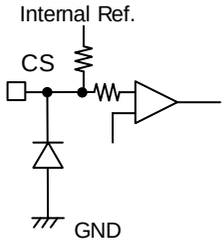
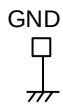


Figure 38. OUT Pin Clamp Voltage vs Temperature

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I/O Equivalence Circuit

7	VH	-	-	6	VCC	5	OUT
		-					
1	LA/ZT	2	FB	3	CS	4	GND
							

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

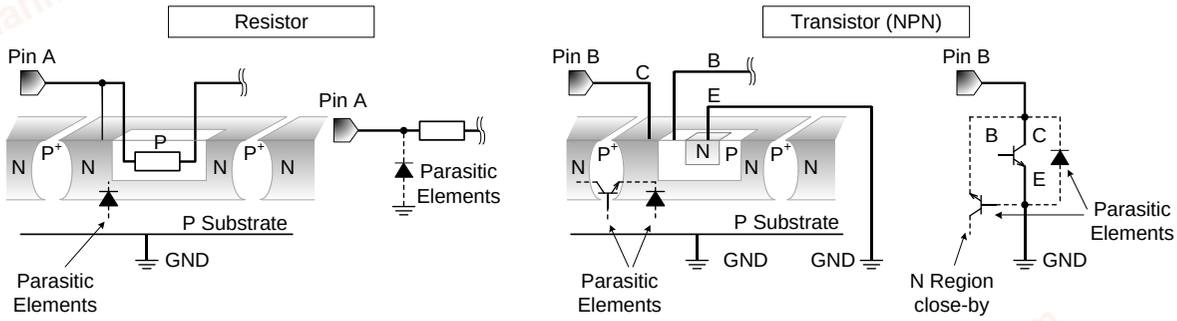


Figure 39. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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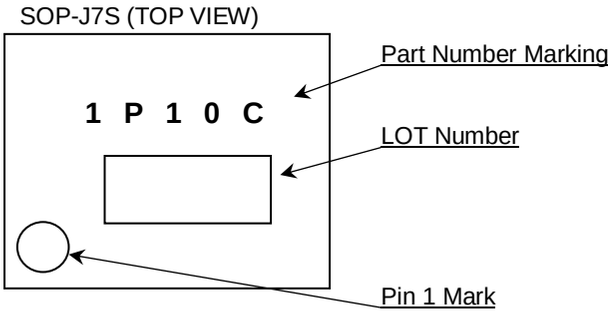
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Ordering Information

B	M	1	P	1	0	C	F	J	-	E 2

Packing and forming specification
E2: Embossed tape and reel

Marking Diagram

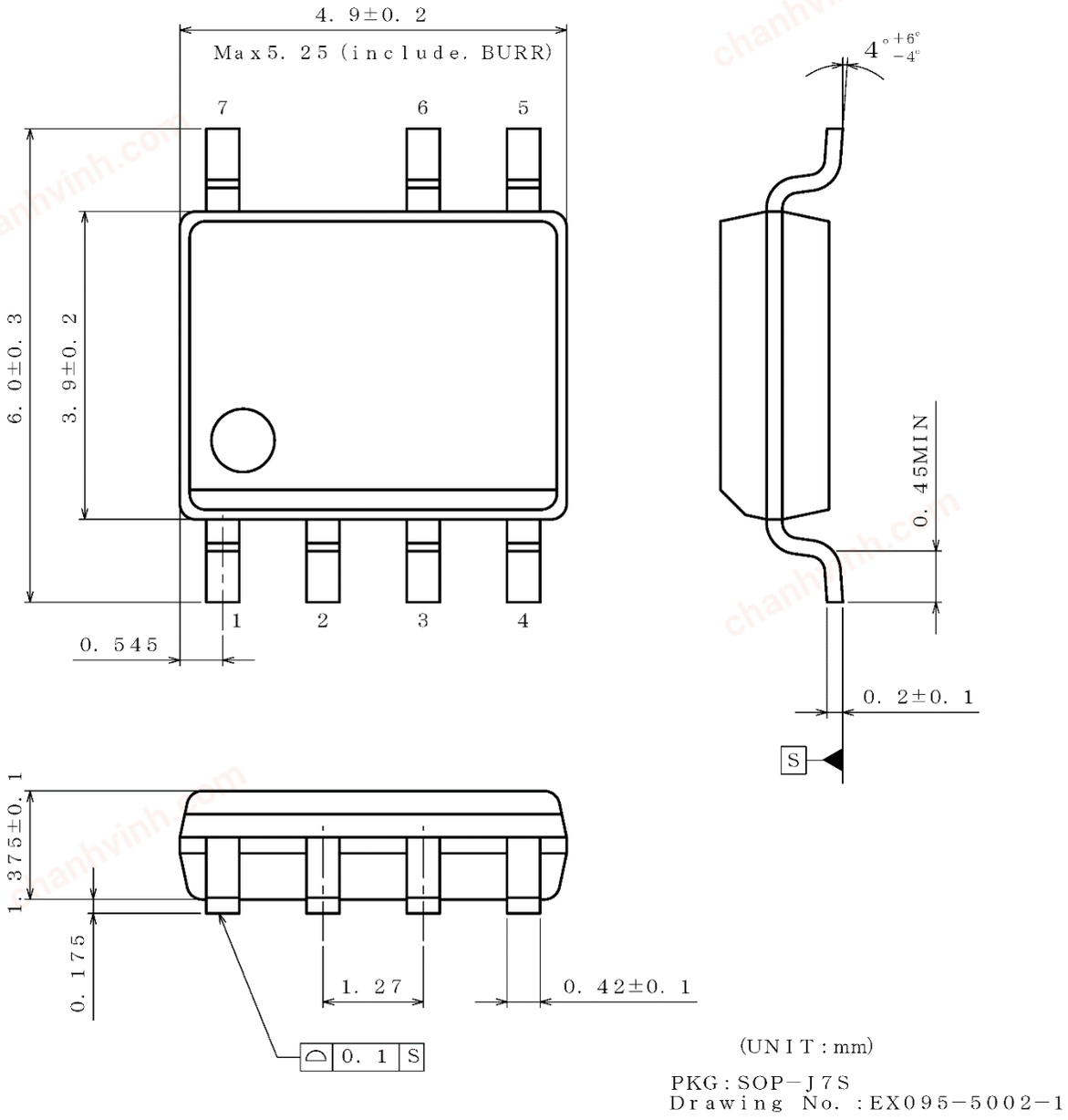


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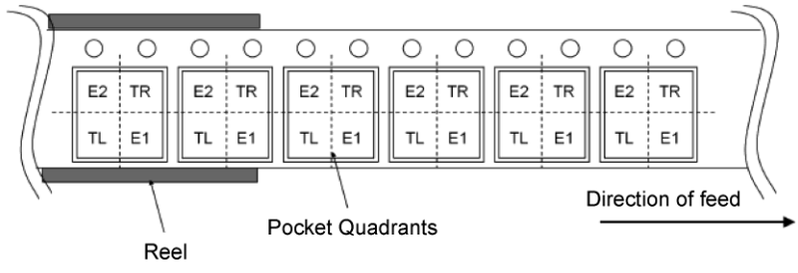
Physical Dimension and Packing Information

Package Name	SOP-J7S



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Rev.	Changes
03.Feb.2020	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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