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Datasheet

16V to 60V, 1A 1ch 2.1MHz Synchronous Buck Converter Integrated FET

BD9V101MUF-LB

General Description

This is the product guarantees long time support in Industrial market.

BD9V101MUF-LB is a current mode synchronous buck converter integrating high voltage rating POWER MOSFETs. The wide range input 16V to 60V and very short minimum pulse width down to 20ns enables direct conversion from 60V power supply to 3.3V at 2.1MHz operation by Nano Pulse Control™.

Key Specifications

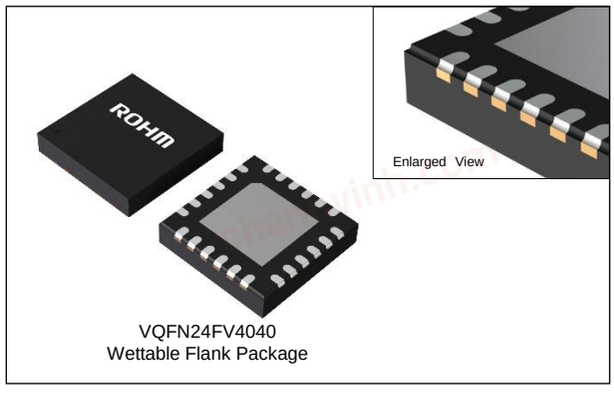
- Input Voltage Range: 16V to 60V
- Output Voltage Range: 0.8V to 5.5V
- Output Current: 1A(Max)
- Operating Frequency: 1.9MHz to 2.3MHz
- Reference Voltage Accuracy: ±2%
- Shutdown Circuit Current: 0μA(Typ)
- Operating Junction Temperature Range: -40°C to +150°C

Features

- Nano Pulse Control™ Enables Direct Conversion 60V to 3.3V at 2.1MHz
- Long Time Support Product for Industrial Applications.
- SW Minimum ON Time 20ns(Max)
- Synchronous Switching Regulator Integrating POWER MOSFETs
- Soft Start Function
- Current Mode Control
- Over Current Protection
- Input Under Voltage Lock Out Protection
- Input Over Voltage Lock Out Protection
- Thermal Shutdown Protection
- Output Over Voltage Protection
- Short Circuit Protection
- Wettable Flank QFN Package

Package

	W(Typ) x D(Typ) x H(Max)
VQFN24FV4040	4.00mm x 4.00mm x 1.00mm



VQFN24FV4040
Wettable Flank Package

Applications

- Industrial Equipment
- Consumer Supplies

Typical Application Circuit

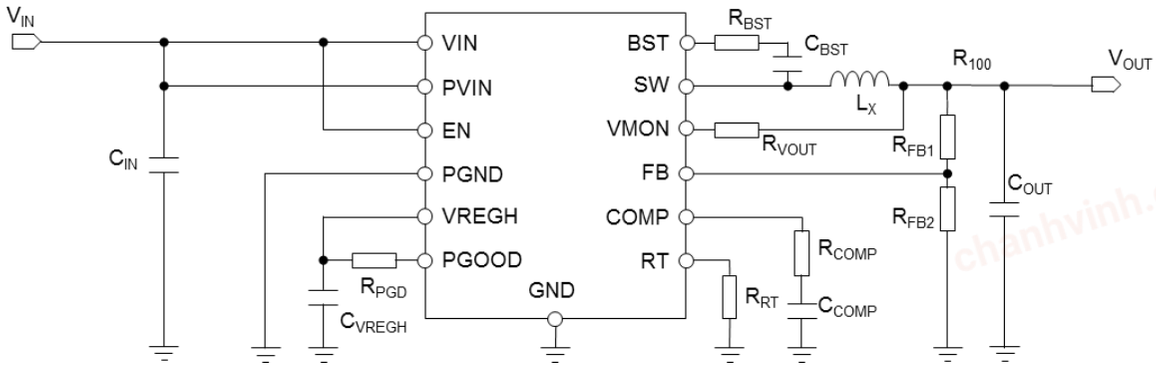


Figure 1. Application Circuit

Nano Pulse Control™ is a trademark of ROHM Co., Ltd.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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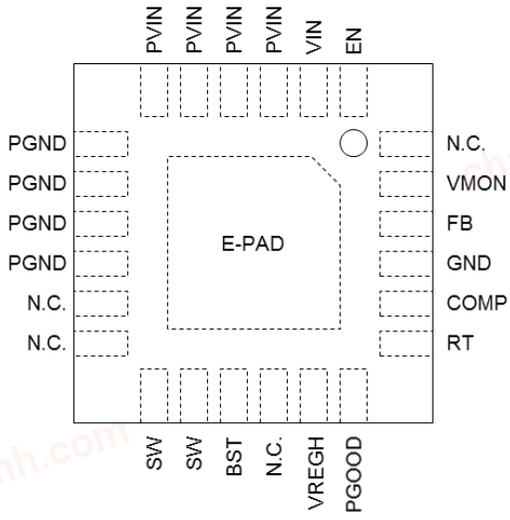
Pin Configuration



(TOP VIEW)
Figure 2. Figure of Terminal Placement

Pin Description

Pin No.	Pin Name	Function
1	EN	Enable pin. Apply Low-level (0.8V or lower) to turn this device off. Apply High-level (2.5V or higher) to turn this device on.
2	VIN	Power supply input pin of the internal circuitry. Connect this pin to PVIN.
3 to 6	PVIN	Power supply input pins that are used for the output stage of the switching regulator. Connecting input ceramic capacitors with values of 2.2µF and 0.1µF to this pin is recommended.
7 to 10	PGND	Power GND input pins.
11,12	N.C.	No connection pins. Leave these pins open, or connect PGND pin.
13,14	SW	Switching node pins. These pins are connected to the source of the internal the Top POWER MOSFET and the drain of the internal Bottom side POWER MOSFET. Connect the power inductor and the bootstrap capacitor 0.022µF and resistor 3.3Ω to these pins.
15	BST	Power supply pin of the internal the Top POWER MOSFET. Connect a 3.3Ω resistor to this pin in series with a 0.022µF bootstrap capacitor connected to SW pin. This capacitor's voltage becomes the power supply of the Top POWER MOSFET gate driver.
16	N.C.	No connection pin. Leave this pin open.
17	VREGH	Internal power supply output pin. This node supplies power 5V(Typ) to other blocks which are mainly responsible for the control function of the switching regulator. Connect a ceramic capacitor with value of 2.2µF to ground.
18	PGOOD	Power Good pin. This pin is in open drain configuration so pull-up resistor is needed to turn it HIGH or LOW.
19	RT	This pin is used for setting the switching frequency. Connect a frequency setting resistor between this pin and GND pin.
20	COMP	Output of the gm error amplifier, and the input of PWM comparator. Connect phase compensation components to this pin. See page 23 on calculate the resistance and capacitance of phase compensation.
21	GND	Ground pin.
22	FB	V_{OUT} voltage feedback pin. Inverting input node for the gm error amplifier. Connect output voltage divider to this pin to set the output voltage. See page 22 on how to compute for the resistor values.
23	VMON	Short Circuit Protection threshold detect pin. This node is monitoring the output voltage and discharging it during shutdown.
24	N.C.	No connection pin. Leave this pin open.
-	E-PAD	Exposed pad. Connect this pad to the internal PCB ground plane using multiple via holes to obtain excellent heat dissipation characteristics.

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Block Diagram

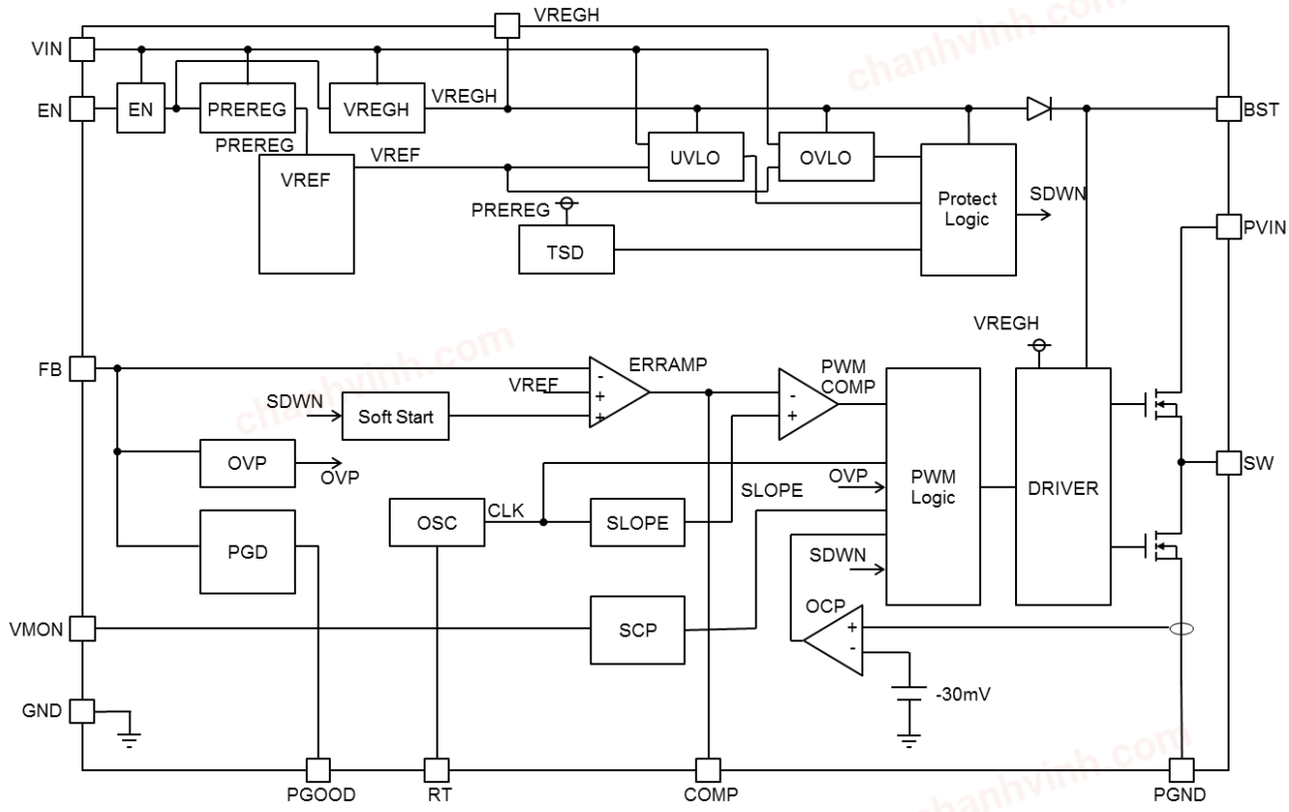

Figure 3. Block Diagram

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Description of Blocks

- ERRAMP
  The ERRAMP block is an error amplifier and its inputs are the reference voltage 0.8V(Typ) and the FB pin voltage. The duty of switching pulse is controlled by ERRAMP output COMP. Set output voltage with FB pin. Moreover, the external resistor and capacitor are required to COMP pin as phase compensation circuit (refer to Selection of the Phase Compensation Circuit R_{COMP}, C_{COMP} on page 23).

- Soft Start
  The Soft Start block prevents the overshoot of the output voltage by gradually increasing the input of the error amplifier when the power supply turns ON to gradually increase the switching duty cycle. The soft start time is set to 1.1ms (f_{SW}=2.1MHz). The soft start time can be changed by adjusting the oscillating frequency (refer to Soft Start Time on page 24).

- EN
  This IC is in normal operation when the voltage at EN terminal is 2.5V or more. The IC will be shutdown when the voltage at EN terminal becomes open or 0.8V or less.

- VREGH
  This block outputs a regulated 5V(Typ) and supplies it to different blocks in the chip. Connect 2.2µF ceramic capacitor to GND.

- OSC (Oscillator)
  This circuit generates a clock signal that determines converter switching frequency which is 1.9MHz to 2.3MHz. The frequency of the clock can be set by a resistor connected between the RT pin and the GND pin (refer to page 24 Figure 38). The OSC output send the clock signal to PWM Logic. This clock is also used to set the Soft Start time and Protect block counter.

- SLOPE
  This block generates a sawtooth waveform from OSC clock. The inductor current feedback is added to the sawtooth signal.

- PWM COMP
  This block modulates duty cycle by comparing the COMP pin voltage and the sawtooth signal from the SLOPE block.

- PWM Logic
  The PWM Logic block controls the POWER MOSFETs ON and OFF timings. In normal operation, the clock signal from OSC block determines the Top POWER MOSFET ON timing, and the PWM COMP block output determines the OFF timing. In addition, each protection output signal is passed to the PWM Logic and it controls proper protection functions.

- TSD (Thermal Shutdown)
  This block is a thermal shutdown circuit. Both of the output MOSFETs are turned OFF and the VREGH is stopped to prevent thermal damage or a thermal-runaway of the IC when the chip temperature reaches to approximately 175°C(Typ) or more, and the operation comes back when the chip temperature comes down to 150°C(Typ) or less. Note that the thermal shutdown circuit is intended to prevent destruction of the IC itself. Therefore, it is highly recommended to keep the IC temperature always within the operating temperature range. Operation above operating temperature range will reduce the lifetime of the IC.

- OCP (Over Current Protection)
  While the Bottom POWER MOSFET is ON, if the voltage between the drain and source exceeds the reference voltage which is internally set within IC, OCP will activate. This protection is a self-return type. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected).

- OVP (Over Voltage Protection)
  This is the output over voltage protection circuit. When the output becomes 120%(Typ) or more of the target voltage, both of the output MOSFETs are turned OFF and the regulator operation is stopped. When the output voltage becomes 110%(Typ) or less of the target voltage, it returns to normal operation.

- UVLO (Under Voltage Lock-Out)
  UVLO is a protection circuit that prevents low voltage malfunction, especially during power up and down. It monitors the V_{IN} power supply voltage. If V_{IN} becomes 15.0V(Max) or less, both of the output MOSFETs are turned OFF and the regulator operation is stopped. When the input voltage becomes 16.0V(Max) or more, the regulator restarts the operation with Soft Start.

- DRIVER
  This circuit drives the gate of the output POWER MOSFETs.

- OVLO (Over Voltage Lock-Out)
  This is the input over voltage protection circuit. When the input voltage becomes 60.0V(Min) or more, the regulator is shutdown. When the input voltage becomes 59.0V(Min) or less the falling threshold, the regulator restarts the operation with SOFT START. This hysteresis is 1.0V(Typ).

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Description of Blocks - continued

- PGD
  The PGOOD circuit is a reference voltage monitoring circuit. The PGOOD pin sets to Hi-Z when the FB voltage is 90%(Typ) or more and 110%(Typ) or less of reference voltage, otherwise the PGOOD pin is pulled down to GND. PGOOD detection has a hysteresis of 20mV(Typ) for each of the upper and lower thresholds.

- SCP (Short Circuit Protection)
  The short circuit protection circuit. Depending on the level of the VIN terminal voltage and VMON terminal voltage, a reference pulse signal with varying ON time will be produced. If the SW ON time exceeds 2.5times(Typ) the ON time of this reference pulse signal for 2clk cycles, short circuit protection will be activated. Then the Top and Bottom POWER MOSFETs will be turned OFF.

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Absolute Maximum Ratings (Tj=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}, PV_{IN}	-0.3 to +70	V
EN Input Voltage	V_{EN}	-0.3 to V_{IN}	V
BST Voltage	V_{BST}	-0.3 to +70	V
Voltage from SW to BST	ΔV_{BST}	V_{SW} -0.3 to V_{SW} + 7	V
FB, RT, COMP, PGOOD Input Voltage	V_{FB}, V_{RT}, V_{COMP}, V_{PGOOD}	-0.3 to +7	V
VMON Input Voltage	V_{VMON}	-0.3 to +7	V
VREGH Input Voltage	V_{VREGH}	-0.3 to +7	V
Storage Temperature Range	Tstg	-55 to +150	˚C
Maximum Junction Temperature	Tjmax	150	˚C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance(Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN24FV4040				
Junction to Ambient	θ_{JA}	150.6	37.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	20	9	°C/W

(Note 1) Based on JESD51-2A (Still-Air)

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{IN}	16	-	60	V
Operating Junction Temperature	Tjopr	-40	-	+150	˚C
Output Voltage	V_{OUT}	0.8	-	5.5	V
SW Minimum ON Time(Note 1)	t_{ONMIN}	-	9	20	ns
Output Current	I_{OUT}	0	-	1	A
Switching Frequency	f_{SW}	1.9	2.1	2.3	MHz
Input Capacitor(Note 2)	C_{IN}	1.2	-	-	µF
Switching Frequency Setting Resistor	R_{RT}	6.9	7.5	8.1	kΩ

(Note 1) This parameter is for 0.5A output. Not 100% tested.
(Note 2) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be larger than minimum value (Refer to Selection of Input Capacitor CIN, CBLK on page 22). Also, the IC might not function properly when the PCB layout or the position of the capacitor is not good. Please check PCB Layout Design on page 30.

Electrical Characteristics (Unless otherwise specified Tj=25˚C, V_{IN}=48V, V_{EN}=5V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Shutdown Circuit Current	I_{SDN}	-	0	5	µA	V_{EN}=0V, Tj=105˚C
Circuit Current	I_{CC}	-	2.5	3.8	mA	V_{FB}=2.0V
Reference Voltage	V_{FB}	0.784	0.800	0.816	V	V_{FB}=V_{COMP}
FB Input Current	I_{FB}	-1	0	+1	µA	V_{FB}=5.0V
COMP Pin Sink Current	I_{CPSINK}	35	60	85	µA	V_{COMP}=1.0V, V_{FB}=2V
COMP Pin Source Current	$I_{CPSOURCE}$	-85	-60	-35	µA	V_{COMP}=1.0V, V_{FB}=0V
Soft Start Time(Note1)	t_{SS}	0.7	1.1	1.5	ms	f_{SW}=2.1MHz, R_{RT}=7.5kΩ
Top Power NMOS ON Resistance	R_{ONH}	-	600	900	mΩ	I_{OUT}=-50mA
Bottom Power NMOS ON Resistance	R_{ONL}	-	400	600	mΩ	I_{OUT}=50mA
Output Leak Current H	I_{OLEAKH}	-5	0	+5	µA	V_{IN}=70V, V_{EN}=0V Tj=105˚C, V_{SW}=0V
Output Leak Current L	I_{OLEAKL}	-5	0	+5	µA	V_{IN}=70V, V_{EN}=0V Tj=105˚C, V_{SW}=70V
Operating Output Switch Current of Overcurrent Protection	I_{SW}	1.5	2.4	3.3	A	
Oscillating Frequency	f_{SW}	1.9	2.1	2.3	MHz	R_{RT}=7.5kΩ
EN Threshold Voltage H	V_{ENH}	2.5	-	V_{IN}	V	
EN Threshold Voltage L	V_{ENL}	0	-	0.8	V	
EN Input Current	I_{EN}	-	8.5	20	µA	V_{EN}=5V
VIN Under Voltage Protection Detection Voltage	V_{UV_ON}	12.5	13.7	15.0	V	V_{IN} Falling
VIN Under Voltage Protection Return Voltage	V_{UV_OFF}	13.5	14.7	16.0	V	V_{IN} Rising
VIN Over Voltage Protection Detection Voltage	V_{OV_ON}	60.0	62.5	65.0	V	V_{IN} Rising
VIN Over Voltage Protection Return Voltage	V_{OV_OFF}	59.0	61.5	64.0	V	V_{IN} Falling
OVP Threshold Voltage H	V_{OVPH}	0.87	0.96	1.05	V	V_{FB} Rising
OVP Threshold Voltage L	V_{OVPL}	0.83	0.92	1.01	V	V_{FB} Falling
PGOOD L Threshold	V_{PGDL}	V_{FB} x 0.82	V_{FB} x 0.90	V_{FB} x 0.98	V	V_{FB} Falling
PGOOD L Hysteresis	V_{PGDLH}	4	20	40	mV	
PGOOD H Threshold	V_{PGDH}	V_{FB} x 1.02	V_{FB} x 1.10	V_{FB} x 1.18	V	V_{FB} Rising
PGOOD H Hysteresis	V_{PGDHL}	-40	-20	-4	mV	
PGOOD ON Resistance	R_{PGD}	-	0.22	1	kΩ	I_{PGOOD}=10mA
PGOOD Leak Current	I_{PGD}	-	0	1	µA	V_{PGOOD}=5V

(Note 1) V_{FB} transient time from 0.1V to 0.7V.
(Note 2) Not 100% tested.

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Typical Performance Curves

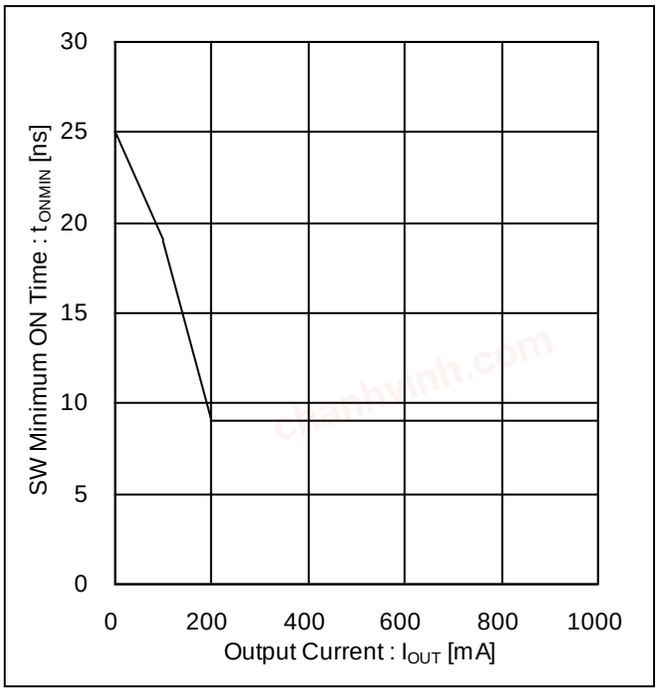

Figure 4. SW Minimum ON Time vs Output Current

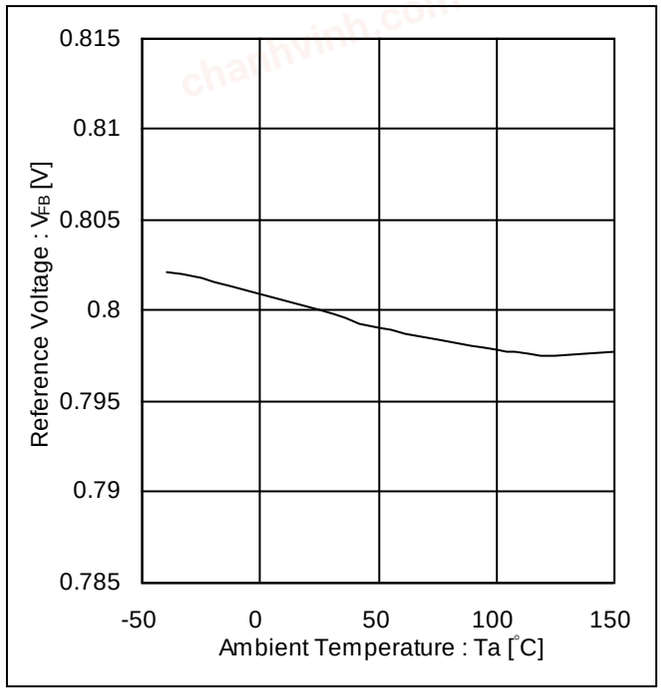

Figure 5. Reference Voltage vs Ambient Temperature

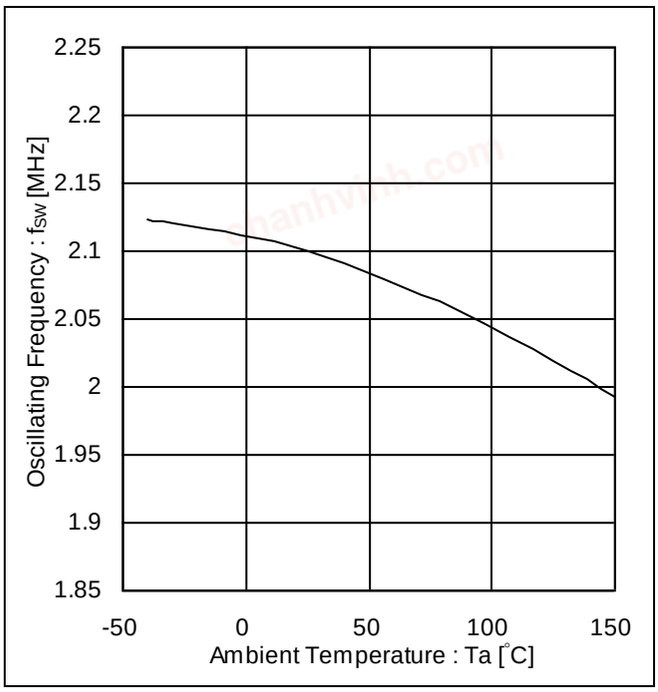

Figure 6. Oscillating Frequency vs Ambient Temperature

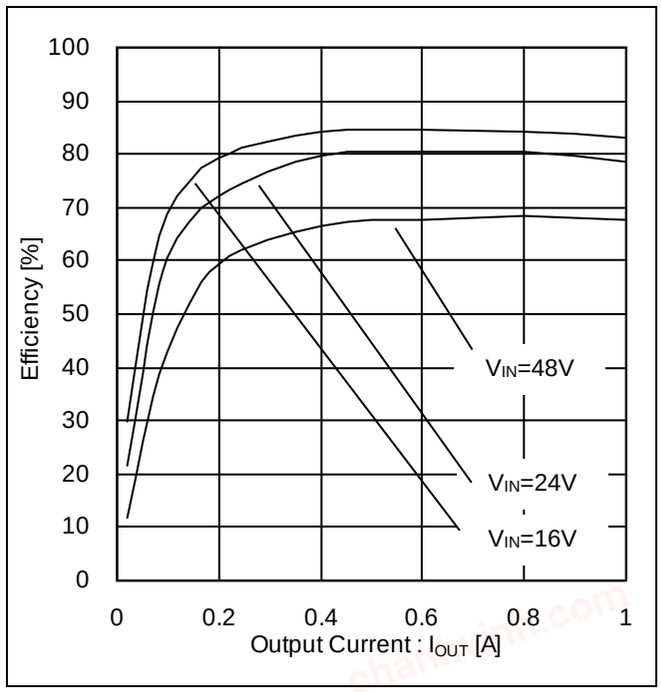

Figure 7. Efficiency vs Output Current
(V_{OUT}=5.5V, f_{SW}=1.9MHz)

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Typical Performance Curves - continued

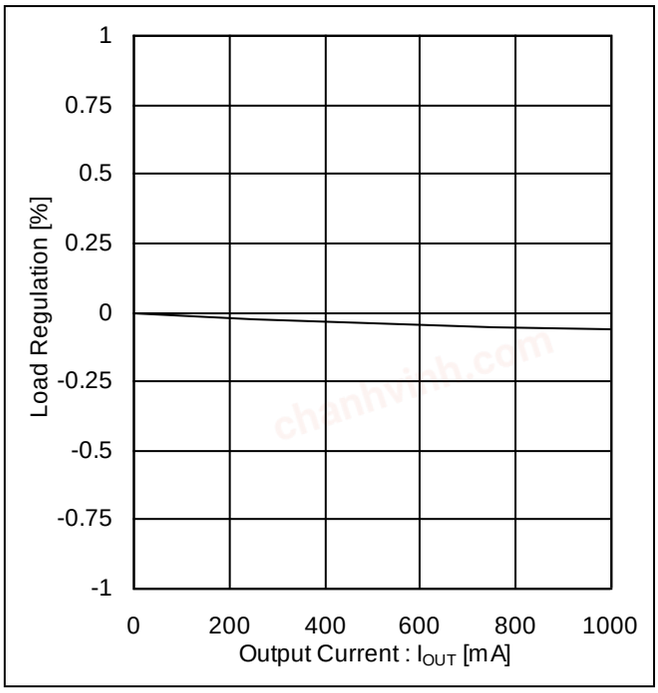

Figure 8. Load Regulation
(V_{IN}=48V, V_{OUT}=5V)

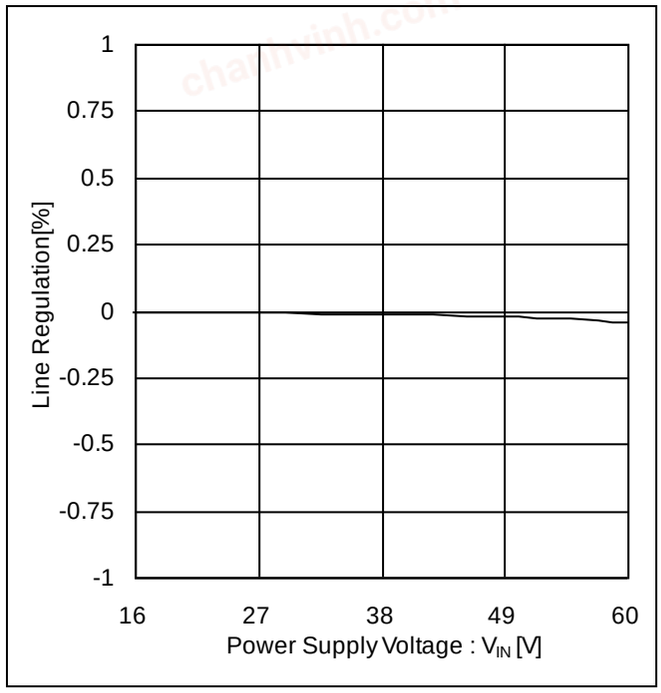

Figure 9. Line Regulation
(V_{OUT}=5V, I_{OUT}=500mA)

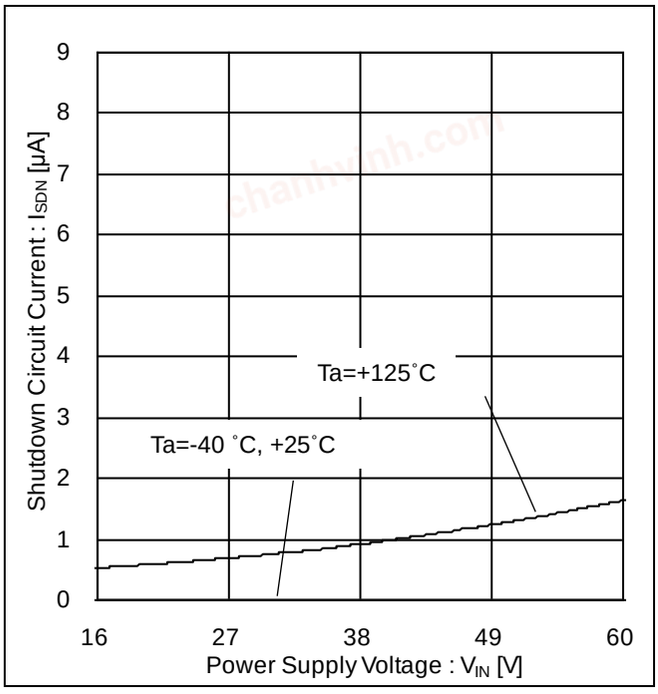

Figure 10. Shutdown Circuit Current vs Power Supply Voltage (V_{EN}=0V)

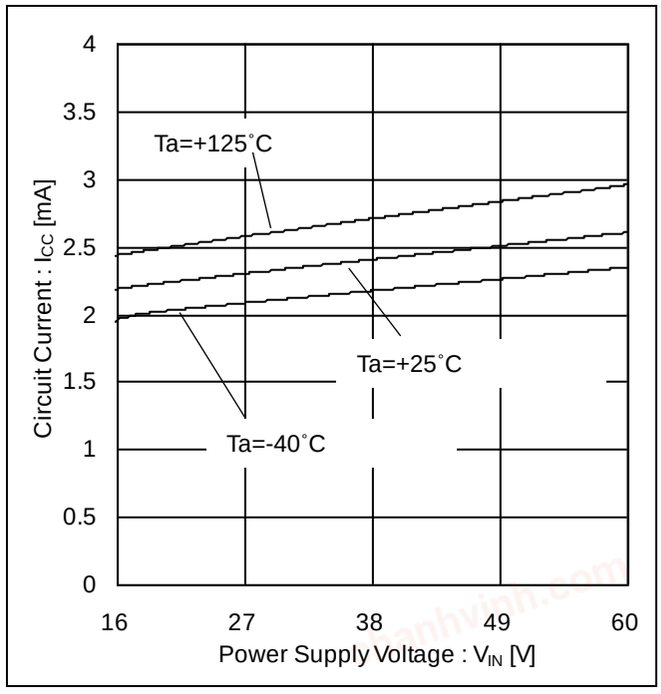

Figure 11. Circuit Current vs Power Supply Voltage
(V_{EN}=V_{IN}, No Switching)

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Typical Performance Curves - continued

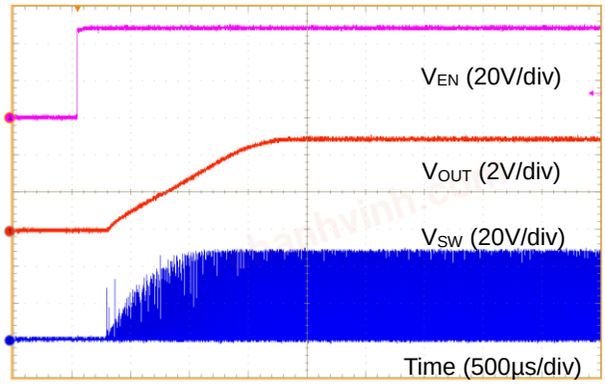

Figure 12. Startup Waveform
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0.5A)

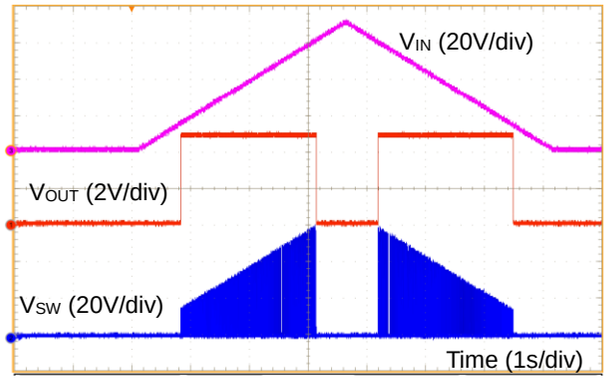

Figure 13. Startup and Shutdown Waveform
(V_{IN}=0V ↔ 70V, V_{OUT}=5V, I_{OUT}=0.5A)

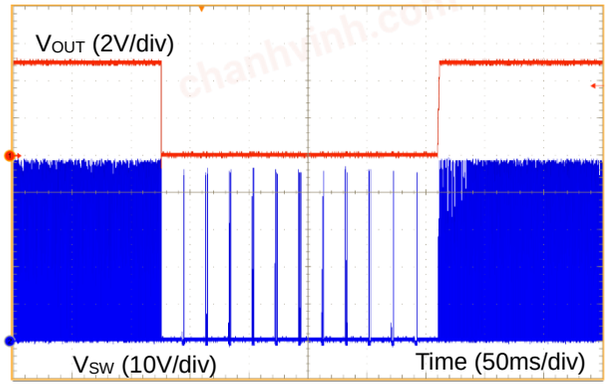

Figure 14. V_{OUT} Short and Release Waveform
(V_{IN}=48V)

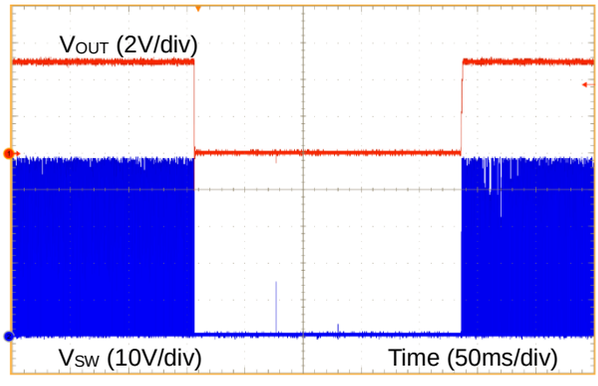

Figure 15. SW Short and Release Waveform
(V_{IN}=48V)

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Typical Performance Curves - continued

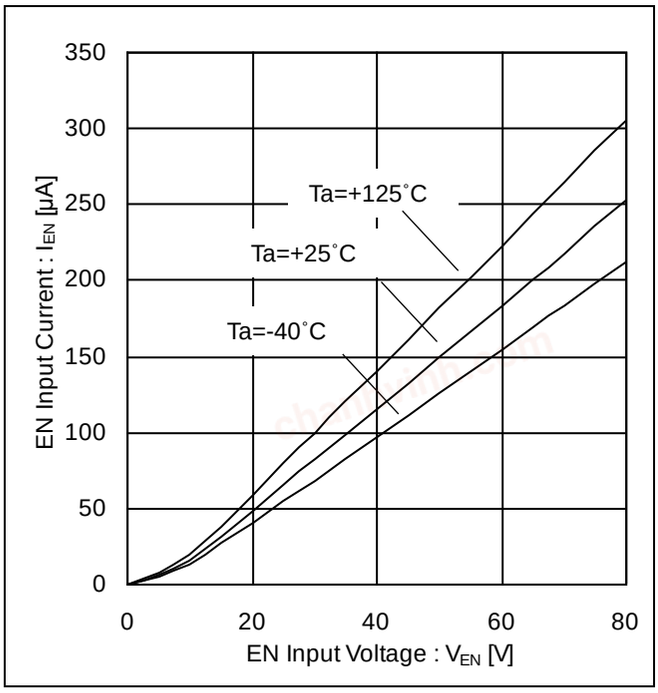

Figure 16. EN Input Current vs EN Input Voltage

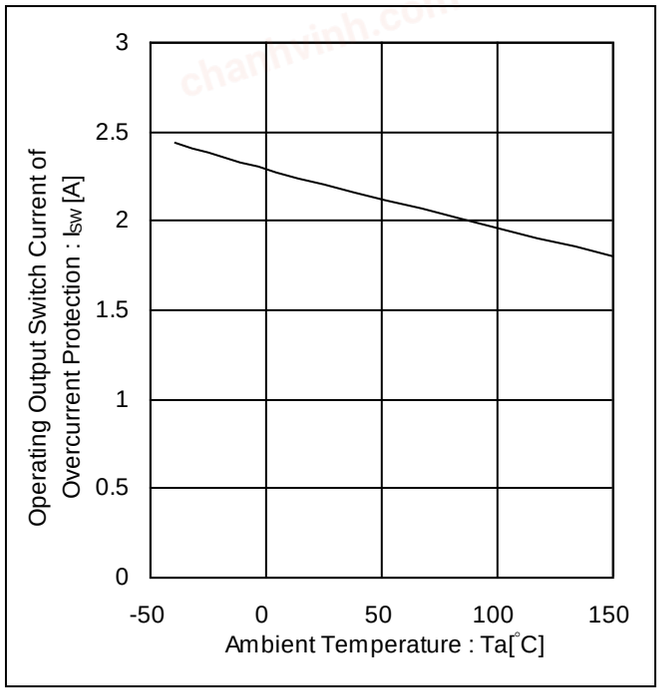

Figure 17. Operating Output Switching Current of Over Current Protection vs Ambient Temperature (V_{IN}=48V, V_{OUT}=5V)

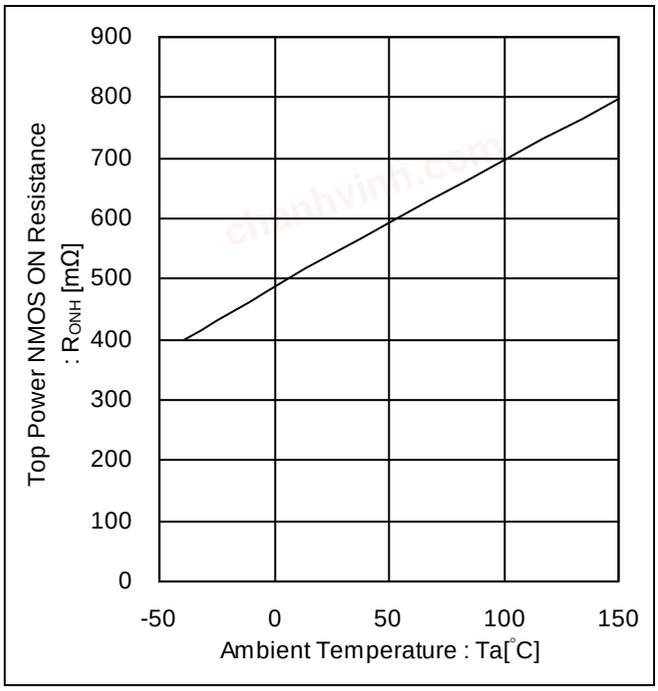

Figure 18. Top Power NMOS ON Resistance vs Ambient Temperature

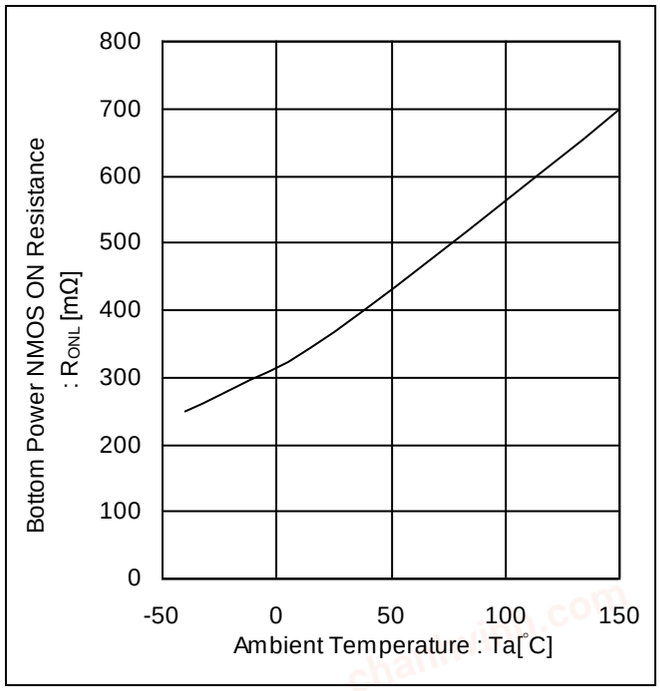

Figure 19. Bottom Power NMOS ON Resistance vs Ambient Temperature

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Typical Performance Curves - continued

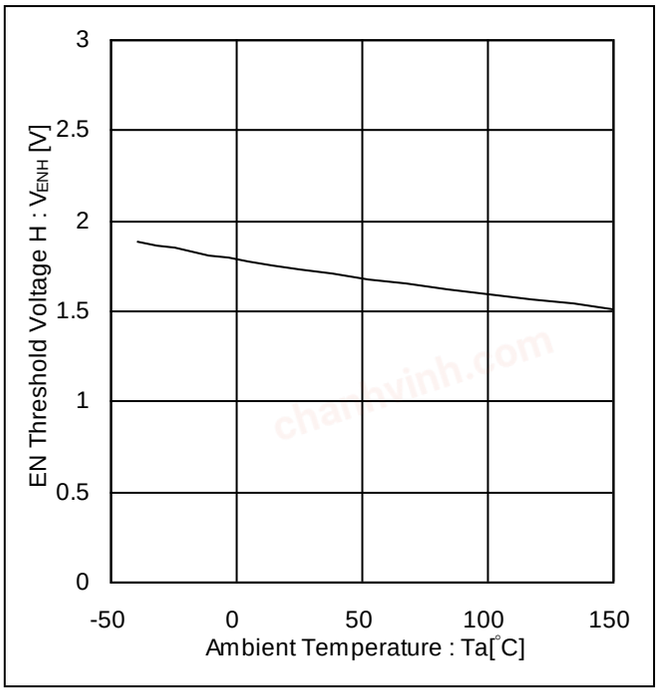

Figure 20. EN Threshold Voltage H vs Ambient Temperature
(V_{IN}=48V, V_{OUT}=5V)

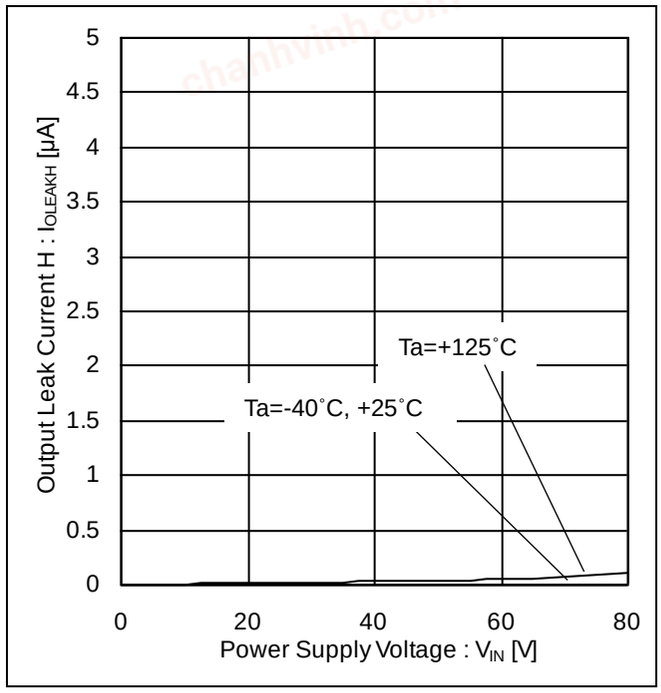

Figure 21. Output Leak Current H vs Power Supply Voltage
(EN=0V, SW=V_{IN})

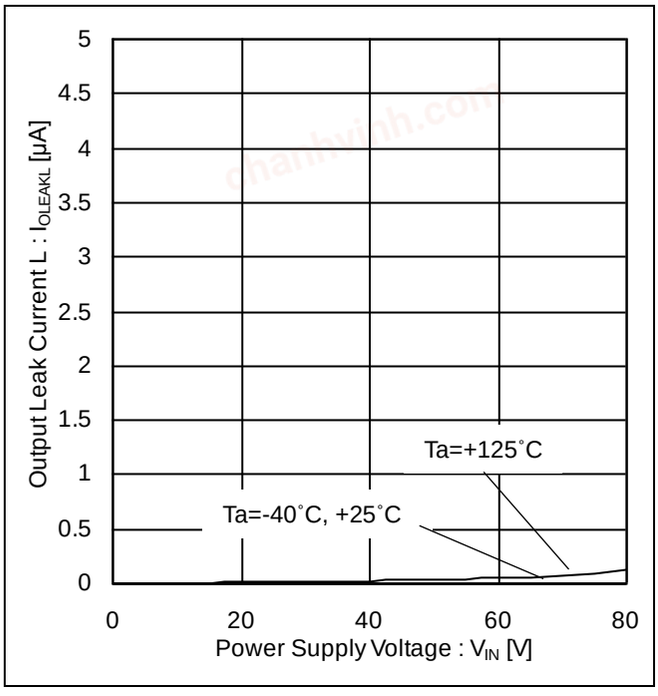

Figure 22. Output Leak Current L vs Power Supply Voltage
(EN=0V, SW=GND)

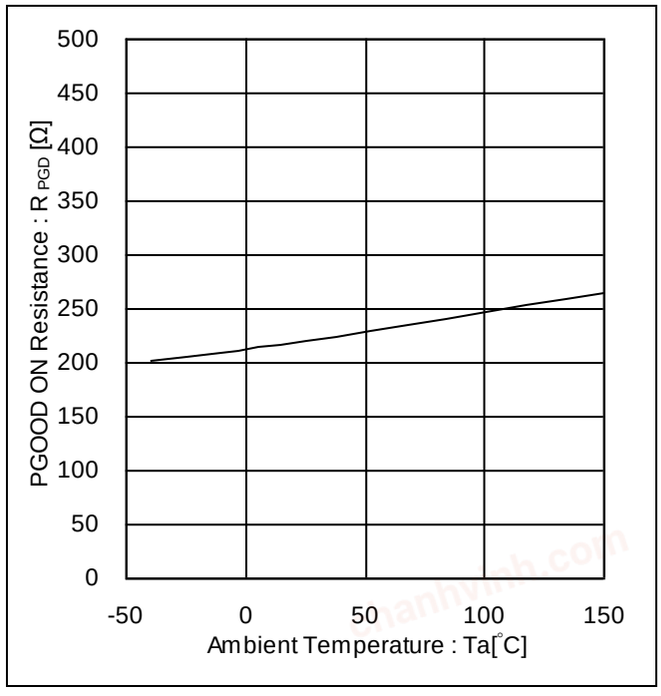

Figure 23. PGOOD ON Resistance vs Ambient Temperature

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Function Explanation

1. Nano Pulse Control™
Nano Pulse Control™ is an original technology developed by ROHM Co., Ltd. It enables to control voltage stably, which is difficult in the conventional technology, even in a narrow SW ON Pulse such as less than 50ns at typical condition. Therefore, high frequency switching operation become possible. BD9V101MUF-LB is designed with 9ns(Typ) Minimum SW ON time for current sense and 2.1MHz(Typ) switching frequency by using this technology.

(1) High V_{IN} Low V_{OUT} Operation
Narrow SW ON Pulse enables direct convert of high output voltage to low output voltage. BD9V101MUF-LB, the output voltage V_{OUT} 3.3V can be output directly from the supply voltage V_{IN} 60V at 2.1MHz.

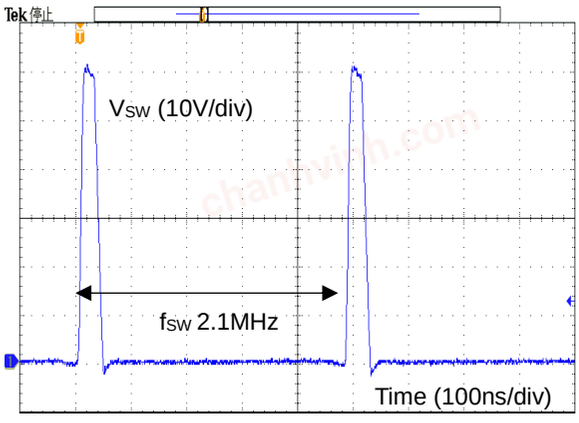

Figure 24. Switching Waveform
(V_{IN}=60V, V_{OUT}=3.3V, I_{OUT}=0.5A, f_{SW}=2.1MHz)

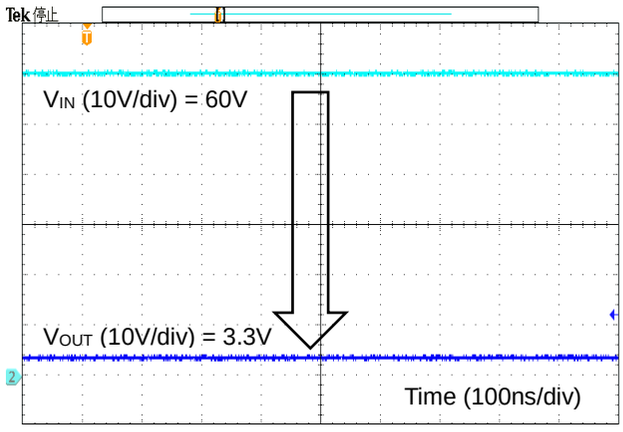

Figure 25. V_{IN} V_{OUT} Waveform
(V_{IN}=60V, V_{OUT}=3.3V, I_{OUT}=0.5A, f_{SW}=2.1MHz)

(2) Stable Startup Waveform
Narrow SW ON Pulse enables stable output waveform even at startup. BD9V101MUF-LB achieves a stable Soft Start operation under wide input voltage conditions.

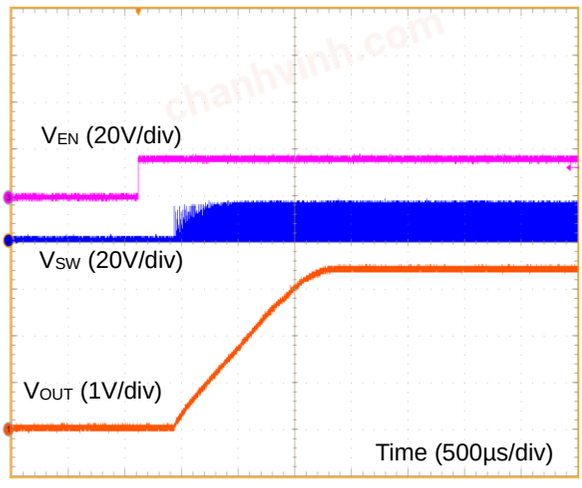

Figure 26. Startup Waveform
(V_{IN}=16V, V_{OUT}=3.3V, I_{OUT}=0.5A, f_{SW}=2.1MHz)

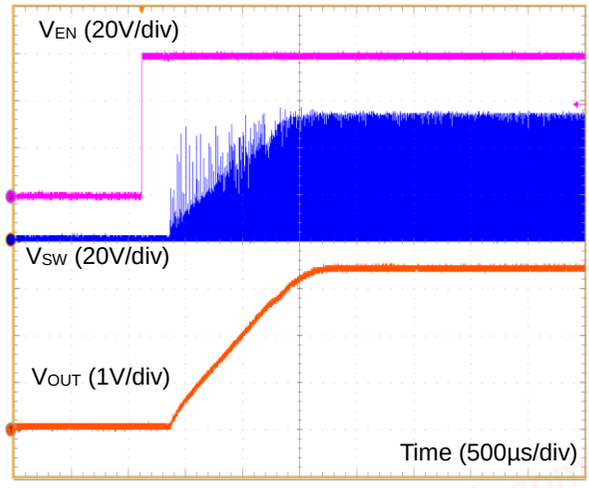

Figure 27. Startup Waveform
(V_{IN}=60V, V_{OUT}=3.3V, I_{OUT}=0.5A, f_{SW}=2.1MHz)

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Function Explanation - continued

2. Enable Operation
Shutdown and startup of the IC can be controlled by the voltage applied to the EN pin. When EN voltage reaches 2.5V(Max) or more, the internal VREGH activates and the IC operates. When an EN voltage become 0.8V(Max) or less, the IC will be shutdown.

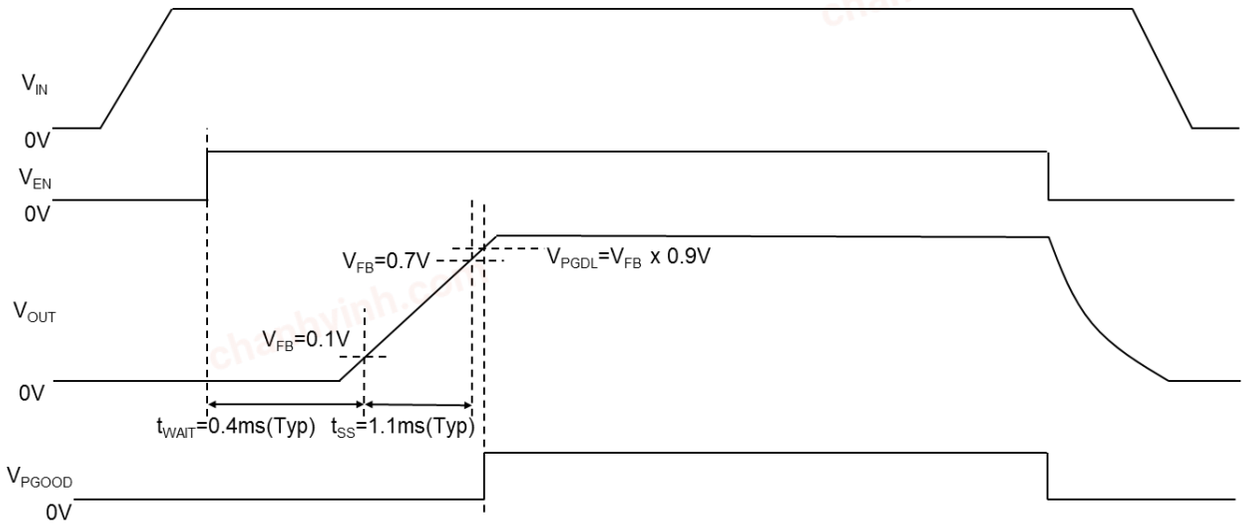

Figure 28. Enable ON/OFF Timing Chart

3. Power Good
When the output voltage is within the voltage range of ±10%(Typ), the PGOOD pin set Hi-Z. When the output voltage is outside the voltage range of ±10%(Typ), the PGOOD pin is pulled down with a built-in MOSFET of 0.22kΩ(Typ). Pull up the PGOOD pin to VREGH with a resistor of about 10kΩ to 100kΩ.

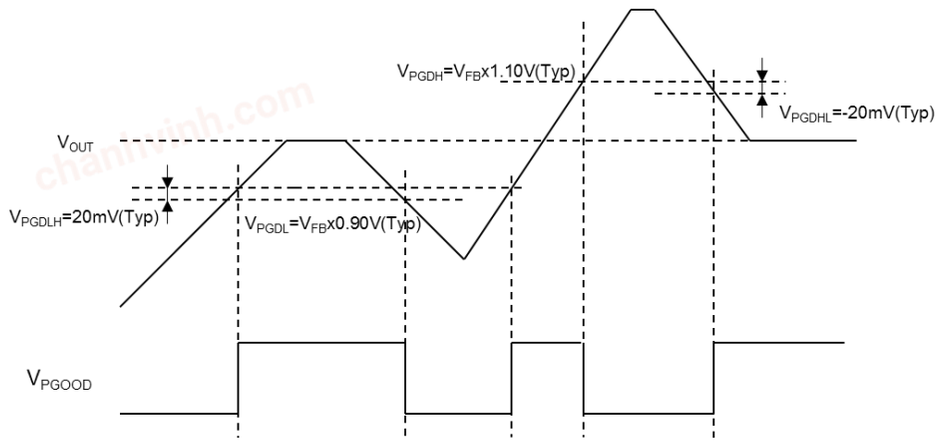

Figure 29. PGOOD Timing Chart

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Protect function

1. Under Voltage Lockout (UVLO)
   Under Voltage Lockout monitors the VIN terminal voltages. When the VIN voltage is at 15.0V(Max) or less, both of the output MOSFETs are turned OFF and the regulator operation is stopped. When the input voltage becomes 16.0V(Max) or more, the regulator restarts the operation with Soft Start.

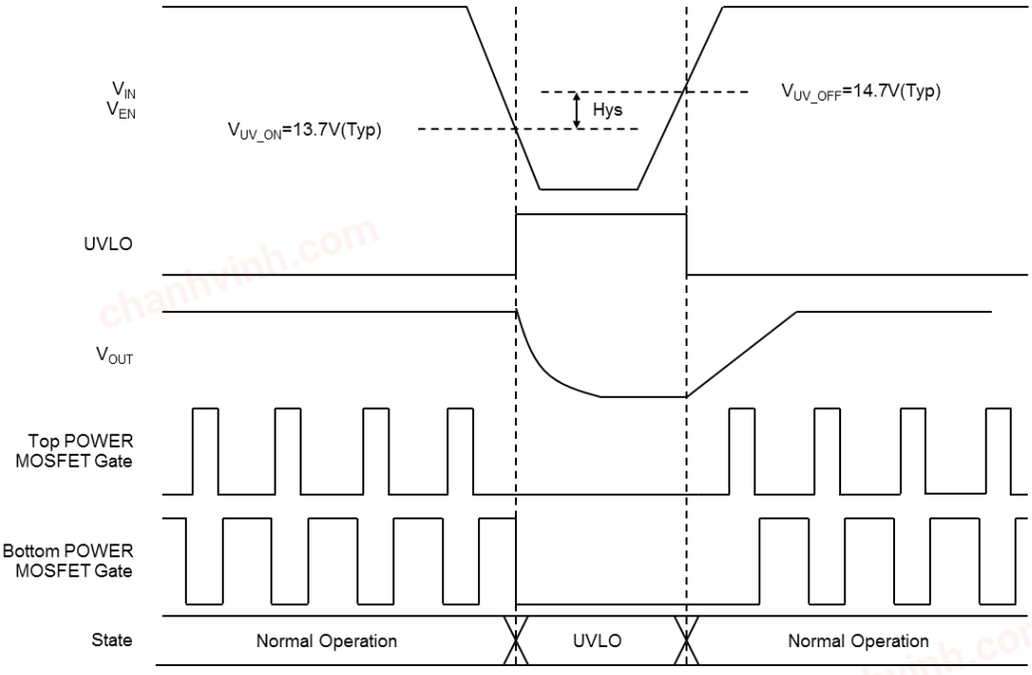

Figure 30. UVLO Timing Chart

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Protect function - continued

2. Short Circuit Protection(SCP)
The Short Circuit Protection function produces a reference pulse that has an ON time derived from V_{IN} and V_{OUT}. This reference pulse's ON time is compared to the SW ON time. If the SW ON time exceeds 2.5times(Typ) of the expected SW ON time, and remains in that state for 2clk (clk = 1/f_{SW}) cycles, it will stop both of the output MOSFETs for 32ms(Typ) and then restarts again. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected).

The assumed SW ON Time is obtained from the following formula:

$$t_{pulse} = \frac{1}{2.1[\mathrm{MHz}]} \times \frac{V_{OUT}}{V_{IN}} \ [\mu s]$$

$$t_{pulse_clamp} = \frac{1}{2.1[\mathrm{MHz}]} \times \frac{V_{OUT}}{V_{IN}} \times 2.5 \ [\mu s]$$

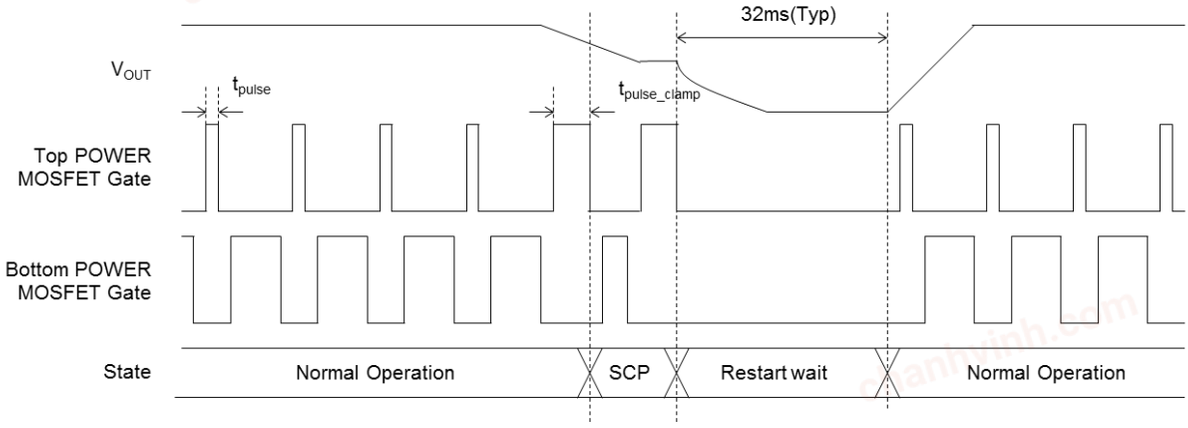

Figure31. SCP Timing Chart

3. Thermal Shutdown(TSD)
When the chip temperature exceeds Tj=175°C(Typ), both of the output MOSFETs are turned OFF and the VREGH is stopped. The operation comes back when the chip temperature comes down to 150°C(Typ) or less. TSD prevents the IC from thermal runaway under abnormal conditions exceeding Tjmax=150°C. The TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

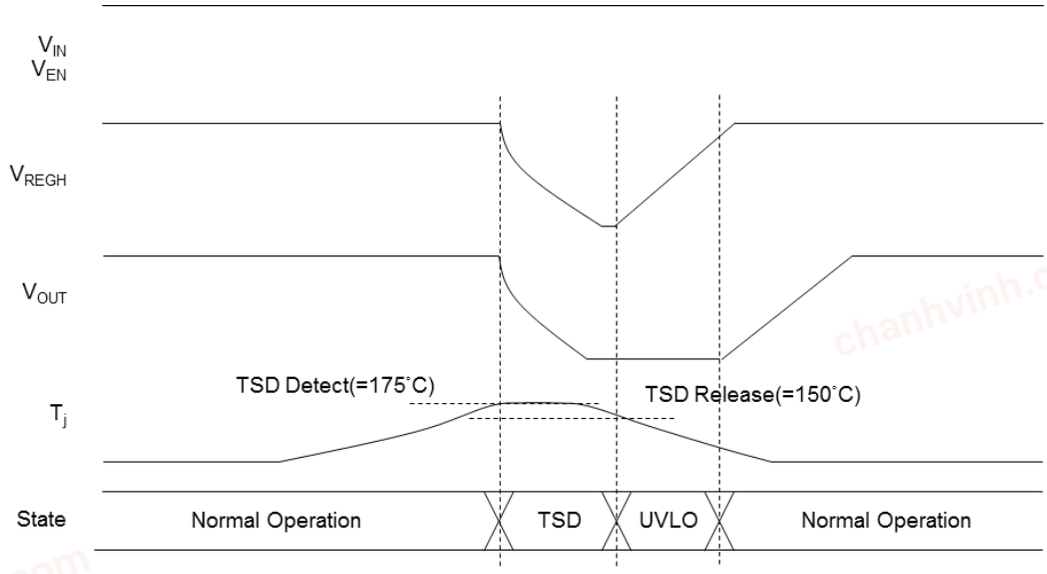

Figure 32. TSD Timing Chart

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Protect function - continued

4. Over Current Protection (OCP)
   Over Current Protection detects the lower limit value of the inductor current. The OCP is designed at 2.4A(Typ). This circuit prevents the Top POWER MOSFET from turning ON until the inductor current I_L falls below the OCP limit I_{SW}. If OCP is detected 8times in 30µs(Typ), operation stops for 32ms(Typ) and then restarts again. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected).

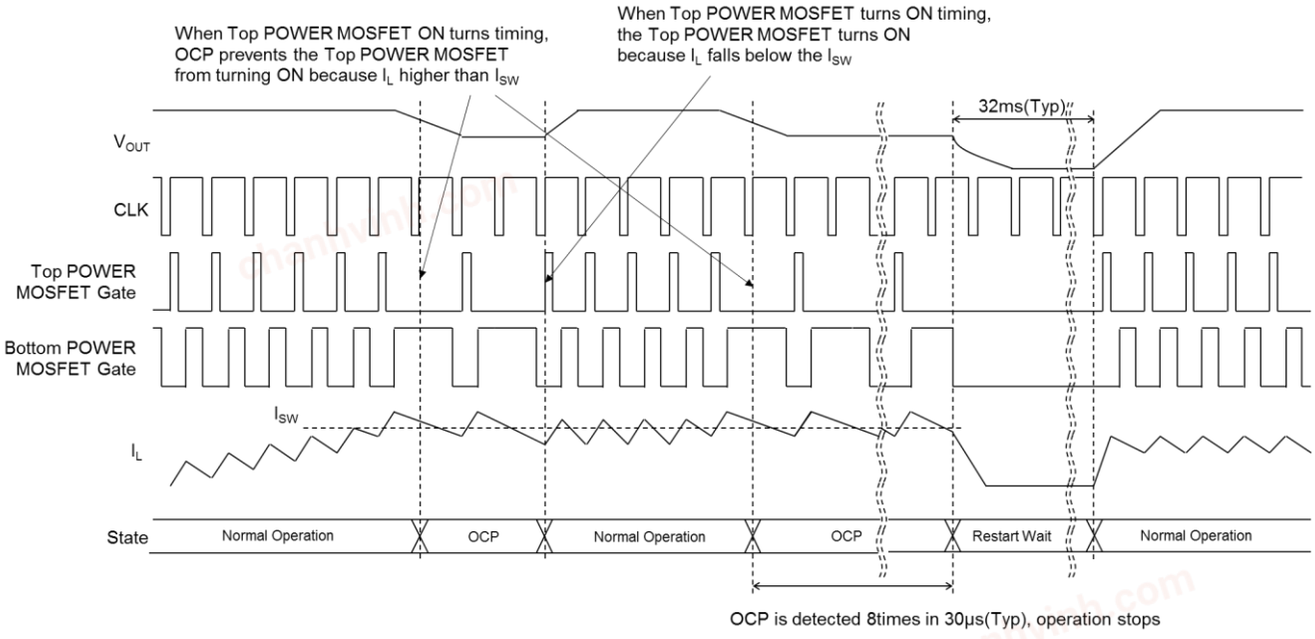

Figure 33. OCP Timing Chart

5. Over Voltage Protection (OVP)
   Over Voltage Protection compares the feedback voltage with an internal reference voltage. When the feedback voltage exceeds 0.96V(Typ) or more, the Top and Bottom POWER MOSFETs will turn OFF. When the output voltage decreases to a value of 0.92V(Typ) or less, it goes back to normal operation.

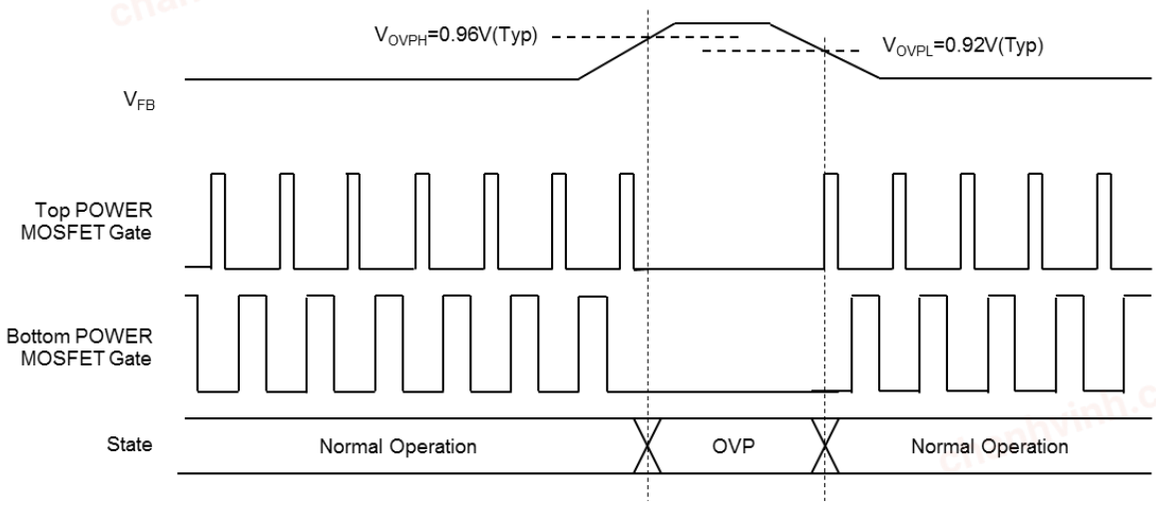

Figure 34. OVP Timing Chart

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Protect function - continued

6. Over Voltage Lockout(OVLO)
   Over Voltage Lockout monitors the VIN terminal voltage. When the VIN voltage is 60.0V(Min) or more, the chip will be on standby mode, and when the VIN voltage is 59.0V(Min) or less, the chip will startup again.

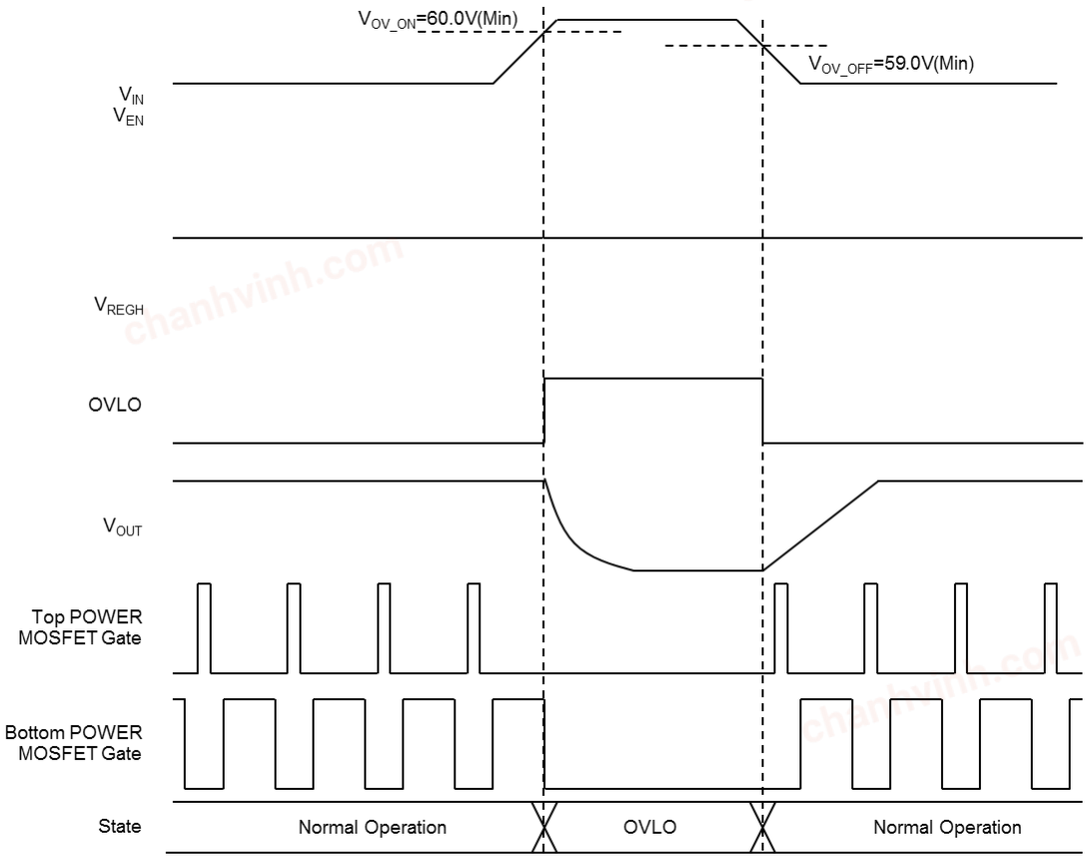

Figure 35. OVLO Timing Chart

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Selection of Components Externally Connected

Contact us if not use the recommended constant in the application circuit.

Necessary parameters in designing the power supply are as follows:

Table 1. Application Specification

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	16V to 60V
Output Voltage	V_{OUT}	5.0V
Output Ripple Voltage	ΔV_{P-P}	$20mV_{p-p}$
Output Current	I_{OUT}	Min 0.1A / Typ 0.5A / Max 1.0A
Switching Frequency	f_{SW}	2.1MHz
Operating Junction Temperature	Tjopr	-40°C to +150°C

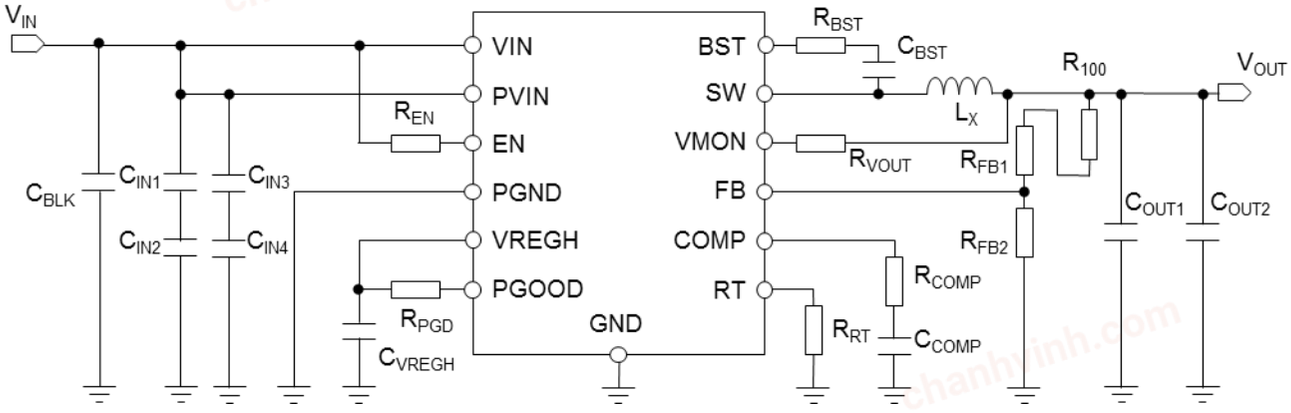

Figure 36. Application Sample Circuit

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Selection of Components Externally Connected - continued

1. Selection of the inductor L_X value

Role of the coil in the switching regulator is that it also serves as a filter for smoothing the output voltage to supply a continuous current to the load. The Inductor ripple current ΔI_L that flows to the inductor becomes small when an inductor with a large inductance value is selected. Consequently, the voltage of the output ripple ΔV_{P-P} also becomes small. It is the trade-off between the size and the cost of the inductor.

The inductance of the inductor is shown in the following equation:

$$L = \frac{(V_{IN(Max)} - V_{OUT}) \times V_{OUT}}{V_{IN(Max)} \times f_{SW} \times \Delta I_L} \quad [H]$$

Where:

$V_{IN\ (Max)}$	is the maximum input voltage
V_{OUT}	is the output voltage
f_{SW}	is the switching frequency
ΔI_L	is the peak to peak inductor current

In current mode control, sub-harmonic oscillation may happen. The slope compensation circuit is integrated into the IC in order to prevent sub-harmonic oscillation. The sub-harmonic oscillation depends on the rate of increase of output switch current. If the inductor value is too small, the sub-harmonic oscillation may happen because the inductor ripple current ΔI_L is increased. And if the inductor value is too large, the feedback loop may not achieve stability because the inductor ripple current ΔI_L is decreased. Therefore, use an inductor value of the coil within the range of 3.3µH to 10µH. The smaller the ΔI_L, the smaller the Inductor core loss (iron loss), and the smaller is the loss due to ESR of the output capacitor. In effect, ΔV_{P-P} (Output peak-to-peak ripple voltage) will be reduced. ΔV_{P-P} is shown in the following equation.

$$\Delta V_{P-P} = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} \quad [V] \qquad (a)$$

Where:

ESR	is the equivalent series resistance of the output capacitor
C_{OUT}	is the output capacitance
ΔI_L	is the peak to peak inductor current
f_{SW}	is the switching frequency

Generally, even if ΔI_L is somewhat large, the ΔV_{P-P} target is satisfied because the ceramic capacitor has a very-low ESR. It also contributes to the miniaturization of the application board. Also, because of the lower rated current, smaller inductor is possible since the inductance is small. The disadvantages are increase in core losses in the inductor and the decrease in maximum output current. When other capacitors (electrolytic capacitor, tantalum capacitor, and electro conductive polymer etc.) are used for output capacitor C_{OUT}, check the ESR from the manufacturer's data sheet and determine the ΔI_L to fit within the acceptable range of ΔV_{P-P}. Especially in the case of electrolytic capacitor, because the decrease in capacitance at low temperatures is significantly large, this will make ΔV_{P-P} increase. When using capacitor at low temperature, this is an important consideration.

The shielded type (closed magnetic circuit type) is the recommended type of inductor to be used. Please note that magnetic saturation may occur. It is important not to saturate the core in all cases. Precautions must be taken into account on the given provisions of the current rating because it differs on every manufacturer. Please confirm the rated current at maximum ambient temperature of application to the manufacturer.

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Selection of Components Externally Connected - continued

2. Selection of Output Capacitor C_{OUT}

The output capacitor is selected based on the ESR that is required from the equation (a). ΔV_{P-P} can be reduced by using a capacitor with a small ESR. The ceramic capacitor is the best option that meets this requirement. It is because not only does it has a small ESR but the ceramic capacitor also contributes to the size reduction of the application circuit. Please confirm the frequency characteristics of ESR from the datasheet of the manufacturer, and consider a low ESR value for the switching frequency being used. It is necessary to consider the ceramic capacitor because the DC biasing characteristic is important. For the voltage rating of the ceramic capacitor, twice or more than the maximum output voltage is usually required. By selecting a high voltage rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristics of X7R or better is recommended. Because the voltage rating of a large ceramic capacitor is low, the selection becomes difficult for an application with high output voltage. In that case, please connect multiple ceramic capacitors in series or select electrolytic capacitor. Consider having a voltage rating of 1.2 times or more of the output voltage when using electrolytic capacitor. Electrolytic capacitors have a high voltage rating, large capacitance, small amount of DC biasing characteristics, and are generally reasonable. Since the electrolytic capacitor is usually OPEN when it fails, it is effective to use for applications when reliability is required. But there are disadvantages such as, ESR is relatively high, and decreases capacitance value at low temperatures. In this case, please take note that ΔV_{P-P} may increase at low temperature conditions. Moreover, consider the lifetime characteristic of this capacitor because it has a possibility to dry up. A tantalum capacitor and a conductive polymer hybrid capacitor have excellent temperature characteristics unlike the electrolytic capacitor. Moreover, since their ESR is smaller than an electrolytic capacitor, the ripple voltage is relatively-small over a wide temperature range. Since these capacitors have almost no DC bias characteristics, design will be easier. Regarding voltage rating, the tantalum capacitor is selected such that its capacitance is twice the value of the output voltage, and for the conductive polymer hybrid capacitor, it is selected such that the voltage rating is 1.2 times the value of the output voltage. The disadvantage of a tantalum capacitor is that it is SHORTED when it is destroyed, and its breakdown voltage is low. It is not generally selected in an application that reliability is a demand. An electro conductive polymer hybrid capacitor is OPEN when destroyed. Though it is effective for reliability, its disadvantage is that it is generally expensive.

To improve the performance of ripple voltage in this condition, following is recommended:

1. Use low ESR capacitor like ceramic or conductive polymer hybrid capacitor.
2. Use a capacitor C_{OUT} with a higher capacitance value.

These capacitors are rated in ripple current. The RMS values of the ripple current that can be obtained in the following equation must not exceed the ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \text{ [A]}$$

Where:

$I_{CO(RMS)}$	is the value of the ripple electric current
ΔI_L	is the peak to peak inductor current

In addition, for the total value of capacitance in the output line C_{OUT}(Max), choose a capacitance value less than the value obtained by the following equation:

$$C_{OUT(Max)} < \frac{t_{SS(Min)} \times (I_{SW(Min)} - I_{SWSTART(Max)})}{V_{OUT}} \text{ [F]}$$

Where:

$I_{SW(Min)}$	is the OCP operation switch current (Min)
$t_{SS(Min)}$	is the Soft Start Time (Min)
$I_{SWSTART(Max)}$	is the maximum output current during startup
V_{OUT}	is the output voltage

Startup failure may happen if the limits from the above-mentioned are exceeded. Especially if the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup preventing the output to turn on. Please confirm this on the actual application. For stable transient response, the loop is dependent to C_{OUT}. Please select after confirming the setting of the phase compensation circuit.

Also, in case of large changing input voltage and load current, select the capacitance accordingly by verifying that the actual application setup meets the required specification.

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Selection of Components Externally Connected - continued

3. Selection of Input Capacitor C_{IN}, C_{BLK}

The input capacitor is usually required for two types of decoupling: capacitors C_{IN} and bulk capacitors C_{BLK}. Ceramic capacitors with values more than 1.2µF are necessary for the decoupling capacitor C_{IN}. Ceramic capacitors are effective by placing it as close as possible to the VIN pin. The voltage rating of the capacitors is recommended to be more than 1.2 times the maximum input voltage, or twice the normal input voltage. The capacitor value including device variation, temperature change, DC bias change, and aging change must be larger than minimum value. Also, the IC might not operate properly when the PCB layout or the position of the capacitor is not good. Please check “Notes on the PCB Layout” on page 30.

The bulk capacitor is optional. The bulk capacitor prevents the decrease in the line voltage and serves as a backup power supply to keep the input voltage constant. A low ESR electrolytic capacitor with large capacitance is suitable for the bulk capacitor. It is necessary to select the best capacitance value for each set of application. In that case, please take note not to exceed the rated ripple current of the capacitor.

The RMS value of the input ripple current $I_{CIN(RMS)}$ is obtained in the following equation:

$$I_{CIN(RMS)} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \text{ [A]}$$

Where:

$I_{OUT(MAX)}$ is the maximum output current.

In addition, applications requiring high reliability, it is recommended to connect the capacitors in parallel to accommodate multiple electrolytic capacitors and minimize the chances of drying up. For ceramic capacitors, it is recommended to make two series + two parallel structures to decrease the risk of capacitor destruction due to short circuit conditions.

When the impedance on the input side is high for some reason (because the wiring from the power supply to VIN is long, etc.), then high capacitance is needed. In actual conditions, it is necessary to verify that there are no problems like IC turns off, or the output overshoots due to the change in V_{IN} at transient response.

4. Selection of Output Voltage Setting Resistance R_{FB1}, R_{FB2}

The output voltage is described by the following equation:

$$V_O = 0.8 \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \text{ [V]}$$

Power efficiency is reduced with a small R_{FB1} + R_{FB2}, please set the current flowing through the feedback resistors as small as possible in comparison to the output current I_{OUT}.

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Selection of Components Externally Connected - continued

5. Selection of the Phase Compensation Circuit R_{COMP}, C_{COMP}

A good high frequency response performance is achieved by setting the 0dB crossing frequency, fc, (frequency at 0dB gain) high. However, you need to be aware of the trade-off correlation between speed and stability. Moreover, DC / DC converter application is sampled by switching frequency, so the gain of this switching frequency must be suppressed. It is necessary to set the 0dB crossing frequency to 80kHz or less of the switching frequency. In general, target these characteristics as follows:

- At 0dB crossing frequency, fc, phase lag should be 135˚ or less (phase margin is 45˚ or more).
- The 0dB crossing frequency, fc, must be 80kHz or less.

Achieving stability by using phase compensation is done by cancelling the f_{P1} and f_{P2} (error amp pole and power stage pole) of the feedback loop by the use of f_{Z1}. f_{P1}, f_{P2} and f_{Z1} are determined in the following equations:

$$f_{Z1} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \text{ [Hz]}$$

$$f_{P1} = \frac{1}{2\pi \times C_{OUT} \times R_{OUT}} \text{ [Hz]}$$

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_{COMP} \times A_V} \text{ [Hz]}$$

Where:

R_{OUT} is the resistance assumed actual load[Ω] = Output Voltage[V] / Output Current[A]
G_{EA} is the Error Amp trans conductance (300µA/V)
A_V is the Error Amp Voltage Gain (63dB)

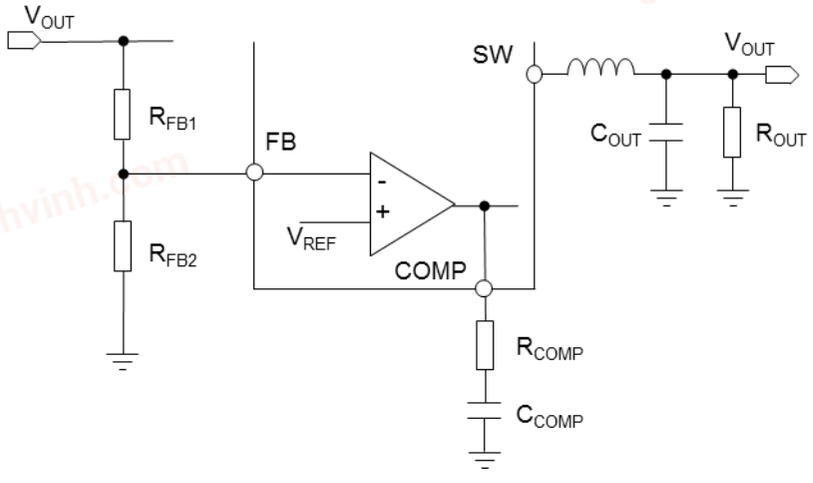

Figure 37. Setting the Phase Compensation Circuit

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Selection of Components Externally Connected - continued

6. Selection of the Switching Frequency Setting Resistance R_{RT}

The internal switching frequency can be set by connecting a resistor between RT and GND.
The range of frequency that can be set is 1.9MHz to 2.3MHz, and the relation between resistance and the switching frequency is decided as shown in the figure below. When setting beyond this range, there is a possibility that there is no oscillation and IC operation cannot be guaranteed.

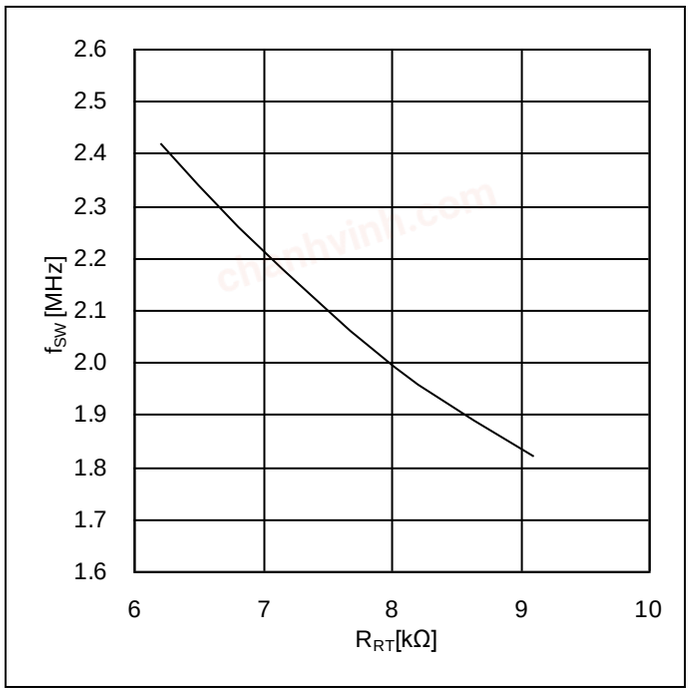

Figure 38. Switching Frequency
vs Switching Frequency Setting Resistance

Table 2. R_{RT} vs f_{SW}

R_{RT} [kΩ]	f_{SW} [MHz]
6.8	2.26
7.5	2.10
8.2	1.96

7. Selection of the Bootstrap Capacitor and Resistor

Bootstrap capacitor C_{BST} value shall be 0.022µF. Bootstrap resistor R_{BST} value shall be 3.3Ω. Connect the bootstrap capacitor in series with the bootstrap resistor between SW pin and BST pin. Recommended products are described in Application Examples1 on page 25.

8. Selection of the VREGH Capacitor.

VREGH capacitor C_{VREGH} shall be 2.2µF ceramic capacitor. Connect the VREGH capacitor between VREGH pin and GND.

9. Selection of the VMON Resistor

At the time of V_{OUT} short circuit, current may be drawn from the VMON terminal due to an inductive load. Connect a resistor to limit that current. VMON resistor R_{VOUT} shall be 2kΩ.

10. Soft Start Time

Soft Start prevents the overshoot of the output voltage. It changes in proportion to the switching frequency f_{SW}. Soft start time at f_{SW} 2.1MHz(Typ) is 1.1ms(Typ). The production tolerance of t_{SS} is ±36%. t_{SS} can be calculated by using the equation.

$$t_{SS} = \frac{2310}{fsw} \text{ [s]}$$

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Application Examples1

Table 3. Specification Example 1

Parameter	Symbol	Specification Case
Product Name	IC	BD9V101MUF-LB
Input Voltage	V_{IN}	16V to 60V
Output Voltage	V_{OUT}	5.0V
Output Ripple Voltage	ΔV_{P-P}	20mVp-p
Output Current	I_{OUT}	0A to 1.0A
Switching Frequency	f_{SW}	2.1MHz
Operating Junction Temperature	Tjopr	-40°C to +150°C

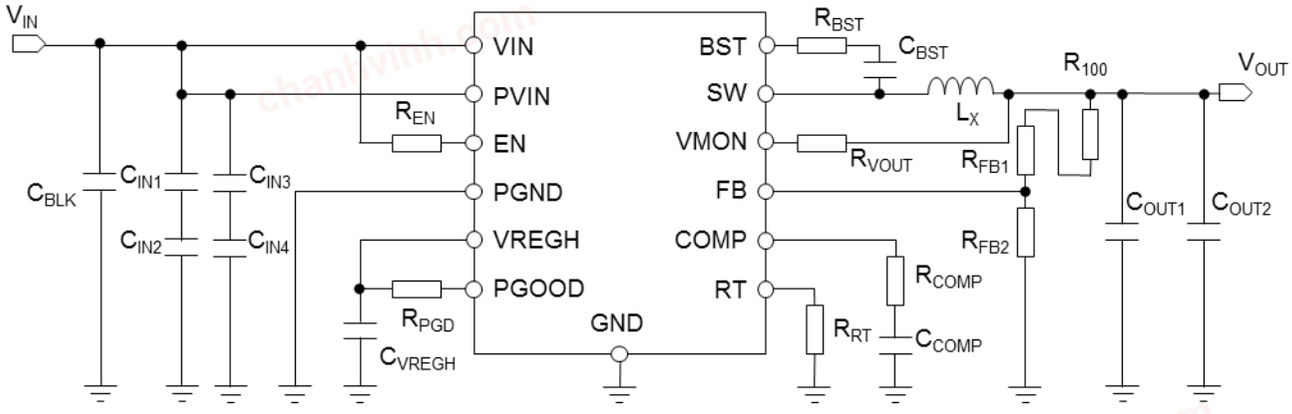

Figure 39. Reference Circuit 1

Table 4. Parts List 1

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{BLK}	-	-	-	-	-
C_{IN1}	3225	4.7µF, X7R, 50V	GCM32ER71H475K	Ceramic	MURATA
C_{IN2}	3225	4.7µF, X7R, 50V	GCM32ER71H475K	Ceramic	MURATA
C_{IN3}	1608	0.1µF, X7R, 50V	GCM188R71H104K	Ceramic	MURATA
C_{IN4}	1608	0.1µF, X7R, 50V	GCM188R71H104K	Ceramic	MURATA
C_{BST}	1608	0.022µF, X7R, 50V	GCM188R71H223K	Ceramic	MURATA
R_{BST}	1608	3.3Ω, 5%, 1/10W	MCR03EZPJ3R3	Chip Resistor	ROHM
C_{VREGH}	2012	2.2µF, X7R ,16V	GCM21BR71C225K	Ceramic	MURATA
R_{PGD}	1608	100kΩ, 0.5%, 1/10W	MCR03EZPD1003	Chip Resistor	ROHM
R_{VOUT}	1608	2.0kΩ, 0.5%, 1/10W	MCR03EZPD2001	Chip Resistor	ROHM
R_{100}	-	Short	-	-	-
R_{FB1}	1608	43kΩ, 0.5%, 1/10W	MCR03EZPD4302	Chip Resistor	ROHM
R_{FB2}	1608	8.2kΩ, 0.5%, 1/10W	MCR03EZPD8201	Chip Resistor	ROHM
R_{RT}	1608	7.5kΩ, 0.5%, 1/10W	MCR03EZPD7501	Chip Resistor	ROHM
R_{COMP}	1608	51kΩ, 0.5%, 1/10W	MCR03EZPD5102	Chip Resistor	ROHM
C_{COMP}	1608	1000pF, X7R, 50V	GCM188R71H102K	Ceramic	MURATA
L_X	-	4.7µH	CLF6045NIT-4R7N-D	Inductor	TDK
C_{OUT1}	3225	22µF, X7R, 16V	GCM32ER71C226K	Ceramic	MURATA
C_{OUT2}	3225	22µF, X7R, 16V	GCM32ER71C226K	Ceramic	MURATA

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Application Examples1 - continued

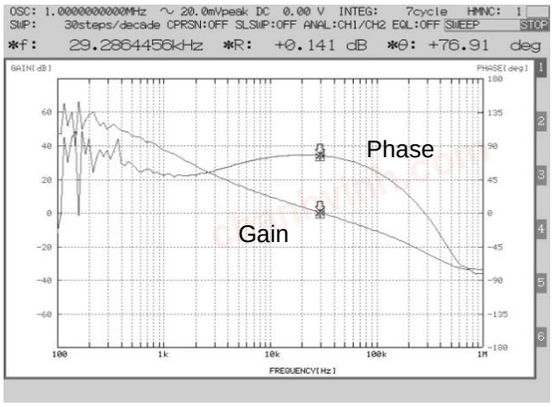

Figure 40. Frequency Characteristics
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=500mA)

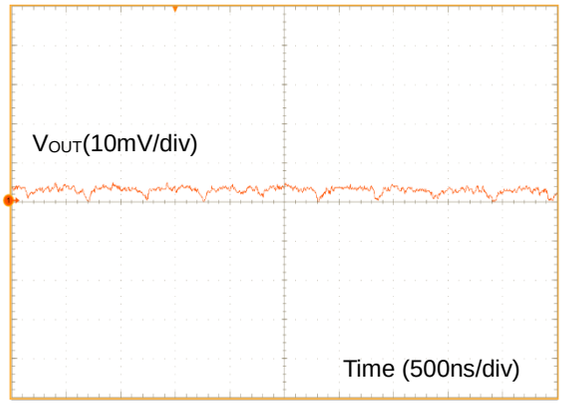

Figure 41. Ripple Voltage
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=500mA)

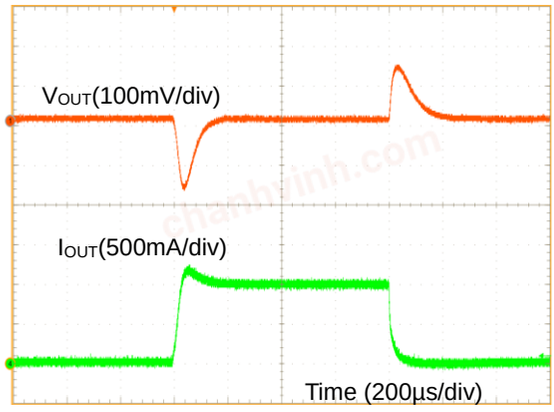

Figure 42. V_{IN} Load Response
(V_{IN}=48V, V_{OUT}=5V, I_{OUT}=0A ↔ 1A)

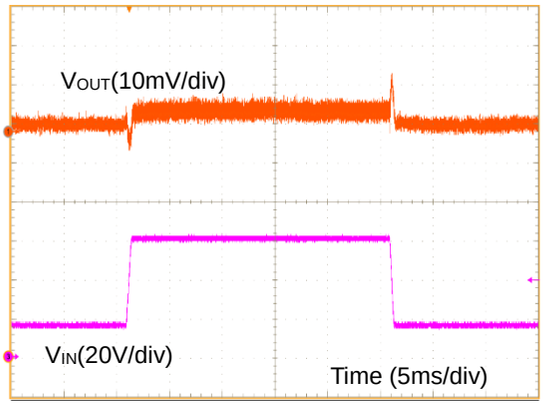

Figure 43. V_{IN} Transient Response
(V_{IN}=16V ↔ 60V, V_{OUT}=5V, I_{OUT}=500mA)

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Application Examples2

Table 5. Specification Example 2

Parameter	Symbol	Specification Case
Product Name	IC	BD9V101MUF-LB
Input Voltage	V_{IN}	16V to 60V
Output Voltage	V_{OUT}	3.3V
Output Ripple Voltage	ΔV_{P-P}	20mVp-p
Output Current	I_{OUT}	0A to 1.0A
Switching Frequency	f_{SW}	2.1MHz
Operating Junction Temperature	Tjopr	-40°C to +150°C

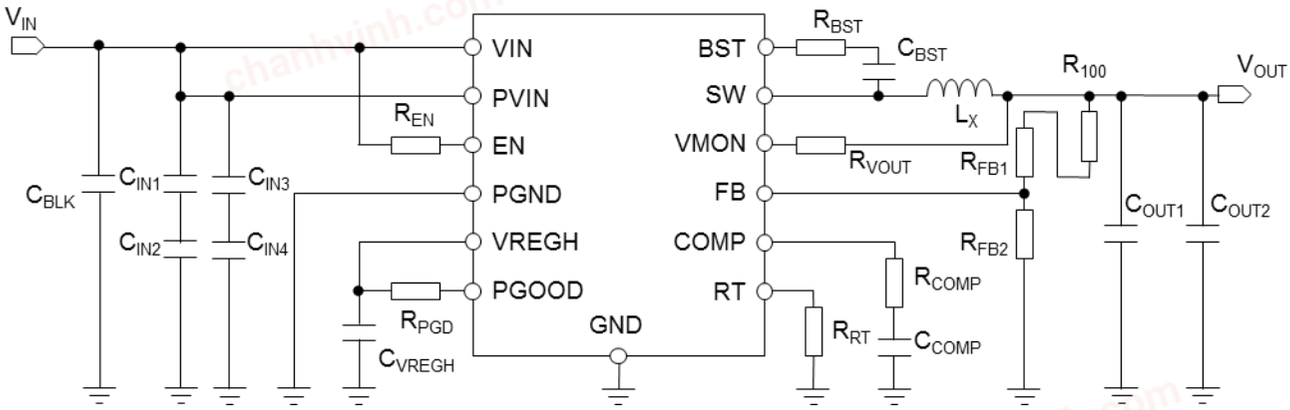

Figure 44. Reference Circuit 2

Table 6. Parts List 2

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{BLK}	-	-	-	-	-
C_{IN1}	3225	4.7µF, X7R, 50V	GCM32ER71H475K	Ceramic	MURATA
C_{IN2}	3225	4.7µF, X7R, 50V	GCM32ER71H475K	Ceramic	MURATA
C_{IN3}	1608	0.1µF, X7R, 50V	GCM188R71H104K	Ceramic	MURATA
C_{IN4}	1608	0.1µF, X7R, 50V	GCM188R71H104K	Ceramic	MURATA
C_{BST}	1608	0.022µF, X7R, 50V	GCM188R71H223K	Ceramic	MURATA
R_{BST}	1608	3.3Ω, 5%, 1/10W	MCR03EZPJ3R3	Chip Resistor	ROHM
C_{VREGH}	2012	2.2µF, X7R ,16V	GCM21BR71C225K	Ceramic	MURATA
R_{PGD}	1608	100kΩ, 0.5%, 1/10W	MCR03EZPD1003	Chip Resistor	ROHM
R_{VOUT}	1608	2.0kΩ, 0.5%, 1/10W	MCR03EZPD2001	Chip Resistor	ROHM
R_{100}	-	Short	-	-	-
R_{FB1}	1608	47kΩ, 0.5%, 1/10W	MCR03EZPD4702	Chip Resistor	ROHM
R_{FB2}	1608	15kΩ, 0.5%, 1/10W	MCR03EZPD1502	Chip Resistor	ROHM
R_{RT}	1608	7.5kΩ, 0.5%, 1/10W	MCR03EZPD7501	Chip Resistor	ROHM
R_{COMP}	1608	75kΩ, 0.5%, 1/10W	MCR03EZPD7502	Chip Resistor	ROHM
C_{COMP}	1608	560pF, X7R, 50V	GCM188R71H561K	Ceramic	MURATA
L_X	-	4.7µH	CLF6045NIT-4R7N-D	Inductor	TDK
C_{OUT1}	3225	22µF, X7R, 16V	GCM32ER71C226K	Ceramic	MURATA
C_{OUT2}	3225	22µF, X7R, 16V	GCM32ER71C226K	Ceramic	MURATA

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Application Examples2 - continued

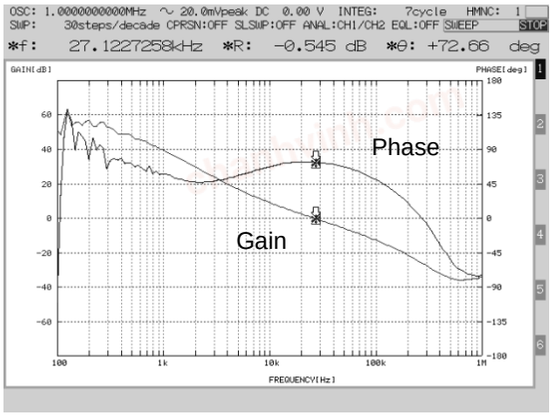

Figure 45. Frequency Characteristics
(V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=500mA)

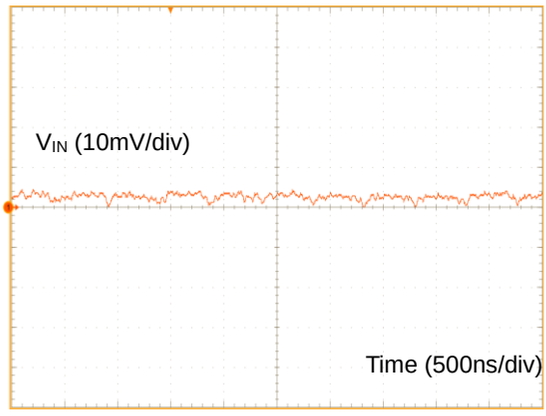

Figure 46. Ripple Voltage
(V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=500mA)

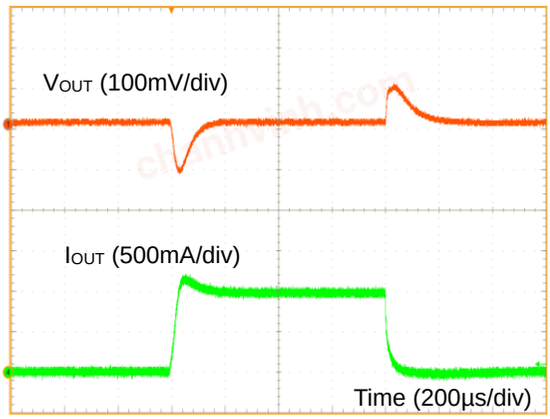

Figure 47. V_{IN} Load Response
(V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=0A ↔ 1A)

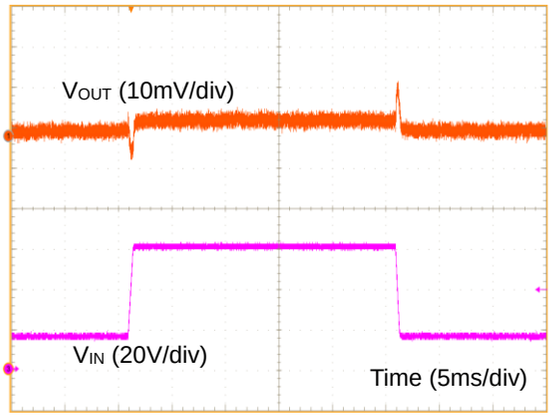

Figure 48. V_{IN} Transient Response
(V_{IN}=16V ↔ 60V, V_{OUT}=3.3V, I_{OUT}=500mA)

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Power Supply Line Circuit

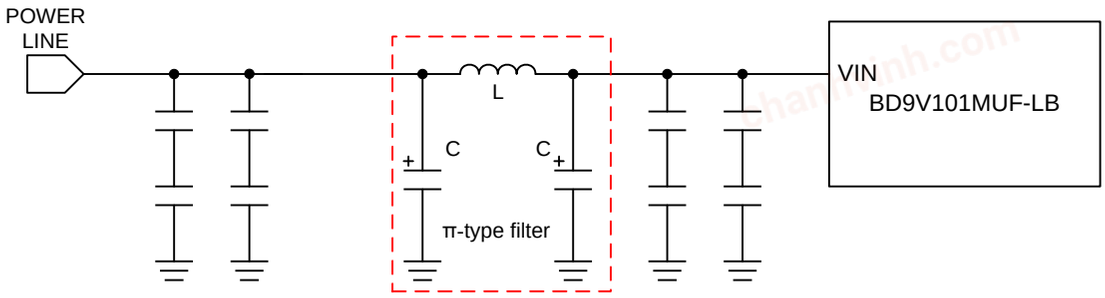

Figure 49. Power Supply Line Circuit

As a reference, the power supply line circuit example is given in Figure 49.
π-type filter is a third-order LC filter. In general, it is used in combination with decoupling capacitors for high frequency. Large attenuation characteristics can be obtained and thus excellent characteristic as a EMI filter. Devices used for π-type filters should be placed close to each other.

Table 7. Reference Parts of Power Supply Line Circuit

Device	Part name (series)	Manufacturer
L	CLF series	TDK
L	XAL series	Coilcraft
C	CJ series / CZ series	NICHICON

Recommended Parts Manufacturer List

Shown below is the list of the recommended parts manufacturers for reference.

Type	Manufacturer	URL
Electrolytic Capacitor	NICHICON	www.nichicon-us.com
Ceramic Capacitor	Murata	www.murata.com
Inductor	TDK	product.tdk.com
Inductor	Coilcraft	www.coilcraft.com
Inductor	SUMIDA	www.sumida.com
Resistor	ROHM	www.rohm.com

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PCB Layout Design

PCB layout design for DC/DC converter power supply IC is as important as the circuit design. Appropriate layout can avoid various problems caused by power supply circuit. Figure 50-a to 50-c show the current path in a buck converter circuit. The Loop 1 in Figure 50-a is a current path when H-side switch is ON and L-side switch is OFF, the Loop 2 in Figure 50-b is when H-side switch is OFF and L-side switch is ON. The thick line in Figure 50-c shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element H-side and L-side switch change from OFF to ON, and vice versa. These sharp changes induce several harmonics in the waveform. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more detail refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

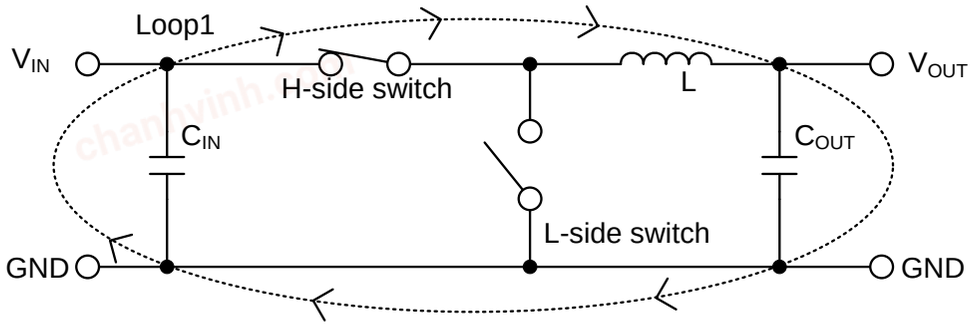

Figure 50-a. Current path when H-side switch = ON, L-side switch = OFF

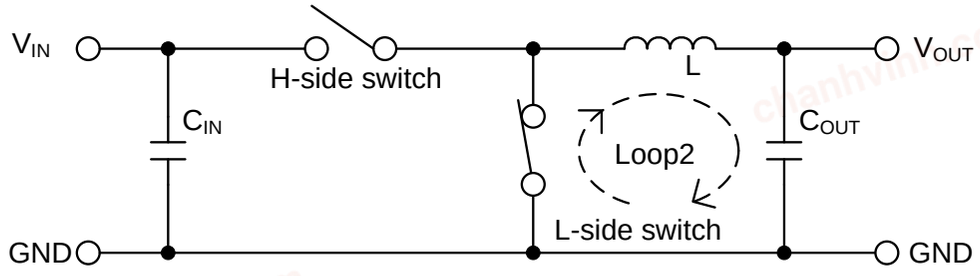

Figure 50-b. Current path when H-side switch = OFF, L-side switch = ON

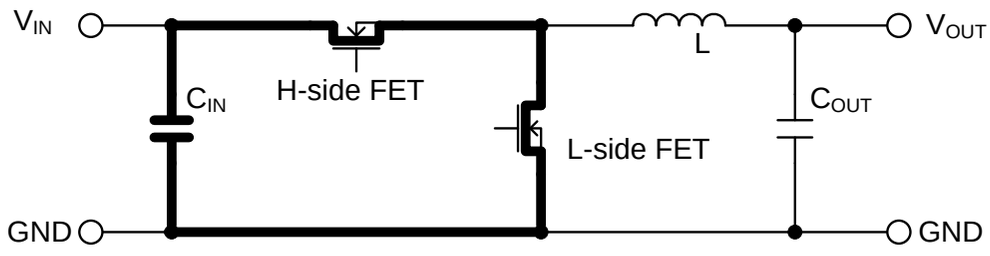

Figure 50-c. Difference of current and critical area in layout

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PCB Layout Design - continued

When designing the PCB layout, please pay extra attention to the following points:

- Place input capacitor on the same PCB surface as the IC and as close as possible to the IC's PVIN terminal.
- Switching nodes should be traced as thick and short as possible to the inductor, because they may induce the noise to the other nodes due to AC coupling.
- Please keep the lines connected to FB and COMP away from the SW node as far as possible.
- Please place output capacitor away from input capacitor to avoid harmonics noise from the input.
- R_{100} is an option, used for feedback's frequency response measurement.
  By inserting a resistor at R_{100}, it is possible to measure the frequency response (phase margin) using a FRA.
  However, the resistor will not be used in actual application, please use this resistor pattern in short-circuit mode.

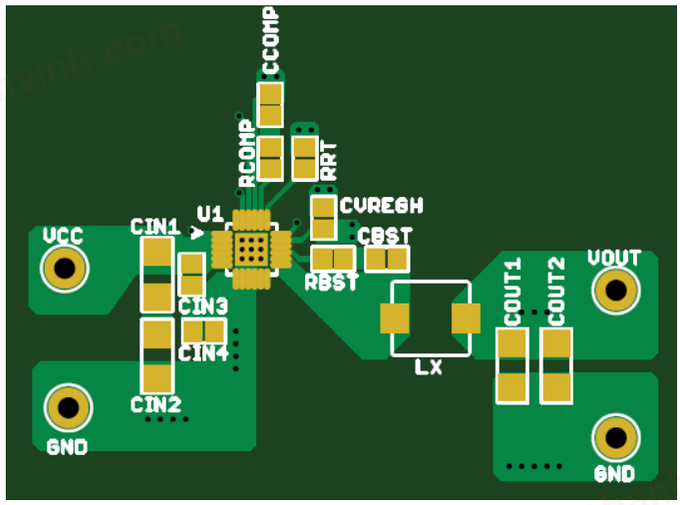

Figure 51. Evaluation Board Layout Example

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Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature Ta is to be 125 °C or less.
2. The chip junction temperature Tj is to be 150 °C or less.

The chip junction temperature Tj can be considered in the following two patterns:

1. To obtain Tj from the package surface center temperature Tt in actual use

$$Tj = Tt + \psi_{JT} \times W \ [°C]$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta_{JA} \times W \ [°C]$$

Where:

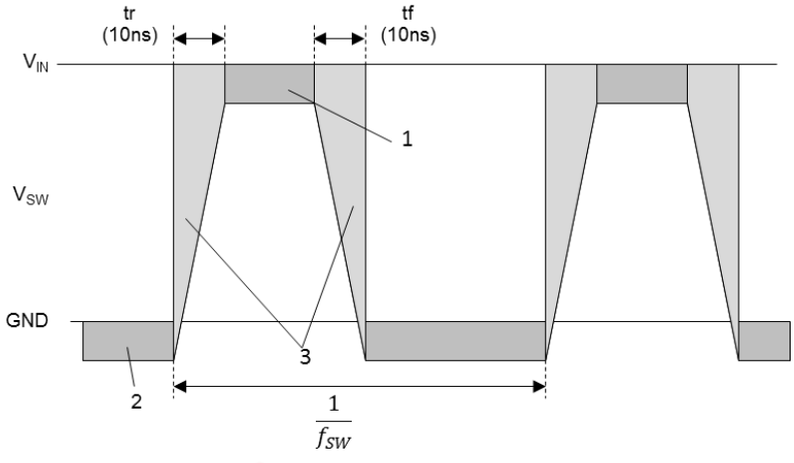
ψ_{JT}	is junction to top characterization parameter (Refer to page 6)
θ_{JA}	is junction to ambient (Refer to page 6)

The heat loss W of the IC can be obtained by the formula shown below:

$$W = R_{ONH} \times {I_{OUT}}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times {I_{OUT}}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{CC} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \ [W]$$

Where:

R_{ONH}	is the Top Power NMOS ON Resistance (Refer to page 7) [Ω]
R_{ONL}	is the Bottom Power NMOS ON Resistance (Refer to page 7) [Ω]
I_{OUT}	is the Load Current [A]
V_{OUT}	is the Output Voltage [V]
V_{IN}	is the Input Voltage [V]
I_{CC}	is the Circuit Current (Refer to page 7) [A]
tr	is the Switching Rise Time [s] (Typ:10ns)
tf	is the Switching Fall Time [s] (Typ:10ns)
f_{SW}	is the Switching Frequency [Hz]



1. $R_{ONH} \times {I_{OUT}}^2$
2. $R_{ONL} \times {I_{OUT}}^2$
3. $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_O \times f_{SW}$

Figure 52. SW Waveform

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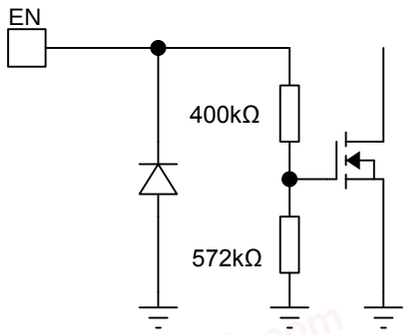
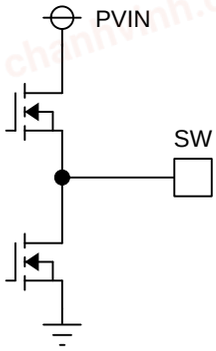
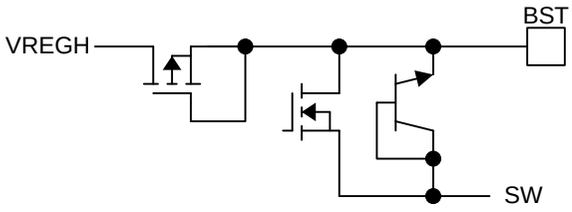
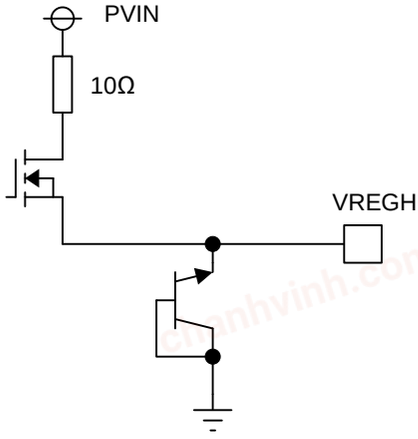
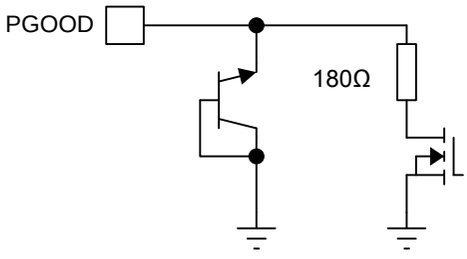
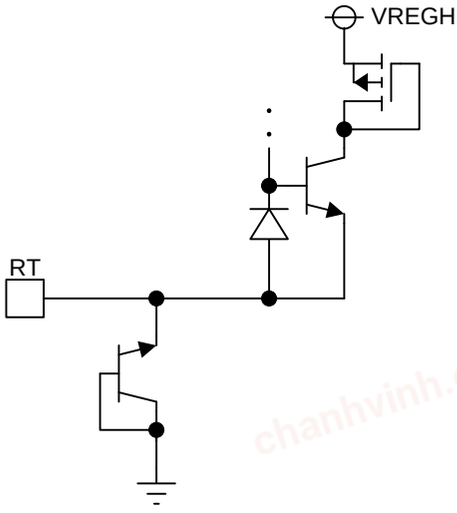
I/O Equivalent Circuit

1. EN	13,14 SW
	
15. BST	**17. VREGH**
	
18. PGOOD	**19. RT**
	

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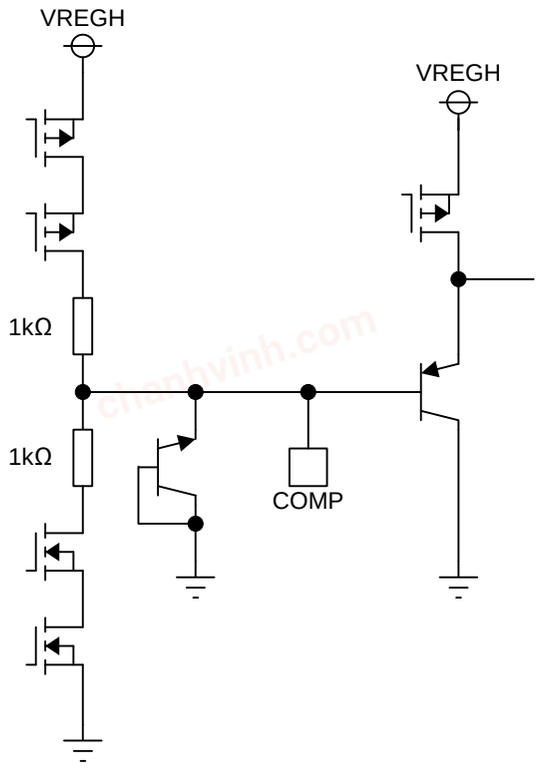
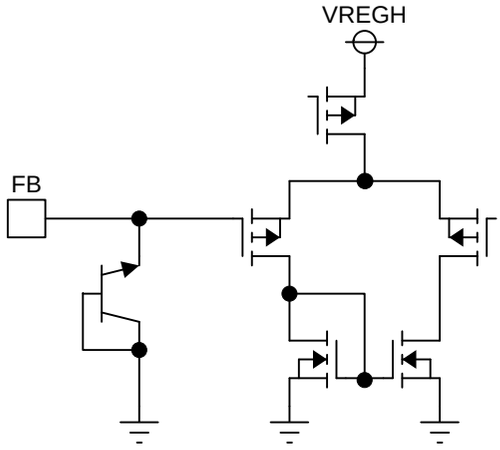
I/O Equivalent Circuit - continued

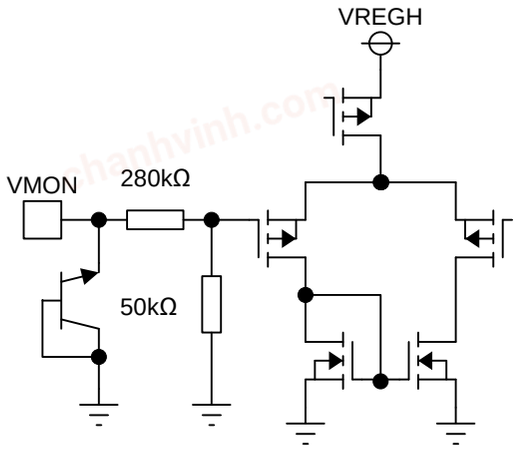
20. COMP



22. FB



23. VMON



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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

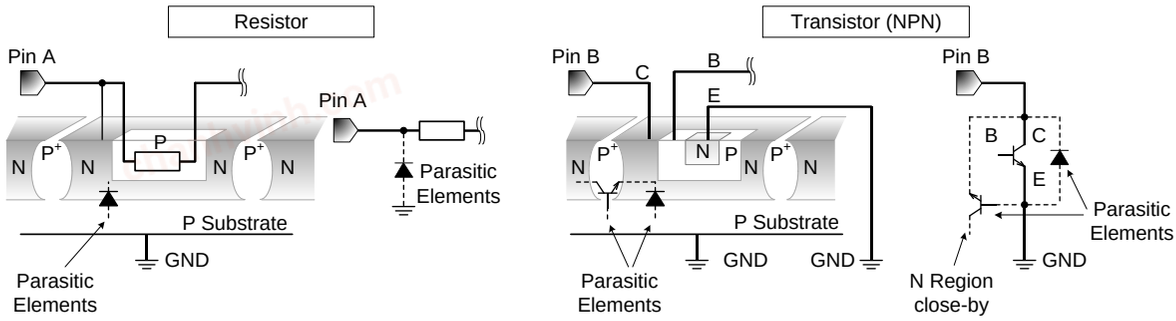

Figure 53. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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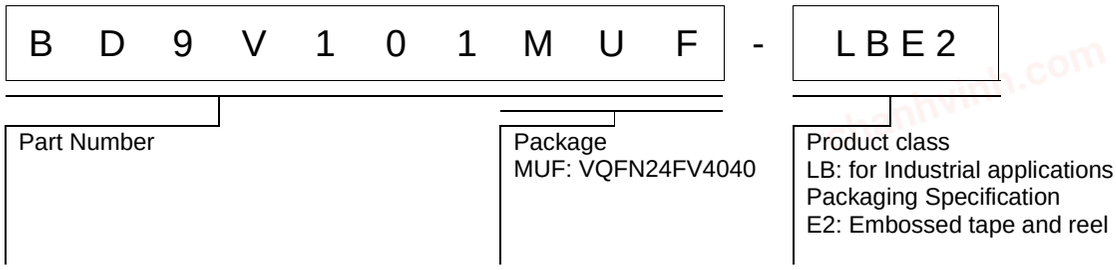
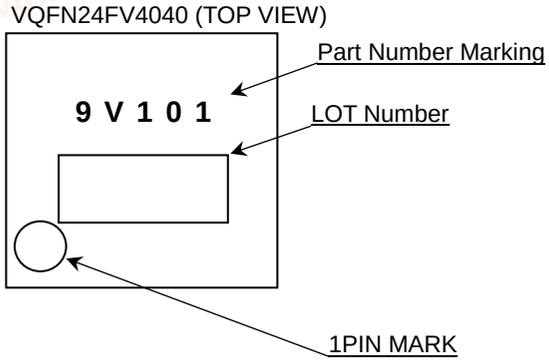
Ordering Information



Marking Diagrams



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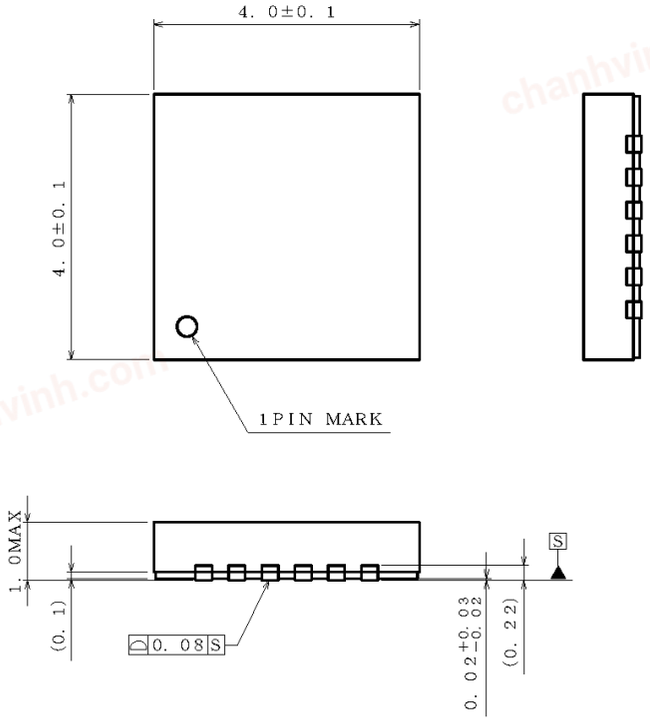
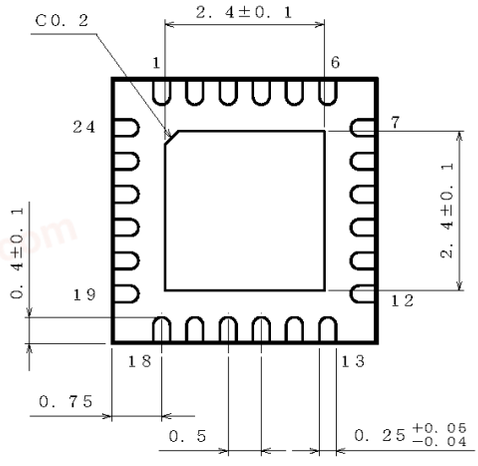
Physical Dimension, Tape and Reel Information

Package Name	VQFN24FV4040



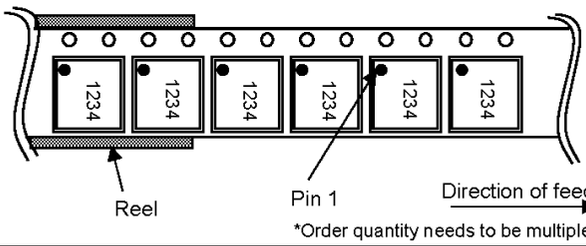


(UINT : mm)
PKG : VQFN24FV4040
Drawing No. EX394-5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
15.Sept.2017	001	New Release

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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General Precaution

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