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3.5 V to 40 V Input, 2 A Single 2.2 MHz Buck DC/DC Converter For Automotive

BD9P2x5MUF-C Series

General Description

BD9P2x5MUF-C Series are current mode synchronous buck DC/DC converter integrating POWER MOSFETs.

Features

- Nano Pulse Control™
- AEC-Q100 Qualified*(Note 1)*
- Minimum ON Pulse 50 ns (Max)
- Synchronous Buck DC/DC Converter Integrating POWER MOSFETs
- Soft Start Function
- Current Mode Control
- Reset Function
- Quiescent Current 10 µA (Typ) with 12 V Input to 5.0 V Output
- Light Load Mode (LLM)
- Forced Pulse Wide Modulation (PWM) Mode
- Phase Compensation Included
- Selectable Spread Spectrum Switching
- External Synchronization Function
- Selectable Over Current Protection (OCP)
- Input Under Voltage Lockout (UVLO) Protection
- Thermal Shutdown (TSD) Protection
- Output Over Voltage Protection (OVP)
- Short Circuit Protection (SCP)

(Note 1) Grade 1

Applications

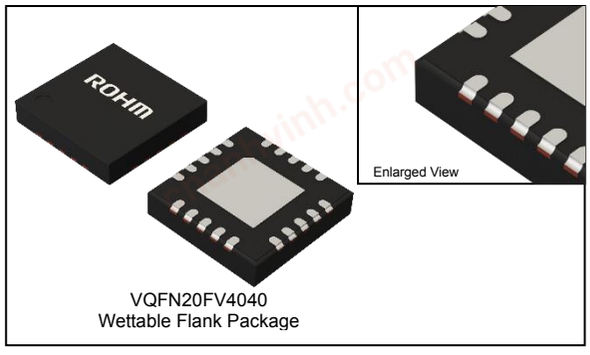
- Automotive Powered Supplies
- Consumer Powered Supplies

Key Specifications

- Input Voltage Range: 3.5 V to 40 V (Initial startup is 4.0 V or more)
- Output Voltage Range
  - BD9P205MUF-C: 0.8 V to 8.5 V
  - BD9P235MUF-C: 3.3 V (Typ)
  - BD9P255MUF-C: 5.0 V (Typ)
- Output Current:
  - OCP_SEL = H: 1.5 A (Max)
  - OCP_SEL = L: 2.0 A (Max)
- Switching Frequency: 2.2 MHz (Typ)
- Output Voltage Accuracy: ±1.75 % (-40 °C to +125 °C)
- Shutdown Current: 2.1 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

	W (Typ) x D (Typ) x H (Max)
VQFN20FV4040	4.0 mm x 4.0 mm x 1.0 mm



Typical Application Circuit

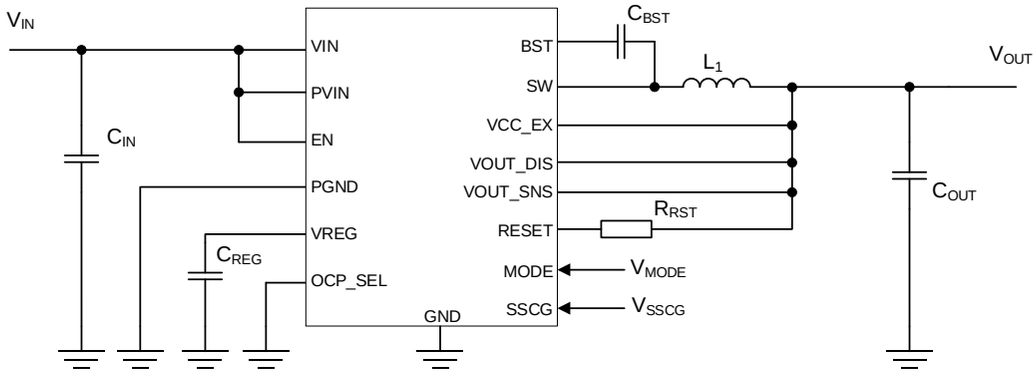


Figure 1. Application Circuit with Discharge Function (BD9P235MUF-C, BD9P255MUF-C)

Nano Pulse Control™ is a trademark or a registered trademark of ROHM Co., Ltd.

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

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Typical Application Circuit - continued

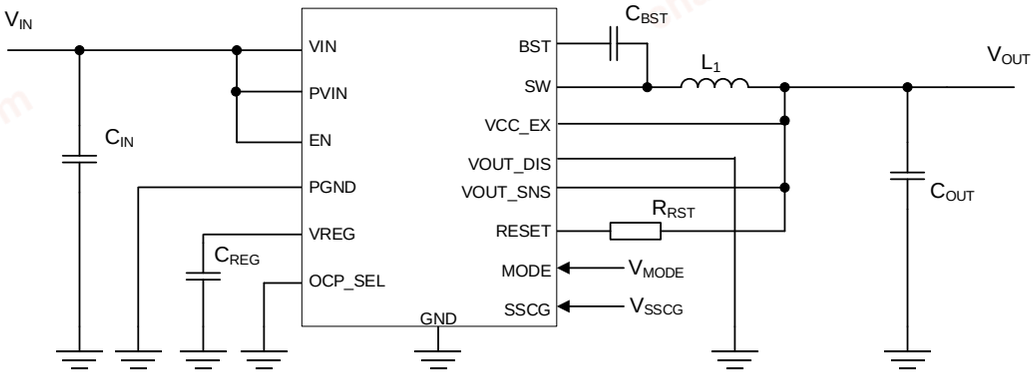


Figure 2. Application Circuit without Discharge Function (BD9P235MUF-C, BD9P255MUF-C)

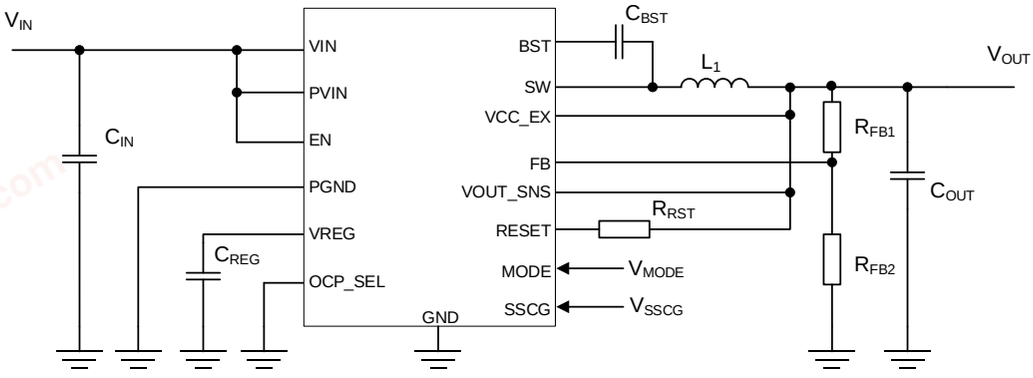


Figure 3. Application Circuit (BD9P205MUF-C)

Note: The Difference between BD9P205MUF-C, BD9P235MUF-C and BD9P255MUF-C
The VOUT_DIS pin and discharge function are not available with BD9P205MUF-C. The FB pin is assigned on the BD9P205MUF-C and the resistors dividing the output voltage are connected. The output voltage is defined by the resistors (R_{FB1}, R_{FB2}).
The VOUT discharge function are available with BD9P235MUF-C and BD9P255MUF-C, and connect the VOUT_DIS pin to VOUT. And connect the VOUT to the VOUT_SNS pin.

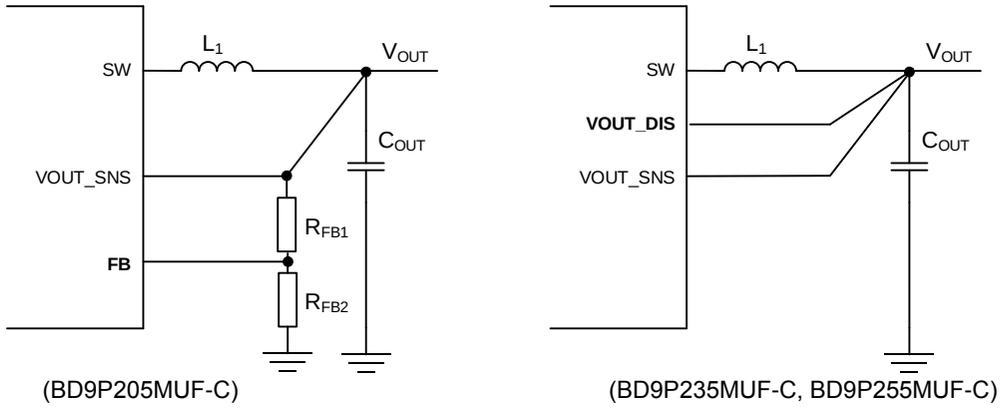
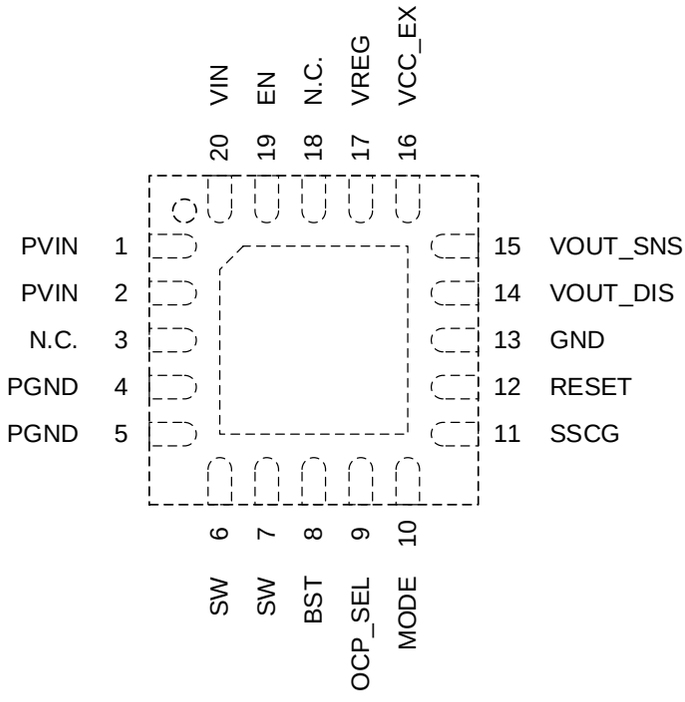


Figure 4. The Difference between BD9P205MUF-C, BD9P235MUF-C and BD9P255MUF-C

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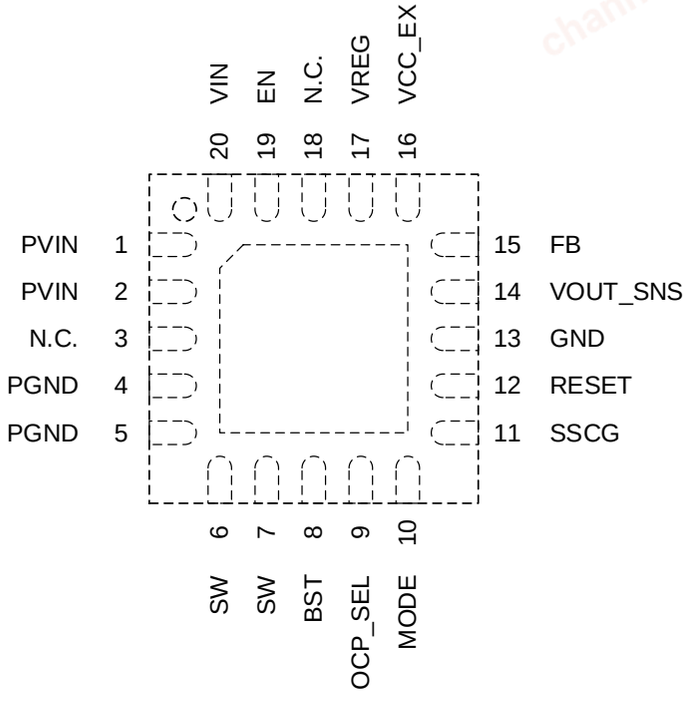
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Pin Configuration



(TOP VIEW)

Figure 5. Pin Configuration (BD9P235MUF-C, BD9P255MUF-C)



(TOP VIEW)

Figure 6. Pin Configuration (BD9P205MUF-C)

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Pin Description

Pin No.	Pin Name	Function
1, 2	PVIN	Power supply input pins that are used for the output stage of the switching regulator. Connect input ceramic capacitors referring Page 33 between the PGND pins and these pins.
3	N.C.	This pin is not connected to the chip. Use this as open. If this pin is used other than open and adjacent pins are expected to be shorted, please confirm if there is any problem with the actual application.
4, 5	PGND	Ground pins for the output stage of the switching regulator.
6, 7	SW	Switching node pins. These pins are connected to the source of the internal High Side FET and the drain of the internal Low Side FET. Connect the power inductor and the bootstrap capacitor.
8	BST	Connect a bootstrap capacitor of 0.1 µF (Typ) between this pin and the SW pins. The voltage of this capacitor is the gate drive of the High Side FET.
9	OCP_SEL	This is OCP threshold selective pin. OCP threshold is set to 2.250 A (Typ) at high, and 3.000 A (Typ) at low. These values mean the average inductor current. Connect this pin to VREG (High) or GND (Low).
10	MODE	Pin to select FPWM (Forced PWM) mode, AUTO (Automatically switched between PWM mode and LLM) mode, or SYNC (Activate synchronization) mode. In case of using FPWM mode, set high. In case of using AUTO mode, set low or open. In case of using SYNC mode, apply a clock to this pin.
11	SSCG	Pin to select Spread Spectrum function. Set high to enable Spread Spectrum and set low to disable Spread Spectrum. Connect this pin to VREG (High) or GND (Low).
12	RESET	Output reset pin with open drain. Connect a pull-up resistor to the VREG pin or the power supply within the absolute maximum voltage ratings of the RESET pin. Using a 5 kΩ to 100 kΩ resistance is recommended.
13	GND	Ground pin.
14 (BD9P235MUF-C, BD9P255MUF-C)	VOUT_DIS	This pin discharges the VOUT node. Connect this pin to the VOUT when discharge function is required. Otherwise, connect this pin to GND.
14 (BD9P205MUF-C)	VOUT_SNS	Pin to define the clamp voltage of GmAmp2 output and phase compensation. Connect this pin to the output voltage.
15 (BD9P235MUF-C, BD9P255MUF-C)		Inverting input node of the GmAmp1. This pin is used for OVP, SCP and RESET detection. And, this pin is used for defining the clamp voltage of GmAmp2 output and phase compensation. Connect this pin to the output voltage.
15 (BD9P205MUF-C)	FB	Inverting input node of the GmAmp1. This pin is used for OVP, SCP and RESET detection. Connect output voltage divider to this pin to set the output voltage.
16	VCC_EX	This pin is power supply input for internal circuit. VREG voltage is supplied from VCC_EX when voltage between 3.2 V (V_{TEXH}, Max) and 5.65 V (V_{EXOVPL}, Min) is connected to this pin. Connecting this pin to VOUT improves efficiency. In case of not use this function, connect this pin to GND.
17	VREG	Pin to output 3.3 V (Typ) for internal circuit. Connect a ceramic capacitor of 1.0 µF (Typ). Do not connect to any external loads except the OCP_SEL pin, the MODE pin, the SSCG pin and a pull-up resistor to the RESET pin.
18	N.C.	This pin is not connected to the chip. Use this as open. If this pin is used other than open and adjacent pins are expected to be shorted, please confirm if there is any problem with the actual application.
19	EN	Enable pin. Apply low level (0.8 V or less) to disable device and apply high level (2.0 V or more) to enable device. This pin must not be left open. If this pin is connected to other devices, it is recommended to insert a current limiting resistor to avoid damages caused by a short between pins.
20	VIN	Power supply input pins for the internal circuit. Connect this pin to the PVIN pins.
-	EXP-PAD	Exposed pad. The EXP-PAD is connected to the P substrate of the IC. Connect this pad to the internal PCB ground plane using multiple via holes to obtain excellent heat dissipation characteristics.

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Block Diagram

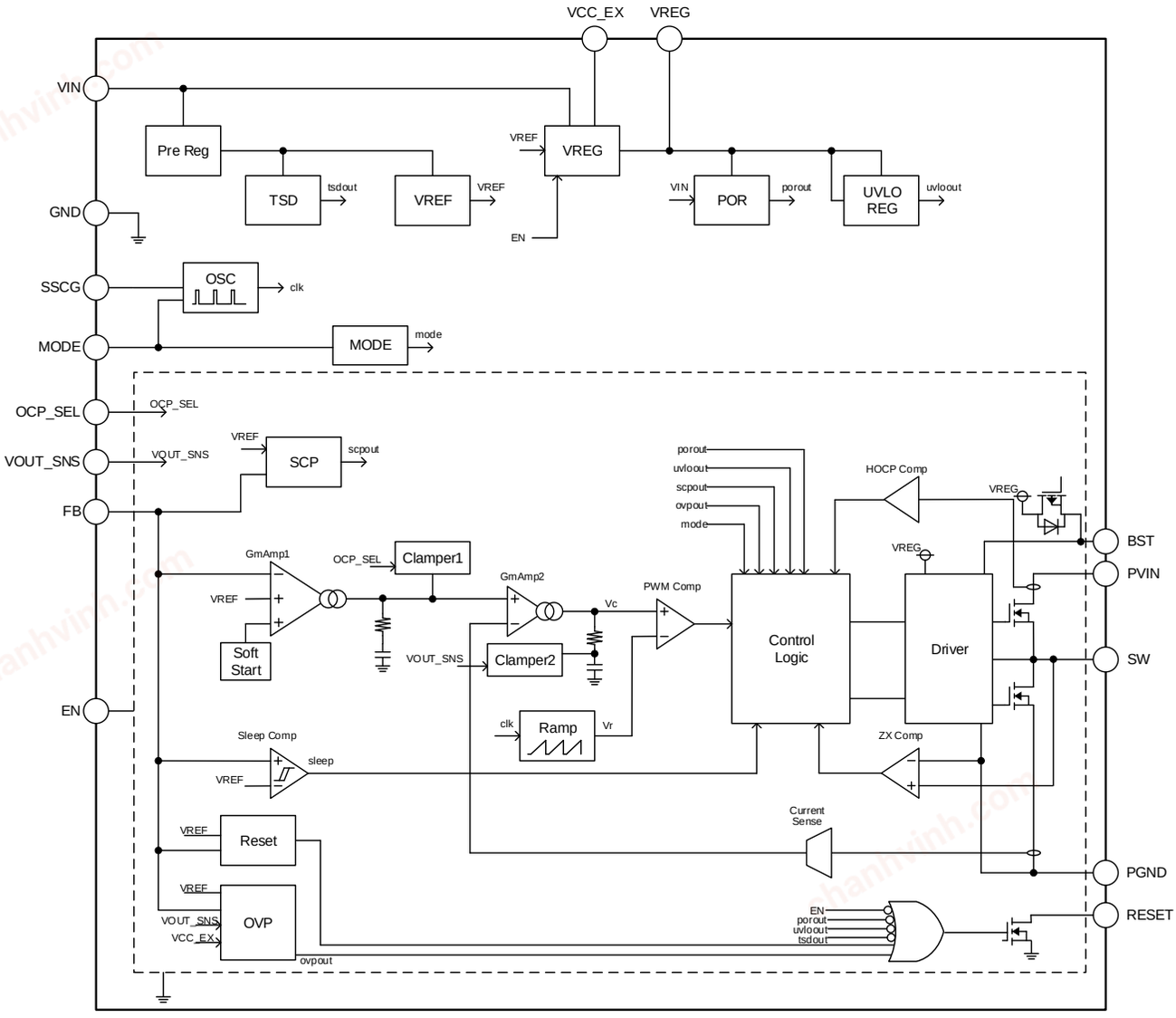


Figure 7. Block Diagram (BD9P205MUF-C)

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Block Diagram - continued

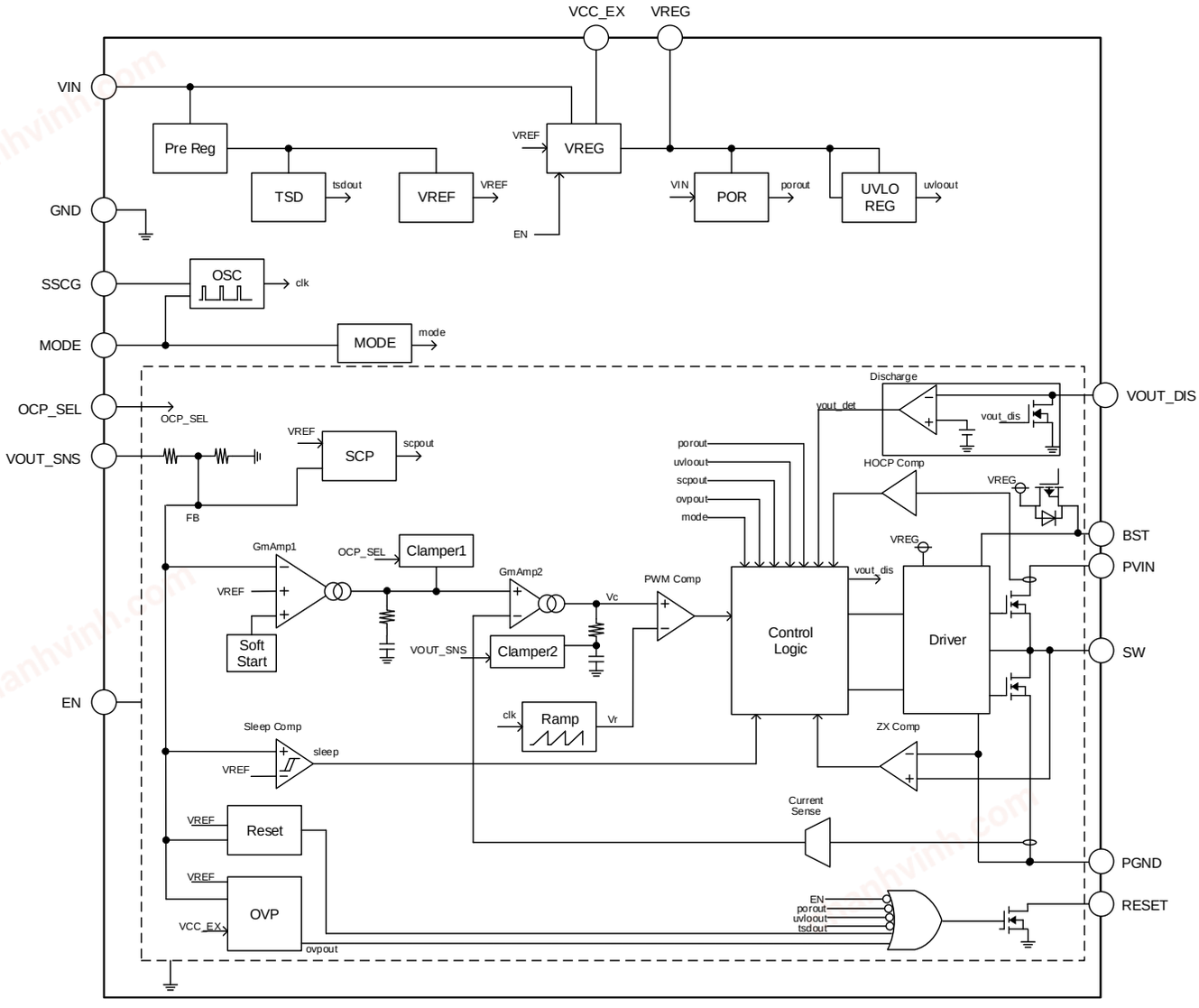


Figure 8. Block Diagram (BD9P235MUF-C, BD9P255MUF-C)

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Description of Blocks

- PreReg
  This block is the internal power supply for TSD and VREF circuits.

- VREG
  This block is the internal power supply circuit. It outputs 3.3 V (Typ) and is the power supply to the control circuit and Driver.

- TSD
  This is the thermal shutdown circuit. It will shut down the device when the junction temperature (Tj) reaches to 175 °C (Typ) or more. When the Tj falls below the TSD threshold with hysteresis of 25 °C (Typ), the circuits are automatically restored to normal operation.

- VREF
  The VREF block generates the internal reference voltage.

- POR
  The POR block is power on reset for internal logic circuit. The IC releases power on reset and starts operation with soft start when the VIN rises to 3.8 V (Typ) or more.

- UVLO REG
  The UVLO block is for under voltage lockout protection. It will shut down the device when the VREG falls to 2.85 V (Typ) or less. This protection is released when VREG voltage increase to 2.95 V (Typ) or more.

- MODE
  This block detects the MODE pin signal and controls switching mode. When the MODE pin is logic high level or is applied external clock, switching operation becomes forced PWM mode regardless load current. When the MODE pin is open or logic low level, switching operation changes between PWM and light load operation depending on load current.

- OSC
  This block generates the clock frequency. When the clock is applied to the MODE pin, it synchronizes to external clock. Connect the SSCG pin to GND to disable Spread Spectrum function and connect the SSCG pin to the VREG pin to enable it.

- OVP
  This is the output over voltage protection (OVP) circuit. When the output voltage +7.3 % (Typ) or more of the normal regulation voltage, VOUT is reduced by forced PWM switching. After output voltage falls +4.7 % (Typ) or less, the operation recovers into normal condition.

- SCP
  This is the short circuit protection circuit. After soft start is completed, the switching is disabled if the output voltage falls SCP Threshold voltage or less for 0.9 ms (Typ). This short circuit protection is maintained for 30 ms (Typ) and then automatically released.

- Soft Start
  This function starts up the output voltage taking 3 ms (Typ) to prevent the overshoot.

- GmAmp1
  This block is an error amplifier and its inputs are the reference voltage 0.8 V (Typ) and the FB voltage.

- GmAmp2
  This block sends the signal Vc which is composed of the GmAmp1 output and the current sense signal to PWM Comp.

- Clamper1
  This block clamps GmAmp1 output voltage and inductor current. It works as the over current protection and LLM control current.

- Clamper2
  This block clamps GmAmp2 output voltage.

- Current Sense
  This block detects the amount of change in inductor current through the Low Side FET and sends a current sense signal to GmAmp2.

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Description of Blocks - continued

- PWM Comp
  This block compares the output voltage of the GmAmp2 (Vc) and the saw tooth waveform (Vr) to control the switching duty.

- Ramp
  This block generates the saw tooth waveform (Vr) from the clock signal generated by OSC.

- Control Logic
  This block controls switching operation and protection functions.

- Driver
  This circuit drives the gates of the output FETs.

- Sleep Comp
  If output/feedback voltage becomes 101.3 % (Typ) or more, this block puts the device into SLEEP state. This state is released when output/feedback voltage becomes 101.0 % (Typ) or less.

- ZX Comp
  This block stops the switching by detecting reverse current of the SW current at LLM control.

- HOCP Comp
  This block detects the current flowing through the High Side FET and limits the current of 4.0 A (Min) or more. This function works in abnormal situation such as the SW pin shorted to GND condition in order to prevent the High Side FET from destruction.

- Reset
  When the output voltage reaches -4.7 % (Typ) or more of the normal regulation voltage, the open drain MOSFET connected to the RESET pin turns off in 3.6 ms (Typ) and the output of the RESET pin becomes high by its external pull-up resistor.
  When the output voltage reaches -7.2 % (Typ) or less, the RESET pin open drain MOSFET turns on and the RESET pin is pulled down with an impedance of 190 Ω (Typ).

- Discharge
  This block discharges the output voltage during EN is low and before VOUT start up. The VOUT_DIS pin is pulled down with an impedance of 75 Ω (Typ).

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V_{VIN}, V_{PVIN}	-0.3 to +42	V
EN Voltage	V_{EN}	-0.3 to +42	V
BST Voltage	V_{BST}	-0.3 to +49	V
Voltage from SW to BST	ΔV_{BST}	V_{SW} -0.3 to V_{SW} +7	V
FB, RESET, MODE, SSCG, OCP_SEL Voltage	V_{FB}, V_{RESET}, V_{MODE}, V_{SSCG} V_{OCP_SEL}	-0.3 to +7	V
VOUT_DIS Voltage	V_{VOUT_DIS}	-0.3 to +10	V
VOUT_SNS Voltage	V_{VOUT_SNS}	-0.3 to +10	V
VCC_EX Voltage	V_{VCC_EX}	-0.3 to +7	V
VREG Voltage	V_{REG}	-0.3 to +7	V
Storage Temperature Range	Tstg	-55 to +150	˚C
Maximum Junction Temperature	Tjmax	150	˚C
Human Body Model (HBM)*(Note 1)*	V_{ESD_HBM}	±2	kV

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) These voltages are guaranteed by design. Not tested.

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
VQFN20FV4040				
Junction to Ambient	θ_{JA}	120.0	38.7	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	15	8	°C/W

(Note 2) Based on JESD51-2A(Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{VIN}, V_{PVIN}	3.5	-	40	V
Operating Temperature	Ta	-40	-	+125	˚C
Output Voltage for BD9P205MUF-C *(Note 1)*	V_{OUT}	0.8	-	8.5	V
Output Voltage for BD9P235MUF-C	V_{OUT}	-	3.3	-	V
Output Voltage for BD9P255MUF-C	V_{OUT}	-	5.0	-	V
SW Minimum ON Time *(Note 2)*	t_{ONMIN}	-	-	50	ns
SW Minimum OFF Time (V_{REG} = 3.3 V)	t_{OFFMIN}	-	-	130	ns
SW Minimum OFF Time (V_{REG} = 5.0 V)	t_{OFFMIN}	-	-	100	ns
Output Current	I_{OUT}	-	-	2	A
Input Capacitor (V_{IN} Continuous Condition) *(Note 3)*	C_{IN}	2.3	-	-	µF
VREG Capacitor *(Note 3)*	C_{REG}	0.6	1.0	2.0	µF
BST Capacitor *(Note 3)*	C_{BST}	0.05	0.1	0.2	µF

(Note 1) Although the output voltage is configurable at 0.8 V or more, it may be limited by the SW min ON pulse width.
For the same reason, although the output voltage is configurable at 8.5 V and more, it may be limited by the SW minimum OFF pulse width.
For the configurable range, please refer to the Output Voltage Setting in Selection of Components Externally Connected (page 30).
(Note 2) This parameter is for 1.0 A output. Not tested.
(Note 3) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be considered. If a bulk capacitor is used with Input ceramic capacitors, please select capacitors referring page 33.

Electrical Characteristics (Unless otherwise specified Ta = -40 ˚C to +125 ˚C, V_{IN} = 12 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Shutdown Current	I_{SDWN}	-	2.1	10.0	µA	V_{EN} = 0 V, Ta = -40 ˚C to +105 ˚C
Quiescent Current from VIN	I_{Q_VIN1}	-	2.1	6.0	µA	V_{MODE} = 0 V, V_{VCC_EX} = 5 V V_{FB} = V_{FB1} x 1.04 (SLEEP)
	I_{Q_VIN2}	-	15	30	µA	V_{MODE} = 0 V, V_{VCC_EX} = 0 V V_{FB} = V_{FB1} x 1.04 (SLEEP)
	I_{Q_VIN3}	-	33	66	µA	V_{MODE} = 5 V, V_{VCC_EX} = 5 V V_{FB} =V_{FB1} x 1.04 (No SLEEP)
	I_{Q_VIN4}	-	1200	2400	µA	V_{MODE} = 5 V, V_{VCC_EX} = 0 V V_{FB} = V_{FB1} x 1.04 (No SLEEP)
Quiescent Current from VCC_EX	$I_{Q_VCC_EX1}$	-	16	60	µA	V_{MODE} = 0 V V_{FB} = V_{FB1} x 1.04 (SLEEP)
	$I_{Q_VCC_EX2}$	-	1500	3000	µA	V_{MODE} = 5 V V_{FB} = V_{FB1} x 1.04 (No SLEEP)
VIN Power On Reset Rising	V_{POR_R}	3.6	3.8	4.0	V	V_{IN} Sweep Up
VREG Under Voltage Lockout Falling	V_{UVLO_F}	2.70	2.85	3.00	V	V_{REG} Sweep Down
VREG Under Voltage Lockout Rising	V_{UVLO_R}	2.75	2.95	3.15	V	V_{REG} Sweep Up
EN/MODE/OCP_SEL/SSCG						
EN Input Voltage High	V_{ENH}	2.0	-	40	V	
EN Input Voltage Low	V_{ENL}	0	-	0.8	V	
EN Hysteresis Voltage	V_{ENHYS}	0.10	0.25	0.50	V	
EN Input Current	I_{EN}	-	0	1	µA	V_{EN} = 5 V
MODE Input Voltage High	V_{MODEH}	2.0	-	5.5	V	
MODE Input Voltage Low	V_{MODEL}	-	-	0.8	V	
MODE Input Current	I_{MODE}	-	6	10	µA	V_{MODE} = 5 V
OCP_SEL Input Voltage High	V_{SELH}	2.0	-	5.5	V	
OCP_SEL Input Voltage Low	V_{SELL}	-	-	0.8	V	
OCP_SEL Input Current	I_{SEL}	-	0	1	µA	V_{OCP_SEL} = 5 V
SSCG Input Voltage High	V_{SSCGH}	2.0	-	5.5	V	
SSCG Input Voltage Low	V_{SSCGL}	-	-	0.8	V	
SSCG Input Current	I_{SSCG}	-	0	1	µA	V_{SSCG} = 5 V

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Electrical Characteristics - continued (Unless otherwise specified Ta = -40 ˚C to +125 ˚C, V_{IN} = 12 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VREG						
VREG Voltage	V_{REG}	3.0	3.3	3.6	V	Voltage Follower V_{VCC_EX} = 0 V
VCC_EX Switch ON Resistance	R_{ONEX}	-	6	12	Ω	V_{VCC_EX} = 5 V
VCC_EX Threshold Voltage High	V_{TEXH}	2.90	3.05	3.20	V	V_{VCC_EX} Sweep Up
VCC_EX Threshold Voltage Low	V_{TEXL}	2.70	2.90	3.10	V	V_{VCC_EX} Sweep Down
VCC_EX OVP Threshold Voltage High	V_{EXOVPH}	5.85	6.20	6.55	V	
VCC_EX OVP Threshold Voltage Low	V_{EXOVPL}	5.65	6.00	6.35	V	
VOUT_DIS Discharge ON Resistance	R_{DIS}	-	75	150	Ω	V_{EN} = 0 V, V_{OUT_DIS} = 0.3 V
VOUT Discharge Deactivate Voltage	V_{DISL}	100	200	300	mV	V_{OUT_DIS} Sweep Down
Oscillator						
Switching Frequency	f_{SW}	2.0	2.2	2.4	MHz	
Synchronization Frequency Range	f_{SW_EX}	1.8	-	2.4	MHz	External Clock Input
Switching Frequency (Spread Spectrum)	f_{SWSSR}	1.90	-	2.52	MHz	V_{SSCG} = 5 V
Spread Spectrum Modulation Rate	Δf_{SSCG}	-	4.5	-	%	V_{SSCG} = 5 V
Spread Spectrum Modulation Cycle	t_{SSCG_CYCLE}	-	466	-	µs	V_{SSCG} = 5 V
VREF/GmAmp						
Feedback Reference Voltage (BD9P205MUF-C)	V_{FB1}	0.788	0.802	0.816	V	V_{FB} Voltage, PWM Mode
Enter SLEEP State Voltage (BD9P205MUF-C)	V_{FB2}	0.794	0.812	0.830	V	V_{FB} Rising, Light Load Mode
Exit SLEEP State Voltage (BD9P205MUF-C)	V_{FB3}	0.792	0.810	0.828	V	V_{FB} Falling, Light Load Mode
Output Voltage (BD9P235MUF-C)	V_{OUT_SNS1}	3.250	3.308	3.366	V	V_{OUT_SNS} Voltage, PWM Mode
Enter SLEEP State Voltage (BD9P235MUF-C)	V_{OUT_SNS2}	3.275	3.349	3.424	V	V_{OUT_SNS} Rising, Light Load Mode
Exit SLEEP State Voltage (BD9P235MUF-C)	V_{OUT_SNS3}	3.266	3.341	3.416	V	V_{OUT_SNS} Falling, Light Load Mode
Output Voltage (BD9P255MUF-C)	V_{OUT_SNS1}	4.925	5.013	5.100	V	V_{OUT_SNS} Voltage, PWM Mode
Enter SLEEP State Voltage (BD9P255MUF-C)	V_{OUT_SNS2}	4.963	5.076	5.188	V	V_{OUT_SNS} Rising, Light Load Mode
Exit SLEEP State Voltage (BD9P255MUF-C)	V_{OUT_SNS3}	4.949	5.063	5.176	V	V_{OUT_SNS} Falling, Light Load Mode
FB Input Current for BD9P205MUF-C	I_{FB}	-	0	1	µA	V_{FB} = 5 V
VOUT_SNS Input Current	I_{VOUT_SNS}	-	0.5	2.0	µA	V_{OUT_SNS} = 5 V
Start Delay Time	t_{DLY}	-	400	800	µs	
Soft Start Time	t_{SS}	2.5	3.0	3.9	ms	V_{FB1} x 0.1 to V_{FB1} x 0.9
Driver						
High Side FET ON Resistance	R_{ONH}	-	140	310	mΩ	V_{BST}-V_{SW} = 3.3 V
Low Side FET ON Resistance	R_{ONL}	-	90	210	mΩ	V_{VCC_EX} = 3.3 V
High Side FET Leakage Current	I_{LKH}	-10	0	-	µA	V_{IN} = 40 V, V_{EN} = 0 V, Ta = 25 ˚C, V_{SW} = 0 V
Low Side FET Leakage Current	I_{LKL}	-	0	10	µA	V_{IN} = 40 V, V_{EN} = 0 V, Ta = 25 ˚C, V_{SW} = 40 V
Over Current Protection Threshold	I_{OCP20}	2.400	3.000	3.600	A	V_{OCP_SEL} = 0 V
	I_{OCP15}	1.800	2.250	2.700	A	V_{OCP_SEL} = 5 V

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Electrical Characteristics - continued (Unless otherwise specified Ta = -40 ˚C to +125 ˚C, V_{IN} = 12 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Reset						
Reset Threshold Voltage Low (BD9P205MUF-C)	V_{RTL}	0.718	0.744	0.770	V	V_{FB} Sweep Down
Reset Threshold Voltage Low (BD9P235MUF-C)		3.000	3.065	3.130	V	V_{OUT_SNS} Sweep Down
Reset Threshold Voltage Low (BD9P255MUF-C)		4.550	4.650	4.750	V	
Reset Threshold Voltage High (BD9P205MUF-C)	V_{RTH}	0.738	0.764	0.790	V	V_{FB} Sweep Up
Reset Threshold Voltage High (BD9P235MUF-C)		3.08	3.16	3.24	V	V_{OUT_SNS} Sweep Up
Reset Threshold Voltage High (BD9P255MUF-C)		4.66	4.78	4.90	V	
Reset Leakage Current	I_{RSTLK}	-	0	1	µA	V_{RESET} = 5.0 V, V_{FB} = 0.8 V
Reset ON Resistance	R_{RST}	-	190	400	Ω	V_{IN} = 2 V, V_{EN} = 0 V I_{RESET} = 1 mA
Reset Active Time	$t_{RSTNACT}$	2.0	3.6	5.0	ms	
Reset Filtering Time	$t_{RSTNFILT}$	1	5	10	µs	
OVP/SCP						
FB OVP Threshold Voltage High (BD9P205MUF-C)	V_{OVPH}	0.825	0.860	0.895	V	V_{FB} Sweep Up
FB OVP Threshold Voltage Low (BD9P205MUF-C)	V_{OVPL}	0.805	0.840	0.875	V	V_{FB} Sweep Down
VOUT_SNS OVP Threshold Voltage High (BD9P205MUF-C)	$V_{SNSOVPH}$	9.0	9.5	10.0	V	V_{OUT_SNS} Sweep Up
VOUT_SNS OVP Threshold Voltage High (BD9P235MUF-C)		3.402	3.541	3.693	V	
VOUT_SNS OVP Threshold Voltage High (BD9P255MUF-C)		5.156	5.379	5.595	V	
VOUT_SNS OVP Threshold Voltage Low (BD9P205MUF-C)	$V_{SNSOVPL}$	8.5	9.0	9.5	V	V_{OUT_SNS} Sweep Down
VOUT_SNS OVP Threshold Voltage Low (BD9P235MUF-C)		3.321	3.455	3.609	V	
VOUT_SNS OVP Threshold Voltage Low (BD9P255MUF-C)		5.033	5.249	5.467	V	
SCP Threshold Voltage High (BD9P205MUF-C)	V_{SCPH}	0.68	0.72	0.76	V	V_{FB} Sweep Up
SCP Threshold Voltage High (BD9P235MUF-C)		2.81	2.97	3.14	V	V_{OUT_SNS} Sweep Up
SCP Threshold Voltage High (BD9P255MUF-C)		4.25	4.50	4.75	V	
SCP Threshold Voltage Low (BD9P205MUF-C)	V_{SCPL}	0.60	0.64	0.68	V	V_{FB} Sweep Down
SCP Threshold Voltage Low (BD9P235MUF-C)		2.48	2.64	2.81	V	V_{OUT_SNS} Sweep Down
SCP Threshold Voltage Low (BD9P255MUF-C)		3.75	4.00	4.25	V	
SCP Deactivate Rate of VIN/VOUT_SNS	V_{SCP_DACT}	1.20	1.33	1.45	V/V	SCP function is deactivated this value or less

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Typical Performance Curves

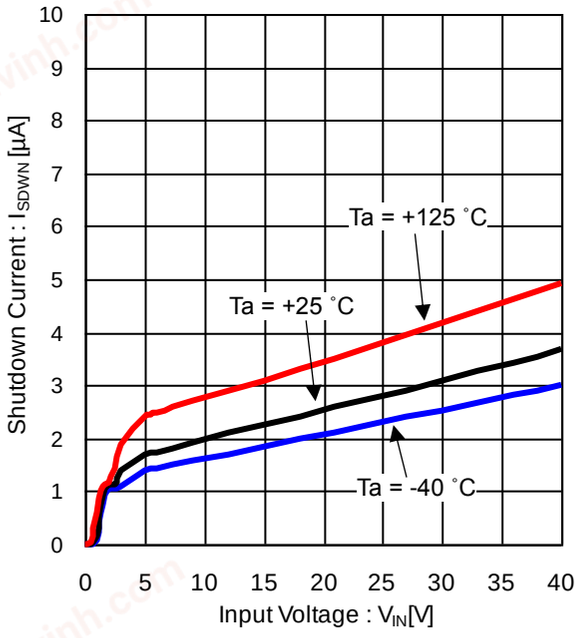


Figure 9. Shutdown Current vs Input Voltage

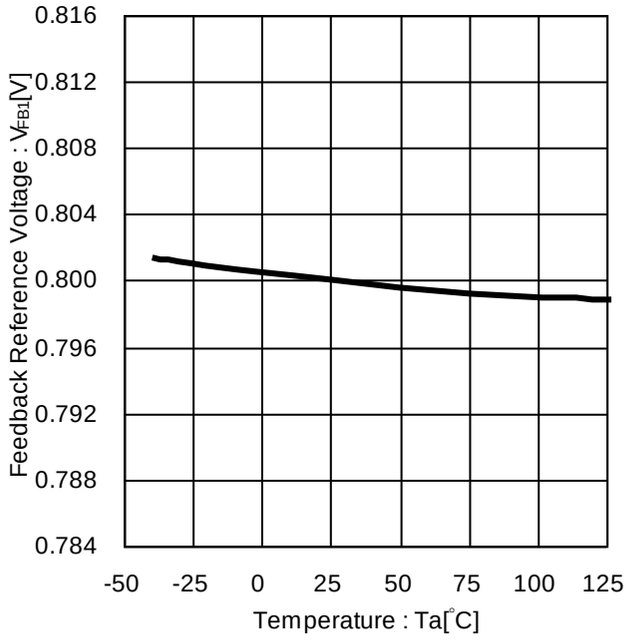


Figure 10. Feedback Reference Voltage vs Temperature
(BD9P205MUF-C)

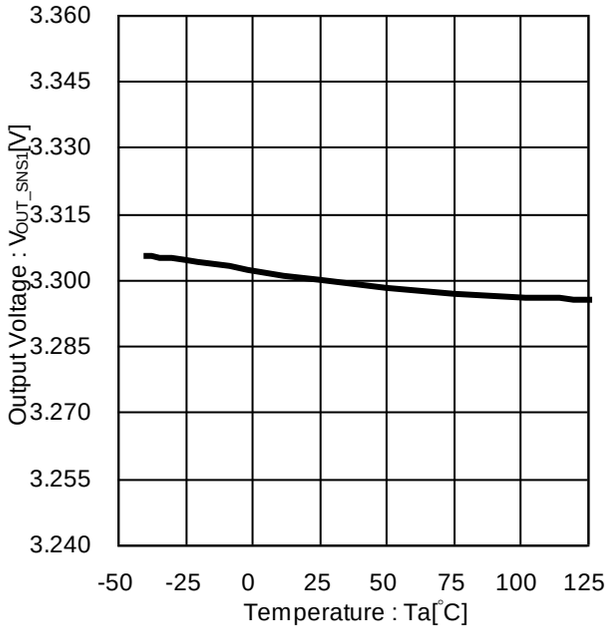


Figure 11. Output Voltage vs Temperature
(BD9P235MUF-C)

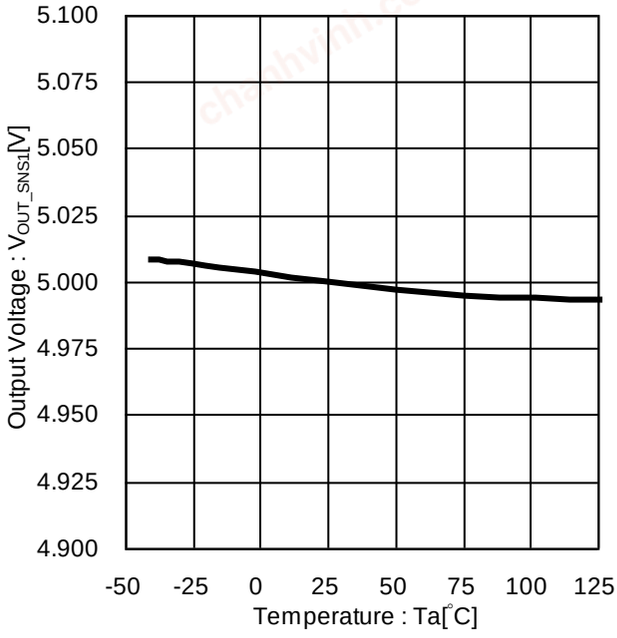


Figure 12. Output Voltage vs Temperature
(BD9P255MUF-C)

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Typical Performance Curves - continued

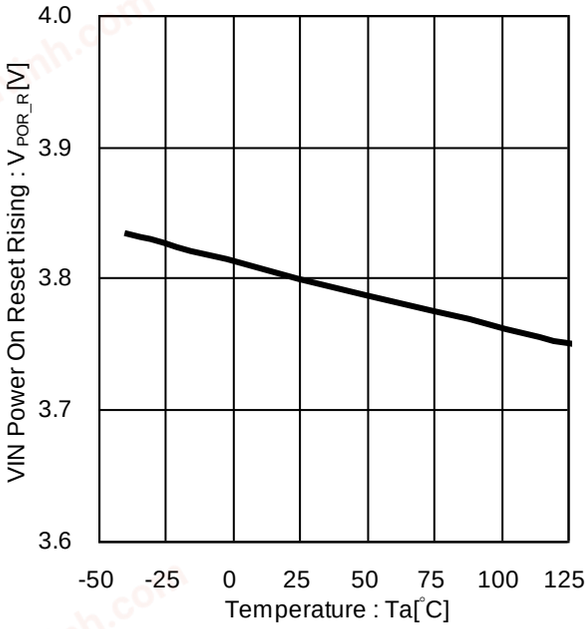


Figure 13. VIN Power On Reset Rising vs Temperature

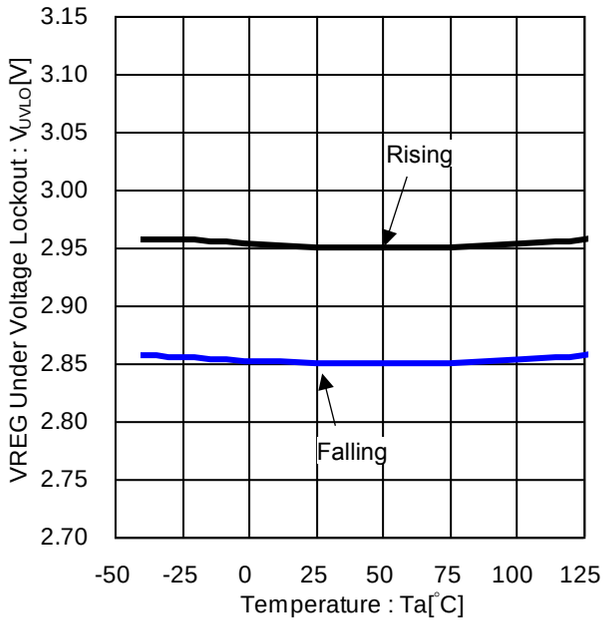


Figure 14. VREG Under Voltage Lockout vs Temperature

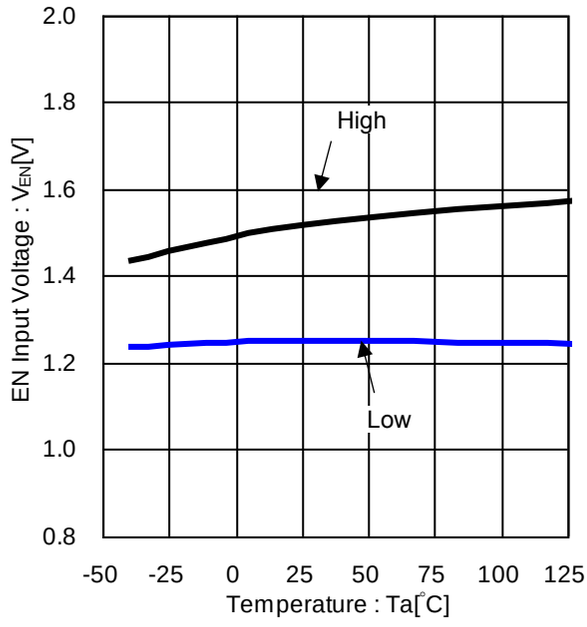


Figure 15. EN Input Voltage vs Temperature

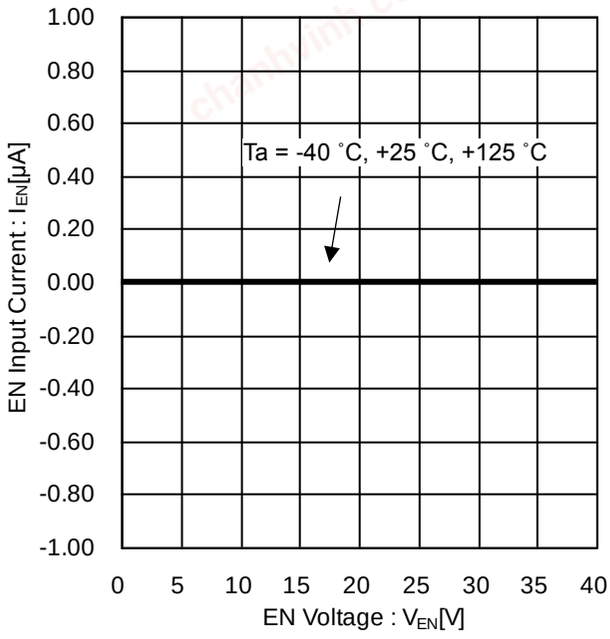


Figure 16. EN Input Current vs EN Voltage

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Typical Performance Curves - continued

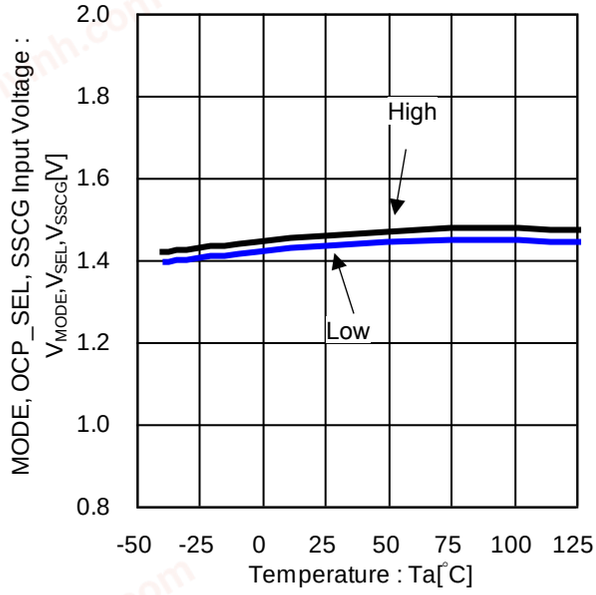


Figure 17. MODE, OCP_SEL, SSCG Input Voltage vs Temperature

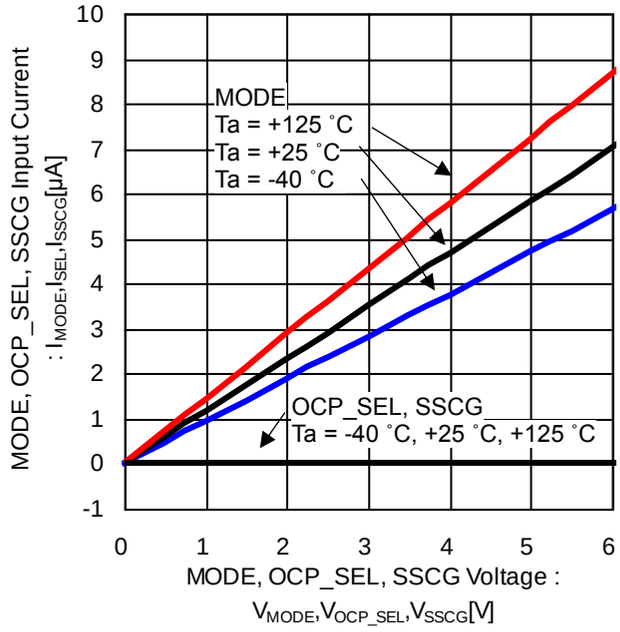


Figure 18. MODE, OCP_SEL, SSCG Input Current vs MODE, OCP_SEL, SSCG Voltage

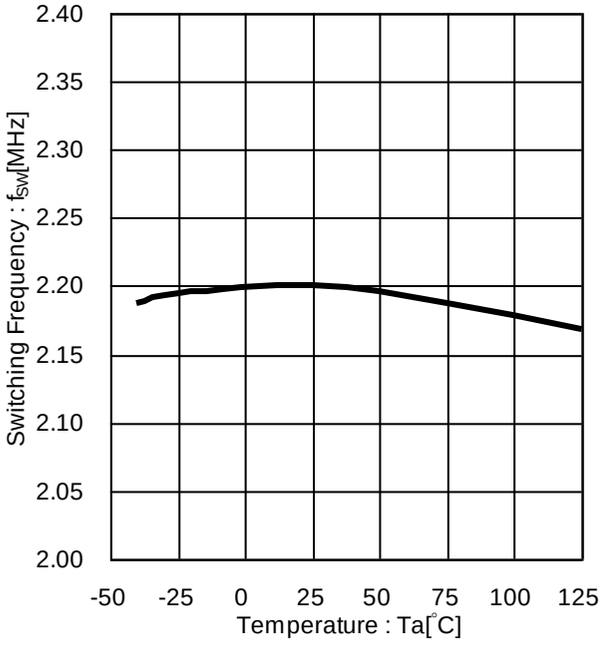


Figure 19. Switching Frequency vs Temperature

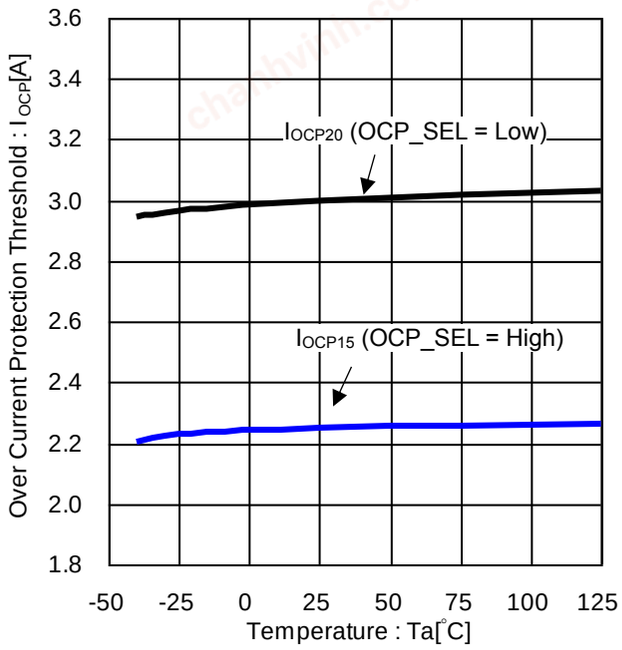


Figure 20. Over Current Protection Threshold vs Temperature

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Typical Performance Curves - continued

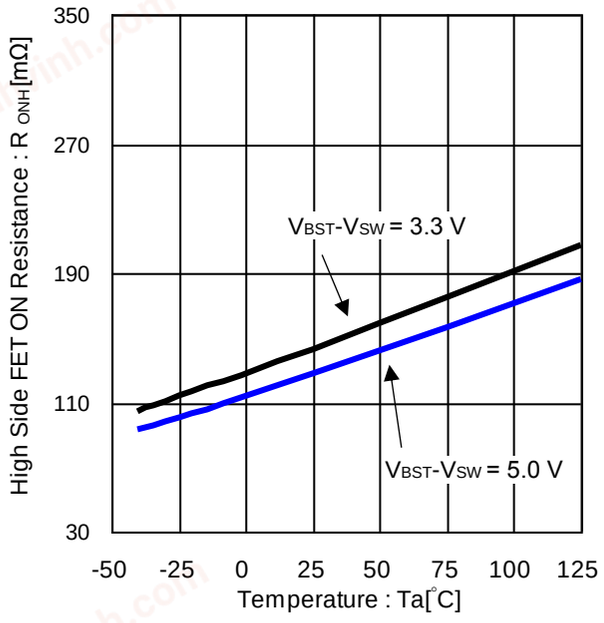


Figure 21. High Side FET ON Resistance vs Temperature

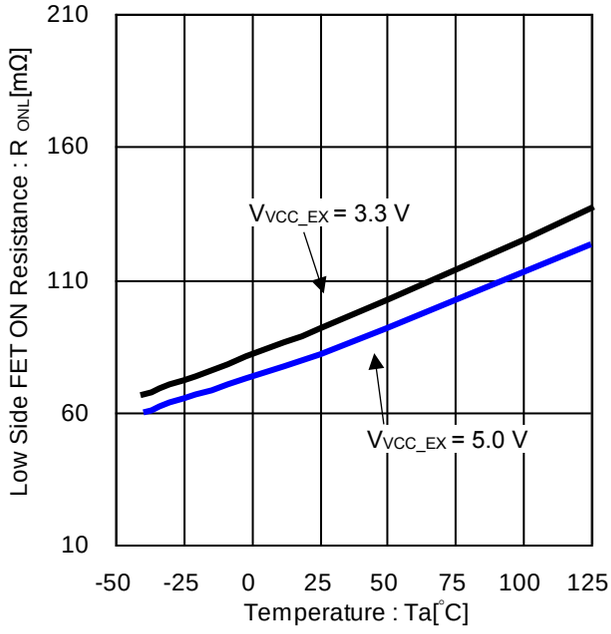


Figure 22. Low Side FET ON Resistance vs Temperature

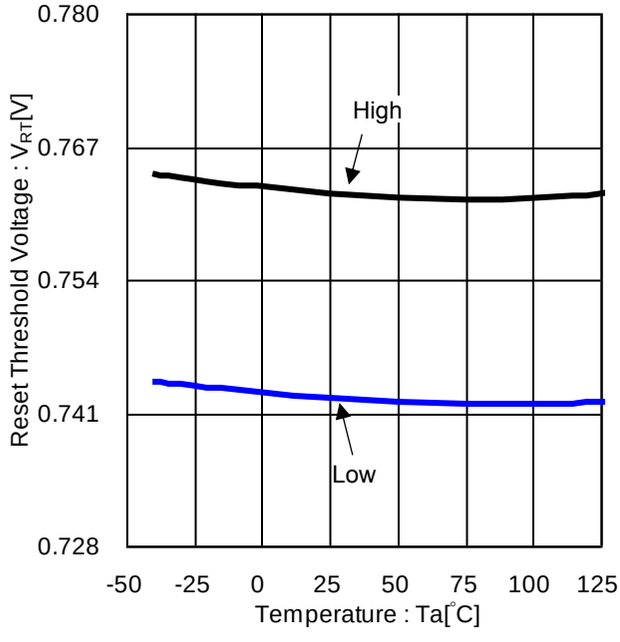


Figure 23. Reset Threshold Voltage vs Temperature (BD9P205MUF-C)

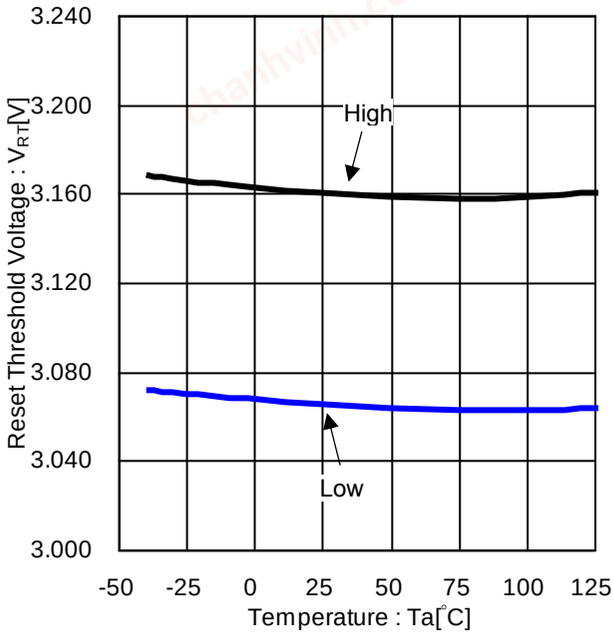


Figure 24. Reset Threshold Voltage vs Temperature (BD9P235MUF-C)

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Typical Performance Curves - continued

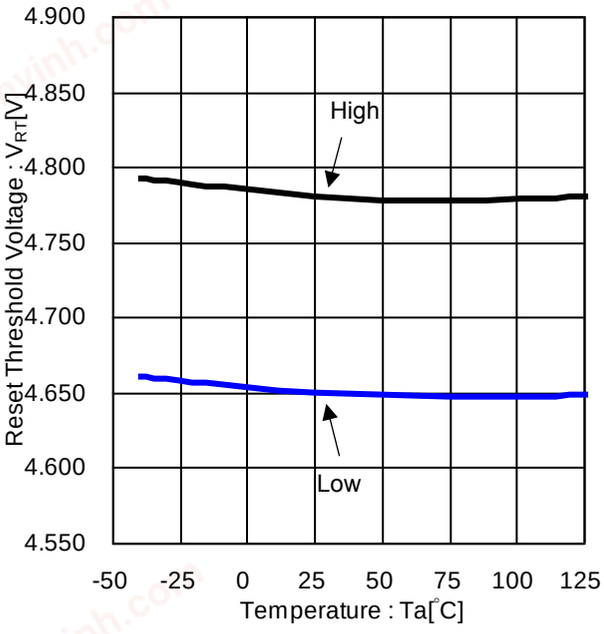


Figure 25. Reset Threshold Voltage vs Temperature
(BD9P255MUF-C)

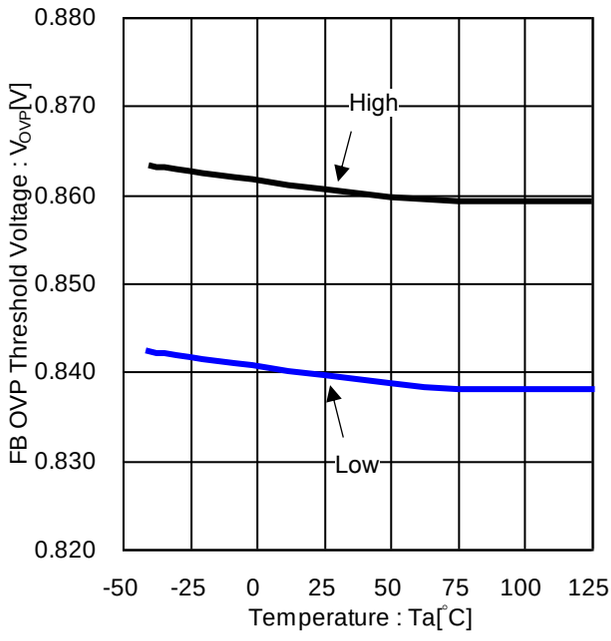


Figure 26. FB OVP Threshold Voltage vs Temperature
(BD9P205MUF-C)

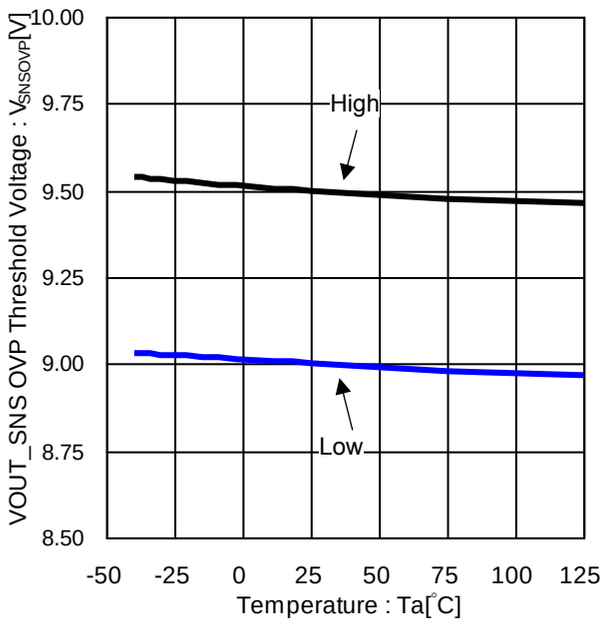


Figure 27. VOUT_SNS OVP Threshold Voltage vs Temperature
(BD9P205MUF-C)

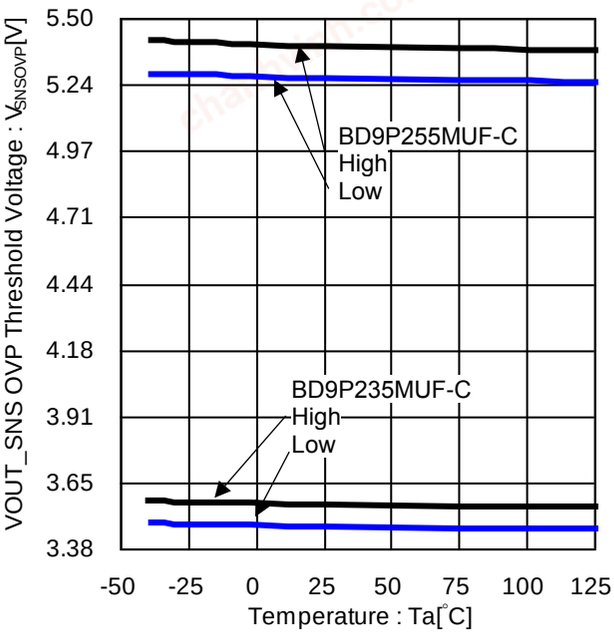


Figure 28. VOUT_SNS OVP Threshold Voltage vs Temperature
(BD9P235MUF-C/BD9P255MUF-C)

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Function Explanation

1. Nano Pulse Control™

Nano Pulse Control™ is an original technology developed by ROHM Co., Ltd. It enables to control voltage stably, which is difficult in the conventional technology, even in a narrow SW ON time such as less than 50 ns at typical condition. Narrow SW ON Pulse enables direct convert of high input voltage to low output voltage. The output voltage V_{OUT} 3.3 V can be output directly from the supply voltage V_{IN} 24 V at 2.2 MHz.

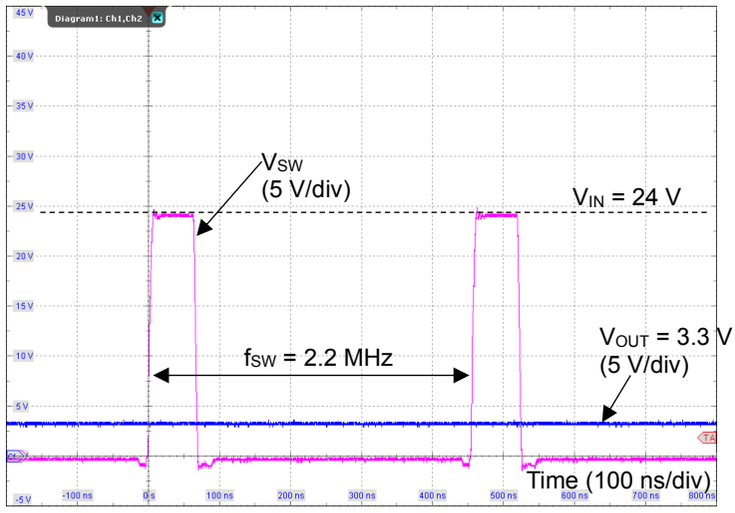


Figure 29. Switching Waveform (V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, f_{SW} = 2.2 MHz)

2. Light Load Mode Control and Forced PWM Mode Control

BD9P2x5MUF-C is a synchronous DC/DC converter with integrated POWER MOSFETs and realizes high transient response by using current mode Pulse Width Modulation (PWM) mode control architecture. Under a heavy load, the switching operation is performed with the PWM mode control at a fixed frequency. When the load is lighter, the operation is changed over to the Light Load Mode (LLM) control to improve the efficiency.

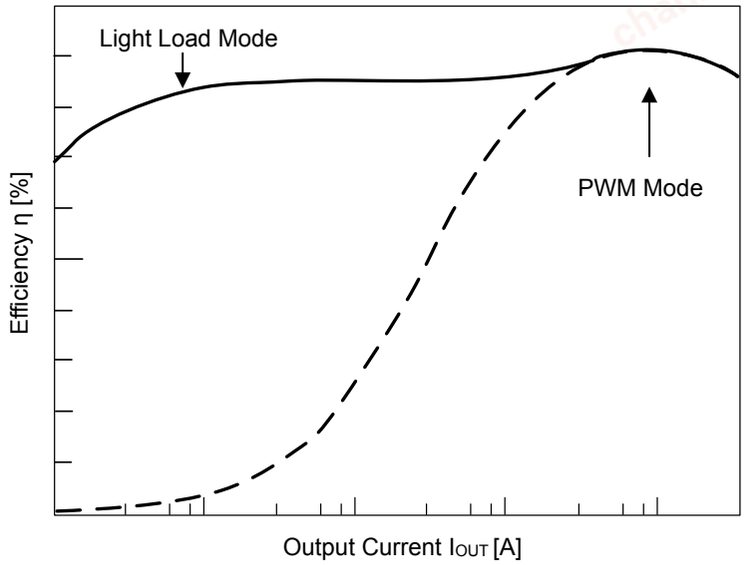


Figure 30. Efficiency (Light Load Mode, PWM Mode)

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2. Light Load Mode control and Forced PWM Mode control - continued

If the output load decreases below 400 mA (Typ) (OCP_SEL = L), the output voltage rises and power state is changed to SLEEP state when the output voltage exceeds to V_{FB2} (101.3 % of its setting voltage V_{FB1}). During SLEEP state, switching operation is stopped and the circuit current is reduced by stopping the circuit operation except for the monitor circuit of output voltage monitor. Then, the switching operation restarts when the output voltage decreases less than V_{FB3} (101.0 % of its setting voltage V_{FB1}) by the load current.

If the light load mode operation is not required, the IC operates in forced PWM mode by applying high voltage or an external clock to the MODE pin. In forced PWM mode, the IC operates with fixed frequency regardless of the output load and the ripple voltage of output can be reduced. Also, during soft start time, the IC operates in forced PWM mode regardless of the condition of the MODE pin. After detecting RESET high, the IC operates according to the MODE pin condition.

If OCP_SEL set high level, then the threshold current of switched between PWM mode and LLM is changed to 300 mA (Typ).

In addition, good EMI performance in AM band may not be provided by a load condition in LLM. To avoid this, use Forced PWM mode.

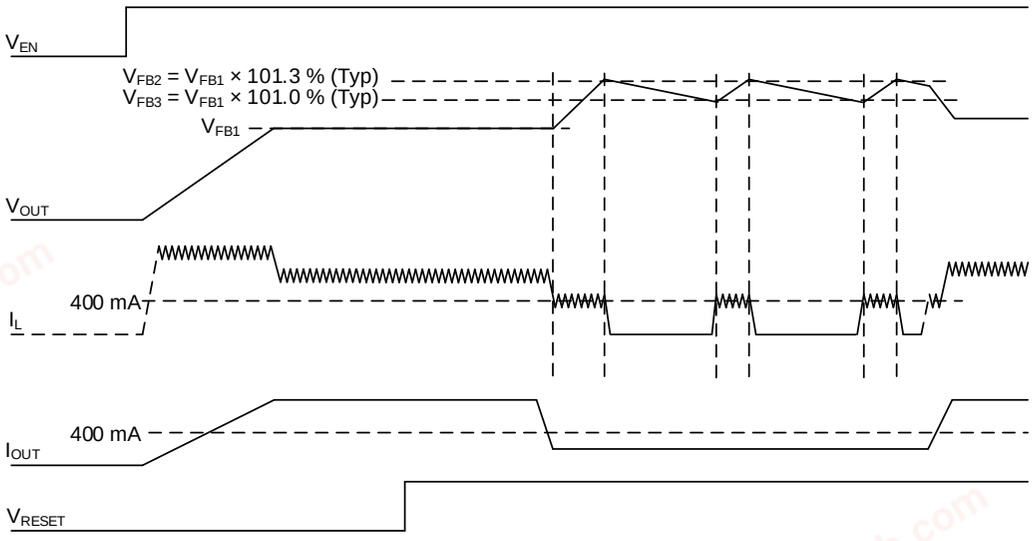


Figure 31. Timing Chart in Light Load Mode (OCP_SEL = L)

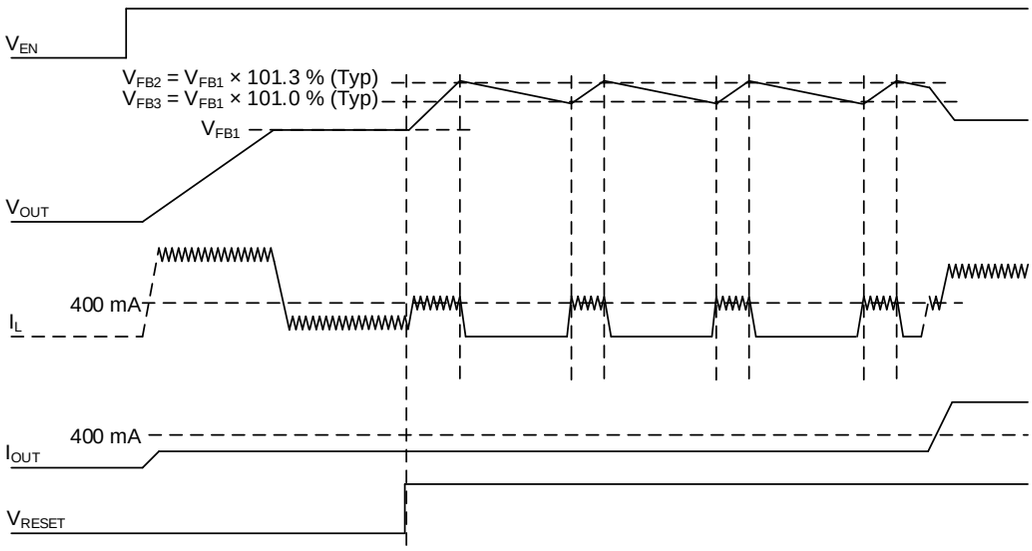


Figure 32. Timing Chart in Light Load Mode after Detecting RESET High (OCP_SEL = L)

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Function Explanation - continued

3. Enable Control

The device shutdown can be controlled by the EN pin. When V_{EN} reaches V_{ENH} (2.0 V) or more, the internal circuit is activated. When the VOUT_DIS pin is connected to output voltage and the EN pin is low, the VOUT_DIS pin is pulled down by the resistance of R_{DIS} (75 Ω, Typ) and discharges the output voltage. This discharge function is deactivated when VOUT_DIS voltage falls below V_{DISL} (200 mV, Typ) at once or 30 ms (Typ) pass after the EN pin becomes high. After being deactivated, the VOUT starts up with soft start operation. The delay time t_{DLY} (400 µs, Typ) is implemented from the EN pin becoming high to VOUT starting up regardless of VOUT_DIS voltage. The soft start time (V_{OUT} x 0.1 to V_{OUT} x 0.9) is set to t_{SS} (3.0 ms, Typ). When an EN voltage becomes V_{ENL} (0.8 V) or less, the device is shut down. When discharge function is not required, connect the VOUT_DIS pin to GND.
The discharge function is available with only BD9P235MUF-C and BD9P255MUF-C.

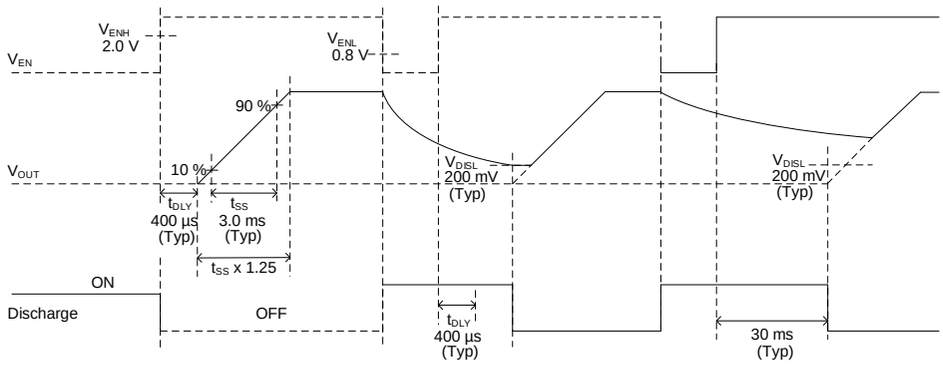


Figure 33. Enable ON/OFF Timing Chart

4. Reset Function

For BD9P205MUF-C, the reset function monitors the FB pin voltage. When the output voltage reaches V_{RTH} (95.3 %, Typ) or more of the normal regulation voltage, the open drain MOSFET on the RESET pin is turned off in $t_{RSTNACT}$ (3.6 ms, Typ) and the output of the RESET pin becomes high by its pull-up resistor. In addition, when the FB voltage reaches V_{RTL} (92.8 %, Typ) or less, the open drain MOSFET on the RESET pin is turned on and the RESET pin is pulled down with an impedance of R_{RST} (190 Ω, Typ). To reject noise, the filtering time $t_{RSTNFILT}$ (5 µs, Typ) is implemented after FB voltage decreases below its threshold voltage (V_{RTL}).
The reset function also works when output over voltage is detected. When the output voltage reaches V_{OVPH} (107.3 %, Typ) or more, the open drain MOSFET on the RESET pin is turned on. Then, when the FB voltage goes below V_{OVPL} (104.7 %, Typ) or less, the open drain MOSFET on the RESET pin is turned off. The reset active time and filtering time are activated when over voltage conditions are detected.
For BD9P235MUF-C and BD9P255MUF-C, this function monitors the VOUT_SNS pin voltage.
The RESET output voltage low level ($V_{RESET_LOW(Max)}$) when the open drain MOSFET is turned on is calculated by the following equation. It is recommended to use resistance of 5 kΩ to 100 kΩ and pull it up to the VREG pin or the power supply in the absolute maximum voltage ratings of the RESET pin.
During shutdown condition, the RESET pin is pulled down regardless the output voltage as far as V_{IN} is 2 V or more.

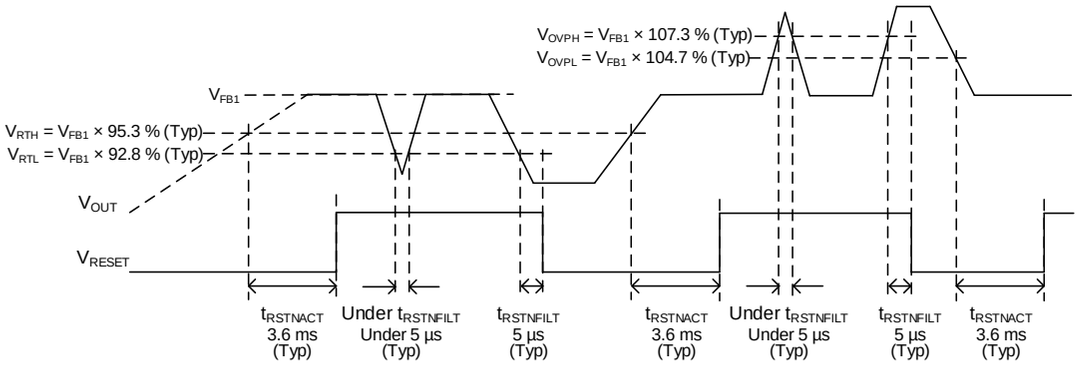


Figure 34. Reset Timing Chart (BD9P205MUF-C)

$$V_{RESET_LOW(Max)} = V_{PULL-UP} \times \frac{R_{RST(Max)}}{R_{RST(Max)} + R_{PULL-UP}} \text{ [V]}$$

Where:

$V_{RESET_LOW(Max)}$	is the RESET Low voltage level (Max) [V]
$V_{PULL-UP}$	is the Voltage of pull-up power source [V]
$R_{RST(Max)}$	is the RESET ON Resistance (Max) [Ω]
$R_{PULL-UP}$	is the value of pull-up resistor to V_{PULL_UP} [Ω]

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Function Explanation - continued

5. External Synchronization Function

By applying clock signal to the MODE pin, the switching frequency can be synchronized to the external clock signal. When clock signal is applied with the synchronization frequency range between 1.8 MHz and 2.4 MHz and the duty range between 25 % and 75 %, the Synchronous mode is started after 4 rising edges of the clock signal. In addition, this function is enabled after V_{RESET} becomes high. If the duration between each rising edge exceeds 0.9 µs (Typ) or more, the Synchronous mode is deactivated and switching operation by internal clock is activated (the Non-Synchronous mode). The Spread Spectrum function cannot be activated during the Synchronous mode.

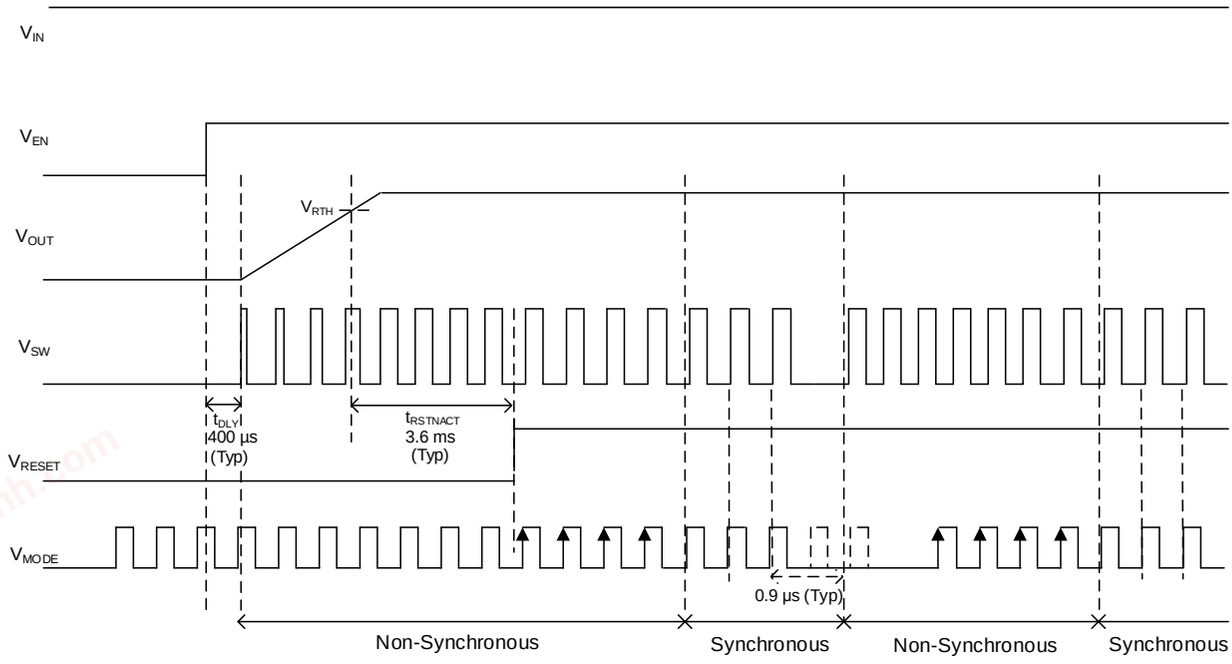


Figure 35. External Synchronization Function

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Function Explanation - continued

6. Frequency Division Function

This device drives the High Side FET with a bootstrap and requires the ON time of the Low Side FET to charge the BST pin. Therefore, the minimum OFF time of the SW pin is specified, and the output voltage is limited by the minimum OFF time under the condition in which the voltage between input and output are close. To prevent this situation, OFF pulses are skipped when the voltage between input and output are small to keep the High Side FET turned on and increase the ON duty of the SW pin. The OFF pulse skip is done for 7 consecutive switching cycles in maximum (The switching frequency becomes a one eighth of nominal frequency). In this case, the output voltage can be calculated with the following equation.

$$V_{OUT} = MaxDuty \times (V_{IN} - R_{ONH} \times I_{OUT}) - R_{DC} \times I_{OUT}$$
$$= \left(1 - t_{OFFMIN} \times \frac{f_{SW}}{8}\right) \times (V_{IN} - R_{ONH} \times I_{OUT}) - R_{DC} \times I_{OUT} \text{ [V]}$$

Where:

$MaxDuty$	is the SW pin Maximum ON Duty Cycle [%]	
V_{IN}	is the Input Voltage [V]	
R_{ONH}	is the High Side FET ON Resistance [Ω]	(Refer to page 11)
I_{OUT}	is the Output Current [A]	
R_{DC}	is the DCR of Inductor [Ω]	
t_{OFFMIN}	is the SW pin Minimum OFF Time [s]	(Refer to page 10)
f_{SW}	is the Switching Frequency [Hz]	(Refer to page 11)

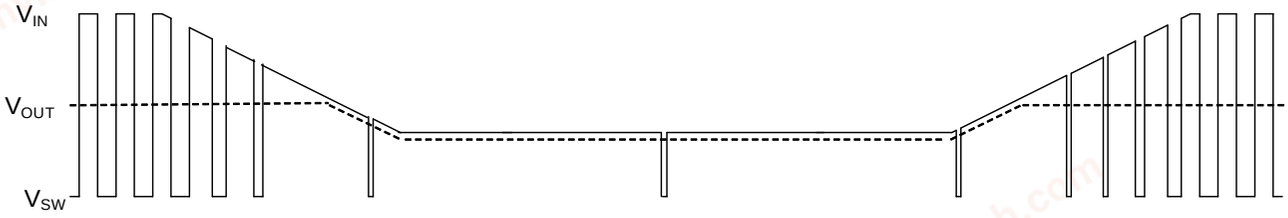


Figure 36. Frequency Division Function

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Function Explanation - continued

7. Spread Spectrum Function
Connecting the SSCG pin with the VREG pin activates the Spread Spectrum function, reducing the EMI noise level. When the Spread Spectrum function is activated, the switching frequency is varied with triangular wave of Δf_{SSCG} (±4.5 %, Typ) amplitude centered on typical frequency f_{SW} (2.2 MHz, Typ). The period of the triangular wave is t_{SSCG_CYCLE} (466 µs, Typ). However, this function is masked when the RESET output is low. Connecting the SSCG pin with GND deactivates this function.

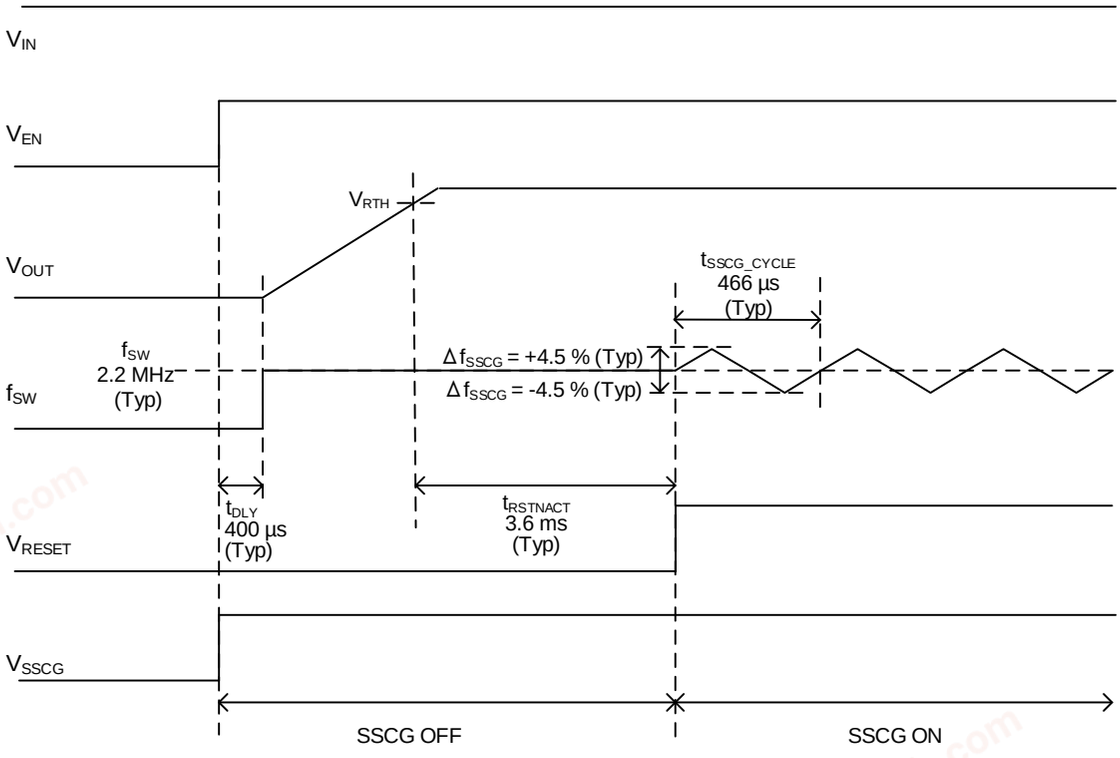


Figure 37. Spread Spectrum Function

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Function Explanation - continued

8. VCC_EX Function

This IC has the function that supplies power from VOUT to internal supply VREG to improve the efficiency. When V_{VCC_EX} goes above V_{TEXH} (3.05 V, Typ) or more, V_{REG} is supplied from the VCC_EX pin. In case of the VCC_EX pin connected with VOUT, the output voltage is used as a power supply for the internal circuitry and driver block. To protect the internal circuit, VOUT is reduced with PWM switching when VCC_EX voltage exceeds V_{EXOVPH} (6.0 V, Typ). Therefore, the VCC_EX pin connection can be used when the output voltage is in the range of between V_{TEXH} (3.2 V, Max) and V_{EXOVPL} (5.65 V, Min). Connect the VCC_EX pin with GND when VCC_EX function is not required.
The bias current I_{BIAS} using VCC_EX function can be calculated using the following formula.

$$I_{BIAS} = I_{Q_VIN1} + I_{Q_VCC_EX1} \times \frac{1}{\eta} \times \frac{V_{VCC_EX}}{V_{IN}} \text{ [µA]}$$

Where:

I_{BIAS}	is total current from VIN [µA]	
I_{Q_VIN1}	is quiescent current from VIN (without current from VCC_EX) [µA]	(Refer to page 10)
$I_{Q_VCC_EX1}$	is quiescent current from VCC_EX [µA]	(Refer to page 10)
η	is efficiency of Buck Converter.	
V_{VCC_EX}	is the VCC_EX voltage [V]	
V_{IN}	is the input voltage [V]	

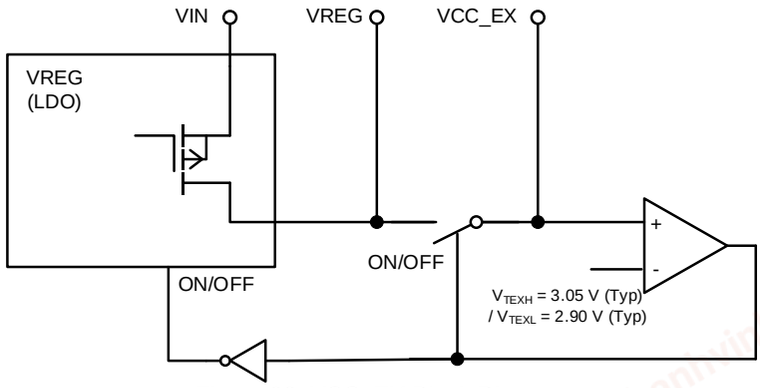


Figure 38. VCC_EX Block Diagram

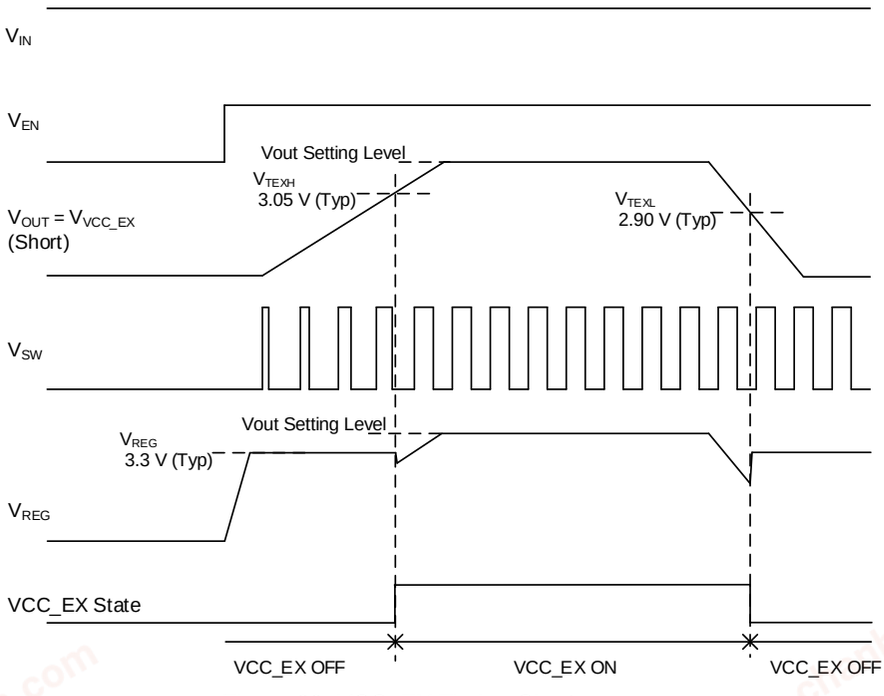


Figure 39. VCC_EX Timing Chart

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Protect Function

1. Over Current Protection (OCP)
   The Over Current Protection (OCP) monitors the average inductor current. The OCP detection level can be selected by the OCP_SEL pin. When the OCP_SEL voltage is high, it is I_{OCP15} (2.250 A, Typ) and when the OCP_SEL voltage is low, it is I_{OCP20} (3.000 A, Typ). When the average inductor current exceeds to its setting value, the duty cycle of the switching is limited and the output voltage decreases. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should never be used in applications where the protection circuit operates continuously (e.g. when a load that significantly exceeds the output current capability of the chip is connected).

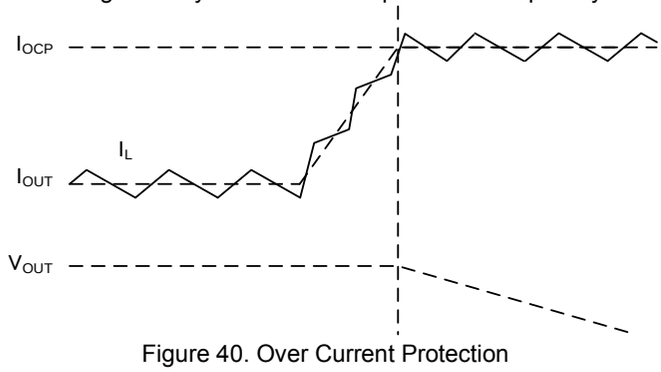


Figure 40. Over Current Protection

2. Short Circuit Protection (SCP)
   For BD9P205MUF-C, the Short Circuit Protection (SCP) block compares the FB pin voltage with the internal reference voltage VREF. When the FB pin voltage has decreased to V_{SCPL} (0.64 V, Typ) or less and remained there for 0.9 ms (Typ), SCP stops the operation for 30 ms (Typ) and subsequently initiates a restart. If the FB pin voltage decreases to V_{SCPL} (0.64 V, Typ) or less and increases to V_{SCPH} (0.72 V, Typ) or more within 0.9 ms afterwards, SCP protection is released and output voltage recovers to normal operation. For BD9P235MUF-C and BD9P255MUF-C, the SCP block monitors the VOUT_SNS pin for the protection. SCP detection voltage V_{SCPL} is 80 % (Typ) of normal output voltage. On the other hand, SCP release voltage V_{SCPH} is 90 % (Typ) of normal output voltage.
   The SCP function is deactivated during 7 ms (Typ) from VOUT starting up. In addition, when VIN decreases and VOUT also decreases, the SCP function is deactivated not to detect short circuit protection. The SCP function is likewise deactivated when VIN voltage is lower than V_{SCP_DACT} (133 %, Typ) of the VOUT_SNS pin voltage, and then is activated after 7 ms (Typ) from VIN voltage exceeds V_{SCP_DACT} (133 %, Typ) of the VOUT_SNS pin voltage. Therefore, in the case of short circuit from VIN close to VOUT condition, SCP stops the switching operation after 7.9 ms (Typ) from short circuit. However, the device should never be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected).

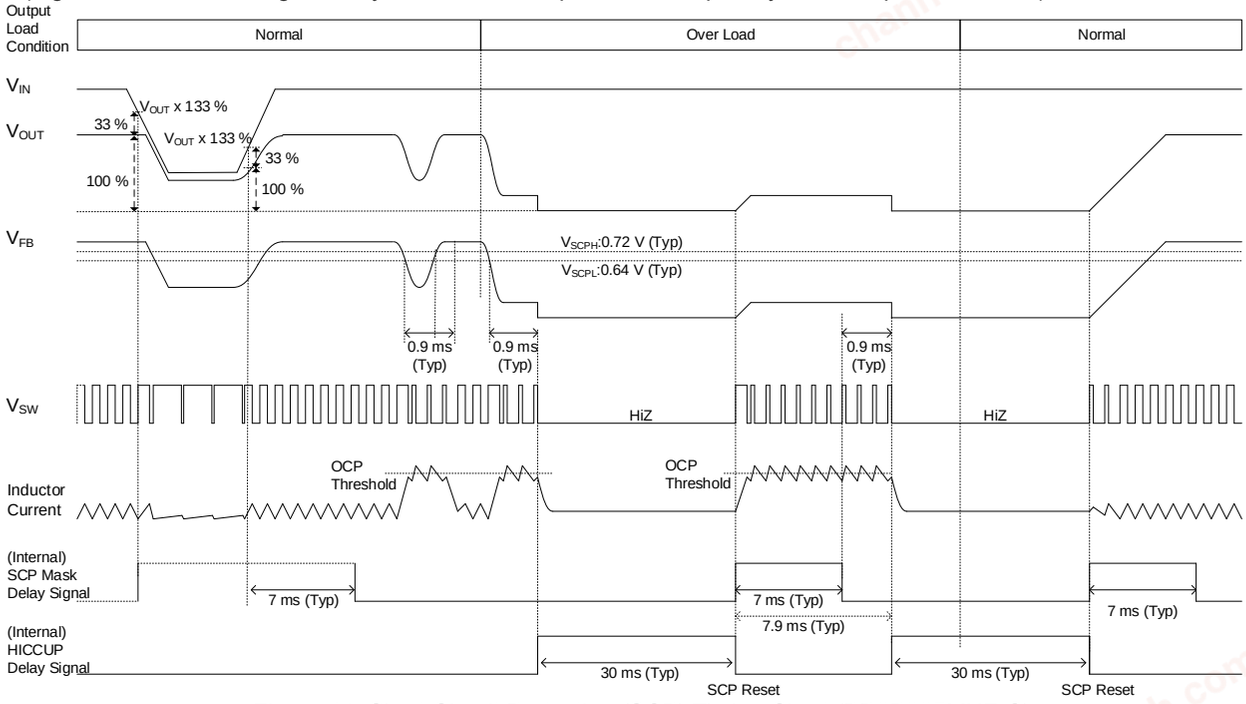


Figure 41. Short Circuit Protection (SCP) Timing Chart (BD9P205MUF-C)

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Protect Function - continued

3. Power On Reset (POR)/Under Voltage Lockout Protection (UVLO)
   The UVLO and POR are integrated to prevent the malfunction when the power supply voltage is decreased. The POR monitors the VIN pin voltage. On the other hand, UVLO monitors the VREG pin voltage.
   In the sequence of VIN rising, the VREG pin voltage also rises up to 3.3 V (Typ) following VIN voltage. First, UVLO is released when VREG voltage increase above V_{UVLO_R} (2.95 V, Typ). Next, POR is released when VIN voltage increase above V_{POR_R} (3.8 V, Typ). When both POR and UVLO are released, the IC starts up with soft start.
   In the sequence of VIN falling, VREG voltage also falls. When VREG voltage decreases below V_{UVLO_F} (2.85 V, Typ), UVLO is detected and puts the IC goes into standby state. At the same time, POR is detected. When the VCC_EX pin is connected to VOUT, VREG voltage supplied from VCC_EX. In this case, drop voltage between VIN and VREG becomes larger than the case of VCC_EX connected to GND because VOUT voltage is restricted by maximum duty at low VIN condition. Therefore, UVLO is detected at higher VIN condition than the case when the VCC_EX pin is connected to GND.

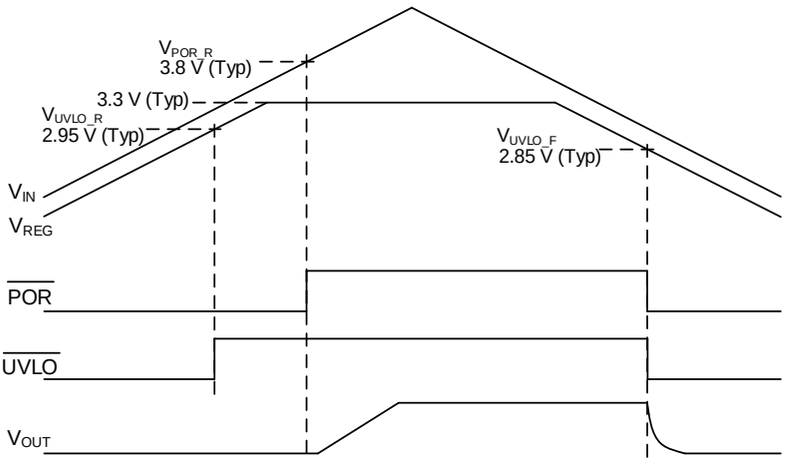


Figure 42. POR/UVLO Timing Chart

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Protect Function - continued

4. Thermal Shutdown (TSD)
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. If junction temperature (Tj) exceeds TSD detection temperature (175 °C, Typ), the POWER MOSFETs are turned off. When the Tj falls below the TSD temperature (150 °C, Typ), the IC restarts up with soft start. Where the input voltage required for the restart is the same as that for the initial startup (Input voltage 4.0 V or more). Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

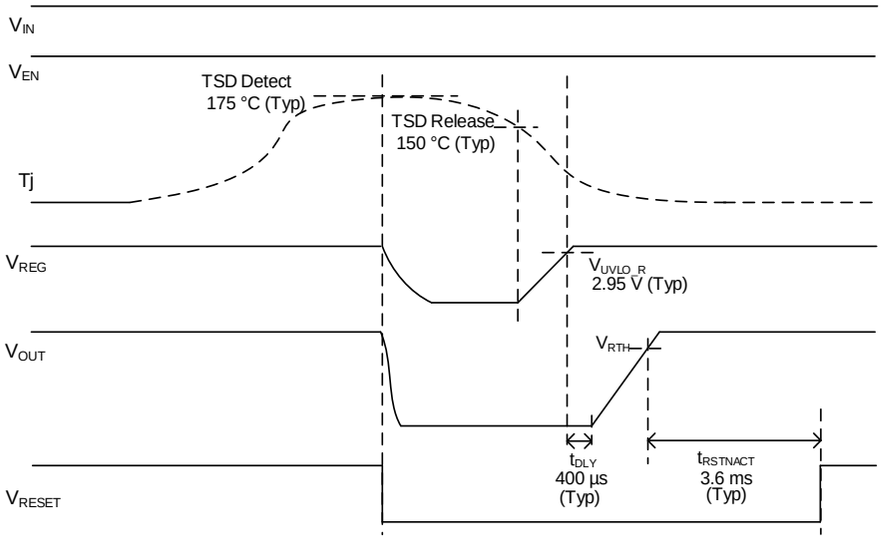


Figure 43. TSD Timing Chart

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Protect Function - continued

5. Over Voltage Protection (OVP)
This IC has Over Voltage Protection (OVP) monitoring FB to prevent the increase of output voltage in case of external injected current to VOUT. When FB voltage exceeds V_{OVPH} (107.3 % of its setting voltage V_{FB1}), the switching regulator sinks current from VOUT by changing state to PWM. The sink current during OVP is restricted to I_{NCP} (2.500 A, Typ) (OCP_SEL = L). In addition, the RESET pin is pulled down to GND during OVP detection. To prevent the malfunction by noise, the internal delay $t_{RSTNFILT}$ of 5 µs (Typ) is implemented after OVP detection. When FB voltage falls below V_{OVPL} (104.7 % of its setting voltage V_{FB1}), OVP function is released. The RESET pin is kept low and PWM switching is also kept during $t_{RSTNACT}$ (3.6 ms, Typ) after OVP function is released. When OCP_SEL is set high level, then I_{NCP} value is changed to I_{NCP} (1.875 A, Typ).
If the FB pin is open, this IC cannot regulate VOUT correctly. In this case, if VOUT voltage exceeds $V_{SNSOVPH}$ or VCC_EX voltage exceed V_{EXOVPH}, the VOUT is pulled down by PWM switching to protect internal devices same as the situation that the FB pin over voltage is detected.

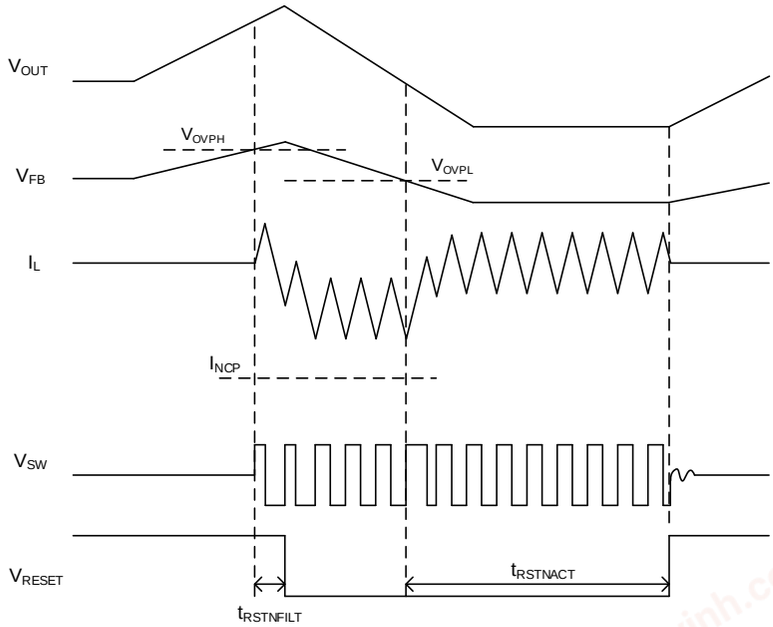


Figure 44. FB OVP Timing Chart

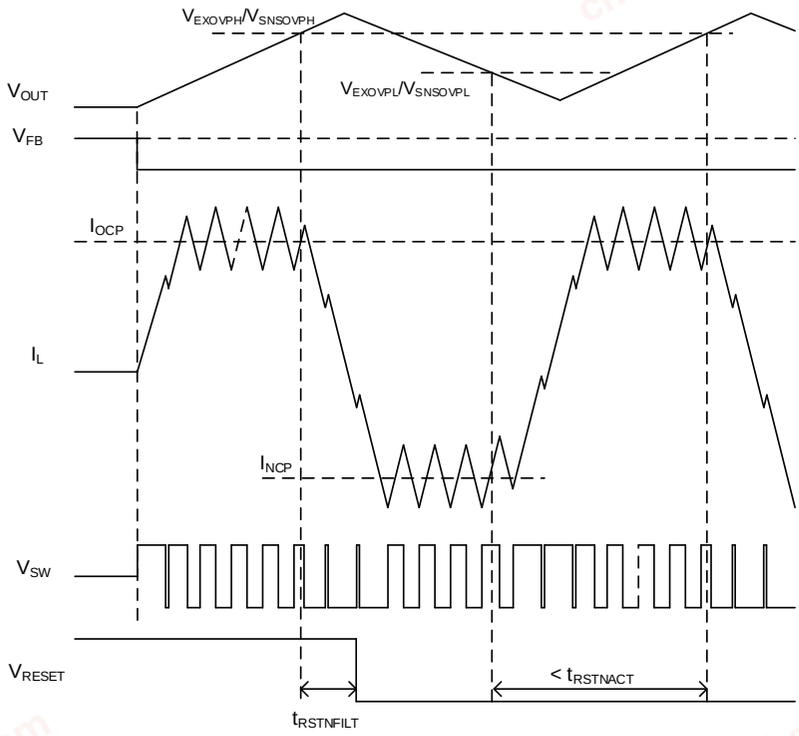


Figure 45. VCC_EX/VOUT_SNS OVP Timing Chart

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5. Over Voltage Protection (OVP) - continued

If VOUT is shorted to the Battery Line as following figure, the DC/DC converter (BD9P2x5MUF-C) sinks current from VOUT to the Low Side FET. If a Reverse Polarity Protection Diode is on the Battery Line, the VIN voltage results in being boosted up and might exceed the absolute maximum ratings.

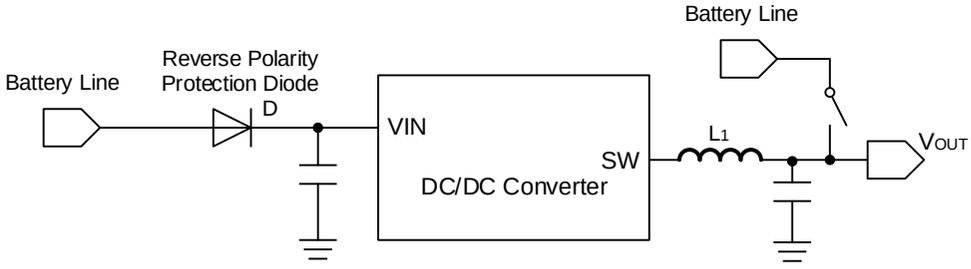


Figure 46. VOUT Shorted to Battery Line

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Selection of Components Externally Connected

Contact us if not use the recommended constant in the application circuit.

Necessary parameters in designing the power supply are as follows:

Table 1. Application Sample Specification

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	3.5 V to 40 V
Output Voltage	V_{OUT}	5.0 V
Output Ripple Voltage	ΔV_{P-P}	20 mV_{p-p}
Output Current	I_{OUT}	Typ 1.0 A/Max 2.0 A
Switching Frequency	f_{SW}	2.2 MHz
Operating Temperature Range	Ta	-40 °C to +125 °C

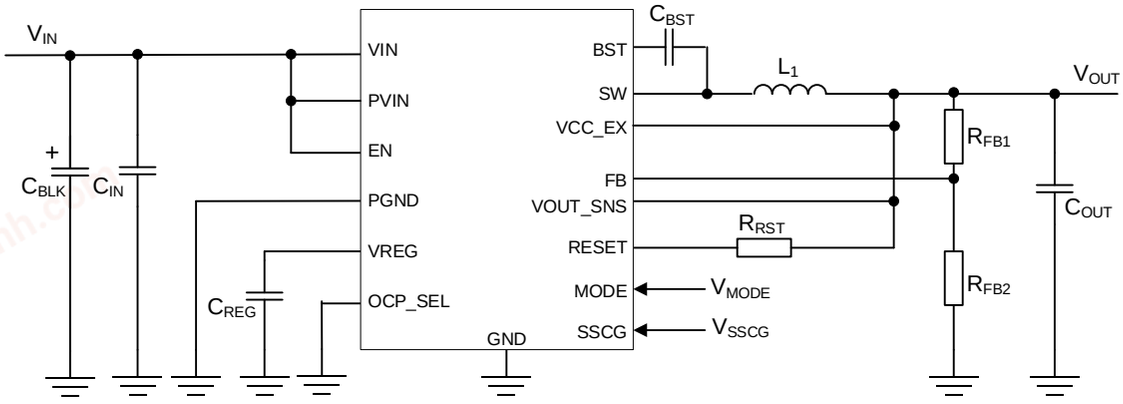


Figure 47. Application Sample Circuit

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Selection of Components Externally Connected - continued

1. Selection of the Inductor L_1 value

The inductor in the switching regulator supplies a continuous current to the load and functions as a filter to smooth the output voltage. In current mode control, the sub-harmonic oscillation may happen. The slope compensation circuit is integrated into the IC to prevent the sub-harmonic oscillation. The sub-harmonic oscillation depends on the rate of increase of output switch current. If the inductor value is too small, the sub-harmonic oscillation may happen because the inductor ripple current ΔI_L is increased. If the inductor value is too large, the feedback loop may not achieve stability because the inductor ripple current ΔI_L is decreased.
The recommended inductor value for each output voltage and OCP_SEL pin setting is shown below.

Table 2. Recommended Inductor Value

Output voltage	OCP_SEL	Maximum output current	Inductor value
1.1 V < V_{OUT}	L	2.0 A	3.3 µH
	H	1.5 A	4.7 µH
V_{OUT} ≤ 1.1 V	L	2.0 A	4.7 µH
	H	1.5 A	6.8 µH

The peak to peak inductor current is shown by the following equation:

$$\Delta I_L = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times f_{SW}\times L} \text{ [A]}$$

Where:

V_{IN} is the input voltage [V]
V_{OUT} is the output voltage [V]
f_{SW} is the switching frequency [Hz]
L is the inductor value [H]

ΔV_{P-P} (Output peak-to-peak ripple voltage) is shown in the following equation.

$$\Delta V_{P-P} = \Delta I_L \times ESR + \frac{\Delta I_L}{8\times C_{OUT}\times f_{SW}} \text{ [V]} \quad \text{(a)}$$

Where:

ESR is the equivalent series resistance of the output capacitor [Ω]
C_{OUT} is the output capacitance [F]
f_{SW} is the switching frequency [Hz]

The shielded type (closed magnetic circuit type) is the recommended type of inductor to be used. It is important not to magnetic saturate the core in any situation, so please make sure that the definition of rated current is different according to the manufactures. Please check the rated current at maximum ambient temperature of application to inductor manufacturer.

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Selection of Components Externally Connected - continued

2. Selection of Output Capacitor C_{OUT}

The output capacitor is selected based on the ESR that is required from the previous page equation (a). ΔV_{P-P} can be reduced by using a capacitor with a small ESR.

The ceramic capacitor is the best option that meets this requirement. It is because not only it has a small ESR but the ceramic capacitor also contributes to the size reduction of the application circuit. Please confirm the frequency characteristics of ESR from the datasheet of the capacitor manufacturer, and consider a low ESR value for the switching frequency being used. It is necessary to consider that the capacitance of the ceramic capacitor changes obviously according to DC biasing characteristic. For the voltage rating of the ceramic capacitor, twice or more the maximum output voltage is usually required. By selecting a high voltage rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristics of X7R or better is recommended. Because the voltage rating of a large ceramic capacitor is low, the selection becomes difficult for an application with high output voltage. In that case, please connect multiple ceramic capacitors.

These capacitors are rated in ripple current. The RMS values of the ripple current that can be obtained in the following equation and must not exceed the ripple current rating.

$$I_{COUT(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \text{ [A]}$$

Where:

$I_{COUT(RMS)}$ is the value of the ripple electric current [A]

Next, when the output setting voltage is 3.3 V or more, it is recommended that the output ceramic capacitor C_{OUT} is 44 µF (Typ) or more for OCP_SEL = L and 32 µF (Typ) or more for OCP_SEL = H. When the output setting voltage less than 3.3 V, the output ceramic capacitor C_{OUT} is recommended to the following equation.

Table 3. Output Ceramic Capacitor Recommended Capacitance Value

OCP_SEL	$V_{OUT} \geq 3.3$ V	1.1 V < V_{OUT} < 3.3 V	$V_{OUT} \leq 1.1$ V
L	$C_{OUT} \geq 44$ [µF]	$C_{OUT} \geq \frac{145.2}{V_{OUT}}$ [µF]	$C_{OUT} \geq \frac{217.8}{V_{OUT}}$ [µF]
H	$C_{OUT} \geq 32$ [µF]	$C_{OUT} \geq \frac{105.6}{V_{OUT}}$ [µF]	$C_{OUT} \geq \frac{126.7}{V_{OUT}}$ [µF]

When selecting the capacitor ensure that the capacitance C_{OUT_WORST} of the following equation is maintained at the characteristics of DC Bias, AC Voltage, temperature, and tolerance.

Table 4. Output Ceramic Capacitor Minimum Capacitance Value

OCP_SEL	$V_{OUT} \geq 3.3$ V	1.1 V < V_{OUT} < 3.3 V	$V_{OUT} \leq 1.1$ V
L	$C_{OUT} \geq 30$ [µF]	$C_{OUT} \geq \frac{99.0}{V_{OUT}}$ [µF]	$C_{OUT} \geq \frac{148.5}{V_{OUT}}$ [µF]
H	$C_{OUT} \geq 20$ [µF]	$C_{OUT} \geq \frac{66.0}{V_{OUT}}$ [µF]	$C_{OUT} \geq \frac{100.0}{V_{OUT}}$ [µF]

If the capacitance falls below this value, the oscillation may happen. When using the electrolytic capacitor and the conductive polymer hybrid aluminum electrolytic capacitor, please place it in addition to the ceramic capacitors with the capacity described above. Actually, the changes in the frequency characteristic are greatly affected by the type and the condition (temperature, etc.) of parts that are used, the wire routing and layout of the PCB. Please confirm stability and responsiveness in actual application. And please place PCB patterns that allows C_{OUT} adjustment from the initial design in case of insufficient stability and responsiveness.

In addition, for the total value of capacitance in the output line $C_{OUT(Max)}$, please choose a capacitance value less than the value obtained by the following equation:

$$C_{OUT(Max)} < \frac{t_{SS(Min)} \times 1.25 \times (I_{OCP(Min)} - I_{OUT_START(Max)})}{V_{OUT}} \text{ [F]}$$

Where:

$I_{OCP(Min)}$ is the OCP operation current (Min) [A]

$t_{SS(Min)}$ is the Soft Start Time (Min) [s]

$I_{OUT_START(Max)}$ is the maximum load current during startup [A]

V_{OUT} is the output voltage [V]

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Selection of Components Externally Connected - continued

3. Selection of Input Capacitor C_{IN}, C_{BLK}
For input capacitors, there are two types of capacitor: decoupling capacitors C_{IN} and bulk capacitors C_{BLK}.
Ceramic capacitors with total values 2.3 µF or more are necessary for the decoupling capacitors C_{IN} for ripple noise reduction. If a low ESR electrolytic capacitor with large capacitance is connected parallel to the decoupling capacitors as a bulk capacitor, ceramic capacitors with 0.5 µF or more are necessary for the decoupling capacitors. (However, to reduce EMI noise level, 2.3 µF or more are recommended for ceramic capacitors.) These capacitor values including device variation, temperature characteristics, DC bias characteristics, and aging change must be larger than minimum value. It is effective for switching noise reduction to place one of ceramic capacitor close to the PVIN and the VIN pins. The voltage rating of the capacitors is recommended to be 1.2 times or more the maximum input voltage, or twice the normal input voltage. Also, the IC might not operate properly when the PCB layout or the position of the capacitor is not good. Please check “PCB Layout Design” on page 48.

   The bulk capacitor is optional. The bulk capacitor prevents the decrease in the line voltage and serves as a backup power supply to keep the input voltage constant. A low ESR electrolytic capacitor with large capacitance is suitable for the bulk capacitor. It is necessary to select the best capacitance value for each of application. In that case, please take note not to exceed the rated ripple current of the capacitor.

   The RMS value of the input ripple current $I_{CIN(RMS)}$ is obtained in the following equation:

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left\{ {I_{OUT(Max)}}^2 \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + \frac{1}{12} \times {\Delta I_L}^2 \right\}} \text{ [A]}$$

   Where:
   $I_{OUT(Max)}$ is the output current (Max) [A]

   In addition, in automotive and other applications requiring high reliability, it is recommended to connect the capacitors in parallel to accommodate multiple electrolytic capacitors and minimize the chances of drying up. For ceramic capacitors, it is recommended to make two series + two parallel structures to decrease the risk of capacitor destruction due to short circuit conditions.

   When the impedance on the input side is high for some reason (because the wiring from the power supply to the VIN pin is long, etc.), then high capacitance is required. In actual conditions, it is necessary to verify that there are no problems like IC is turned off, or the output overshoots due to the change in V_{IN} at transient response.

4. Selection of the Bootstrap Capacitor
For Bootstrap capacitor C_{BST}, please connect a 0.1 µF (Typ) ceramic capacitor as close as possible between the BST pin and the SW pin.

5. Selection of the VREG Capacitor.
For VREG capacitor C_{REG}, please connect a 1.0 µF (Typ) ceramic capacitor between the VREG pin and GND.

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Selection of Components Externally Connected - continued

6. Selection of Output Voltage Setting Resistor R_{FB1}, R_{FB2} (BD9P205MUF-C)

For the BD9P205MUF-C, the output voltage is set with output voltage setting resistors R_{FB1} and R_{FB2}. The reference voltage of GmAmp1 is set to 0.8 V and the IC operates to regulate the FB pin voltage to 0.8 V. The output voltage is defined by the formula (1). R_{FB1} and R_{FB2} should be adjusted to set the required output voltage. If R_{FB1} and R_{FB2} are large, the current flowing through on these resistors is small and the circuit current at no load can be reduced. However, the phase shift is likely to happen because of the parasitic capacitance of IC and PCB on the FB pin. Therefore, the combined resistance $R_{FB1}//R_{FB2}$ should be set to 100 kΩ or less. If the combined resistance $R_{FB1}//R_{FB2}$ is 100 kΩ or more, C_{FB1} and C_{FB2} should be chosen to satisfy the formula (2). In this case, the value of C_{FB1} and C_{FB2} should be chose the capacitor of 47 pF or more that is much larger than C_P.

$$V_{OUT} = \frac{R_{FB1}+R_{FB2}}{R_{FB2}} \times 0.8 \text{ [V]} \quad (1)$$

$$\frac{R_{FB1} \times C_{FB1}}{R_{FB2} \times C_{FB2}} \approx 1 \quad (2)$$

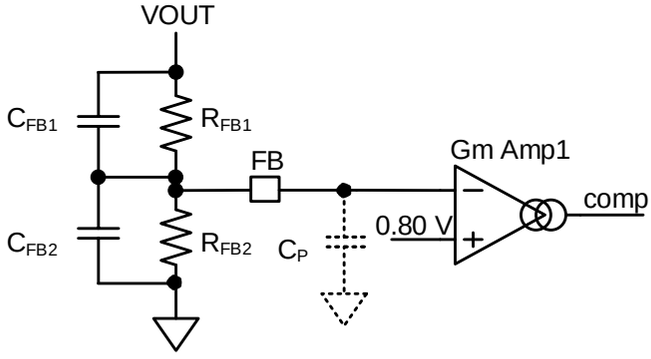


Figure 48. Setting for Output Setting Resistor

The changes in the frequency characteristic are greatly affected by the type and the condition (temperature, etc.) of parts that are used. Please ensure a phase margin of 45° or more and a gain margin of 5 dB or more in actual application. If it cannot ensure, C_{FB1} and C_{FB2} should be chosen to satisfy the following equation as a guide. Please place PCB patterns that allows C_{FB1} and C_{FB2} adjustment from the initial design in case of insufficient stability and responsiveness.

$$C_{FB1} \leq \frac{8000}{R_{FB1}} \text{ [pF]}$$

$$C_{FB1} \times \left(\frac{R_{FB1}}{R_{FB2}}\right) \leq C_{FB2} \leq C_{FB1} \times \left(\frac{5 \times R_{FB1}}{R_{FB2}} + 4\right) \text{ [pF]}$$

Where:

R_{FB1} is the output voltage setting resistors [kΩ]

R_{FB2} is the output voltage setting resistors [kΩ]

If the voltage between input and output increases and the ON time of the SW decreases to under t_{ONMIN}, the switching frequency is decreased. To ensure stable switching frequency, the output voltage must satisfy the following equation. If this equation is not satisfied, the SW pulse is skipped. In this case, the switching frequency decreases and the output voltage ripple increases.

$$V_{OUT} \geq V_{IN(Max)} \times f_{SW(Max)} \times t_{ONMIN(Max)} \text{ [V]}$$

Where:

$V_{IN(Max)}$ is the Input Voltage (Max) [V]

$f_{SW(Max)}$ is the Switching Frequency (Max) [Hz] (Refer to page 11)

$t_{ONMIN(Max)}$ is the SW Minimum ON time (Max) [s] (Refer to page 10)

If the voltage between input and output decreases, the ON time of the SW increases by skipping the off time and the switching frequency is decreased. To keep switching frequency stably, the following equation must be satisfied.

$$V_{OUT} \leq V_{IN(Min)} \times (1 - f_{SW(Max)} \times t_{OFFMIN(Max)}) \text{ [V]}$$

Where:

$t_{OFFMIN(Max)}$ is the SW Minimum OFF Time (Max) [s] (Refer to page 10)

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Application Examples 1

Table 5. Specification Example 1

Parameter	Symbol	Specification Case
Product Name	IC	BD9P205MUF-C
Input Voltage	V_{IN}	8 V to 18 V
Output Voltage	V_{OUT}	6.0 V
Output Current	I_{OUT}	Typ 1.0 A / Max 2.0 A
Operating Temperature Range	Ta	-40 °C to +125 °C

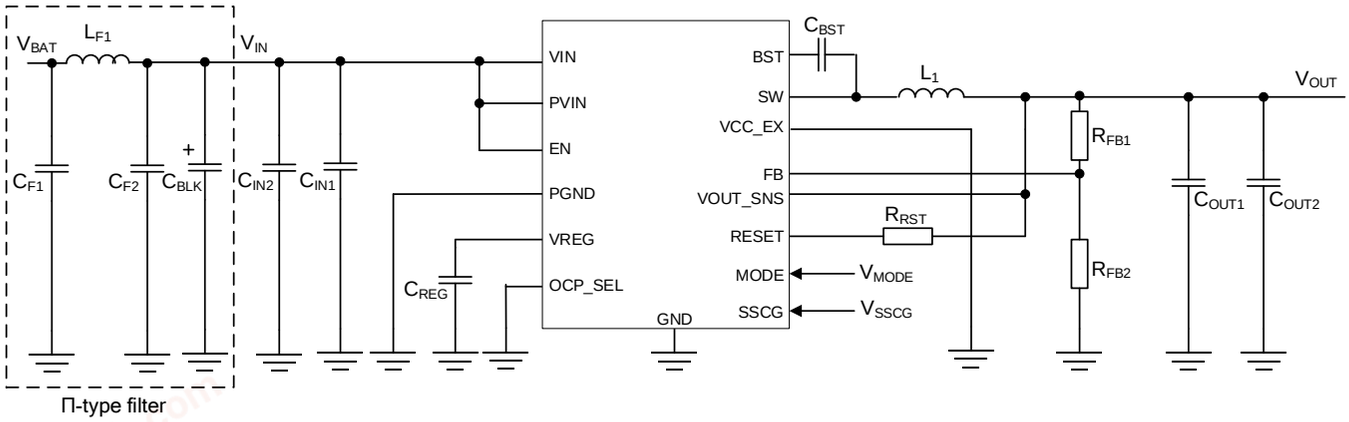


Figure 49. Reference Circuit 1

Table 6. Application Example 1 Parts List with π-type Filter

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1} *(Note 1)*	3216	1 µF, X7R, 50 V	GCJ31MR71H105K	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK
C_{F2}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{BLK}	φ10 mm x L10 mm	220 µF, 35 V	UWD1V221MCL1GS	Electrolytic capacitor	NICHICON
C_{IN2} *(Note 1)*	3216	1 µF, X7R, 50 V	GCJ31MR71H105K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	2012	1 µF, X7R, 16 V	GCM21BR71C105K	Ceramic	MURATA
C_{BST}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
R_{RST}	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip resistor	ROHM
L_1	W6.0 x H4.5 x L6.3 mm^3	3.3 µH	CLF6045NIT-3R3N-D	Inductor	TDK
C_{OUT1}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT2}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
R_{FB1}	1005	130 kΩ, 1 %, 1/16 W	MCR01MZPF1303	Chip resistor	ROHM
R_{FB2}	1005	20 kΩ, 1 %, 1/16 W	MCR01MZPF2002	Chip resistor	ROHM

(Note 1) To reduce EMI noise level, 4.7 µF, (3225, X7R, 50 V, GCM32ER71H475K) is recommended for C_{F1} and C_{IN2}.

Table 7. Application Example 1 Parts List without π-type Filter

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1}	-	Open	-	-	-
L_{F1}	-	Open	-	-	-
C_{F2}	-	Open	-	-	-
C_{BLK}	-	Open	-	-	-
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA

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Application Examples 1 - continued

(Ta = 25 °C)

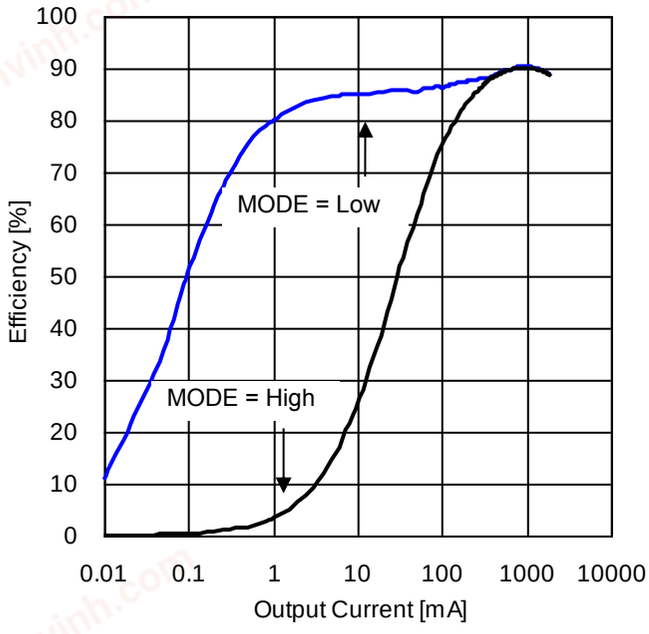


Figure 50. Efficiency vs Output Current
(V_{IN} = 12 V)

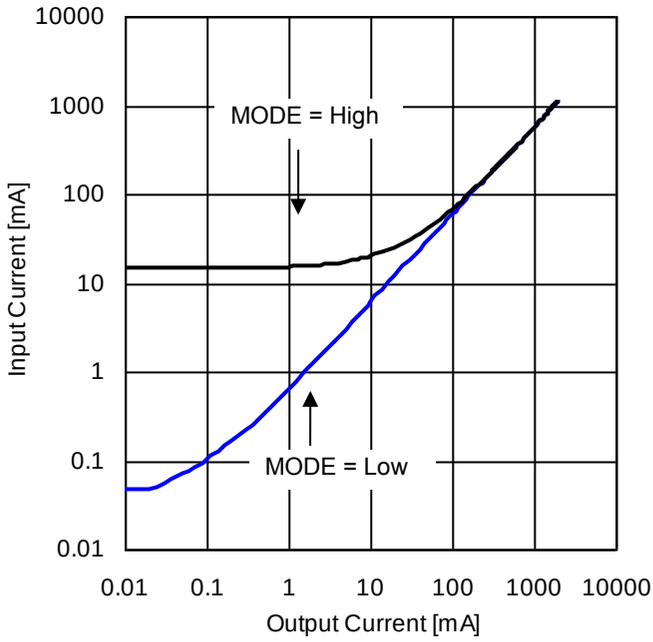


Figure 51. Input Current vs Output Current
(V_{IN} = 12 V)

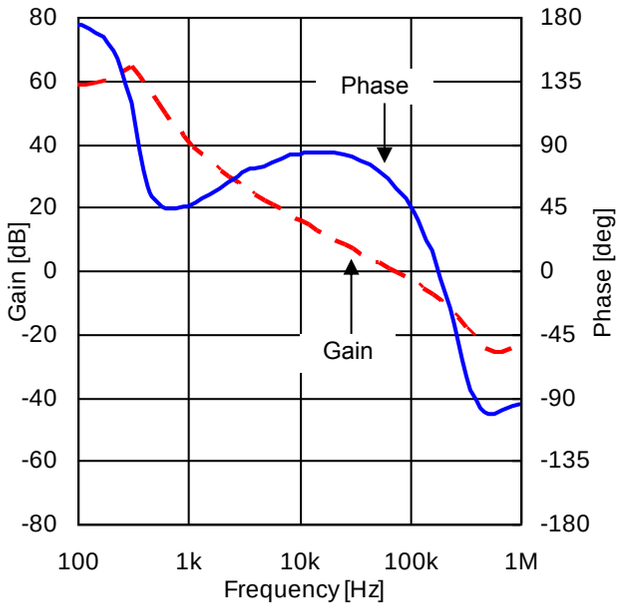


Figure 52. Frequency Characteristic
(V_{IN} = 12 V, I_{OUT} = 1.0 A)

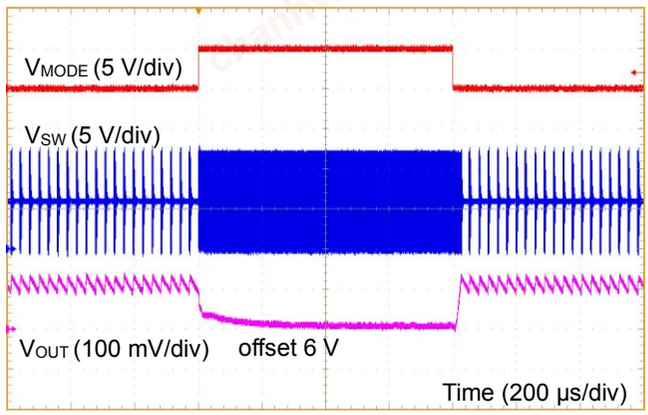


Figure 53. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

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Application Examples 1 - continued

(Ta = 25 °C)

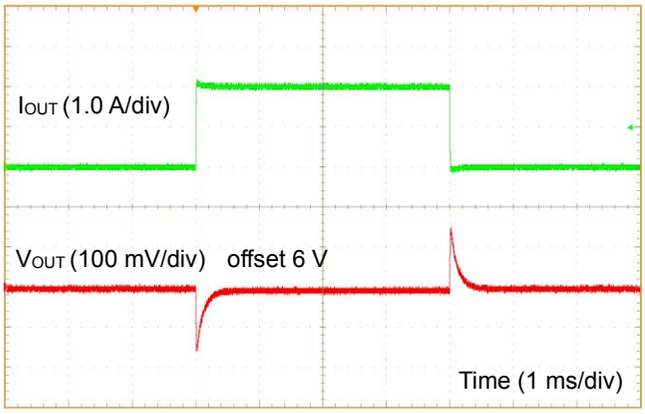


Figure 54. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 2 A)

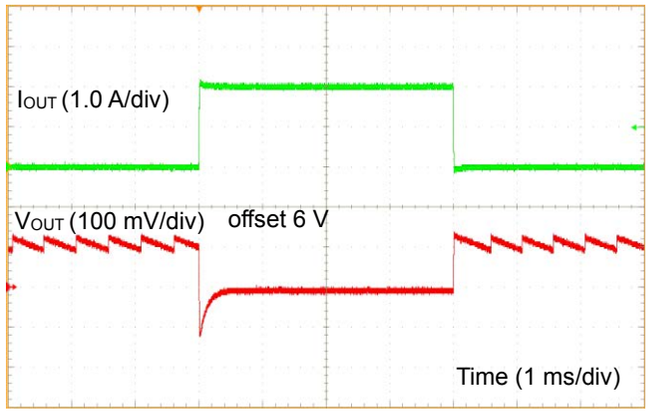


Figure 55. Load Response 2
(V_{IN} = 12 V, V_{MODE} = 0 V, I_{OUT} = 0 A to 2 A)

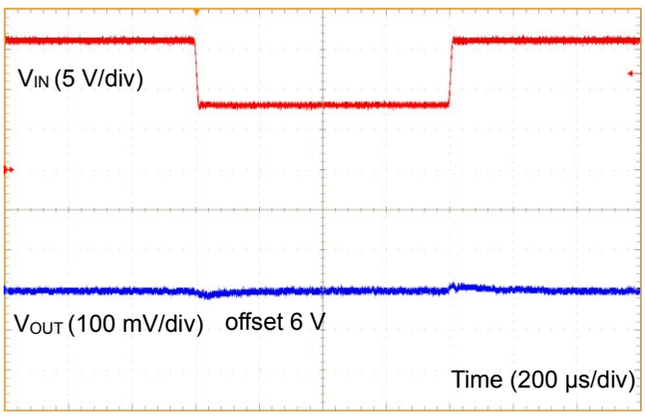


Figure 56. Line Response 1
(V_{IN} = 16 V to 8 V, I_{OUT} = 2 A)

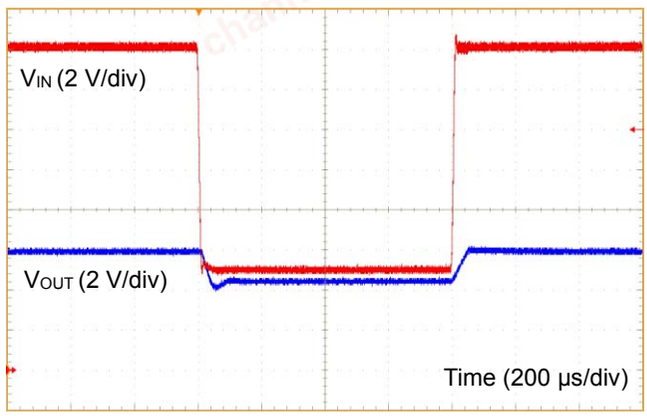


Figure 57. Line Response 2
(V_{IN} = 16 V to 5 V, I_{OUT} = 2 A)

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Application Examples 1 - continued

(Ta = 25 °C)

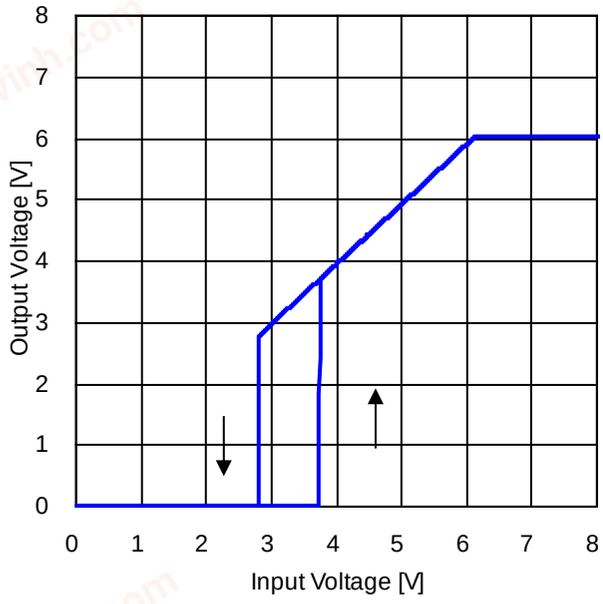


Figure 58. Output Voltage vs Input Voltage 1
(R_{LOAD} = 300 Ω)

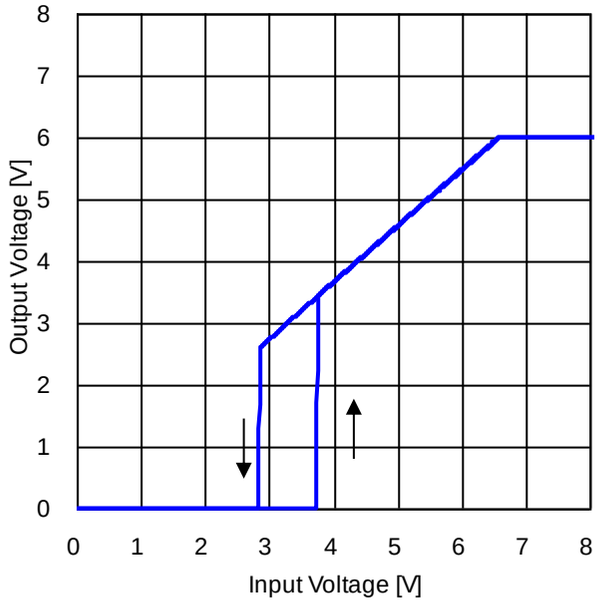


Figure 59. Output Voltage vs Input Voltage 2
(R_{LOAD} = 3 Ω)

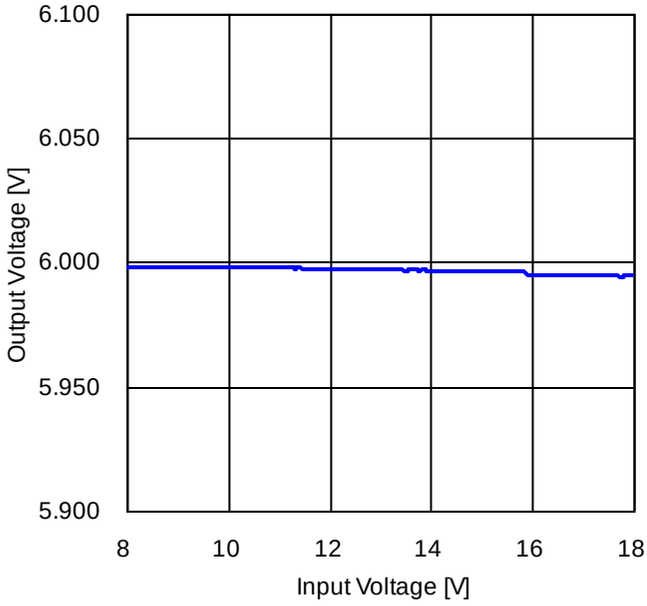


Figure 60. Line Regulation
(I_{OUT} = 2 A)

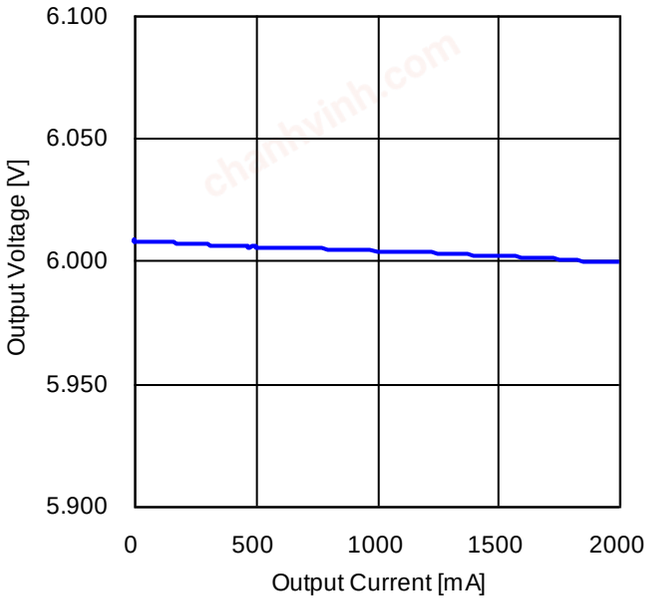


Figure 61. Load Regulation
(V_{IN} = 12 V)

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Application Examples 2

Table 8. Specification Example 2

Parameter	Symbol	Specification Case
Product Name	IC	BD9P235MUF-C
Input Voltage	V_{IN}	8 V to 18 V
Output Voltage	V_{OUT}	3.3 V
Output Current	I_{OUT}	Typ 1.0 A / Max 2.0 A
Operating Temperature Range	Ta	-40 °C to +125 °C

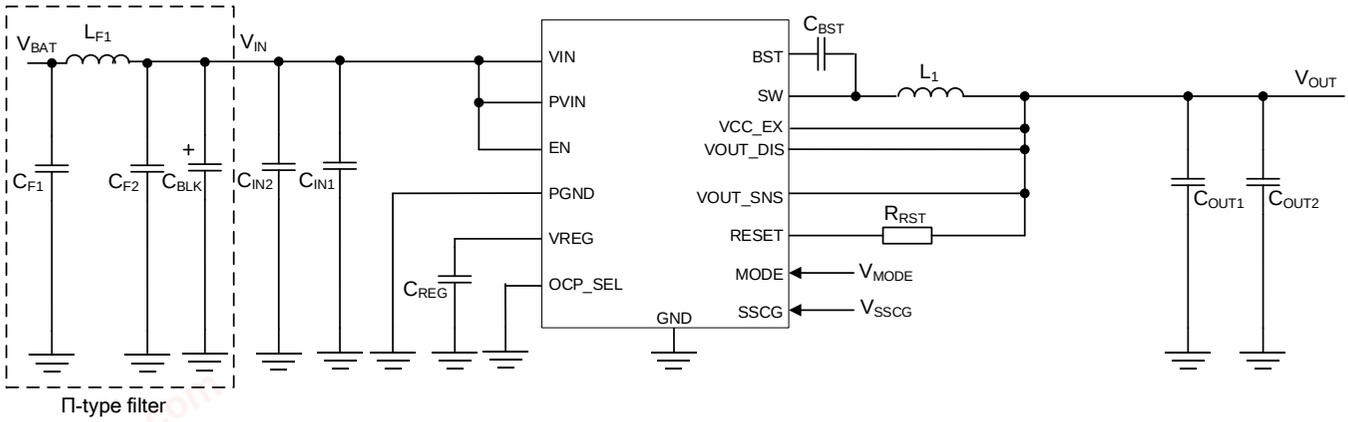


Figure 62. Reference Circuit 2

Table 9. Application Example 2 Parts List with π-type Filter

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1} *(Note 1)*	3216	1 µF, X7R, 50 V	GCJ31MR71H105K	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK
C_{F2}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{BLK}	φ10 mm x L10 mm	220 µF, 35 V	UWD1V221MCL1GS	Electrolytic capacitor	NICHICON
C_{IN2} *(Note 1)*	3216	1 µF, X7R, 50 V	GCJ31MR71H105K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	2012	1 µF, X7R, 16 V	GCM21BR71C105K	Ceramic	MURATA
C_{BST}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
R_{RST}	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip resistor	ROHM
L_1	W6.0 x H4.5 x L6.3 mm^3	3.3 µH	CLF6045NIT-3R3N-D	Inductor	TDK
C_{OUT1}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT2}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA

(Note 1) To reduce EMI noise level, 4.7 µF, (3225, X7R, 50 V, GCM32ER71H475K) is recommended for C_{F1} and C_{IN2}.

Table 10. Application Example 2 Parts List without π-type Filter

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1}	-	Open	-	-	-
L_{F1}	-	Open	-	-	-
C_{F2}	-	Open	-	-	-
C_{BLK}	-	Open	-	-	-
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA

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Application Examples 2 - continued

(Ta = 25 °C)

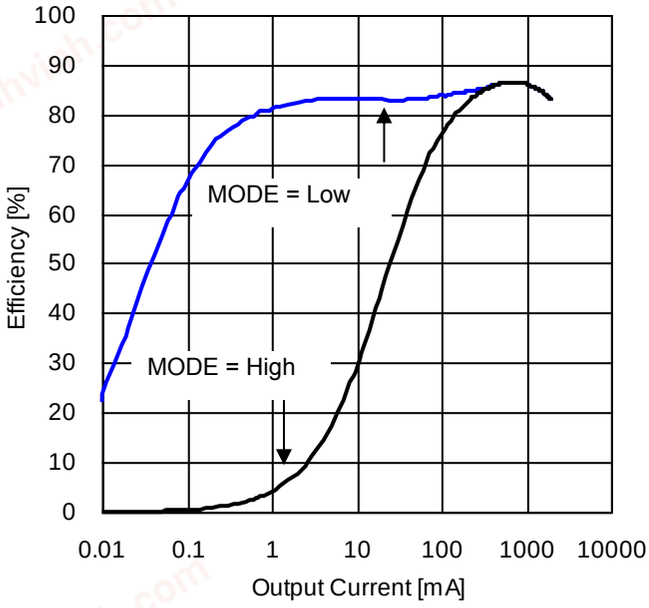


Figure 63. Efficiency vs Output Current
(V_{IN} = 12 V)

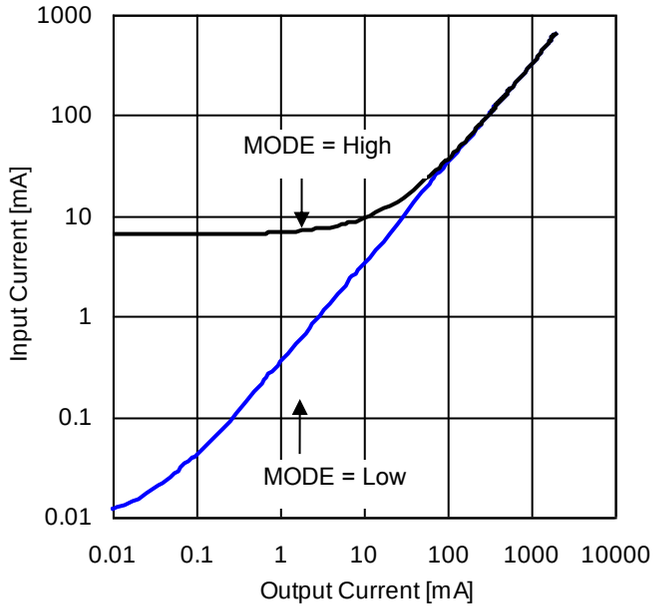


Figure 64. Input Current vs Output Current
(V_{IN} = 12 V)

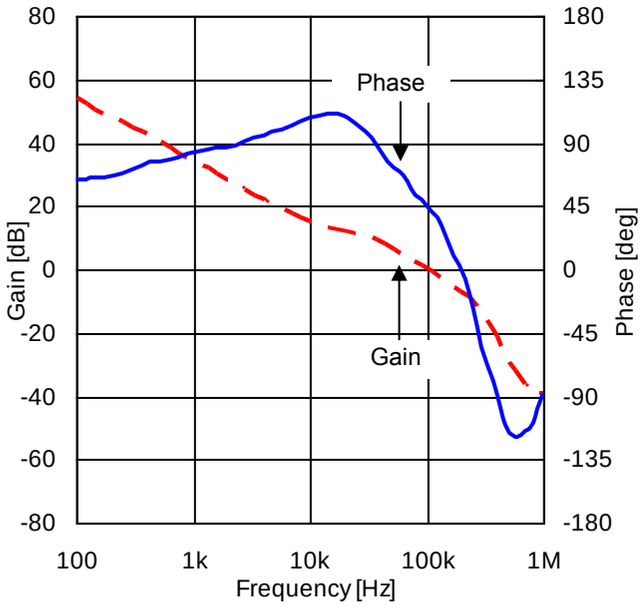


Figure 65. Frequency Characteristic
(V_{IN} = 12 V, I_{OUT} = 1.0 A)

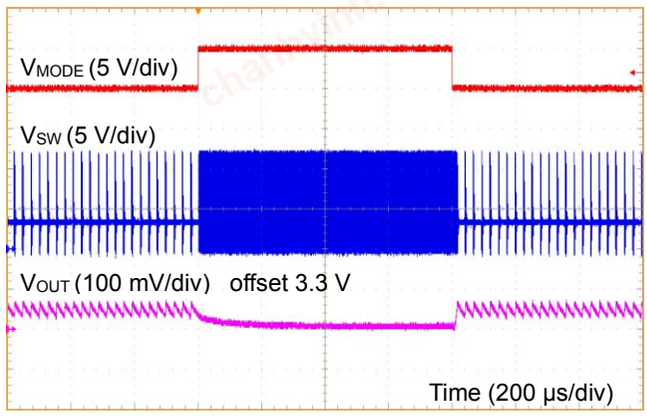


Figure 66. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

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Application Examples 2 - continued

(Ta = 25 °C)

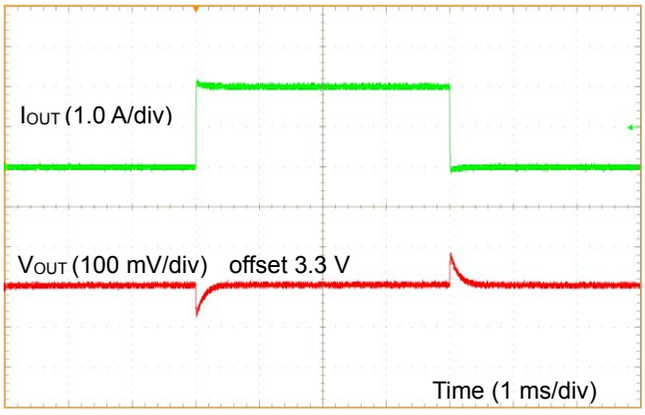


Figure 67. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 2 A)

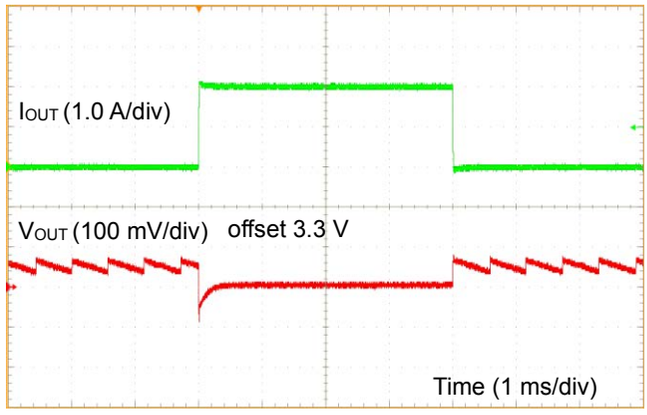


Figure 68. Load Response 2
(V_{IN} = 12 V, V_{MODE} = 0 V, I_{OUT} = 0 A to 2 A)

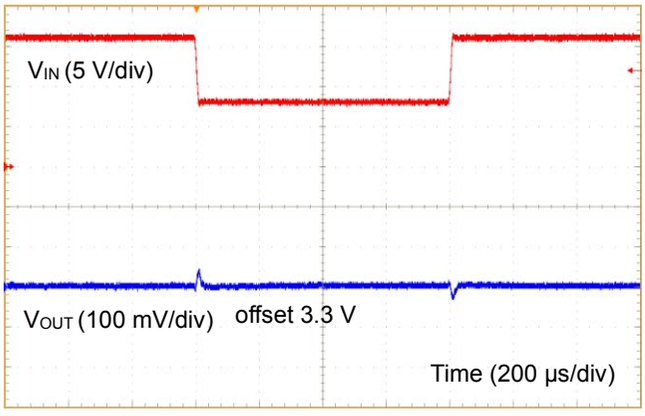


Figure 69. Line Response 1
(V_{IN} = 16 V to 8 V, I_{OUT} = 2 A)

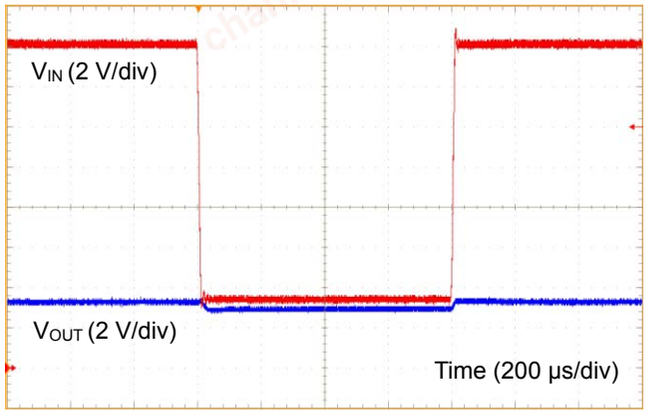


Figure 70. Line Response 2
(V_{IN} = 16 V to 3.5 V, I_{OUT} = 2 A)

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Application Examples 2 - continued

(Ta = 25 °C)

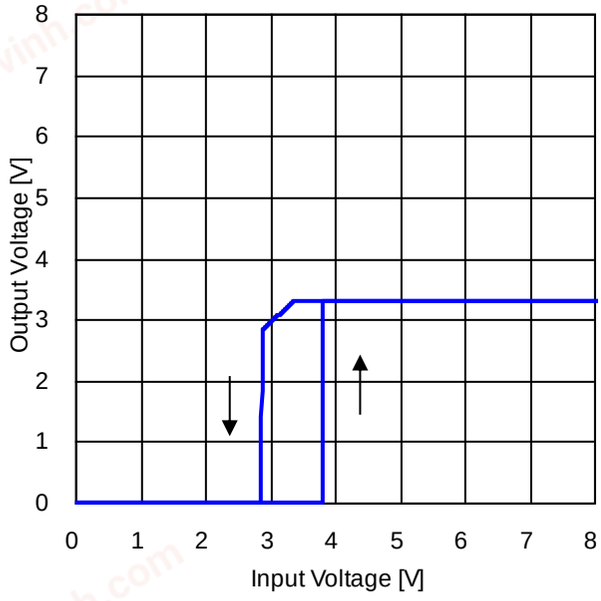


Figure 71. Output Voltage vs Input Voltage 1
(R_{LOAD} = 165 Ω)

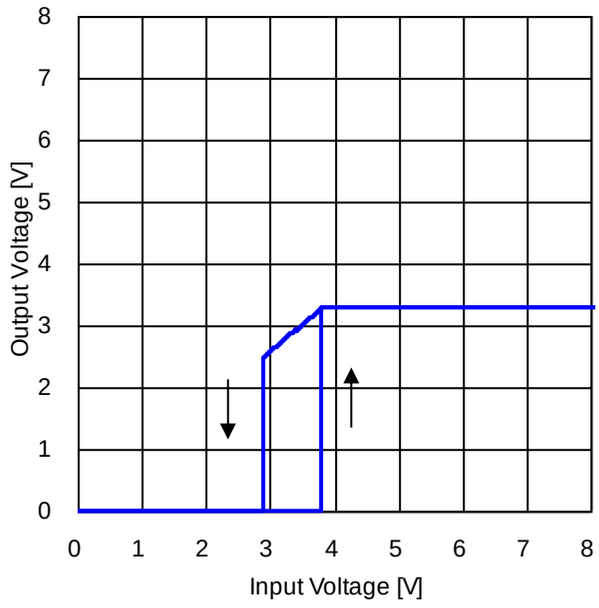


Figure 72. Output Voltage vs Input Voltage 2
(R_{LOAD} = 1.65 Ω)

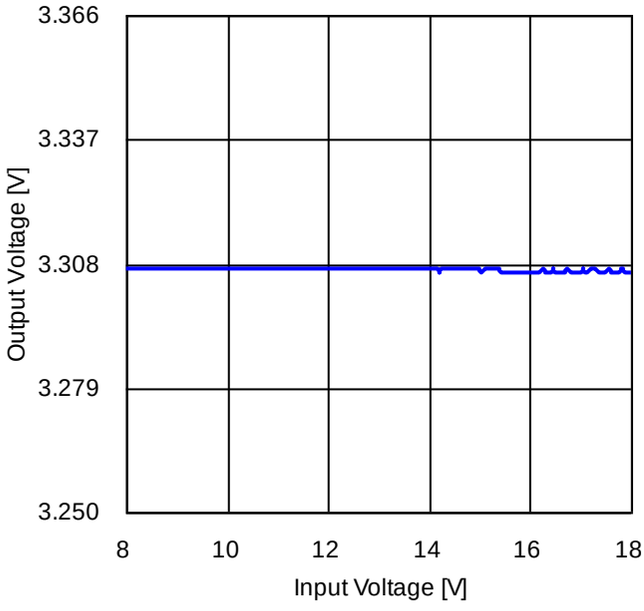


Figure 73. Line Regulation
(I_{OUT} = 2 A)

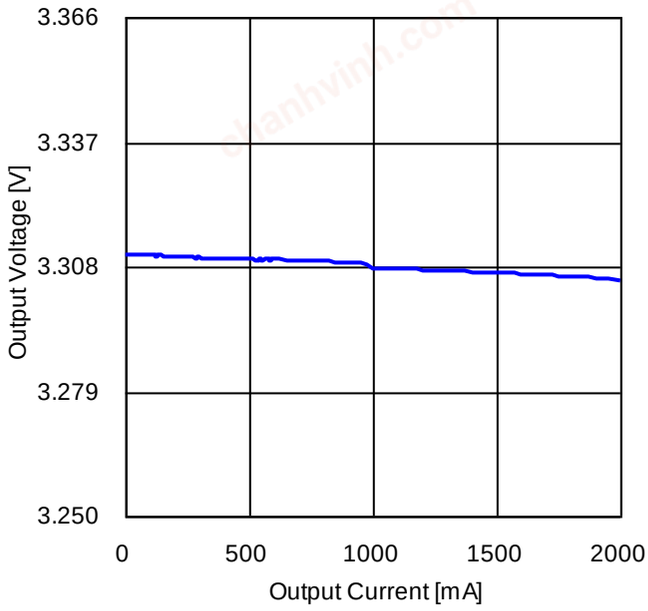


Figure 74. Load Regulation
(V_{IN} = 12 V)

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Application Examples 3

Table 11. Specification Example 3

Parameter	Symbol	Specification Case
Product Name	IC	BD9P255MUF-C
Input Voltage	V_{IN}	8 V to 18 V
Output Voltage	V_{OUT}	5.0 V
Output Current	I_{OUT}	Typ 1.0 A / Max 2.0 A
Operating Temperature Range	Ta	-40 °C to +125 °C

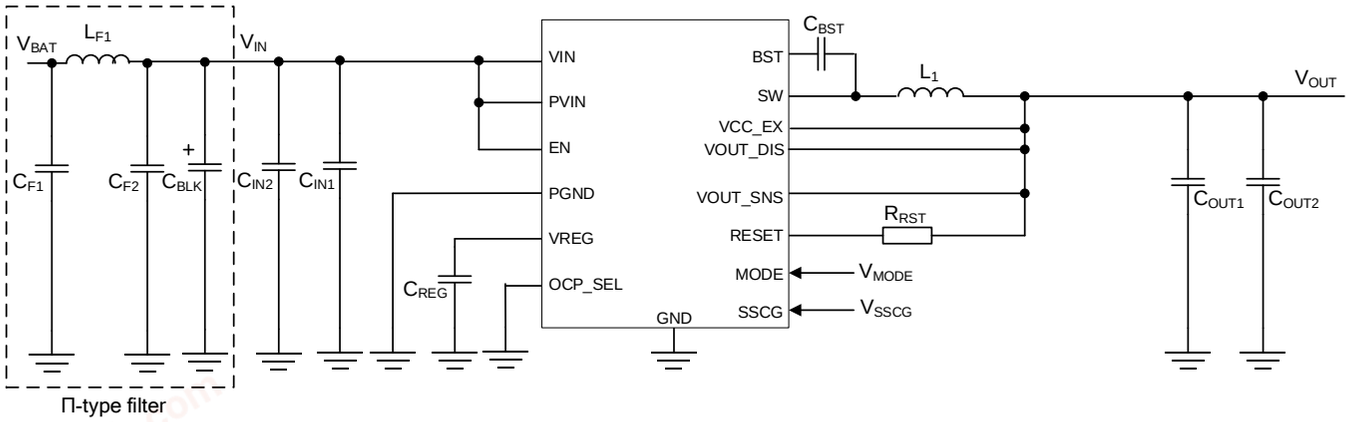


Figure 75. Reference Circuit 3

Table 12. Application Example 3 Parts List with π-type Filter

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1} *(Note 1)*	3216	1 µF, X7R, 50 V	GCJ31MR71H105K	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK
C_{F2}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{BLK}	φ10 mm x L10 mm	220 µF, 35 V	UWD1V221MCL1GS	Electrolytic capacitor	NICHICON
C_{IN2} *(Note 1)*	3216	1 µF, X7R, 50 V	GCJ31MR71H105K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	2012	1 µF, X7R, 16 V	GCM21BR71C105K	Ceramic	MURATA
C_{BST}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
R_{RST}	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip resistor	ROHM
L_1	W6.0 x H4.5 x L6.3 mm^3	3.3 µH	CLF6045NIT-3R3N-D	Inductor	TDK
C_{OUT1}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT2}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA

(Note 1) To reduce EMI noise level, 4.7 µF, (3225, X7R, 50 V, GCM32ER71H475K) is recommended for C_{F1} and C_{IN2}.

Table 13. Application Example 3 Parts List without π-type Filter

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1}	-	Open	-	-	-
L_{F1}	-	Open	-	-	-
C_{F2}	-	Open	-	-	-
C_{BLK}	-	Open	-	-	-
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA

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Application Examples 3 - continued

(Ta = 25 °C)

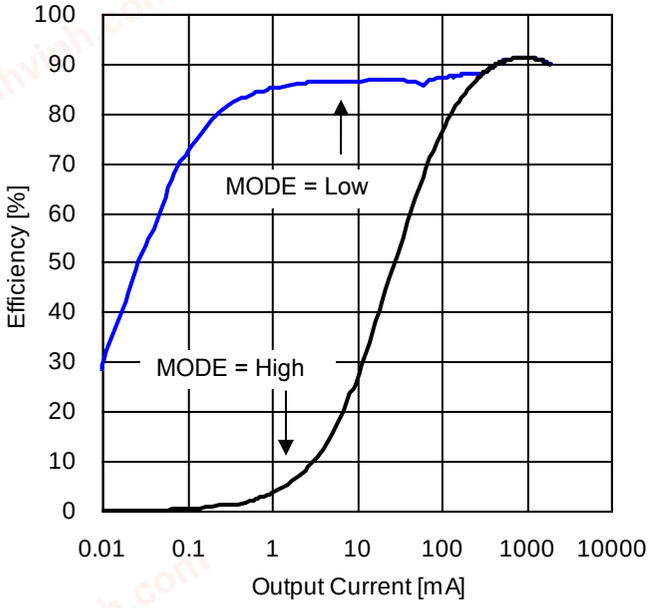


Figure 76. Efficiency vs Output Current
(V_{IN} = 12 V)

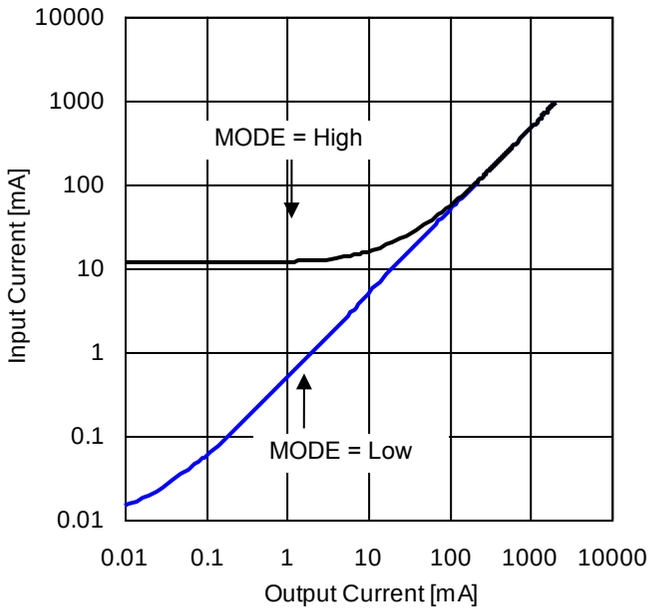


Figure 77. Input Current vs Output Current
(V_{IN} = 12 V)

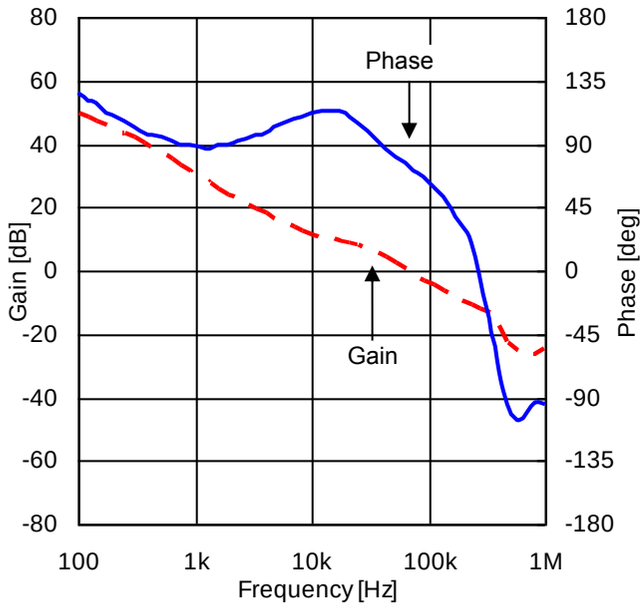


Figure 78. Frequency Characteristic
(V_{IN} = 12 V, I_{OUT} = 1.0 A)

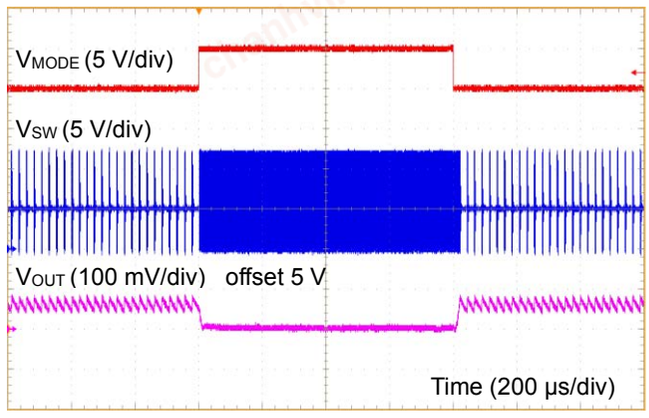


Figure 79. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

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Application Examples 3 - continued
(Ta = 25 °C)

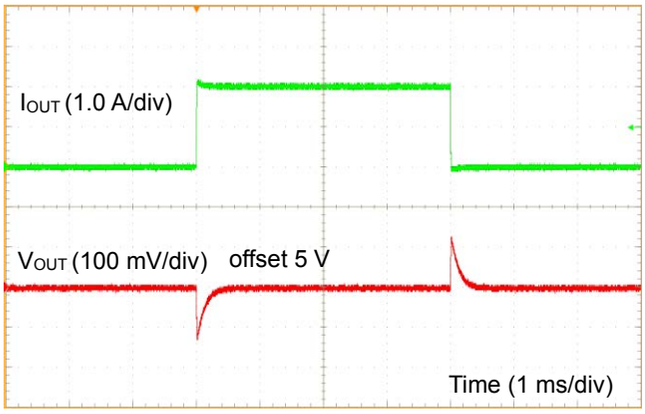


Figure 80. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 2 A)

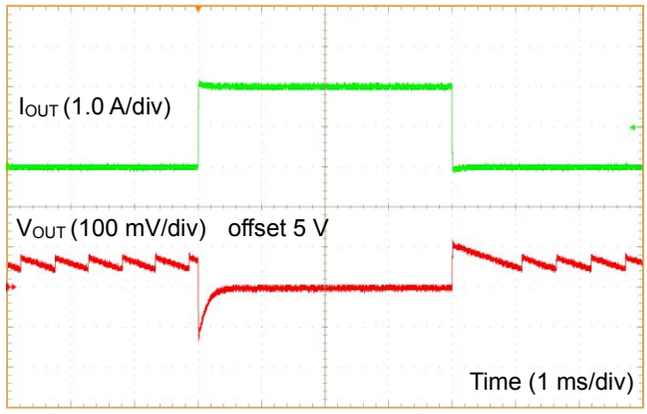


Figure 81. Load Response 2
(V_{IN} = 12 V, V_{MODE} = 0 V, I_{OUT} = 0 A to 2 A)

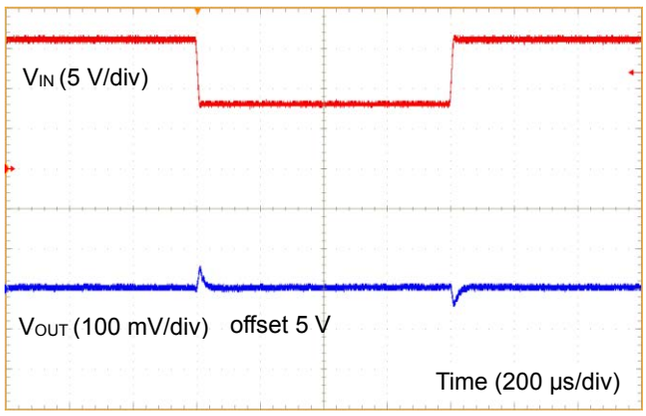


Figure 82. Line Response 1
(V_{IN} = 16 V to 8 V, I_{OUT} = 2 A)

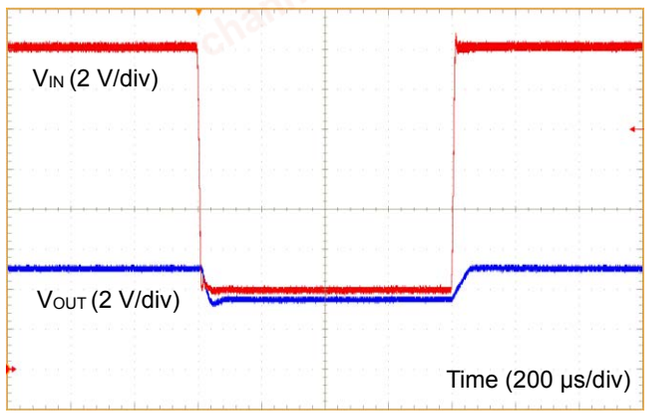


Figure 83. Line Response 2
(V_{IN} = 16 V to 4 V, I_{OUT} = 2 A)

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Application Examples 3 - continued

(Ta = 25 °C)

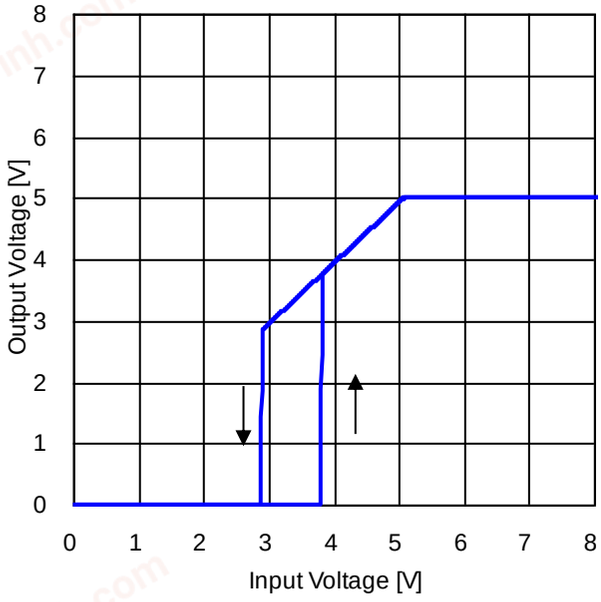


Figure 84. Output Voltage vs Input Voltage 1
(R_{LOAD} = 250 Ω)

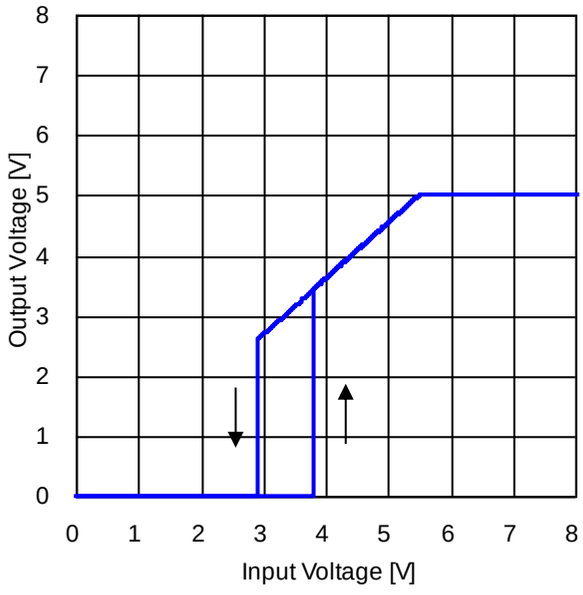


Figure 85. Output Voltage vs Input Voltage 2
(R_{LOAD} = 2.5 Ω)

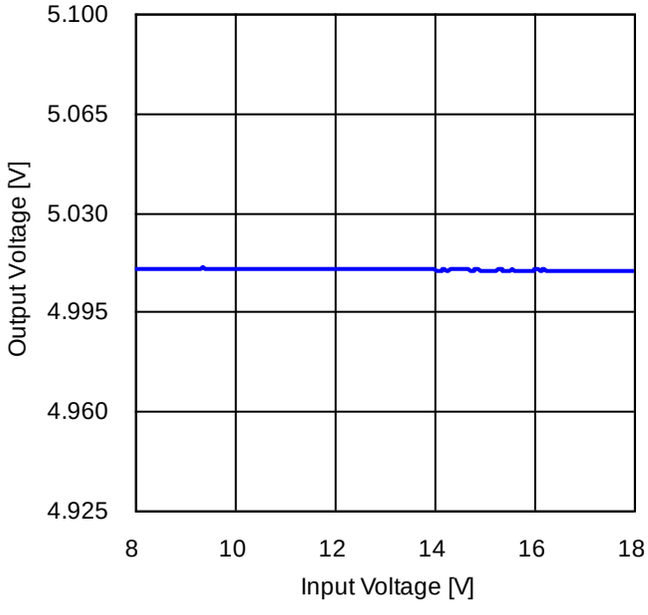


Figure 86. Line Regulation
(I_{OUT} = 2 A)

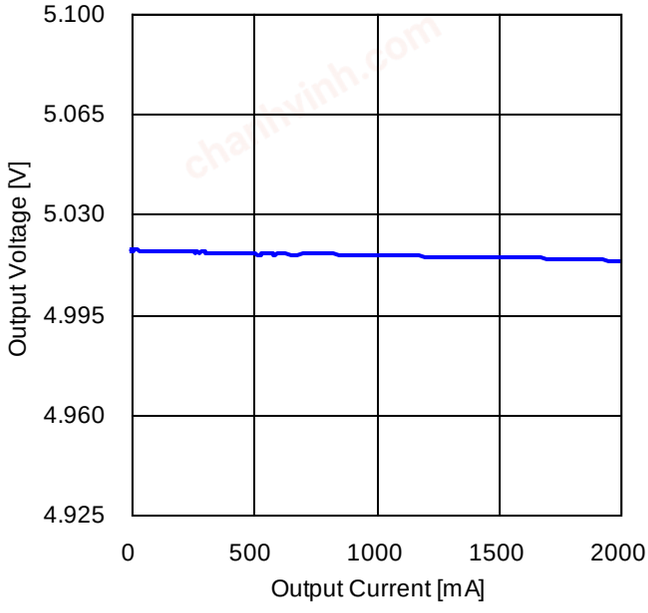


Figure 87. Load Regulation
(V_{IN} = 12 V)

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Automotive Power Supply Line Circuit

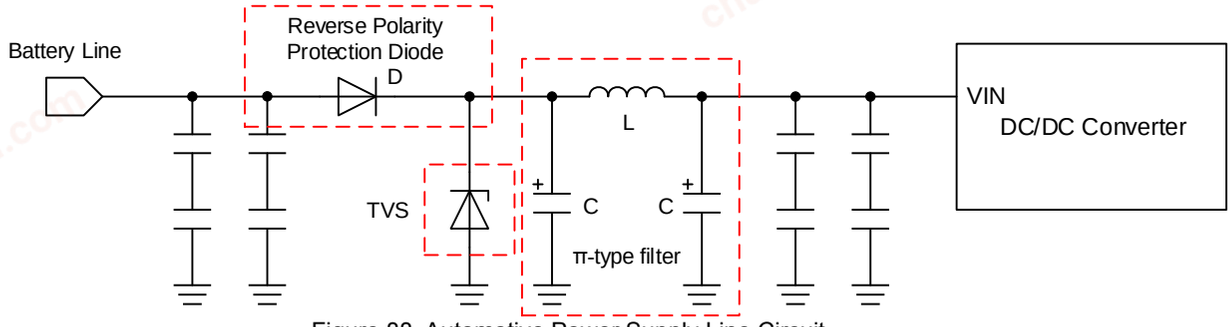


Figure 88. Automotive Power Supply Line Circuit

As a reference, the automotive power supply line circuit example is given in figure above.
The π-type filter is a third-order LC filter. In general, it is used in combination with decoupling capacitors for high frequency. Since large attenuation characteristics can be obtained, excellent characteristic is also obtained as an EMI filter. Devices used for π-type filters should be placed close to each other.
TVS (Transient Voltage Suppressors) is used for primary protection of the automotive power supply line. Since it is necessary to withstand high energy of load dump surge, a general zener diode is insufficient. Recommended device is shown in the following table.
In addition, a reverse polarity protection diode is needed considering if a power supply such as Battery is accidentally connected in the opposite direction.

Table 14. Reference Parts of Automotive Power Supply Line Circuit

Device	Part name (series)	Manufacturer	Device	Part name (series)	Manufacturer
L	CLF series	TDK	TVS	SMB series	Vishay
L	XAL series	Coilcraft	D	S3A to S3M series	Vishay
C	CJ series / CZ series	NICHICON			

Recommended Parts Manufacturer List

Shown below is the list of the recommended parts manufacturers for reference.

Type	Manufacturer	URL
Electrolytic Capacitor	NICHICON	www.nichicon.co.jp
Ceramic Capacitor	Murata	www.murata.com
Hybrid Capacitor	Suncon	www.sunelec.co.jp
Inductor	TDK	product.tdk.com
Inductor	Coilcraft	www.coilcraft.com
Inductor	SUMIDA	www.sumida.com
Diode	Vishay	www.vishay.com
Diode/Resistor	ROHM	www.rohm.com

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PCB Layout Design

PCB layout design for DC/DC converter power supply IC is as important as the circuit design. Appropriate layout can avoid various problems caused by power supply circuit. Figure 89 (a) to Figure 89 (c) figure the current path in a buck converter circuit. The Loop1 in Figure 89 (a) is a current path when High Side Switch is ON and Low Side Switch is OFF, the Loop2 in Figure 89 (b) is when High Side Switch is OFF and Low Side Switch is ON. The thick line in Figure 89 (c) shows the difference between Loop1 and Loop2. The current in thick line changes sharply each time the switching element High Side Switch and Low Side Switch change from OFF to ON, and vice versa. These sharp changes induce several harmonics in the waveform. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more detail, refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

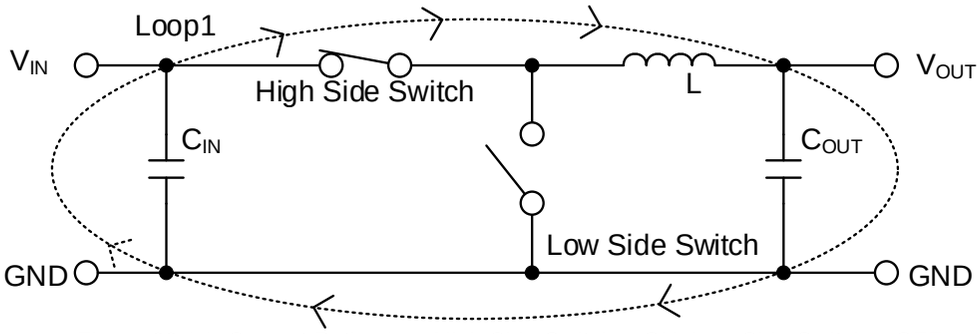


Figure 89 (a). Current Path when High Side Switch = ON, Low Side Switch = OFF

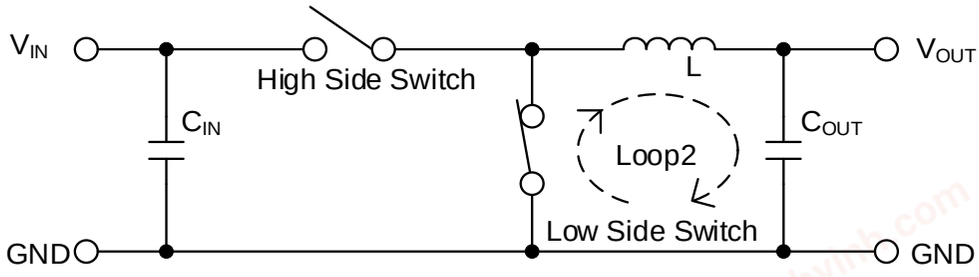


Figure 89 (b). Current Path when High Side Switch = OFF, Low Side Switch = ON

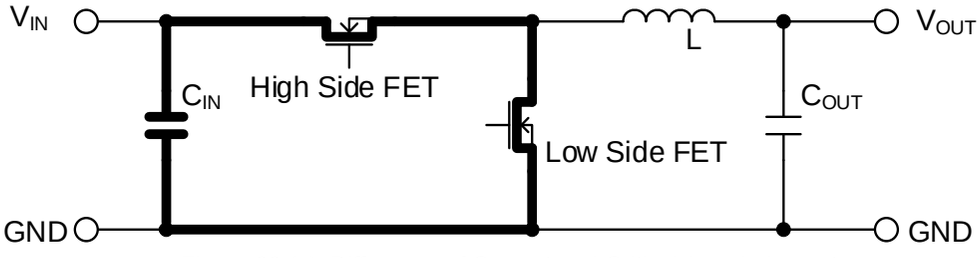


Figure 89 (c). Difference of Current and Critical Area in Layout

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PCB Layout Design – continued

When designing the PCB layout, please pay extra attention to the following points.

1. The decoupling capacitors (C_{IN1}) for the VIN pin (pin 20) and the PVIN pins (pin 1, 2) should be placed closest to the PVIN pins and the PGND pins (pin 4, 5). In addition, placing a capacitor 0.1 μF close to the PVIN pin results in minimizing the high-frequency noise.
2. The device, the input capacitor, the output inductor and the output capacitor should be placed on the same side of the board and the connection of each part should be made on the same layer.
3. Place the ground plane in a layer closest to the surface layer where the device is mounted.
4. The GND pin (pin 13) is the reference ground and the PGND pins are the power ground. These pins should be connected through the back side of the device. The power systems ground should be connected to the ground plane using as many vias as possible.
5. The capacitor for VREG should be placed closest to the VREG pin (pin 17), the GND pin and the PGND pin. As shown in the Recommended Board Layout Example, it can be realized that connecting with the shortest distance for the GND pin and the PGND pins by placing the capacitor for VREG on the closest to the VREG pin and wiring at the back side of the IC.
6. Place Bootstrap capacitor C_{BST} close to the device with short traces to the SW pins (pin 6, 7) and the BST pin (pin 8).
7. To minimize the emission noise from switching node, the distance between the SW pins to inductor should be as short as possible and not to expand the copper area more than necessary.
8. Place the output capacitor close to the inductor and power ground area.
9. Make the feedback line from the output away from the inductor and the switching node. If this line is affected by external noise, an error may be occurred in the output voltage or the control may become unstable. Therefore, move the feedback line to back side layer of the board through via and connect it to the VOUT_SNS pin (pin 14 [BD9P205MUF-C], pin 15 [BD9P235MUF-C, BD9P255MUF-C]). When the VCC_EX function and the output discharge function are used, connect it to the VCC_EX (pin 16) and the VOUT_DIS pin (pin 14 [BD9P235MUF-C, BD9P255MUF-C]) as well, respectively.
10. R_{FB1} and R_{FB2} Feedback resistors are needed for BD9P205MUF-C. Place R_{FB1}, R_{FB2} close to the FB pin (pin 15).
11. R_{FB0} is for measuring the frequency characteristic of the feedback. By inserting a resistor in R_{FB0}, the frequency characteristics (phase margin) of the feedback can be measured. R_{FB0} should be short-circuited for the normal use.

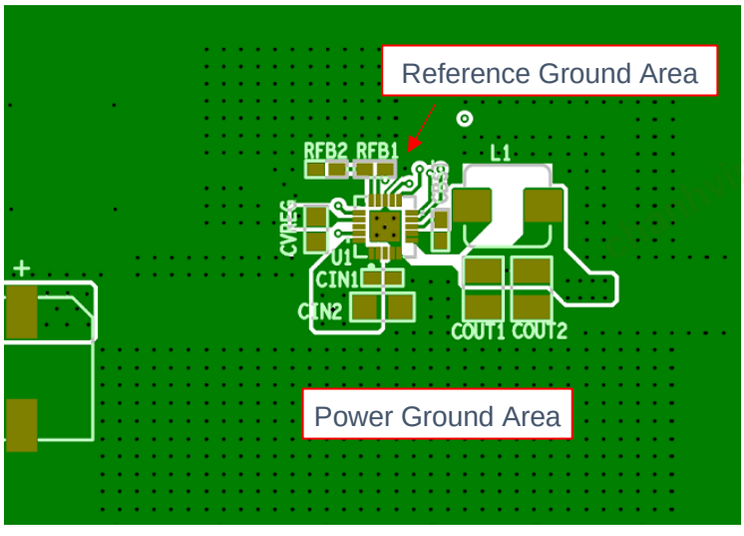


Figure 90. Recommended Board Layout Example (for BD9P2x5MUF-C)

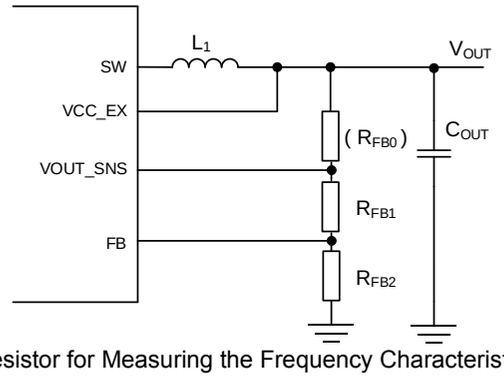


Figure 91. The Resistor for Measuring the Frequency Characteristic of the Feedback

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Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature Ta is to be 125 °C or less.
2. The chip junction temperature Tj is to be 150 °C or less.

The chip junction temperature Tj can be considered in the following two patterns:

1. To obtain Tj from the package surface center temperature Tt in actual use

$$Tj = Tt + \psi_{JT} \times W \ [°C]$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta_{JA} \times W \ [°C]$$

Where:

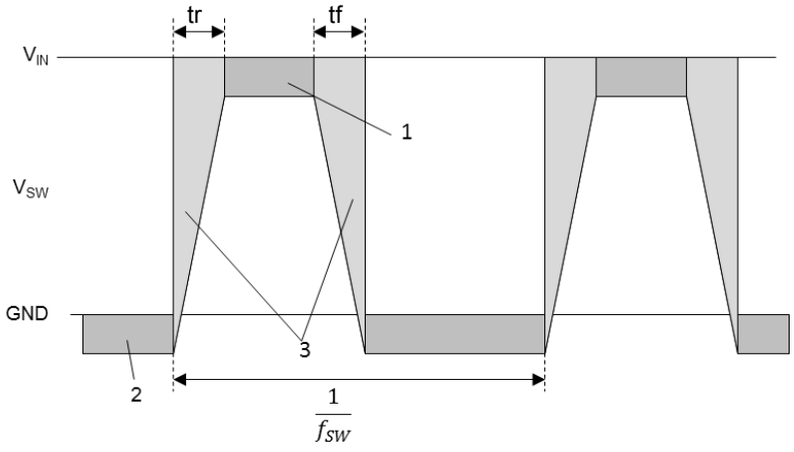
ψ_{JT}	is junction to top characterization parameter.	(Refer to page 9)
θ_{JA}	is junction to ambient.	(Refer to page 9)

The heat loss W of the IC can be obtained by the formula shown below.
This formula is approximation, please confirm this on the actual application circuit.

$$W = R_{ONH} \times {I_{OUT}}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times {I_{OUT}}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{Q_VIN4} + V_{OUT} \times I_{Q_VCC_EX2} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \ [W]$$

Where:

R_{ONH}	is the High Side FET ON Resistance [Ω]	(Refer to page 11)
R_{ONL}	is the Low Side FET ON Resistance [Ω]	(Refer to page 11)
I_{OUT}	is the Load Current [A]	
V_{OUT}	is the Output Voltage [V]	
V_{IN}	is the Input Voltage [V]	
I_{Q_VIN4}	is the Quiescent Current from VIN [A]	(Refer to page 10)
$I_{Q_VCC_EX2}$	is the Quiescent Current from VCC_EX [A]	(Refer to page 10)
tr	is the Switching Rise Time [s] (5 ns, Typ)	
tf	is the Switching Fall Time [s] (5 ns, Typ)	
f_{SW}	is the Switching Frequency [Hz]	(Refer to page 11)



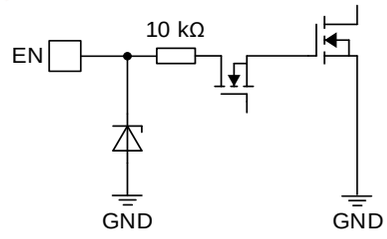
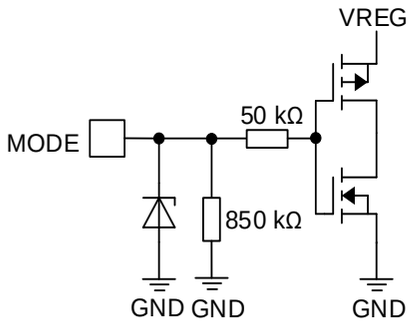
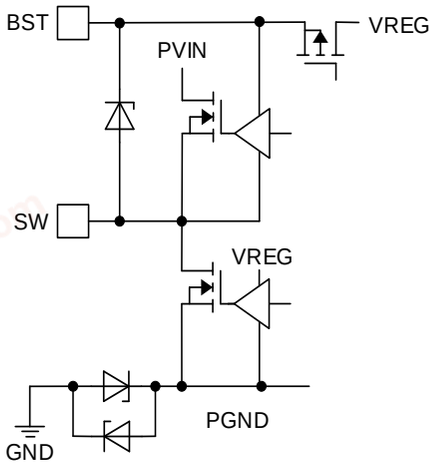
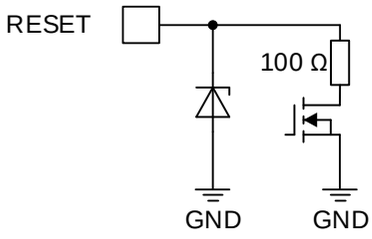
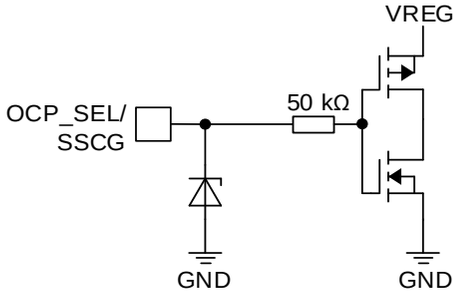
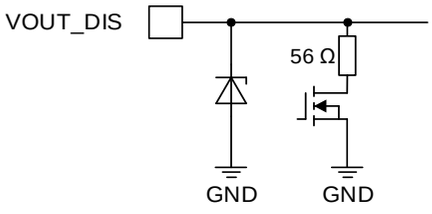
1. $R_{ONH} \times {I_{OUT}}^2$
2. $R_{ONL} \times {I_{OUT}}^2$
3. $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW}$

Figure 92. SW Waveform

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I/O Equivalence Circuits

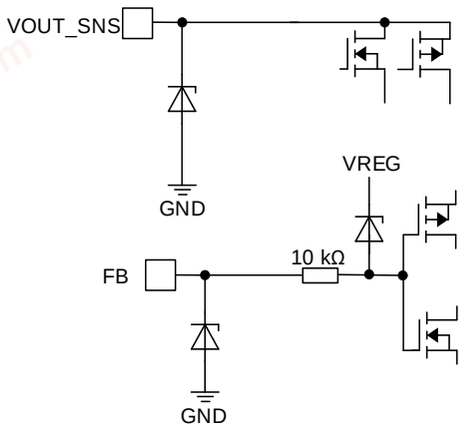
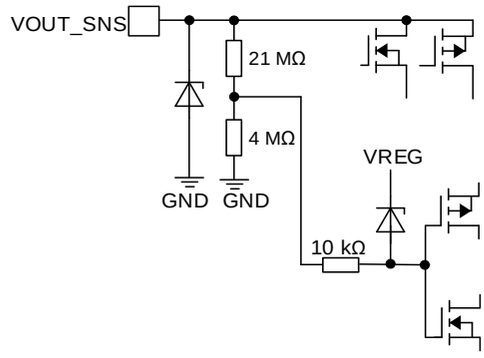
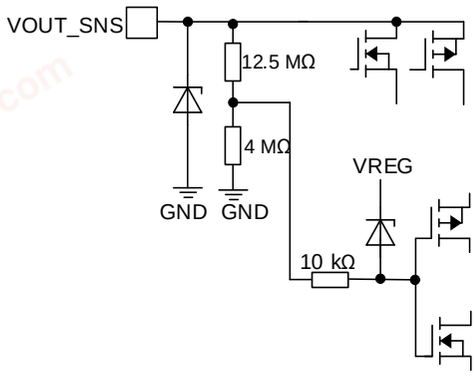
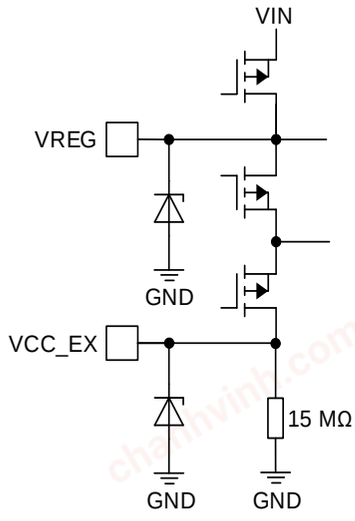
19. EN	10. MODE
	
6,7. SW, 8.BST	**12. RESET**
	
9. OCP_SEL, 11. SSCG	**14. VOUT_DIS (BD9P235MUF-C, BD9P255MUF-C)**
	

*Resistance value is Typ.

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I/O Equivalence Circuits - continued

14. VOUT_SNS, 15. FB (BD9P205MUF-C)	15. VOUT_SNS (BD9P255MUF-C)
	
15. VOUT_SNS (BD9P235MUF-C)	**16. VCC_EX, 17. VREG**
	

*Resistance value is Typ.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

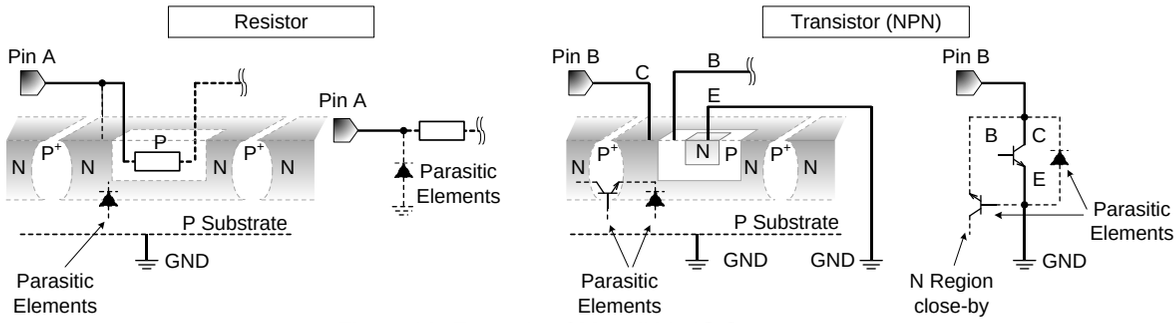


Figure 93. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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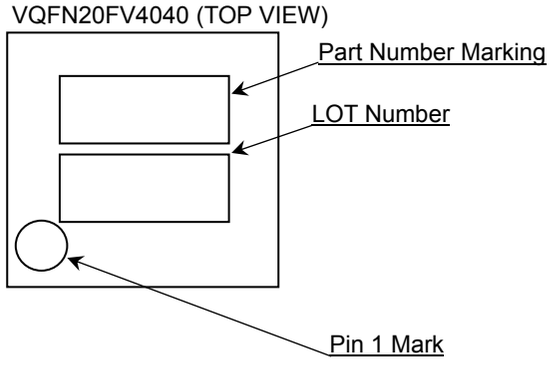
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Ordering Information

B D 9 P 2 x 5 M U F - C E 2

Part Number	Output Voltage	Package	Product Rank / Packaging Specification
	0: Adjustable 3: 3.3 V 5: 5.0 V	MUF: VQFN20FV4040	C: for Automotive E2: Embossed tape and reel

Marking Diagram



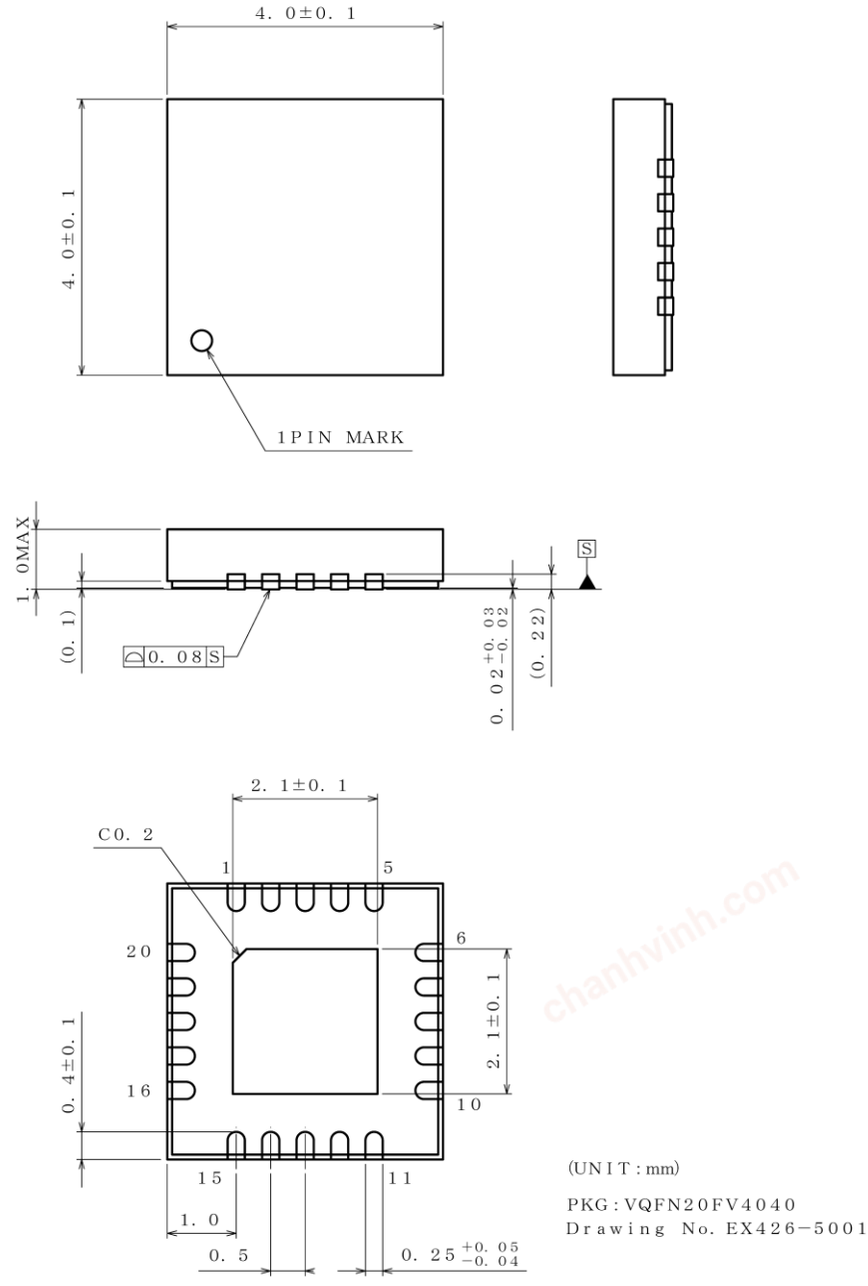
Orderable Part Number	Output Voltage	Part Number Making
BD9P205MUF-CE2	Adjustable	9P205
BD9P235MUF-CE2	3.3 V	9P235
BD9P255MUF-CE2	5.0 V	9P255

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Physical Dimension and Packing Information

Package Name	VQFN20FV4040



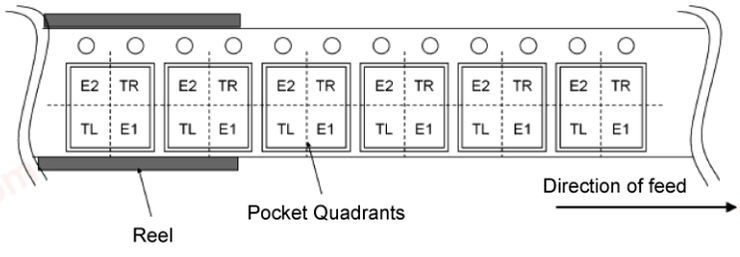
(UNIT : mm)

PKG : VQFN20FV4040
Drawing No. EX426−5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
28.Apr.2020	001	New Release
04.Oct.2022	002	Selection of Components Externally Connected Change description of selection of the inductor L_1 value Change description of selection of Output Capacitor C_{OUT} Change description of selection of Output Voltage Setting Resistor R_{FB1}, R_{FB2}

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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General Precaution

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