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Datasheet

4.5 V to 26 V Input, 2.0 A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9E200FP4-Z

General Description

BD9E200FP4-Z is a single synchronous buck DC/DC converter with built-in low on-resistance power MOSFETs. The Light Load Mode control provides excellent efficiency characteristics in light-load conditions, which make the product ideal for equipment, and devices that demand minimal standby power consumption. BD9E200FP4-Z is a current mode control DC/DC converter and features good transient response. It includes internal phase compensation. It achieves the high power density and offers a small footprint on the PCB by employing small package.

Features

- Single Synchronous Buck DC/DC Converter
- Light Load Mode Control
- Frequency Spread Spectrum
- Internal Phase Compensation
- Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Short Circuit Protection (SCP)
- Thermal Shutdown Protection (TSD)
- Under Voltage Lockout Protection (UVLO)
- Reduced External Diode
- TSOT23-6L Package

Applications

- Home Appliance Products (i.e., Air Conditioner, Refrigerator)
- Secondary Power Supply and Adapter Equipment
- Telecommunication Devices

Key Specifications

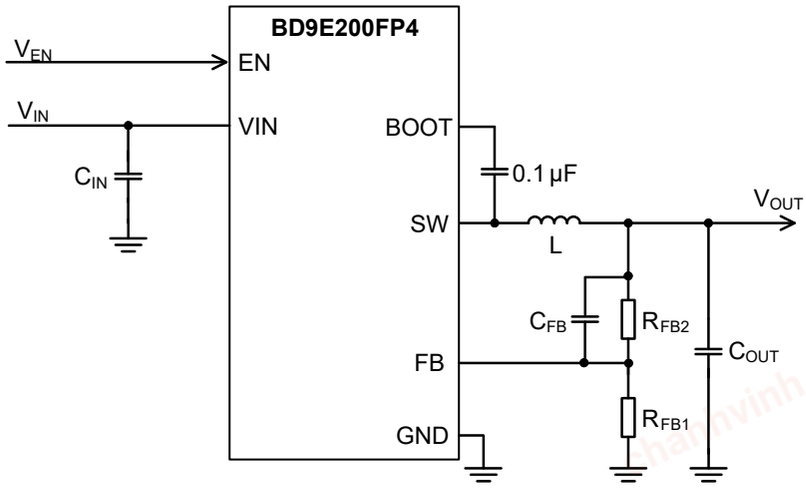
- Input Voltage Range: 4.5 V to 26.0 V
- Output Voltage Range: V_{IN}x0.1 or 0.7 V to V_{IN}x0.8 V
- Output Current: 2 A (Max)
- Switching Frequency: 500 kHz (Typ)
- High Side FET ON Resistance: 185 mΩ (Typ)
- Low Side FET ON Resistance: 98 mΩ (Typ)
- Shutdown Current: 4 µA (Typ)
- Operating Quiescent Current: 95 µA (Typ)

Package	W (Typ) x D (Typ) x H (Max)
TSOT23-6L	2.8 mm x 2.9 mm x 0.95 mm



TSOT23-6L

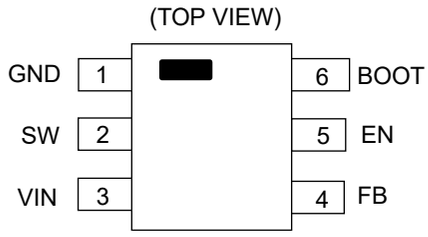
Typical Application Circuit



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Pin Configuration



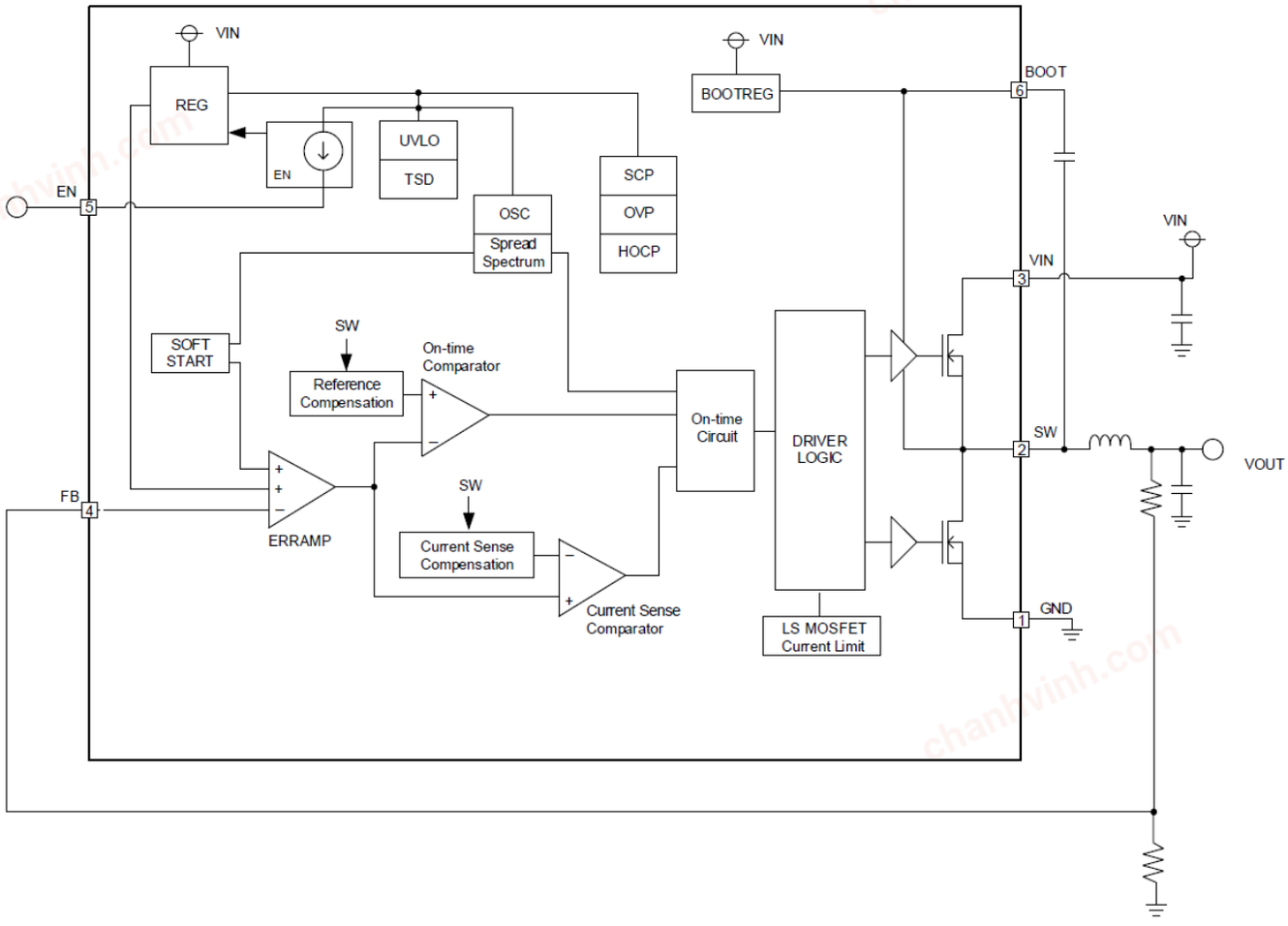
Pin Description

Pin No.	Pin Name	Function
1	GND	Ground pins for the control circuit and output stage of the switching regulator.
2	SW	Switch pin. This pin is connected to the source of the High Side FET and the drain of the Low Side FET. Connect a bootstrap capacitor of 0.1 µF between this pin and the BOOT pin. In addition, connect an inductor considering the direct current superimposition characteristic.
3	VIN	Power supply pin. Connecting 0.1 µF (Typ) and 10 µF (Typ) ceramic capacitors is recommended. The detail of a selection is described in Selection of Components Externally Connected 1. Input Capacitor.
4	FB	Output voltage feedback pin. See Selection of Components Externally Connected 3. Output Voltage Setting, FB Capacitor for the output voltage setting.
5	EN	Enable pin. The device starts up with setting V_{EN} to 1.21 V (Typ) or more. The device enters the shutdown mode with setting V_{EN} to 1.19 V (Typ) or less. When this pin is open, this pin is pull-up to IC internal regulator and the device is enabled.
6	BOOT	Pin for bootstrap. Connect a bootstrap capacitor of 0.1 µF (Typ) between this pin and the SW pin. The voltage of this pin is the gate drive voltage of the High Side FET.

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Block Diagram



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Description of Blocks

1. REG
   This block generates the internal regulator voltage.

2. BOOTREG
   Block creating gate drive voltage.

3. SOFT START
   The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. The internal soft start time is 5 ms (Typ).

4. ERRAMP
   This is the error amplifier. This block compares the FB voltage (V_{FB}) and the internal reference voltage. The output voltage is set by the FB external resistors.

5. On-time Comparator
   The On-time Comparator compares the Error Amplifier output voltage and the reference voltage compensated by SW average voltage. When the Error Amplifier output voltage becomes higher than the reference voltage, the output turns low and reports to the On-time Circuit that the output voltage has dropped below the control voltage.

6. On-time Circuit
   This block generates the High Side FET on-time signal. Generates an on-time signal set by the On-time comparator output, OSC signal and Current Sense Comparator output.

7. Current Sense Comparator
   This is a comparator that compares the ERRAMP signal with the current sense signal compensated by ramp signal.

8. UVLO
   The UVLO block is for under voltage lockout protection. The device is shutdown when input voltage (V_{IN}) falls to 3.9 V (Typ) or less. The threshold voltage has the 350 mV (Typ) hysteresis.

9. TSD
   The TSD block is for thermal protection. The device is shutdown when the junction temperature Tj reaches to 175 °C (Typ) or more. The device is automatically restored to normal operation with a hysteresis of 25 °C (Typ) when the Tj goes down.

10. EN
    The EN Block is for enabling or shutting down the IC. The device operate when the EN voltage is 1.21 V (Typ) or more and shutdown when EN voltage is 1.19 V (Typ) or less. When this pin is open, this pin is pull-up to IC internal regulator and the device is enabled.

11. OVP
    The OVP block is for over voltage protection. When the FB voltage (V_{FB}) exceeds 120 % (Typ) or more of FB threshold voltage V_{FBTH}, the output MOSFETs are turned off. After V_{FB} falls 115 % (Typ) or less of V_{FBTH}, the device is returned to normal operation condition.

12. HOCP
    This block is for over current protection of the High Side FET. When the current that flows through the High Side FET reaches the value of over current limit, it turns off the High Side FET and turns on the Low Side FET.

13. SCP
    This block is for short circuit protection. After soft start is completed and in condition where V_{FB} is 70 % (Typ) of 0.596 V or less and remained there for 128 µs (Typ), the device is shutdown for 32.8 ms (Typ) and subsequently initiates a restart.

14. LS MOSFET Current Limit
    This circuit is a comparator that monitors the inductor current. When inductor current falls below 0 A (Typ) while the Low Side FET is on, it turns off the Low Side FET.

15. OSC
    This block generates the internal oscillation frequency.

16. Spread Spectrum
    This block introduces Spread Spectrum Operation.

17. DRIVER LOGIC
    This block controls the switching operation and protection function operation.

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Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	-0.3 to +30	V
SW Voltage	V_{SW}	-0.3 to V_{IN}+0.3	V
SW Voltage (5 ns pulse width)	V_{SWAC}	-3	V
Voltage from GND to BOOT	V_{BOOT}	-0.3 to +35	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
FB Voltage	V_{FB}	-0.3 to +3	V
EN Voltage	V_{EN}	-0.3 to +3	V
Output Current	I_{OUT}	2	A
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
TSOT23-6L				
Junction to Ambient	θ_{JA}	229.5	117.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	45	40	°C/W

(Note 1) Based on JESD51-2A (Still-Air), using a BD9E200FP4 Chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{IN}	4.5	-	26.0	V
Operating Temperature *(Note 1)*	Topr	-40	-	+85	°C
Output Current *(Note 1)*	I_{OUT}	0	-	2	A
Output Voltage Setting *(Note 2)*	V_{OUT}	0.7	-	V_{IN}x0.8	V

(Note 1) Tj must be 150 °C or less under the actual operating environment. Life time is derated at junction temperature greater than 125 °C.
(Note 2) Please use within the range of $V_{OUT} \geq V_{IN} \times 0.1$ [V].

Electrical Characteristics (Unless otherwise specified Ta = 25 °C, V_{IN} = 12 V, V_{EN} = 3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Supply						
Shutdown Current	I_{SDN}	-	4	15	µA	V_{EN} = 0 V
Operating Quiescent Current	I_Q	-	95	175	µA	I_{OUT} = 0 A, No switching
UVLO Threshold Voltage	V_{UVLO}	3.7	3.9	4.1	V	V_{IN} falling
UVLO Hysteresis Voltage	$V_{UVLOHYS}$	300	350	400	mV	
Enable						
EN Threshold Voltage High	V_{ENH}	-	1.21	1.28	V	V_{EN} rising
EN Threshold Voltage Low	V_{ENL}	1.10	1.19	-	V	V_{EN} falling
EN Input Current *(Note 3)*	I_{EN}	-	0.7	-	µA	V_{EN} = 1 V
EN Input Hysteresis Current *(Note 3)*	I_{EN_HYS}	-	1.50	-	µA	$I_{EN_2V} - I_{EN_1V}$
Reference Voltage, Error Amplifier, Soft Start						
FB Threshold Voltage	V_{FBTH}	0.587	0.596	0.605	V	
FB Input Current	I_{FB}	-	-	100	nA	V_{FB} = 0.7 V
Soft Start Time	t_{SS}	3.5	5.0	6.5	ms	
SW (MOSFET)						
Switching Frequency	f_{SW}	390	500	590	kHz	
Maximum Duty Ratio	D_{MAX}	80	-	-	%	
High Side FET ON Resistance	R_{ONH}	-	185	270	mΩ	V_{BOOT} - V_{SW} = 5 V
Low Side FET ON Resistance	R_{ONL}	-	98	140	mΩ	
Protection						
High Side Over Current Limit *(Note 3)*	I_{HOCP}	2.5	3.2	3.9	A	No switching

(Note 3) No tested on outgoing inspection.

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Typical Performance Curves

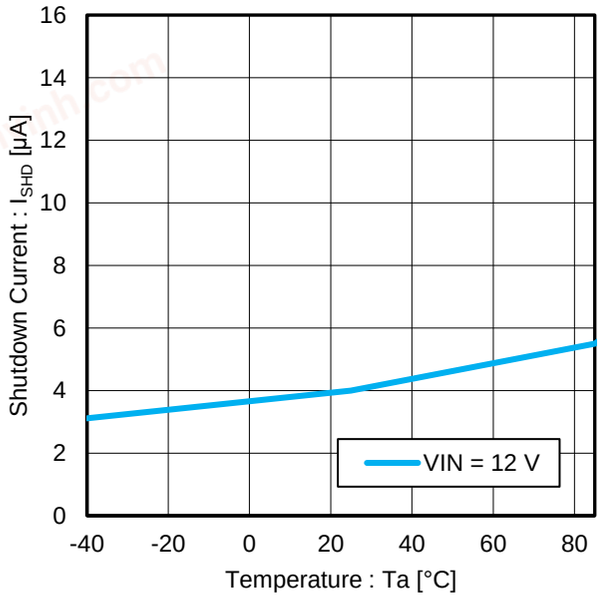


Figure 1. Shutdown Current vs Temperature

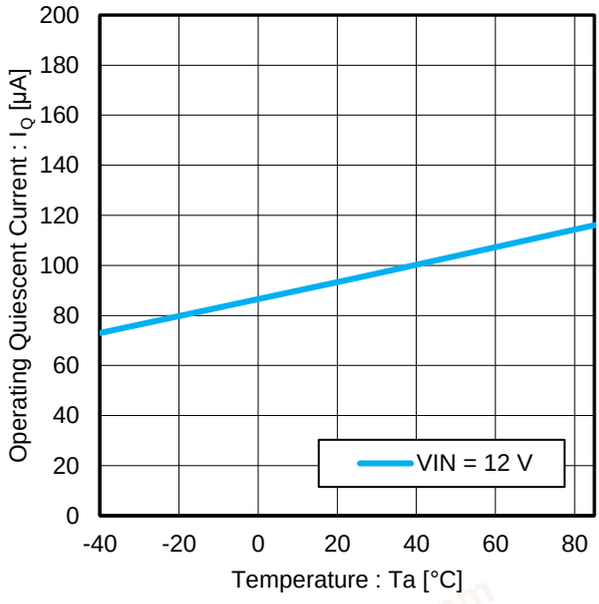


Figure 2. Operating Quiescent Current vs Temperature

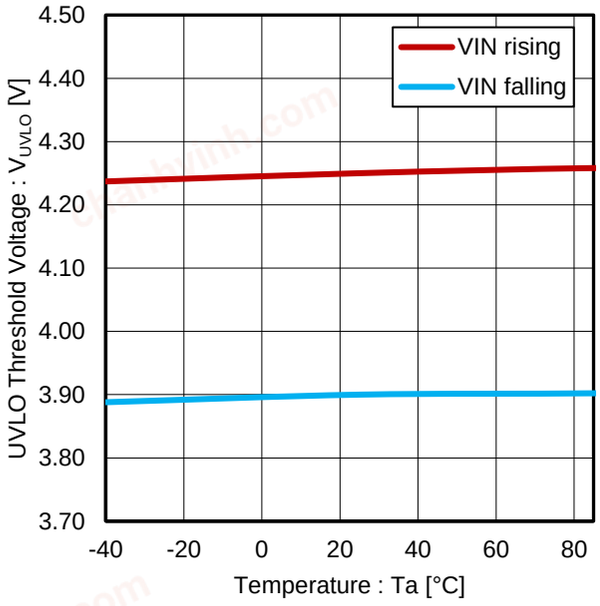


Figure 3. UVLO Threshold Voltage vs Temperature

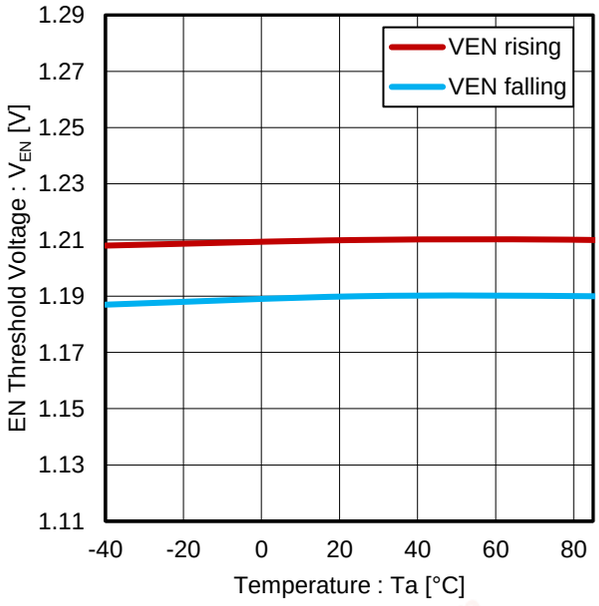


Figure 4. EN Threshold Voltage vs Temperature

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Typical Performance Curves – continued

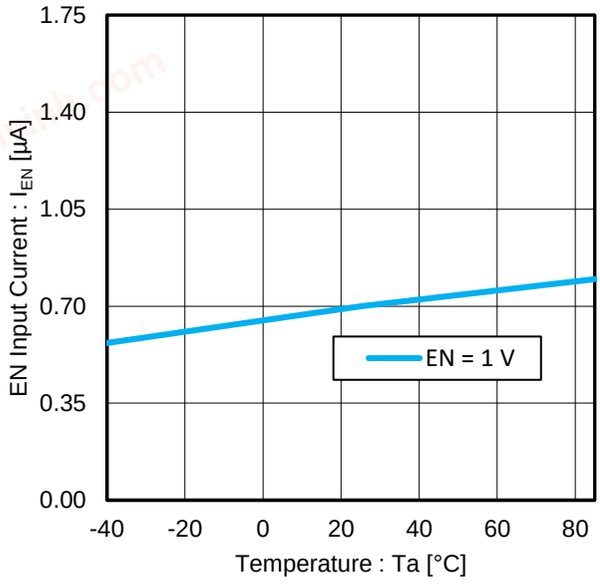


Figure 5. EN Input Current vs Temperature

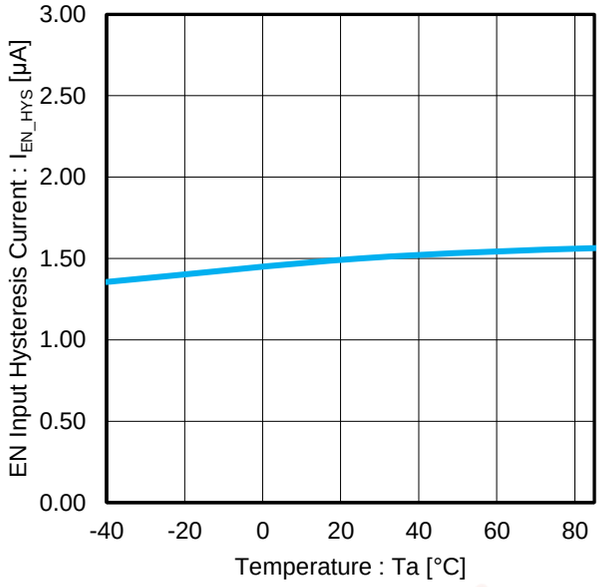


Figure 6. EN Input Hysteresis Current vs Temperature

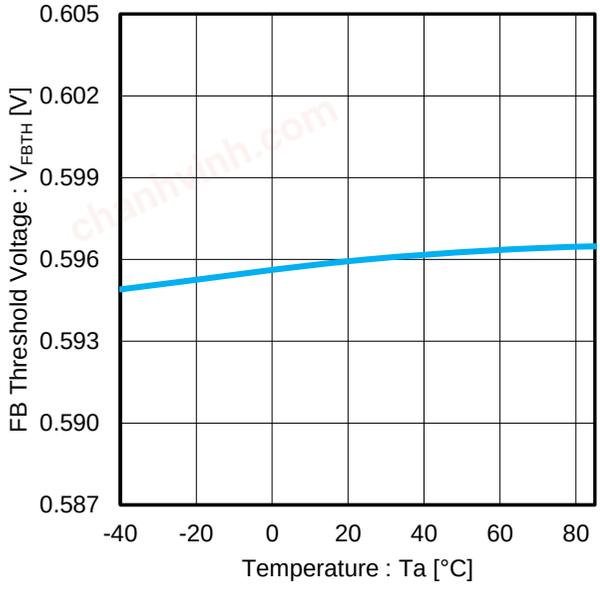


Figure 7. FB Threshold Voltage vs Temperature

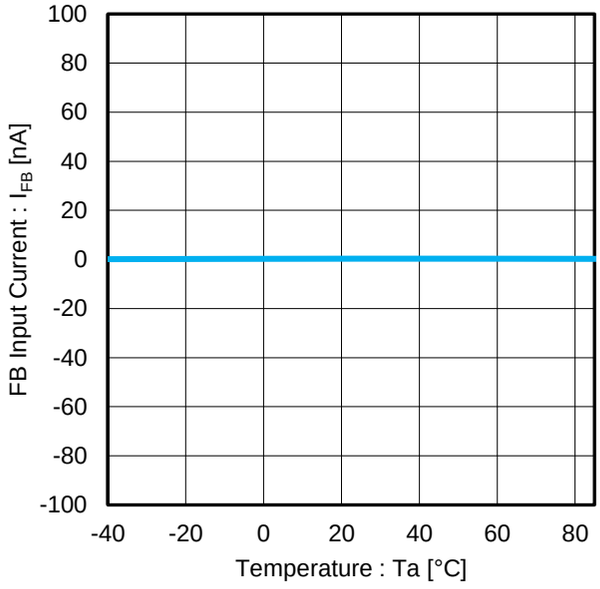


Figure 8. FB Input Current vs Temperature

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Typical Performance Curves – continued

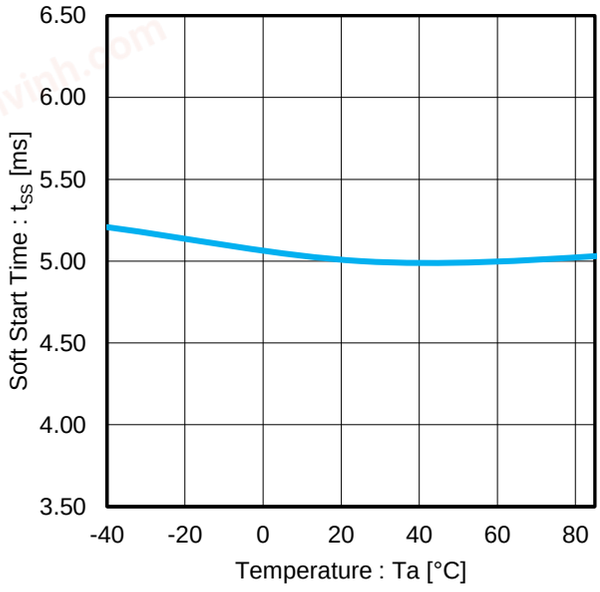


Figure 9. Soft Start Time vs Temperature

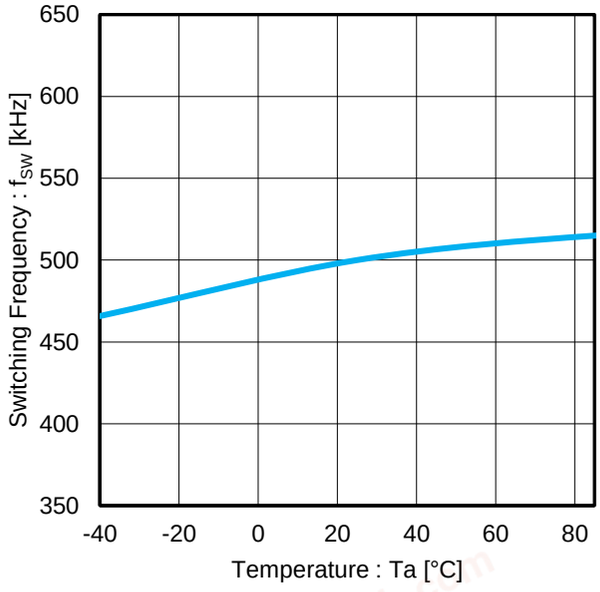


Figure 10. Switching Frequency vs Temperature

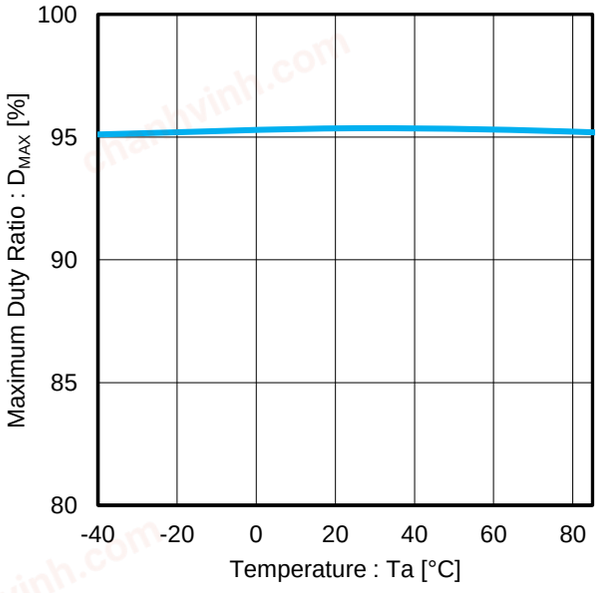


Figure 11. Maximum Duty Ratio vs Temperature

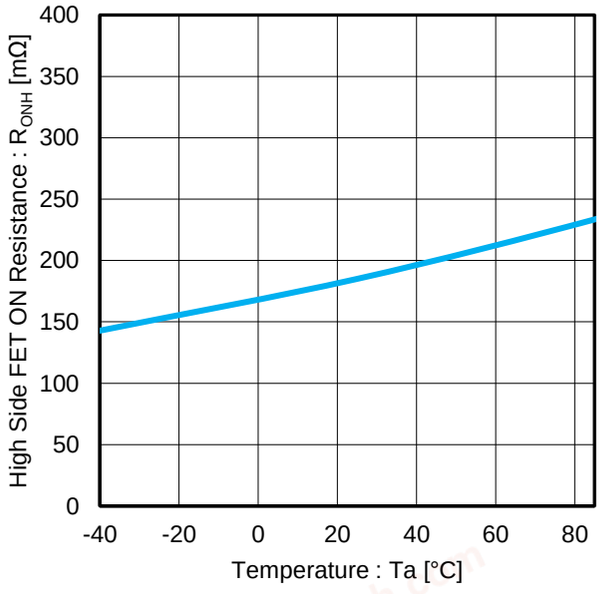


Figure 12. High Side FET ON Resistance vs Temperature

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Typical Performance Curves – continued

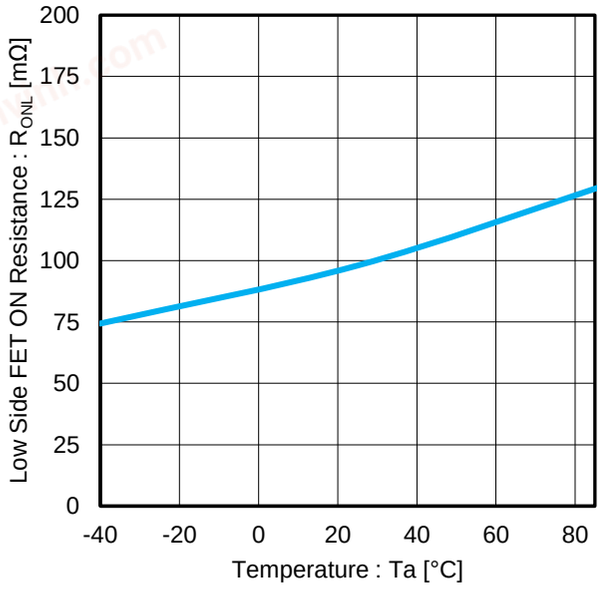


Figure 13. Low Side FET ON Resistance vs Temperature

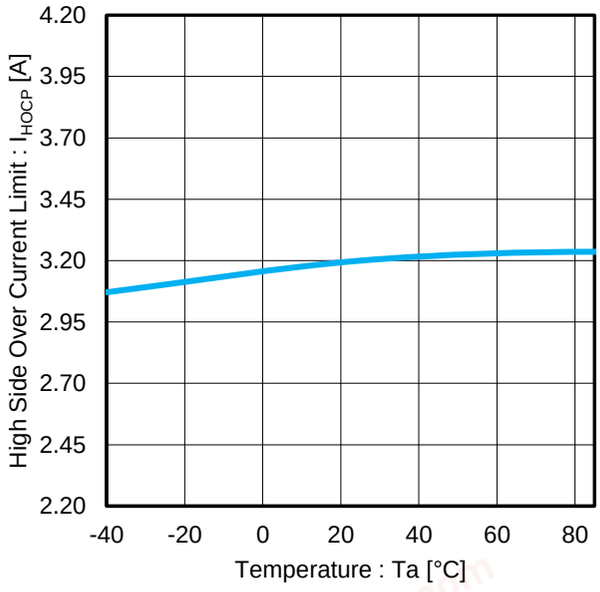


Figure 14. High Side Over Current Limit vs Temperature

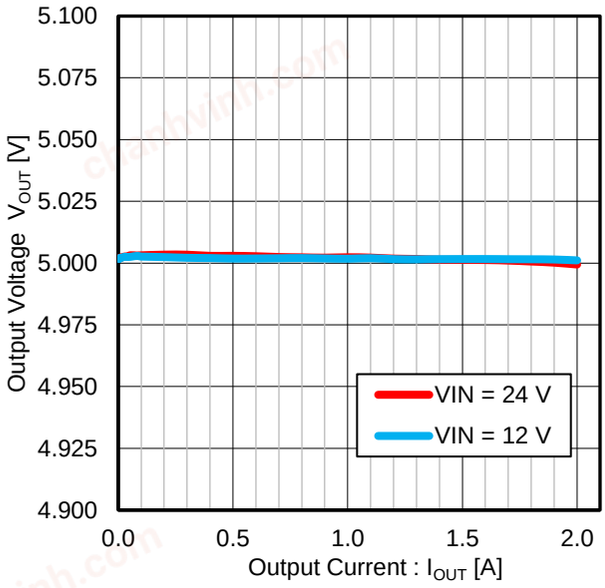


Figure 15. Output Voltage vs Output Current

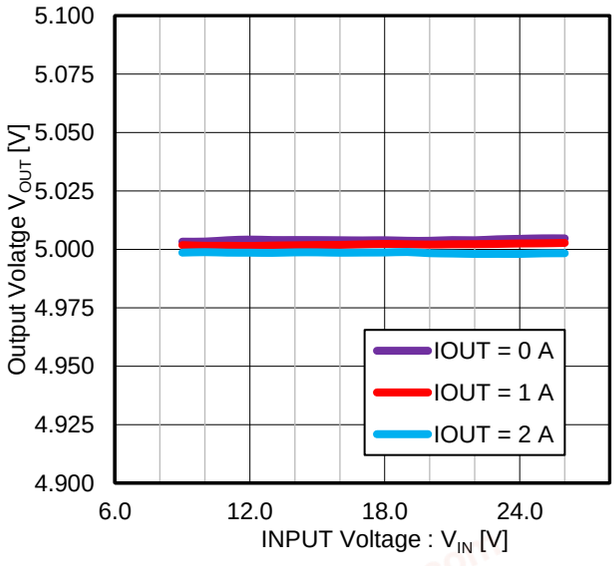


Figure 16. Output Voltage vs Input Voltage

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Typical Performance Curves – continued

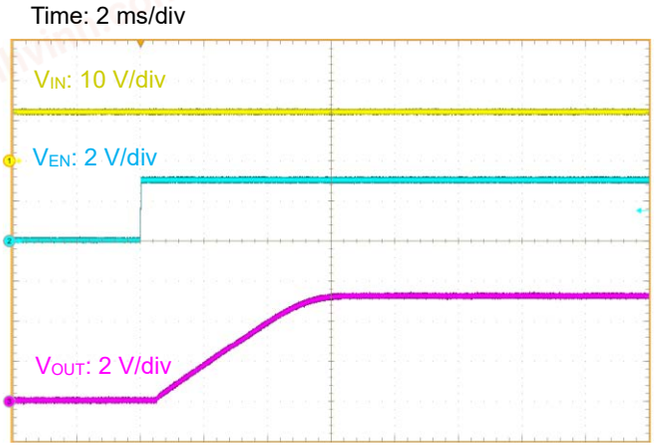


Figure 17. Start-up at No load: V_{EN} = 0 V to 3 V
(V_{IN} = 12 V, V_{OUT} = 5 V)

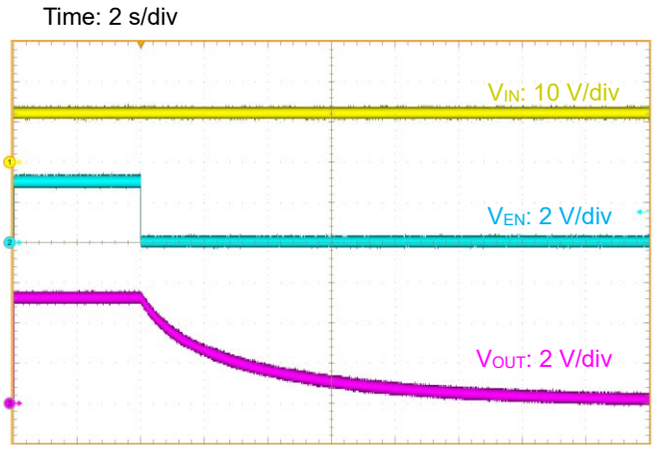


Figure 18. Shutdown at No Load V_{EN} = 3 V to 0 V
(V_{IN} = 12 V, V_{OUT} = 5 V)

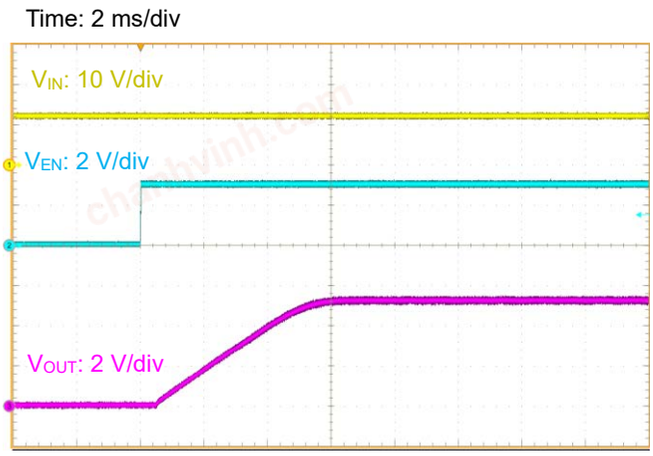


Figure 19. Start-up at R_{LOAD} = 2.5 Ω: V_{EN} = 0 V to 3 V
(V_{IN} = 12 V, V_{OUT} = 5 V)

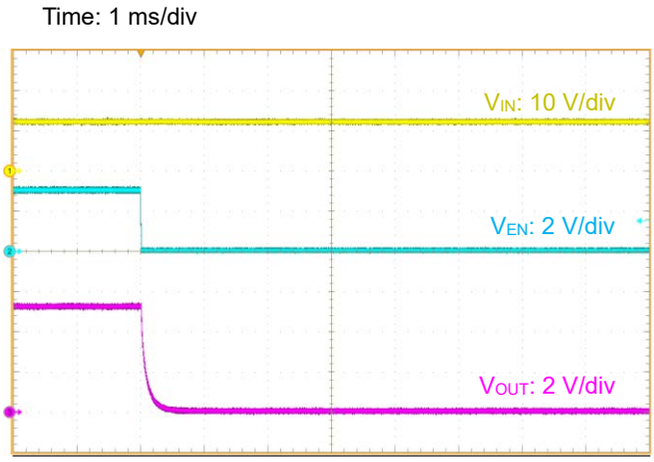


Figure 20. Shutdown at R_{LOAD} = 2.5 Ω: V_{EN} = 3 V to 0 V
(V_{IN} = 12 V, V_{OUT} = 5 V)

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Typical Performance Curves – continued

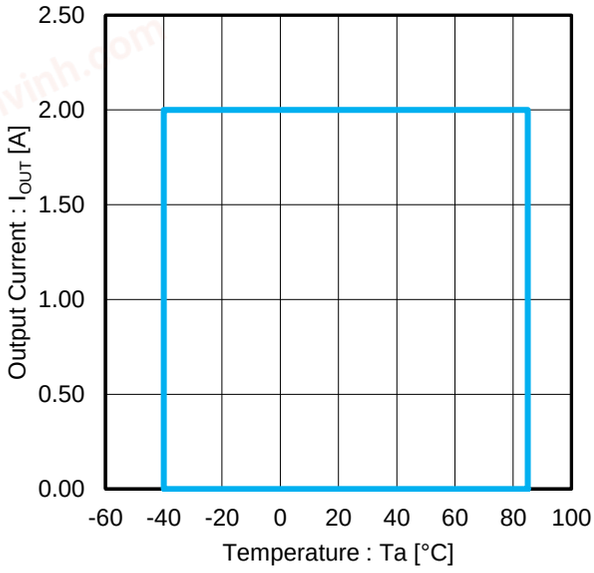


Figure 21. Output Current vs Temperature(Note 1)
Operating Range: Tj < 150 °C (V_{IN} = 12 V, V_{OUT} = 3.3 V)

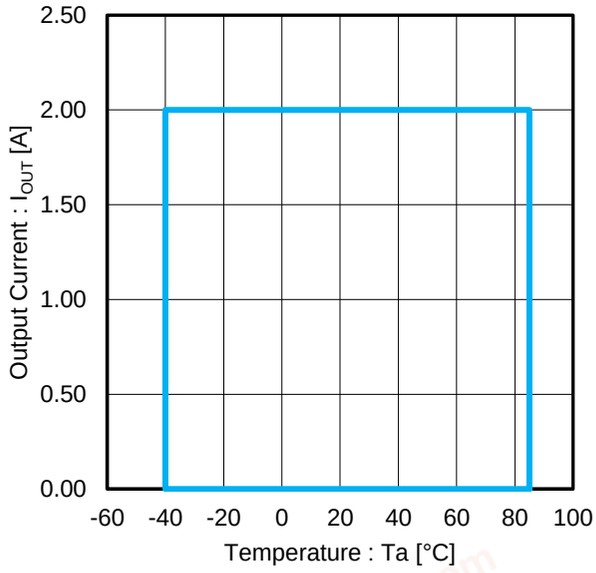


Figure 22. Output Current vs Temperature(Note 1)
Operating Range: Tj < 150 °C (V_{IN} = 12 V, V_{OUT} = 5 V)

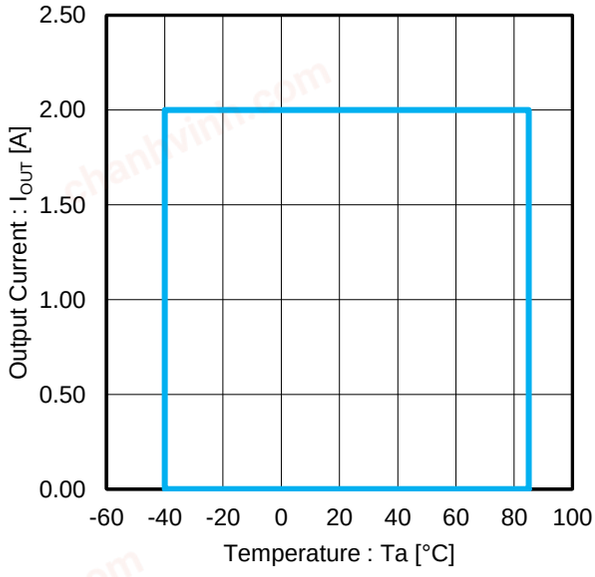


Figure 23. Output Current vs Temperature(Note 1)
Operating Range: Tj < 150 °C (V_{IN} = 24 V, V_{OUT} = 12 V)

(Note 1) Measured on FR-4 board 67.5 mm x 67.5 mm, Copper Thickness: Top and Bottom 70 µm, 2 Internal Layers 35 µm.

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Typical Performance Curves – continued

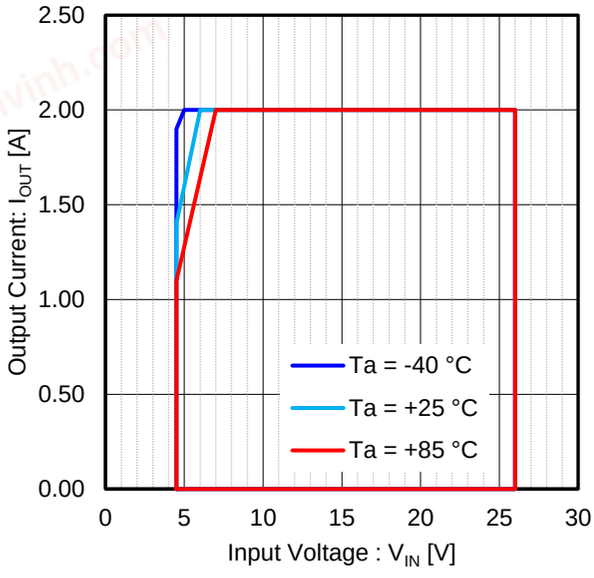


Figure 24. Output Current vs Input Voltage *(Note 1) (Note 2)*
Operating Range: Tj < 150 °C (V_{OUT} = 3.3 V)

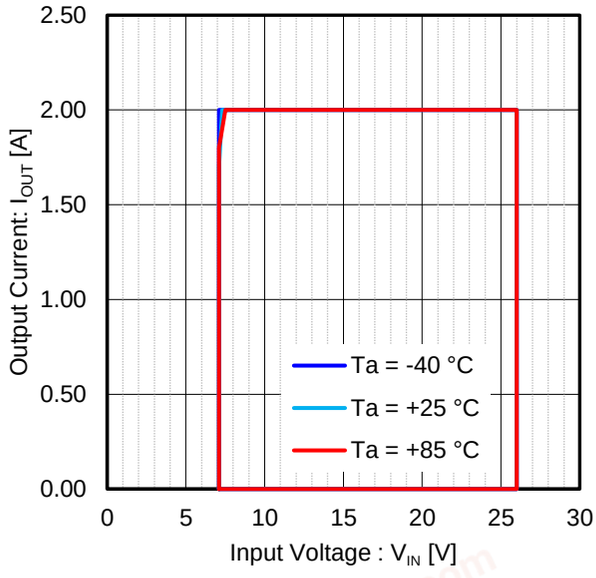


Figure 25. Output Current vs Input Voltage *(Note 1) (Note 2)*
Operating Range: Tj < 150 °C (V_{OUT} = 5.0 V)

(Note 1) Measured on FR-4 board 67.5 mm x 67.5 mm, Copper Thickness: Top and Bottom 70 µm, 2 Internal Layers 35 µm.
(Note 2) At low input voltage and high output voltage setting, I_{OUT} ability is reduced due to increase in ON resistance losses.

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Function Explanation

1. Basic Operation

(1) DC/DC Converter Operation

BD9E200FP4-Z is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes Light Load Mode control for lighter load to improve efficiency.

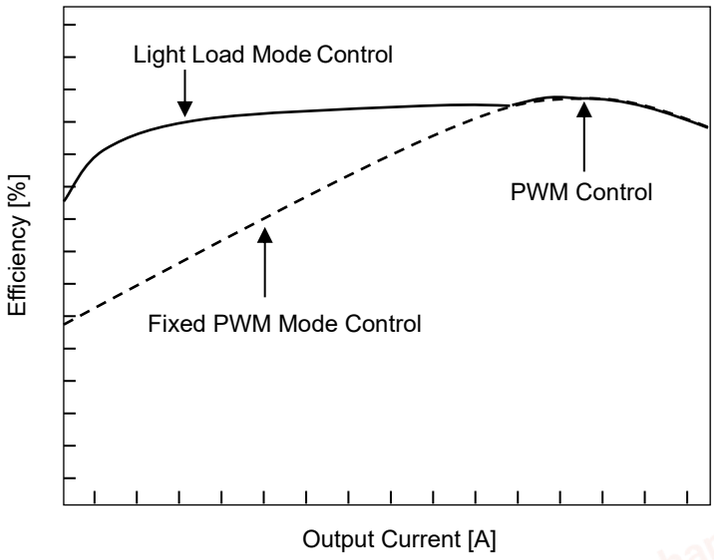


Figure 26. Efficiency Image between Light Load Mode Control and PWM Mode Control

(2) Enable Control

The startup and shutdown can be controlled by the EN voltage (V_{EN}). When V_{EN} becomes 1.21 V (Typ) or more, the internal circuit is activated and the device starts up. When V_{EN} becomes 1.19 V (Typ) or less, the device is shutdown. To enable shutdown control with the EN pin, the shutdown interval must be set to 100 µs or longer. When this pin is open, this pin is pull-up to IC internal regulator and the device is enabled.

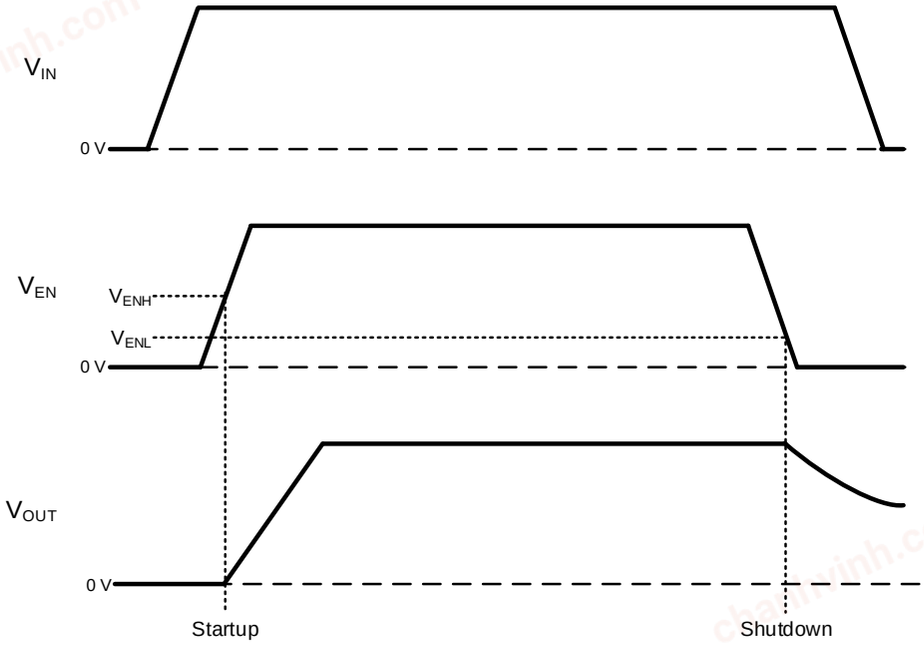


Figure 27. Startup and Shutdown with Enable Control Timing Chart

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1. Basic Operation – continued

(3) Soft Start

When V_{EN} goes high, soft start function operates and output voltage gradually rises. This soft start function can prevent overshoot of the output voltage and excessive inrush current. The soft start time t_{SS} is 5 ms (Typ).

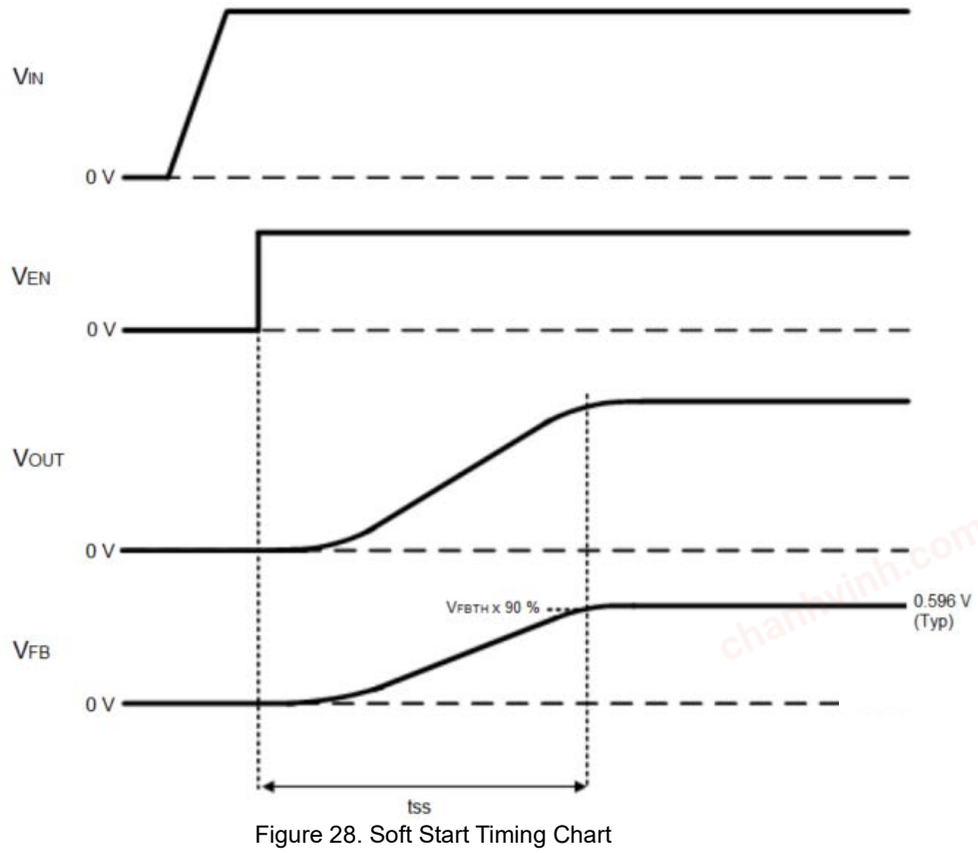


Figure 28. Soft Start Timing Chart

(4) Frequency Spread Spectrum

When soft start function (SSEND) is completed, Spread Spectrum function activates and then reducing the EMI noise level. When the Spread Spectrum function is activated, the switching frequency varies with triangular wave by ±6 % (Typ) from center frequency 500 kHz (Typ). The period of the triangular wave is 1.024 ms (Typ).

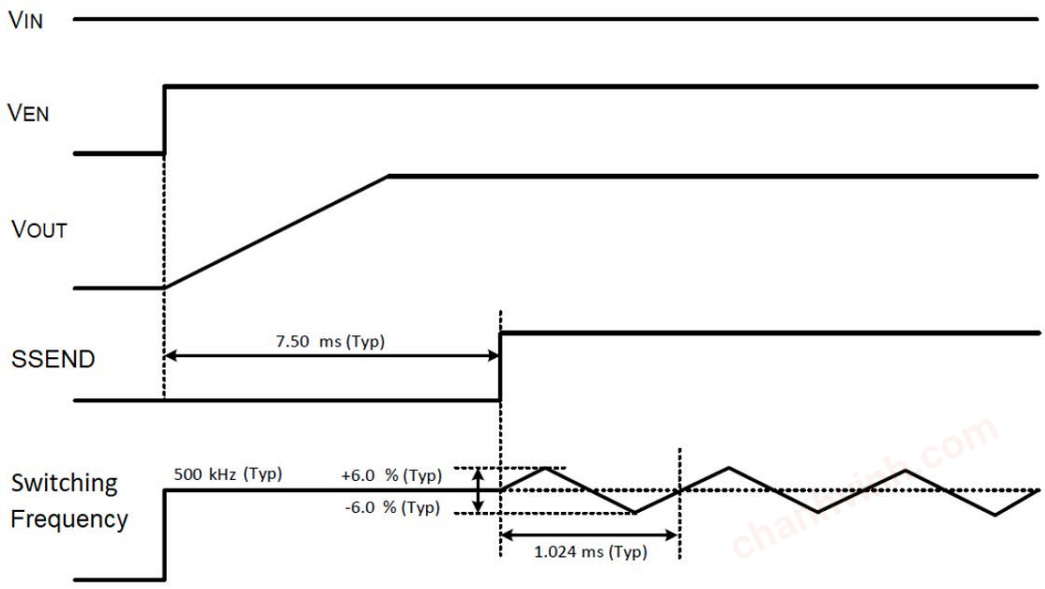


Figure 29. Frequency Spread Spectrum

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Function Explanation – continued

2. Protection

The protection circuits are intended for prevention of damage caused by unexpected accidents. Do not use the continuous protection.

(1) Over Current Protection (OCP) / Short Circuit Protection (SCP)

Over Current Protection (OCP) restricts the flowing current through the High Side FET for every switching period. SW switching is masked by 3clock cycles when OCP is detected.

Short Circuit Protection (SCP) function is a Hiccup mode. When V_{FB} remains V_{FBTH} x 70 % or less for 128 µs (Typ), the device stops the switching operation for 32.8 ms (Typ). After that, the device restarts. SCP does not operate during the soft start even if the device is in the SCP conditions. Do not exceed the maximum junction temperature (Tjmax = 150 °C) during OCP and SCP operation.

Table 1. The Operating Condition of OCP and SCP

V_{EN}	V_{FB}	Start-up	OCP	SCP
≥ 1.21 V (Typ)	≤ V_{FBTH} x 70 % (Typ)	During Soft Start	Enable	Disable
	> V_{FBTH} x 70 % (Typ)	Complete Soft Start	Enable	Disable
	≤ V_{FBTH} x 70 % (Typ)		Enable	Enable
≤ 1.19 V (Typ)	-	Shutdown	Disable	Disable

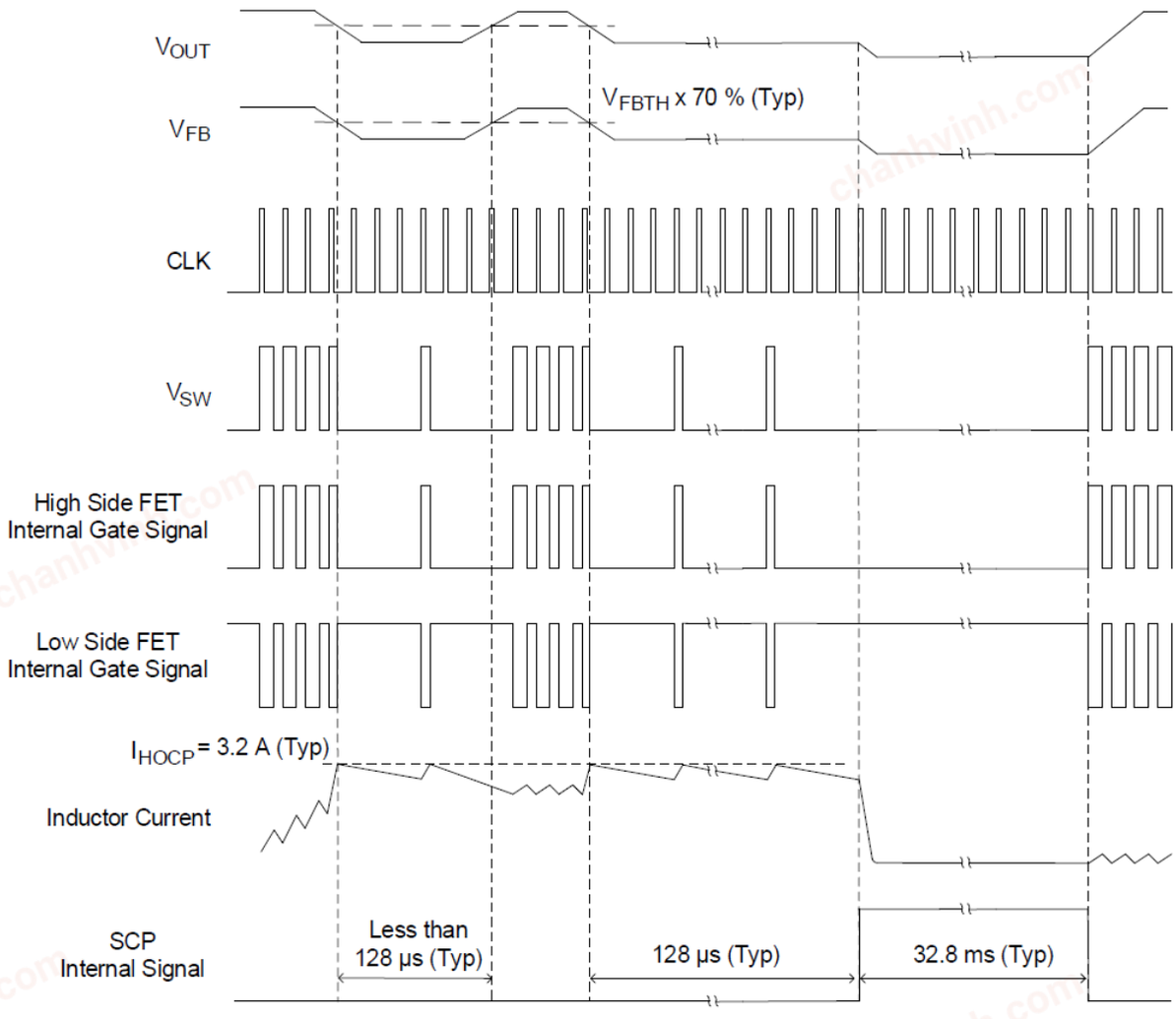


Figure 30. OCP and SCP Timing Chart

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2. Protection - continued

(2) Under Voltage Lockout Protection (UVLO)

When input voltage V_{IN} falls to 3.9 V (Typ) or less, the device is shutdown. When V_{IN} becomes 4.25 V (Typ) or more, the device starts up. The hysteresis is 350 mV (Typ).

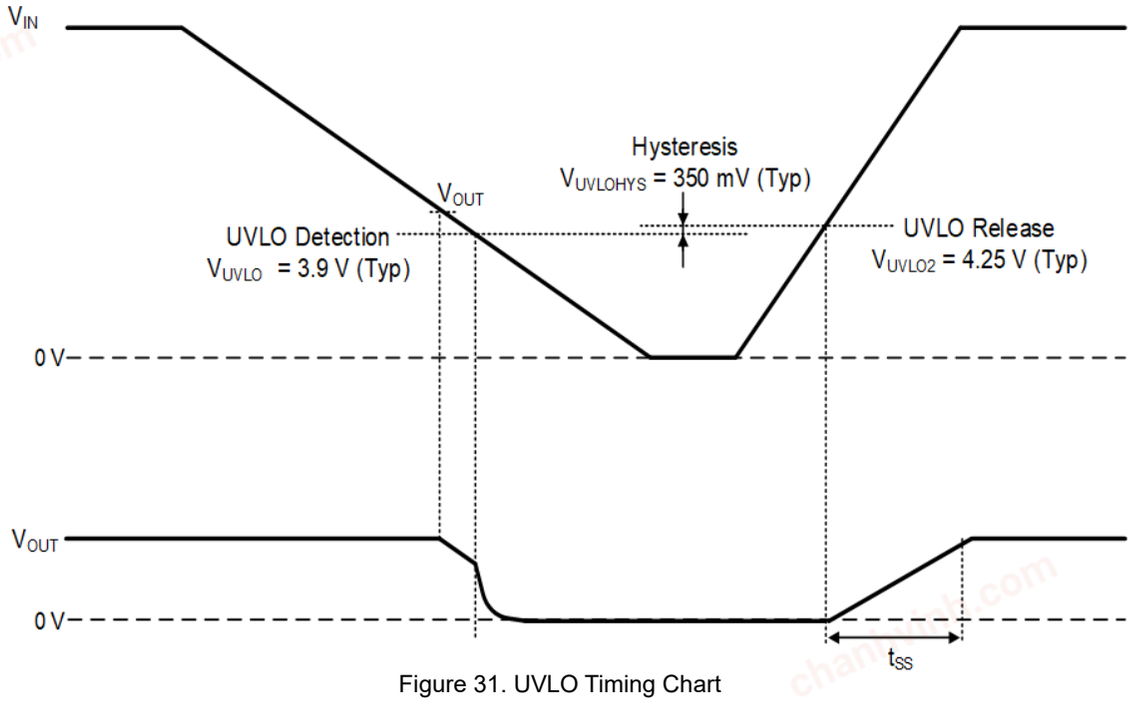


Figure 31. UVLO Timing Chart

The under voltage lock-out protection (UVLO) threshold voltages can be set higher than the internal UVLO threshold voltage by the resistor divider network connected between the VIN and EN pins.

Resistor divider network can be computed as follows

$$R_4 = \frac{V_{START} \times \frac{V_{ENL}}{V_{ENH}} - V_{STOP}}{I_{EN} \times \left(1 - \frac{V_{ENL}}{V_{ENH}}\right) + I_{EN_HYS}} \quad \Omega$$

$$R_5 = \frac{R_4 \times V_{ENL}}{V_{STOP} - V_{ENL} + R_4 \times (I_{EN} + I_{EN_HYS})} \quad \Omega$$

where as

V_{START}, V_{STOP} : external VIN UVLO setting
V_{START} - V_{STOP} = 500 mV (Typ)
V_{ENL} = 1.19 V (Typ)
V_{ENH} = 1.21 V (Typ)
I_{EN} = 0.7 µA (Typ)
I_{EN_HYS} = 1.5 µA (Typ)

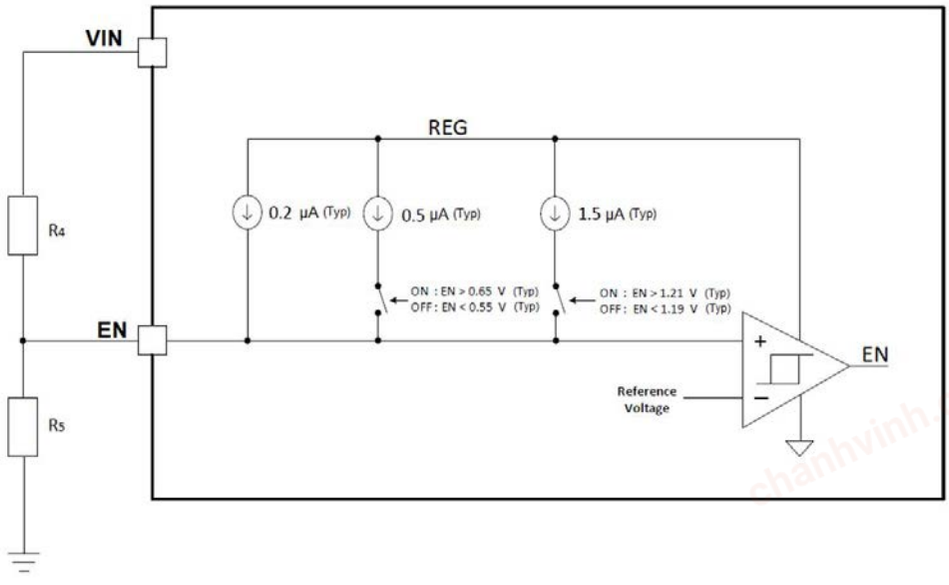


Figure 32. External UVLO Setting

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2. Protection - continued

(3) Thermal Shutdown Protection (TSD)

Thermal shutdown circuit prevents heat damage to the IC. The device should always operate within the IC's maximum junction temperature rating (Tjmax = 150 °C). However, if it continues exceeding the rating and the junction temperature Tj rises to 175 °C (Typ), the TSD circuit is activated and it turns the output MOSFETs off. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. The TSD threshold has a hysteresis of 25 °C (Typ). Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings. Therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

(4) Over Voltage Protection (OVP)

When the FB voltage V_{FB} exceeds V_{FBTH} x 120 % (Typ) or more, the output MOSFETs are turned off to prevent the increase in the output voltage. After the V_{FB} falls V_{FBTH} x 115 % (Typ) or less, the output MOSFETs are returned to normal operation condition. Switching operation restarts after V_{FB} falls below V_{FBTH} (Typ).

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Application Examples

1. V_{IN} = 9 V to 24 V, V_{OUT} = 3.3 V

Table 2. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	9 V to 24 V (Typ)
Output Voltage	V_{OUT}	3.3 V (Typ)
Maximum Output Current	I_{OUTMAX}	2 A
Temperature	Ta	25 °C

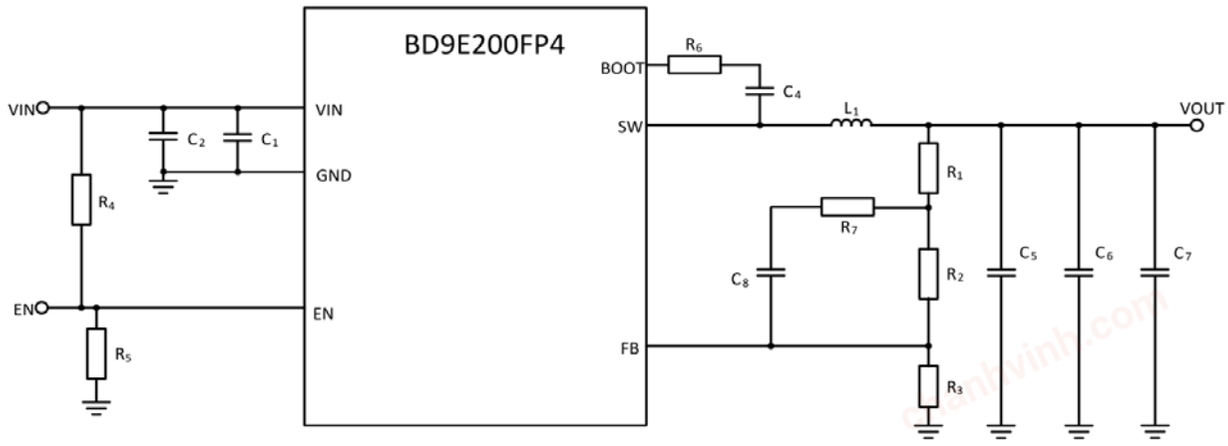


Figure 33. Application Circuit

Table 3. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L_1	10 µH	1217AS-H-100M	8080	Murata
C_1 *(Note 1)*	0.1 µF (50 V, X5R, ±10 %)	GRM155R61H104KE14	1005	Murata
C_2 *(Note 2)*	10 µF (100 V, X7S, ±10 %)	GRM32EC72A106KE05	3225	Murata
C_4 *(Note 3)*	0.1 µF (50 V, X5R, ±10 %)	GRM155R61H104KE14	1005	Murata
R_6	Short	-	-	-
C_5 *(Note 4)*	22 µF (25 V, X7R, ±10 %)	GRM32ER71E226KE15	3225	Murata
C_6 *(Note 4)*	22 µF (25 V, X7R, ±10 %)	GRM32ER71E226KE15	3225	Murata
C_7 *(Note 4)*	-	-	-	-
C_8	56 pF (50 V, C0G, ±5 %)	GRM0335C1H560JA01D	0603	Murata
R_7	Short	-	-	-
R_1 *(Note 5)*	Short	-	-	-
R_2	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	1005	ROHM
R_3	22 kΩ (1 %, 1/16 W)	MCR01MZPF2202	1005	ROHM
R_4 *(Note 6)*	510 kΩ (1 %, 1/16 W)	MCR01MZPF5103	1005	ROHM
R_5 *(Note 6)*	82 kΩ (1 %, 1/16 W)	MCR01MZPF8202	1005	ROHM

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1 µF ceramic capacitor C_1 as close as possible to the VIN pin and the GND pin.
(Note 2) For the input capacitor C_2, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3.0 µF.
(Note 3) For the bootstrap capacitor C_4, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022 µF.
(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor C_5, C_6 and C_7, the loop response characteristics may change. Confirm the actual application.
(Note 5) R_1 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_1, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.
(Note 6) R_4 and R_5 are used to set VIN UVLO to higher voltage setting. Calculation is explained in page 17.

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1. V_{IN} = 9 V to 24 V, V_{OUT} = 3.3 V – continued

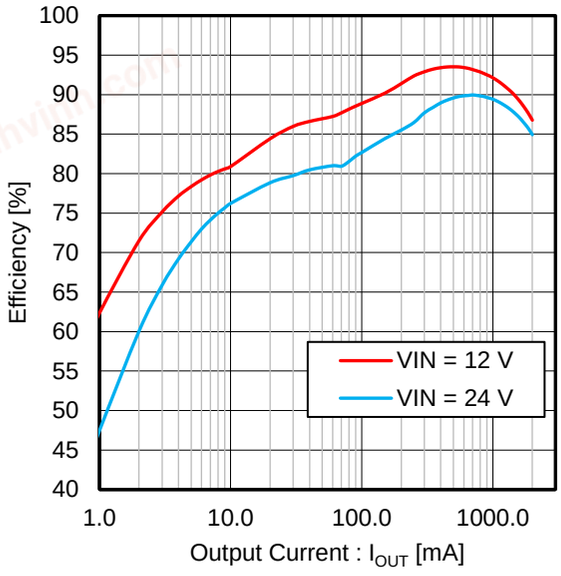


Figure 34. Efficiency vs Output Current

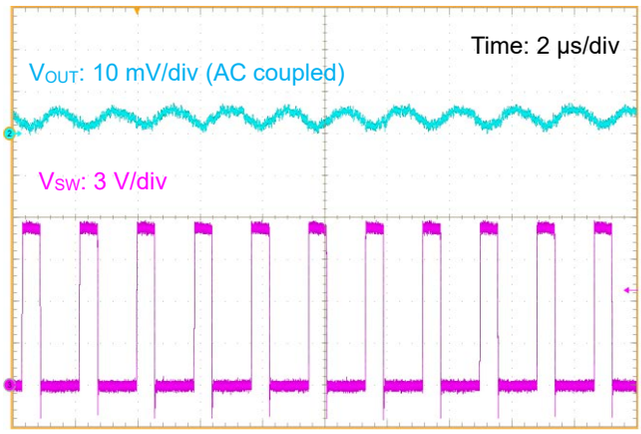


Figure 35. Output Ripple Voltage (V_{IN} = 12 V, I_{OUT} = 2 A)

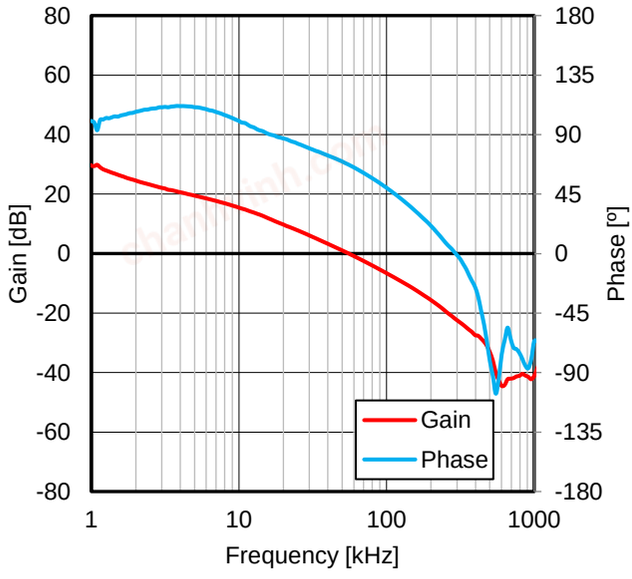


Figure 36. Frequency Characteristics
(V_{IN} = 12 V, I_{OUT} = 2 A)

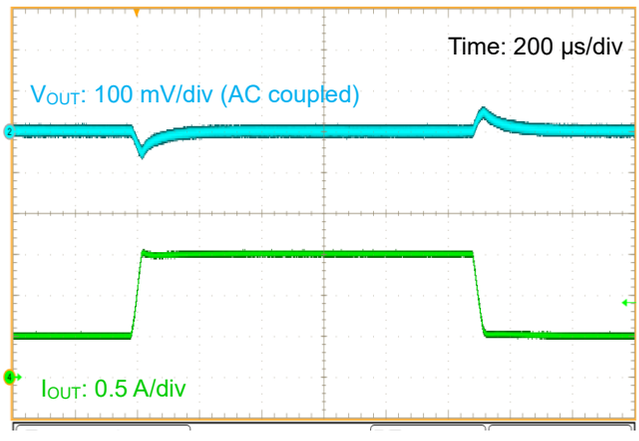


Figure 37. Load Transient Response
(V_{IN} = 12 V, I_{OUT} = 0.5 A to 1.5 A)

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Application Examples – continued

2. V_{IN} = 9 V to 24 V, V_{OUT} = 5 V

Table 4. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	9 V to 24 V (Typ)
Output Voltage	V_{OUT}	5 V (Typ)
Maximum Output Current	I_{OUTMAX}	2 A
Temperature	Ta	25 °C

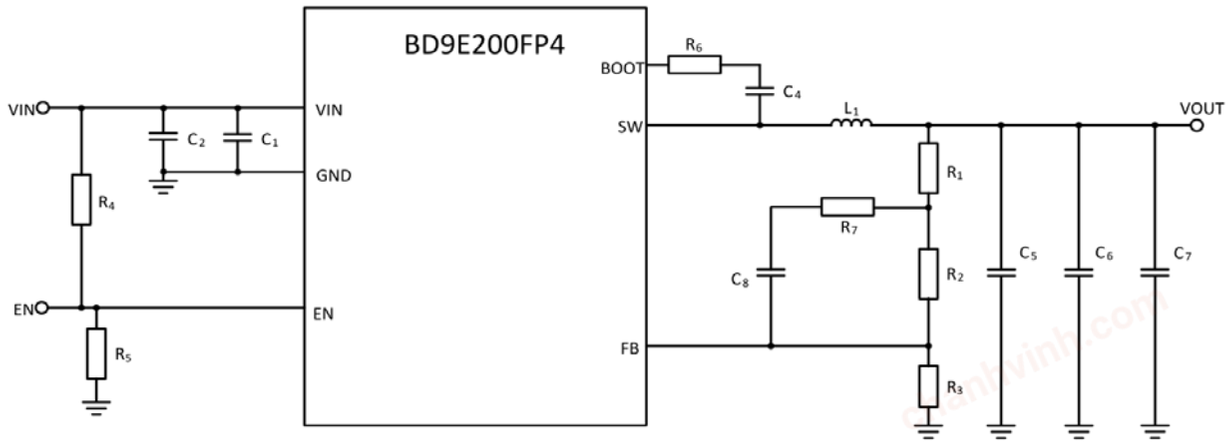


Figure 38. Application Circuit

Table 5. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L_1	15 µH	1217AS-H-150M	8080	Murata
C_1 *(Note 1)*	0.1 µF (50 V, X5R, ±10 %)	GRM155R61H104KE14	1005	Murata
C_2 *(Note 2)*	10 µF (100 V, X7S, ±10 %)	GRM32EC72A106KE05	3225	Murata
C_4 *(Note 3)*	0.1 µF (50 V, X5R, ±10 %)	GRM155R61H104KE14	1005	Murata
R_6	Short	-	-	-
C_5 *(Note 4)*	22 µF (25 V, X7R, ±10 %)	GRM32ER71E226KE15	3225	Murata
C_6 *(Note 4)*	22 µF (25 V, X7R, ±10 %)	GRM32ER71E226KE15	3225	Murata
C_7 *(Note 4)*	-	-	-	-
C_8	75 pF (50 V, C0G, ±5 %)	GRM0335C1H750JA01D	0603	Murata
R_7	Short	-	-	-
R_1 *(Note 5)*	0.82 kΩ (1 %, 1/16 W)	MCR01MZPF8200	1005	ROHM
R_2	110 kΩ (1 %, 1/16 W)	MCR01MZPF1103	1005	ROHM
R_3	15 kΩ (1 %, 1/16 W)	MCR01MZPF1502	1005	ROHM
R_4 *(Note 6)*	510 kΩ (1 %, 1/16 W)	MCR01MZPF5103	1005	ROHM
R_5 *(Note 6)*	82 kΩ (1 %, 1/16 W)	MCR01MZPF8202	1005	ROHM

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1 µF ceramic capacitor C_1 as close as possible to the VIN pin and the GND pin.
(Note 2) For the input capacitor C_2, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3.0 µF.
(Note 3) For the bootstrap capacitor C_4, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022 µF.
(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor C_5, C_6 and C_7, the loop response characteristics may change. Confirm the actual application.
(Note 5) R_1 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_1, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.
(Note 6) R_4 and R_5 are used to set VIN UVLO to higher voltage setting. Calculation is explained in page 17.

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2. V_{IN} = 9 V to 24 V, V_{OUT} = 5 V – continued

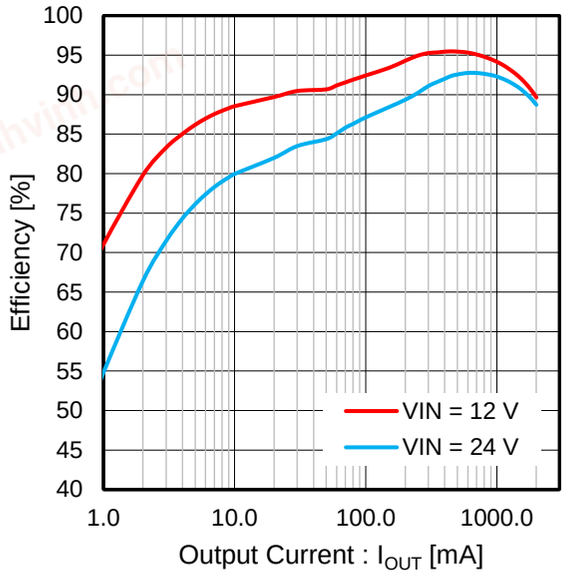


Figure 39. Efficiency vs Output Current

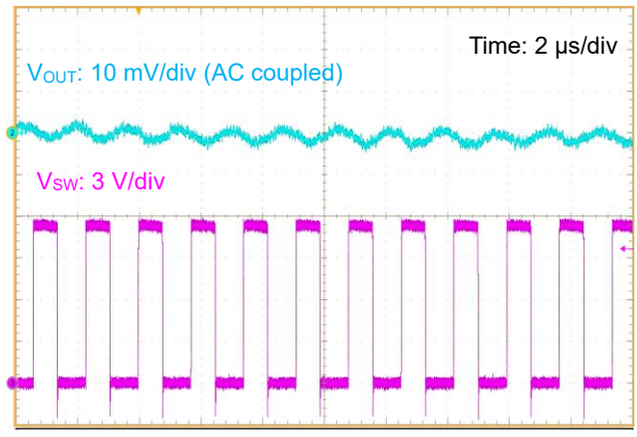


Figure 40. Output Ripple Voltage (V_{IN} = 12 V, I_{OUT} = 2 A)

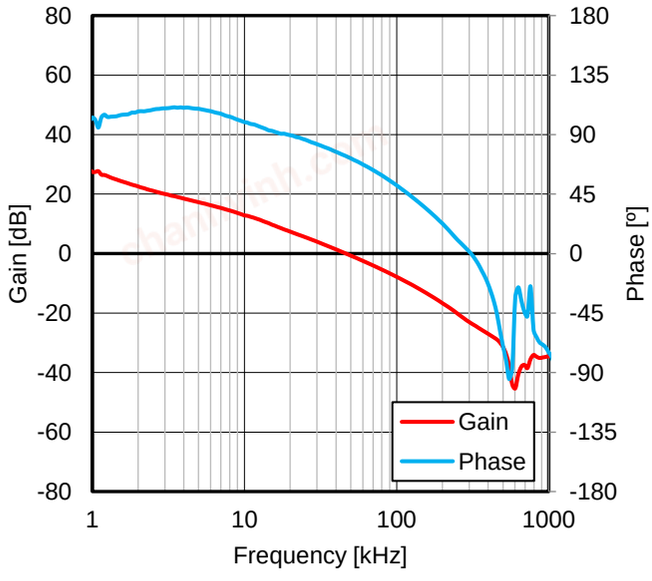


Figure 41. Frequency Characteristics
(V_{IN} = 12 V, I_{OUT} = 2 A)

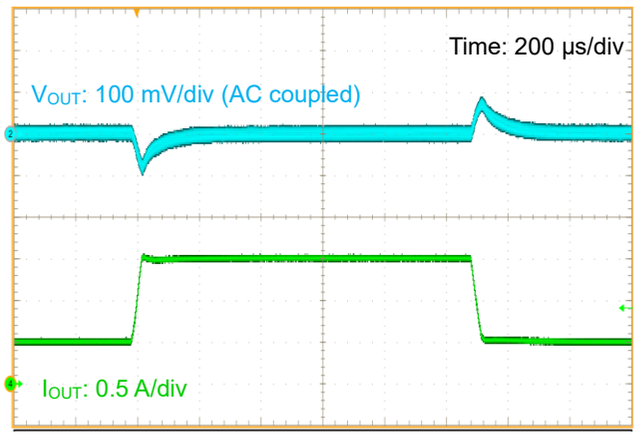


Figure 42. Load Transient Response
(V_{IN} = 12 V, I_{OUT} = 0.5 A to 1.5 A)

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Application Examples - continued

3. V_{IN} = 24 V, V_{OUT} = 12 V

Table 6. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	24 V (Typ)
Output Voltage	V_{OUT}	12 V (Typ)
Maximum Output Current	I_{OUTMAX}	2 A
Temperature	Ta	25 °C

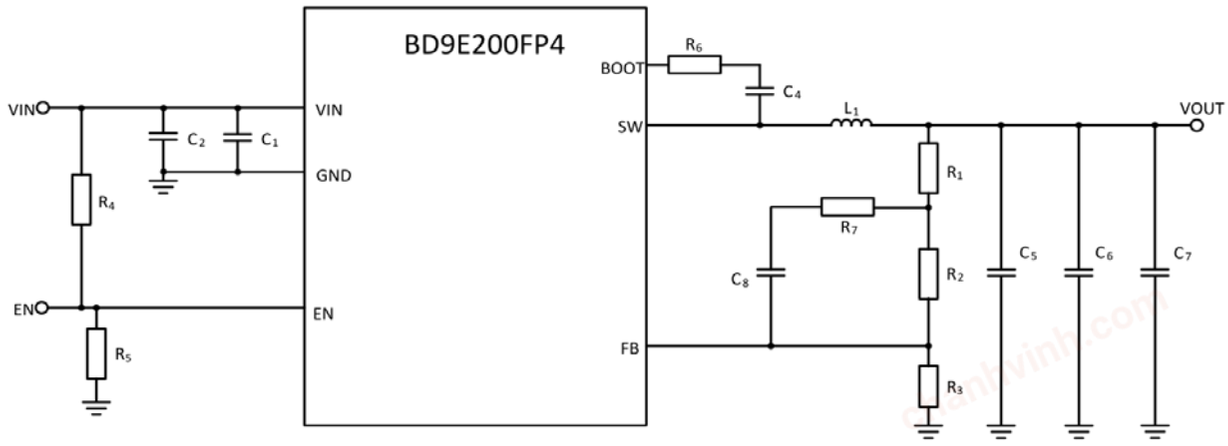


Figure 43. Application Circuit

Table 7. Recommended Component Values

Part No.	Value	Part Name	Size Code (mm)	Manufacturer
L_1	22 µH	1217AS-H-220M	8080	Murata
C_1 *(Note 1)*	0.1 µF (50 V, X5R, ±10 %)	GRM155R61H104KE14	1005	Murata
C_2 *(Note 2)*	10 µF (100 V, X7S, ±10 %)	GRM32EC72A106KE05	3225	Murata
C_4 *(Note 3)*	0.1 µF (50 V, X5R, ±10 %)	GRM155R61H104KE14	1005	Murata
R_6	Short	-	-	-
C_5 *(Note 4)*	22 µF (25 V, X7R, ±10 %)	GRM32ER71E226KE15	3225	Murata
C_6 *(Note 4)*	22 µF (25 V, X7R, ±10 %)	GRM32ER71E226KE15	3225	Murata
C_7 *(Note 4)*	-	-	-	-
C_8	100 pF (50 V, C0G, ±5 %)	GRM0335C1H101JA01D	0603	Murata
R_7	Short	-	-	-
R_1 *(Note 5)*	Short	-	-	-
R_2	130 kΩ (1 %, 1/16 W)	MCR01MZPF1303	1005	ROHM
R_3	6.8 kΩ (1 %, 1/16 W)	MCR01MZPF6801	1005	ROHM
R_4 *(Note 6)*	470 kΩ (1 %, 1/16 W)	MCR01MZPF4703	1005	ROHM
R_5 *(Note 6)*	33 kΩ (1 %, 1/16 W)	MCR01MZPF3302	1005	ROHM

(Note 1) In order to reduce the influence of high frequency noise, connect a 0.1 µF ceramic capacitor C_1 as close as possible to the VIN pin and the GND pin.
(Note 2) For the input capacitor C_2, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 3.0 µF.
(Note 3) For the bootstrap capacitor C_4, take temperature characteristics, DC bias characteristics, etc. into consideration to set to the actual capacitance of no less than 0.022 µF.
(Note 4) In case of changing the actual capacitance value due to temperature characteristics, DC bias characteristics, etc. of the output capacitor C_5, C_6 and C_7, the loop response characteristics may change. Confirm the actual application.
(Note 5) R_1 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_1, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.
(Note 6) R_4 and R_5 are used to set VIN UVLO to higher voltage setting. Calculation is explained in page 17.

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3. V_{IN} = 24 V, V_{OUT} = 12 V – continued

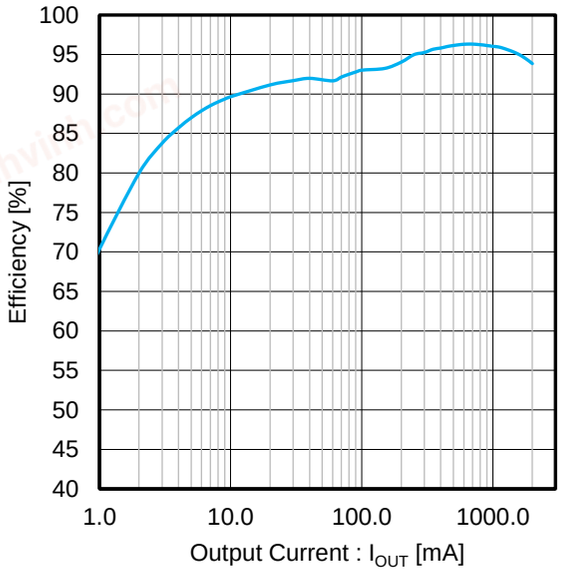


Figure 44. Efficiency vs Output Current

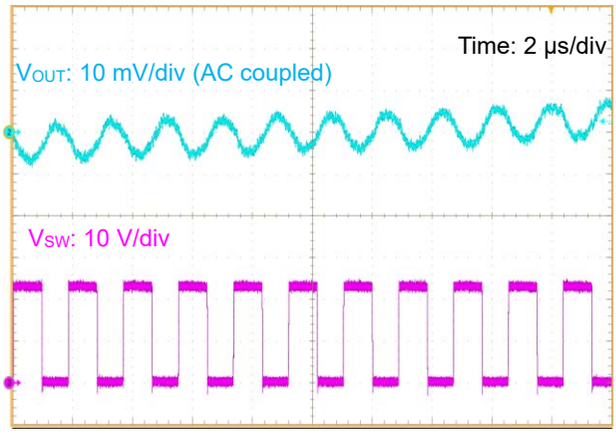


Figure 45. Output Ripple Voltage (V_{IN} = 24 V, I_{OUT} = 2 A)

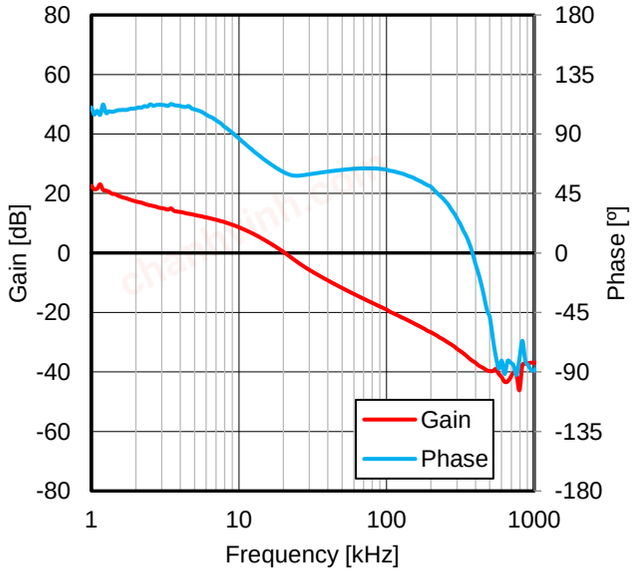


Figure 46. Frequency Characteristics
(V_{IN} = 24 V, I_{OUT} = 2 A)

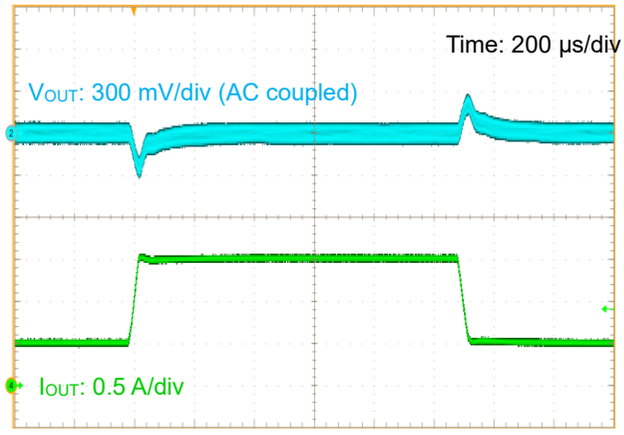


Figure 47. Load Transient Response
(V_{IN} = 24 V, I_{OUT} = 0.5 A to 1.5 A)

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Selection of Components Externally Connected

Contact us if not use the recommended component values in Application Examples.

1. Input Capacitor

Use ceramic type capacitor for the input capacitor. The input capacitor is used to reduce the input ripple noise and it is effective by being placed as close as possible to the VIN pin. Set the capacitor value so that it does not fall to 3 µF considering the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. The PCB layout and the position of the capacitor may lead to IC malfunction. Refer to the notes on the PCB layout on PCB Layout Design when designing PCB layout. In addition, the capacitor with value 0.1 µF can be connected as close as possible to the VIN pin and the GND pin in order to reduce the high frequency noise.

2. Output LC Filter

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. For recommended inductance, use the values listed in Table 8.

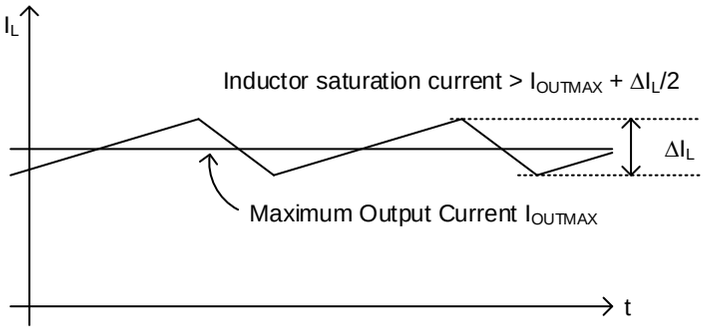


Figure 48. Waveform of Inductor Current

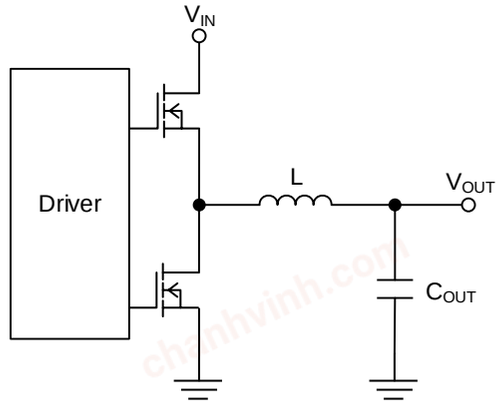


Figure 49. Output LC Filter Circuit

For example, given that V_{IN} = 12 V, V_{OUT} = 5 V, L = 15 µH, and the switching frequency f_{SW} = 500 kHz, Inductor current ΔI_L can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L} = 0.389 \quad [\mathrm{A}]$$

The rated current of the inductor (Inductor saturation current) must be larger than the sum of the maximum output current I_{OUTMAX} and 1/2 of the inductor ripple current ΔI_L.

Use ceramic type capacitor for the output capacitor C_{OUT}. For recommended actual capacitance, use the values listed in Table 8. C_{OUT} affects the output ripple voltage. Select C_{OUT} so that it must satisfy the required ripple voltage characteristics.

The output ripple voltage can be estimated by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \quad [\mathrm{V}]$$

where:

R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.

For example, given that C_{OUT} = 44 µF and R_{ESR} = 5 mΩ, ΔV_{RPL} can be calculated as below.

$$\Delta V_{RPL} = 0.389\ A \times \left(5\ m\Omega + \frac{1}{8 \times 44\ \mu F \times 500\ kHz} \right) = 4.15 \ \ [\mathrm{mV}]$$

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2. Output LC Filter – continued

In addition, the total capacitance connected to V_{OUT} needs to satisfy the value obtained by the following equation.

$$C_{OUTMAX} < \frac{t_{SSMIN}}{V_{OUT}} \times (I_{OUTSS} - I_{OUTMAX} - \frac{\Delta I_L}{2}) \quad [F]$$

where:
t_{SSMIN} is the minimum soft start time.
V_{OUT} is the output voltage.
I_{OUTMAX} is the maximum output current.
ΔI_L is the inductor ripple current.
I_{OUTSS} is the maximum output current during soft start.

For example, given that V_{IN} = 12 V, V_{OUT} = 5.0 V, L = 15 µH, f_{SW} = 500 kHz (Typ), t_{SSMIN} = 3.5 ms, I_{OUTMAX} = 2 A, and I_{OUTSS} = 2.5 A, C_{OUTMAX} can be calculated as below.

$$C_{OUTMAX} < \frac{3.5\ ms}{5.0\ V} \times \left(2.5\ A - 2\ A - \frac{0.389\ A}{2}\right) = 214 \quad [\mu F]$$

If the total capacitance connected to V_{OUT} is larger than C_{OUTMAX}, over current protection may be activated by the inrush current at startup and prevented to turn on the output. Confirm this on the actual application.

Table 8. Recommended External Parts Value

V_{IN} [V]	V_{OUT} [V]	Inductor L [µH]	C_{OUT_EFF} (Note 1) [µF]	R_2 [kΩ]	R_3 [kΩ]	C_{FB} [pF]
9 to 24	3.3	10	44	100	22	56
9 to 24	5	15	44	110.82	15	75
24	12	22	44	130	6.8	100

(Note 1) C_{OUT_EFF} is the sum of actual output capacitance.

3. Output Voltage Setting, FB Capacitor

The output voltage can be set by the feedback resistance ratio connected to the FB pin. For recommended R_2 and R_3 use the values listed in Table 8.

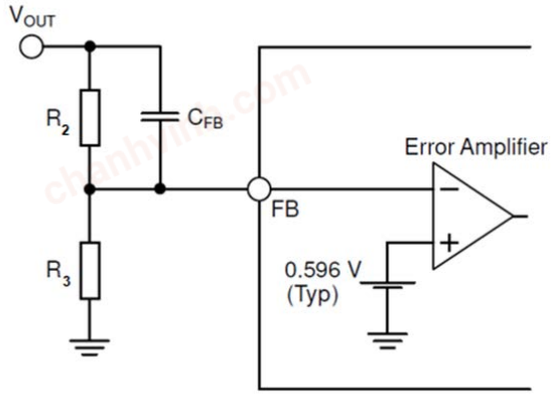


Figure 50. Feedback Resistor Circuit

The output voltage V_{OUT} can be calculated as below.

$$V_{OUT} = \frac{R_2+R_3}{R_3} \times 0.596 \ [V]$$

$$0.7 \leq V_{OUT} \leq (V_{IN} \times 0.8) \quad [V]$$

4. Bootstrap Capacitor

The bootstrap capacitor 0.1 µF is recommended. Connect the capacitor between the SW pin and the BOOT pin. For the capacitance, take temperature characteristics, DC bias characteristics, and etc. into consideration to set to the actual capacitance of no less than 0.022 µF.

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PCB Layout Design

PCB layout design for DC/DC converter is very important. Appropriate layout can avoid various problems concerning power supply circuit. Figure 51-a to Figure 51-c show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 51-a is a current path when H-side switch is ON and L-side switch is OFF, the Loop 2 in Figure 51-b is when H-side switch is OFF and L-side switch is ON. The thick line in Figure 51-c shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element H-side and L-side switch change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series "PCB Layout Techniques of Buck Converter".

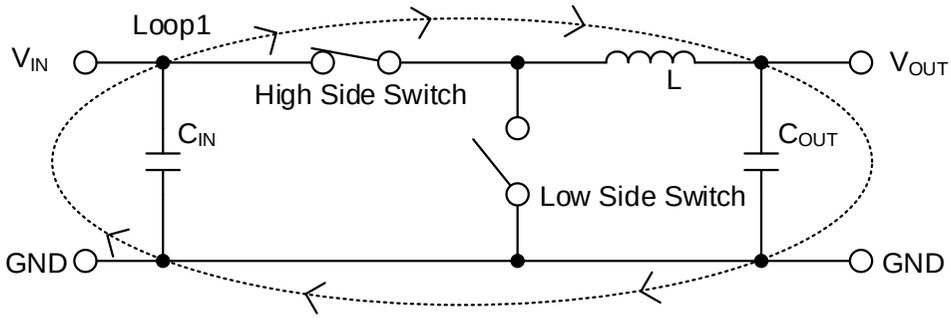


Figure 51-a. Current Path when High Side Switch = ON, Low Side Switch = OFF

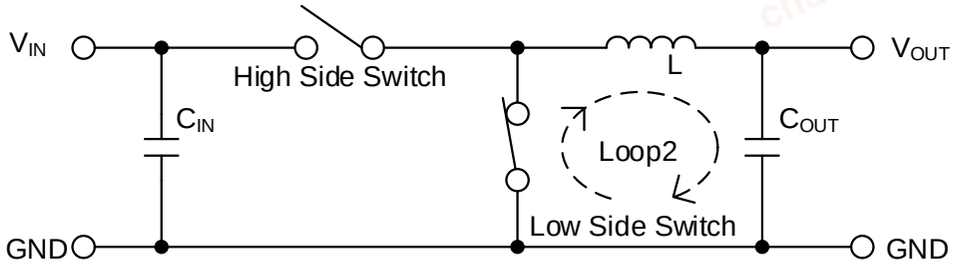


Figure 51-b. Current Path when High Side Switch = OFF, Low Side Switch = ON

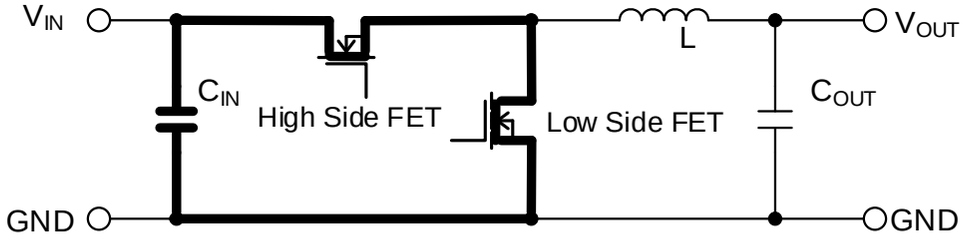


Figure 51-c. Difference of Current and Critical Area in Layout

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PCB Layout Design – continued

When designing the PCB layout, pay attention to the following points:

- Connect the input capacitor C_1 and C_2 as close as possible to the VIN pin and the GND pin on the same plane as the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern L as thick and as short as possible.
- The feedback line connected to the FB pin should be as far away from the SW nodes as possible.
- Place the output capacitor C_5, C_6 and C_7 away from input capacitor C_1 and C_2 to avoid harmonics noise from the input.
- R_1 is provided for the measurement of feedback frequency characteristics (optional). By inserting a resistor into R_1, it is possible to measure the frequency characteristics of feedback (phase margin) using FRA etc. R_1 is short-circuited for normal use.

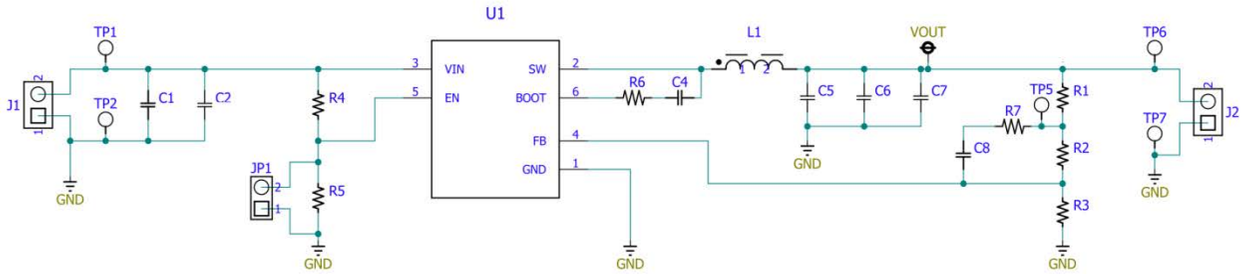


Figure 52. Application Circuit

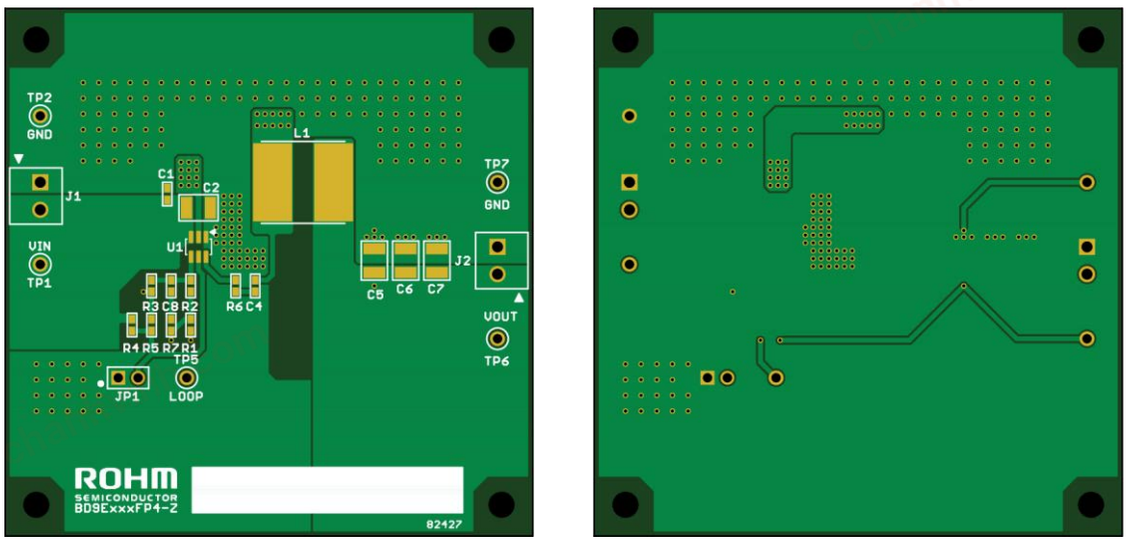
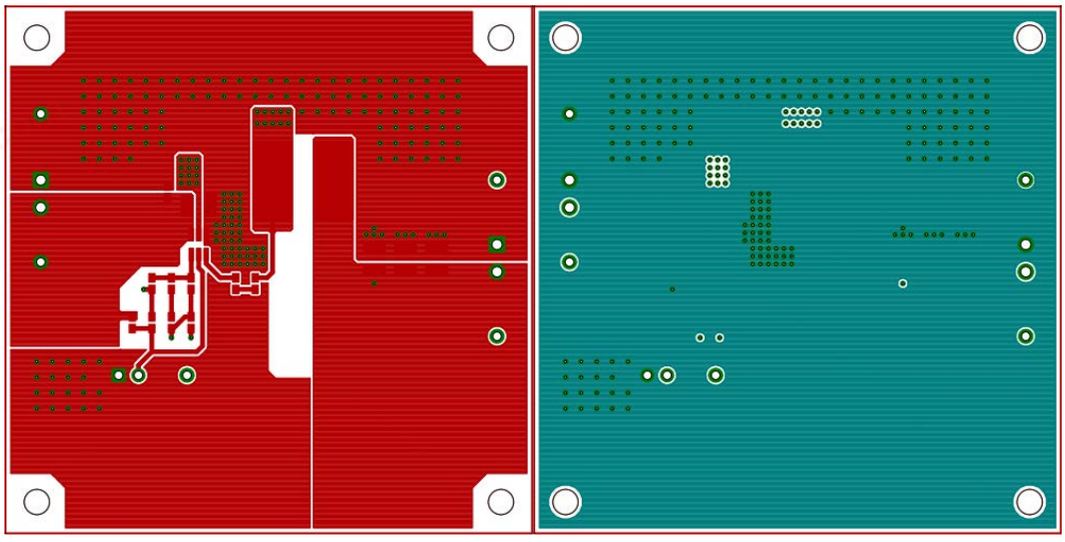


Figure 53. Example of PCB Layout (Silkscreen Overlay)

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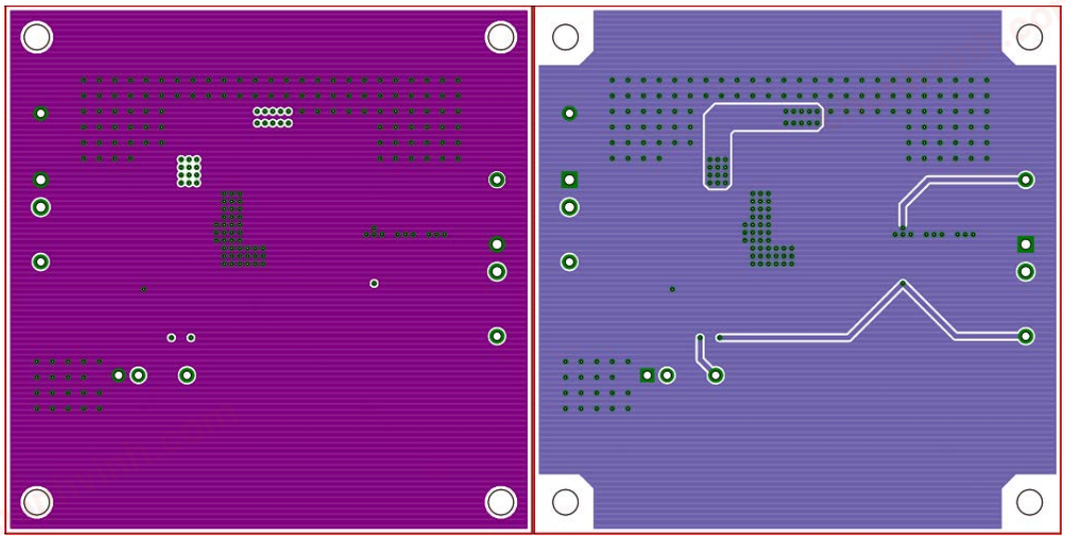
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PCB Layout Design – continued



Top Layer

Inner 1 Layer



Inner 2 Layer

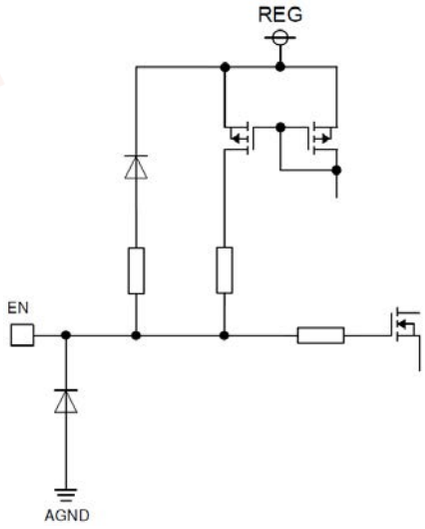
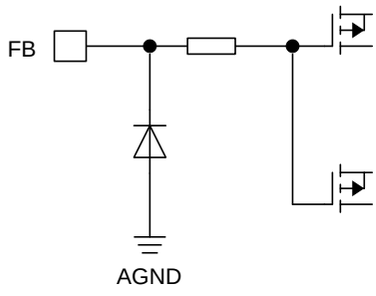
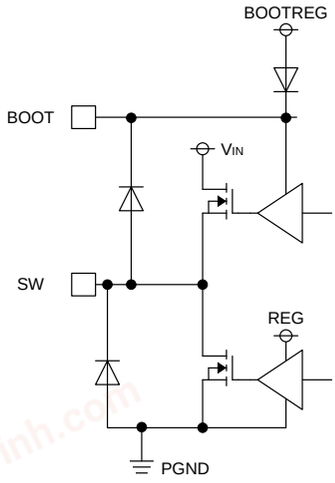
Bottom Layer

Figure 54. Example of PCB Layout

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I/O Equivalence Circuits

5. EN	4. FB
	
2. SW 6. BOOT	
	

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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

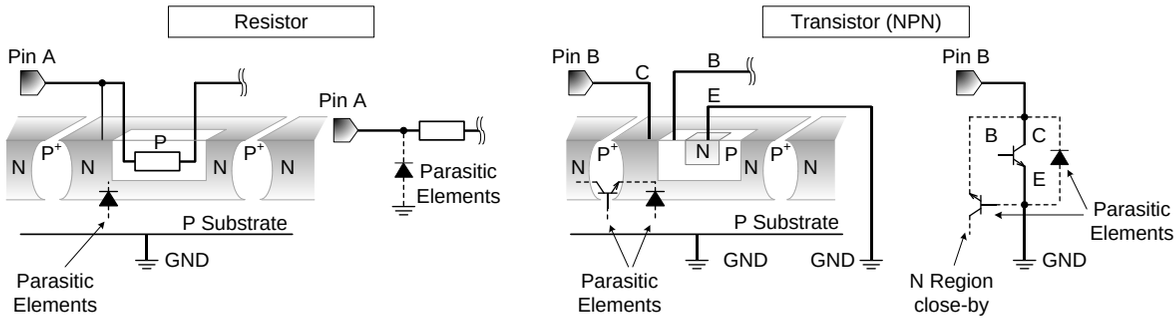


Figure 55. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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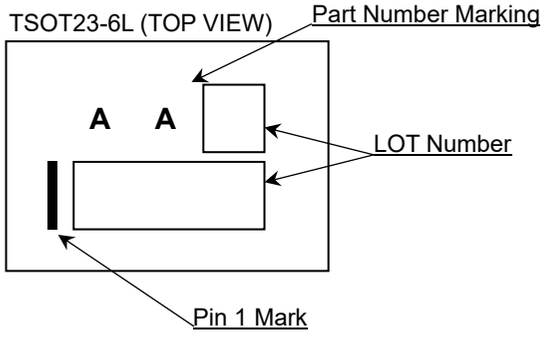
Ordering Information

B	D	9	E	2	0	0	F	P	4	-	Z T L

Package
TSOT23-6L

Packaging and forming specification
TL: Embossed tape and reel

Marking Diagram

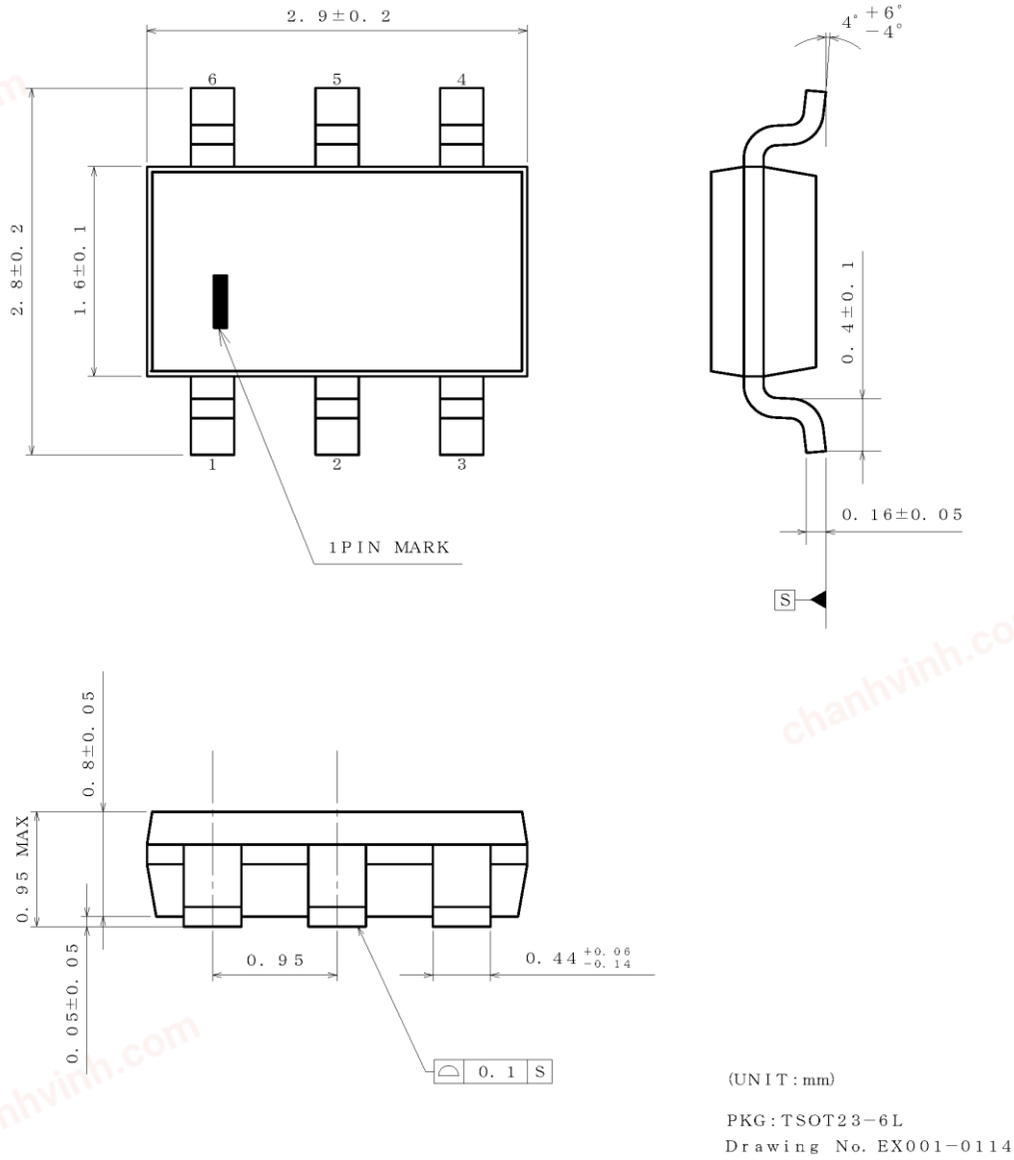


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Physical Dimension and Packing Information

Package Name	TSOT23-6L

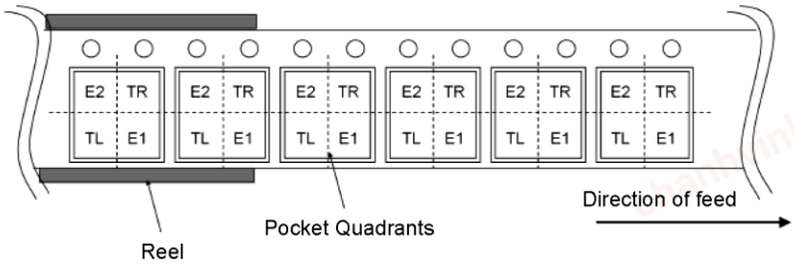


(UNIT : mm)

PKG : TSOT23−6L
Drawing No. EX001−0114

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3500pcs
Direction of feed	TL The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
25.Mar.2022	001	New Release
22.Mar.2023	002	Corrected R_5 calculation formula (Page 17).

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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