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Datasheet

7.0V to 36V Input, 1.0 A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9E101FJ-LB

General Description

This is the product guarantees long time support in Industrial market.

BD9E101FJ-LB is a synchronous buck switching regulator with built-in power MOSFETs. It is capable of an output current of up to 1.0A. It is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

Features

- Long Time Support Product for Industrial Applications.
- Synchronous single DC/DC converter.
- Over-Current Protection.
- Short Circuit Protection.
- Thermal Shutdown Protection.
- Undervoltage Lockout Protection.
- Soft Start.
- SOP-J8 package.

Applications

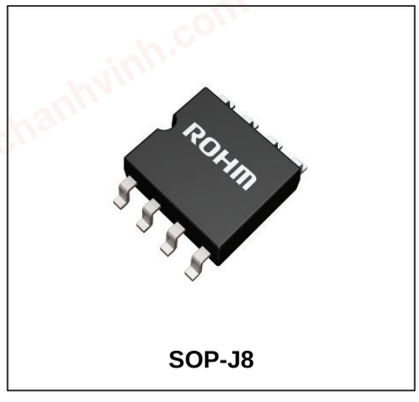
- Industrial Equipment.
- Power supply for FA's industrial device using 24V bass.
- Consumer applications such as home appliance. Distribution type power supply system for 12V, and 24V.

Key Specifications

- Input Voltage Range: 7.0V to 36V
- Output Voltage Range: 1.0V to V_{IN} × 0.7V
- Output Current: 1.0A (Max)
- Switching Frequency: 570kHz (Typ)
- High-Side MOSFET ON-Resistance: 300mΩ (Typ)
- Low-Side MOSFET ON-Resistance: 300mΩ (Typ)
- Standby Current: 0μA (Typ)

Package

	W (Typ) x D (Typ) x H (Max)
SOP-J8	4.90mm x 6.00mm x 1.65mm



SOP-J8

Typical Application Circuit

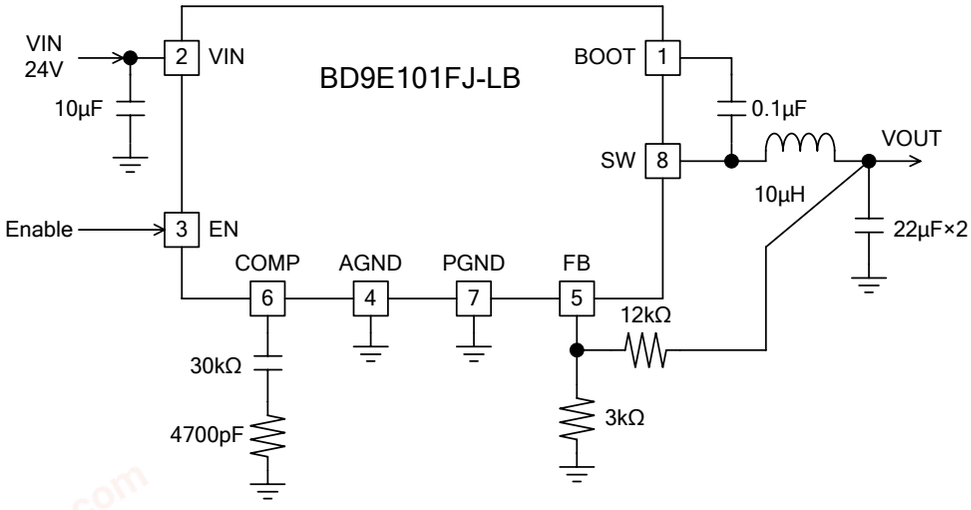


Figure 1. Application circuit

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Pin Configuration

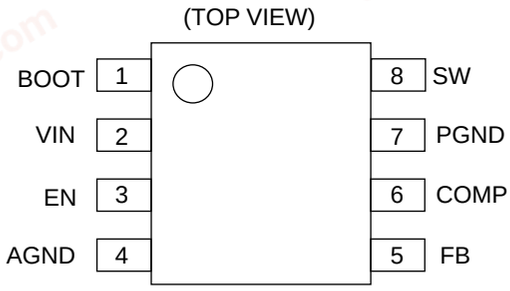


Figure 2. Pin assignment

Pin Description(s)

Pin No	Pin Name	Description
1	BOOT	Connect a bootstrap capacitor of 0.1µF between this terminal and SW terminal. The voltage of this capacitor is the gate drive voltage of the high-side MOSFET.
2	VIN	Power supply terminal for the switching regulator and control circuit. Connecting a 10µF ceramic capacitor is recommended.
3	EN	Turning this terminal signal low-level (0.8V or lower) forces the device to enter the shut down mode. Turning this terminal signal high-level (2.5V or higher) enables the device. This terminal must be terminated.
4	AGND	Ground terminal for the control circuit.
5	FB	Inverting input node for the gm error amplifier. See page 22 on how to calculate the resistance of the output voltage setting.
6	COMP	Input terminal for the gm error amplifier output and the output switch current comparator. Connect a frequency phase compensation component to this terminal. See page 23 on how to calculate the resistance and capacitance for phase compensation.
7	PGND	Ground terminal for the output stage of the switching regulator.
8	SW	Switch node. This terminal is connected to the source of the high-side MOSFET and drain of the low-side MOSFET. Connect a bootstrap capacitor of 0.1µF between this terminal and BOOT terminal. In addition, connect an inductor considering the direct current superimposition characteristic.

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Block Diagram

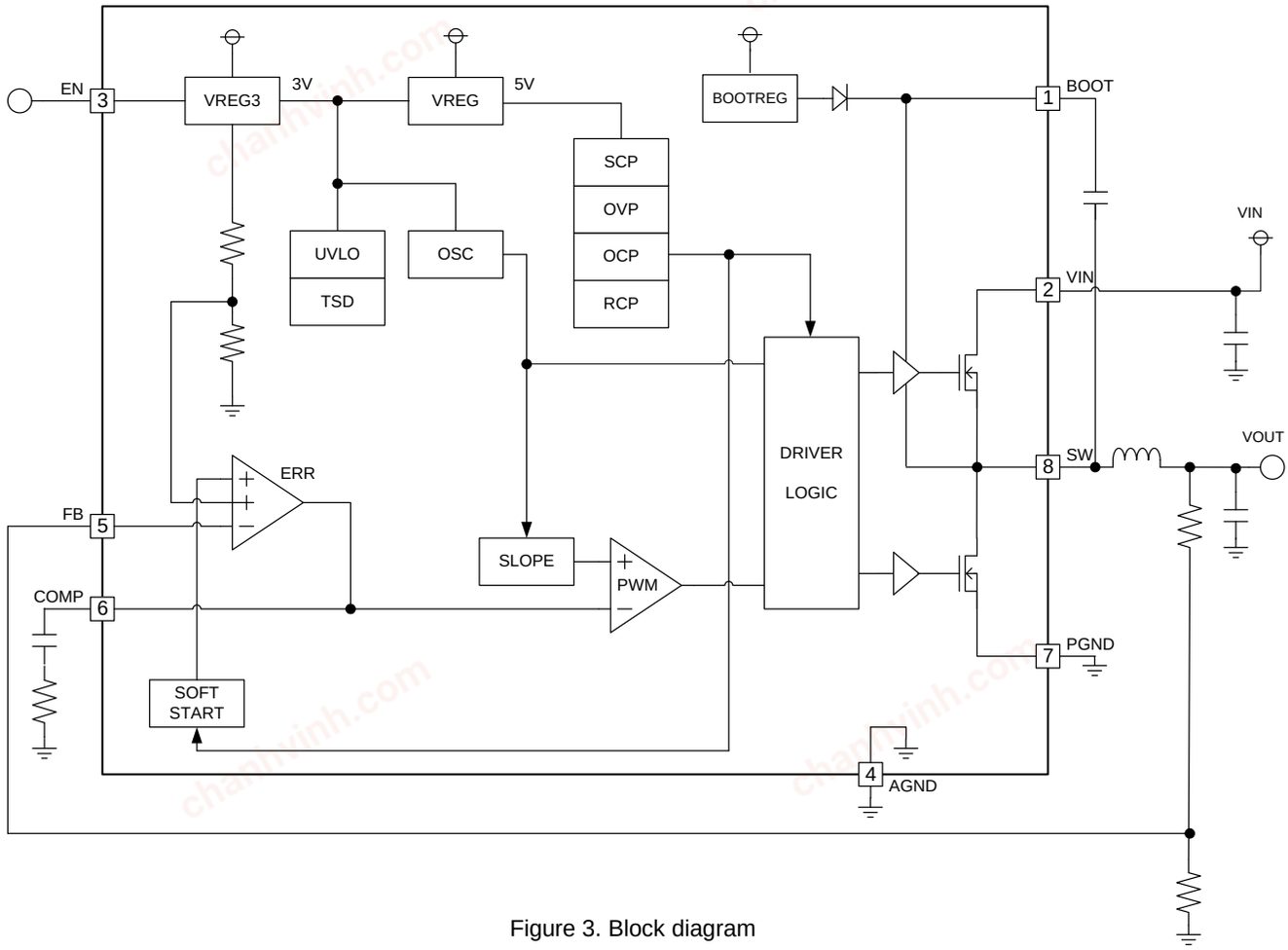


Figure 3. Block diagram

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Description of Block

- VREG3
  Block creating internal reference voltage 3V (Typ).

- VREG
  Block creating internal reference voltage 5V (Typ).

- BOOTREG
  Block creating gate drive voltage.

- TSD
  This is the thermal shutdown block. Thermal shutdown circuit shuts down the whole system if temperature exceeds 175°C (Typ). When the temperature decreases, it returns to normal operation with hysteresis of 25°C (Typ).

- UVLO
  This is the under voltage lock-out block. IC shuts down when VIN is under 6.4V (Typ). The threshold voltage has a hysteresis of 200mV (Typ).

- ERR
  This circuit compares the feedback voltage at the output to the reference voltage. The output of this circuit is the COMP terminal voltage and this determines the switching duty. Also, because of soft start during start-up, COMP terminal voltage is controlled by internal slope voltage.

- OSC
  Block generating oscillation frequency.

- SLOPE
  This circuit creates a triangular wave from generated clock in OSC. The voltage converted from current sense signal of high side MOSFET and the triangular wave is sent to PWM comparator.

- PWM
  This block determines the switching duty by comparing the output COMP terminal voltage of error amplifier and output of SLOPE block.

- DRIVER LOGIC
  This is the DC/DC driver block. Input to this block is signal from PWM and output drives the MOSFETs.

- SOFT START
  This circuit prevents the overshoot of output voltage and In-rush current by forcing the output voltage to rise slowly, thus, avoiding surges in current during start-up.

- OCP
  This block limits the current flowing in high side MOSFET for each cycle of switching frequency during over-current.

- RCP
  This block limits the current flowing in low side MOSFET for each cycle of switching frequency during over-current.

- SCP
  The short circuit protection block compares the FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage has fallen below 0.85V (Typ) and remained in that state for 1.0msec (Typ), SCP activates and stops the operation for 16msec (Typ) and subsequently initiates a restart.

- OVP
  Over voltage protection function (OVP) compares FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage exceeds 1.30V (Typ), it turns output MOSFETs off. When output voltage drops until it reaches the hysteresis, it will return to normal operation.

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	VIN	-0.3 to +40	V
EN Input Voltage	VEN	-0.3 to +40	V
Voltage from GND to BOOT	VBOOT	-0.3 to +45	V
Voltage from SW to BOOT	⊿VBOOT	-0.3 to +7	V
FB Input Voltage	VFB	-0.3 to +7	V
COMP Input Voltage	VCOMP	-0.3 to +7	V
SW Input Voltage	VSW	-0.5 to VIN + 0.3	V
Allowable Power Dissipation	Pd	0.67 (Note 1)	W
Operating Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) Derating in done 5.36 mW/°C for operating above Ta≧25°C (Mount on 1-layer 70.0mm x 70.0mm x 1.6mm board)

Caution1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution2: Reliability is decreased at junction temperature greater than 125°C.

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	VIN	7.0	-	36	V
Output Current	IOUT	0	-	1.0	A
Output Voltage Range	VRANGE	1.0(Note 2)	-	VIN × 0.7	V

(Note 2) Please use it in I/O voltage setting of which output pulse width does not become 150nsec (Typ) or less. See the page 22 for how to calculate the resistance of the output voltage setting.

Electrical Characteristics (Unless otherwise specified V_{IN}=24V V_{EN}=3V Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Current in Operating	IOPR	-	1.5	2.5	mA	VFB = 1.1V No switching
Supply Current in Standby	ISTBY	-	0	10	μA	VEN = 0V
Reference Voltage	VFB	0.98	1.00	1.02	V	
FB Input Current	IFB	-1	0	1	μA	VFB = 0V
Switching frequency	FOSC	484	570	656	KHz	
Maximum Duty ratio	Maxduty	85	90	95	%	
High-side FET on-resistance	RONH	-	300	-	mΩ	ISW = 100mA
Low-side FET on-resistance	RONL	-	300	-	mΩ	ISW = 100mA
Over Current limit	ILIMIT	-	3.0	-	A	
UVLO detection voltage	VUVLO	6.1	6.4	6.7	V	VIN falling
UVLO hysteresis voltage	VUVLOHYS	100	200	300	mV	
EN high-level input voltage	VENH	2.5	-	VIN	V	
EN low-level input voltage	VENL	-	-	0.8	V	
EN Input current	IEN	2.1	4.2	8.4	μA	VEN = 3V
Soft Start time	TSS	1.5	3.0	6.0	msec	EN rising to FB=0.85V

- VFB : FB Input Voltage. VEN : EN Input Voltage.
- Pd should not be exceeded.

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Typical Performance Curves

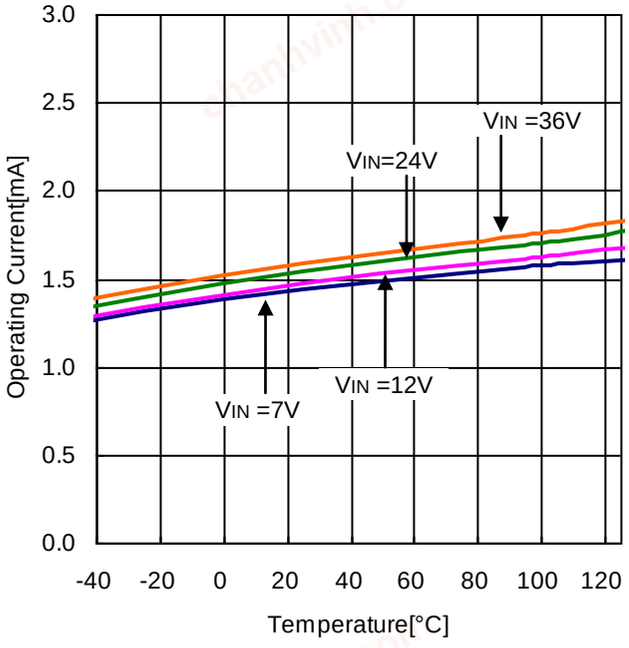


Figure 4. Operating Current vs Junction Temperature

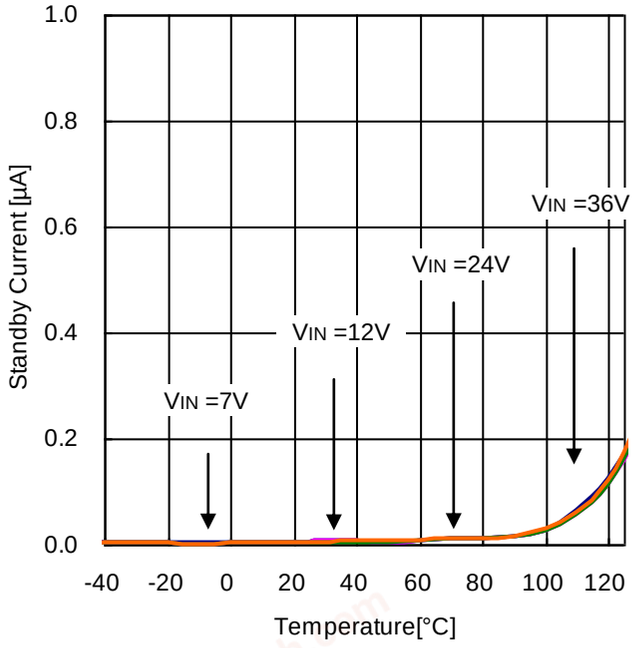


Figure 5. Stand-by Current vs Junction Temperature

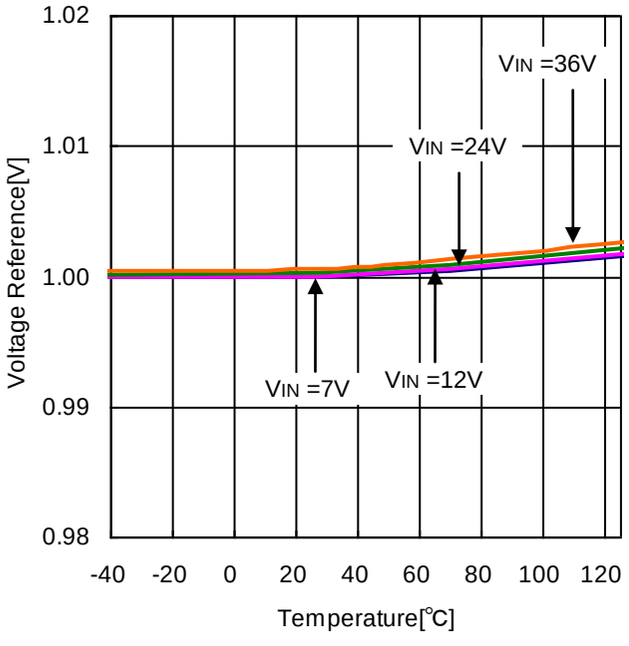


Figure 6. FB Voltage Reference vs Junction Temperature

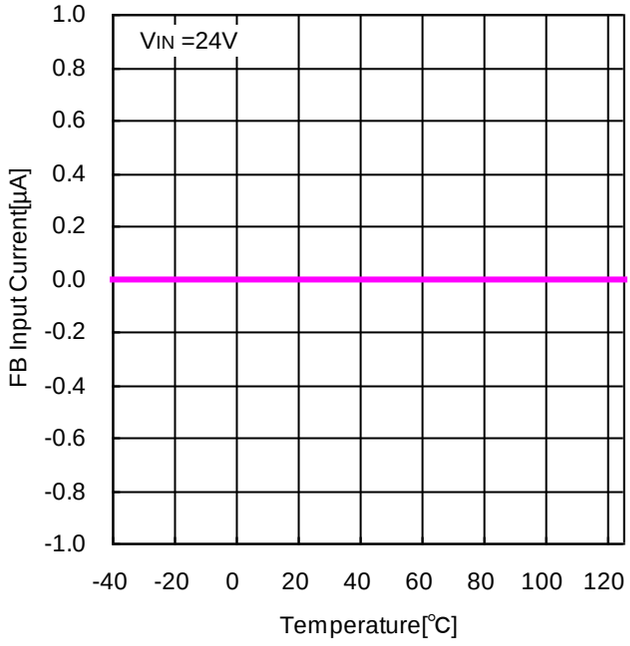


Figure 7. FB Input Current vs Junction Temperature

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Typical Performance Curves - continued

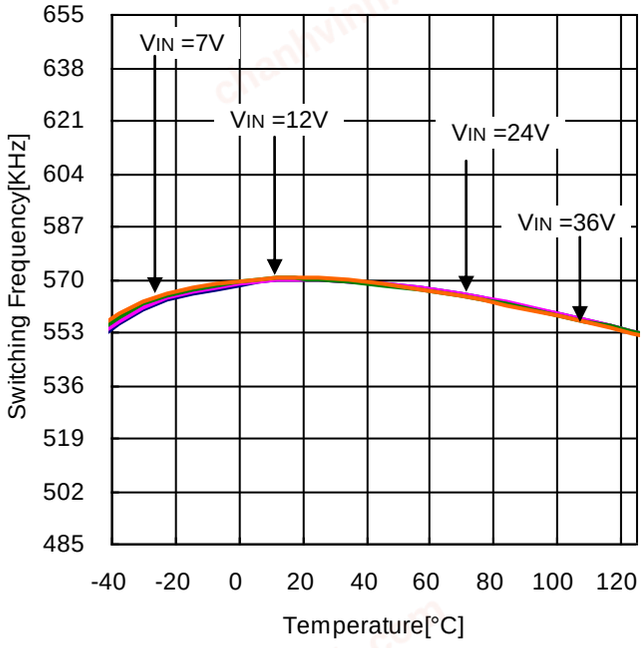


Figure 8. Switching Frequency vs Junction Temperature

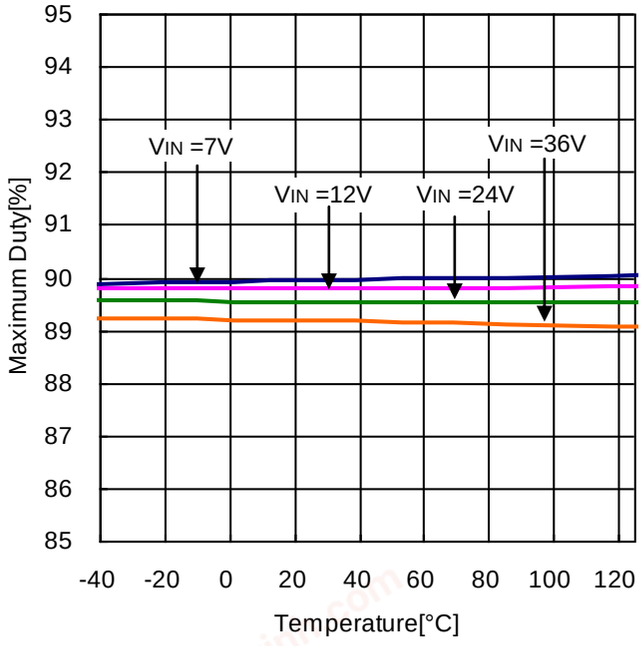


Figure 9. Maximum Duty vs Junction Temperature

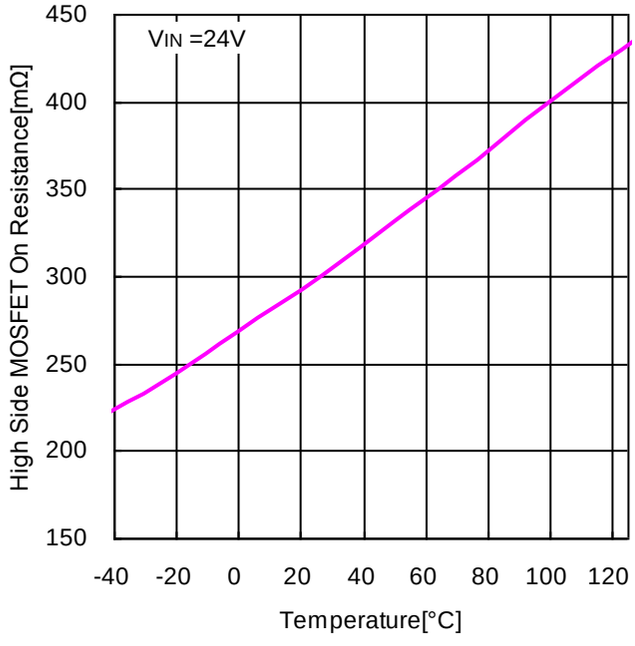


Figure 10. High Side MOSFET ON - Resistance vs Junction Temperature

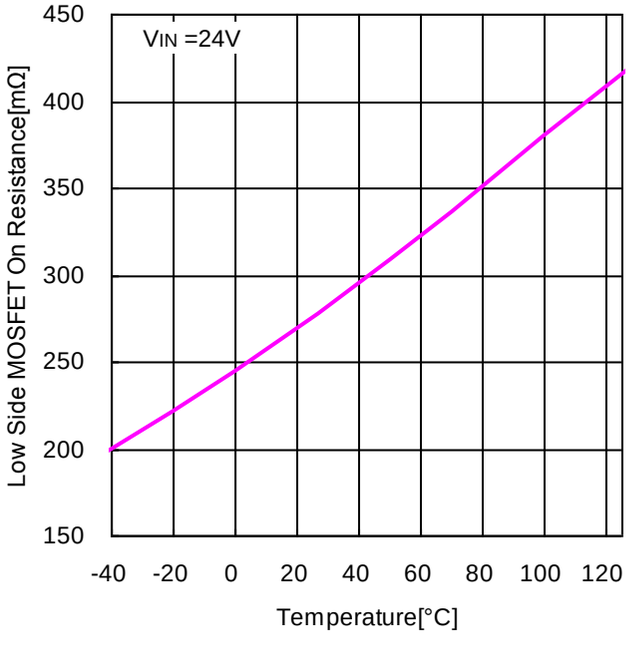


Figure 11. Low Side MOSFET ON -Resistance vs Junction Temperature

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Typical Performance Curves - continued

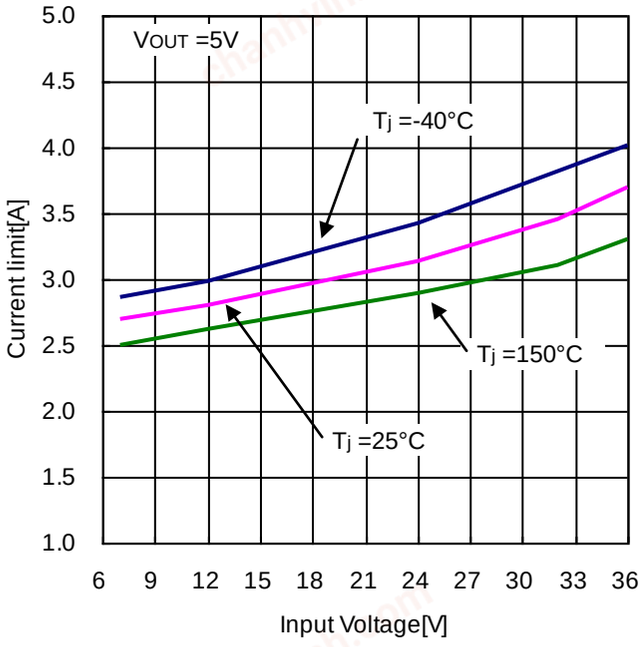


Figure 12. Current Limit vs Input Voltage

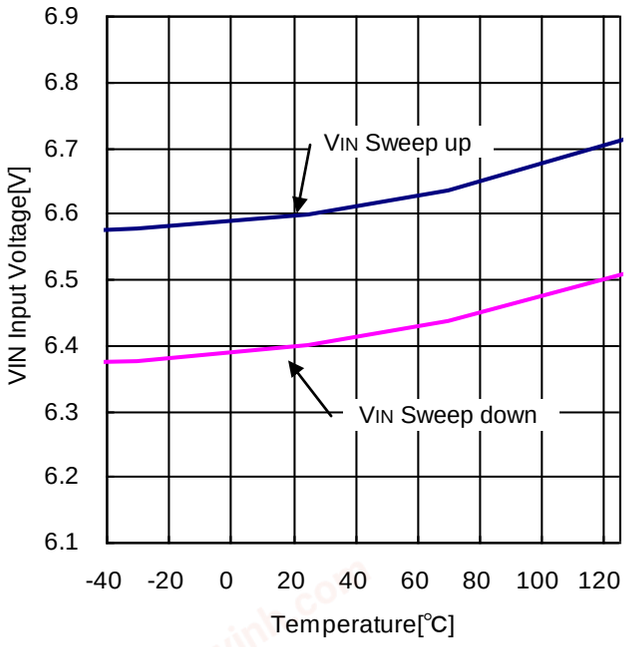


Figure 13. UVLO Threshold vs Junction Temperature

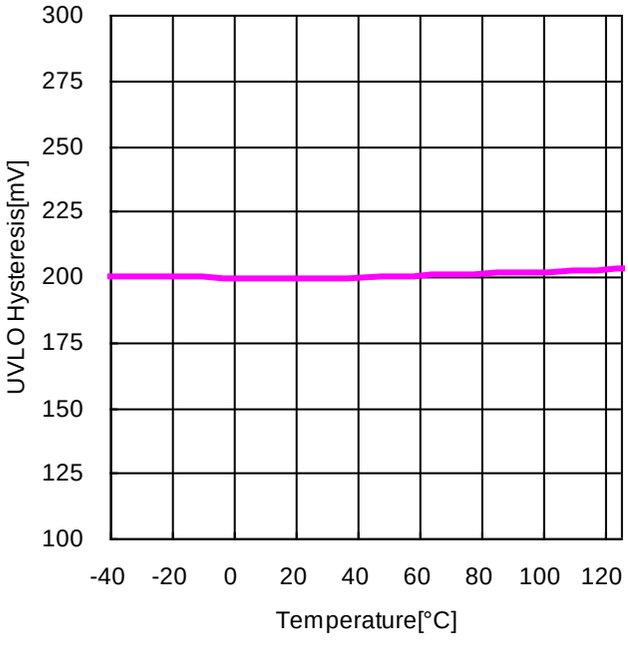


Figure 14. UVLO Hysteresis vs Junction Temperature

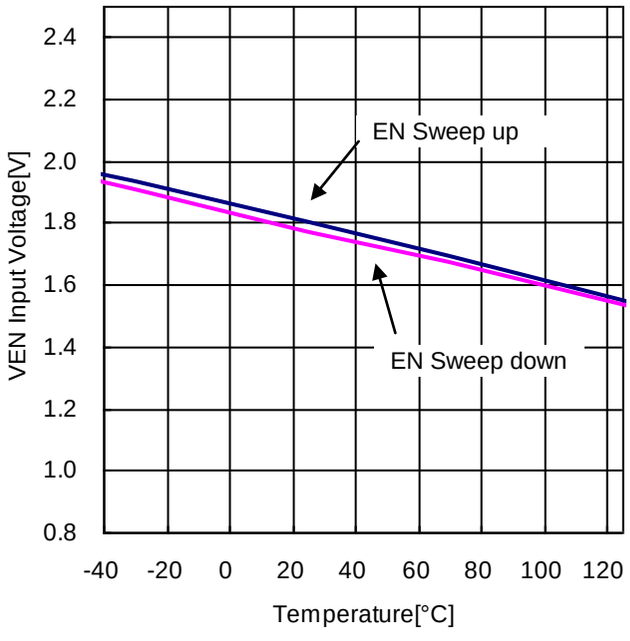


Figure 15. EN Threshold vs Junction Temperature

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Typical Performance Curves - continued

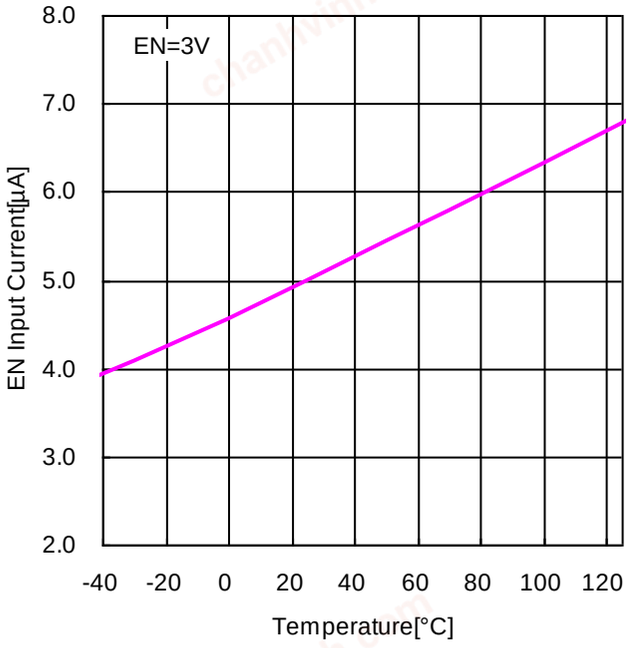


Figure 16. EN Input Current vs Junction Temperature

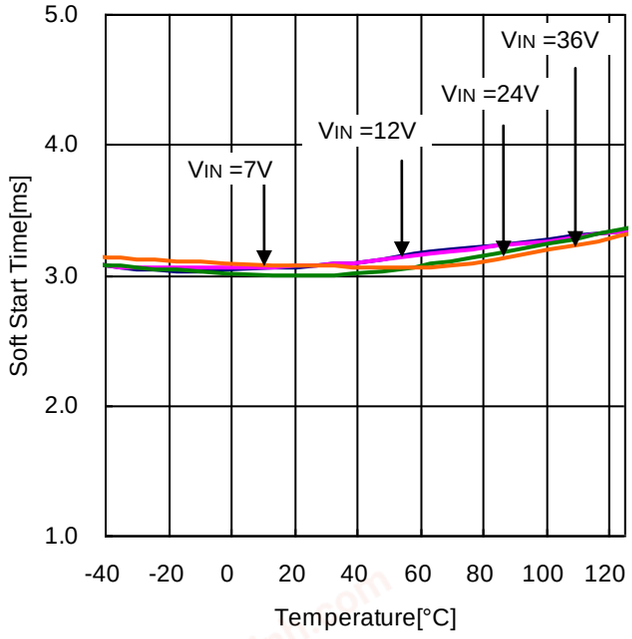


Figure 17. Soft Start Time vs Junction Temperature

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Typical Performance Curves - continued

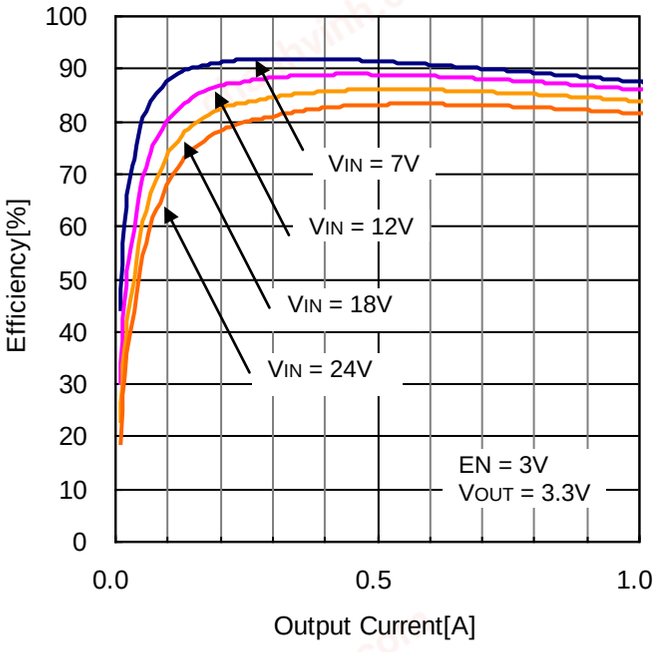


Figure 18. Efficiency vs Output Current
(VOUT = 3.3V, L=10μH)

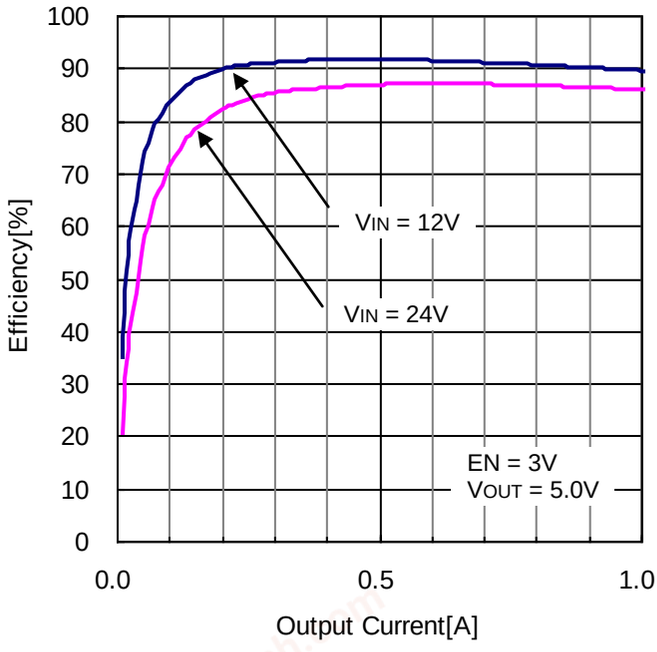


Figure 19. Efficiency vs Output Current
(VOUT = 3.3V, L=10μH)

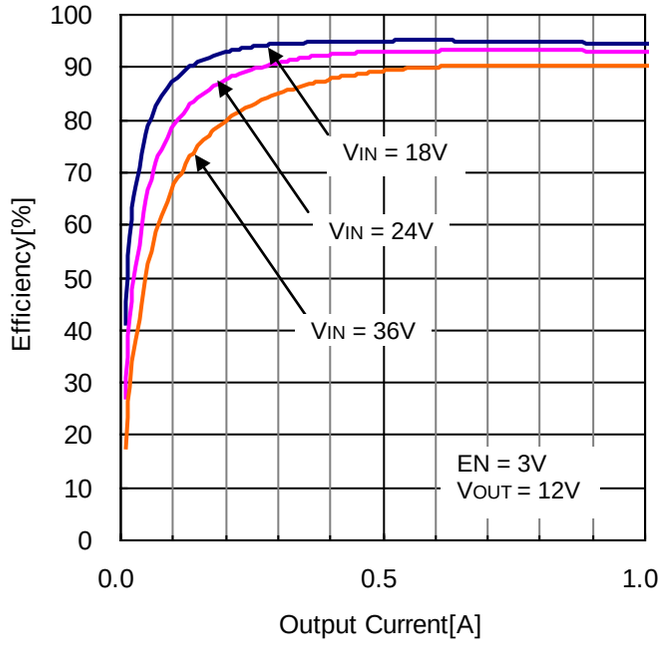


Figure 20. Efficiency vs Output Current
(VOUT = 12V, L=10μH)

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Typical Performance Curves - continued

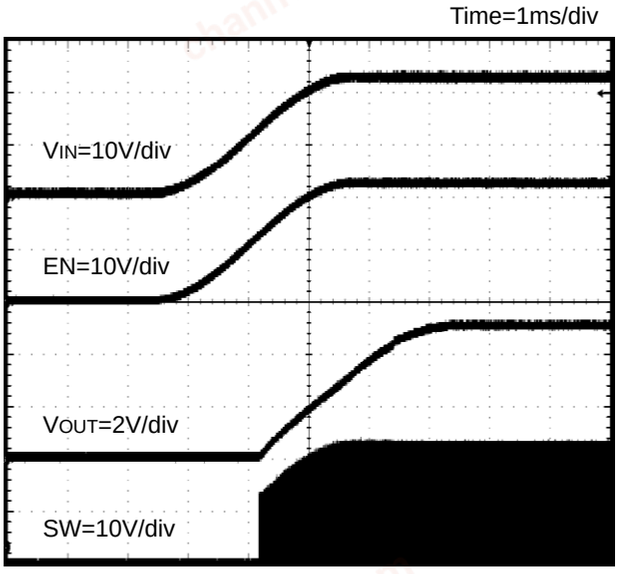


Figure 21. Power Up (VIN = EN)
(VOUT = 5.0V)

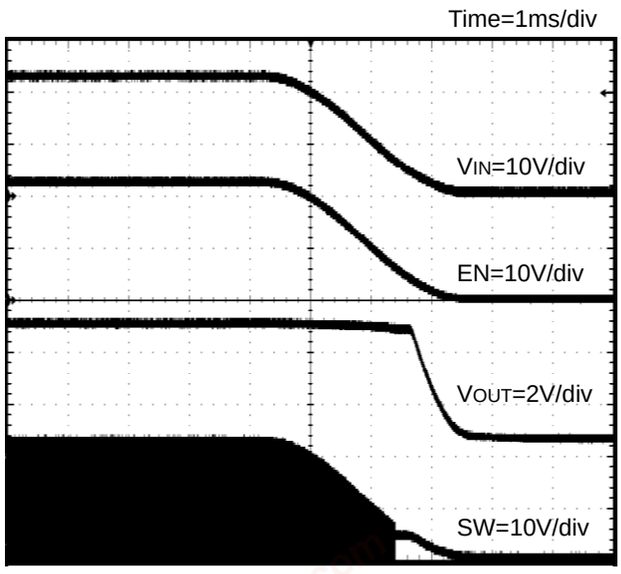


Figure 22. Power Down (VIN = EN)
(VOUT = 5.0V)

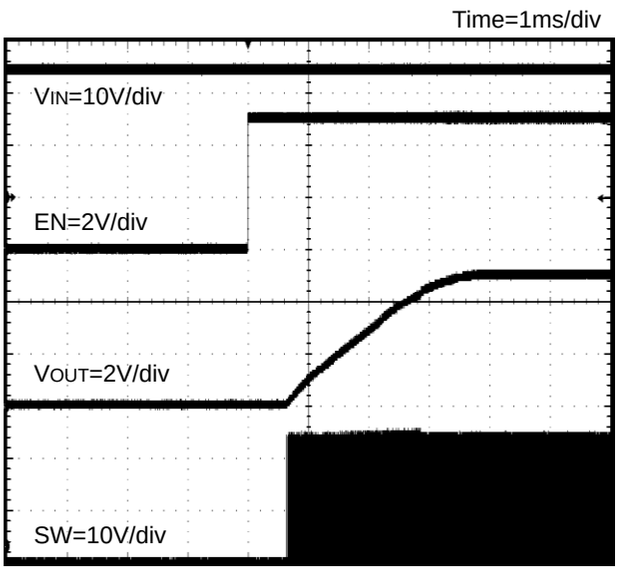


Figure 23. Power Up (EN = 0V→5V)
(VOUT = 5.0V)

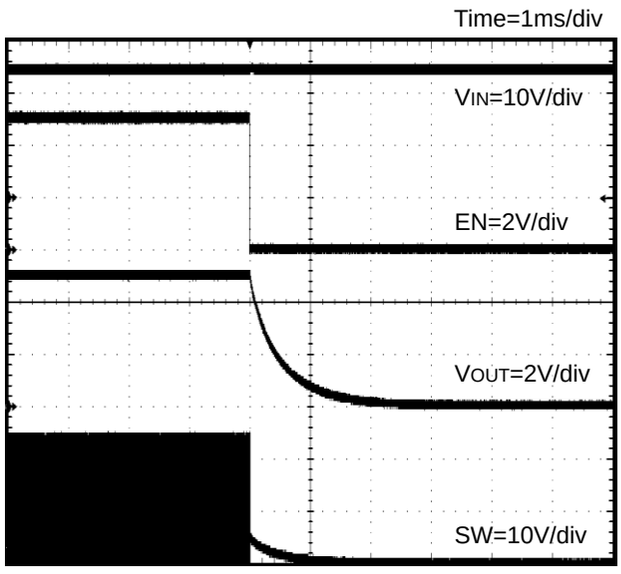


Figure 24. Power Down (EN = 5V→0V)
(VOUT = 5.0V)

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Typical Performance Curves - continued

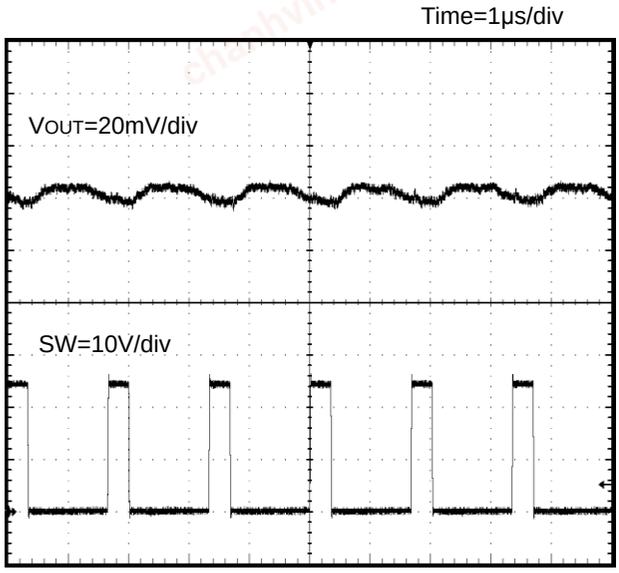


Figure 25. VOUT Ripple
(VIN = 24V, VOUT = 5V, IOUT = 0A)

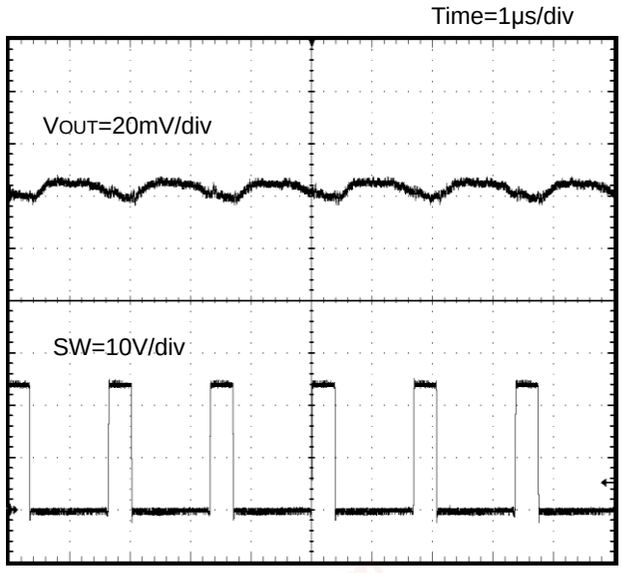


Figure 26. VOUT Ripple
(VIN = 24V, VOUT = 5V, IOUT = 1.0A)

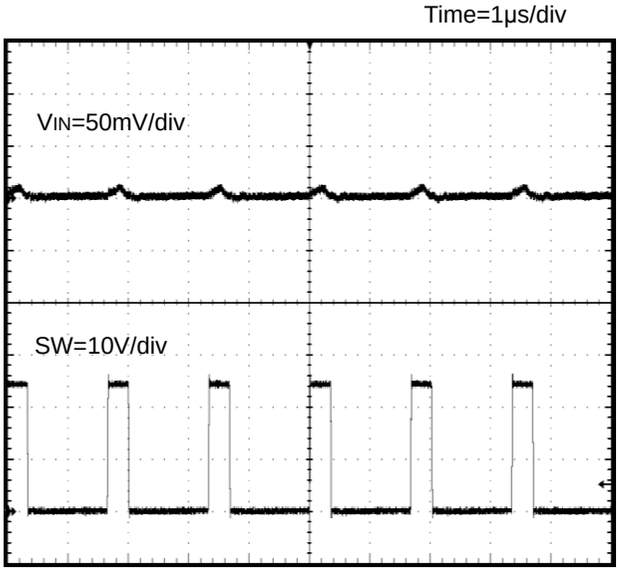


Figure 27. VIN Ripple
(VIN = 24V, VOUT = 5V, IOUT = 0A)

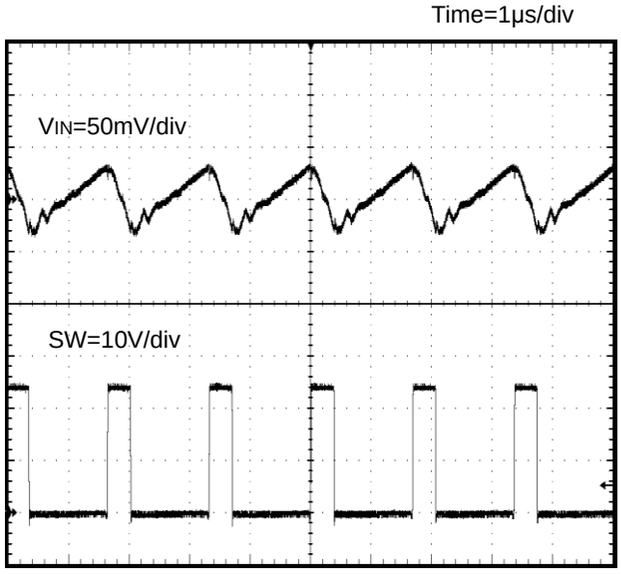


Figure 28. VIN Ripple
(VIN = 24V, VOUT = 5V, IOUT = 1.0A)

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Typical Performance Curves - continued

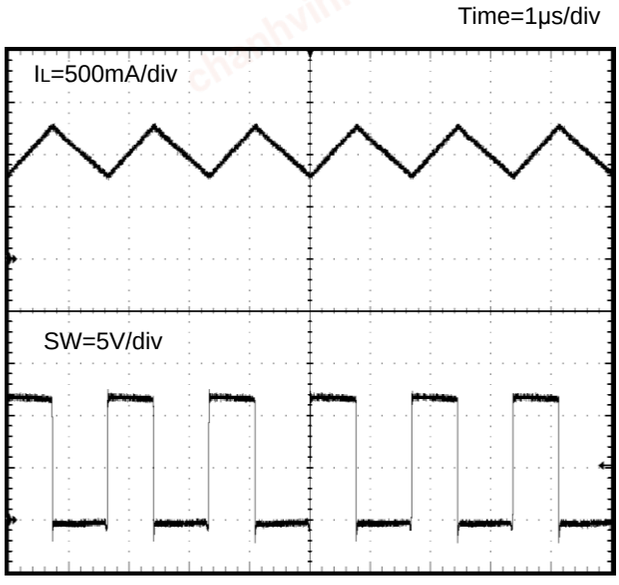


Figure 29. Switching Waveform
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.0A)

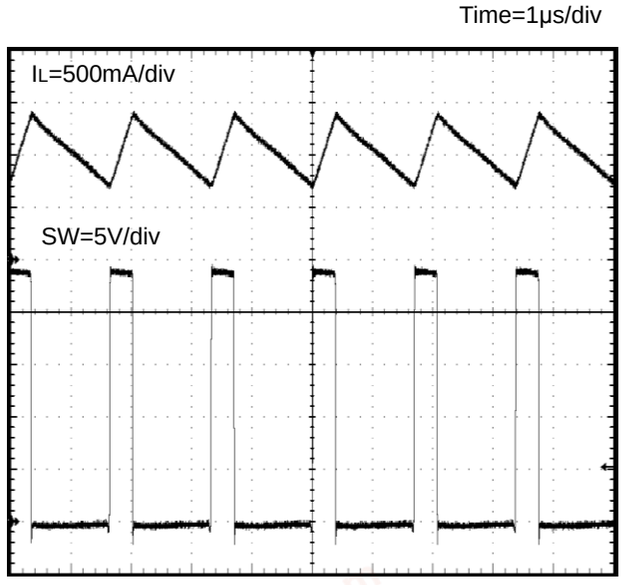


Figure 30. Switching Waveform
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1.0A)

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Typical Performance Curves - continued

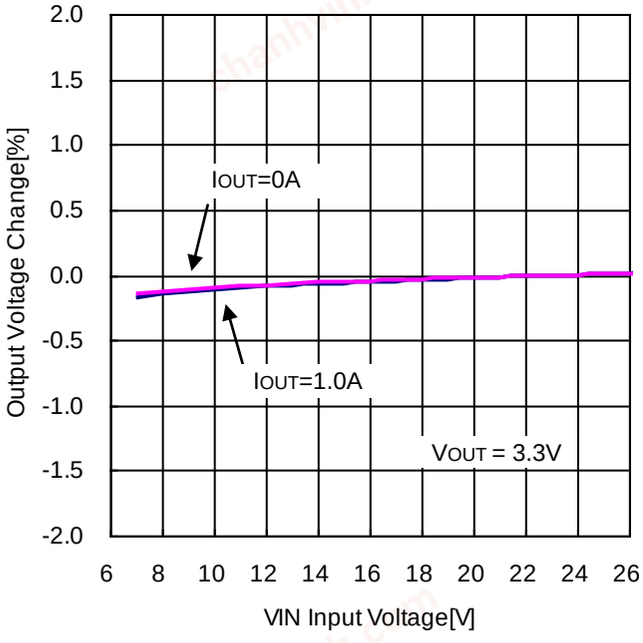


Figure 31. VOUT Line Regulation

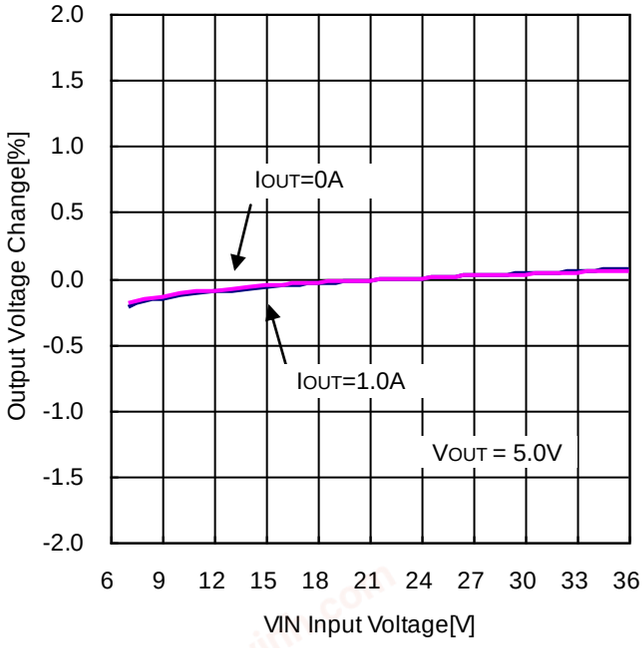


Figure 32. VOUT Line Regulation

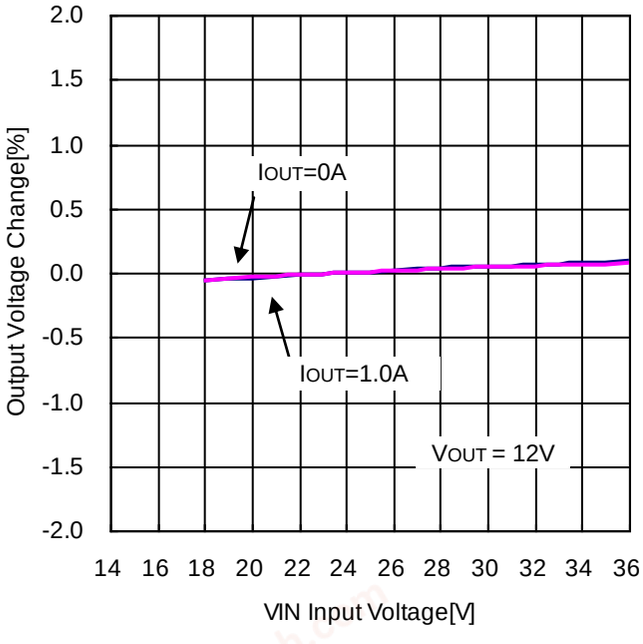


Figure 33. VOUT Line Regulation

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Typical Performance Curves - continued

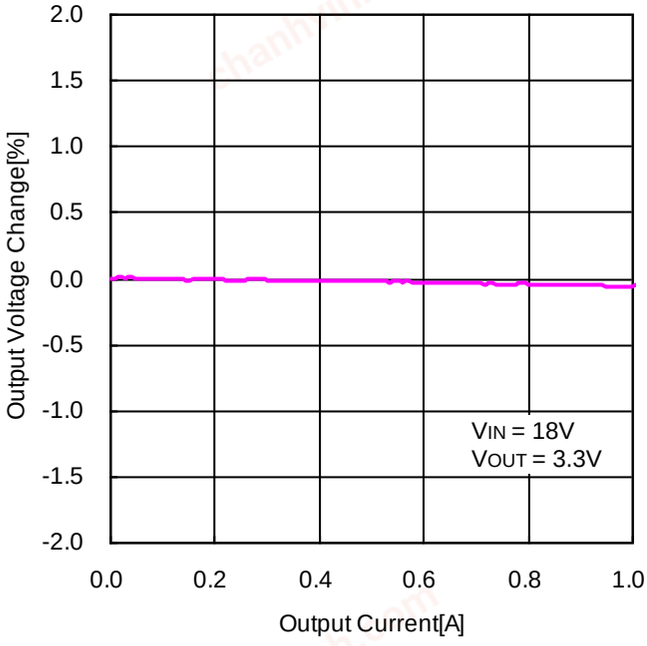


Figure 34. VOUT Load Regulation

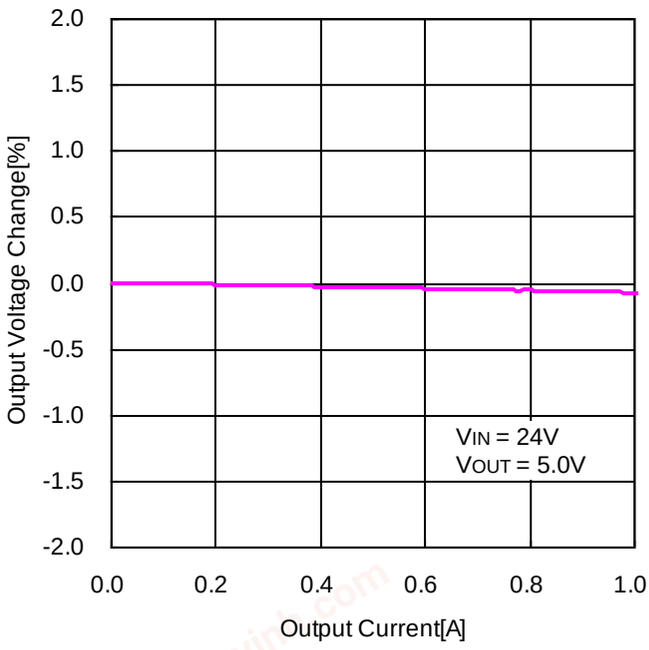


Figure 35. VOUT Load Regulation

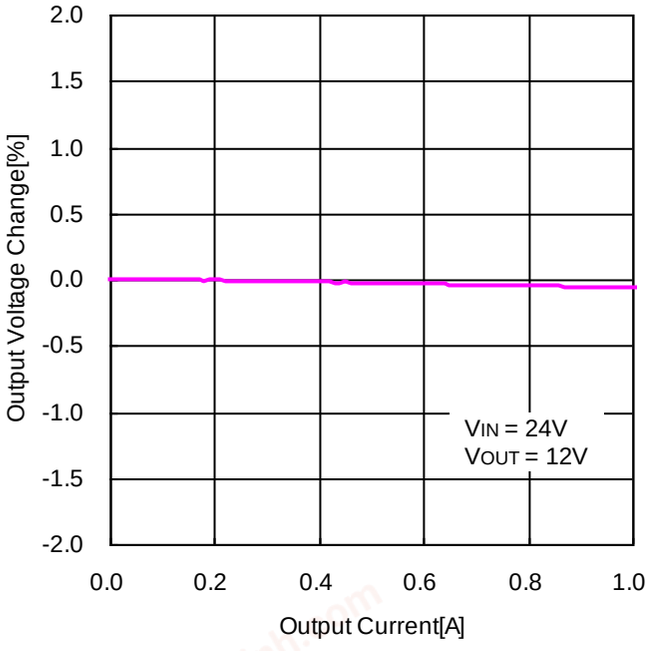


Figure 36. VOUT Load Regulation

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Typical Performance Curves – continued

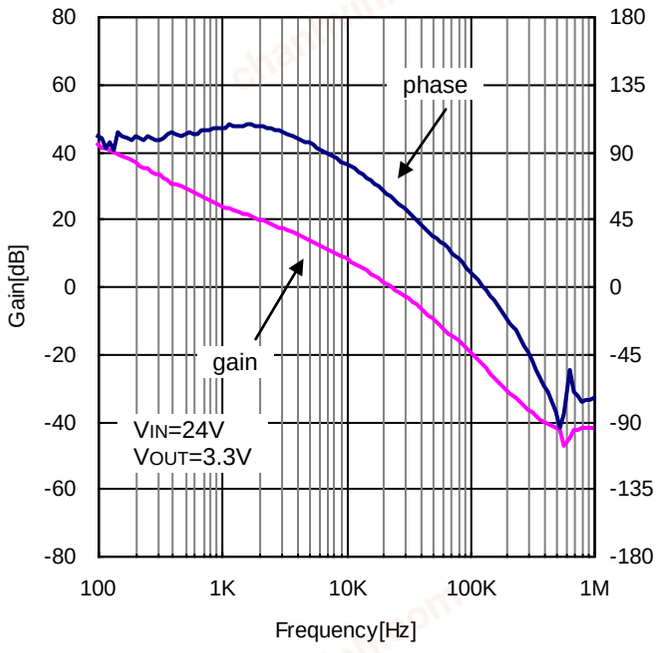


Figure 37. Loop Response
(VIN=12V, VOUT=3.3V, IOUT=1.0A, COUT=Ceramic22μF × 2)

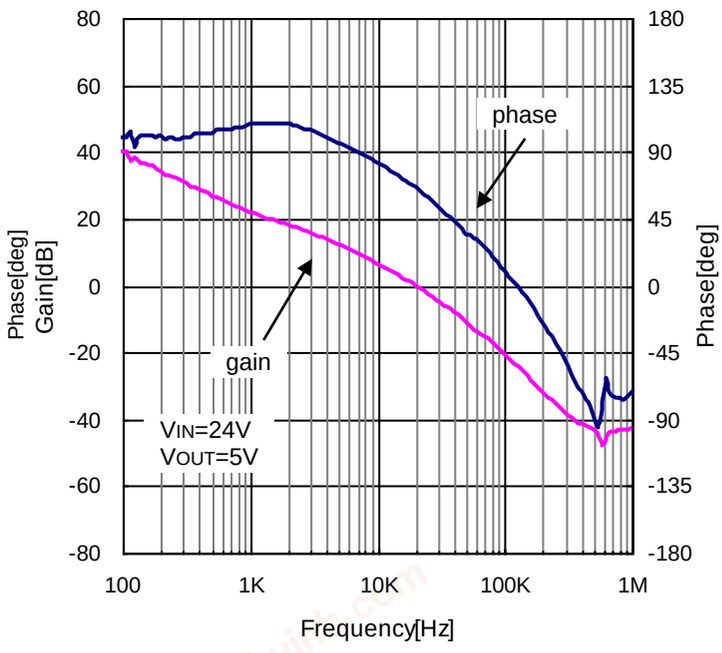


Figure 38. Loop Response
(VIN=24V, VOUT=5V, IOUT=1.0A, COUT=Ceramic22μF × 2)

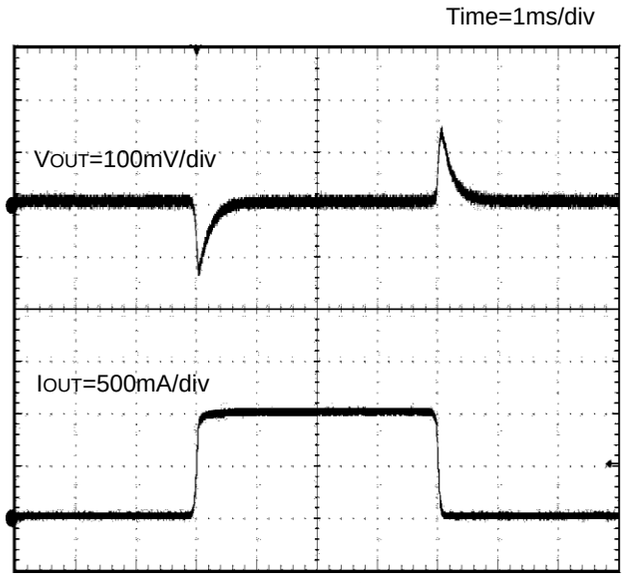


Figure 39. Load Transient Response IOUT=0A – 1.0A
(VIN=12V, VOUT=3.3V, COUT=Ceramic22μF × 2)

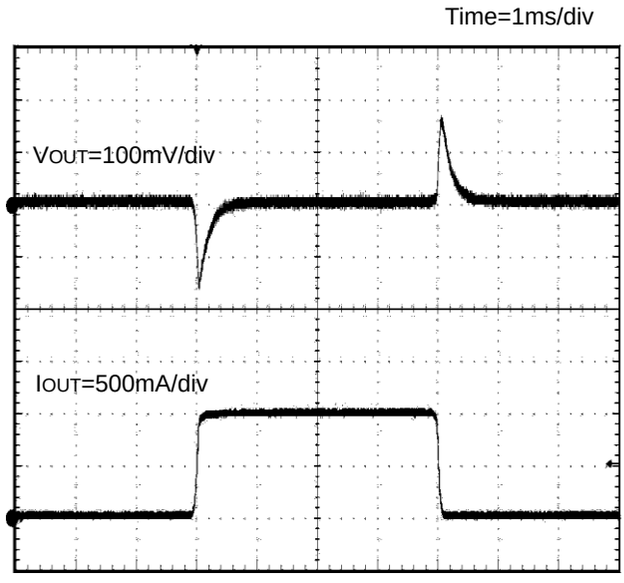


Figure 40. Load Transient Response IOUT=0A – 1.0A
(VIN=24V, VOUT=5.0V, COUT=Ceramic22μF × 2)

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Function Description

1. Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When EN voltage reaches 2.5V (Typ), the internal circuit is activated and the IC starts up. Setting the shutdown interval (Low Level interval) of EN to 100µs or longer will enable the shutdown control with the EN terminal.

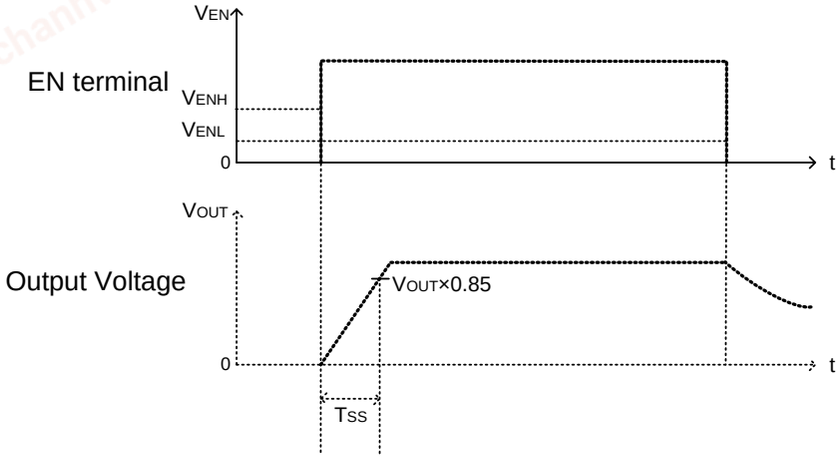


Figure 41. Timing Chart with Enable Control

2. Protective Functions

The protective circuits are intended for the prevention of damages caused by unexpected accidents. Do not use them for continuous protective operation.

(1) Short Circuit Protection (SCP)

The short circuit protection block compares the FB terminal voltage with the internal reference voltage VREF. When the FB terminal voltage has fallen below 0.85V (Typ) and remained in that state for 1.0msec (Typ), SCP activates and stops the operation for 16msec (Typ) and subsequently initiates a restart.

Table 1. Short Circuit Protection Function

EN pin	FB pin	Short circuit protection	Switching Frequency
2.5V or higher	0.30V (Typ)≦FB	Enabled	142.5kHz (Typ)
	0.30V (Typ)＞B≦0.85V (Typ)		285kHz (Typ)
	FB＞0.85V (Typ)		570kHz (Typ)
0.8V or lower	-	Disabled	OFF

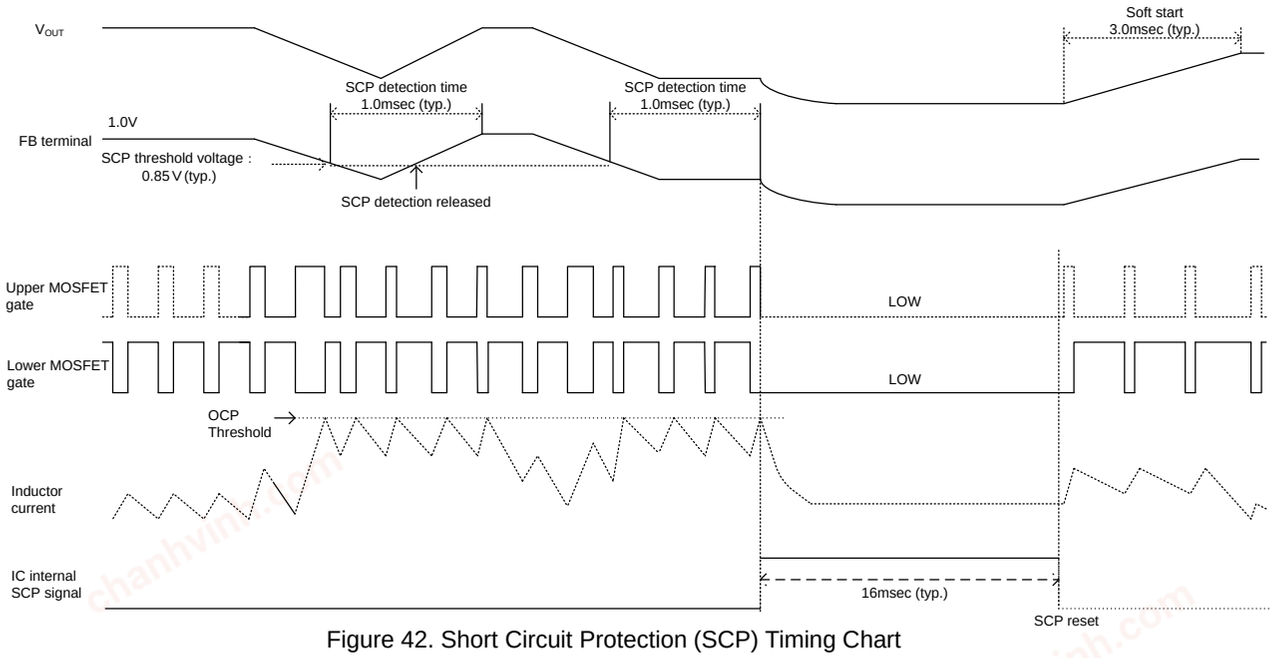


Figure 42. Short Circuit Protection (SCP) Timing Chart

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(2) Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection circuit monitors the VIN terminal voltage.
The operation enters standby when the VIN terminal voltage is 6.4V (Typ) or lower.
The operation starts when the VIN terminal voltage is 6.6V (Typ) or higher.

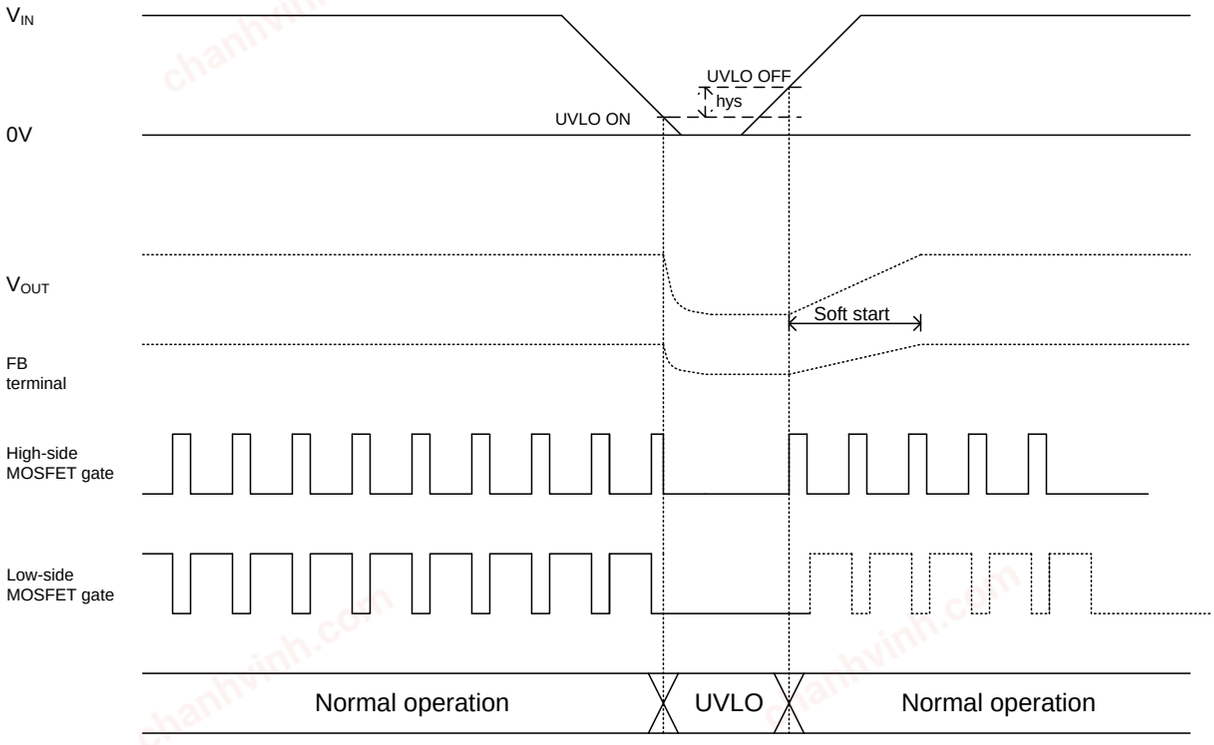


Figure 43. UVLO Timing Chart

(3) Thermal Shutdown (TSD)

When the chip temperature exceeds Tj = 175°C, the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax = 150°C. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

(4) Over Current Protection (OCP)

The over-current protection function is realized by using the current mode control to limit the current that flows through the high-side MOSFET at each cycle of the switching frequency.

(5) Reverse Current Protection (RCP)

The reverse current protection function is realized by using the current mode control to limit the current that flows through the low-side MOSFET at each cycle of the switching frequency.

(6) Over Voltage Protection (OVP)

Over voltage protection function (OVP) compares FB terminal voltage with internal standard voltage VREF. When the FB terminal voltage exceeds 1.30V (Typ), it turns output MOSFETs off. When output voltage drops until it reaches the hysteresis, it will return to normal operation.

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Application Example

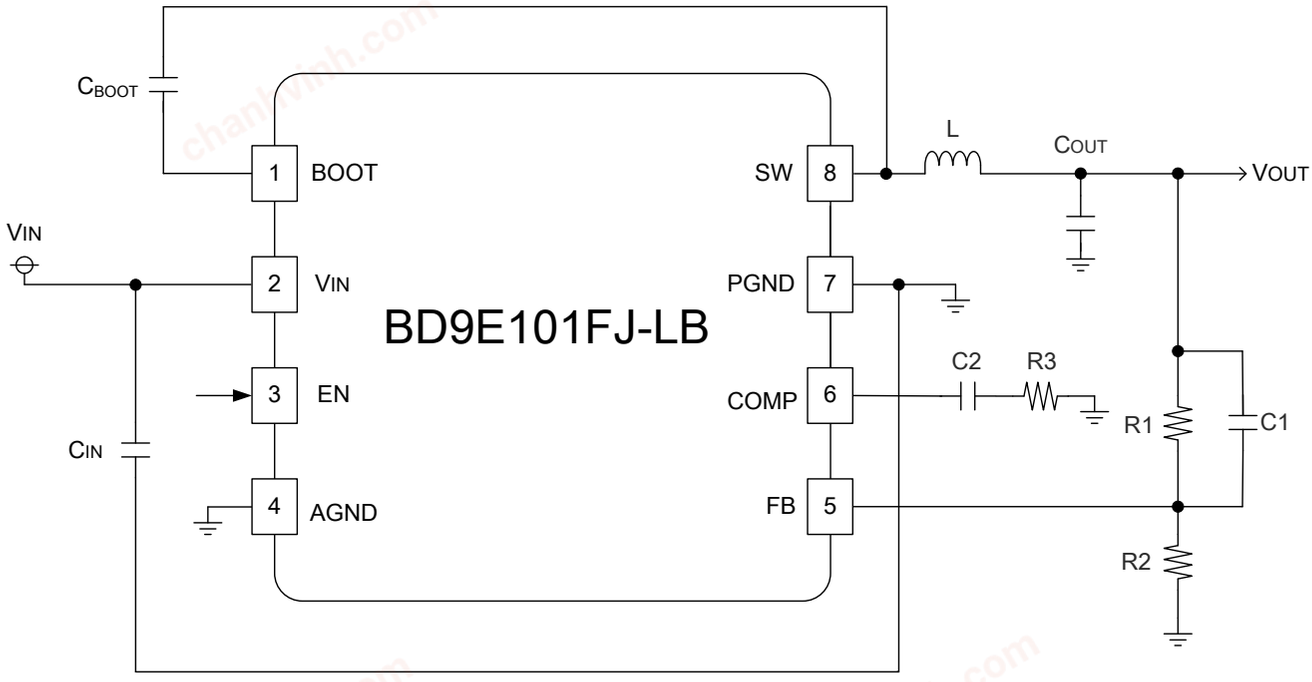


Figure 44. Application Circuit

Table 2. Recommendation Component Valves

VIN	12V			24V		
VOUT	3.3V			5V		
CIN	10µF	10µF	10µF	10µF	10µF	10µF
CBOOT	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF	0.1µF
L	6.8µH	6.8µH	6.8µH	10µH	10µH	10µH
R1	6.8kΩ	6.8kΩ	6.8kΩ	12kΩ	12kΩ	12kΩ
R2	3.0kΩ	3.0kΩ	3.0kΩ	3.0kΩ	3.0kΩ	3.0kΩ
R3	24kΩ	24kΩ	24kΩ	30kΩ	30kΩ	30kΩ
C1	-	-	-	-	-	-
C2	6800pF	6800pF	6800pF	4700pF	4700pF	4700pF
COUT	Ceramic 22µF×2	Ceramic 10µF×3	Ceramic 10µF and Aluminum 100µF	Ceramic 22µF×2	Ceramic 10µF×3	Ceramic 10µF and Aluminum 100µF

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Selection of Components Externally Connected

1. Output LC Filter

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. Selecting an inductor with a large inductance causes the ripple current ΔIL that flows into the inductor to be small, decreasing the ripple voltage generated in the output voltage, but it is not advantageous in terms of the load transient response characteristic. Selecting an inductor with a small inductance improves the transient response characteristic but causes the inductor ripple current to be large, which increases the ripple voltage in the output voltage, showing a trade-off relationship. Here, select an inductance so that the size of the ripple current component of the inductor will be 20% to 50% of the average output current (average inductor current).

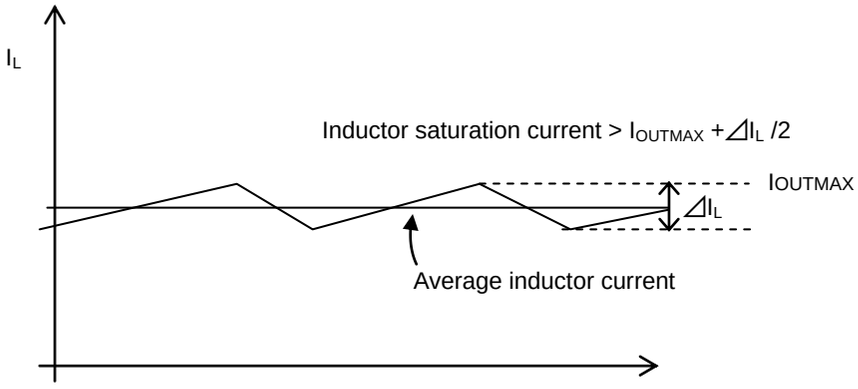


Figure 45. Waveform of current through inductor

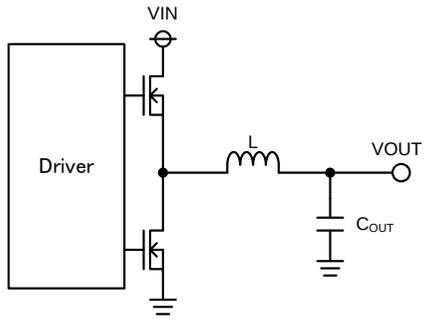


Figure 46. Output LC filter circuit

Computation with VIN = 24V, VOUT = 5V, L = 10μH, switching frequency FOSC = 570kHz, the method is as below.

Inductor ripple current

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times L} = 694 \text{ [mA]}$$

where :

ΔI_L is the inductor ripple current

F_{OSC} is the swithing frequency

L is the inductor

V_{IN} is the input voltage

V_{OUT} is the output voltage

Also for saturation current of inductor, select the one with larger current than maximum output current added by 1/2 of inductor ripple current ΔIL.

Output capacitor COUT affects output ripple voltage characteristics. Select output capacitor COUT so that necessary ripple voltage characteristics are satisfied.

Output ripple voltage can be expressed in the following method.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}}) \text{ [V]}$$

where :

ΔV_{RPL} is the output ripple voltage

R_{ESR} is the serial equivalent series resistance

C_{OUT} is the output capacitor

With COUT = 44μF, RESR = 10mΩ the output ripple voltage is calculated as

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$$\Delta V_{RPL} = 0.69 \times (10m + \frac{1}{8 \times 44\mu \times 570k}) = 10.3 \text{ [mV]}$$

* When selecting the value of the output capacitor COUT, please note that the value of capacitor CLOAD will add up to the value of COUT to be connected to VOUT.
Charging current to flow through the CLOAD, COUT and the IC startup, must be completed within the soft-start time this charge. Over-current protection circuit operates when charging is continued beyond the soft-start time, the IC may not start. Please consider in the calculation the condition that the lower maximum value capacitor CLOAD that can be connected to VOUT (max) is other than COUT.

Inductor ripple current maximum value of start-up (ILSTART) < Over Current Protection Threshold 1.8 [A](min)

Inductor ripple current maximum value of start-up (ILSTART) can be expressed in the following method.

ILSTART = Output maximum load current(IOMAX) + Charging current to the output capacitor (ICAP) + $\frac{\Delta IL}{2}$ [mV]

Charging current to the output capacitor (ICAP) can be expressed in the following method.

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{T_{SS}} \text{ [A]}$$

where :

C_{OUT} is the output capacitance

C_{LOAD} is the output load capacitance

T_{SS} is the soft start time

From the above equation, VIN = 24V, VOUT = 5V, L = 10µH, IOMAX = 1.0A (max), switching frequency FOSC = 484kHz (min), the output capacitor COUT = 44µF, TSS = 1.5ms soft-start time (min), it becomes the following equation when calculating the maximum output load capacitance CLOAD (max) that can be connected to VOUT.

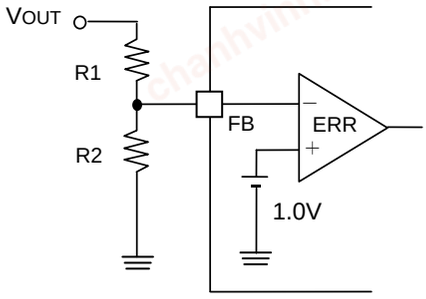
$$C_{LOAD}(max) < \frac{(1.8 - I_{OMAX} - \Delta I_L/2) \times T_{SS}}{V_{OUT}} - C_{OUT} = 73 \text{ [µF]}$$

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2. Output Voltage Set Point

The output voltage value can be set by the feedback resistance ratio.



$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times 1.0 \text{ [V]}$$

※ Minimum pulse range that can be produced at the output stably through all the load area is 150nsec for BD9E101FJ-LB.
Use input/output condition which satisfies the following method.

$$150(nsec) \leq \frac{V_{OUT}}{V_{IN} \times F_{OSC}}$$

Figure 47. Feedback Resistor Circuit

3. Input voltage start-up

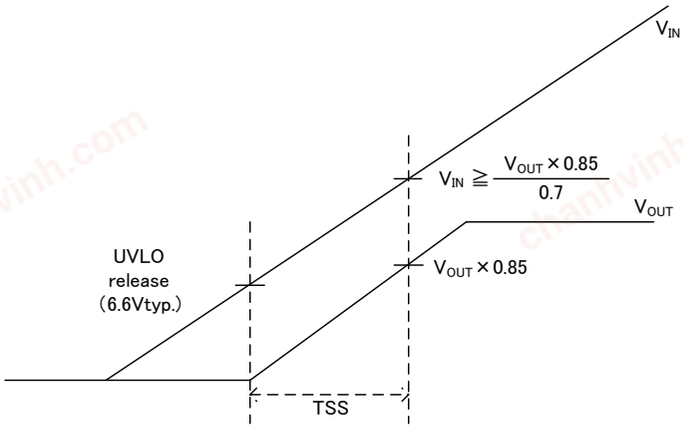


Figure 48. Input Voltage Start-up Time

Soft-start function is designed for the IC so that the output voltage will start according to the time it was decided internally. After UVLO release, the output voltage range will be less than 70% of the input voltage at soft-start operation. Please be sure that the input voltage of the soft-start after startup is as follows.

$$V_{IN} \geq \frac{V_{OUT} \times 0.85}{0.7} \text{ [V]}$$

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4. Phase Compensation

A current mode control buck DC/DC converter is a two-pole, one-zero system. The two poles are formed by an error amplifier and load and the one zero point is added by the phase compensation. The phase compensation resistor R_{CMP} determines the crossover frequency F_{CRS} where the total loop gain of the DC/DC converter is 0 dB. The high value of this crossover frequency F_{CRS} provides a good load transient response characteristic but inferior stability. Conversely, specifying a low value for the crossover frequency F_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired.

(1) Selection of Phase Compensation Resistor R_{CMP}

The phase compensation resistance R_{CMP} can be determined by using the following equation.

$$R_{CMP} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} [\Omega]$$

where :

V_{OUT} is the output voltage

F_{CRS} is the crossover frequency

C_{OUT} is the output capacitance

V_{FB} is the feedback reference voltage (1.0 V (Typ))

G_{MP} is the current sense gain (7 A/V (Typ))

G_{MA} is the error amplifier transconductance (150 µA/V (Typ))

(2) Selection of phase compensation capacitance C_{CMP}

For stable operation of the DC/DC converter, inserting a zero point under 1/6 of the zero crossover frequency cancels the phase delay due to the pole formed by the load often, thus, providing favorable characteristics.

The phase compensation capacitance C_{CMP} can be determined by using the following equation.

$$C_{CMP} = \frac{1}{2\pi \times R_{CMP} \times F_Z} [F]$$

where

F_Z is the Zero point inserted

(3) Loop stability

To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided. Phase margin of at least 45 degrees in the worst conditions is recommended. The feed forward capacitor C_{RUP} is used for the purpose of forming a zero point together with the resistor R_{UP} to increase the phase margin within the limited frequency range. Using a C_{RUP} is effective when the R_{UP} resistance is larger than the combined parallel resistance of R_{UP} and R_{DW}.

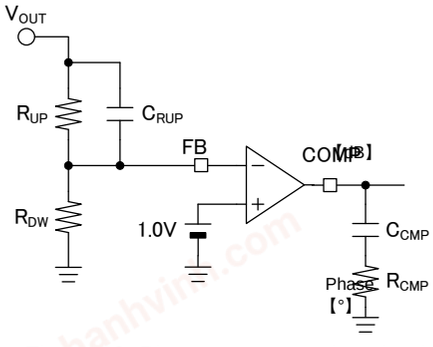


Figure 49. Phase compensation circuit

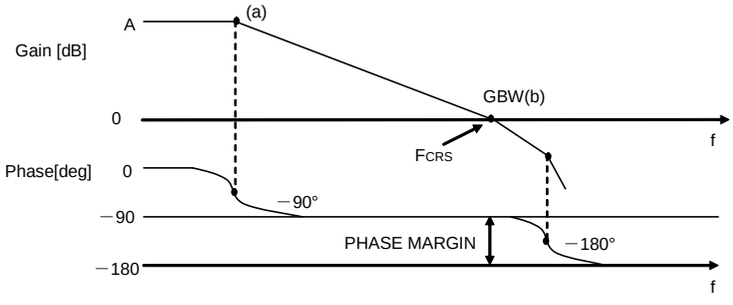


Figure 50. Bode plot

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PCB Layout Design

In buck DC/DC converters, a large pulsed current flows in two loops. The first loop is the one into which the current flows when the High Side FET is turned on. The flow starts from the input capacitor CIN, runs through the FET, inductor L and output capacitor COUT and back to ground of CIN via ground of COUT. The second loop is the one into which the current flows when the Low Side FET is turned on. The flow starts from the Low Side FET, runs through the inductor L and output capacitor COUT and back to ground of the Low Side FET via ground of COUT. Tracing these two loops as thick and short as possible allows noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors, in particular, to the ground plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

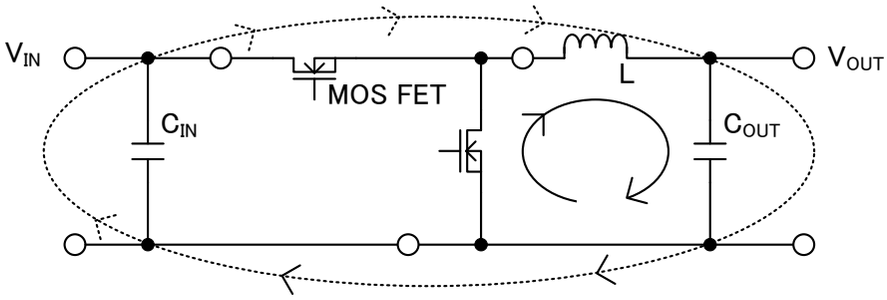
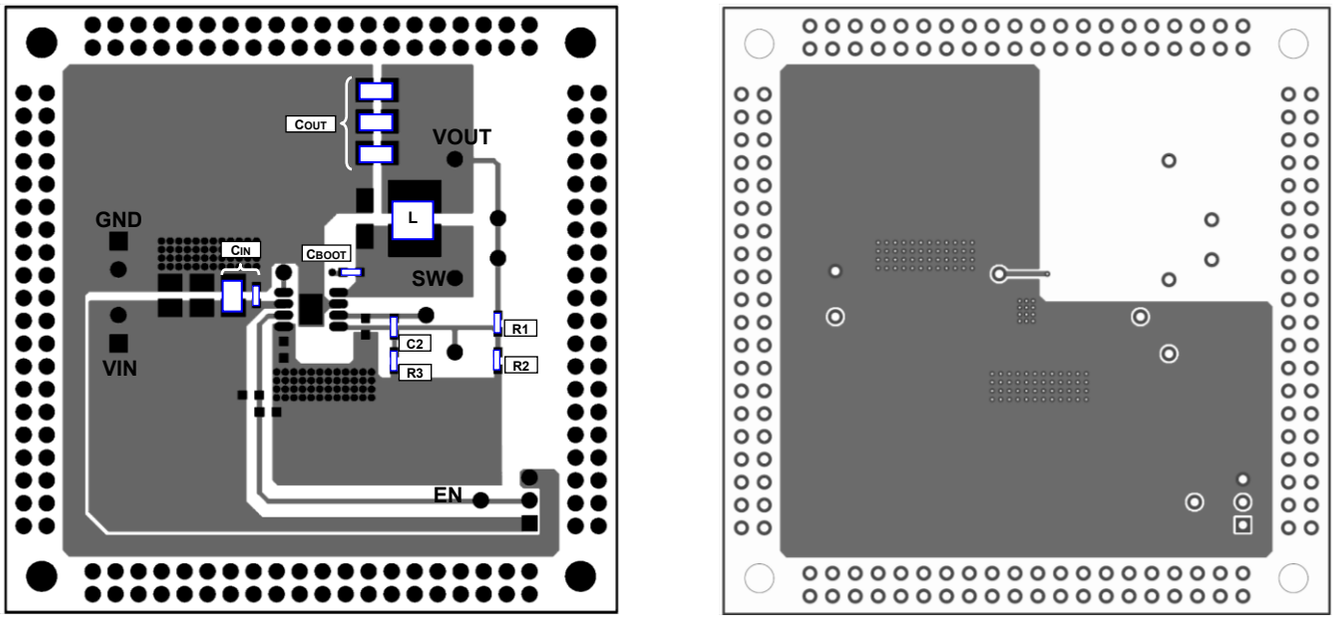


Figure 51. Current Loop of Buck Converter

Accordingly, design the PCB layout with particular attention paid to the following points.

- Provide the input capacitor as close to the VIN terminal as possible on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the ground node to assist in heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Trace to the inductor as thick and as short as possible.
- Provide lines connected to FB and COMP as far as possible from the SW node.
- Provide the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.



Top Layer

Bottom Layer

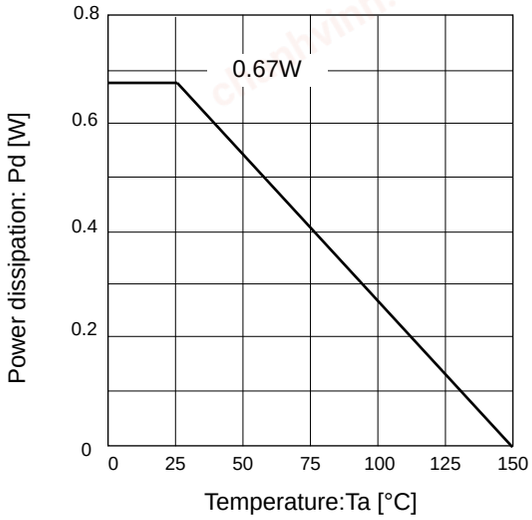
Figure 52. Example of Sample Board Layout Pattern

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Power Dissipation

When designing the PCB layout and peripheral circuitry, sufficient consideration must be given to ensure that the power dissipation is within the allowable dissipation curve.



θJA=185.2°C/W
1 layer board
(back side copper foil area:70mm × 70mm)

Figure 53. Power Dissipation (SOP-J8)

I/O equivalence circuit(s)

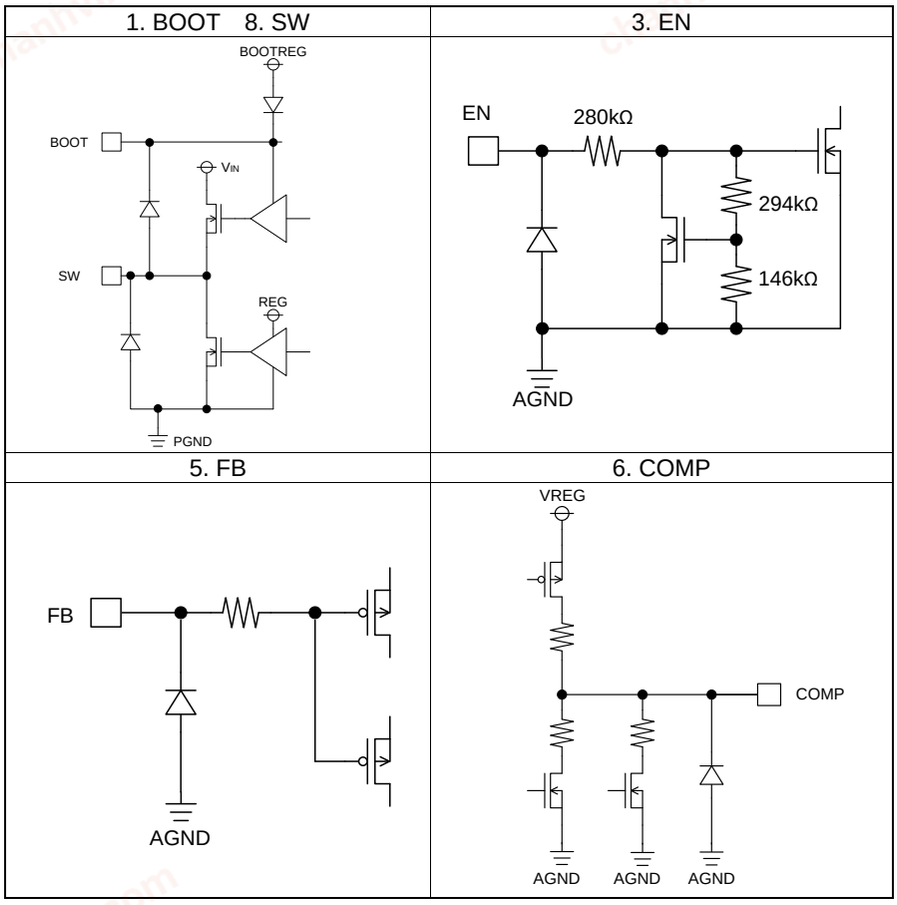


Figure 54. I/O Equivalent Circuit Chart

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Terminals

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

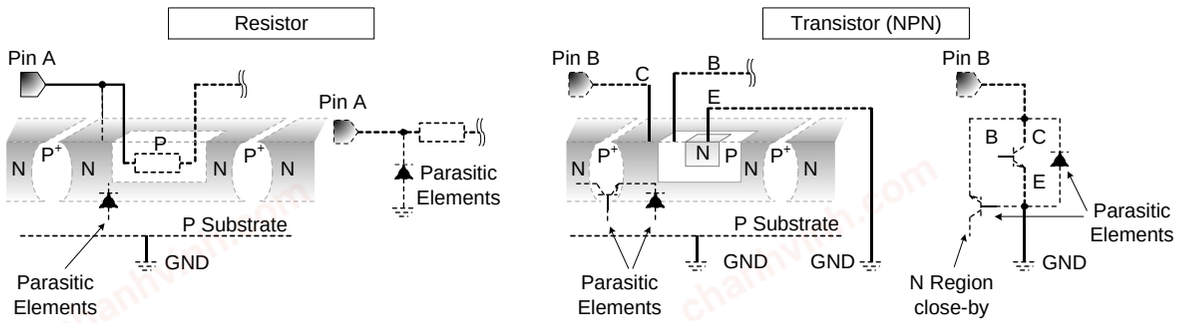


Figure 55. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information

B D 9 E 1 0 1 F J - L B H 2

Part Number

Package
FJ: SOP-J8

Product class
LB: for Industrial applications
Packaging and forming specification
H2: Embossed tape and 18cm reel
(Quantity : 250pcs)

B D 9 E 1 0 1 F J - L B E 2

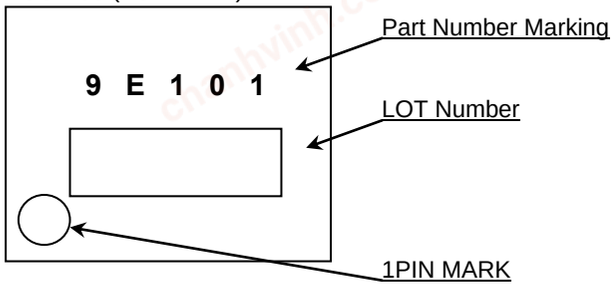
Part Number

Package
FJ: SOP-J8

Product class
LB: for Industrial applications
Packaging and forming specification
E2: Embossed tape and 32.8cm reel
(Quantity : 2500pcs)

Marking Diagrams

SOP-J8 (TOP VIEW)

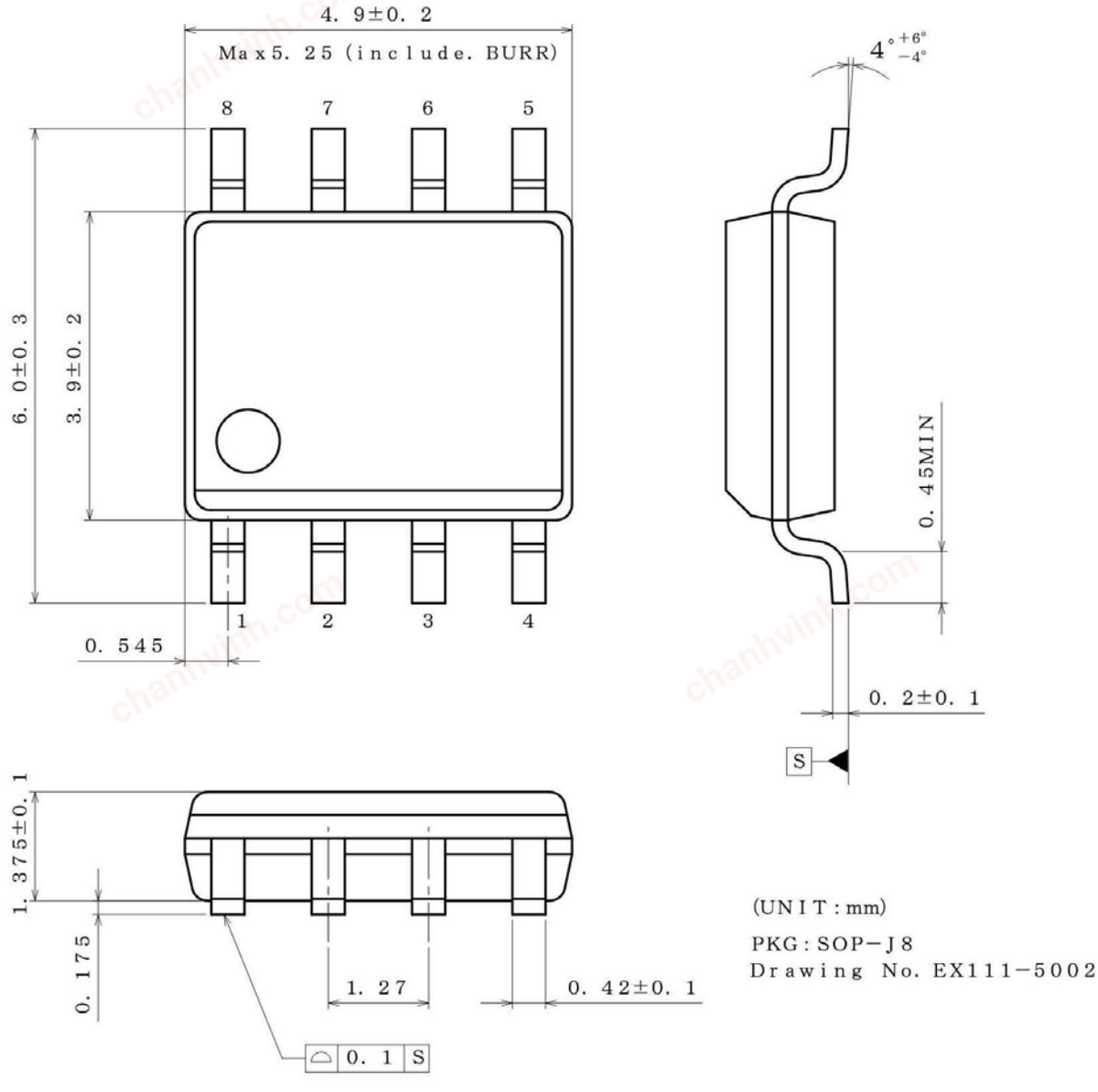


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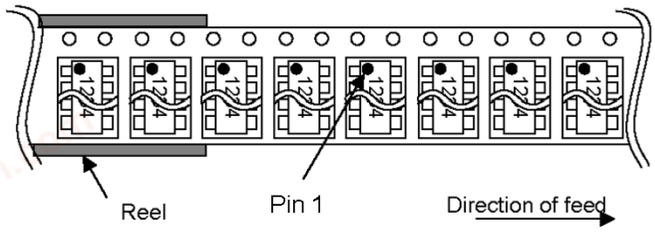
Physical Dimension, Tape and Reel Information

Package Name	SOP-J8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	E2 : 2500pcs / H2 : 250pcs
Direction of feed	The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Draft	Changes
01.Nov.2013	001	New Release
21.Feb.2014	002	Delete sentence “and log life cycle” in General Description and Futures. Change “Packaging and forming specification” from E2 to H2.
14.May.2014	003	Add E2 rank of “Packaging and forming specification”

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM’s internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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