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Datasheet

LED Drivers for LCD Backlights

White LED Driver for large LCD Panels (DCDC Converter type)

BD9479FV

●General Description

BD9479FV is a high efficiency driver for white LEDs and designed for large LCDs. This IC is built-in a boost DCDC converters that employ an array of LEDs as the light source. BD9479FV has some protect function against fault conditions, such as the over-voltage protection (OVP), the over current limit protection of DCDC (OCP), the short circuit protection (SCP), the open detection of LED string. Therefore BD9479FV is available for the fail-safe design over a wide range output voltage.

●Key Specification

- Operating power supply voltage range: 9.0V to 35.0V
- Oscillator frequency: 150kHz (RT=100kΩ)
- Operating Current: 8.7mA (typ.)
- Operating temperature range: -40℃ to +85℃

●Applications

TV, Computer Display, Notebook, LCD Backlighting

●Features

- 8ch LED constant current driver (external PNP Tr Type)
- Maximum LED setting current 500mA (VREF pin setting)
- Build-in DC/DC converter
- Analog Dimming (Linear) function
- Individual channel PWM Dimming function
- LED protection function (Open Short protection) [PWM-independent Type]
- Output short protection (OVP)
- Built-in Timer latch function (CP)
- Built-in under voltage Lockout function (UVLO)・over voltage protection (OVP)
- Built-in FAIL indication function
- Built-in OVP voltage Feedback function
- Built-in PWM-independent soft start circuit
- SSOP-B40 Package

●Package

	W(Typ.)	D(Typ.)	H(Max.)
SSOP-B40:	13.6mm x 7.80mm x 1.80mm		
Pin Pitch:			0.65mm

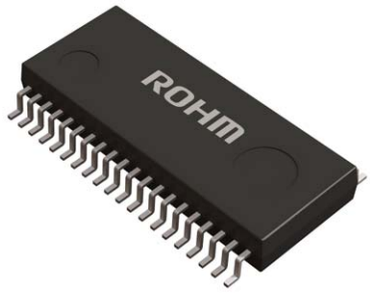


Figure 1. SSOP-B40

●Typical Application Circuit

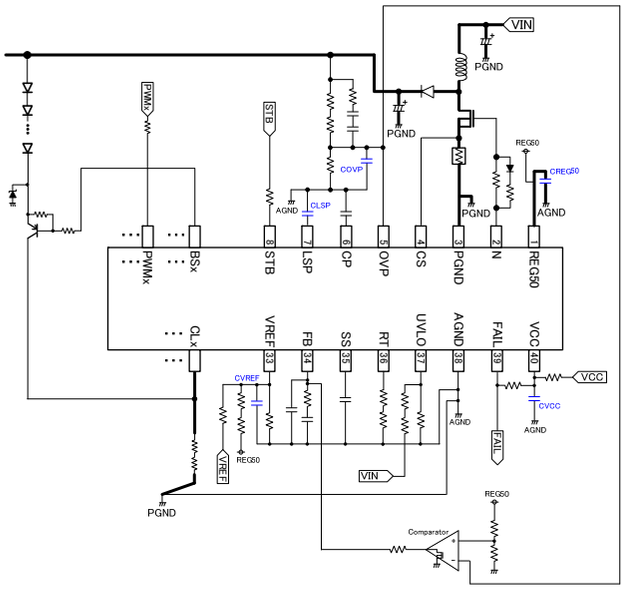


Figure 2. Typical Application Circuit

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●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Power supply voltage	VCC	36	V
BS1-8 terminal voltage	BS1-8	40	V
OVP, STB, PWM1-8,VREF,UVLO terminal voltage	OVP, STB, PWM1-8,VREF,UVLO	20	V
REG50, N, CS, CP, LSP, CL1-8, FB, SS, RT terminal voltage	REG50, N, CS, CP, LSP, CL1-8, FB, SS, RT	7	V
Power dissipation (SSOP-B40)*1	Pd	1.125(Note1)	W
Operating temperature range	Ta(opr)	-40 to +85	℃
Storage temperature range	Tstg	-55 to +150	℃
Junction temperature	Tjmax	150	℃

(Note1) SSOP-B40 package at Ta=25°C or higher, de-rating power rating by −9.0mW/°C(70.0mm x 70.0mm x1.6mm with 1-layer board)

●Operating Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
VCC supply voltage	VCC	9.0 to 35.0	V
Analog Dimming setting (VREF Pin) range	VREF	0.6 to 3.0	V
LSP setting voltage range	VLSP	0.3 to 3.0	V
DC/DC oscillation frequency	FCT	100 to 800	kHz
PWM pin input frequency range	F_PWM	0.05 to 20	kHz

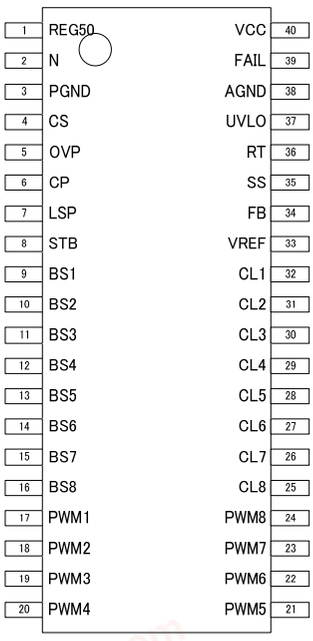
Above operating condition are the constants of IC itself. Please pay attention at the actual set.

●Recommended external component range

Parameter	Symbol	Limits	Unit
VCC pin connecting capacity	CVCC	1 to 100	uF
DC/DC frequency setting resistant	RRT	18.75 to 150	kΩ
REG50 pin connecting capacity	CREG50	1.0 to 10	uF
Soft start setting capacity	CSS	0.001 to 1.0	uF
Timer Latch setting capacity	CCP	0.001 to 1.0	uF

Above operating condition are the constants of IC itself. Please pay attention at the actual set.

●Pin Configuration



SSOP-B40

Figure 3. Pin Configuration

●Marking diagram and physical dimension

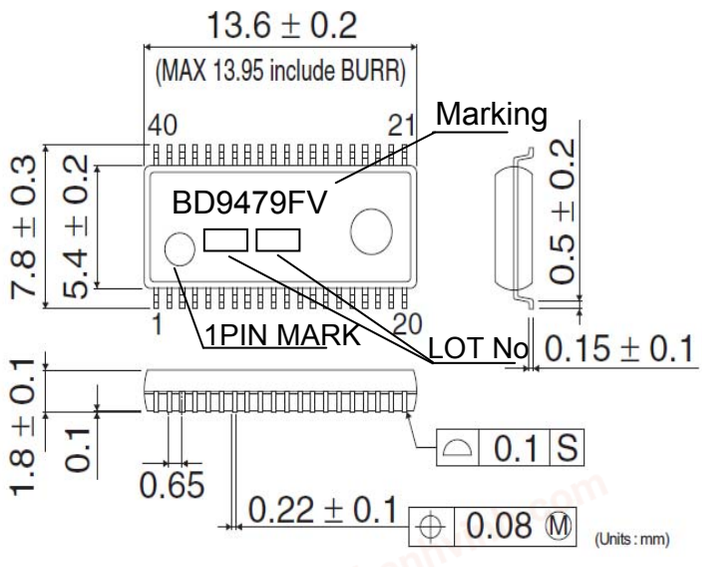


Figure 4. Physical Dimension

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●**Electrical Characteristics** (Unless otherwise noted, Ta = 25°C, VCC=24V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[Whole Device]						
Operation current	ICC	—	8.7	14.0	mA	STB=3V, PWM1-8=0V
Standby current	IST	—	12	24	uA	STB=0V
[UVLO Block]						
Operation Voltage（VCC）	VUVLO_VCC	6.5	7.5	8.5	V	VCC=SWEEP UP
Hysteresis Voltage（VCC）	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
Operation Voltage（UVLO）	VUVLO	2.91	3.00	3.09	V	UVLO=SWEEP UP
Hysteresis Voltage（UVLO）	VUHYS	170	210	250	mV	UVLO=SWEEP DOWN
[DC/DC Block]						
Error amp Base Voltage	VEAMP	0.55	0.60	0.65	V	BSx pin, VREF=0.9V
Oscillation frequency	FCT	142.5	150.0	157.5	kHz	RT=100kΩ
N pin MAX DUTY output	NMAX_DUTY	90	95	99	%	RT=100kΩ
N pin source ON resistor	RNSO	0.5	1	2	Ω	
N pin sink ON resistor	RNSI	0.5	1	2	Ω	
RT pin Voltage	VRT	1.00	1.50	2.00	V	RT=100kΩ
SS pin source current	ISSSO	-2.4	-2.0	-1.6	uA	
Soft start ended Voltage	VSS_ED	3.6	4.0	4.4	V	
FB pin source current	IFBSO	-110	-100	-90	uA	
FB pin sink current	IFBSI	85	100	115	uA	
Over current detect Vlotage	VCS	0.35	0.40	0.45	V	
[DC/DC Protection Block]						
CP pin source current	ICPSO	-2.4	-2.0	-1.6	uA	
CP pin detect Voltage	VCP	2.375	2.500	2.625	V	
OVP High detect voltage	VOVPH	2.137	2.250	2.363	V	
OVP Feedback Voltage	VOVPFB	2.375	2.500	2.625	V	
OVP Low detect Voltage	VOVPL	0.14	0.20	0.30	V	
[LED PNP Driver Block]						
CL pin current setting Voltage	VRCL	295.5	300.0	304.5	mV	VREF=0.9V
CL pin current setting Voltage (Analog MAX)	VRCLMAX	-3%	1.0	+3%	V	VREF max=3.0V
CL pin current setting Voltage (Analog MIN)	VRCLMIN	-3%	200.0	+3%	mV	VREF min=0.6V
PNP Driver output sink resistor	RBS	55	80	120	Ω	PWMx=High, VCL=Low
VREF pin input current	IVREF	-1.0	0.0	1.0	uA	VREF=1V

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●**Electrical Characteristics** (Unless otherwise noted, Ta = 25°C, VCC=24V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[LED protection Block]						
LED OPEN Detect Voltage	VOPEN	0.05	0.10	0.15	V	BSx=SWEEP DOWN
LED SHORT Detect Voltage	VLSP	8.5	9.0	9.5	V	BSx=SWEEP UP, LSP=OPEN
CL pin Detect Voltage	VCLLVP	0.05	0.10	0.15	V	
LSP pin pull high resistor	RULSP	1260	2100	3180	kΩ	LSP=0V
LSP pin pull down resistor	RDLSP	540	900	1620	kΩ	LSP=3V
[REG50 Block]						
REG50 output Voltage	REG50	4.95	5.00	5.05	V	Io=-5mA
REG50 maximum output current	|IREG50|	5	-	-	mA	※DCDC block consumption is neglected.
[STB Block]						
STB pin HIGH Voltage	STBH	2.0	-	VCC	V	STB=SWEEP UP
STB pin LOW Voltage	STBL	-0.3	-	0.8	V	STB=SWEEP DOWN
STB pin Pull Down resistor	RSTB	0.5	1.0	2.0	MΩ	STB=3.0V
[PWM input Block]						
PWMx pin High detect voltage	PWM_H	2.0	-	18	V	PWM=SWEEP UP
PWMx pin Low detect voltage	PWM_L	-0.3	-	0.8	V	PWM=SWEEP DOWN
PWMx pin Pull Down resistor	RPWM	0.5	1.0	2.0	MΩ	PWM=3.0V
[FAIL Block(OPEN DRAIN)]						
FAIL pin Ron	RFAIL	30	50	85	Ω	
FAIL pin Leakage current	ILFAIL	-1.0	0.0	1.0	uA	FAIL=36V

(This product is not designed to be radiation-proof.)

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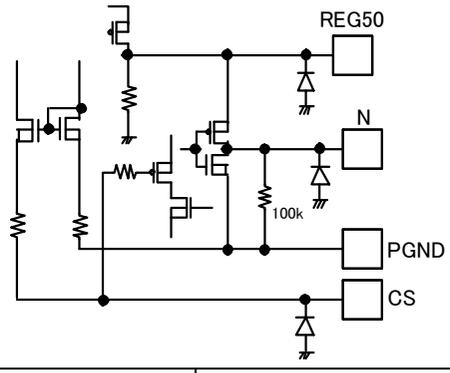
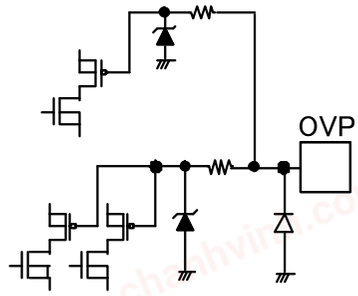
●Pin Descriptions

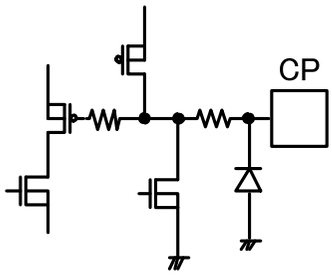
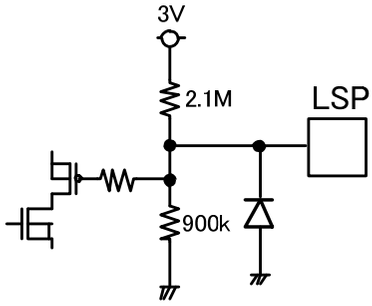
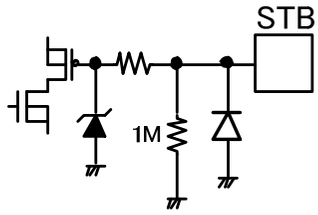
Pin No	Pin Name	In/Out	Function	Rating [V]
1	REG50	Out	5V regulator output for N output pin	-0.3 ~ 7
2	N	Out	DC/DC switching output pin	-0.3 ~ 7
3	PGND	-	Power GND	-
4	CS	In	DCDC external NMOS current monitor pin	-0.3 ~ 7
5	OVP	In	Overvoltage protection detection pin	-0.3 ~ 20
6	CP	Out	Timer Latch setting pin	-0.3 ~ 7
7	LSP	In	LED short voltage setting pin	-0.3 ~ 7
8	STB	In	Enable pin	-0.3 ~ 20
9	BS1	In	PNP Tr Base connecting pin1	-0.3 ~ 40
10	BS2	In	PNP Tr Base connecting pin2	-0.3 ~ 40
11	BS3	In	PNP Tr Base connecting pin3	-0.3 ~ 40
12	BS4	In	PNP Tr Base connecting pin4	-0.3 ~ 40
13	BS5	In	PNP Tr Base connecting pin5	-0.3 ~ 40
14	BS6	In	PNP Tr Base connecting pin6	-0.3 ~ 40
15	BS7	In	PNP Tr Base connecting pin7	-0.3 ~ 40
16	BS8	In	PNP Tr Base connecting pin8	-0.3 ~ 40
17	PWM1	In	Dimming signal input pin1	-0.3 ~ 20
18	PWM2	In	Dimming signal input pin2	-0.3 ~ 20
19	PWM3	In	Dimming signal input pin3	-0.3 ~ 20
20	PWM4	In	Dimming signal input pin4	-0.3 ~ 20
21	PWM5	In	Dimming signal input pin5	-0.3 ~ 20
22	PWM6	In	Dimming signal input pin6	-0.3 ~ 20
23	PWM7	In	Dimming signal input pin7	-0.3 ~ 20
24	PWM8	In	Dimming signal input pin8	-0.3 ~ 20
25	CL8	Out	PNP Tr collector ・current detection pin8	-0.3 ~ 7
26	CL7	Out	PNP Tr collector ・current detection pin7	-0.3 ~ 7
27	CL6	Out	PNP Tr collector ・current detection pin6	-0.3 ~ 7
28	CL5	Out	PNP Tr collector ・current detection pin5	-0.3 ~ 7
29	CL4	Out	PNP Tr collector ・current detection pin4	-0.3 ~ 7
30	CL3	Out	PNP Tr collector ・current detection pin3	-0.3 ~ 7
31	CL2	Out	PNP Tr collector ・current detection pin2	-0.3 ~ 7
32	CL1	Out	PNP Tr collector ・current detection pin1	-0.3 ~ 7
33	VREF	In	LED voltage setting pin	-0.3 ~ 20
34	FB	In/Out	DCDC phase-compensation pin	-0.3 ~ 7
35	SS	Out	Soft Start pin	-0.3 ~ 7
36	RT	Out	DCDC frequency setting resistor connection pin	-0.3 ~ 7
37	UVLO	In	Under voltage Lockout protection pin	-0.3 ~ 20
38	AGND	-	Analog GND	-
39	FAIL	Out	Error detection output pin	-0.3 ~ 36
40	VCC	-	Power supply pin	-0.3 ~ 36

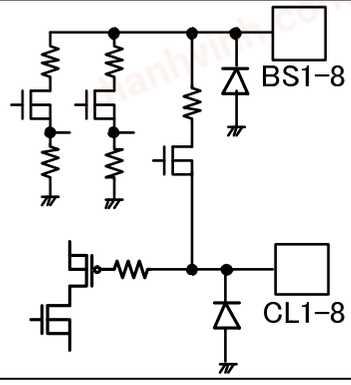
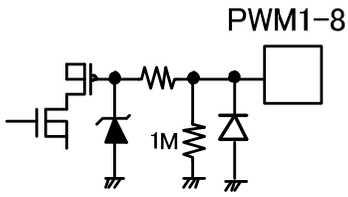
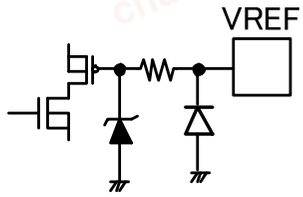
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●Pin ESD Type

REG50 / N / PGND / CS	OVP
	

CP	LSP	STB
		

$BS_{(1-8)}$ / $CL_{(1-8)}$	$PWM_{(1-8)}$	VREF
		

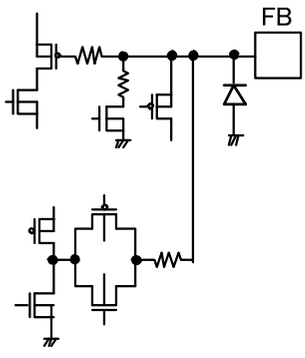
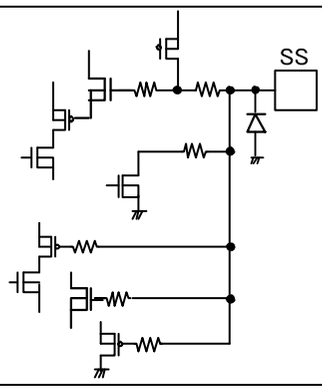
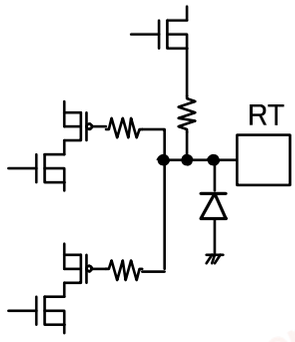
FB	SS	RT
		

Figure 5-1. Pin ESD Type

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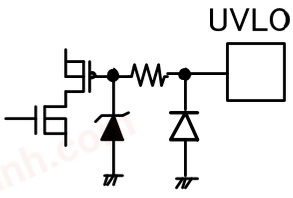
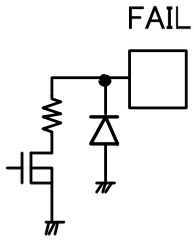
UVLO	FAIL
	

Figure 5-2. Pin ESD Type

●Block Diagram

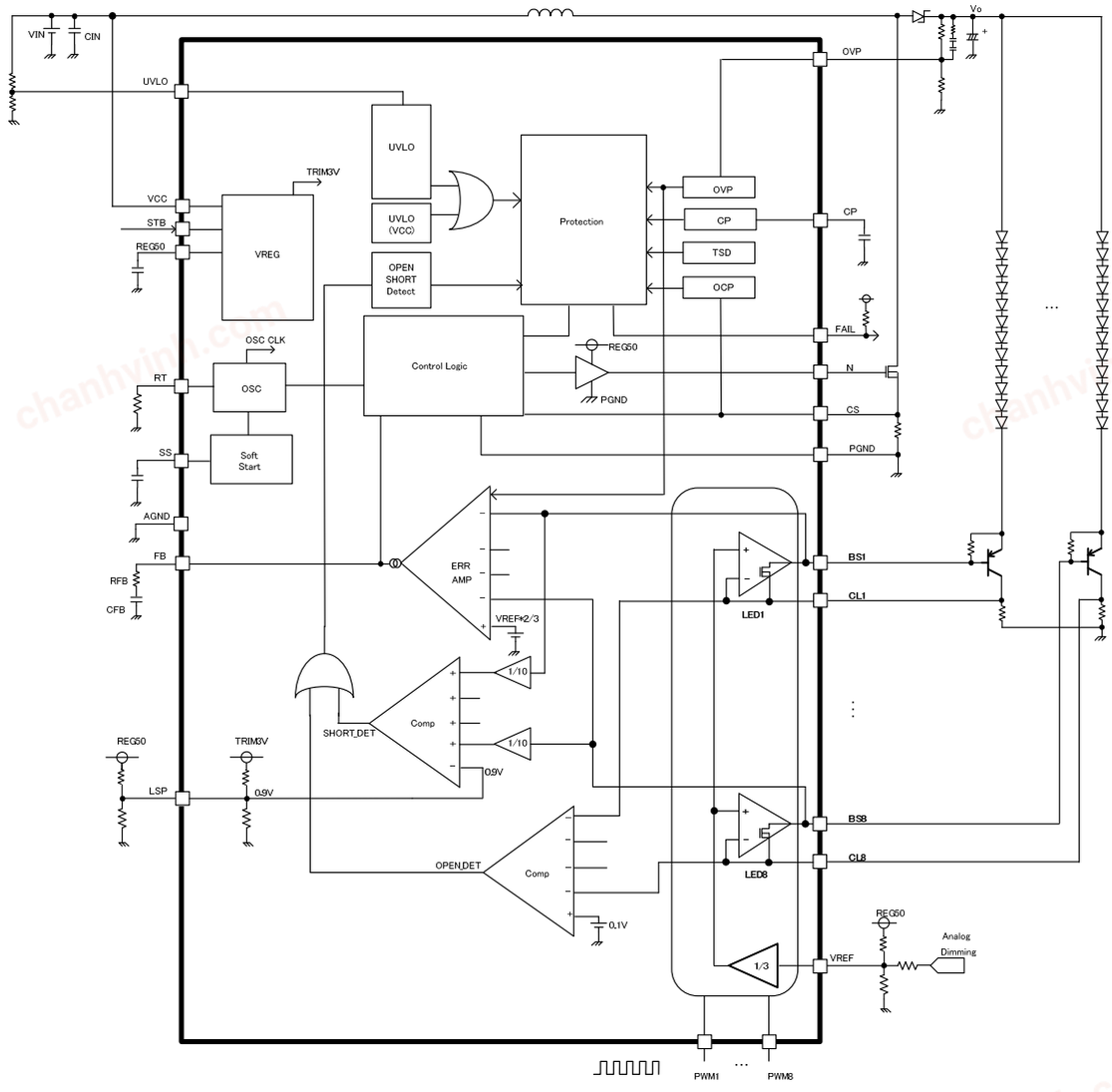


Figure 6. Block Diagram

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●Typical Performance Curve

Figure 7. Operating Current (ICC) [mA] vs. VCC[V]

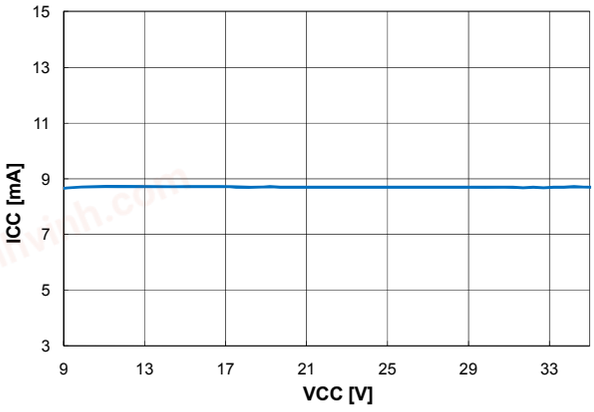


Figure 8. REG50[V] vs. VCC[V]

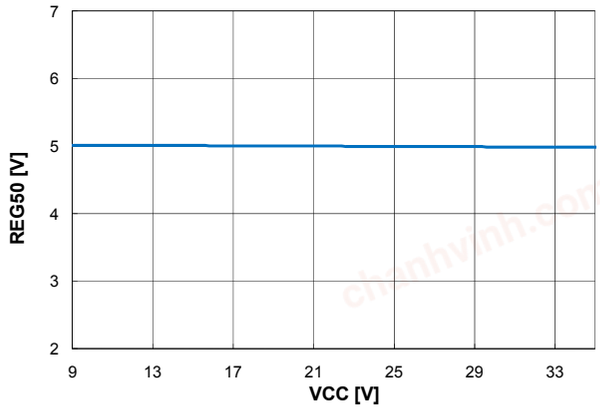


Figure 9. CL1 Voltage (VRCL1) [V] vs. VREF [V]

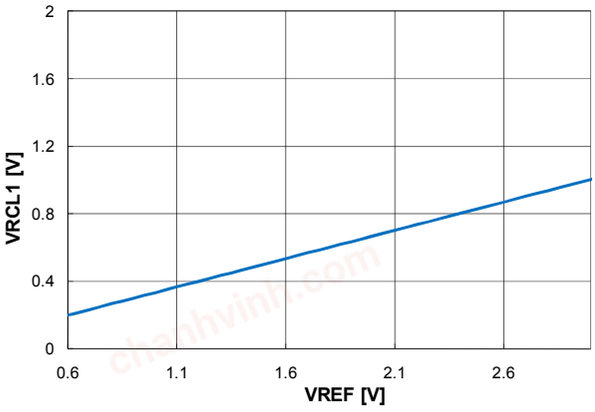


Figure 10. N Frequency [MHz] vs. R_RT [MΩ]

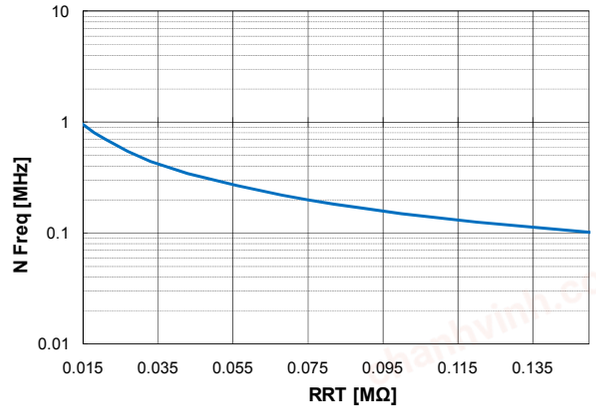


Figure 11. CL1 Voltage (VRCL1) [V] vs. Temp [℃]

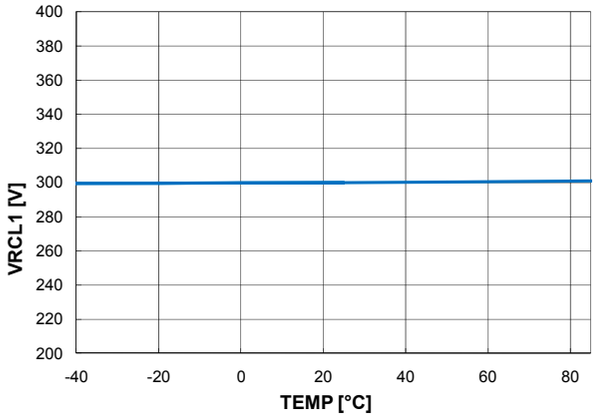
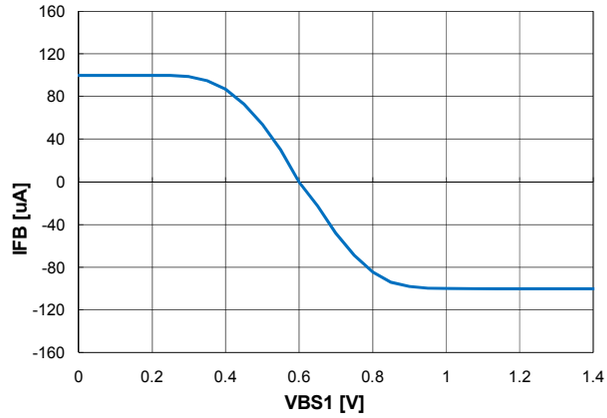


Figure 12. FB Current (IFB) [uA] vs. VBS1 [V]



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●Pin Function

○Pin 1: REG50

The REG pin is used in the DC/DC converter driver block to output 5V power. The maximum operating current is 5mA. Using the REG pin at a current higher than 5mA can affect the N pin output pulse, causing the IC to malfunction and leading to heat generation of the IC itself. To avoid this problem, it is recommended to make load setting to the minimum level.

○Pin 2:N

The N pin is used to output power to the external NMOS gate driver for the DC/DC converter in the amplitude range of approx. 0 to 5V. Frequency setting can be made with a resistor connected to the RT pin. For details of frequency setting, refer to the description of the ＜RT pin＞.

○Pin 3: PGND

The PGND pin is a power ground pin for the driver block of the N output pin.

○Pin 4: CS

CS pin is current detect for DC/DC current mode inductor current control pin.

Current flowing through the inductor is converted into voltage by the current sensing resistor RCS connected to the CS pin and this voltage is compared with voltage set with the error amplifier to control the DC/DC output voltage.

The CS pin also incorporates the overcurrent protection (OCP) function. If the CS pin voltage reaches 0.4V (Typ.) or more, switching operation will be forcedly stopped.

In order to prevent the malfunction while OCP occurred in BD9479FV,it equipped with mask function.It mask OCP signal within 200ns interval after N driver is outputted.

○ Pin 5: OVP

The OVP pin is an input pin for overvoltage protection and short circuit protection of DC/DC output voltage.When voltage of it over 2.25V or higher,CP pin start to charge.When it over 2.5V(typ),it will control FB pin.When OVP pin voltage is near 2.5V,DCDC output feedback will controlled by OVP pin voltage.
When OVP pin voltage<0.2V (typ.) or lower,short circuit protection (SCP) function is activated, and output of Gate driver will become low immediately.

○ Pin 6: CP

CP pin which sets the time from detection of abnormality until shutdown (Timer latch).It charges constant current of 2.0uA to capacitor externally connected with CP pin and shuts down when it exceeds 2.5V(Typ.).

○ Pin 7: LSP

LED Short detect voltage setting pin.When LSP=OPEN, LSP pin voltage is 0.9V(typ), the BSx pin of LED SHORT detect voltage is set to 9V.
The 10 times of LSP pin voltage is the BSx pin LED SHORT protection detect voltage.
Please set LSP pin input voltage range from 0.3V～3.0V.

○ Pin 8 :STB

ON/OFF setting pin and allowed for use to reset the IC from shutdown.
※The IC state is switched (i.e., The IC is switched between ON and OFF state) according to voltages input in the STB pin. Avoid using the STB pin between two states (0.8 to 2.0V).

○ Pin 9-16 :BS1-BS8

LED DRIVER output pin.Please connect to Base Terminal of external PNP Tr.

○ Pin 17-24 :PWM1 – PWM8

ON/OFF terminal of LED driver pin.It inputs PWM dimming signal directly to adjust output DUTY dimming.
High/Low level of PWM terminal is shown as follows:

State	PWM Voltage
LED ON state	PWM= 2.0V~5.0V
LED OFF state	PWM= －0.3V～0.8V

○ Pin 25-32 : CL8 – CL1

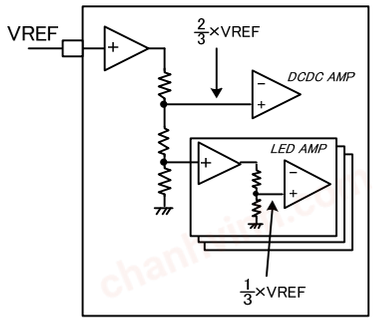
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LED current detect pin.By monitoring voltage of CLx pin to detect LED current.Please connect resistor to collector pin of external PNP Tr.

○ Pin 33 : VREF

LED current setting pin.1/3(typ) of applied voltage to VREF pin will be LED current feedback voltage, 2/3(typ.) of its voltage will be DCDC feedback voltage（the lowest BSx pin feedback voltage）.
Basically, because hi accuracy of resistor divider is inputted to VREF pin externally, the IC internally will be OPEN（High Impedance）state.Please use external power to design it.It cannot be used in OPEN state.



○ Pin 34 : FB

Current mode control DC/DC converter error amplifier output pin.By monitoring voltage of BS（1～8）pin, the highest Vf of LED column will set 2/3(typ.) of applied VREF voltage to BS pin voltage to control inductor current.
The phase compensation setting has described separately.
In addition, PWM pin will become High Impedance when all PWM signals are in low state, and will maintain FB voltage.

○ Pin 35 : SS

The SS pin is used to set the soft start time and duty for soft start duration.SS pin normally sources 2.0uA (Typ.) of current.When STB pin become high, it wait for in any one PWMx signal from low to high.In start-up duration, SS will not charge because all PWMx pin are in low state.
The BD9479FV has a built-in soft start startup circuit independent of PWM light modulation, and thereby raises FB voltage as SS pin voltage rises independent of the duty cycle range of PWM light modulation.Please pay attention to overshoot problem will occur while low duty is inputted to IC IN start-up duration.

○ Pin 36 : RT

RT sets charge/discharge current determining frequency inside IC.
Only a resistor connected to RT determines saw-tooth wave frequency inside IC.
When RT=100,Frequency=150kHz(typ.).

For calculation example, please refer to section in “3.2.2 – DC/DC drive frequency setting”.

○ Pin 37 : UVLO

UVLO pin of the coil of step-up DC/DC converter and the power for external NMOSFET.
At 3.0 V (typ.) or higher, IC starts step-up operation and stops at 2.79V or lower (typ.). (It is not shutdown of IC.)

○ Pin 38 : AGND

GND pin for analog system inside IC.

○ Pin 39 : FAIL

FAIL signal indication output pin (Open Drain).In normal operation, FAIL pin is OPEN when STB=Low.When an abnormality is detected, CP starts to charge to external capacitance and then shutdown IC while it reach 2.5V or higher.NMOS ON is 50 ohm(typ.）when IC is shutdown.When VCC voltage is insufficient or UVLO pin voltage is lower, FAIL pin is also in open state.

State	FAIL Output
Normal, STB=Low, （Under abnormality detection）	OPEN
Abnormality (shutdown), UVLO is detected	GND Level (50 ohm typ.)

○ Pin 40 : VCC

Power source pin of IC, which should be input in the range of 9 – 35 V.
Operation starts when VCC is 7.5V (TYP.) or higher and shuts down when VCC is 7.2 V (TYP.).

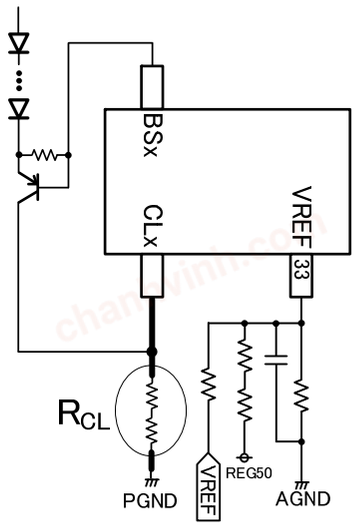
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●LED current setting (VREF pin, CLx pin)

Please decide VREF pin input voltage first.When Analog dimming is performed, please be noted that VREF pin input voltage range is (0.6V ～ 3.0V), and decide the input voltage in normal operation.Basically, if VREF pin voltage is high, it will cause power dissipation of external PNP Tr become high, so it is preferred to set the VREF pin voltage lower.

Later, VREF＝0.9V will be set as basic.For example if you create 0.9V from REG50, it is possible to use resistive divider by setting 82kohm and 18kohm.



In BD9479FV, the LED current detection is performed by CLx pin.CLx pin is controlled so that the voltage of 1/3V(typ.) of VREF voltage.If VREF=0.9V, CLx=0.3V to control external PNP Tr.Therefore,if 「R_{CL}」 is set as a resistance which between CLx pin and GND, and VREF pin voltage is set as 「V_{VREF}」, LED current 「I_{LED}」can be calculated as below.

$$R_{CL}\,[ohm] = \frac{V_{VREF}\,[V]}{I_{LED}\,[A] \times 3}$$

For current setting, set at each channel.For this reason, in 1ch～4ch and 5ch～8ch, it is possible to change current by setting 「R_{CL}」value.

●DCDC operation frequency setting (RT Pin)

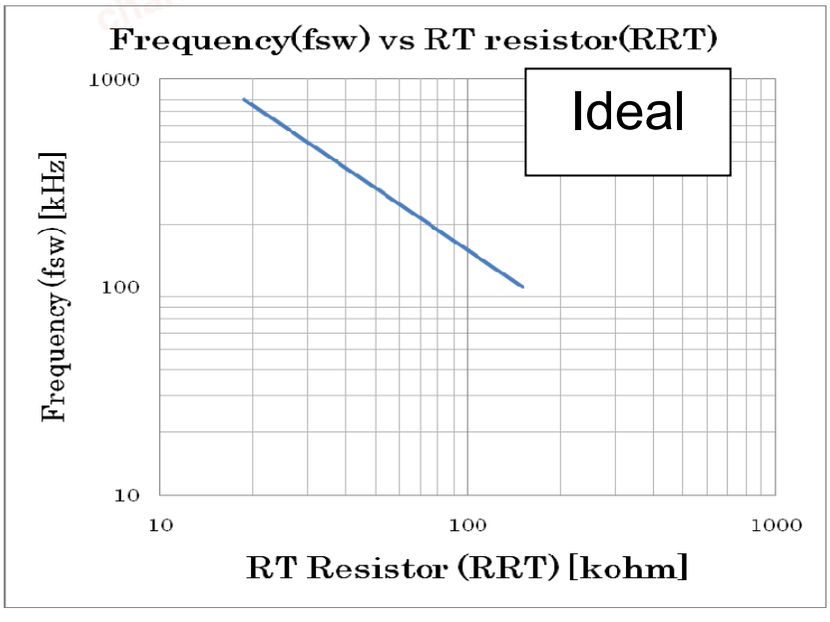
The operation frequency of DCDC output is set by resistance which connected to RT pin.

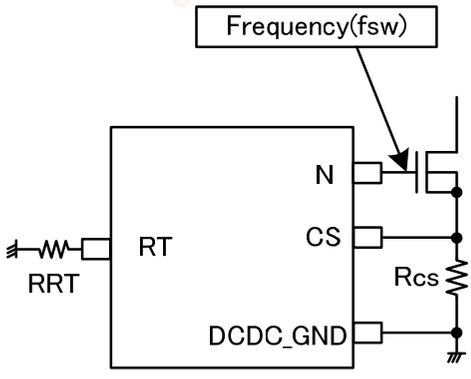
○**The relationship between operation and RT resistance (ideal)**

$$R_{RT} = \frac{15000}{f_{SW}\,[kHz]} \quad [k\Omega]$$

Here, fsw＝DCDC converter oscillation frequency[kHz]

Above is an ideal equation which do not putted with correction terms。
For accurate frequency setting, please confirm on the real system。
but, the frequency setting range is 100kHz～800kHz。





【Setting Example】

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If DCDC frequency is set to be 200kHz, RRT as below:

$$R_{RT} = \frac{15000}{f_{sw}[kHz]} = \frac{15000}{200[kHz]} = 75 \quad [k\Omega]$$

●Maximum DCDC output Voltage

In BD9479FV, the voltage of BSx pin is depending on VREF pin voltage.The maximum voltage of VREF pin（VREF＝3.0V）, the voltage of BSx pin will become 2.0V（2/3 of VREF voltage ）.

The maximum voltage of DCDC output will have be vary with 1.6V while Analog dimming is performed (2/3 of 3.0V - 0.6V).

●Soft Start Time setting (SS Pin)

The start-up time of DCDC output is adjusted by condenser which connected to SS pin.its performs constant current charge of 2.0uA to the external capacitor connected with SS pin, and the each protection and CP charge function will not activated before SS pin reaches to 4.0V.

（soft start time set here is mask time of CP charge, please pay attention to it is different from the time to stabilize DCDC output.The time to stabilize DCDC output is largely depending on step-up ratio and load condition.）

The soft start time「T_{SS}」, and SS pin external condenser「C_{SS}」 can be calculated as below.

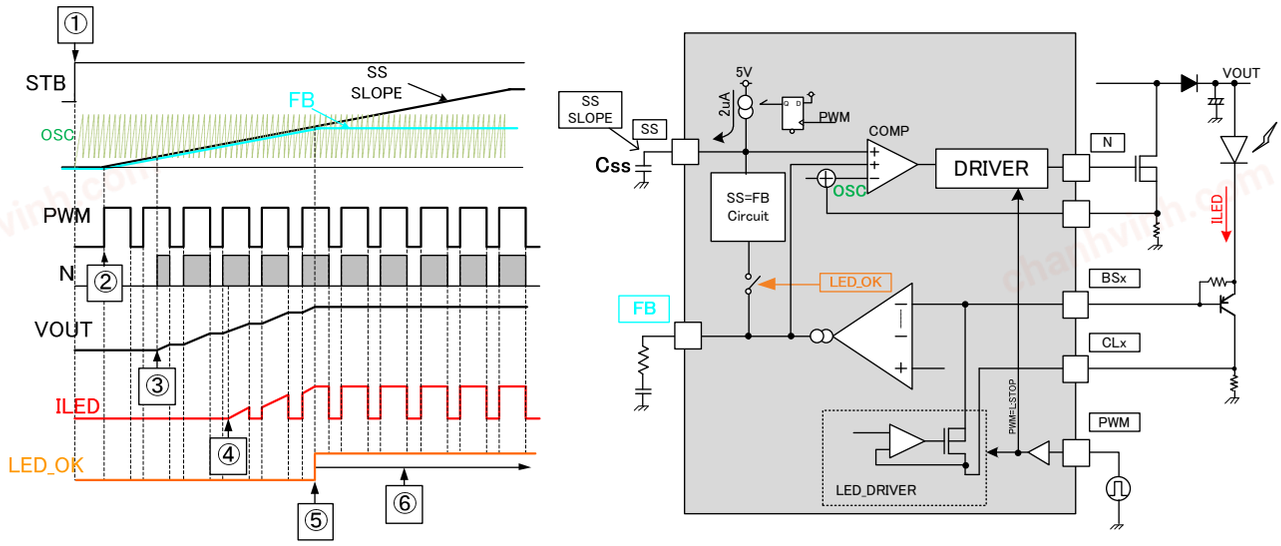
$$C_{SS}\ [F] = \frac{T_{SS}\ [\mathrm{sec}] \times 2.0 \times 10^{-6}\ [A]}{4.0[V]}$$

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●Start-up and soft start (SS) capacitance setting

The following describes the start-up sequence of this IC.



○Description of start-up sequence

①Set STB from Low to High

②System will be activated while PWM=H.SS start to charge.
At this time, a circuit in which SS pin voltage for slow start becomes equal to FB pin voltage operates to equalize the FB pin and SS pin voltages regardless of whether the PWM pin is set to Low or High l eve.

③Since the FB pin and SS pin reach the lower limit of the internal sawtooth wave of the IC, the DC/DC converter operates to start VOUT voltage rising.

④The Vout voltage continues rising to reach a voltage at which LED current starts flowing.

⑤When the LED current reaches the amount of current, isolate the FB circuit from the SS circuit. With this, the startup operation is completed.

⑥After that, normal operation is controlled by following the feedback voltage of LED pins.
If the SS pin voltage reaches 4V or higher, the LED protection function will be activated to forcedly end the SS and FB equalizing circuit.

○SS capacitance setting procedure

As mentioned above, this IC stops DC/DC converter when the PWM pin is set to Low level.conducts step-upoperation only in the section in which the PWM pin is maintained at High level. Consequently, setting the PWM duty cycle to the minimum will extend the start-up time.In addition, start-up time also varies with application of output capacitance selection, LED current, output voltage, and others.

Start-up time at minimum duty cycle can be approximated according to the following method.First, measure the start-up time of VOUT with a 100% DUTY and take this value as Trise_100.The startup time “Trise_min” for the relevant application with the minimum duty cycle is given by the following equation.

However, this calculation method is just for approximation, use it only as a reference.

Please set a time「T_{DCDCSS}」during which the SS pin voltage reaches the FB pin voltage longer than this star-tup.

Assuming that the FB pin voltage is VFB, the time is given by the following equation:

$$T_{rise_\min} = \frac{T_{rise_100}[\mathrm{sec}]}{Min_Duty[ratio]} \quad [\mathrm{sec}]$$

As a result, it is recommended to make SS capacitance setting so that “TDCDCSS” will be longer than “Trise_min”

$$T_{DCDCSS} = \frac{C_{SS}[F] \times VFB[V]}{2[\mu A]} \quad [\mathrm{sec}]$$

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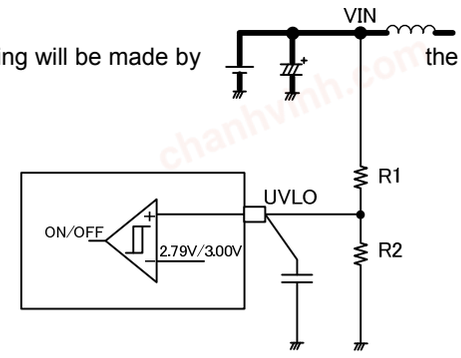
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●UVLO setting procedure

It is UVLO function for the DC/DC converter power supply.If its voltage reaches 3.0V (Typ.) or higher, the IC will start step-up operation. If it reaches 2.79V (Typ.) or less, the IC will stop the step-up operation.The UVLO pin is the high impedance type and involves no pull-down resistor, resulting in unstable operation in the open-circuited state. Avoid this problem, please make sure to input voltage by using resistor divider or otherwise.
If the VIN pin voltage to be detected is set by resistor divider R1 and R2 as described below, resistance setting will be made by the following equation:

○UVLO detection setting equation

Assuming that a voltage VIN decreasing, UVLO is "VIN_{DET}", R1 and R2 setting will be made by the following equation:



$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.79[V])}{2.79[V]} \quad [k\Omega]$$

○UVLO release voltage setting equation

When R1 and R2 setting is determined by the equation shown above, UVLO release voltage will be given by the following equation:

$$VIN_{CAN} = 3.0V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

【Setting example】

Assuming that the VIN input voltage is 24V, UVLO detection voltage is 17.36V, and R2 resistance is 13kΩ, R1 resistance setting is decided by the following equation:

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.79[V])}{2.79[V]} = 13[k\Omega] \times \frac{(17.36[V] - 2.79[V])}{2.79[V]} = 68[k\Omega]$$

Furthermore, VIN_{CAN} can be calculated as below equation when R1(68kΩ), R2(13kΩ) are decided above

$$VIN_{CAN} = 3.0[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 3.0[V] \times \frac{13[k\Omega] + 68[k\Omega]}{13[k\Omega]}[V] = 18.69[V]$$

***For the selection of DC/DC components, please also consider the inaccuracy of each componentts**.

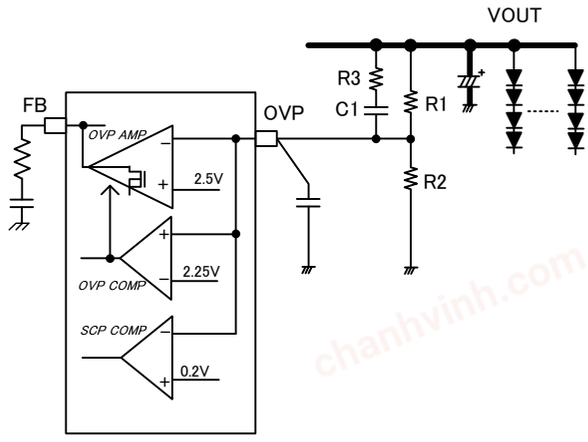
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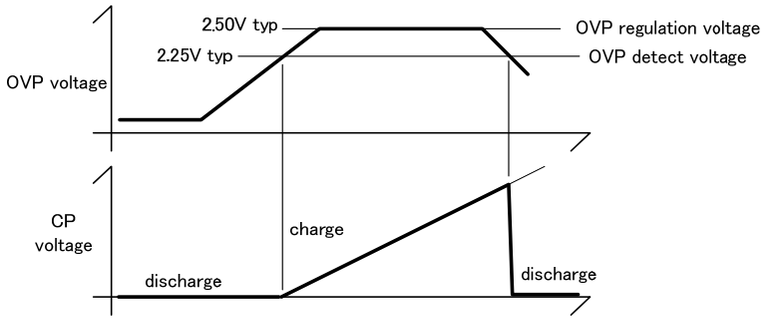
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●OVP/SCP setting procedure (OVP Pin)

There are two type of over voltage protection in BD9479FV.The one is OVP detection, another is OVP feedback.

Basically, the CP pin start to charge when OVP pin voltage higher than 2.25V.when OVP pin voltage is between 2.25V with 2.5V, the operation of DCDC is continued and CP start to charge only.When OVP pin voltage reaches 2.5V, until then the feedback voltage control will be switch from BSx pin to OVP pin（please refer to below figure）.For this reason, its prevent the voltage of OVP pin become 2.5V or higher when LED column has closed with impendence causing the rising of DCDC voltage.





OVP pin is also used for feedback control, please noted that not only the resistor divider of monitoring normal voltage, but also the external CR of phase compensation is needed.Basically, it is needed to aligned with the feedback gain to LED driver section.If R3 is same as R2（1k～10kΩ）, the breakdown voltage of C which connected to it should be confirmed first（And in series of two or more if necessary）, about 0.1uF is assumed and need to be decided in real system.

The following section describes setting procedures to be followed if the VOUT pin voltage to be detected is setby the use of resistive dividers R1 and R2.

○OVP detection setting equation

Assuming that voltage of VOUT rising abnormally and detecting OVP is "$VOVP_{DET}$", R1 and R2 setting will be made by the following equation.

（R2 will also affect phase compensation of feedback section, please set 1k ～ 10kΩ as basic.）

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 2.25[V])}{2.25[V]} \quad [k\Omega]$$

○OVP feedback setting equation

The OVP feedback「$VOVP_{FEED}$」voltage is calculated as below when R1,R2 is decided above:

$$VOVP_{FEED} = 2.5V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

○SCP detection setting

The SCP setting「$VSCP_{DET}$」voltage is calculated as below when R1,R2 is decided above:

$$VSCP_{DET} = 0.2V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

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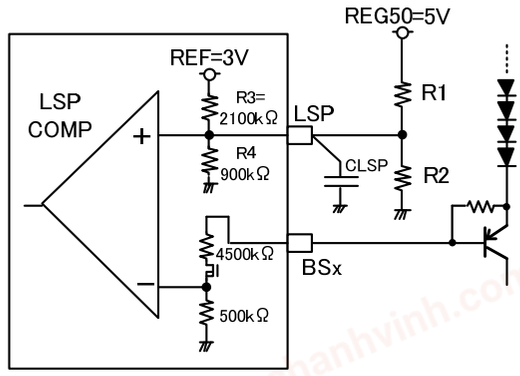
●LED short voltage setting(BSx pin, LSP pin)

The detection voltage of LED short when BSx pin higher than 9V while LSP pin is in OPEN state.

It is possible to change the LED short detection voltage, please input (0.3V～3.0V) to LSP pin.

The relationship between LED short detection voltage 「$VLED_{short}$」, and LSP pin voltage 「V_{LSP}」 as below equation.

$$V_{LSP}\,[V] = \frac{VLED_{short}\,[V]}{10}$$



In addition, because LSP pin has split 3V of terminal resistance inside IC.（Refer to upper right schematic）, it will be combined resistance value of IC's internal resistance and connecting to external resistor.For this reason, when configure the voltage of LSP in resistor divider, it is recommended to connect a resistor which has a little impact from internal resistance value.（Resistance is less susceptible to internal resistor, but care must be taken because power consumption will become large.）

○LSP setting procedure

Below equation shows how to calculate the detection voltage of VLSP by using R1,R2 resistor divide which connect to REG50 voltage.

$$VLSP = \left(REG50[V] \times \frac{R2[k\Omega]}{(R1[k\Omega] + R2[k\Omega]} \right) \times 10 \quad [V] \cdots (1)$$

However, this equation is without considering IC resistance. If internal resistance is taken into account, the detection voltage VLSP will be given by the following equation:

$$VLSP = \left(\frac{R2[k\Omega] \times R4[k\Omega] \times (REG50[V] \times R3 + REF[V] \times R1[k\Omega])}{(R1[k\Omega] \times R3[k\Omega] \times (R2 + R4) + R2[k\Omega] \times R4[k\Omega] \times (R1[k\Omega] + R3[k\Omega])} \right) \times 10 \quad [V] \ldots (2)$$

Please set R1 and R2 resistance so that a difference between resistance values found by Equations (1) and (2) will come to approximately 2% or less as a reference.

【Setting example】

Assuming that LSP is approximated by Equation (1) in order to set LSP detection voltage to 5V, R1 comes to 45kΩ and R2 comes to 5kΩ.

When calculating LSP detection voltage taking into account internal IC resistance by Equation (2), it will be given as:

$$VLSP = \left(\frac{5[k\Omega] \times 900[k\Omega] \times (5[V] \times 2100 + 3[V] \times 45[k\Omega])}{(45[k\Omega] \times 2100[k\Omega] \times (5 + 900) + 5[k\Omega] \times 900[k\Omega] \times (45[k\Omega] + 2100[k\Omega])} \right) \times 10 = 5.028V[V]$$

The difference is given as:

$$(5.028[V] - 5[V]) / 5[V] \times 100 = 0.56\%$$

As a result, this setting will be little affected by internal impedance.

□**For the selection of DC/DC components, please also consider the inaccuracy of each componentts**.

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●**Timer latch time (CP Pin)**

The CP pin will source 2.0uA current when any abnormal problem is detected.Even is an error is detected, IC does not stop as long as CP pin is not to 2.5V.CP pin which sets the time from detection of abnormality until shutdown (Timer latch). CP charge time「T_{CP}」 is set by the following equation:

$$C_{CP}\,[F] = \frac{T_{CP}\,[\mathrm{sec}] \times 2.0 \times 10^{-6}\,[A]}{2.5\,[V]}$$

●**FAIL Signal**

FAIL pin will change to Low when UVLO and latch occurred after CP charged.Please make sure that there is no logic problem in module design.The breakdown voltage of this pin is 36V.

state	FAIL output
Normal, STB=Low, （Under Abnormal detection）	OPEN
Abnormality detected(shutdown), UVLO detected	GND Level (50 ohm typ.)

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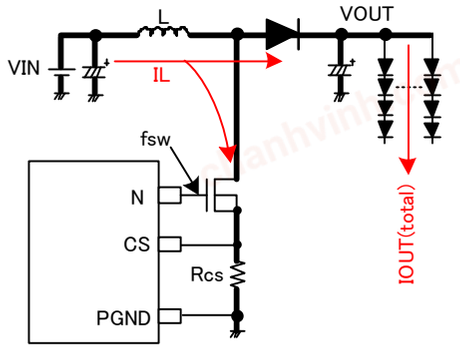
●OCP setting / DCDC component current tolerance selection guide

The OCP detection function that is one of the functions of the CS pin will stop the DC/DC converter operating ifthe CS pin voltage becomes larger than 0.4V.Consequently, it is needed to calculate a peak current flowing through the coil L and then review the resistance of RCS.Furthermore, a current tolerance for DC/DC components should be larger than that for peak current flowing through the coil L.The following describes the peak coil current calculation procedure, CS pin connection resistor RCS selection procedure, and DC/DC component current tolerance selection procedure .

○Peak coil current Ipeak calculation

Ripple voltage generated at the CS pin is determined by conditions for DC/DC application components first, Assuming the conditions as below:

「output voltage=VOUT[V] 」
「LED total current=IOUT[A] 」
「DCDC input voltage=VIN[V] 」
「DCDC efficiency=η[%] 」



And then mean input current IIN required for the whole system is given by the following equation.

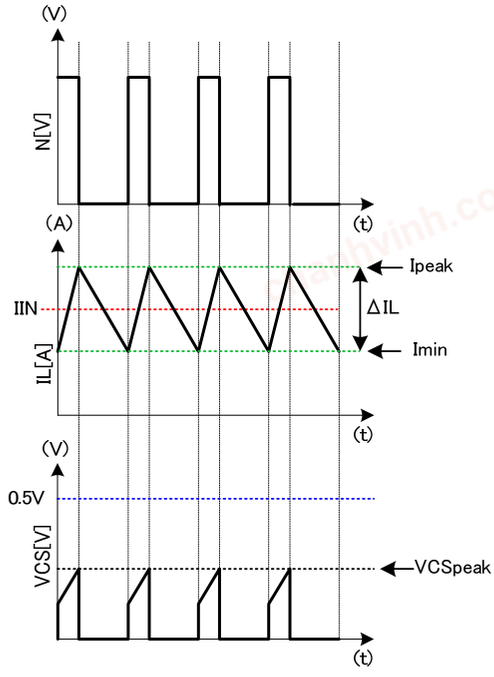
$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

Further, according to drive operation with the DC/DC converter switching frequency fsw [Hz], inductor ripple current ΔIL [A] generated at the inductor L (or H) is given by the following equation.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

As a result, the peak current Ipeak of IL is given by the following equation.

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A] \cdots (1)}$$



○CS pin connection resistor RCS selection procedure

The current Ipeak flows into RCS to generate voltage.（See the timing chart shown to the right）The voltage VCSpeak is given by the following equation.

$$VCS_{peak} = Rcs \times Ipeak \quad [V]$$

If VCSpeak voltage reaches 0.4V, DC/DC output will stop.Consequently, to select RCS resistance, the following condition should be met.

$$\boxed{Rcs \times Ipeak[V] < 0.4[V]}$$

○DC/DC component current tolerance selection procedure

Iocp current needed for OCP detection voltage CS to reach 0.4V is given by the following equation:

$$I_{OCP} = \frac{0.4[V]}{Rcs[\Omega]} \quad [A] \cdots (2)$$

The relation among Ipeak current (Equation (1)), Iocp current (Equation (2)), and Maximum current tolerance for component should meet the following equation.

$$\boxed{I_{peak} < I_{OCP} < \text{MAX current tolerance}}$$

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DC/DC application components including FETs, inductors, and diodes should be selected so that the Equation shown above will be met.

In addition, it is recommended to use continuous mode in DCDC application.And the lower limit value of coil ripples current Imin so as to meet the following equation:

$$I\min = I_{IN}[A] - \frac{\Delta IL[A]}{2}[A] > 0$$

A failure to meet this condition is referred to as discontinuous mode and this failure may result in an inadequate rise in output voltage.

【Setting example】

Output=VOUT[V]=40V
LED 1ch current=120mA, total LED current IOUT[A]=120mA×8ch=0.96A
DCDC input voltage=VIN [V] =24V
DCDC efficiency=η[%]=90%

Mean input current IIN required for the whole system is given by the following equation:

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} = \frac{40[V] \times 0.96[A]}{24[V] \times 0.9} = 1.78 \quad [A]$$

DCDC switching frequency=fsw[Hz]=200kHz
Inductor [H]=33μH

The inductor ripple current ΔIL [A] is given by the following equation:

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} = \frac{(40[V] - 24[V]) \times 24[V]}{33 \times 10^{-6}[H] \times 40[V] \times 200 \times 10^{3}[Hz]} = 1.45 \quad [A]$$

As a result, the peak current Ipeak of IL is given by the following equation.

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] = 1.78[A] + \frac{1.45[A]}{2} = 2.51[A]}$$

When RCS resistance is set to 0.1ohm, the VCS peak voltage will be given by the following equation:

$$\boxed{VCS_{peak} = Rcs \times Ipeak = 0.1[\Omega] \times 2.51[A] = 0.251[V] < 0.4[V]}$$

Consequently, the result meets the condition.

Furthermore, I_{OCP} current at which OCP is detected is given by the following equation:

$$I_{OCP} = \frac{0.4[V]}{0.1[\Omega]} = 4.0 \quad [A]$$

So must select the component of about 5A in order to meet the above result.

$$I_{peak} < I_{OCP} < \qquad = 2.51[A] < 4.0[A] < 5.0[A]$$

Particularly, To select DC/DC components, give consideration to IC variations as well as individual component variations, and then conduct thorough verification on practical systems..

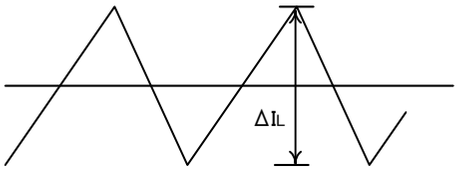
The lower limit value of coil ripple current Imin is given by the following equation, the component will not be put into discontinuous mode.

$$I\min = I_{IN}[A] - \frac{\Delta IL[A]}{2}[A] = 1.78[A] - 0.73[A] = 1.05[A] > 0$$

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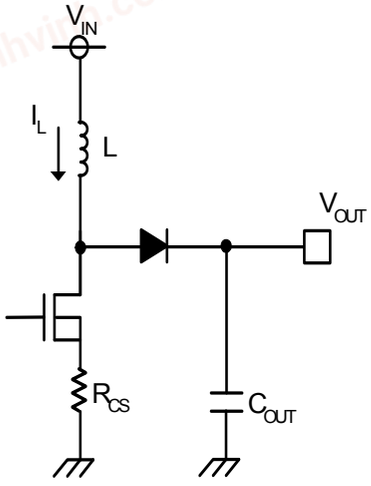
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●Selection of inductor L



The value of inductor has significant influence on the input ripple current. As shown by Equation (1), the larger the inductor and the higher the switching frequency, the inductor ripple current ΔIL becomes increasingly lower.

$$\Delta IL = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{L \times V_{OUT} \times f_{SW}} [A] \quad \cdots\cdots \quad (1)$$



Expressing efficiency as shown by Equation (2), peak input current is given as Equation (3).

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \quad \cdots\cdots \quad (2)$$

$$IL_{MAX} = I_{IN} + \frac{\Delta IL}{2} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{\Delta IL}{2} \quad \cdots\cdots \quad (3)$$

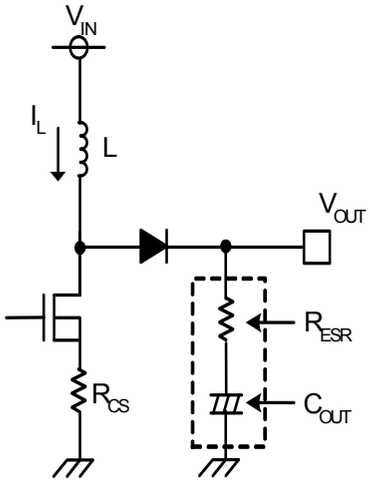
Here,

L: Inductor value[H] V_{OUT}: DC/DC output voltage[V]
V_{IN}: input voltage[V] I_{OUT}: output total current[A]
I_{IN}: input current[A] F_{SW}: Oscillation frequency[Hz]

Basically, make setting of ΔIL to approximately 30% to 50% of the output load current.

※ If a current in excess of the rated current of the inductor applies to the coil, the inductor will cause magnetic saturation, resulting in efficiency degradation.
Select an inductor with an adequate margin so that peak current will not exceed the rated current of the inductor.
※ To reduce power dissipation from and increase efficiency of inductor, select an inductor with low resistance component (DCR or ACR).

●Selection of output capacitor C_{OUT}



Select a capacitor on the output side taking into account the stability region of output voltage and equivalent series resistance necessary to smooth ripple voltage. Note that higher output ripple voltage may result in a drop in LED pin voltage, making it impossible to supply set LED current.
The output ripple voltage ΔV_{OUT} is given by Equation (4).

$$\Delta V_{OUT} = ILMAX \times R_{ESR} + \frac{1}{C_{OUT}} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f_{SW}} [V] \quad \cdots\cdots \quad (4)$$

Here, R_{ESR} = Equivalent series resistance of C_{OUT}.

※ Select capacitor ratings with an adequate margin for output voltage.
※ To use an electrolytic capacitor, an adequate margin should be provided for permissible current. Particularly to apply PWM light modulation to LED, note that a current higher than the set LED current transiently flows.

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●Selection of switching MOSFET transistors

There will be no problem for switching MOSFET transistors having absolute maximum rating higher than rated current of the inductor L and VF higher than "C_{OUT} breakdown voltage + Rectifier diode". However, to achieve high-speed switching, select transistors with small gate capacity (injected charge amount).

Note: Rated current larger than overcurrent protection setting current is recommended.
Note: Selecting transistors with low on resistance can obtain high efficiency.

●Selection of rectifier diodes

Select Schottky barrier diodes having current capability higher than the rated current of the inductor L and inverse breakdown voltage higher that C_{OUT} breakdown voltage, particularly having low forward voltage VF.

●Selection of Load switch MOSFET and soft start function

In usual DC/DC converter, because there is no switching to a path leading from V_{IN} to V_{OUT} resulting in output voltage is also occur even if IC is in OFF state.Please insert PMOSFET between V_{IN} and inductor if you want voltage to 0V until the IC starts to operate.In addition, FAIL pin can be used for driving load switch after confirmed the logic theory, and the breakdown voltage of drain-source needed to be selected larger than V_{IN}.

Furthermore, if you would like to make soft start function to load switch, please insert a condenser between Gate and Source.

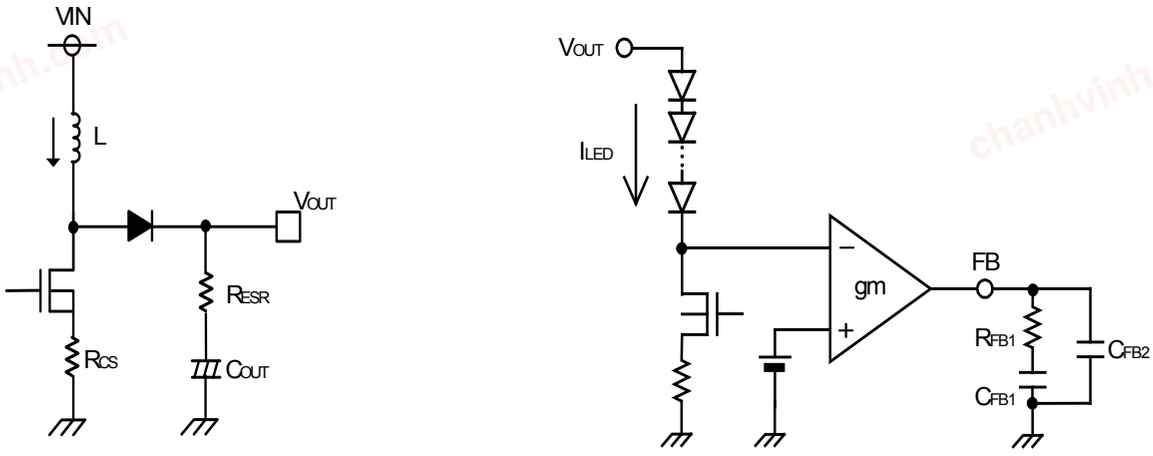
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●Phase Compensation Setting Procedure

DC/DC converter application for current mode control includes one each of pole f_p (phase delay) by CR filer consisting of output capacitor and output resistor (i.e., LED current) and zero (phase lead) f_Z by the output capacitor and capacitor ESR.

Furthermore, the step-up DC/DC converter includes RHP zero "f_{ZRHP}" as the second zero. Since the RHP zero has phase delay (−90°) characteristics like the pole, the crossover frequency f_c should be set to not more than RHP zero.



i. Find Pole f_p and RHP zero f_{ZRHP} of DC/DC converter.

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} [Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} [Hz]$$

Here, I_{LED} =LED Total current[A], $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$

ii. Find phase compensation to be inserted to error amplifier.(set f_c is 1/5 to f_{ZRHP})

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} [\Omega] \qquad C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_p} [F]$$

Here, $gm = 4.0 \times 10^{-4} [S]$

iii. Find zero used to compensate ESR (R_{ESR}) of C_{OUT} (electrolytic capacitor).

$$C_{FB2} = \frac{R_{ESR} \times C_{OUT}}{R_{FB1}} [F]$$

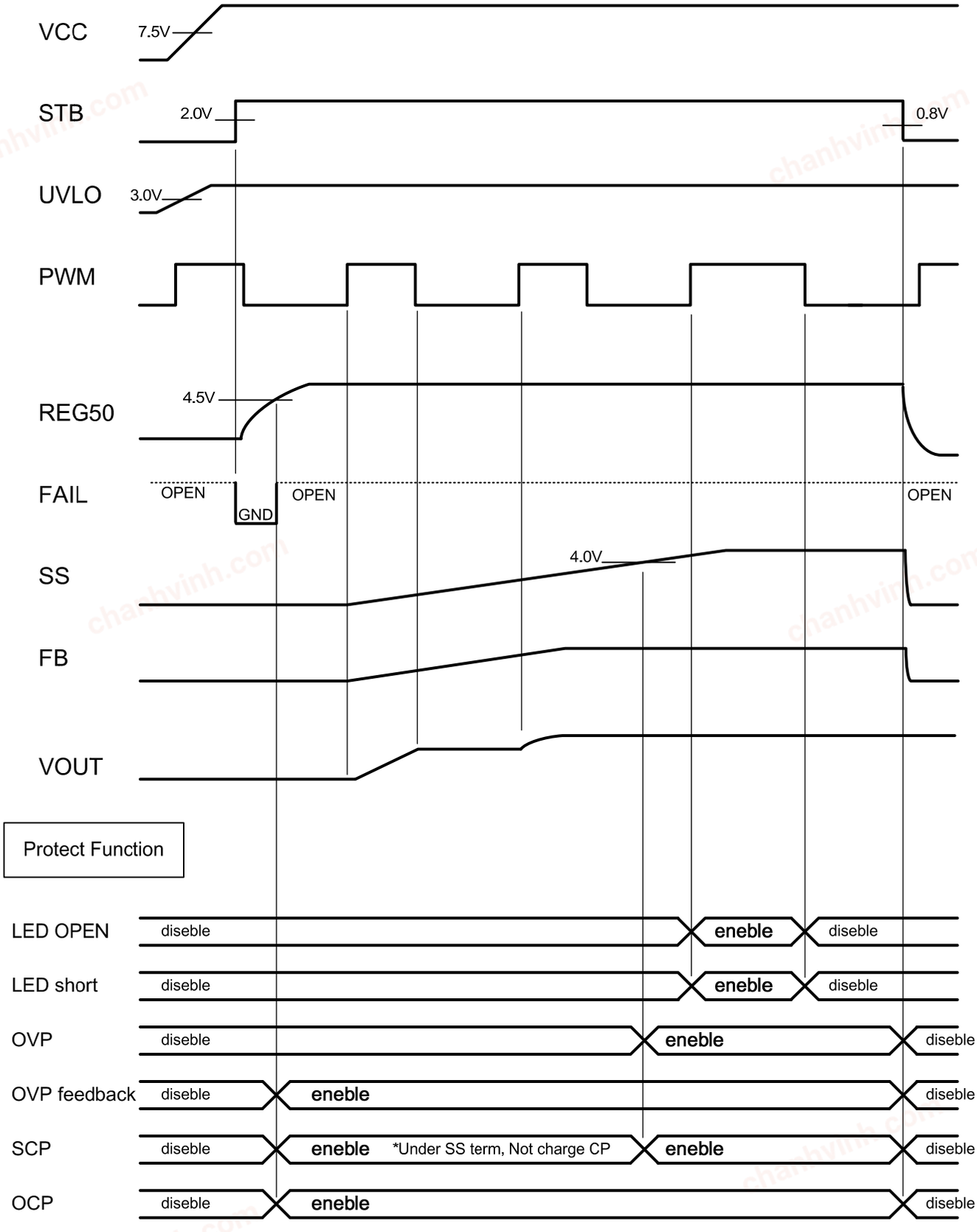
□Even if a ceramic capacitor (R_{ESR} of the order of milliohms) for C_{OUT}, it is recommended to insert C_{FB2} for stable operation.

To improve transient response, it is necessary to increase R_{FB1} and reduce C_{FB1}. However, this improvement reduces a phase margin. To avoid this problem, conduct thorough verification, including variations in external components, on practical systems.

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●Timing Chart



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●List of Protect Function (typ condition)

Protection Name	Detection Pin	Detect Condition			Release Condition	Protect type
		Detection Pin Condition	PWM	SS		
LED OPEN	BSx	BSx < 0.1V	H	SS > 4V	BSx > 0.1V	Latch
	CLx	CLx < 0.1V	H	SS > 4V	CLx > 0.1V	Latch
LED SHORT	BSx	BSx > 9V	H	SS > 4V	BSx < 9V	Latch
UVLO	UVLO	UVLO < 2.79V	-	-	UVLO > 3V	Auto-restart
	REG50	REG50 < 4.2V	-	-	REG50 > 4.5V	Auto-restart
	VCC	VCC < 7.2V	-	-	VCC > 7.5V	Auto-Restart
OVP	OVP	OVP > 2.25V	-	SS > 4V	OVP < 2.25V	Latch
OVP Feedback	OVP	OVP > 2.5V	H	-	OVP < 2.5V	Pulse-by-pulse
SCP	OVP	OVP < 0.2V	-	-	OVP > 0.2V	Latch (Pulse-by-pulse and gate is OFF)
OCP	CS	CS > 0.4V	-	-	CS < 0.4V	N output stops (200ns Mask from Gate ON)

To release the latch function, STB should be set to “L” once, and then to “H”.
(CP does not charged under Soft start duration.)
*When abnormality is detected under PWM=H, CP will continue to charge even if PWM=L.

To release the latch function, STB should be set from “L” to “H”.(CP does not charged under Soft start duration.)

Protect Function	Operation after protect function detects error			
	DC/DC	LED Driver	Soft Start	FAIL Pin
STB	Instantaneously stops	Instantaneously stops	Instantaneously discharged	OPEN
LED Open	Stops operating after CP charged	Stops operating after CP charged	Discharge after CP discharged	GND after CP charged
LED short	Stops operating after CP charged	Stops operating after CP charged	Discharge after CP discharged	GND after CP charged
UVLO	Instantaneously stops	Instantaneously stops	Instantaneously discharged	GND
OVP	Stops operating after CP charged	Stops operating after CP charged	Discharge after CP discharged	GND after CP charged
SCP	N output stops	Stops operating after CP charged	Discharge after CP discharged	GND after CP charged
OCP	N pin limits duty cycle	Normal operation	Normal operation	OPEN

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●Operational Notes

1) We pay utmost attention to the quality control of this product. However, if it exceeds the absolute maximum ratings including applied voltage and operating temperature range, it may lead to its deterioration or breakdown. Further, this makes it impossible to assume a breakdown state such as short or open circuit mode. If any special mode to exceed the absolute maximum ratings is assumed, consider adding physical safety measures such as fuses.
2) Making a reverse connection of the power supply connector can cause the IC to break down. To protect the IC form breakdown due to reverse connection, take preventive measures such as inserting a diode between the external power supply and the power supply pin of the IC.
3) Since current regenerated by back electromotive force flows back, take preventive measures such as inserting a capacitor between the power supply and the ground as a path of the regenerative current and fully ensure that capacitance presents no problems with characteristics such as lack of capacitance of electrolytic capacitors causes at low temperatures, and then determine the power supply line. Provide thermal design having an adequate margin in consideration of power dissipation (Pd) in the practical operating conditions.
4) The potential of the GND pin should be maintained at the minimum level in any operating state.
5) Provide thermal design having an adequate margin in consideration of power dissipation (Pd) in the practical operating conditions.
6) To mount the IC on a printed circuit board, pay utmost attention to the direction and displacement of the IC. Furthermore, the IC may get damaged if it is mounted in an erroneous manner or if a short circuit is established due to foreign matters entered between output pins or between output pin and power supply GND pin.
7) Note that using this IC in strong magnetic field may cause it to malfunction.
8) This IC has a built-in thermal-protection circuit (TSD circuit), which is designed to be activated if the IC junction temperature reached 150°C to 200°C and deactivated with hysteresis of 10°C or more. The thermal-protection circuit (TSD circuit) is a circuit absolutely intended to protect the IC from thermal runaway, not intended to protect or guarantee the IC. Consequently, do not use the IC based on the activation of this TSD circuit for subsequent continuous use and operation of the IC.
9) When testing the IC on a set board with a capacitor connected to the pin, the IC can be subjected to stress. In this case, be sure to discharge the capacitor for each process. In addition, to connect the IC to a jig up to the testing process, be sure to turn OFF the power supply prior to connection, and disconnect the jig only after turning OFF the power supply.
10) This monolithic IC contains P + Isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersections of these P layers and the N layers of other elements, thus making up different types of parasitic elements.
For example, if a resistor and a transistor is connected with pins respectively as shown in Fig.
○When GND>(Pin A) for the resistor, or when GND>(Pin B) for the transistor (NPN), P-N junctions operate as a parasitic diode.
○When GND>(Pin B) for the transistor (NPN), the parasitic NPN transistor operates by the N layer of other element adjacent to the parasitic diode aforementioned.
Due to the structure of the IC, parasitic elements are inevitably formed depending on the relationships of potential. The operation of parasitic diodes can result in interferences in circuit operation, leading to malfunctions and eventually breakdown of the IC. Consequently, pay utmost attention not to use the IC for any applications by which the parasitic elements are operated, such as applying a voltage lower than that of GND (P substrate) to the input pin.

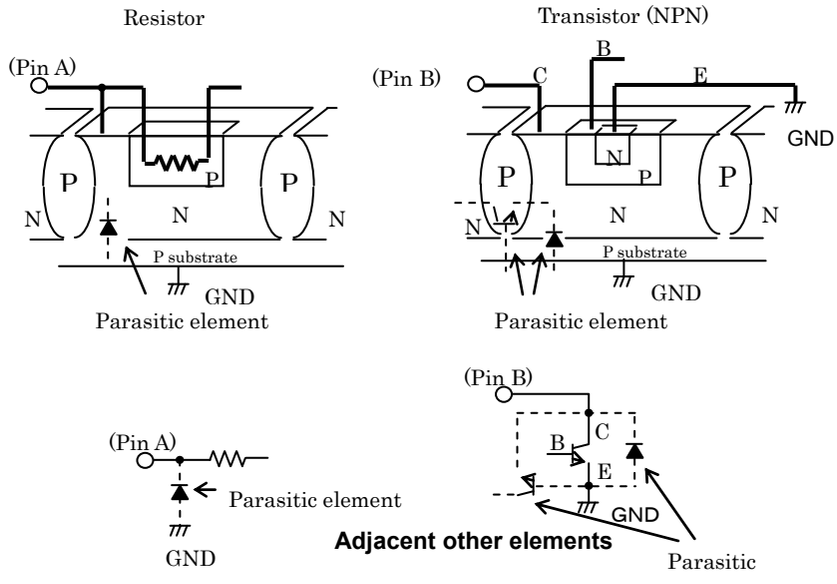


Figure 13. Example of Simple Structure of Monolithic IC

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

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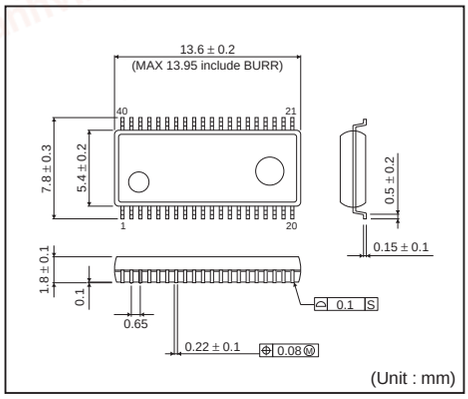
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●Ordering Information

B D 9 4 7 9 F V	-	XX
Part Number	Package FV:SSOP	Packaging and forming specification XX: Please confirm the formal name to our sales.

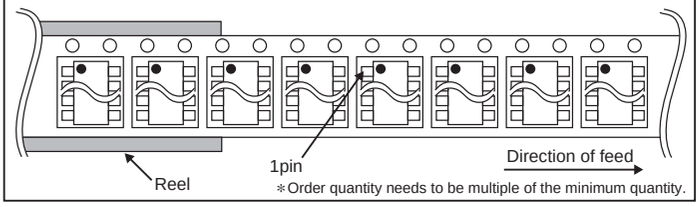
●Physical Dimension Tape and Reel Information

SSOP-B40



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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