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Datasheet

100 V VB 3.5 A/4.5 A Peak Current

High Frequency High-Side and Low-Side Driver

BD2320EFJ-LA BD2320UEFJ-LA

General Description

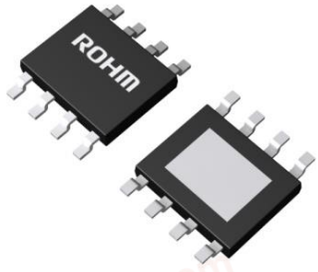
This is the product guarantees long time support in industrial market.

BD2320EFJ-LA and BD2320UEFJ-LA are the 100 V maximum voltage High-Side and Low-Side gate drivers which can drive external Nch-FET using the bootstrap method. The driver includes a 100 V bootstrap diode and independent inputs control for High-Side and Low-Side. 3.3 V and 5.0 V are available for interface voltage. Under Voltage Lockout circuits are built in for High-Side and Low-Side.

Key Specification

- High-Side Supply Voltage and Floating Voltage: 100 V
- Output Voltage Range: 7.5 V to 14.5 V
- Output Current Io+/Io-: 3.5 A/4.5 A
- Propagation Delay: 27 ns (Typ)
- Delay Matching: 12 ns (Max)
- Offset Voltage Pin Leak Current: 10 µA (Max)
- Operating Temperature Range: -40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
HTSOP-J8	4.9 mm x 6.0 mm x 1.0 mm



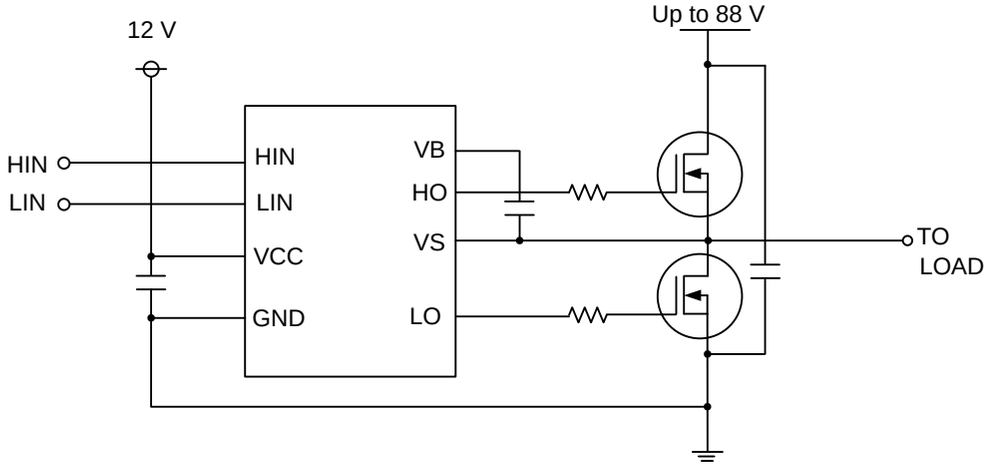
Features

- Long Time Support Product for Industrial Applications.
- Under Voltage Lockout (UVLO) for High-Side and Low-Side Driver
- 3.3 V and 5.0 V Interface Voltage
- Output In-phase with Input Signal

Applications

- Power Supplies for Telecom and Datacom.
- MOSFET Application
- Half-bridge and Full-bridge Converters
- Forward Converters

Typical Application Circuit

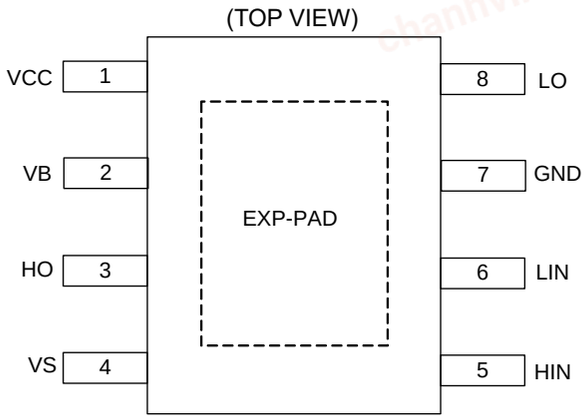


○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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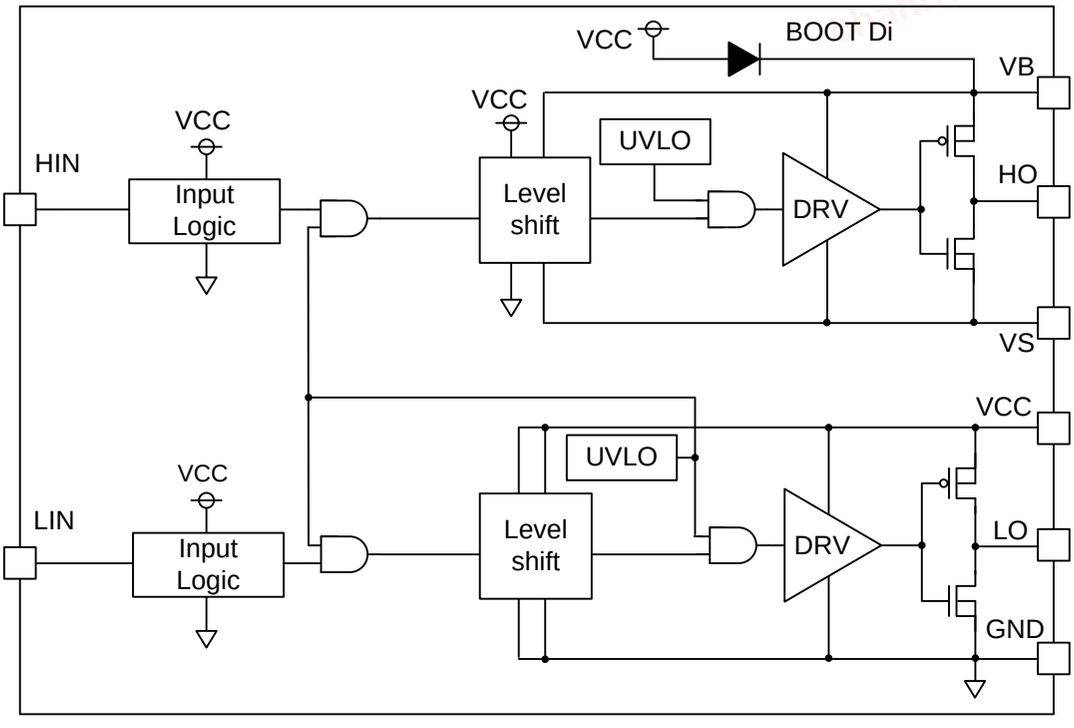
Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	VCC	Low-Side supply voltage
2	VB	High-Side supply voltage
3	HO	High-Side output
4	VS	High-Side return
5	HIN	Logic input for High-Side
6	LIN	Logic input for Low-Side
7	GND	Ground
8	LO	Low-Side output
-	EXP-PAD	Connect to GND

Block Diagram



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Absolute Maximum Rating (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VB - VS Voltage	V_{BS}	-0.3 to +15	V
Voltage on VB	V_{VB}	-0.3 to +100	V
Voltage on VS	V_{VS}	-15 to +100	V
Voltage on HO	V_{HO}	V_{VS}-0.3 to V_{VB}+0.3	V
V_{CC} Voltage	V_{CC}	-0.3 to +15	V
Voltage on LO	V_{LO}	-0.3 to V_{CC}+0.3	V
Voltage on HIN and LIN	V_{HIN}, V_{LIN}	-0.3 to V_{CC}+0.3	V
Voltage Slew Rate on VB, VS	SR	-50 to +50	V/ns
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
HTSOP-J8				
Junction to Ambient	θ_{JA}	206.4	45.2	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	21	13	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-40	+25	+125	°C
Voltage on VB	V_{VB}	-0.3	-	+95	V
Voltage on VS	V_{VS}	-7.0	-	+95	V
VB - VS Voltage	V_{BS}	7.0	-	14.5	V
Voltage on HIN LIN	V_{HIN}, V_{LIN}	0	-	V_{CC}	V
V_{CC} Voltage	V_{CC}	7.5	-	14.5	V

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Electrical Characteristics (Unless otherwise specified Ta = -40 °C to +125 °C, V_{CC} = 12.0 V, V_{BS} = 12.0 V, V_{VS} = V_{GND}, HO = open, LO = open)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current						
Offset supply Leakage Current	I_{LK}	-	0	10	µA	V_{VB} = V_{VS} = 100 V
Quiescent V_{BS} Supply Current	I_{QBS}	40	80	160	µA	V_{LIN} = V_{HIN} = 0 V
Operating V_{BS} Supply Current	I_{OBS}	2.75	5.50	11.00	mA	f = 500 kHz
Quiescent V_{CC} Supply Current	I_{QCC}	60	120	240	µA	V_{LIN} = V_{HIN} = 0 V
Operating V_{CC} Supply Current	I_{OCC}	3.00	6.00	12.00	mA	f = 500 kHz
UVLO						
V_{CC} UVLO Rising Threshold	V_{CCUVR}	4.6	6.0	7.4	V	
V_{CC} UVLO Falling Threshold	V_{CCUVF}	4.2	5.5	6.8	V	
V_{CC} UVLO Hysteresis	V_{CCUVH}	-	0.5	-	V	
V_{BS} UVLO Rising Threshold	V_{BSUVR}	4.1	5.4	6.7	V	
V_{BS} UVLO Falling Threshold	V_{BSUVF}	3.7	4.9	6.1	V	
V_{BS} UVLO Hysteresis	V_{BSUVH}	-	0.5	-	V	
Input						
Logic “1” Input Threshold Voltage	V_{IH}	1.50	2.15	2.80	V	
Logic “0” Input Threshold Voltage	V_{IL}	0.80	1.25	1.70	V	
Input Threshold Hysteresis	V_{INHYS}	0.3	0.9	-	V	
Input Pulldown Resistance	R_{IN}	50	100	150	kΩ	
Output						
High Level Output Voltage, V_{CC} - V_{LO}, V_{VB} - V_{HO}	V_{OH}	-	16	-	mV	V_{CC} = 12 V, V_{VB} = 12 V, V_{VS} = 0 V, Io = 10 mA
Low Level Output Voltage, V_{LO} - GND, V_{HO} - V_{VS}	V_{OL}	-	8	-	mV	V_{CC} = 12 V, V_{VB} = 12 V, V_{VS} = 0 V, Io = 10 mA
Output High Short Circuit Pulse Current*(Note 6)*	I_{O+}	-	3.5	-	A	V_{LO}, V_{HO} = 0 V
Output Low Short Circuit Pulse Current*(Note 6)*	I_{O-}	-	4.5	-	A	V_{LO}, V_{HO} = 12 V
Bootstrap Diode						
Bootstrap Diode Forward Voltage1	V_{F1}	0.26	0.53	1.16	V	I_{VCC-VB} = 100 µA
Bootstrap Diode Forward Voltage2	V_{F2}	0.95	1.90	3.80	V	I_{VCC-VB} = 100 mA
Bootstrap Diode Dynamic Resistance	R_D	5.0	10.0	20.0	Ω	I_{VCC-VB} = 80 mA, 100 mA

(Note 6) Not 100 % tested.

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Electrical Characteristics - continued
(Unless otherwise specified Ta = -40 °C to +125 °C, V_{CC} = 12.0 V, V_{BS} = 12.0 V, V_{VS} = V_{GND}, HO = open, LO = open)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
HO Turn-on Propagation Delay	t_{ONH}	10	27	50	ns	
LO Turn-on Propagation Delay	t_{ONL}	10	27	50		
HO Turn-off Propagation Delay	t_{OFFH}	10	29	50		
LO Turn-off Propagation Delay	t_{OFFL}	10	29	50		
HO Turn-on Rise Time	t_{RH}	-	8	-		HO = 1 nF
LO Turn-on Rise Time	t_{RL}	-	8	-		LO = 1 nF
HO Turn-off Fall Time	t_{FH}	-	6	-		HO = 1 nF
LO Turn-off Fall Time	t_{FL}	-	6	-		LO = 1 nF
Delay Matching, HS Turn-off, LS Turn-on	t_{M1}	-	2.0	12		
Delay Matching, HS Turn-on, LS Turn-off	t_{M2}	-	2.0	12		

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Typical Performance (Reference Data)

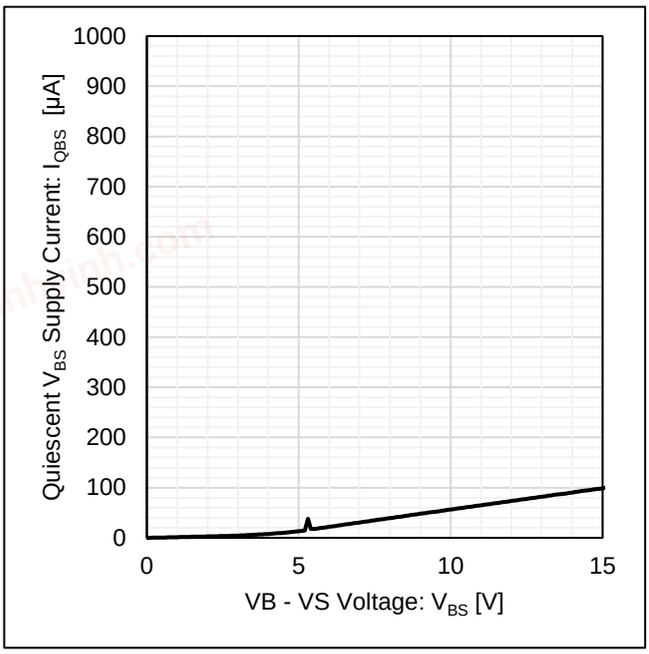


Figure 2. Quiescent V_{BS} Supply Current vs VB - VS Voltage

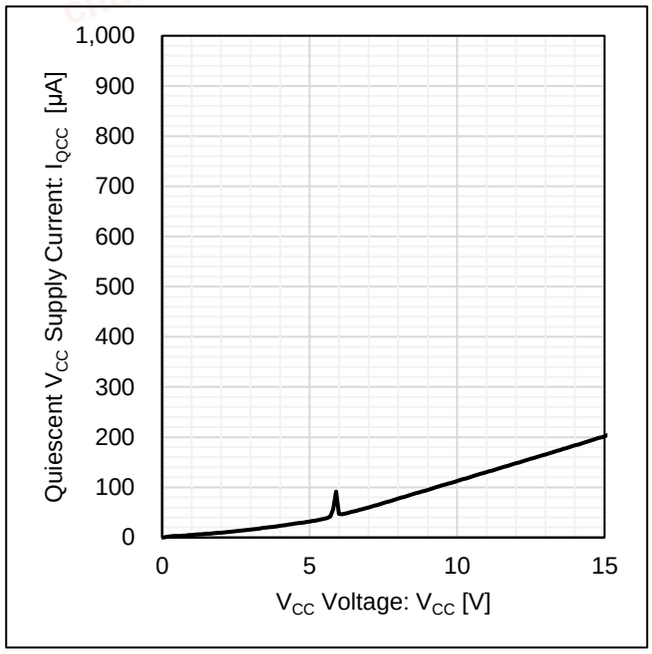


Figure 3. Quiescent V_{CC} Supply Current vs V_{CC} Voltage

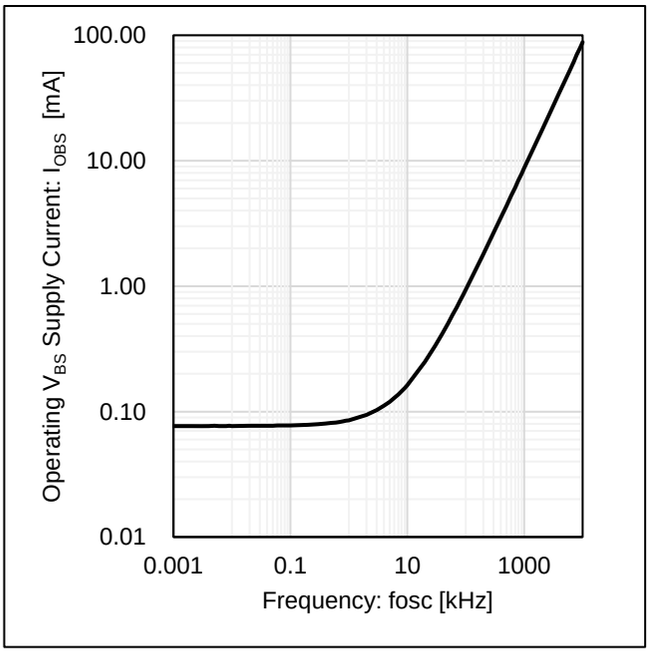


Figure 4. Operating V_{BS} Supply Current vs Frequency

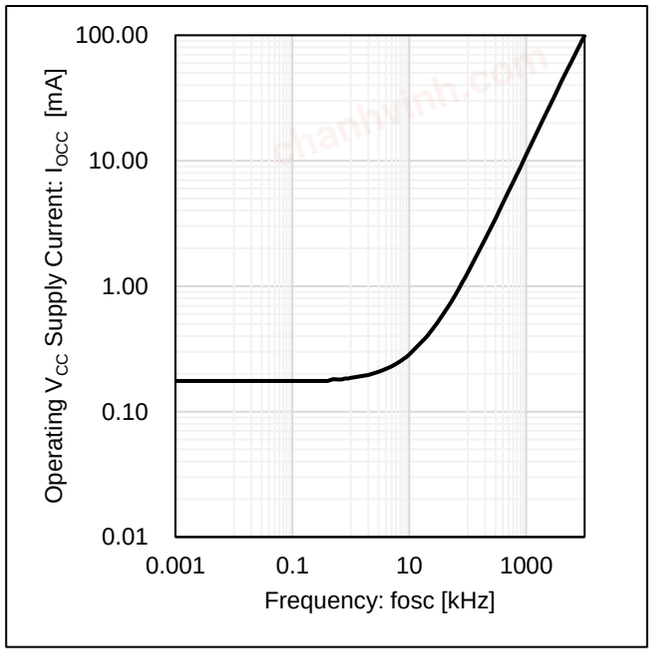


Figure 5. Operating V_{CC} Supply Current vs Frequency

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Typical Performance (Reference Data) -continued

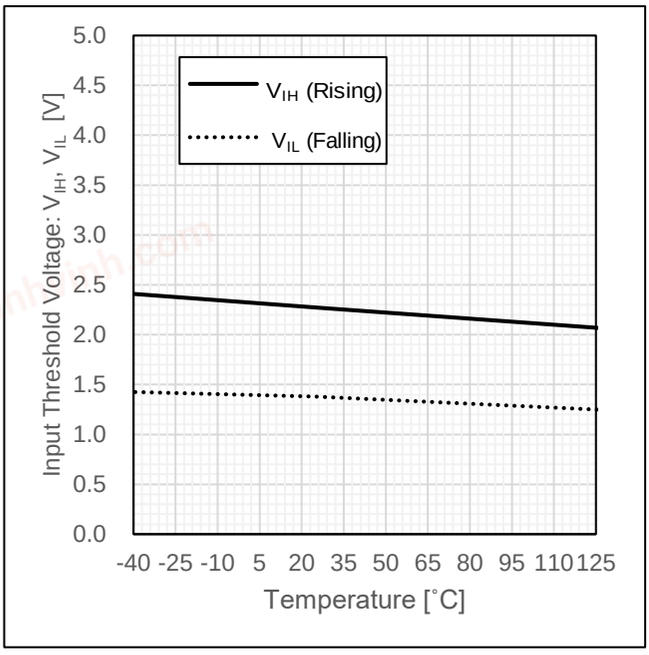


Figure 6. Input Threshold Voltage vs Temperature

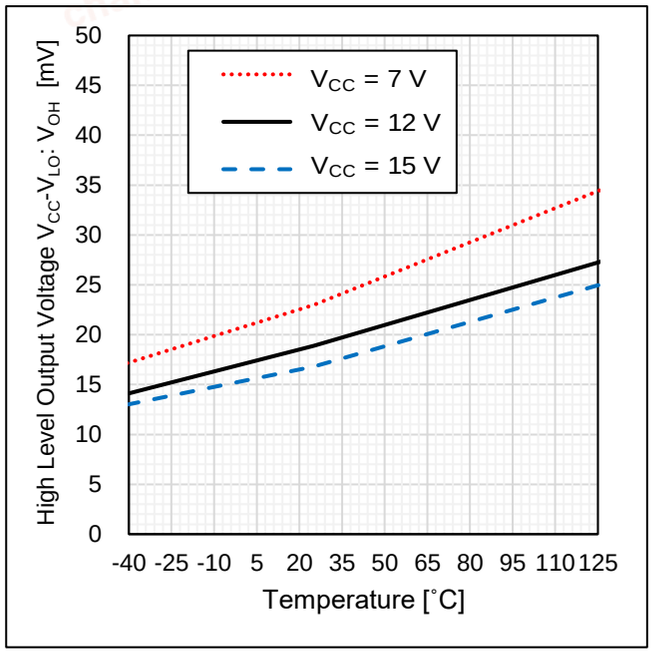


Figure 7. High Level Output Voltage V_{CC} - V_{LO} vs Temperature

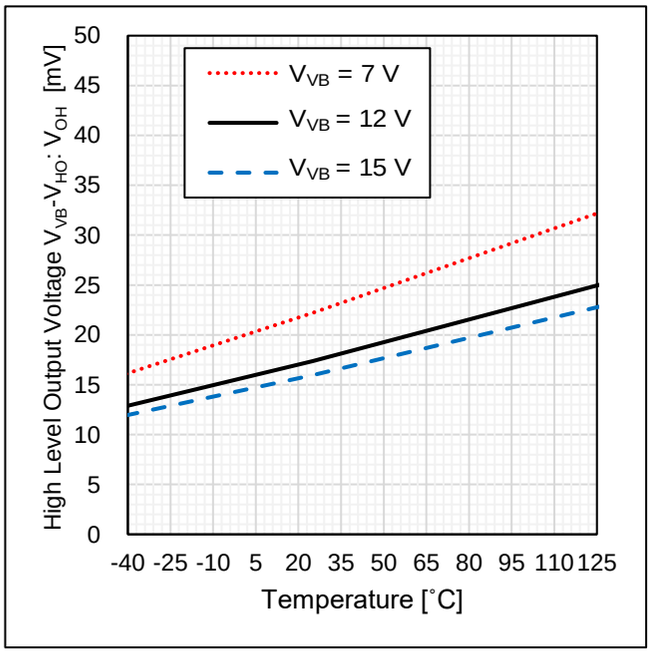


Figure 8. High Level Output Voltage V_{VB} - V_{HO} vs Temperature

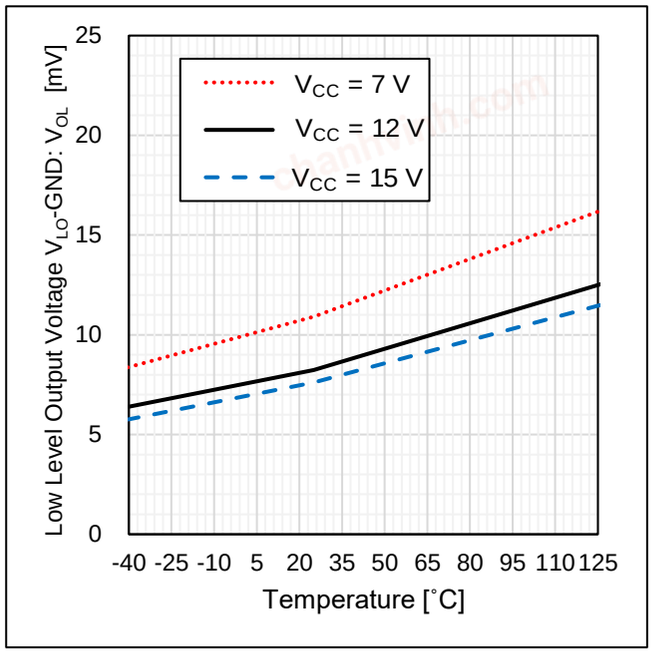


Figure 9. Low Level Output Voltage V_{LO} - GND vs Temperature

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Typical Performance (Reference Data) -continued

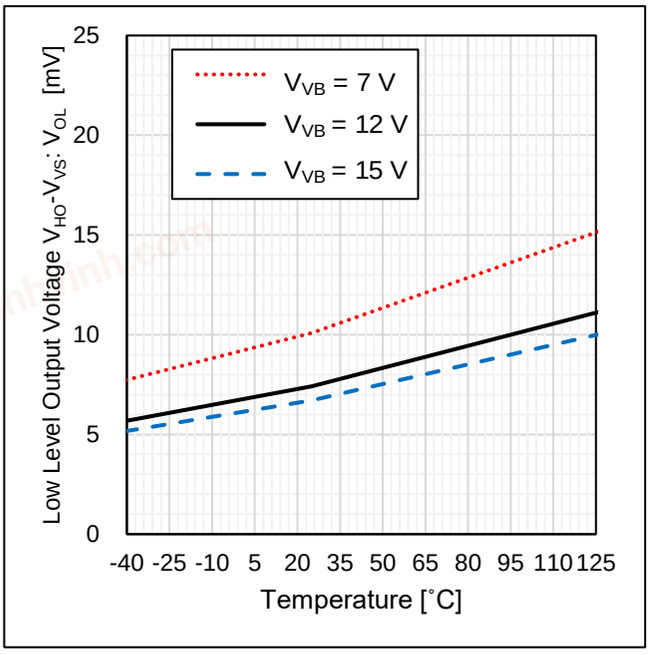


Figure 10. Low Level Output Voltage V_{HO} - V_{VS} vs Temperature

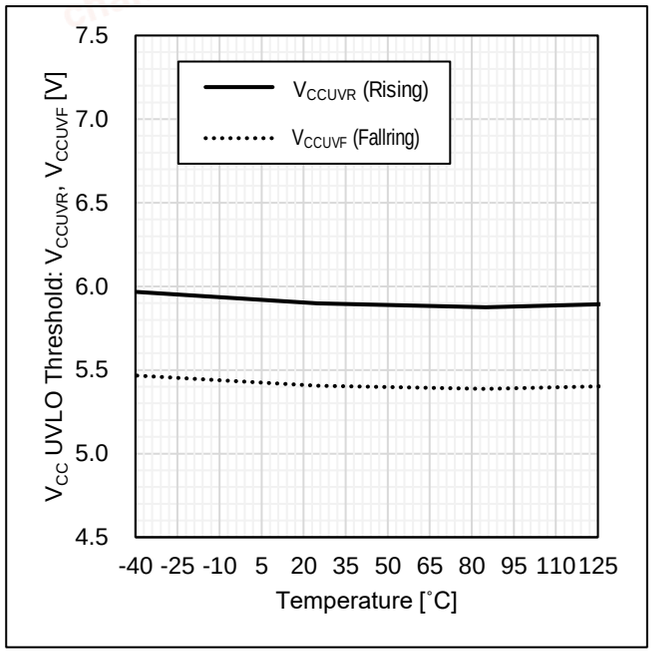


Figure 11. V_{CC} UVLO Threshold vs Temperature

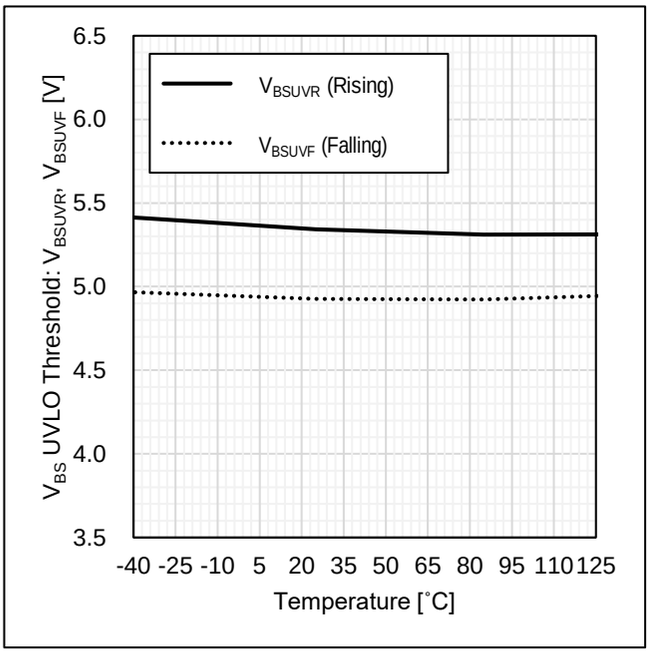


Figure 12. V_{BS} UVLO Threshold vs Temperature

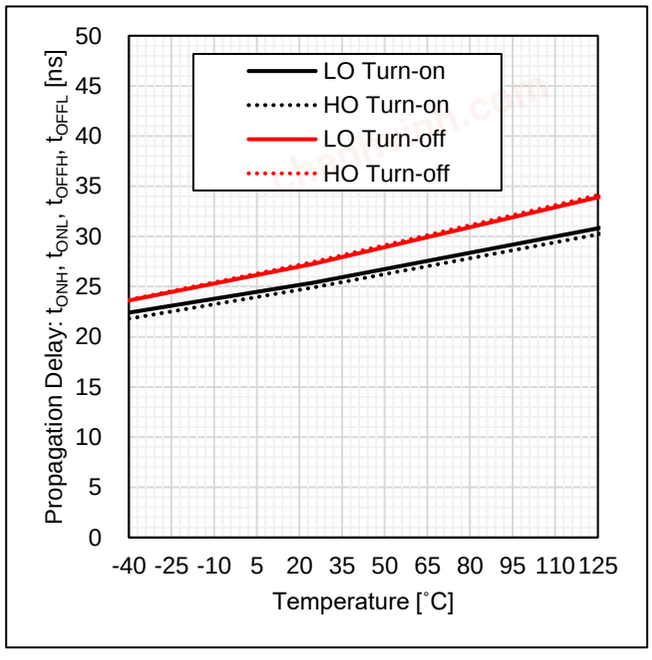


Figure 13. Propagation Delay vs Temperature

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Typical Performance (Reference Data) -continued

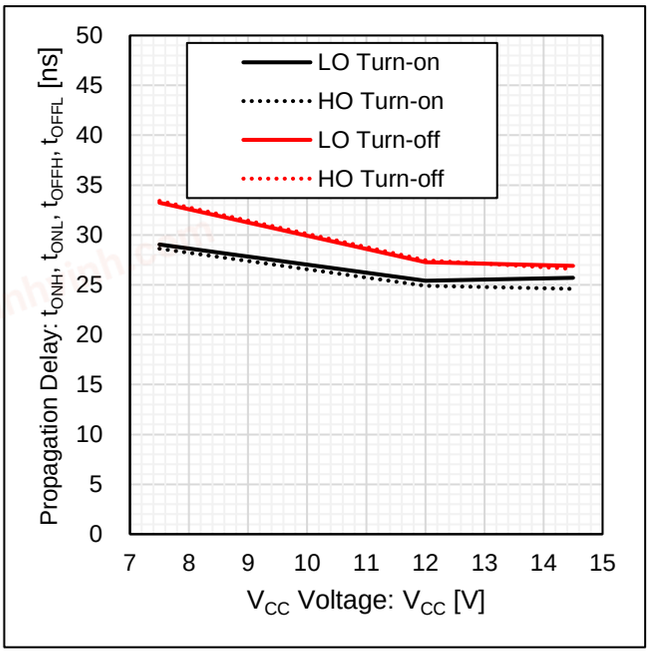


Figure 14. Propagation Delay vs V_{CC} Voltage

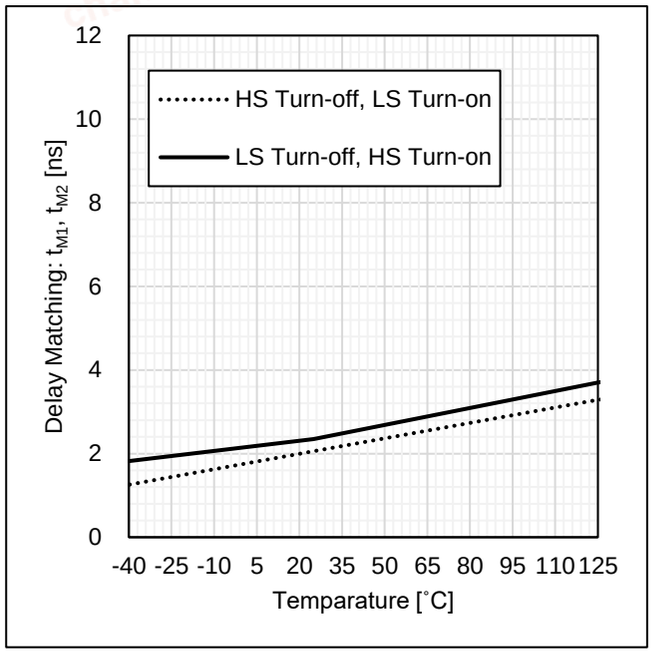


Figure 15. Delay Matching vs Temperature

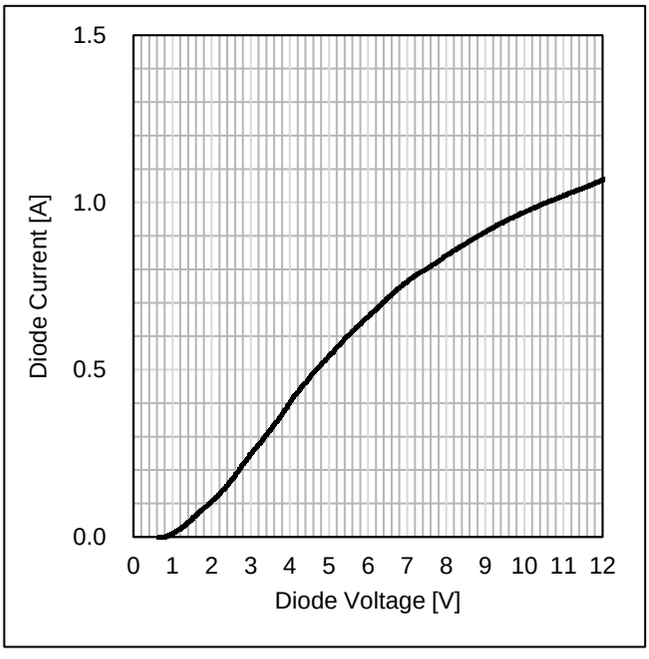


Figure 16. Diode Current vs Diode Voltage

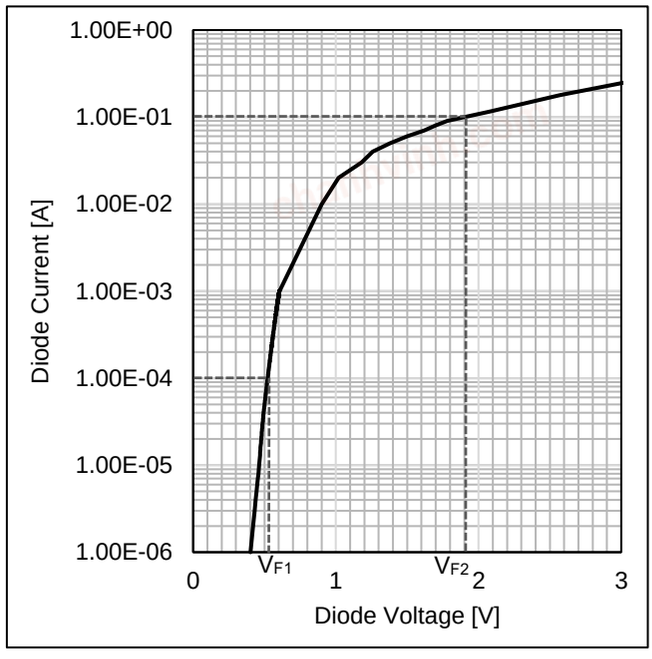
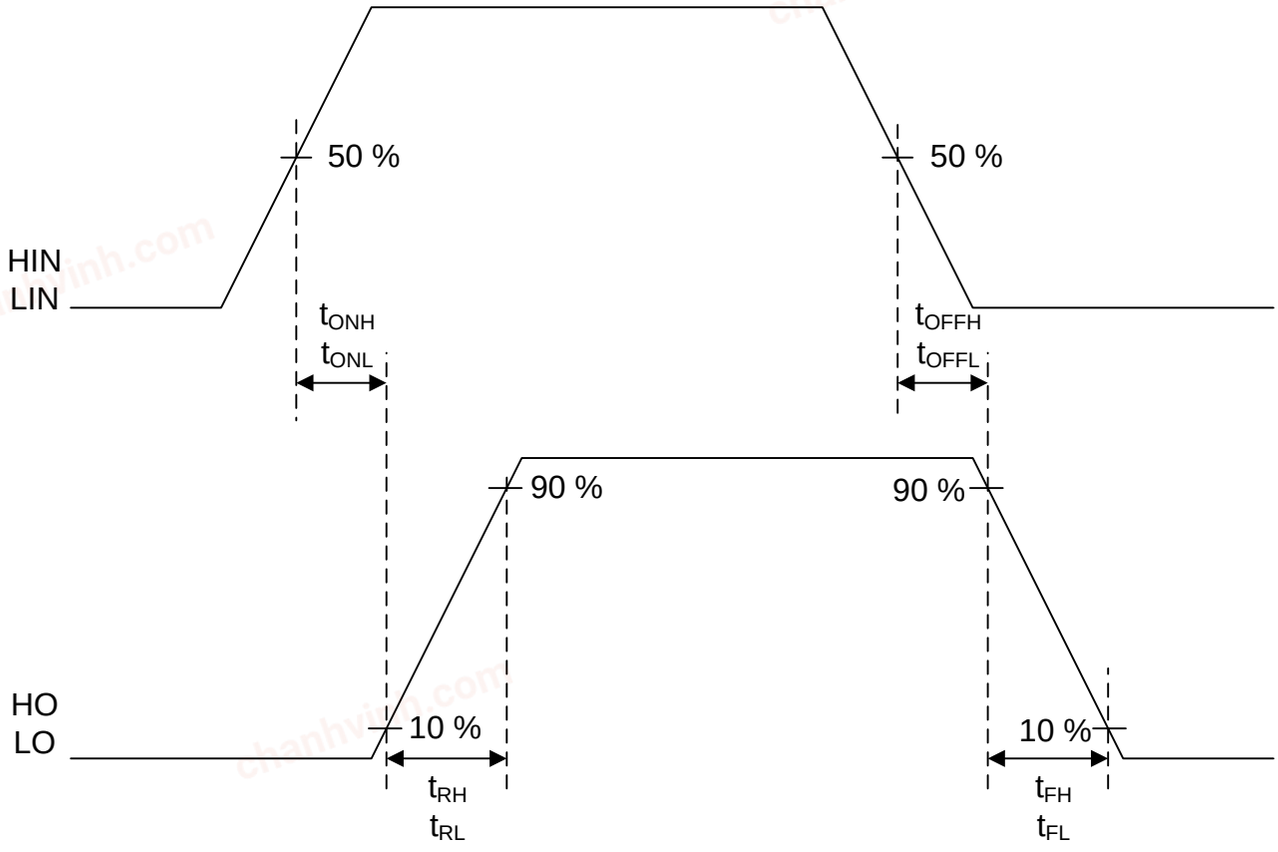


Figure 17. Diode Current vs Diode Voltage (V_{F1}, V_{F2})

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Timing Chart



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Selection of Components Externally Connected

1. Gate Resistor

The gate resistor $R_{G(ON)}$, $R_{G(OFF)}$ can be selected to control the switching speed of the external FET. The turn on time (t_{SW}) is decided by the gate resistor, gate-to-source charge (Q_{GS}) and gate-to-drain charge (Q_{GD}) of the external FET. In mean current flowing to a gate of the external FET is calculated as follows.

$$I_G = \frac{Q_{GS}+Q_{GD}}{t_{SW}} \quad (1)$$

The turn on gate resistor is calculated as follows.

$$R_{TOTAL(ON)} = R_{ONP} + R_{G(ON)} = \frac{V_{CC}-V_{GS}}{I_G} \quad (2)$$

The turn on time is calculated as follows.

$$t_{SW} = \frac{Q_{GS}+Q_{GD}}{I_G} = \frac{(Q_{GS}+Q_{GD})(R_{ONP}+R_{G(ON)})}{(V_{BS}-V_{GS(th)})} \quad (3)$$

The switching slew rate of the external FET (dVs/dt) also can be controlled by the gate resistor. The switching slew rate of the external FET (dVs/dt) is calculated as follows.

$$\frac{\mathrm{dVs}}{dt} = \frac{I_G}{C_{RSS}} \quad (4)$$

where:

C_{RSS} is the feedback capacitance.

Substituting equation (4) into equation (2) yields the following formulas.

$$R_{TOTAL(ON)} = R_{ONP} + R_{G(ON)} = \frac{V_{BS}-V_{GS(th)}}{C_{RSS}\frac{dVs}{dt}} \quad (5)$$

$$R_{G(ON)} = \frac{V_{BS}-V_{GS(th)}}{C_{RSS}\frac{dVs}{dt}} - R_{ONP} \quad (6)$$

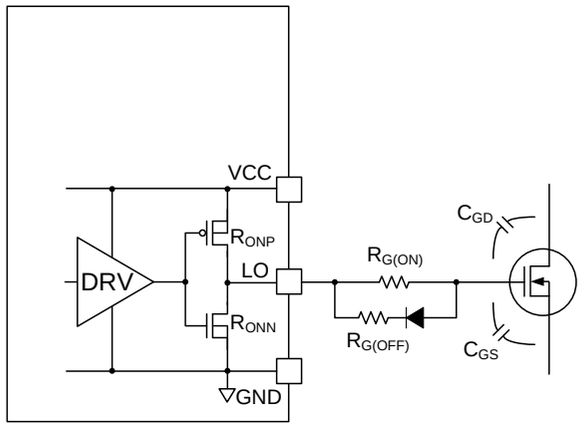


Figure 18. Gate Driver Equivalent Circuit

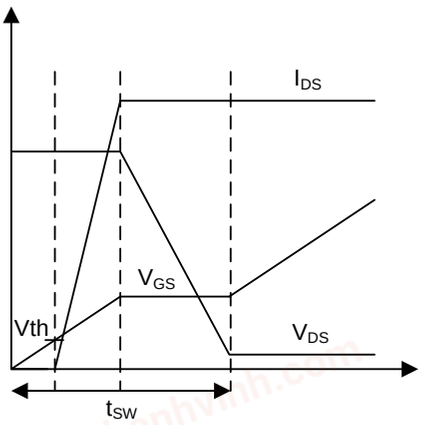


Figure 19. Gate Charge Transfer Characteristics

When the gate driver output turns off, current flows to gate resistor through C_{GD} of the external FET. To prevent that the gate voltage of the external FET becomes higher than the threshold voltage and the external FET self-turn-on, please set up the turn off resistor ($R_{G(OFF)}$) that satisfies the following formulas.

$$V_{GS(th)} \geq I_G\left(R_{ONN} + R_{G(OFF)}\right) = C_{GD}\frac{dVs}{dt}\left(R_{ONN} + R_{G(OFF)}\right) \quad (7)$$

$$R_{G(OFF)} \geq \frac{V_{GS(th)}}{C_{GD}\frac{dVs}{dt}} - R_{ONN} \quad (8)$$

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Selection of Components Externally Connected -continued

2. Bootstrap Capacitor C_{BS}

To reduce ripple voltage, ceramic capacitors with low ESR value are recommended for use in the bootstrap circuit.
The maximum voltage drop (ΔV_{BS}) that we have to guarantee when the high-side external FET is in on state must be:

$$\Delta V_{BS} \leq VCC - VF - V_{BSUVR} - V_{OL} \quad (9)$$

where:
VCC is the gate driver supply voltage,
VF is the forward voltage drop of the bootstrap diode
V_{BSUVR} is the V_{BS} UVLO release voltage
V_{OL} is Drain-source voltage of Low side external FET device
The total charge supplied (Q_{TOTAL}) by the bootstrap capacitor is calculated by following formula.

$$Q_{TOTAL} = Q_G + \left(I_{LKGS} + I_{LKDIO} + I_{QBS}\right)t_{HON} \quad (10)$$

where
Q_G is the total gate charge of external FET,
I_{LKGS} is the gate-source leakage current of external FET,
I_{LKDIO} is the bootstrap diode leakage current,
I_{QBS} is the high-side quiescent current,
t_{HON} is the high-side switch on time.

The bootstrap capacitor value should satisfy the following formula.

$$C_{BS} \geq \frac{Q_{TOTAL}}{\Delta V_{BS}} \quad (11)$$

It is not able to keep being turned on the high side in the same way as the high side switch driver because of the specifications of the bootstrap circuits.

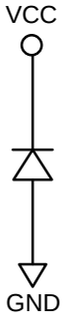
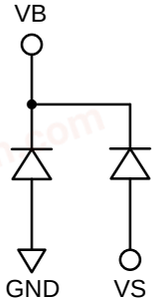
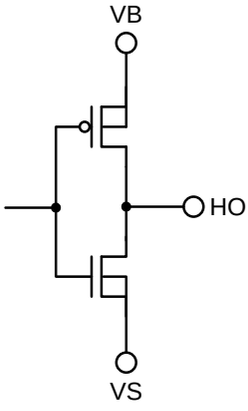
3. Input Capacitor

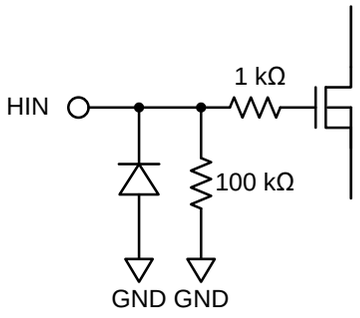
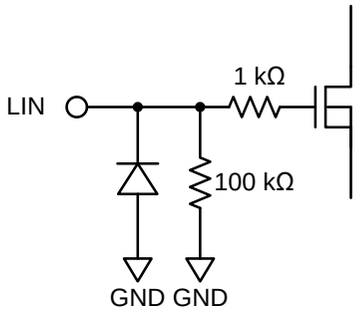
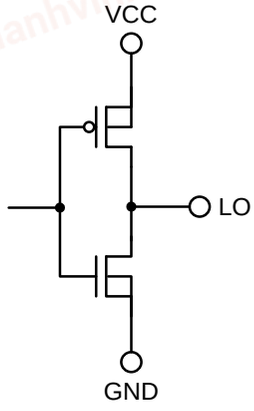
Mount a low-ESR ceramic input capacitor near the VCC pin to reduce input ripple.
For VCC capacitor, it is recommended to use a ceramic capacitor which has a value of two times or larger than that of the boot strap capacitor.

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I/O Equivalence Circuits

Pin No.	Pin Name	Pin Equivalence Circuit
1	VCC	
2, 4	VB, VS	
3	HO	

Pin No.	Pin Name	Pin Equivalence Circuit
5	HIN	
6	LIN	
8	LO	

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Operational Notes

1. Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

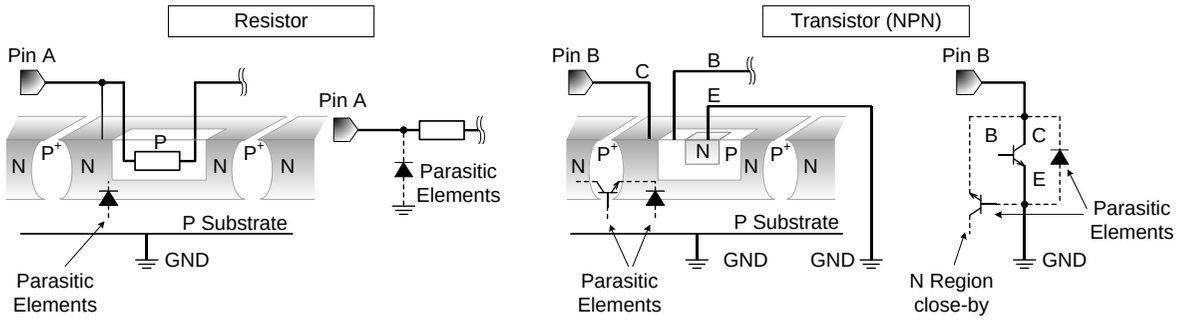


Figure 20. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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Ordering Information

B	D	2	3	2	0	x	E	F	J	-	L	A	E	2

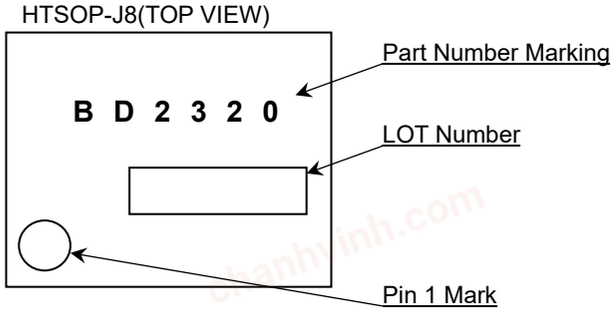
Part Number	Production Line	Package	Product Class	Packaging and Forming Specification
	None: Production line A U: Production line B*(Note7)*	EFJ: HTSOP-J8	LA: For industrial applications	E2: Embossed Tape and Reel

(Note7) For the purpose of improving production efficiency, this product has multi-line configuration. Electric characteristics noted in this datasheet does not differ between the 2 lines. Production line B is recommended for new product.

Marking Diagram

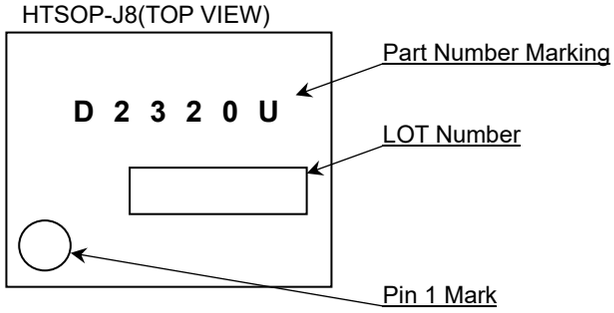
BD2320EFJ-LA

HTSOP-J8(TOP VIEW)



BD2320UEFJ-LA

HTSOP-J8(TOP VIEW)

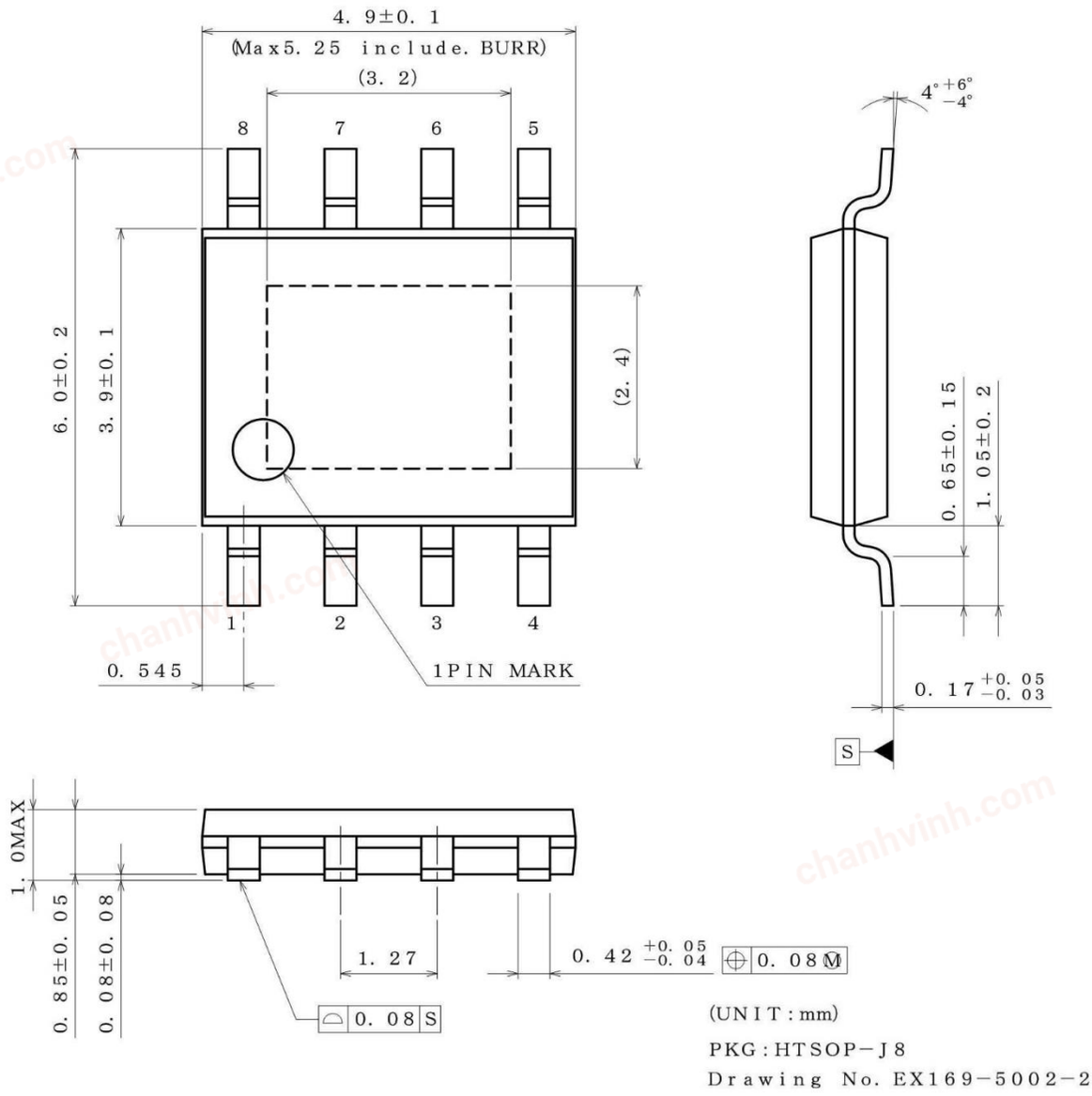


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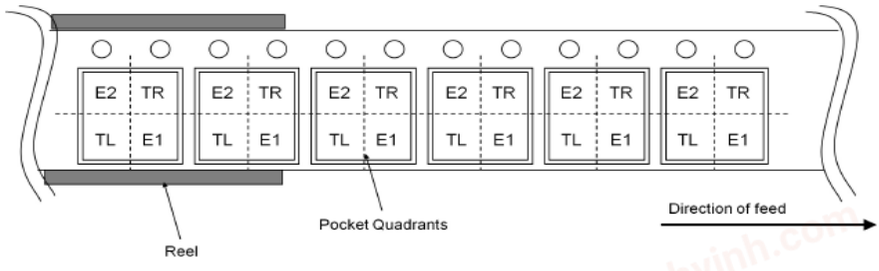
Physical Dimension and Packing Information

Package Name	HTSOP-J8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
04.Dec.2020	001	New Release
29.Mar.2022	002	P1 Added the part number for production line B to the header P17 Added an information for the production line B to Ordering Information P17 Added a marking diagram for the production line B

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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