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Datasheet

Buck LED Driver

2 ch/3 ch Current LED Driver with SPI for Automotive

BD18397RUV-M BD18398RUV-M BD18397EUV-M BD18398EUV-M

General Description

The BD18397/98xxx-M are 2 ch/3 ch synchronous buck DC/DC LED drivers with using on-time topology supporting near fixed switching frequency and fast switching duty regulation and with using average LED current feed buck topology for more accreted LED current regulation system over wide input, LED output range.
The BD18397/98xxx-M can support individual 10-bit analog dimming and 10-bit PWM dimming for LED current by programing the 10-bit register via SPI.
The BD18397/98xxx-M will support LIMP-HOME mode, if SPI communication has an error. In the LIMP-HOME mode, individual LED current can be set by the external pins and can keep LED current sourcing during applying input power without SPI communication.

Features

- AEC-Q100 Qualified*(Note 1)*
- ISO 26262 Process Compliant to Support ASIL-B
- On-time Topology for Near Fixed Frequency Switching
- Average LED Current Regulation
- Protection Diodes Less for Current Sense Pins
- Cycle-by-cycle Switch Over Current Protection
- Thermal Shutdown (TSD)
- Thermal Sensor Reading
- Serial Peripheral Interface (SPI)
- LIMP-HOME Mode

(Note 1) Grade1.

Key Specifications

- Continuous Input Voltage Range
  VIN: 5 V to 45 V
  PIN: 5 V to 65 V
  5VEXT: 4.5 V to 5.5 V
- LED Output Voltage Range: 2.5 V to 60 V
- Maximum Output LED Current/Channel: 2.0 A
- LED Average Current Accuracy: ±3 %
- 10-bit Analog Dimming Range: 5 % to 100 %
- Programmable Switching Frequency Range: 200 kHz to 2.25 MHz
- Junction Temperature Range: -40 °C to +150 °C

Applications

- Automotive Exterior Lamps
  Rear, Turn, DRL/Position, Fog, High/Low Beam etc.

Packages	W (Typ) x D (Typ) x H (Max)
HTSSOP-C48R	12.5 mm x 8.1 mm x 1.0 mm
HTSSOP-C48	12.5 mm x 8.1 mm x 1.0 mm



Typical Application Circuit

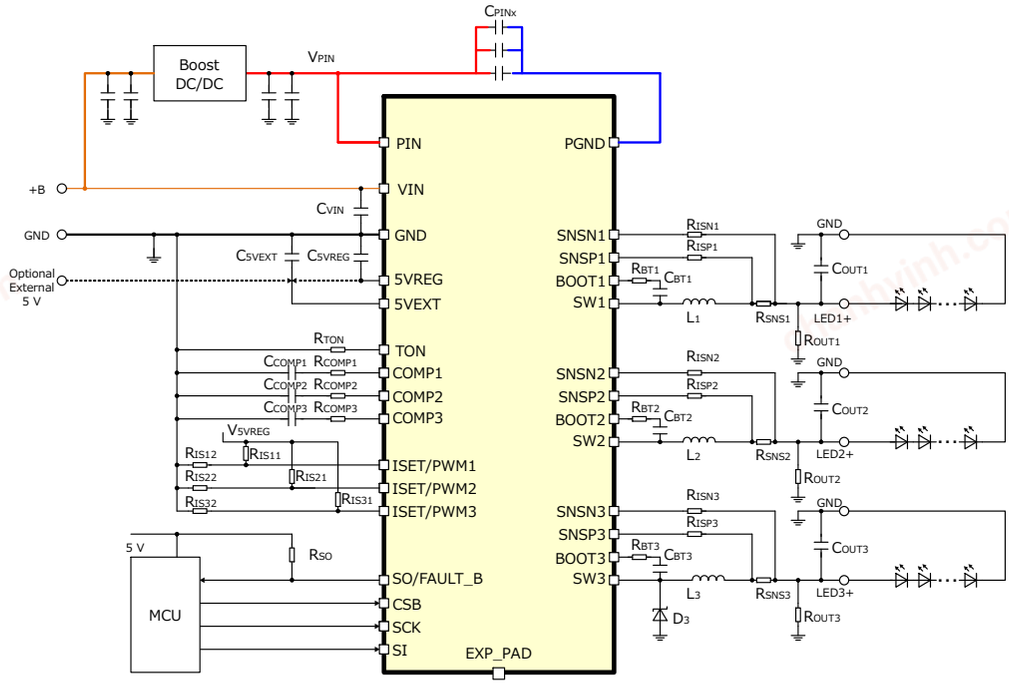


Figure 1. Typical Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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Pin Configurations

(TOP VIEW)

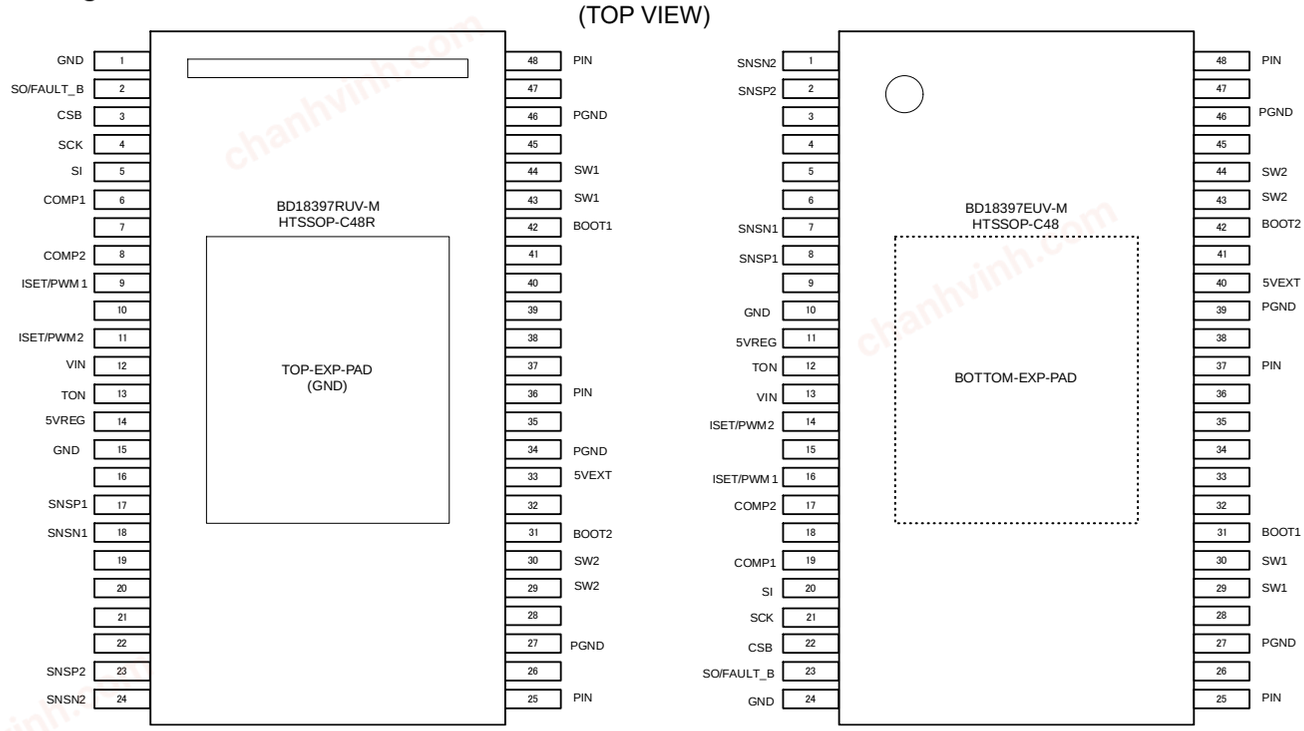


Figure 2. BD18397RUV/EUV-M Pin Configuration

(TOP VIEW)

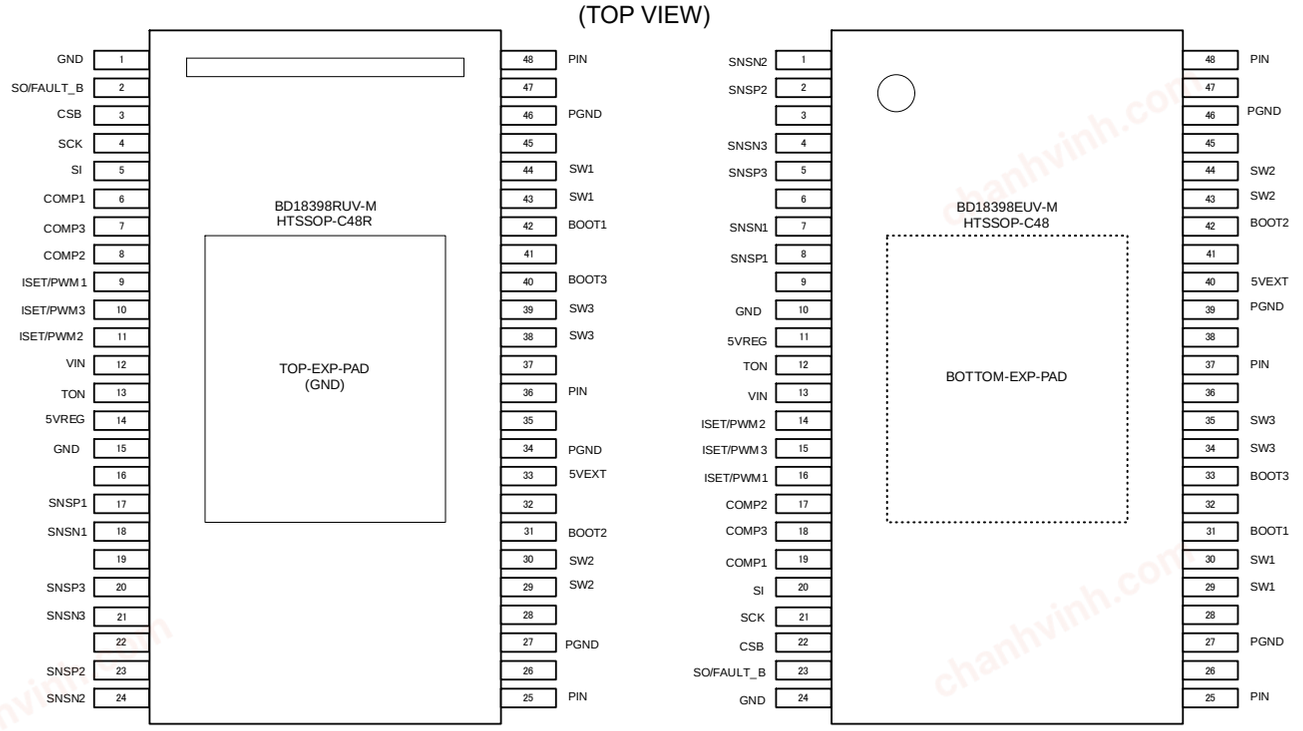


Figure 3. BD18398RUV/EUV-M Pin Configuration

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Pin Descriptions

HTSSOP-C48R	HTSSOP-C48	Pin Name		Function	Unused Pin Setting
		BD18397xxx-M	BD18398xxx-M		
27, 34, 46	27, 39, 46	PGND	PGND	Power ground (channel common).	Not unused
25, 36, 48	25, 37, 48	PIN	PIN	Supply input voltage for power stage (channel common).	Not unused
18	7	SNSN1	SNSN1	LED current sense input - (channel x).	Open
21	4	N.C.	SNSN3		
24	1	SNSN2	SNSN2		
17	8	SNSP1	SNSP1	LED current sense input + (channel x).	Open
20	5	N.C.	SNSP3		
23	2	SNSP2	SNSP2		
42	31	BOOT1	BOOT1	Connecting series resister and boot strap capacitor for high side gate drive (channel x).	Open
40	33	N.C.	BOOT3		
31	42	BOOT2	BOOT2		
43, 44	29, 30	SW1	SW1	Switched output connecting the inductor (channel x). Connecting schottky barrier diode to the SW3 pin.	Open
38, 39	34, 35	N.C.	SW3		
29, 30	43, 44	SW2	SW2		
9	16	ISET/PWM1	ISET/PWM1	LED current setting in the LIMP-HOME mode / PWM dimming (channel x).	Pulled down by external resister
10	15	N.C.	ISET/PWM3		
11	14	ISET/PWM2	ISET/PWM2		
6	19	COMP1	COMP1	Connecting compensation capacitor (channel x).	Open
7	18	N.C.	COMP3		
8	17	COMP2	COMP2		
12	13	VIN	VIN	Supply input voltage for signal block.	Not unused
13	12	TON	TON	Regulator on-time setting resister pin. Connect a resistor between the TON pin and GND to set the switching frequency.	Not unused
14	11	5VREG	5VREG	Internal 5 V regulator output connecting 4.7 µF capacitor.	Not unused
1, 15	10, 24	GND	GND	Signal ground.	Not unused
33	40	5VEXT	5VEXT	5 V input power supply for the internal gate drive's connecting 4.7 µF capacitor.	Not unused
5	20	SI	SI	Serial data input for SPI.	Open for STNAD-ALONE
4	21	SCK	SCK	Serial clock input for SPI.	Open for STNAD-ALONE
3	22	CSB	CSB	Chip select input for SPI.	GND for STNAD-ALONE
2	23	SO/FAULT_B	SO/FAULT_B	Serial data open drain output for SPI. In LIMP-HOME mode, fault condition output (open drain output and low level active) Connecting pulled-up resister.	Open
TOP-EXP-PAD (GND)	BOTTOM-EXP-PAD (GND)	-		Exposed pad for thermal cooling and internal connected to GND. *(Note 1)*	-
-	-	N.C.		Non wire connecting.	Open

(x = 1, 2, 3)

(Note 1) Exposed PAD is signal ground (connecting to the GND pin internally). The exposed pad should not be connecting to Power-supply or any signal nodes.

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Block Diagram

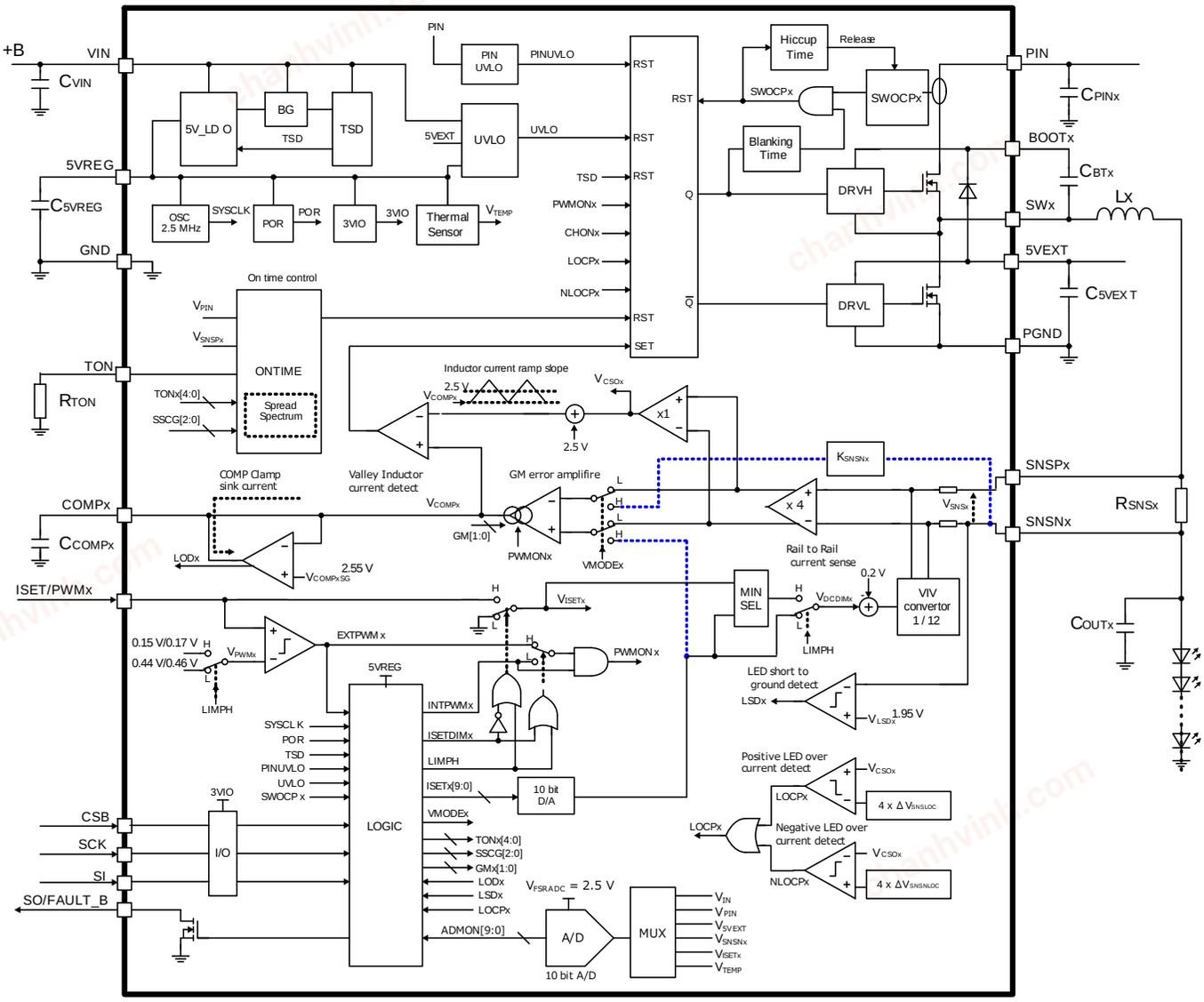


Figure 4. Block Diagram

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Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VIN Supply Voltage	V_{IN}	-0.3 to +50	V
PIN Supply Voltage	V_{PIN}	-0.3 to +70	V
5VEXT Supply Voltage	V_{5VEXT}	-0.3 to +7	V
BOOTx to SWx Voltage	V_{BTSWx}	-0.3 to +7	V
SWx to PGND Voltage	V_{SWx_PGND}	-0.3 to V_{PIN}	V
SNSPx, SNSNx Voltage	V_{SNSPx}, V_{SNSNx},	-0.3 to V_{PIN}	V
SNSPx to SNSNx Voltage	V_{SNSx}	-0.8 to +0.8	V
ISET/PWMx Input Voltage	$V_{ISET/PWMx}$	-0.3 to +7	V
TON Input Voltage	V_{TON}	-0.3 to V_{IN}	V
5VREG Output Voltage	V_{5VREG}	-0.3 to +7	V
VIN to 5VREG Voltage	V_{VIN_5VREG}	-0.3 to +50	V
SI, SCK, CSB Input Voltage	V_{SI}, V_{SCK}, V_{CSB}	-0.3 to +7	V
SO/FAULT_B Output Voltage	$V_{SO/FAULT_B}$	-0.3 to +7	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(x = 1, 2, 3)

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

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Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		JEDEC 2s2p(Note 5)	JEDEC 2s2p + Heat sink(Note 3)	
HTSSOP-C48R				
Junction to Ambient(Note 1)	θ_{JA}	54	13.3	°C/W
Junction to Case-top(Note 2)	θ_{JC_TOP}	1.12	-	°C/W
Junction to Board Characterization Parameter(Note 1) (Note 4)	Ψ_{JB}	31	7	°C/W

(Note 1) θ_{JA}, Ψ_{JB} is measured with JEDEC 2s2p mounted.
(Note 2) $\theta_{JC\text{-}TOP}$ is measured with the IC pressed against the cold plate. The result of N = 1 pc.
For more information about traditional and new thermal metrics, see the Measurement Method and Usage of Thermal Resistance RthJC application note.
(Note 3) Heat sink: 57 mm x 50 mm x 30 mmt, Number of FINs is 6, FIN width 1 mm, Thermal interface material thickness is 1 mm and Thermal conductivity 3.2 W/mK.
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the board located within 1 mm from the IC.
(Note 5) Using a PCB board based on JESD51-5, 7.

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 8)	2s2p(Note 9)	
HTSSOP-C48				
Junction to Ambient(Note 6)	θ_{JA}	62	22	°C/W
Junction to Top Characterization Parameter(Note 6) (Note 7)	Ψ_{JT}	3	2	°C/W

(Note 6) Based on JESD51-2A(Still-Air).
(Note 7) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 8) Using a PCB board based on JESD51-3.
(Note 9) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 10)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 10) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
VIN Continuous Supply Voltage *(Note 1)*		V_{IN}	5	13	45	V
PIN Continuous Supply Voltage *(Note 1)*		V_{PIN}	5	-	65	V
5VEXT Continuous Supply Voltage *(Note 1)*		V_{5VEXT}	4.5	5.0	5.5	V
SNSNx LED Output Voltage		V_{OUTx}	2.5		60	V
Bootstrap Voltage between the BOOTx Pin and the SWx Pin		V_{BTSWx}	3.5	-	-	V
Continuous Average LED Current for channel 1, channel 2		I_{LED1}, I_{LED2}	-	-	1.6	A
Continuous Average LED Current for channel 3 with the SBD *(Note2)*		I_{LED3_SBD}	-	-	1.6	A
Continuous Average LED Current for channel 3 without the SBD *(Note3)*	f_{PWM} = 200 Hz	$I_{LED3_NO_SBD}$	-	-	0.8	A
	f_{PWM} = 400 Hz		-	-	1.1	A
	f_{PWM} = 800 Hz		-	-	1.4	A
	f_{PWM} = 1200 Hz (external PWM only)		-	-	1.6	A
PWM Dimming Frequency for all channel Channel 3 is disable		f_{PWM_CH3OFF}	200	-	-	Hz
PWM Dimming Frequency for all channel Channel 3 is enabled with the SBD *(Note2)*		f_{PWM_SBD}	200	-	-	Hz
PWM Dimming Frequency for all channel without the SBD *(Note3)*	$I_{LED3_NO_SBD}$ = 0.8 A	$f_{PWM_NO_SBD}$	200	-	-	Hz
	$I_{LED3_NO_SBD}$ = 1.1 A		400	-	-	Hz
	$I_{LED3_NO_SBD}$ = 1.4 A		800	-	-	Hz
	$I_{LED3_NO_SBD}$ = 1.6 A		1200	-	-	Hz
Continuous Total Average LED Current *(Note 4)*	BD18397RUV-M	I_{LED_TOTAL}	-	-	3.2	A
	BD18398RUV-M		-	-	4.8	A
	BD18397EUV-M		-	-	2.7	A
	BD18398EUV-M		-	-	2.7	A
Setting Switching Frequency		f_{SWx}	200	-	2250	kHz
PWM Dimming on Pulse Width *(Noet5)*		T_{PWMONx}	50	-	-	µs
PWM Dimming off Pulse Width *(Noet6)*		$T_{PWMOFFx}$	50	-	-	µs
Operating Temperature		Topr	-40	-	+125	°C

(Note 1) ASO should not be exceeded.

(Note 2) For the BD18398xxx-M only, Schottky Barrier Diodes should be needed between the SW3 Pin and the PGND Pin can support higher current setting for the channel 3 and using lower PWM frequency, the forward drop voltage of required SBD is less than 0.81 V at the forward current 2 A.

(Note 3) For the BD18398xxx-M only, without Schottky Barrier Diodes between the SW3 Pin and the PGND Pin, minimum PWM frequency for all channel and maximum current setting for channel 3 should be limited.

(Note 4) Set LED current for each channel less than total LED current: I_{LED_TOTAL} for the BD18397xxx-M = I_{LED1} + I_{LED2}, I_{LED_TOTAL} for the BD18398xxx-M = I_{LED1} + I_{LED2} + I_{LED3}.

(Note 5) Set PWM dimming on pulse width higher than T_{PWMONx} for stable average LED current regulation and detecting LED open.

(Note 6) Set PWM dimming off pulse width higher than $T_{PWMOFFx}$ for stable average LED current regulation. $T_{PWMOFFx}$ should be set higher than following condition: $T_{PWMOFFx} > I_{LEDx} / (V_{OUTx} / L)$.

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Recommended Setting Parts Range

Parameter	Symbol	Min	Typ	Max	Unit
Coupling Capacitor Connecting to the VIN Pin *(Note 1)*	C_{VIN}	0.2	1	-	µF
Coupling Capacitor Connecting to the PIN Pin *(Note 1)*	C_{PINx}	1.0	4.7	-	µF
Coupling Capacitor Connecting to the 5VEXT Pin *(Note 1)*	C_{5VEXT}	2.0	4.7	-	µF
Compensation Capacitor Connecting to the 5VREG Pin *(Note 1)*	C_{5VREG}	2.0	4.7	-	µF
Switching Compensation Capacitor Connecting to the COMPx Pin *(Note 1)*	C_{COMPx}	0.01	0.10	-	µF
Switching Compensation Series Resistor for CC Mode Connecting to the COMPx Pin	R_{COMPx_CC}	-	0	1	kΩ
Switching Compensation Series Resistor for CV Mode Connecting to the COMPx Pin	R_{COMPx_CV}	-	-	4.7	kΩ
Coupling Capacitor Connecting to the SNSNx Pin	C_{OUTx}	0.10	0.47	-	µF
Boot Strap Capacitor Connection between the BOOTx Pin and the SWx Pin *(Note 1)*	C_{BTx}	1.0	2.2	4.7	µF
Series Resistor Connecting to the BOOTx Pin *(Note 2)*	R_{BTx}	0.0	4.7	22.0	Ω
Total Coupling Output Capacitor for CV Mode	C_{OUTx_cv}	10	-	-	µF
Resistor Connecting to the TON Pin	R_{TON}	9.1	-	100	kΩ
Pulled-up Resistor Connecting to the SO/FAULT_B Pin	R_{SO}	1	-	-	kΩ
Current Sense Resister	R_{SNSx}	91	-	-	mΩ
Resistor Connecting to the SNSPx Pin, the SNSNx Pin	R_{ISPx}, R_{ISNx}	0.82	1.00	1.50	kΩ
Pulled-down Resistor Connecting to Output *(Note 3)*	R_{OUTx}	-	-	100	kΩ

(Note 1) Set the capacitor taking temperature characteristics, DC bias characteristics, etc. into consideration.
(Note 2) Set the series resister to improve electromagnetic interference performance.
(Note 3) Set the resister to discharge output capacitor during corresponding channel disable.

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Electrical Characteristics

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = -40 °C to +150 °C)

Parameter		Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
[Total]							
VIN Sleep Circuit Current		I_{INSLP}	-	0.65	1.20	mA	
VIN STANDBY Circuit Current	BD18397xxx-M	I_{INSTB}	-	1.8	3.3	mA	
	BD18398xxx-M		-	2.0	3.6	mA	
PIN STANDBY Circuit Current		I_{PINSTB}	-	43	80	µA	No-Switching
5VEXT STANDBY Circuit Current		$I_{5VEXTSTB}$	-	65	130	µA	No-Switching
5VEXT Switching Circuit Current	BD18397xxx-M	$I_{5VEXTSW}$	-	4.2	-	mA	All Channels Switching f_{SWx} = 400 kHz
	BD18398xxx-M		-	6.3	-	mA	
VIN UVLO Threshold		V_{INUVD}	3.80	4.10	4.30	V	Falling Detect Threshold
		V_{INUVR}	4.15	4.50	4.73	V	Rising Release Threshold
		$V_{INUVHYS}$	-	0.40	-	V	Hysteresis
PIN UVLO Threshold		V_{PINUVD}	3.80	4.10	4.30	V	Falling Detect Threshold
		V_{PINUVR}	4.15	4.50	4.73	V	Rising Release Threshold
		$V_{PINUVHYS}$	-	0.40	-	V	Hysteresis
5VREG, 5VEXT UVLO Threshold		V_{5VUVD}	3.80	4.10	4.30	V	Falling Detect Threshold
		V_{5VUVR}	3.90	4.20	4.40	V	Rising Release Threshold
		$V_{5VUVHYS}$	-	0.10	-	V	Hysteresis
5VREG POR Threshold		$V_{5VRPORD}$	2.50	2.70	2.90	V	Falling Detect Threshold
		$V_{5VRPORR}$	2.70	2.90	3.10	V	Rising Release Threshold
		$V_{5VRPORHYS}$	-	0.20	-	V	Hysteresis
[Reference Voltage]							
5VREG Reference Voltage		V_{5VR}	4.85	5.00	5.15	V	C_{5VREG} = 4.7 µF I_{5VREG} = 0 mA to 25 mA
5VREG Drop Voltage		V_{5VRDP}	-	0.15	0.35	V	V_{IN} = 4.75 V I_{5VREG} = 25 mA
5VREG Output Current Limit		I_{5VRLM}	100	-	-	mA	

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Electrical Characteristics - continued

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[DCDC Convertor Switching]						
SWx ON Resistor High Side	R_{SWxONH}	-	360	470	mΩ	I_{SWx} = -10 mA, Tj = -40 °C to +25 °C
		-	-	720	mΩ	I_{SWx} = -10 mA, Tj = 150 °C
SWx ON Resistor Low Side	R_{SWxONL}	-	260	340	mΩ	I_{SWx} = 10 mA, Tj = -40 °C to +25 °C
		-	-	550	mΩ	I_{SWx} = 10 mA, Tj = 150 °C
SWx Over Current Protection Threshold	I_{SWxOCP}	3.0	3.6	4.2	A	
SWx Over Current Protection Blanking Time	$t_{SWxOCPBLK}$	-	80	-	ns	
SWx Over Current Protection Hiccup Time	$t_{HICCUPx}$	-	128	-	µs	
SWx Over Current Protection Flag Set Delay Time	t_{OCPx}	0.7	1.0	1.3	ms	
SWx Over Current Protection Flag Release Delay Time	t_{OCPxR}	0.7	1.0	1.3	ms	
SWx Minimum On Time	$t_{SWxONMIN}$	-	90	145	ns	V_{SNSNx} = 0 V
SWx Minimum Off Time	$t_{SWxOFFMIN}$	-	100	150	ns	V_{SNSPx} - V_{SNSNx} = 0 V
[On Time]						
On Time Setting	t_{ONx1}	1.120	1.250	1.380	µs	V_{SNSPx} = 30 V, R_{TON} = 51 kΩ TONx[5:0] = 7 (default)
	t_{ONx2}	0.219	0.243	0.267	µs	V_{SNSPx} = 30 V, R_{TON} = 51 kΩ TONx[5:0] = 43
	t_{ONx3}	0.214	0.237	0.260	µs	V_{SNSPx} = 30 V, R_{TON} = 9.1 kΩ TONx[5:0] = 7 (default)
	f_{SSFM}	-	1044	-	Hz	SSCG[2:0] = 7
		-	536	-	Hz	SSCG[2:0] = 5
		-	283	-	Hz	SSCG[2:0] = 3
		-	155	--	Hz	SSCG[2:0] = 1
		Not applicable			-	SSCG[2:0] = 0 (default)
On Time Spread Spectrum Width	$t_{ONSSFMW}$	-	±6	-	%	
[GM Error Amplifier]						
Trans Conductance	gm	-	1360	-	µS	GMx[1:0] = 0 (default)
		-	870	-		GMx[1:0] = 1
		-	530	-		GMx[1:0] = 2
		-	300	-		GMx[1:0] = 3
COMP Source Current	I_{COMPSO}	-	240	-	µA	GMx[1:0] = 0 (default)
		-	120	-		GMx[1:0] = 1
		-	60	-		GMx[1:0] = 2
		-	30	-		GMx[1:0] = 3
COMP Sink Current	I_{COMPSI}	-	240	-	µA	GMx[1:0] = 0 (default)
		-	120	-		GMx[1:0] = 1
		-	60	-		GMx[1:0] = 2
		-	30	-		GMx[1:0] = 3

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Electrical Characteristics - continued

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Current Sense Amplifier]						
SNSPx to SNSNx Total Average Current Sense Threshold Voltage Including SNSPx and SNSNx Differential Input Current Voltage Drop Over R_{ISNx} = 1 kΩ	$V_{SNSxAVE\ 100\%H}$	184.7	191.5	198.2	mV	V_{SNSNx} = 4 V, R_{ISNx} = 1 kΩ ISETx[9:0] = 1023
	$V_{SNSxAVE\ 87\%H}$	160.6	166.6	172.6	mV	V_{SNSNx} = 4 V, R_{ISNx} = 1 kΩ ISETx[9:0] = 901 (default)
	$V_{SNSxAVE\ 50\%H}$	90.7	95.6	100.5	mV	V_{SNSNx} = 4 V, R_{ISNx} = 1 kΩ ISETx[9:0] = 552
	$V_{SNSxAVE\ 10\%H}$	15.1	19.1	23.1	mV	V_{SNSNx} = 4 V, R_{ISNx} = 1 kΩ ISETx[9:0] = 176
	$V_{SNSxAVE\ 87\%L}$	153.3	166.6	179.9	mV	V_{SNSNx} = 0 V, Low-side-sense ISETx[9:0] = 901 (default)
Current Sense Threshold Resolution	$\Delta V_{SNSxLSB}$	-	0.203	-	mV	
Current Sense Threshold Differential Non-Linearity	$\Delta V_{SNSxDNL}$	-	±2	-	LSB	
Input Differential Sense Voltage Dynamic Range	V_{SNSxD}	-200	-	+200	mV	V_{SNSx} Voltage
Input Differential Sense Voltage Output Gain	G_{SNS}	-	4	-	V/V	V_{SNSx} Input to Output for GM Error Amplifier Gain
SNSPx Input Current	I_{SNSPx}	38.0	54.5	85.0	µA	V_{SNSx} = 191.5 mV V_{SNSNx} = 4 V
SNSNx Input Current	I_{SNSNx}	38.0	54.5	85.0	µA	V_{SNSx} = 191.5 mV V_{SNSNx} = 4 V
SNSPx and SNSNx Differential Input Current	$I_{DIF_SNSx_100\%H}$	-1.5	0	+1.5	µA	V_{SNSx} = 191.5 mV V_{SNSNx} = 4 V
	$I_{DIF_SNSx_10\%H}$	-1.0	0	+1.0	µA	V_{SNSx} = 19.1 mV V_{SNSNx} = 4 V
LED Short to Ground Detect Status Set Threshold	V_{LSDx}	1.80	1.95	2.10	V	V_{SNSNx} Falling
LED Short to Ground Flag Set Delay Time	$t_{SNSxLVD}$	7	10	13	ms	
LED Short to Ground Flag Release Delay Time	$t_{SNSxLVDR}$	0.7	1	1.3	ms	
LED Over Current Protection Threshold	$\Delta V_{SNSxLOCP}$	320	390	500	mV	V_{SNSx} Rising ISETx[9:0] = 82 Rising or VMODEx = 1
Negative LED Over Current Protection Threshold	$\Delta V_{SNSxNLOCP}$	-500	-390	-320	mV	V_{SNSx} falling ISETx[9:0] = 82 Rising, or VMODEx = 1
LED Over Current Protection Blanking Time	$t_{SNSxLOCBLK}$	-	120	-	ns	
Negative LED Over Current Protection Blanking Time	$t_{SNSxNLOCBLK}$	-	80	-	ns	
LED Status Good COMP Over Threshold	$V_{COMPxSG}$	-	2.55	-	V	
LED Status Good Flag Set Delay Time	t_{SNSxSG}	7	10	13	ms	
LED Status Good Flag Release Delay Time	$t_{SNSxSGR}$	0.7	1	1.3	ms	

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Electrical Characteristics - continued

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Voltage Sense]						
SNSNx Voltage Sense Resistor Divider Ratio	K_{SNSNx}	-	0.037	-	-	
SNSNx Voltage Sense Threshold	V_{SNSNx_1}	46.5	50.0	53.5	V	ISETx[9:0] = 758
	V_{SNSNx_2}	23.5	25.0	26.5	V	ISETx[9:0] = 379
	V_{SNSNx_3}	14.1	15.0	15.9	V	ISETx[9:0] = 227
	V_{SNSNx_4}	6.60	7.00	7.40	V	ISETx[9:0] = 106
	V_{SNSNx_5}	4.75	5.00	5.25	V	ISETx[9:0] = 76
SNSNx Voltage Sense Threshold Resolution	$\Delta V_{SNSNxLSB}$	-	0.066	-	V	

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Electrical Characteristics - continued

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[A/D Convertor]						
A/D Resolution	RES_{ADC}	-	10	-	bit	
A/D Conversion Time	t_{ADC}	-	11.2	-	µs	
A/D Full Scale Reference Voltage	V_{FSRADC}	2.43	2.50	2.57	V	
Integral Nonlinearity	INL	-	±2	-	LSB	
Differential Nonlinearity	DNL	-	±2	-	LSB	
ADC Monitoring Nodes Full Scale Range	V_{FSR1}	-	48	-	V	V_{IN}
	V_{FSR2}	-	70	-	V	V_{PIN}
	V_{FSR3}	-	67.5	-	V	V_{SNSNx}
	V_{FSR4}	-	5.5	-	V	V_{5VEXT}
	V_{FSR5}	-	V_{FSRADC}	-	V	$V_{ISET/PWMx}$
ADC Monitoring Nodes Read Values Total Accuracy	ΔADC	-6	-	+6	%	
Thermal Sensor Voltage ADC Read Value	ADC_{TEMP25}	394	418	442	-	Tj = 25 °C
	$ADC_{TEMP150}$	577	602	627	-	Tj = 150 °C
[PWM Dimming]						
ISET/PWMx Input for DC/DC Switching On Threshold 1	V_{PWMxH1}	0.42	0.46	0.50	V	Rising In the LEDACTIVE
ISET/PWMx Input for DC/DC Switching Off Threshold 1	V_{PWMxL1}	0.40	0.44	0.48	V	Falling In the LEDACTIVE
ISET/PWMx Input for DC/DC Switching On Threshold 2	V_{PWMxH2}	0.15	0.17	0.19	V	Rising In the LIMP-HOME or STAND-ALONE
ISET/PWMx Input for DC/DC Switching Off Threshold 2	V_{PWMxL2}	0.13	0.15	0.17	V	Falling In the LIMP-HOME or STAND-ALONE
ISET/PWMx to DC/DC Switching On Transition Delay	t_{PWMxH}	-	0.1	1.0	µs	
ISET/PWMx to DC/DC Switching Off Transition Delay	t_{PWMxL}	-	0.2	1.0	µs	
Internal PWM Frequency	f_{PWM}	-	203	-	Hz	PWMDIV[2:0] = 1 (default)
		-	407	-	Hz	PWMDIV[2:0] = 4
		-	610	-	Hz	PWMDIV[2:0] = 6
		-	814	-	Hz	PWMDIV[2:0] = 7
[LOGIC I/O SCK, CSB, SI, SO/FAULT_B]						
Internal Oscillator Frequency	f_{OSC}	2.0	2.5	3.0	MHz	
Input Voltage High	V_{IHxx}	2.2	-	-	V	SCK, CSB, SI pins
Input Voltage Low	V_{ILxx}	-	-	0.6	V	
Input Pull-down Resister	R_{INxx_PD}	250	500	1000	kΩ	SCK, SI pins
CSB Pull-up Current	I_{CSBOL}	-	10	-	µA	V_{CSB} = 0 V
SO/FAULT_B Output Low Voltage	$V_{SO/FAULT_B_OL}$	-	-	0.6	V	$I_{SO/FAULT_B_O}$ = 10 mA
SO/FAULT_B Output Leakage Current	$I_{SO/FAULT_B_LEAK}$	-	-	1	µA	$V_{SO/FAULT_B}$ = 5 V

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Description of Blocks

1 Buck Converter LED Current Regulation

The BD18397/98xxx-M is synchronous buck converter with nearly fixed switching frequency and provides stable LED current over wide input and output voltage dynamic range. The BD18397/98xxx-M is using average inductor current regulation by control inductor valley current in average inductor current sensing feedback loop. In buck convertor topology, Inductor current is same with LED current, so that this inductor valley current control can be used for accurate LED current regulation loop.
The BD18397/98xxx-M are using constant on time topology supporting nearly fixed switching frequency over input and output voltage change. The internal on-time generator supporting nearly fixed switching frequency makes timing for the buck converter SW output tuned off (“RST”) based on desired switching on-duty calculated by the real time sensing V_{PIN} and V_{SNSPx} voltage.
The internal valley current detector makes timing for the buck converter SW output turned on (“SET”) compared with inductor valley current and integrated error output signal V_{COMPx} of the GM amplifier inputs between LED current regulation reference voltage V_{DCDIMx} and LED current sensing differential voltage V_{SNSx} between the SNSPx pin and the SNSNx pin.

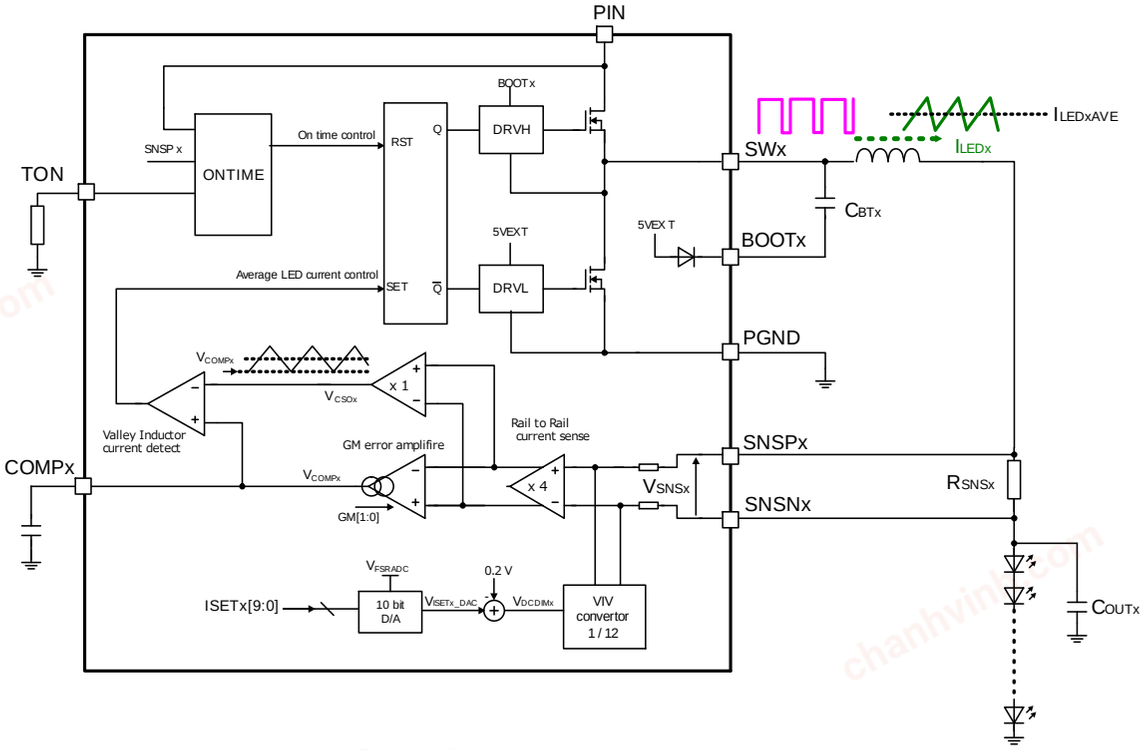


Figure 5. Buck Converter LED Current Regulation

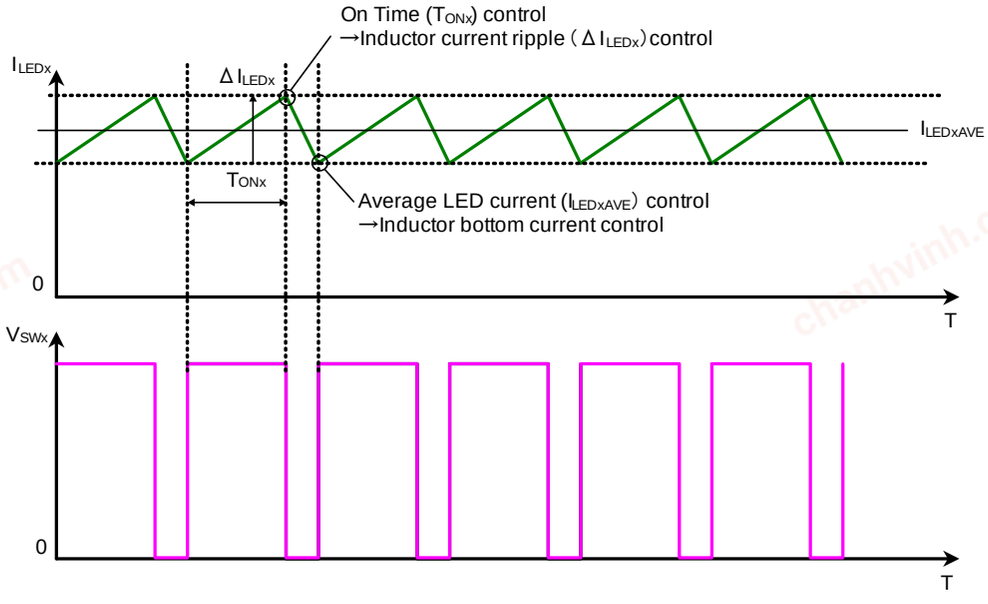


Figure 6. Buck Converter LED Current Regulation Waveforms

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Description of Blocks - continued

2 LED Current Setting (Current Sense)

Full-scale LED average current can be set by resistor R_{SNSx} connected between the SNSPx pin and the SNSNx pin and can be programmable by SPI register ISETx[9:0]. The internal Rail-to-Rail current sense amplifier is monitoring LED current by differential voltage (V_{SNSx}) over R_{SNS} between the SNSPx pin and SNSNx pin and generating an error output voltage compared between the V_{SNSx} and the scaled reference voltage (V_{DCDIMx} / 12). This error output will be integrated by the compensation capacitor C_{COMPX} connecting to the COMPx pin.

The Internal reference voltage V_{DCDIMx} is defined by the fixed internal offset voltage (-0.2 V) and the programable Voltage V_{ISETx_DAC} set by the ISETx[9:0]. The 10-bit DAC convertor full scale range is 2.5 V (V_{FSRADC}) same with the internal 10-bit ADC .Programmable LED average current can be calculated by as following formula.

$$I_{LEDxAVE} = \frac{V_{SNSxAVE}}{R_{SNSx}} = \frac{V_{DCDIMx}}{12 \times R_{SNSx}} = \frac{V_{ISETx_DAC} - 0.2\,V}{12 \times R_{SNSx}}$$
$$= \left(\frac{ISETx[9:0]}{1024} \times V_{FSRADC} - 0.2\,V \right) \times \frac{1}{12 \times R_{SNSx}}$$

Where:

$V_{SNSxAVE}$ is the average current sense regulation voltage.

V_{DCDIMx} is the internal reference voltage before scaling (1 / 12) for the Rail-to-Rail current sense amplifier.

V_{ISETx_DAC} is the 10-bit DAC outputs set by the $ISETx[9:0]$ to define the V_{DCDIMx}.

V_{FSRADC} is the reference voltage of the 10-bit DAC outputs for the V_{ISETx_DAC}.

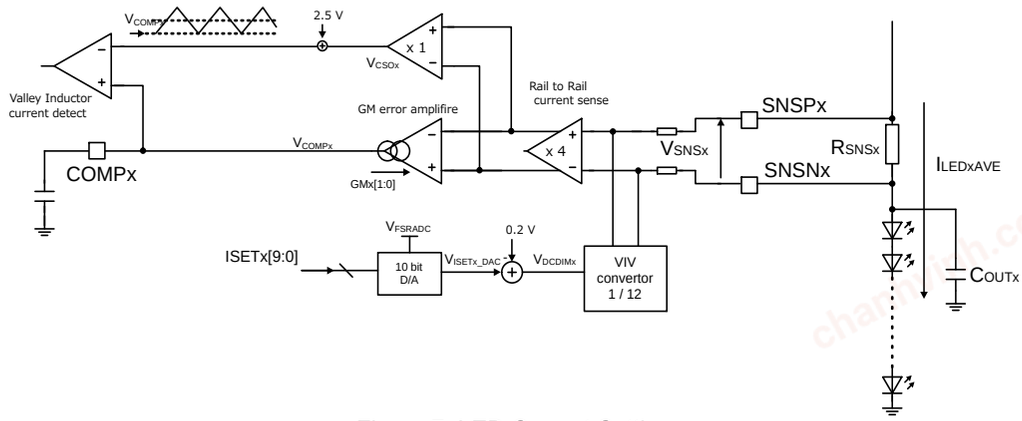


Figure 7. LED Current Setting

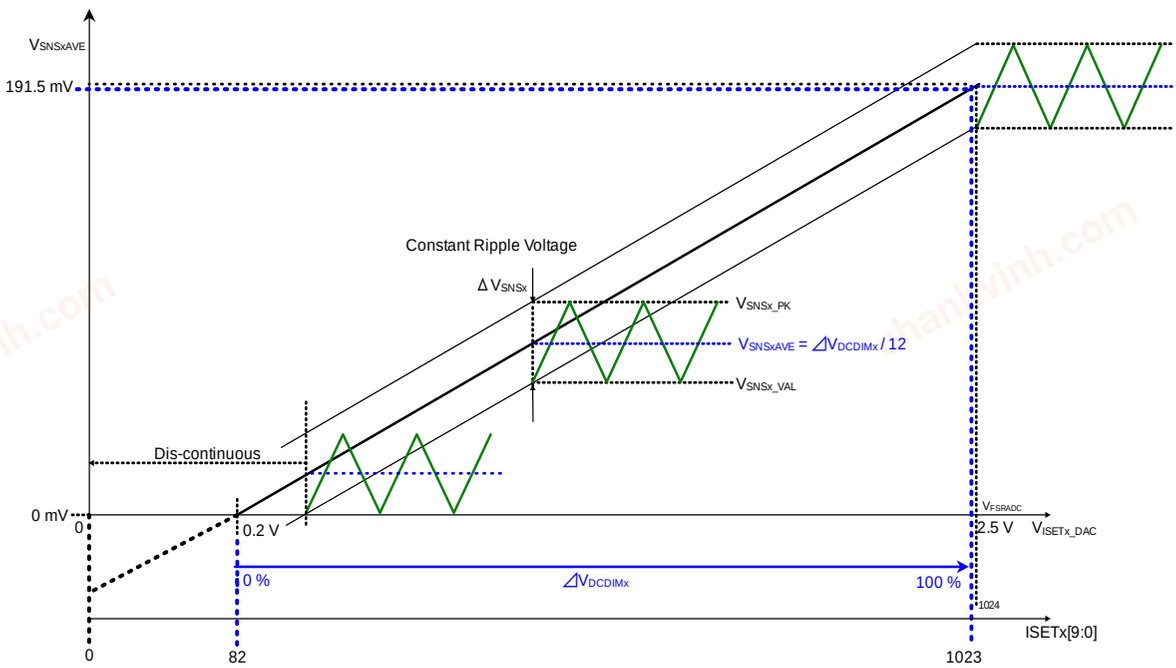


Figure 8. Current Sense Regulation Voltage Setting

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Description of Blocks - continued

3 DCDC Switching Frequency

The buck converter switching on-duty (D_{ONx}) and frequency (f_{SWx}) is defined as following.

$$D_{ONx} = \frac{V_{SNSPx}}{V_{PIN}}, \qquad T_{ONx} = \frac{D_{ONx}}{f_{SWx}} \rightarrow f_{SWx} = \frac{D_{ONx}}{T_{ONx}} = \frac{1}{T_{ONx}} \times \frac{V_{SNSPx}}{V_{PIN}}$$

The buck converter switching frequency (f_{SWx}) can be nearly fixed by the adapting constant on time, this on-time T_{ONx} will be proportional to switching on-duty D_{ONx} by monitoring the buck converter input voltage as the V_{PIN} and output voltage as the V_{SNSPx} as following formula.

$$f_{SWx} \fallingdotseq \frac{1}{T_{ONx}} \times \frac{V_{SNSPx}}{V_{PIN}} \fallingdotseq Constant \rightarrow T_{ONx} \propto \frac{V_{SNSPx}}{V_{PIN}}$$

The BD18397/98xxx-M has the individual on-time circuit in channels generating adapting constant on time T_{ONx} set by the SPI. The On time itself will be changed over switching on-duty changed for fixed switching frequency so that the buck converter switching frequency is set by the SPI register TONx[5:0] and the external resistor (R_{TON}).

$$T_{ONx} \fallingdotseq \frac{k}{TONx[5:0] + 1} \times R_{TON} \times \frac{V_{SNSPx}}{V_{PIN}} \times 10^{-6} + 20 \times 10^{-9}, (k = 0.000386)$$

$$f_{SWx} \fallingdotseq \frac{1}{\frac{k}{TONx[5:0] + 1} \times R_{TON} \times \frac{V_{SNSPx}}{V_{PIN}} \times 10^{-6} + 20 \times 10^{-9}} \times \frac{V_{SNSPx}}{V_{PIN}}$$

*More than 2.25 MHz setting cannot be used.

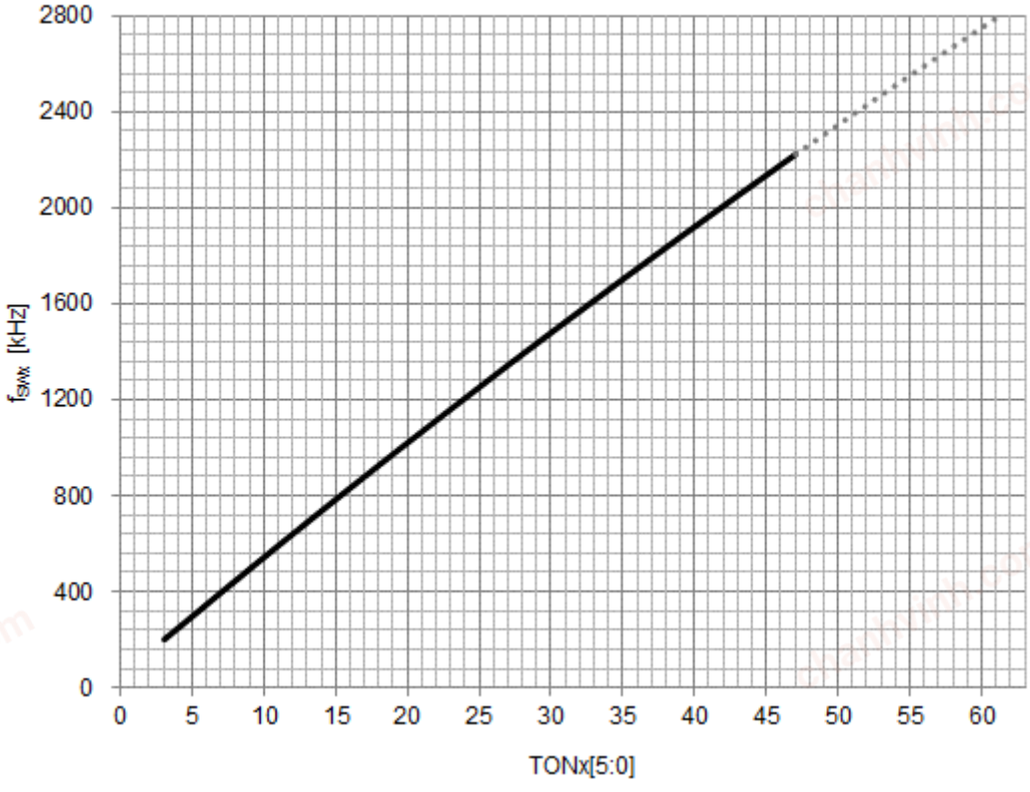


Figure 9. DCDC Switching Frequency vs TONx[5:0] (D_{ONx} = 0.5, R_{TON} = 51 kΩ)

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3 DCDC Switching Frequency - continued

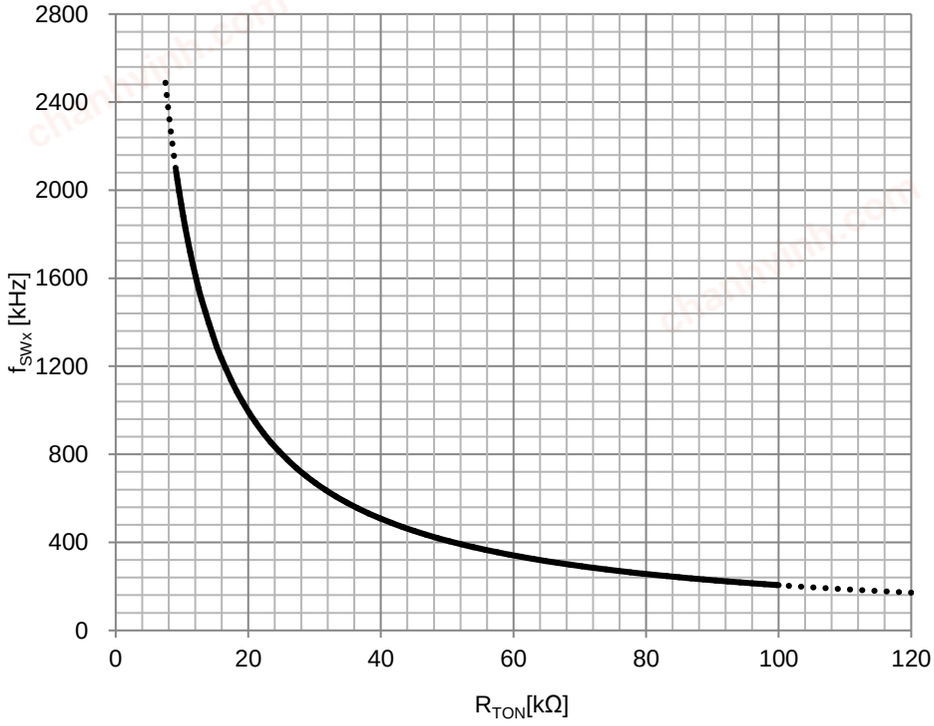


Figure 10. Switching Frequency vs R_{TON} (D_{ONx} = 0.5, TONx[5:0] = 7)

The BD18397/98xxx-M has built-in spread spectrum function and the modulation switching frequency is ± 6% (Typ) around the setting frequency f_{SWx}. The spread spectrum modulation frequency can be programmable by the register SSCG[2:0]. When SSCG[2:0] is set to 0, spread spectrum modulation is not applicable. When enable the SSCG function, all channels of ON time generator use same modulation frequency (f_{SSFM}) to make spread on time based on monitoring on-duty.

SSCG[2:0]	f_{SSFM}[Hz]
0x0	SSCG Not applicable
0x1	155
0x2	185
0x3	283
0x4	361
0x5	536
0x6	763
0x7	1044

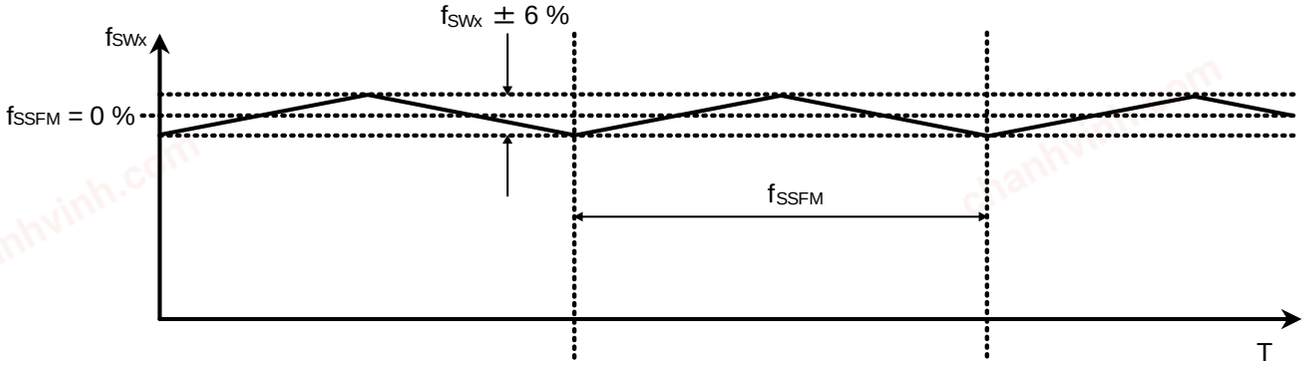


Figure 11. Spread Spectrum

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Description of Blocks - continued

4 Internal PMW Dimming Setting (In the LEDACTIVE Mode)

The BD18397/98xxx-M has an internal 10-bit PWM dimming generator to make timing for individual buck converter switching on/off. The internal PWM dimming (INTPWMx) ON duty cycle (D_{PWMx}) set by SPI register the DPWMx[9:0].
PWM dimming frequency f_{PWM} can be set by SPI register the PWMDIV[2:0] and this PWM dimming frequency setting is commonly used in all buck channels for synchronous PMW dimming within the device itself.

$$D_{PWMx} = \frac{DPWMx[9:0] + 1}{1024}, T_{PWMONx} = \frac{D_{PWMx}}{f_{PWM}}$$

PWMDIV[2:0]	f_{PWM}[Hz]
0x0	153
0x1	203
0x2	244
0x3	305
0x4	407
0x5	488
0x6	610
0x7	814

Minimum PWM dimming pulse width is depends on using inductor and average current setting because of inductor current charge per one DCDC switching on cycle limited.

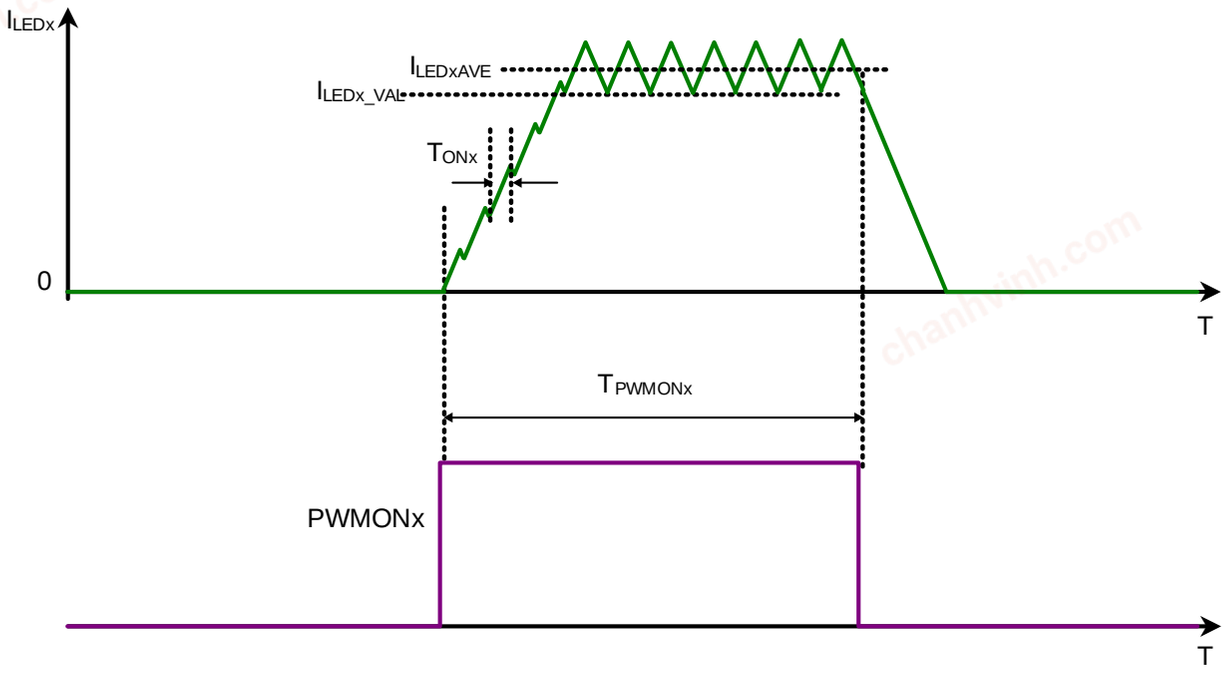


Figure 12. PWM Dimming Waveform

5 External PWM Dimming Setting (In the LEDACTIVE Mode)

PWM Dimming on Pulse Width T_{PWMONx} is controlled by internal PWM dimming generator or external PWM dimming control by the ISET/PWMx pin when the ISETDIMx bit is set in the LEDDC register. If the ISET/PWMx pin is set to high level, TPWM is equal with internal PWM on cycle ($DPWM_x$). If the ISET/PWMx pin is set to low level, TPWM goes low and LED current force turned off. In case of PMM dimming setting DPWMx100% (default), the ISET/PWMx pin can be used for external PWM dimming control for LED current on/off same with internal PWM dimming use case. Minimum PWM dimming pulse width is depends on using inductor and average current setting because of inductor current charge per one DCDC switching on cycle limited.

ISETDIMx	PWMONx Definition for channel x	
	LEDACTIVE	LIMP-HOME or STAND-ALONE
0	DPWMx[9:0]	ISET/PWMx pin
1	ISET/PWMx pin & DPWMx[9:0]	

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Description of Blocks - continued

6 Hybrid External Analog and PWM Dimming Setting (In the LIMP-HOME and STAND-ALONE Mode)

The BD18397/98xxx-M supports “External Analog Dimming mode when the IC state is into the LIMP-HOME or STAND-ALONE mode.

In the external analog dimming mode, internal reference voltage for current regulation can be defined by the ISET/PWMx pin voltage ($V_{ISET/PWMx}$). When the external input voltage $V_{ISET/PWMx}$ pin voltage is less than internal reference voltage V_{ISETx_DAC}, feed-back voltage V_{SNSx} will be regulated by external pin voltage setting.

In case of using analog dimming and PWM dimming by the ISET/PWMx pin, applying PWM peak voltage defines analog dimming level $I_{LEDxAVE}$ and PWM duty (D_{PWMx}) defines PWM dimming ON time T_{PWMONx}. The analog dimming peak voltage V_{PWMx_PK} can be set by the voltage divider (R_{ISX1} and R_{ISX2}) and PWM duty (D_{PWMx}) control by external NPN transistor by applying invert PWM signals (PWMx_B).

Current Setting Definition for channel x	
LEDACTIVE	LIMP-HOME or STAND-ALONE
ISETx[9:0]	ISETx[9:0] & ISET/PWMx pin
$V_{DCDIMx} = V_{ISETx_DAC} - 0.2\,V$	if $V_{ISETx_DAC} > V_{ISET/PWMx}$ $V_{DCDIMx} = V_{ISET/PWMx} - 0.2\,V$, if $V_{ISETx_DAC} < V_{ISET/PWMx}$ $V_{DCDIMx} = V_{ISETx_DAC} - 0.2\,V$

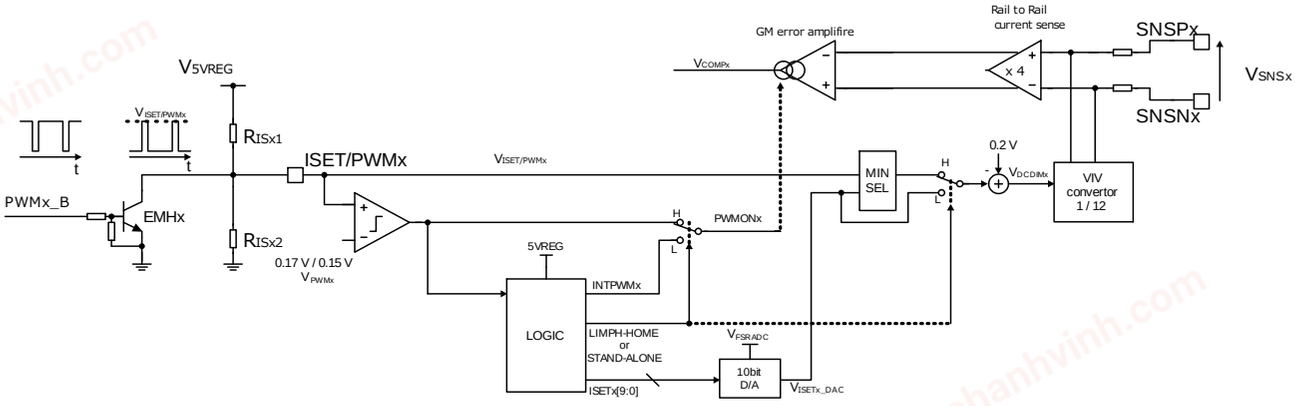


Figure 13. Hybrid External Analog and PWM Dimming

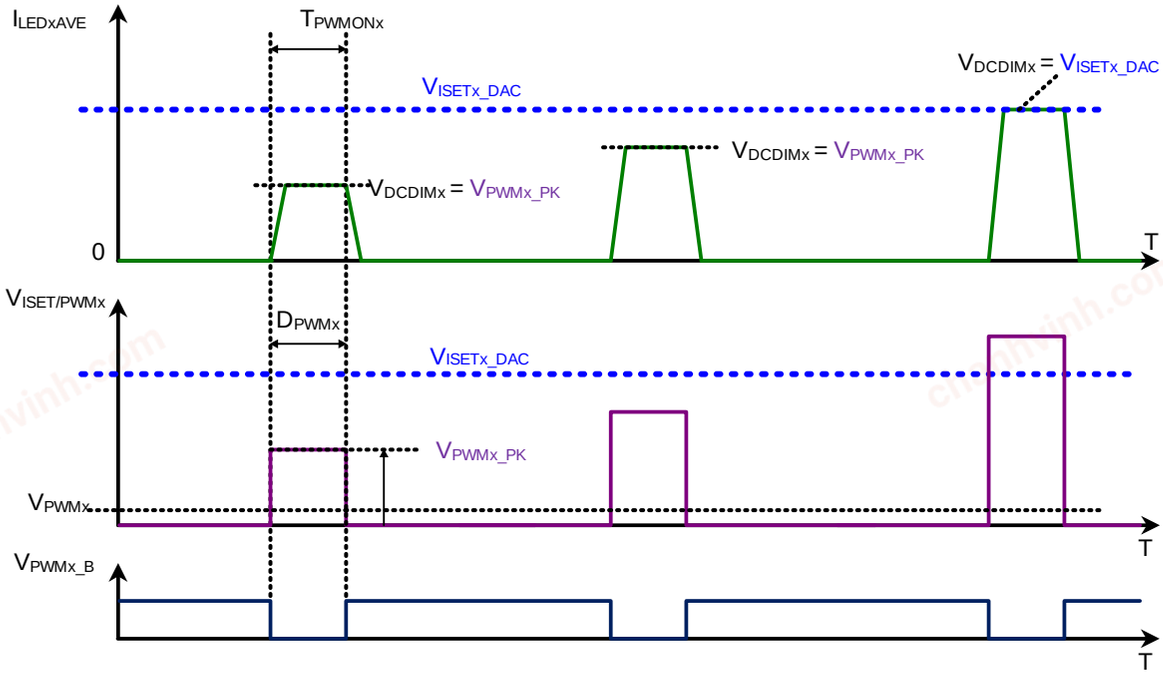


Figure 14. Hybrid External Analog and PWM Dimming Waveforms

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Description of Blocks - continued

7 Bootstrap Charge

The BD18397/98xxx-M is synchronous buck DC/DC LED drivers and contains high side and low side N-channel FETs. The high side gate driver can be working by proper power supply voltage input between the BOOTx pin and the SWx pin. The connecting bootstrap capacitor C_{BTx} can be charged from the 5VEXT pin supply through the internal diode during the SWx pin is pull-down. During the SWx pin switching, corresponding channel bootstrap voltage can maintain by refreshed capacitor energy. When the SWx pin is Hi-z (CHONx = 0 or corresponding channel PWM dimming off time), the bootstrap voltage cannot maintain and becomes lower voltage than recommended bootstrap voltage (V_{BTSWx} > 3.5 V). A large bootstrap capacitor is required to prevent lower bootstrap voltage operation when using lower PWM frequency. An external bleeder resistor R_{OUTx} connecting to the output is required to charge the bootstrap capacitor during the SWx pin is Hi-z (CHONx = 0) and to reduce negative inductor current energy from the output by the SWx pin pulled-down for bootstrap charged at channel turned on. In case of an adding bleeder resistor is not enough off time (CHONx = 0) for completely discharging output capacitor energy, the output capacitor can be fast discharged by the negative inductor current regulation setting (recommended ISETx[9:0] = 57) before channel turned off (CHONx = 0). When turning on the corresponding channel, the output voltage must be sufficiently discharged (V_{OUTx} < 1.5 V) before turning on the corresponding channel (CHONx = 1) to ensure that the bootstrap voltage is above the recommended operating voltage (V_{BTSWx} > 3.5 V).

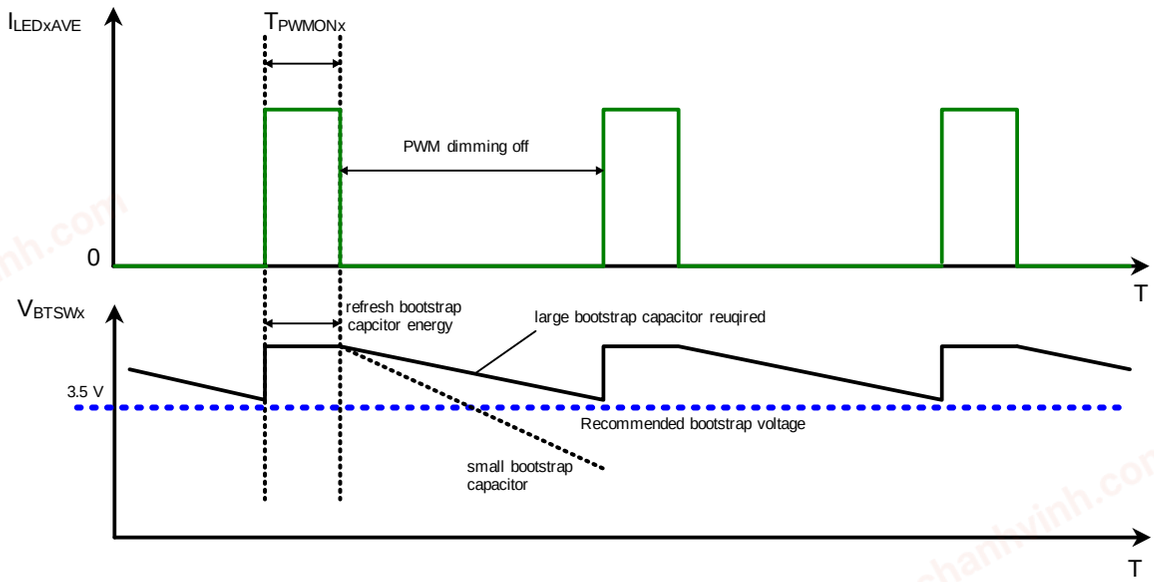


Figure 15. Bootstrap Charge During PWM Dimming Waveforms

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7 Bootstrap Charge - continued

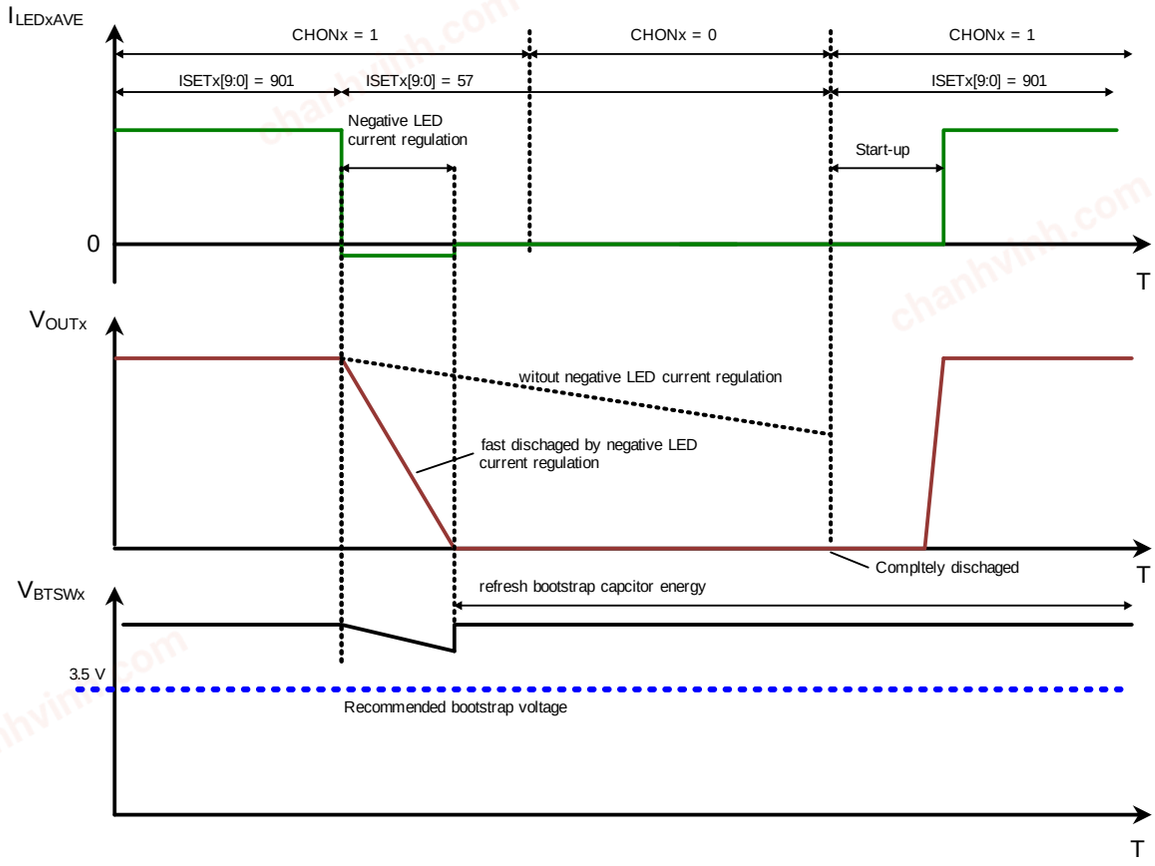


Figure 16. Bootstrap Charge During Channel Off Waveforms

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Description of Blocks - continued

8 Voltage Regulation (In the LEDACTIVE Mode)

The BD18397/98xxx-M supports “Voltage regulation mode when the VMODEx bit is set in the DCDCSET4 register.
In the voltage mode, the BD18397/98xxx-M regulates the SNSNx pin voltage (V_{SNSNx}) by control inductor valley current in average voltage sensing feedback loop. In the voltage mode, The BD18397/98xxx-M are using constant on time topology supporting nearly fixed switching frequency over input and output voltage change. The internal on-time generator supporting nearly fixed switching frequency makes timing for the buck converter SW output tuned off (“RST”) based on desired switching on-duty calculated by the real time sensing V_{PIN} and V_{SNSNx} voltage.
The internal valley current detector makes timing for the buck converter SW output turned on (“SET”) compared with inductor valley current and integrated error output signal V_{COMPx} of the GM amplifier inputs between reference voltage V_{DCDIMx} and output voltage V_{SNSNx} pin.
For soft-output-start to reduce rush charge output current, programmed soft-ramp-up reference voltage (V_{DCDIMx}) or soft-ramp-up the COMP pin voltage by more compensation capacitor (C_{COMPx}).
The voltage regulation mode setting is only activated in LEDACTIVE MODE. In case of LIMP-HOME or STAND-ALONE mode, DCDC coveter should be disabled by corresponding the ISET/PWMx pin pulled down.

$$V_{SNSNx} = \frac{V_{ISETx_DAC}}{K_{SNSNx}} = \left(\frac{ISETx[9:0]}{1024} \times V_{FSRADC}\right) \times \frac{1}{K_{SNSNx}}$$

Where:
V_{SNSNx} is the output regulation voltage.
K_{SNSNx} is the internal voltage divider. $K_{SNSNx} = 1 / 27.$
V_{ISETx_DAC} is the 10-bit DAC outputs set by the $ISETx[9:0]$ for the internal reference voltage of the GM amplifier to define the V_{SNSNx}.
V_{FSRADC} is the reference voltage of the 10-bit DAC outputs the V_{ISETx_DAC}.

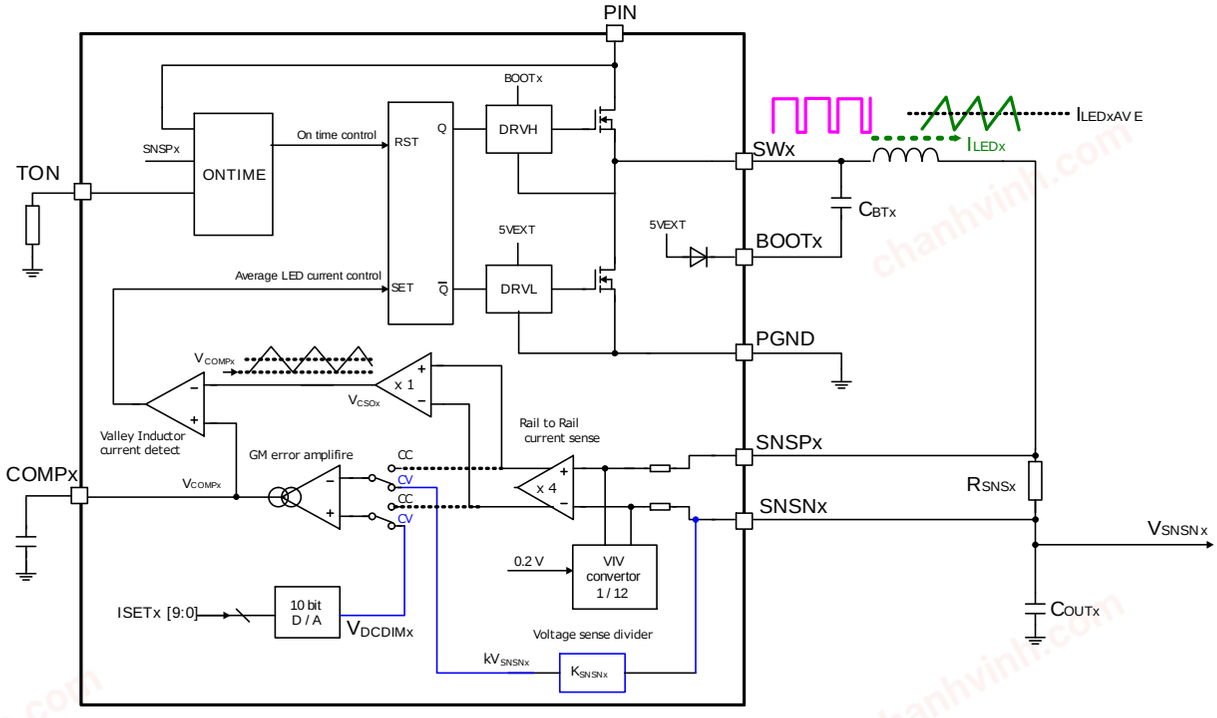


Figure 17. Buck Converter Voltage Regulation

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8 Voltage Regulation (In the LEDACTIVE Mode) - continued

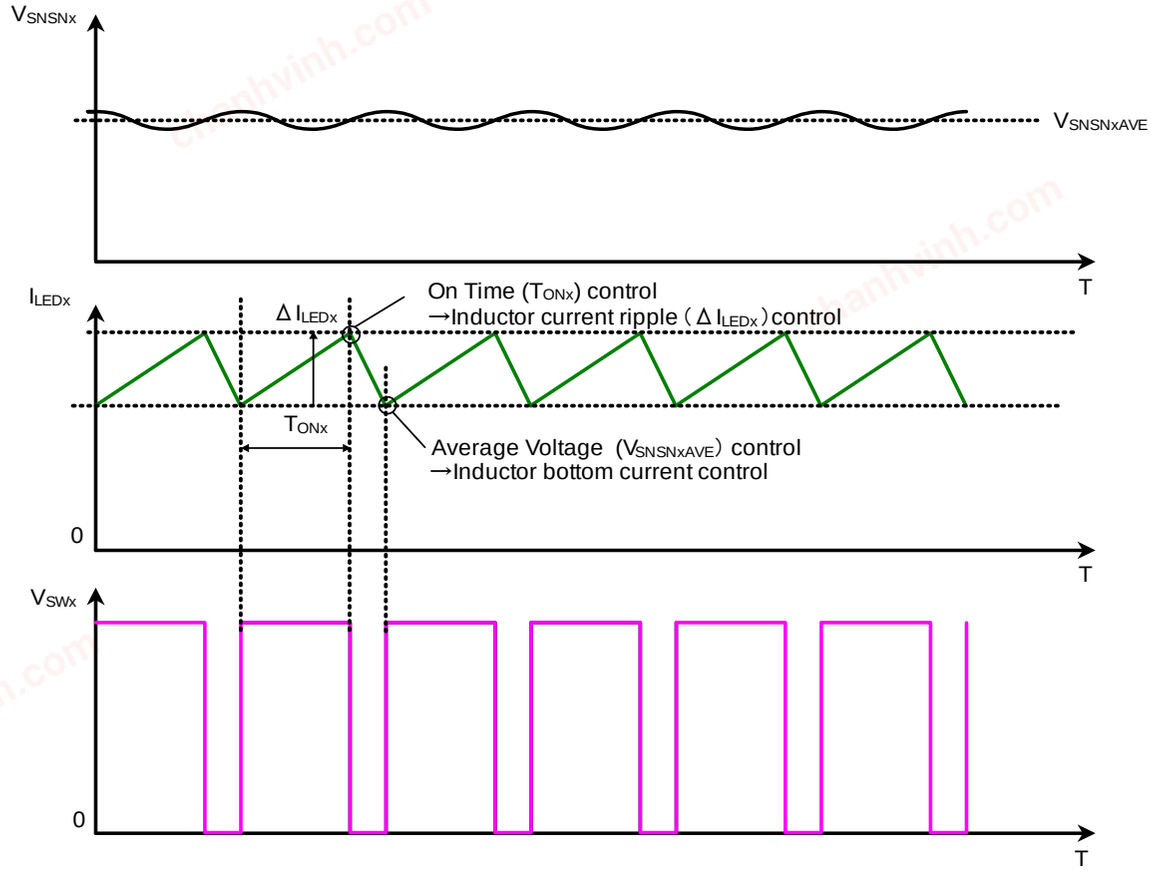


Figure 18. Buck Converter Voltage Regulation Waveforms

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Description of Blocks - continued

9 Abnormal Detection/Protection Function

Detection/ Protection Function	Detecting Condition (all the value is typical)		Description in Detecting			
	Detection	Release	Buck DCDC	Register	ADC	SO/FAULT_B Output STAND-ALONE MODE
5VREG POR	V_{5VREG} ≤ 2.7 V	V_{5VREG} ≥ 2.9 V	All channels SWx = Hi-Z	All registers initialized.	Not Available	Hi-Z
VIN UVLO	V_{IN} ≤ 4.1 V	V_{IN} ≥ 4.5 V	5VREG off All channels SWx = Hi-Z COMPx discharged	Not updated All registers will be initialized by 5VREG POR.	Not Available	Hi-Z
5VREG 5VEXT UVLO	V_{5VREG} ≤ 4.1 V or V_{5VEXT} ≤ 4.1 V	V_{5VREG} ≥ 4.2 V or V_{5VEXT} ≥ 4.2 V	All channels SWx = Hi-Z COMPx discharged	UVLO bit is set in the Status register.	Not Available	Hi-Z
PIN UVLO	V_{PIN} ≤ 4.1 V	V_{PIN} ≥ 4.5 V	All channels SWx = Hi-Z COMPx discharged	PIN UVLO bit is set in the Status register.	Not Available	Hi-Z
SWx Over Current Protection (SWOCPx)	I_{SWx} > 3.6 A	I_{SWx} < 3.6 A	Corresponding channel SWx = Pull-down COMPx discharged with Hiccup time (128 µs)	Corresponding the SWOCPERRx bit is set in the status register and will be reset after 10 ms counts by SWOCPx release.	Available	Low
LED Over Current Protection (LOCPx)	V_{SNSx} > $V_{SNSxAVE}$ + 390 mV	V_{SNSx} < $V_{SNSxAVE}$ + 390 mV	Corresponding channel SWx = Pull-down COMPx discharged.	Corresponding the LEDOCPERRx bit is set in the status register.	Available	Low
Negative LED Over Current Protection (NLOCPx)	V_{SNSx} < $V_{SNSxAVE}$ - 390 mV	V_{SNSx} > $V_{SNSxAVE}$ - 390 mV	Corresponding channel SWx = Pull-up	Corresponding the LEDOCPERRx bit is set in the status register.	Available	Low
LED Open Detection (LODx)	V_{COMPx} > 2.55 V and PWMONx = H	V_{COMPx} < 2.55 V and PWMONx = H	Continue switching.	Corresponding the LODx bit is set in the status register after 10 ms counts.	Available	Low
LED Short to ground Detection (LSDx)	V_{SNSNx} < 1.95 V	V_{SNSNx} > 1.95 V	Continue switching and common mode input range (SNSPx and SNSNx) switched to low-side-sense.	Corresponding the LSDx bit is set in the status register after 10 ms counts.	Available	Hi-Z

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Description of Blocks - continued

10 5VREG, 5VEXT

The 5VREG voltage 5.0 V (Typ) is generated from the VIN pin voltage. This voltage is used as the internal power supply of the IC. 5VEXT is external power supply input for the Gate Driver. The 5VREG can be used for connecting to the 5VEXT for the power supply. 5 V external power supply can be connecting to the 5VEXT for internal gate drive power supply to reduce power loss with high frequency switching in the device. The total current supplied for the internal gate driving should not exceed I_{5VRLM}. The current supplied to the internal gate driving per channel can be calculated by the following formula.

$$I_{FET}/channel = Q_G \times f_{SWx} = 4.8\,[nC] \times f_{SWx}$$

Where:

Q_G is the internal gate charge of the MOSFETs per channel (in case of applying V_{PIN} = 60 V).

f_{SWx} is the DC/DC switching frequency.

Connect C_{5VREG} = 4.7 µF as phase compensation capacitor to the 5VREG pin. Connect C_{5VEXT} = 4.7 µF as Coupling capacitor to the 5VEXT pin. Place ceramic capacitor close to the IC to minimize trace length to the 5VREG pin and 5VEXT pin to the IC ground. The 5VREG pin will not be used for as a power supply other than this IC.

11 Power on Reset (POR)

The BD18397/98xxx-M has a POR circuit monitoring the internal power supply output V_{5VREG}. When detecting POR, Internal all circuits and logic registers will be initialized. POR circuit main purpose is internal logic initialized in POR condition by reset signal. Between the POR detection threshold and UVLO detection threshold of the 5VREG pin, internal register values will not be reset and can be read by SPI.

12 Under Voltage Locked Out (UVLO)

The BD18397/98xxx-M has UVLO circuits monitoring the input power supplies V_{IN} for the internal reference circuits including TSD circuit and V_{5VREG} for the internal 5 V LDO output, and V_{5VEXT} for the internal gate drives and Logic and POR and analog circuits includes thermal sensor, and V_{PIN} for drain node of high-side FET and SWOCPx circuit in all channels.
When detecting a UVLO by the V_{IN} or V_{5VREG} or V_{5VEXT} or V_{PIN}, all buck DC/DC converter, including ADC convertor are immediately shutdown and all SW outputs are Hi-Z. Internal analog circuits are initialized so that all COMP pins will be discharged. When detecting a UVLO by the V_{PIN}, corresponding buck DC/DC converter is disabled immediately and SWx output is off and the COMPx pin will be discharged. When recover a UVLO, buck DC/DC converter needs wait time for start-up until the COMPx pin charged up and reach to desired inductor valley regulation voltage.

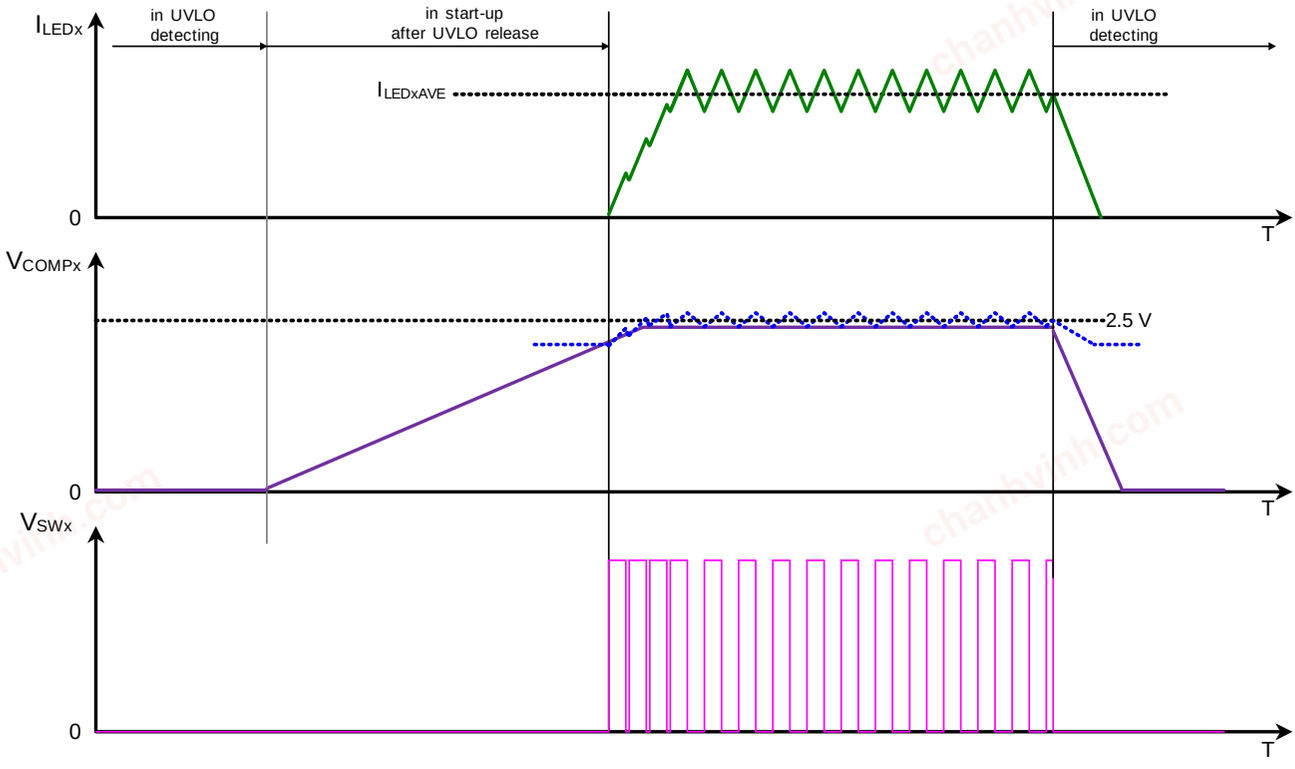


Figure 19. Buck Converter Start-up Waveform

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Description of Blocks - continued

13 Thermal Shutdown (TSD)

In case of a TSD as Tj > 175 °C (Typ), all the buck DC/DC converters will be disable immediately and Internal all circuits and logic registers will be initialized and the SO/FAULT_B pin goes low level output. When TSD recovered at Tj < 150 °C (Typ), the SO/FAULT_B pin goes high level output, the DC/DC converters will be in the SPIWAIT state until start-up sequence trigger happened.

14 SW Over Current Protection (SWOCPx)

The device has a SWOCPx circuit monitoring the output current of the SWx pin. In case of inductor peak current is not limited during the internal high side FET switched on, the internal OCP is detected when the SWx output current exceeds 3.6 A typical. The corresponding channel SWx output will be immediately switched off, and the COMPx pin will be discharged and the SWOCPERRx bit is set in status register. After recovery switching during T_{OCPRx} (10 ms) counts without detecting SWOCPx, the SWOCPERRx bit is reset (set flag latched in case of SWOCPLAT = 1).

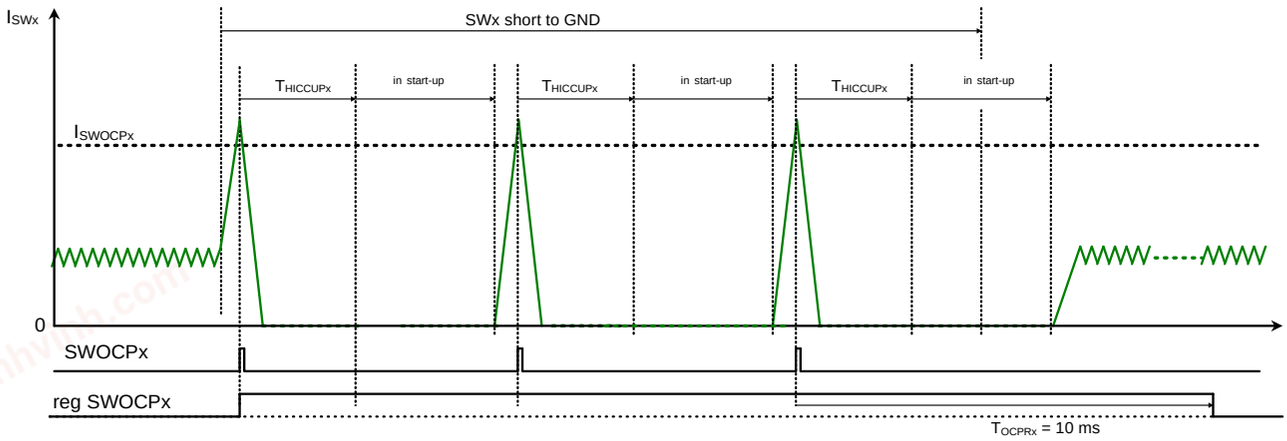


Figure 20. SW Over Current Protection Waveform

15 LED Over Current Protection and Negative LED Over Current Protection (LOCPx and NLOCPx)

The device has LOCPx and NLOCPx circuits and are monitoring LED current by output of the internal Rail-to-Rail current sense amplifier sensing differential voltage over R_{SNSx} between the SNSPx pin and SNSNx pin.
Internal LOCPx is detected when the V_{SNSx} voltage exceeds $\Delta V_{SNSxLOCP}$ (390 mV fixed value) from setting regulation voltage. The corresponding channel the SWx pin output will be immediately switched off, and the COMPx pin will be discharged until LOCPx detecting release. In detecting the LOCPx, corresponding channel of the LEDOCPERRx bit is set in status register (set flag latched in case of LEDOCPLAT = 1).
Internal NLOCPx is detected when the negative V_{SNSx} voltage exceeds $\Delta V_{SNSxNLOCP}$ (-390 mV fixed value) from setting regulation voltage. The corresponding channel the SWx pin output will be immediately switched on (cycle by cycle). In detecting the NLOCPx, corresponding channel of the LEDOCPERRx bit is set in status register (set flag latched in case of LEDOCPLAT = 1).

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Description of Blocks - continued

16 LED Open Detection

LED open detection will happen in a LED open failure, a connector to a LED's boars opened. When a LED opened, a LED current is not flowing through the shunt resistor R_{SNSx} between the SNSPx pin and SNSNx pin so that its differential average voltage $V_{SNSxAVE}$ goes zero level input for average current regulation loop. Internal average LED current regulation loop get feed-back of lower current compared with desired LED current setting. So that the internal error GM amplifier output as the COMP pin output voltage V_{COMPx} will be increased and clamp to the COMPx pin over voltage detect level $V_{COMPxSG}$. This clamp level is optimized, and clamp level is much closed to regulation DC voltage. This technology will help eliminating LED over current incase of LED open failure recovery or lower input voltage recovery. In detecting LED open, corresponding channel of the LODx bit is set in status register after t_{SNSxSG} (10 ms) counts. When LED open detect release by average current sense voltage $V_{SNSxAVE}$ goes high level, the LODx bit is reset after $t_{SNSxSGR}$ (1 ms) counts.

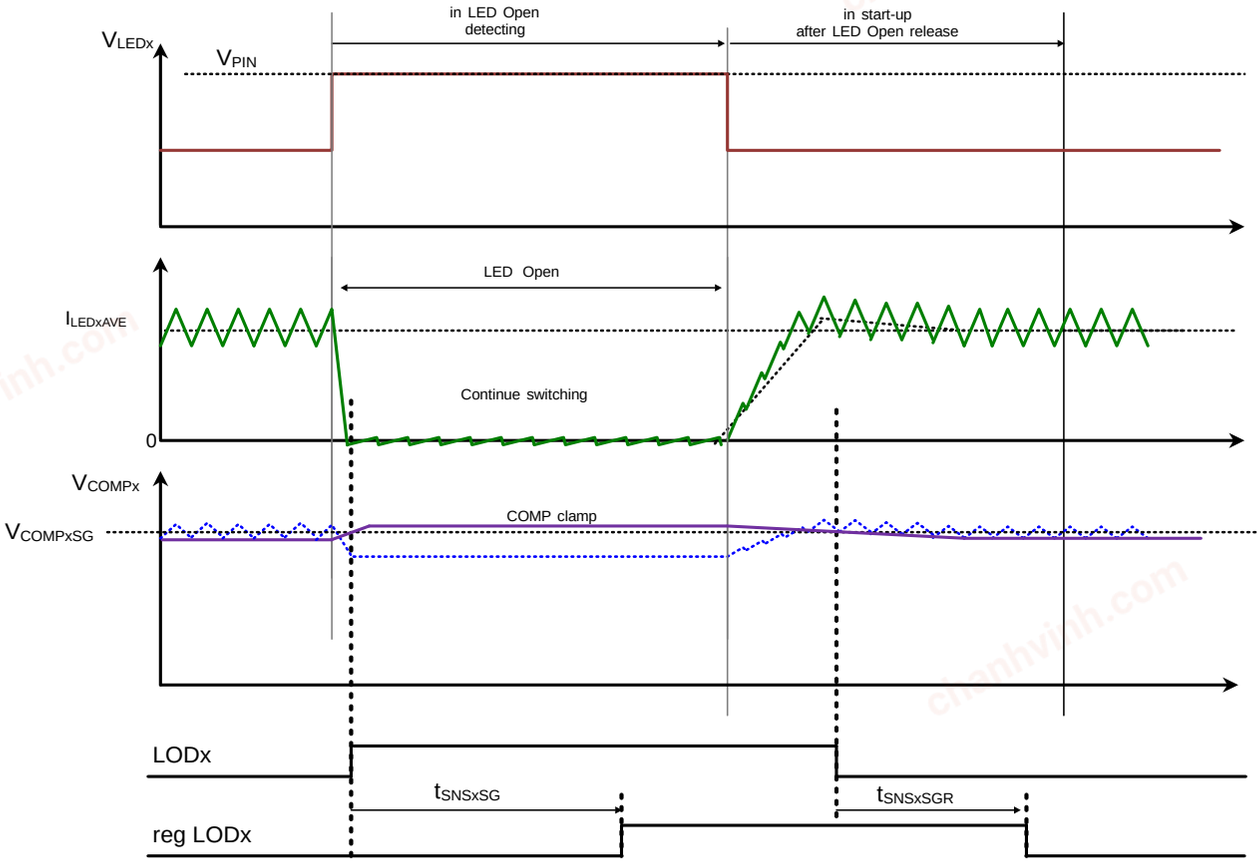


Figure 21. LED Open Detection Waveform

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Description of Blocks - continued

17 LED Short to GND Detection

LED short can be detected by a LED anode voltage at the SNSNx pin less than V_{LSDx} (1.95 V). In case of a LED short to ground condition time is more than $t_{SNSxLVD}$ (10 ms), the corresponding channel of the LSDx bit is set in status register. When a LED short to ground release by the SNSNx pin voltage higher than the V_{LSDx}, the corresponding channel of LSDx bit is reset after $t_{SNSxLVDR}$ (1 ms) counts. In a LED short to ground, the device will continue LED average current regulation and buck DC/DC on time is limited by internal minimum on time $t_{SWxONMIN}$ (90 ns) .and LED ripple current ΔI_{LED_ON} (regulated LED ON current) during $t_{SWxONMIN}$ will be higher than expected LED ripple. In addition, LED current down slope is more less than LED minimum output connecting case and the LED valley detect comparator (for sending ON signal) will wait long off time (T_{OFFx}) until inductor current going down to desired bottom (Valley) current based on regulation loop.

LED short detection is activated by corresponding channel of the CHONx bit is set in CHEN register, including PMWOFF condition so that long PWM off condition will be results in LED short detection flag set in the status register and depends on remaining output capacitor at the SNSNx pin.

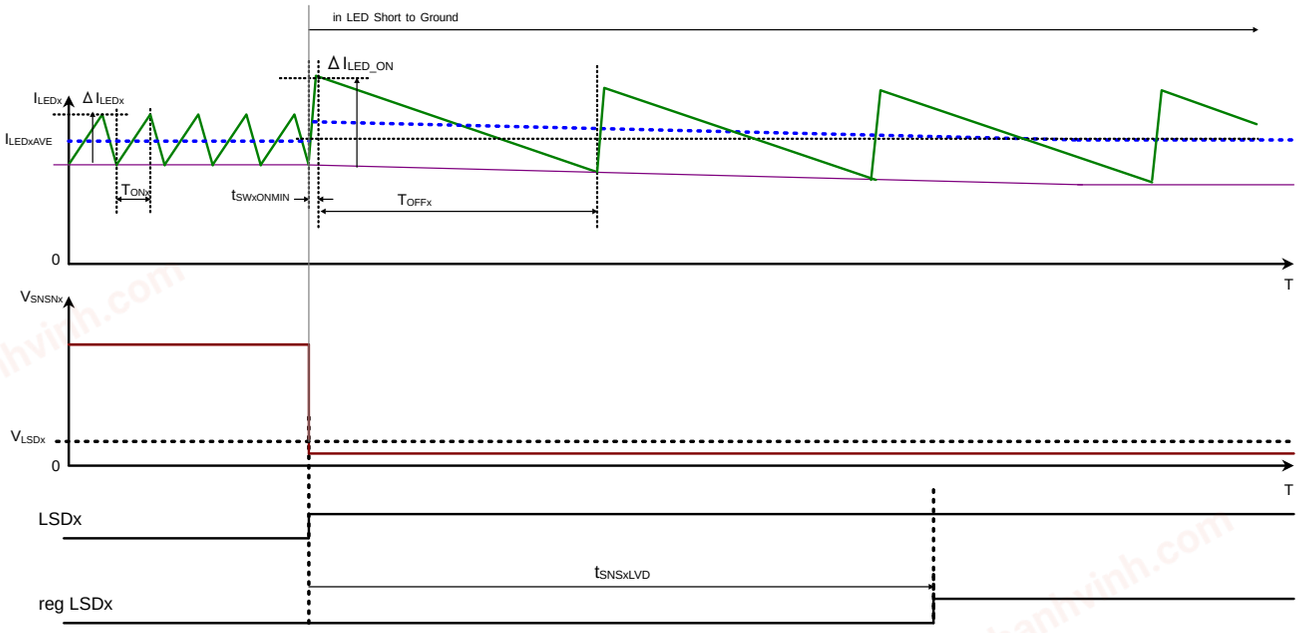


Figure 22. LED Short to GND Detection Waveform

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Description of Blocks - continued

18 State Machine

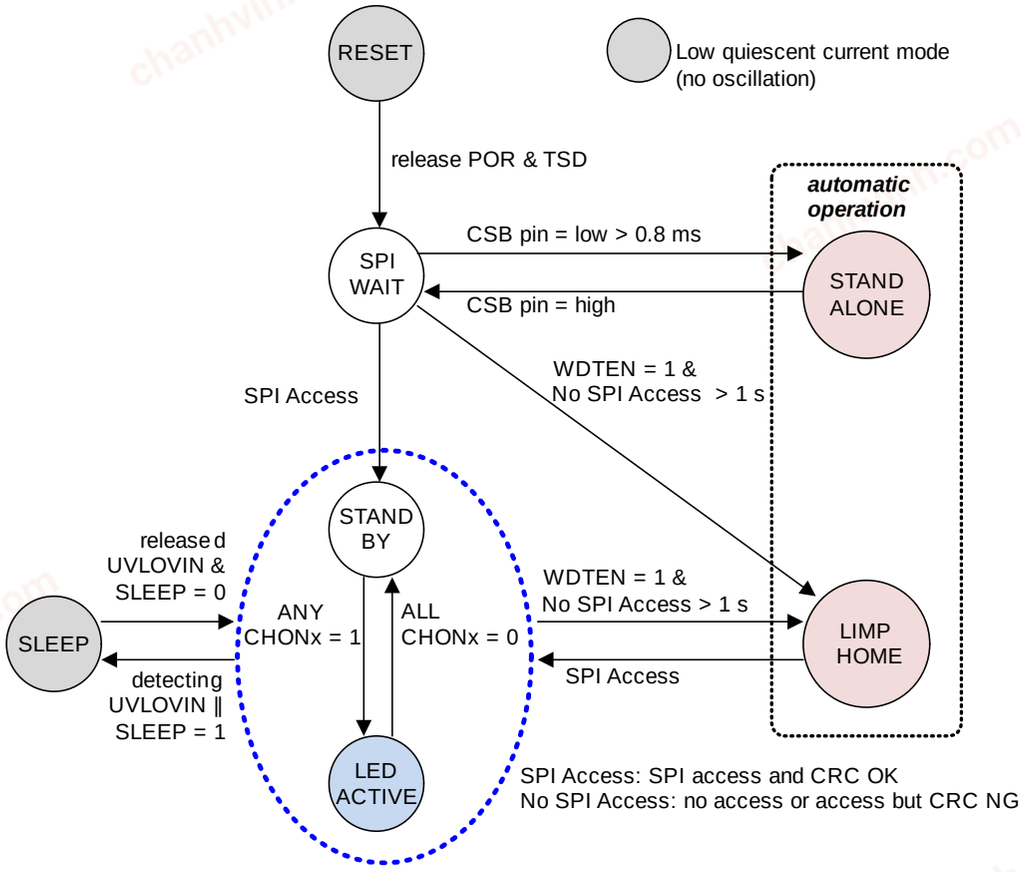


Figure 23. State Machine

Table 1. State Machine Description

State	Quiescent Current	LED Lighting	SO/FAULT_B (Operation)	Description
RESET	Low	OFF	Hi-Z	All internal block is initialized.
SPIWAIT	Normal	OFF	Hi-Z	Dimming mode is selected in this state. IC can enter STAND-ALONE mode by CSB = Low for 0.8 ms. This feature can only be used in this state. If not used, this feature can be available after POR or TSD.
STANDBY	Normal	OFF	SO	During setting register or turn off A/D conversion is available.
LEDACTIVE	Normal	Lighting (Programmed by SPI)	SO	Dimming is programmed by SPI setting. A/D conversion is available. Protection status can be checked by Register polling.
SLEEP	Low	OFF	SO	Keep Low quiescent current until SLEEP = 0. All register value is kept (not initialized).
LIMP-HOME	Normal	Lighting (Programmed by external resistor)	SO	When MCU cannot communicate with this IC, This IC keeps lighting by external resistor setting. No communication includes CRC NG SPI Communication.
STAND-ALONE	Normal	Lighting (Programmed by external resistor)	FAULT_B	When CSB = Low for 0.8 ms, This IC keeps lighting by external resistor setting. Protection can be checked by monitoring SO/FAULT_B = Low.

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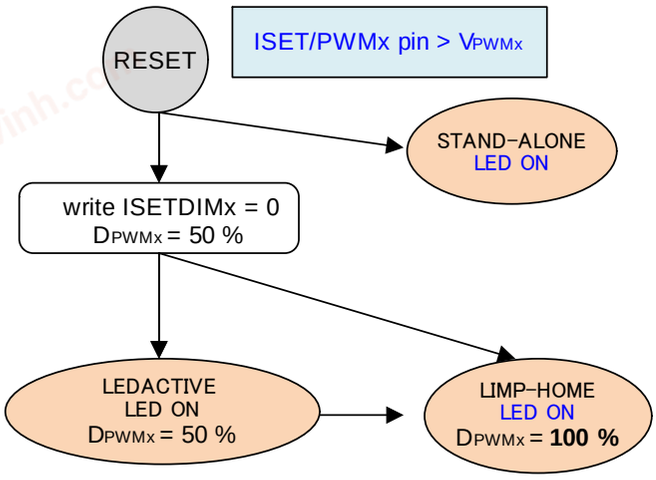
18 State Machine - continued

Table 2. State Machine Description for Dimming

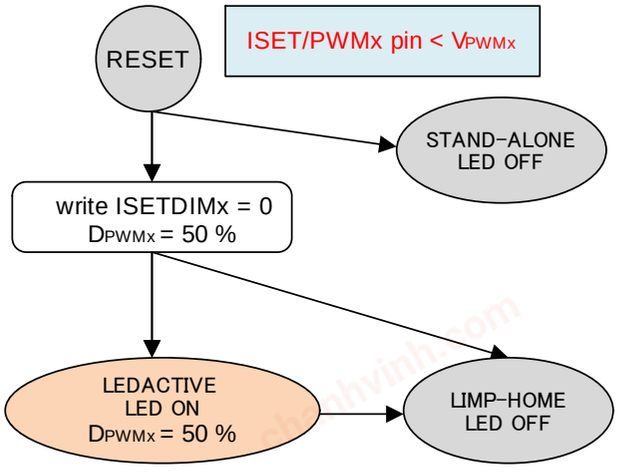
State	ISETDIM (Register)	LED Lighting	LED Current Setting	PWM Dimming Setting
RESET	0	OFF	-	-
SPIWAIT	0		-	-
STANDBY	0/1		-	-
LEDACTIVE	0	Lighting	ISETx[9:0] register	DPWMx[9:0] register
	1			DPWMx[9:0] register & ISET/PWMx pin
SLEEP	0/1	OFF	-	-
LIMP HOME	0/1	Lighting/OFF	ISETx[9:0] register & ISET/PWMx pin	ISET/PWMx pin
STAND-ALONE				

*ISETDIMx initial value = 0

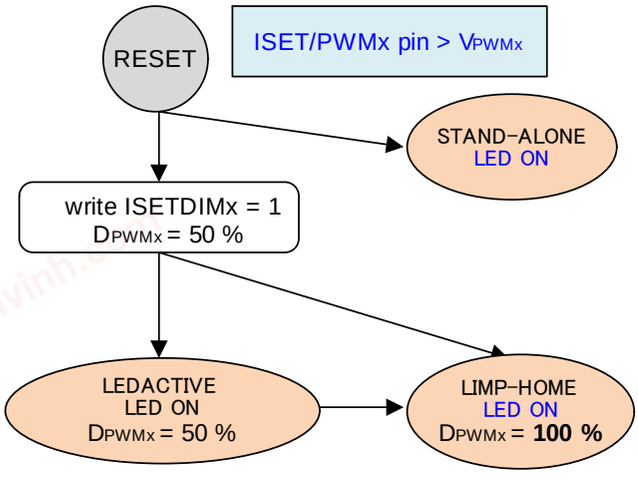
Ex1.) LED ON in LIMP-HOME/STAND-ALONE with ISETDIMx = 0



Ex2.) LED OFF in LIMP-HOME/STAND-ALONE with ISETDIMx = 0



Ex3.) LED ON in LIMP-HOME/STAND-ALONE with ISETDIMx = 1



Ex4.) LED OFF in LIMP-HOME/STAND-ALONE with ISETDIMx = 1

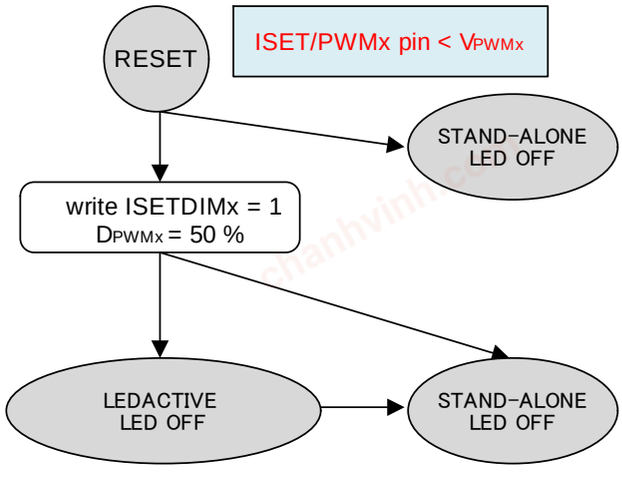


Figure 24. Example of Operation Flow

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Description of Blocks - continued

19 SPI Protocol and AC Electrical Characteristics

This IC can be accessed via SPI using CSB, SCK, SI, SO/FAULT_B terminals as shown in.

CSB	– Chip Select
SCK	– Serial Clock
SI	– Serial Data input
SO/FAULT_B	– Serial Data output

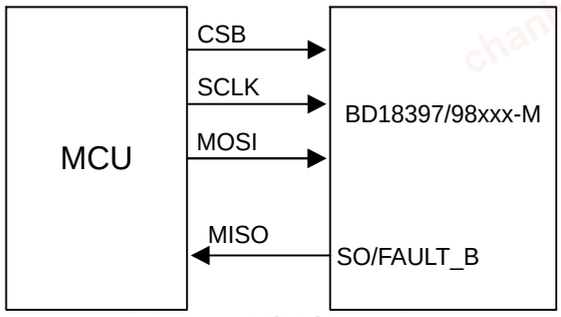


Figure 25. MCU Connection

Select the IC to be accessed by setting the CSB to low. Send the data based on the format as shown in. Data to be sent follow a MSB first 24-bit data format for write: 1-bit RW (read or write), 7-bit register address, 8-bit register data (to be written) and 8-bit CRC. SPI can be accessed in daisy chain connection or parallel connection. There is no multiple bytes write/read feature. After each command, fix SI to low and CSB to high. SI data is outputted with 24 bits shift from SO/FAULT_B. SO/FAULT_B keeps Hi-z when CSB = high.

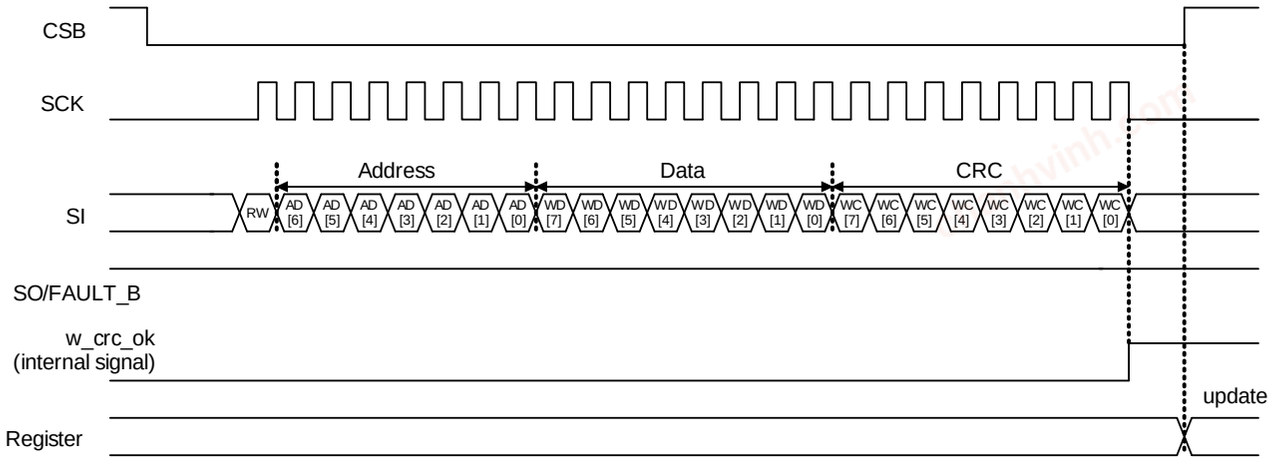


Figure 26. Data Format (Write)

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19 SPI Protocol and AC Electrical Characteristics - continued

Read Command data format is sent as follows: 1-bit RW, 7-bit register address, fixed 0xFF for register data and 8-bit CRC.
When CRC is OK (w_crc_ok = high) after the Read command as shown in, it is necessary to toggle CSB (low -> high -> low) to store the read data.
To output the data, it is necessary to send 24-bit High input data (Dummy Data).
MCU must calculate CRC using 0 as initial value.
For input data: use 16-bit data for calculation. 16-bit data = (RW, Address[6:0], Data[7:0])
For output data: use 15-bit data for calculation.
<RDMODE = 0> 15-bit data = (Address[6:0], Data[7:0]) Not including MSB.
<RDMODE = 1> 15-bit data = (5-bit (blank data), Data0[7:0], Data1[1:0]) Not including MSB.

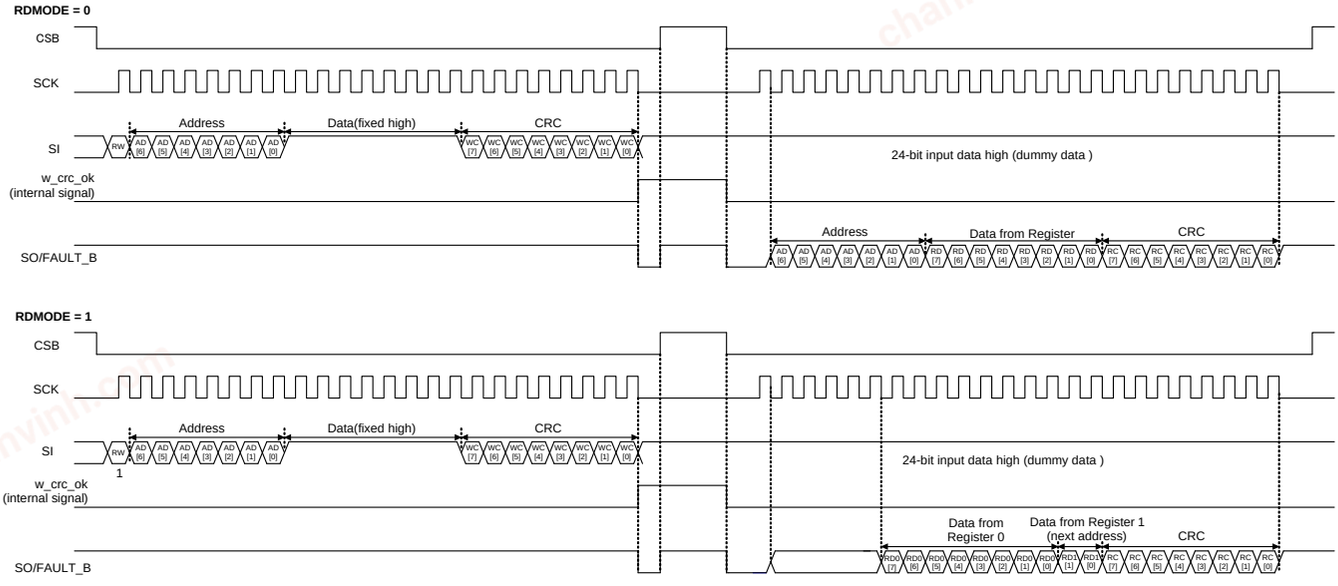


Figure 27. Data Format (Read)

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19 SPI Protocol and AC Electrical Characteristics - continued

SPI AC Timing

SPI AC characteristics is as shown in.

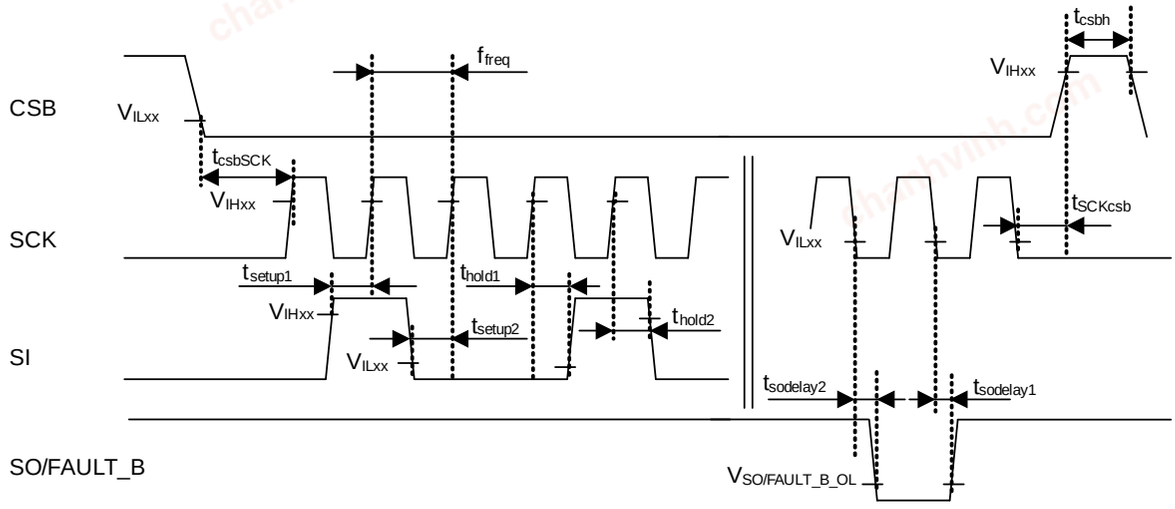


Figure 28. SPI AC Timing

Table 3. SPI AC Timing

Recommended Operation Condition

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = -40 °C to +150 °C)

Item	Symbol	Unit	Min	Typ	Max
SPI Frequency	f_{freq}	MHz	0.1	-	1.0
CSB - SCK Timing	t_{csbSCK}	ns	1,000	-	-
SCK - CSB Timing	t_{SCKcsb}	ns	500	-	-
Setup Time1 (low -> high)	t_{setup1}	ns	200	-	-
Setup Time2 (high -> low)	t_{setup2}	ns	200	-	-
Hold Time1 (low -> high)	t_{hold1}	ns	200	-	-
Hold Time2 (high -> low)	t_{hold2}	ns	200	-	-
SO Delay (low -> high)	$t_{sodelay1}$	ns	-	-	200
SO Delay (high -> low)	$t_{sodelay2}$	ns	-	-	200
CSB High Pulse	t_{csbh}	ns	1,000	-	-

(Output load capacitance: 15 pF)

NOTE (Countermeasure of Noise)

The CSB is used for resetting, clock and enable in SPI and register circuit. If this signal includes glitch around CSB to "high -> low" by communication path noise, internal noise or more, SPI mistake to operate register. Because this condition is not approved in this product. But there is countermeasure for this issue. SPI receives at least one SCK clock pulse (maximum clock pulse is no limitation) during CSB = high after writing data until next writing command. This SPI can protect this wrong operation. Because register return to "no update condition" with SCK clock during CSB = high.

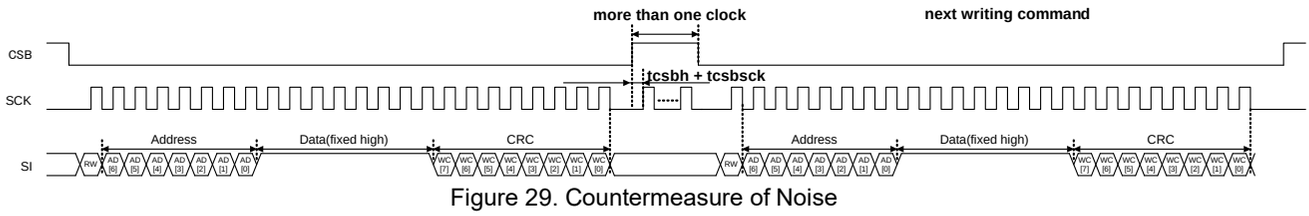


Figure 29. Countermeasure of Noise

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19 SPI Protocol and AC Electrical Characteristics - continued

SPI Protocol

Write/Read, Address

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RW	AD[6:0]						

bit	Parameter	Function
AD[6:0]	Register Address	0x00 to 0x1B

Note: There is no access to addresses that are not between the specified range.

bit	Parameter	Function
RW	Read/Write	0: read access 1: write access

Data

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WD/RD[7:0]							

bit	Parameter	Value
WD/RD[7:0]	Data of Write/Read	0x00 to 0xFF

CRC

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WC/RC[7:0]							

bit	Parameter	Value
WC/RC[7:0]	CRC data of Write/Read	0x00 to 0xFF

This IC has a CRC (cyclic redundancy check) function for detecting errors in the SPI communication.
CRC for write command is calculated using RW bit, 7-bit register address and 8-bit register data and is calculated MSB first.
Read output is calculated the same.
CRC formula is" $x^8+x^5+x^4+1$" which is translated as the circuit as shown in. Initial value of CRC is 0x00.
(It doesn't change value until '1' input because initial 0. (The result of "011111111111111111111111" (binary) is same as result of "111111111111111111111111".))

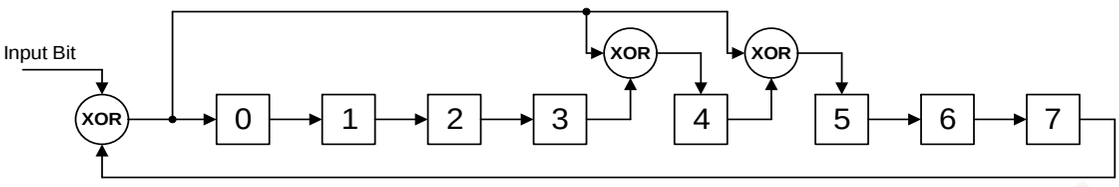


Figure 30. CRC Circuit

NOTE (SPI Restrictions):
Command with the following input is not valid RW = 0, Address = 0x00, Data = 0x00, CRC = 0x00.
SPI will not execute the read command it is treated as dummy and will only shift the input by 24-bit.

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SPI Protocol – continued

SPI Protocol – Daisy-chain Connection

This IC has daisy chain function for SPI communication. Total of 8 devices can be connected in daisy-chain as shown in. Select the device address by controlling CSB input see.

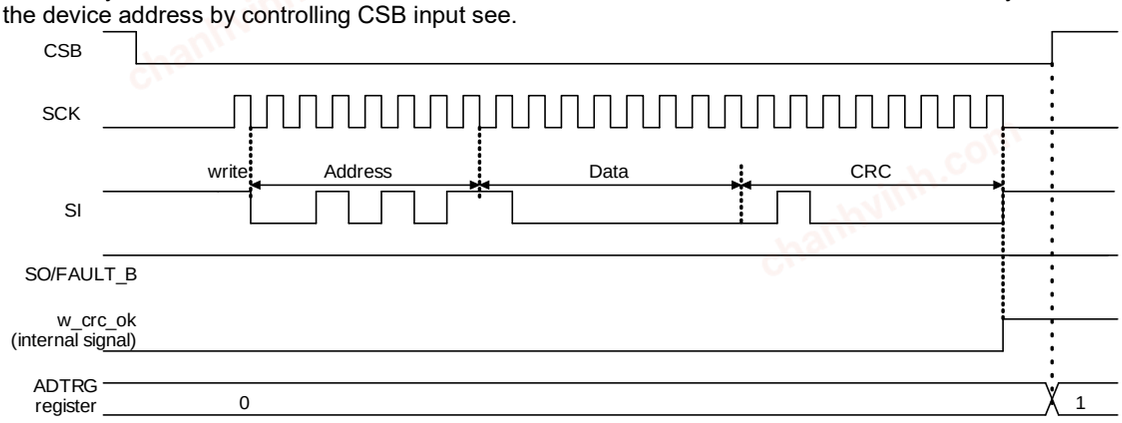


Figure 31. Example of Daisy-chain

When there is a total of N number of devices in the daisy-chain and M is the target device to be written/read, to execute write command, it is necessary to input dummy data (M - 1) to propagate the write command to the desired device in a daisy-chain connection as shown in.

N – Total number of devices connected in daisy-chain
M – Target device to be written/read

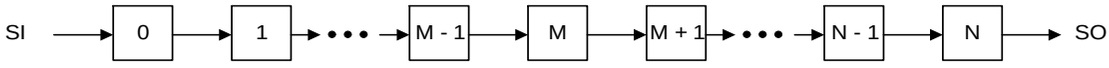


Figure 32. Data Input Image in a Daisy-chain Connection

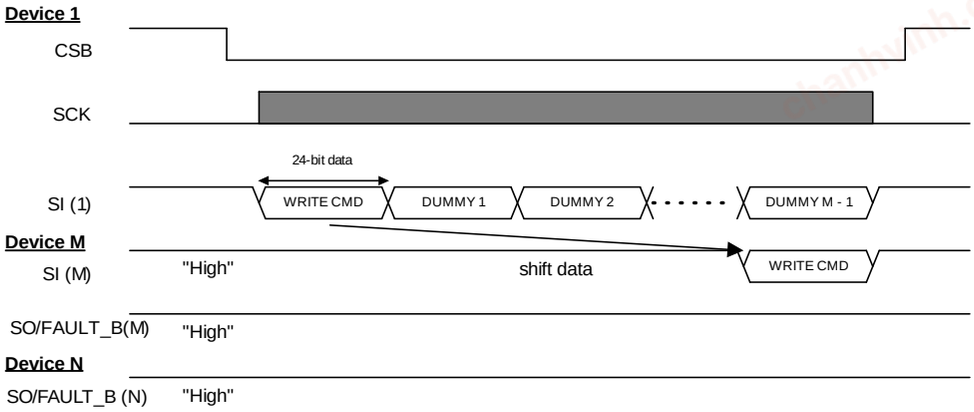


Figure 33. SPI Write in Daisy-chain Connection

Likewise, in Read command, it is necessary to input dummy data (M-1) to propagate the read command to the desired device toggle CSB and input the rest of the dummy data (total of N dummy data) to propagate the Read data output up to the last device in the daisy chain connection. Dummy is 24-bit low data input.

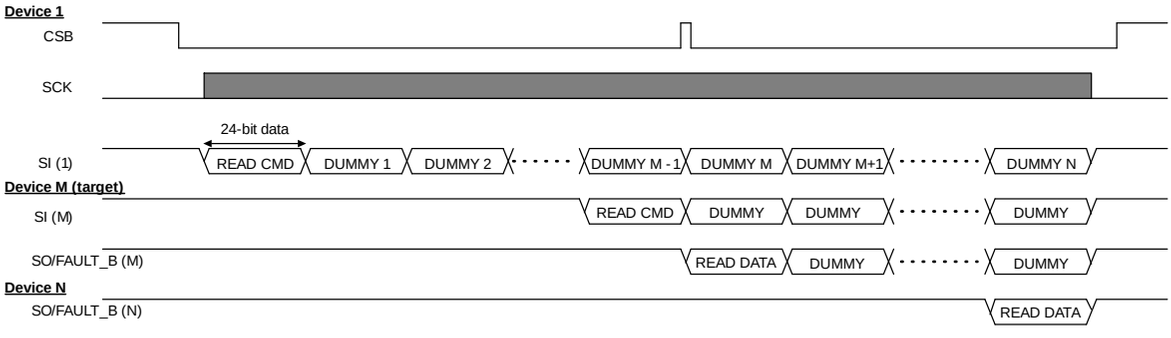


Figure 34. SPI Read in Daisy-chain Connection

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SPI Protocol – Daisy-chain Connection – continued

In Daisy-chain connection, writing to multiple devices is possible; refer to the timing chart. In this SPI transaction, Set CSB to “low”, send the write command consecutively for the target devices starting from Target device M up to Dev 1, Set CSB to “high” to trigger writing to the target registers in the corresponding device number.

N – Total Device in Daisy-chain connection
Dev M to Dev 1 – Target Device to be written (Dev M is between Dev N and Dev 1)

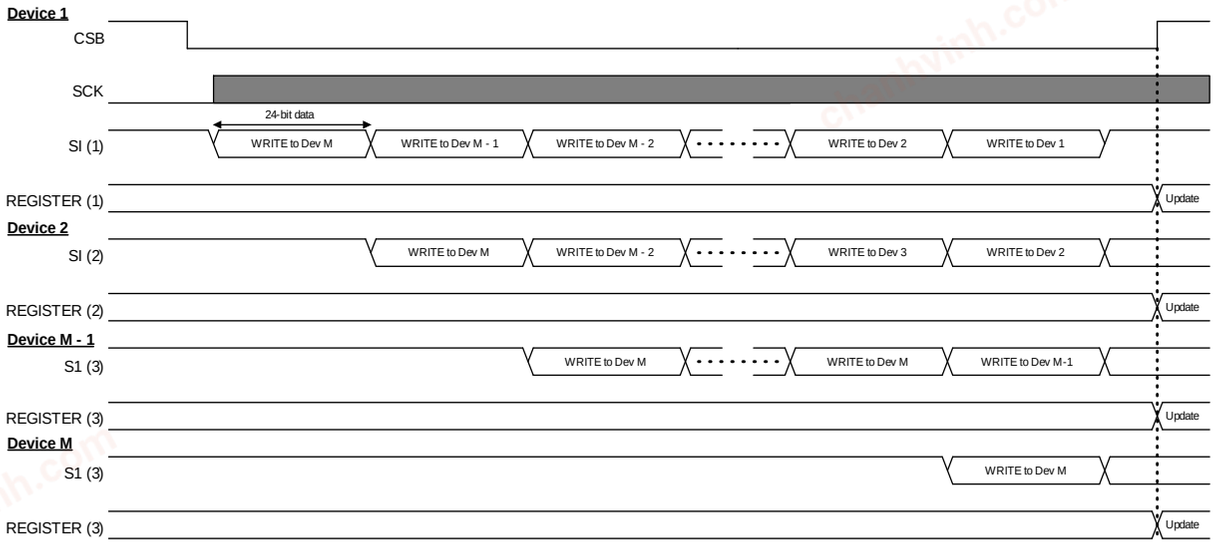


Figure 35. Writing Protocol for Multiple Devices

Reading for multiple devices is also possible in a daisy-chain connection; refer to the timing chart. In this SPI Transaction, Set the CSB to “low”, send the Read Command consecutively starting from target Device M up to Device 1, toggle the CSB to “low -> high -> low”, send total DUMMY data based on total Number of devices (N). It is necessary to input this much DUMMY data to be able to propagate the Read Data output up to the last device in the daisy chain connection.

N – Total Device in Daisy-chain connection
Dev M to Dev 1 – Target Device to be read (Dev M is between Dev N and Dev 1)

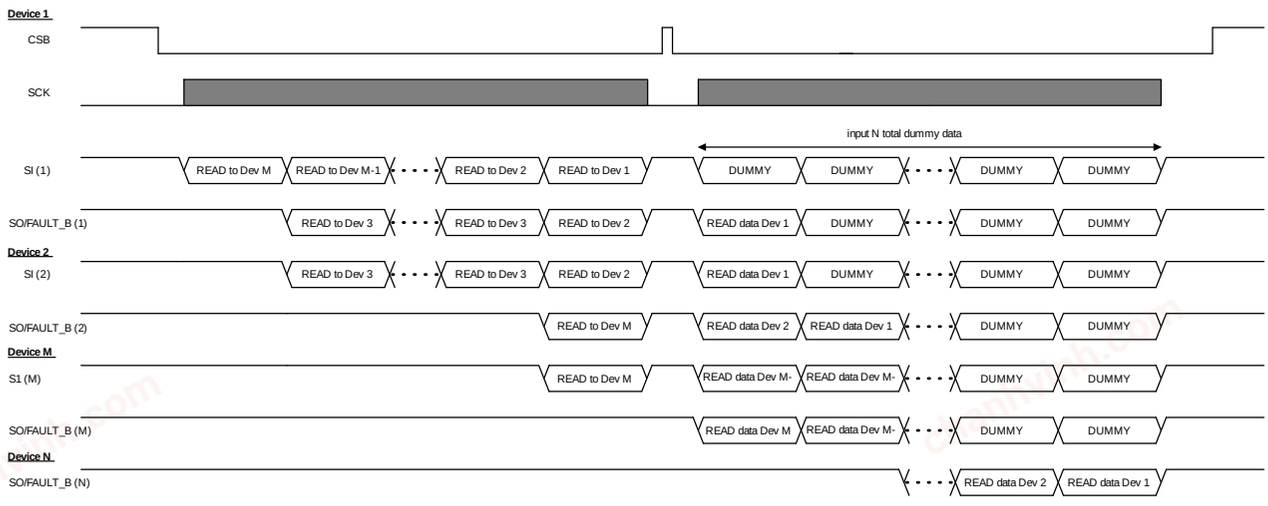


Figure 36. Reading Protocol for Multiple Devices

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SPI Protocol – Daisy-chain Connection – continued

Example 1)
Writing data for 1 device
Address = 0x15 (ADTRG)
Data = 0x80
CRC = 0x40

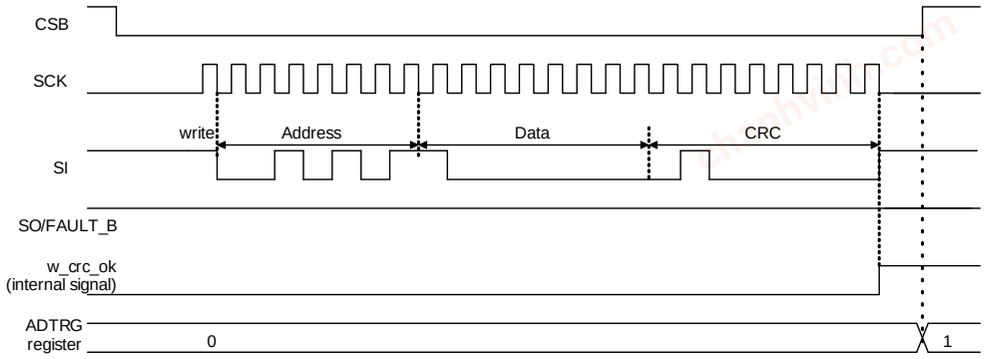


Figure 37. SPI Protocol of the 1 byte Write to Device #1

Example 2)
Reading data for 1 device (RDMODE = 1)
Address = 0x16 (VMON)
Data = 0xFF (dummy)
CRC = 0x98 (MCU -> this device)

Read data = 0x05
CRC = 0x59 (this device -> MCU)

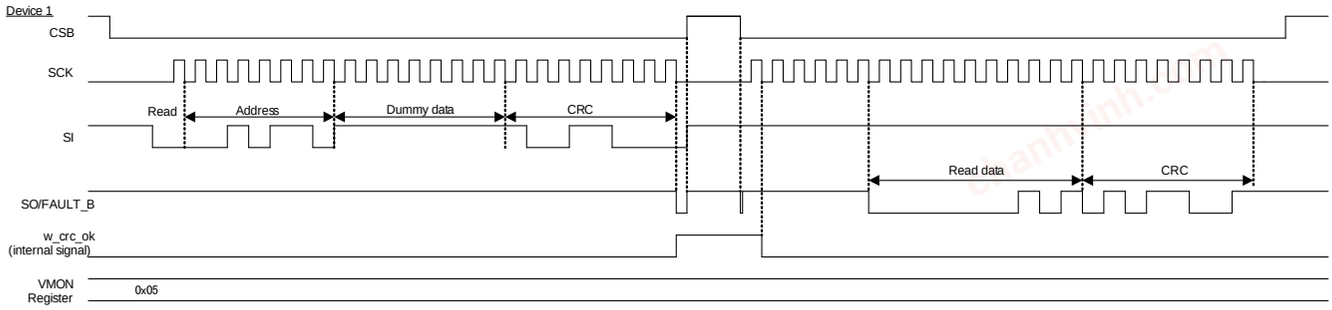


Figure 38. SPI Protocol of the 1 byte Read to Device #1

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SPI Protocol – continued

SPI Protocol – Parallel Connection

This IC can be connected in Parallel for SPI connection as shown in. In this connection, each device has separate CSBx. SI and SO connection are shared. User can choose which DUT to write based on CSBx as shown in.

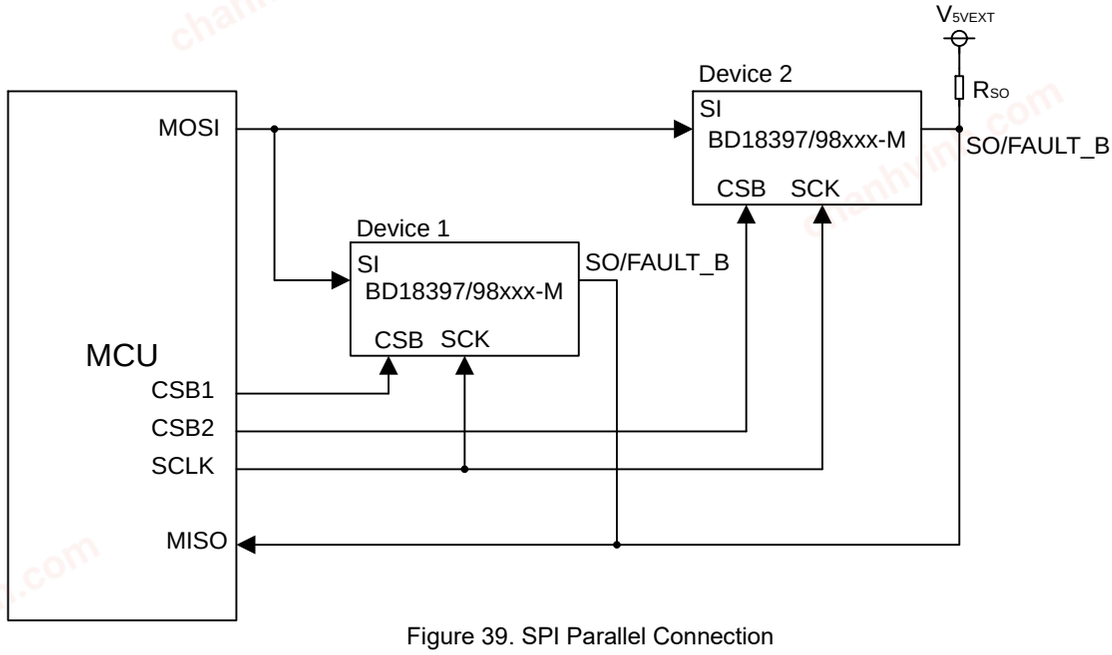


Figure 39. SPI Parallel Connection

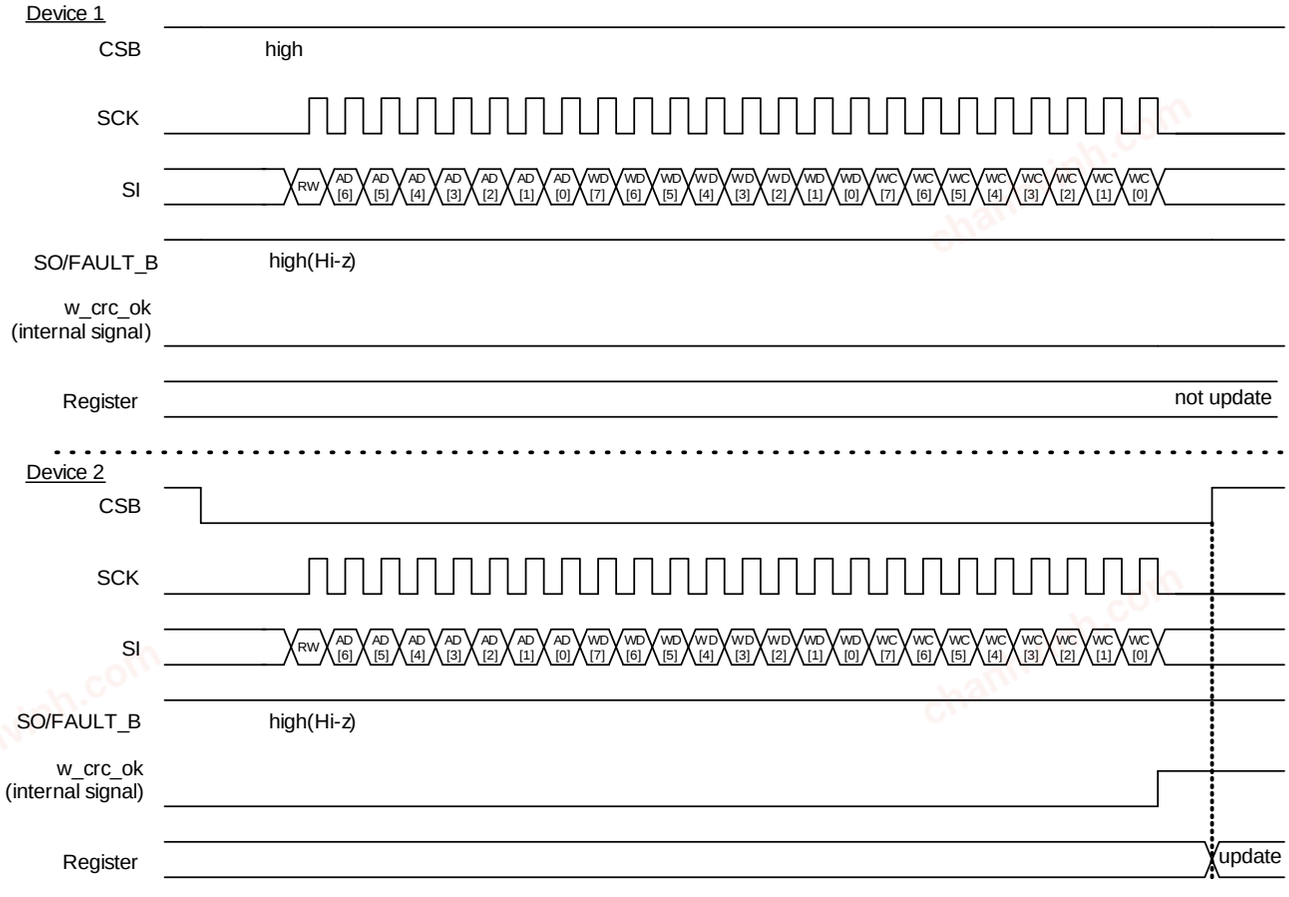


Figure 40. SPI Write to Device #2 in Parallel Connection

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SPI protocol – Parallel Connection – continued

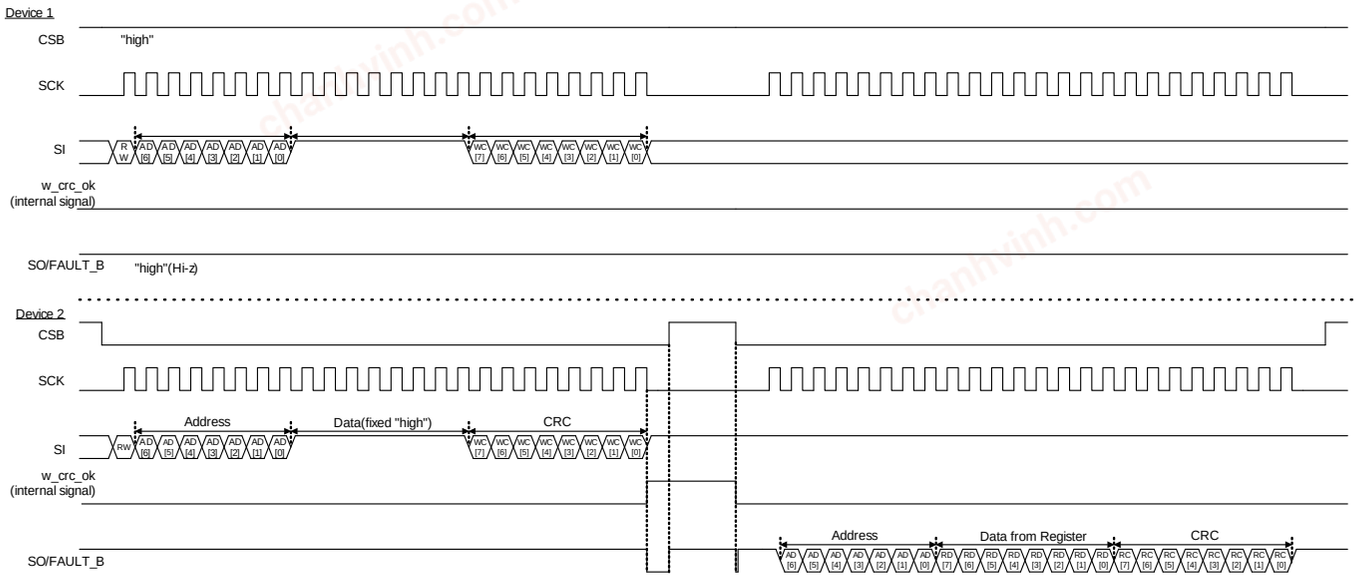


Figure 41. SPI Read to Device #2 in Parallel Connection

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20 Register

Register MAP(Address 0x00 to 0x1B)
This is register MAP of BD18398xxx-M. The channel 3 setting is not included in BD18397xxx-M. (ex, ISETSDIM3, VMODE3, CHON3, ERRDET3, address 0x08-0x09, 0x0E to 0x0F, 0x12, 0x1B), These registers is blank (0x00). If you read these data, it returns 0.

RegisterName	Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Register Access	initial	comments
SYSSET	0x00	WLOCK	WDTEN	RDMODE	SLEEP	-	-	-	SWRST	R/W	0x40	register access control sleep setting, software reset NOTE : POR/TSD for reset of SWRST
-	0x01	-	-	-	-	-	-	-	-	-	-	Not used
ERRSET1	0x02	-	-	-	-	-	FLTRST	LEDOCPLAT	SWOCPLAT	R/W	0x00	protection latch setting and latch released setting
DMSET	0x03	PHEN	PWMDMV[2:0]			-	ISETDM3	ISETDM2	ISETDM1	R/W	0x00	ISET setting selection, output PWM frequency setting, setting of Phase shift
ISET1H	0x04	ISET1[9:2]								R/W	0xE1	Current setting for channel1
ISET1L	0x05	-	-	-	-	-	-	ISET1[1:0]		R/W	0x01	Current setting for channel1
ISET2H	0x06	ISET2[9:2]								R/W	0xE1	Current setting for channel2
ISET2L	0x07	-	-	-	-	-	-	ISET2[1:0]		R/W	0x01	Current setting for channel2
ISET3H	0x08	ISET3[9:2]								R/W	0xE1	Current setting for channel3
ISET3L	0x09	-	-	-	-	-	-	ISET3[1:0]		R/W	0x01	Current setting for channel3
DPWM1H	0x0A	DPWM1[9:2]								R/W	0xFF	PWM ON Duty for channel1
DPWM1L	0x0B	-	-	-	-	-	-	DPWM1[1:0]		R/W	0x03	PWM ON Duty for channel1
DPWM2H	0x0C	DPWM2[9:2]								R/W	0xFF	PWM ON Duty for channel2
DPWM2L	0x0D	-	-	-	-	-	-	DPWM2[1:0]		R/W	0x03	PWM ON Duty for channel2
DPWM3H	0x0E	DPWM3[9:2]								R/W	0xFF	PWM ON Duty for channel3
DPWM3L	0x0F	-	-	-	-	-	-	DPWM3[1:0]		R/W	0x03	PWM ON Duty for channel3
DCDCSET1	0x10	GM1[1:0]		TON1[5:0]						R/W	0x07	switching frequency setting for channel1 vary current detector ripple gain
DCDCSET2	0x11	GM2[1:0]		TON2[5:0]						R/W	0x07	switching frequency setting for channel2 vary current detector ripple gain
DCDCSET3	0x12	GM3[1:0]		TON3[5:0]						R/W	0x07	switching frequency setting for channel3 vary current detector ripple gain
DCDCSET4	0x13	-	VMODE3	VMODE2	VMODE1	-	SSCG[2:0]			R/W	0x00	SSCG setting, Voltage mode setting
CHEN	0x14	-	PWMDIM3	PWMDIM2	PWMDIM1	-	CHON3	CHON2	CHON1	R/W	0x00	DC/DC enable, PWM Dimming enable
ADSEL	0x15	ADTRG	-	-	ADMODE	VMONSEL[3:0]				R/W	0x10	VIN, PIN, V_{5VEXT}, V_{SNSN1}, V_{SNSN2}, V_{SNSN3}, thermal, ISET1, ISET2, ISET3 voltage monitor, A/D converter trigger in manual mode
VMONH	0x16	VMON[9:2]								RO	0x00	Voltage monitor by A/D.
VMONL	0x17	-	-	-	-	-	-	VMON[1:0]		RO	0x00	Voltage monitor by A/D.
ERRSTALL	0x18	WDTERR	CRCERR	PNUVLO	UVLO	-	ERRDET3	ERRDET2	ERRDET1	RO	0x00	Error status register total
ERRST1	0x19	-	-	-	-	LEDOCPERR1	SWOCPERR1	LOD1	LSD1	RO	0x00	Error status register LED open error, LED short error SWOCP1, LOCP1
ERRST2	0x1A	-	-	-	-	LEDOCPERR2	SWOCPERR2	LOD2	LSD2	RO	0x00	Error status register LED open error, LED short error SWOCP2, LOCP2
ERRST3	0x1B	-	-	-	-	LEDOCPERR3	SWOCPERR3	LOD3	LSD3	RO	0x00	Error status register LED open error, LED short error SWOCP3, LOCP3

WO: Write Only, RO: Read Only, R/W: Read and Write
SWRST register reset condition is POR/TSD. All other registers reset condition is POR/TSD/SWRST.
(Note 1) SWRST, FLTRST and ADTRG are “write only”, and reset condition of SWRST is only “POR/TSD”.

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20 Register - continued

Description of Registers

●Address 0x00: SYSSET System setting [Read/Write] initial value 0x40

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	WLOCK	WDTEN	RDMODE	SLEEP	-	-	-	SWRST
Initial value	0	1	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting.

bit[0] SWRST
SWRST register return '0' automatically. Hence, this register is "Write only".
Set this register when you want to reset digital circuit.

Table 4. SWRST Operation

SWRST	Reset
0	Normal
1	Reset for digital circuit (return '0' automatically)

bit[4] SLEEP
This IC has sleep mode which stops internal clock, so this IC is in low "quiescent current" condition. This IC keeps register value when SLEEP = 1.

Table 5. SLEEP Operation

SLEEP	Operation
0	Normal
1	Low "quiescent current" condition. Oscillator is stopped. So, DC/DC and Current Driver are OFF. Only internal regulator is available.

bit[5] RDMODE
This register controls Read protocol. If RDMODE = 1, it outputs Read Data (target address 8-bit + next address bit[1:0]). The detail of protocol can be referred in "SPI Protocol" section.

Table 6. RDMODE Operation

RDMODE	Operation
0	Outputs target address data
1	Outputs target address data + next address data bit [1:0]

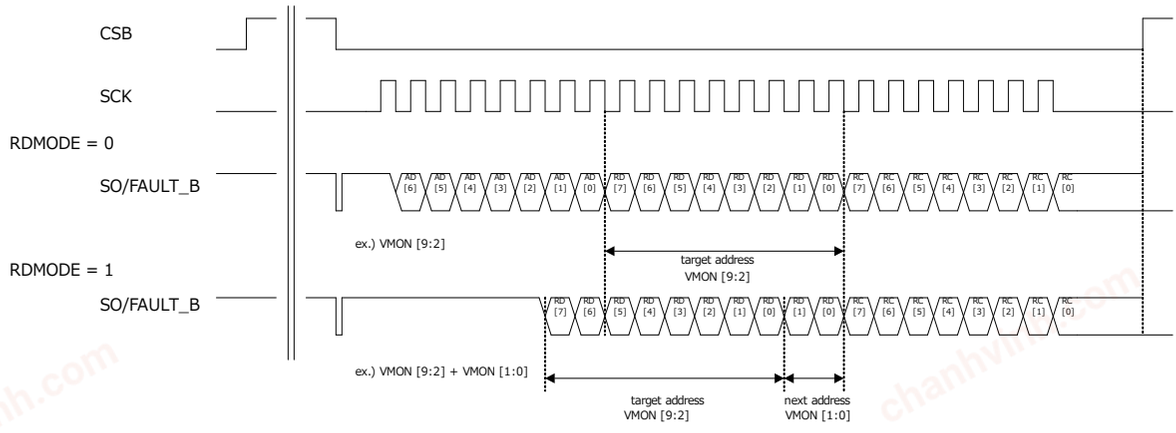


Figure 42. RDMODE Operation

bit[6] WDTEN
This register is "Watchdog timer" function enable. If WDTEN = 1, LIMP-HOME function is available by "Watch Dog Timer error" when state is "LEDACTIVE" or "STANDBY".

Table 7. "Watch Dog Timer" Enable

WDTEN	Enable
0	"Watch Dog Timer" is not available
1	"Watch Dog Timer" is available

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Description of Registers – continued

bit[7] WLOCK

DPWMx registers are split into two registers (higher and lower byte). Normally, whenever a byte (higher or lower) is written, it will immediately be reflected in PWM dimming control. If WLOCK function is used, PWM dimming control will not be updated until the two bytes (higher and lower) are written.
Note that it doesn't matter whether the higher or lower byte is written first.

Table 8. WLOCK Function

WLOCK	Operation
0	Normal update
1	PWM dimming control is not updated until writing the other address. (0x0A to 0x0F)

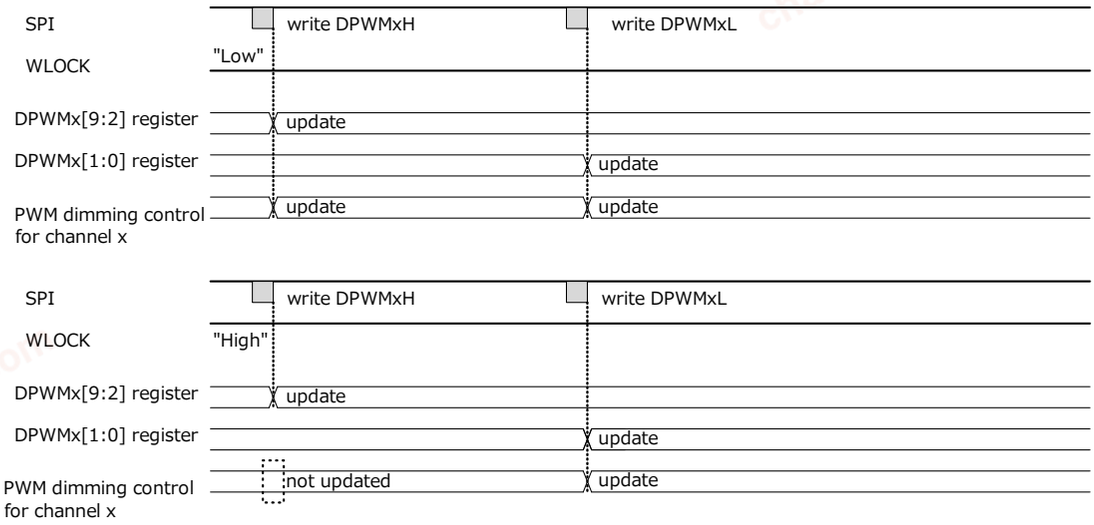


Figure 43. WLOCK Function Example

●Address 0x01: Not Used

●Address 0x02: ERRSET1 protection setting [Read/Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	-	-	FLTRST	LEDOCPLAT	SWOCPLAT
Initial value	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting.

bit[0] SWOCPLAT

The releasing function of “SWx over current error protection” is programmed by this register. If SWOCPLAT = ‘1’, The SWOCPERRx register doesn't become '0' until writing FLTRST = '1'. If SWOCPLAT = '0', The SWOCPERRx becomes '0' by "SWx over current error" released.

Table 9. “SWx Over Current error protection” Latch Operation Setting

SWOCPLAT	Operation
0	If this error condition is released, error status register and FAULT_B returns normal condition.
1	This IC keeps error condition until writing FLTRST = 1.

(x = 1, 2, 3)

bit[1] LEDOCPLAT

The releasing function of “LED over current error protection” is programmed by this register. If LEDOCPLAT = ‘1’, The LEDOCPERRx register doesn't become '0' until writing FLTRST = '1'. If LEDOCPLAT = '0', The LEDOCPERRx becomes '0' by "LED over current error" released.

Table 10. “LED Over Current error protection” Latch Operation Setting

LEDOCPLAT	Operation
0	If this error condition is released, error status register and FAULT_B returns normal condition.
1	This IC keeps error condition until writing FLTRST = 1.

(x = 1, 2, 3)

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Description of Registers – continued

bit[2] FLTRST
The error status registers are initialized by this register. If each protection is latched, its condition is released.

Table 11. Error Status Reset

FLTRST	Operation
0	Normal
1	Initialize error status for LEDOCPERRx and SWOCPERRx, CRCERR and WDTERR. This register is auto return to “0” (Address 0x19 to 0x1B)

(x = 1, 2, 3)

●Address 0x03: DIMSET Dimming setting [Read/Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	PHEN	PWMDIV[2:0]			-	ISETDIM3	ISETDIM2	ISETDIM1
Initial value	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting.

bit[2:0] ISETDIMx (ISETDIM3 is only used for the BD18398xxx-M)
This register selects the LED DC current setting data for channel x (x = 1, 2, 3). If ISETDIMx = 1, the ISETx pin setting is available. If ISETDIMx = 0, LED DC current is programmed by ISETx register.

Table 12. ISET Select

ISETDIMx	PWMONx Definition	ADC Monitor Select
0	LED DC current is programmed by ISETx[9:0] register	Selected by corresponding VMONSEL [3:0] bit setting
1	LED DC current is programmed by ISETx[9:0] & ISET/PWMx pin	Not applicable

(x = 1, 2, 3)

bit[6:4] PWMDIV
The output frequency is programmed for PWM dimming LED by this register. A/D conversion frequency (ADMODE = 1) is also programed by this register.

Table 13. PWM Output Frequency Setting

PWMDIV[2:0]	Output Frequency [Hz]
0	153
1	203
2	244
3	305
4	407
5	488
6	610
7	814

bit[7] PHEN
PWM dimming phase of channel 1 is programmed by this register as shown in Figure 44.

Table 14. PWM Phase Setting

PHEN	Phase Setting	
	BD18398xxx-M	BD18397xxx-M
0	All Channel: No Phase shift	All Channel: No Phase shift
1	Channel 1: no shift Channel 2: 120 degree Channel 3: 240 degree	Channel 1: no shift Channel 2: 180 degree -

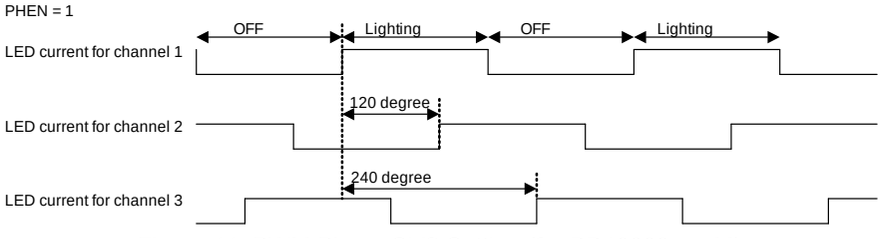


Figure 44. PWM Phase Shift Setting (for BD18398xxx-M)

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Description of Registers – continued

●Address 0x04: ISET1H ISET setting for channel 1 [Read/Write] initial value 0xE1

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ISET1 [9:2]							
Initial value	1	1	1	0	0	0	0	1

●Address 0x05: ISET1L ISET setting for channel 1 [Read/Write] initial value 0x01

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	-	-	-	ISET1[1:0]	
Initial value	0	0	0	0	0	0	0	1

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting.

ISET1H
bit[7:0]: ISET1[9:2]
ISET1L
bit[1:0]: ISET1[1:0]
LED DC current is programmed by this register as following formula.

Formula

$$I_{LEDxAVE} = \left(\frac{ISETx[9:0]}{1024} \times 2.5\ V - 0.2\ V \right) \times \frac{1}{12 \times R_{SNSx}}$$

●Address 0x06 to 0x09: ISETx[9:0] (x = 2 to 3)
This register is used to make setting of LED current for channel 2 and channel 3. The setting procedure is the same as that for channel 1 with Address set to 0x04 and 0x05.
ISET3[9:0] is only used for the BD18398xxx-M.

●Address 0x0A: DPWM1H PWM setting [Read/Write] initial value 0xFF

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	DPWM1 [9:2]							
Initial value	1	1	1	1	1	1	1	1

●Address 0x0B: DPWM1L PWM setting [Read/Write] initial value 0x03

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	-	-	-	DPWM1 [1:0]	
Initial value	0	0	0	0	0	0	1	1

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting. If you want to change value during dimming, WLOCK function can be used.

DPWM1H
bit[7:0]: DPWM1[9:2]
DPWM1L
bit[1:0]: DPWM1[1:0]
LED average current in PWM is programmed by this register. The dimming ratio is calculated as following formula.

$$D_{PWMx} = \frac{DPWMx[9:0] + 1}{1024}$$

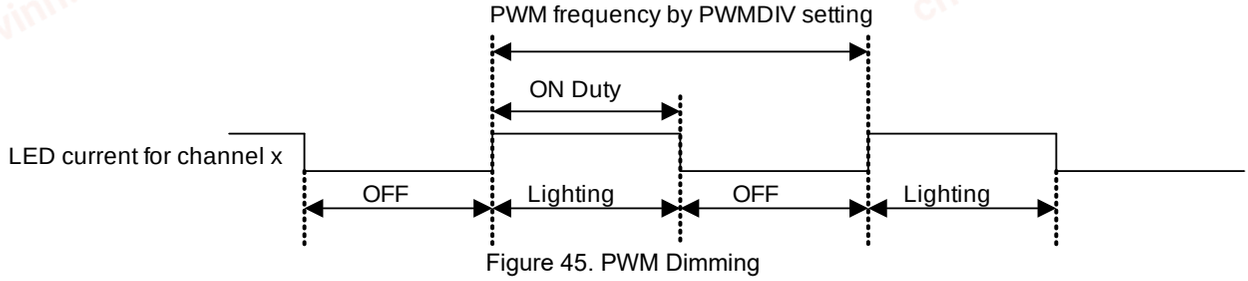


Figure 45. PWM Dimming

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Description of Registers – continued

●Address 0x0C to 0x0F: DPWMx (x = 2 to 3)
This register is used to make setting of PWM for channel 2 and channel 3. The setting procedure is the same as that for channel 1 with Address set to 0x0A and 0x0B
DPWM3 is only used for the BD18398xxx-M.

●Address 0x10: DCDCSET1 DC/DC setting for channel 1 [Read/Write] initial value 0x07

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	GM1[1:0]		TON1[5:0]					
Initial value	0	0	0	0	0	1	1	1

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting.

bit[7:6] GM1[1:0]
GM Amplifier Gain Setting

Table 15. DC/DC GM Amplifier Trans Conductance Setting

GM1[1:0] (Dec)	GM Amplifier Gain Setting [µS]
0	1360
1	870
2	530
3	300

bit[5:0] TON1[5:0]
DC/DC Frequency setting is programmed for channel 1 by this register.
It is available to use DC/DC frequency setting under 2.25 MHz. (over 2.25 MHz setting is prohibited.)

Table 16. DC/DC Frequency Setting for Reference (R_{TON} = 51 kΩ)

TON1[5:0] (Dec)	DCDC Frequency [kHz]
0	50
1	100
2	150
3	200
4	250
5	300
6	350
7	400
8	450
10	550
12	650
14	750
16	850
18	950
30	1,550
42	2,150

Table 17. DC/DC Frequency Setting for Reference (R_{TON} = 9.1 kΩ)

TON1[5:0] (Dec)	DCDC Frequency [kHz]
0	280
1	560
2	841
3	1,121
4	1,401
5	1,681
6	1,962
7	2,242

●Address 0x11 to 0x12: DCDCSETx(x = 2 to 3)
This register is used to make setting of DC/DC setting and GM amplifier gain setting for channel 2 and channel 3. The setting procedure is the same as that for channel 1 with Address set to 0x10.
DCDCSET3 is only used for the BD18398xxx-M.

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Description of Registers – continued

●Address 0x13: DCDCSET4 SSCG and Voltage control mode setting for DC/DC [Read/Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	VMODE3	VMODE2	VMODE1	-	SSCG[2:0]		
Initial value	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting.

bit[2:0] SSCG[2:0]
The modulation DC/DC switching frequency is programmed for all channel by this register.

Table 18. SSCG Modulation Setting

SSCG[2:0]	SSCG Modulation Ratio [Hz]
0	SSCG OFF (Fixed frequency of DC/DC)
1	155
2	185
3	283
4	361
5	536
6	763
7	1,044

bit[6:4] VMODEx
“Voltage control mode” for DC/DC is programmed by this register.
(VMODE3 is only used for the BD18398xxx-M)

Table 19. Voltage Control Mode Setting

VMODEx	Controlled Mode
0	Current control mode for channel x
1	Voltage control mode for channel x

(x = 1, 2, 3)

In the Voltage mode setting (VMODEx = 1), SNSN1 pin voltage is regulated by as following.

$$V_{SNSNx} = \frac{ISETx[9:0]}{1024} \times 67.5\,V\ (@VMODEx = 1)$$

●Address 0x14: CHEN Channel enable and Dimming enable [Read/Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	PWMDIM3	PWMDIM2	PWMDIM1	-	CHON3	CHON2	CHON1
Initial value	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

bit[2:0] CHONx (CHON3 is only used for the BD18398xxx-M)
Each channel starts-up by this register. If CHONx = 1, LED dimming is available for channel x. (x = 1, 2, 3) CHONx = 0, LED dimming is not available for channel x. Protection such as “LED short to ground error protection”, “LED open error protection”, “SW Over Current error protection” and “LED Over Current error protection” in the target channel is not available when CHONx = 0.

Table 20. Channel Enable

CHONx	Enable
0	Channel x is disable.
1	Channel x is enable.

(x = 1, 2, 3)

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Description of Registers – continued

bit[6:4] PWMDIMx

The internal PWM dimming duty is programmed by this register. It is available to dim by the DPWMx[9:0] register when the PWMDIMx = 1. The internal PWM duty can be set to 100 % when the PWMDIMx = 0.

Table 21. PWM Dimming Enable

PWMDIMx	Operation
0	PWM Duty is 100 % fixed.
1	PWM Dimming enable. Dimming ratio is programmed by the DPWMx[9:0] register.

(x = 1, 2, 3)

Table 22. How to Dim by PWM

CHONx	PWMDIMx	DC/DC	Internal PWM Dimming for Channel x
0	0	OFF	OFF
0	1	OFF	OFF
1	0	ON	100 %
1	1	ON	Programmed by the DPWMx[9:0]

(x = 1, 2, 3)

●Address 0x15: ADSEL A/D monitor channel select [Read/Write] initial value 0x10

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ADTRG	-	-	ADMODE	VMONSEL[3:0]			
Initial value	0	0	0	1	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.

bit[3:0] VMONSEL[3:0]

VMON register is shared in for monitoring below node. This register should be programmed before reading VMON register when target node voltage is need.

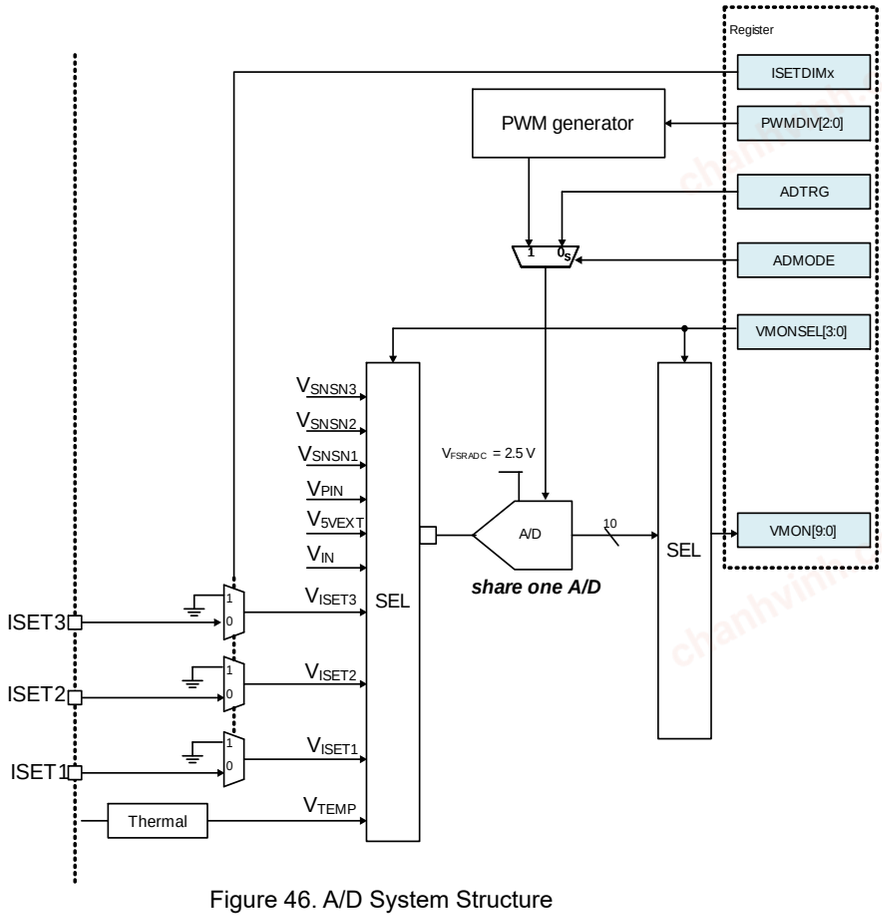


Figure 46. A/D System Structure

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Description of Registers – continued

Table 23. VMONSEL Status

VMONSEL	Monitor Node	Other Register Set Needed
0x0	Thermal (default)	-
0x1	ISET1	ISETDIM1 = 0
0x2	ISET2	ISETDIM2 = 0
0x3	ISET3	ISETDIM3 = 0
0x4	V_{IN}	-
0x5	V_{5VEXT}	-
0x6	V_{PIN}	-
0x7	V_{SNSN1}	-
0x8	V_{SNSN2}	-
0x9	V_{SNSN3}	-
0xA to 0xF	Not Used	-

bit[4] ADMODE

There are two A/D converting modes.

When ADMODE = 1, A/D converter is operated automatically. Conversion frequency is determined by PWMDIV register and is operational only in LEDACTIVE state.

When ADMODE = 0, A/D converter is operated manually by ADTRG. A/D converter becomes sleep condition (low current consumption) after 1 conversion.

Table 24. ADMODE Operation

ADMODE	Operation
0	A/D conversion for only target node by ADTRG register
1	A/D conversion repeatedly. This period is programmed by PWMDIV register.

bit[7] ADTRG

A/D starts to convert the data selected by VMONSEL register after writing ADTRG = 1 during ADMODE = 0. This register will return to '0' after writing '1'. Updated data is available less than 24 µs.

Table 25. ADTRG

ADTRG	Operation
0	No conversion
1	Starts to convert data in ADMODE = 0

●Address 0x16: VMONH common voltage monitor by A/D [Read] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	VMON[9:2]							
Initial value	0	0	0	0	0	0	0	0

●Address 0x17: VMONL common voltage monitor by A/D [Read] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	-	-	-	VMON[1:0]	
Initial value	0	0	0	0	0	0	0	0

The register data is updated to the newest data immediately when the data are updated by A/D converting.

VMONH

bit[7:0] VMON[9:2]

VMONL

bit[1:0]: VMON[1:0]

This register is used for monitoring the thermal sensor voltage (V_{TEMP}), $V_{ISET/PWMx}$, V_{IN}, V_{5VEXT}, V_{PIN} or V_{SNSNx} node (x = 1, 2, 3). This operation is programmed by VMONSEL register.

This data is divided into two register address. If all of 10-bit data is required when ADMODE = 1, or RDMODE function is available.

Formula 1 for thermal sensor voltage

Thermal sensor voltage ADC read value = 418 @25 deg
Thermal sensor voltage ADC read value = 602 @150 deg

1.472 count/temp (1 degree)

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Description of Registers – continued

Formula 2 for external input pin nodes

Monitor voltage 1 [V] = “X” x (VMON + 1) / 1024

V_{IN}: “X” = 48, V_{PIN}: “X” = 70, and V_{SNSNx}: “X” = 67.5, V_{5VEXT}: “X” = 5.5, $V_{ISET/PWMx}$: “X” = 2.5

●Address 0x18: ERRSTALL All error status each protection [Read] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	WDTERR	CRCERR	PINUVLO	UVLO	-	ERRDET3	ERRDET2	ERRDET1
Initial value	0	0	0	0	0	0	0	0

The register data is updated to the newest data immediately when the data (one or more error/protection) is detected.

bit[2:0] ERRDETx (ERRDET3 is only used for the BD18398xxx-M)
This register is error status each channel.

Table 26. Error Status of Each Channel

ERRDETx	Status
0	Normal
1	Detects error LSDx || LODx || SWOCPERRx || LEDOCPERRx

(x = 1, 2, 3)

bit[4] UVLO
This register is error status for UVLO.

Table 27. UVLO

UVLO	Status
0	Normal
1	Detects under voltage error for V_{5VEXT} or V_{5VREG}

bit[5] PINUVLO
This register is error status for PINUVLO.

Table 28. PINUVLO

PINUVLO	Status
0	Normal
1	Detects under voltage error for PIN

bit [6] CRCERR
This register is error status for CRC. If CRC error is detected, this register becomes 1. This register becomes 0 by FLTRST = 1. If CRC Error occurred to the SPI command sent after to sending FLTRST, this will not be detected, for more details refer to Error sequence for “CRC Error”.

Table 29. CRC Error Status

CRCERR	Status
0	Normal
1	Detects CRC error

bit[7] WDTERR
This register is error status for “Watch Dog Timer”. If “Watch Dog Timer error” is detected, this register becomes 1. This register becomes 0 by FLTRST = 1.

Table 30. “Watch Dog Timer error” Status

WDTERR	Status
0	Normal
1	Detects “Watch Dog Timer error”

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Description of Registers – continued

●Address 0x19: ERRST1 channel 1 error status [Read] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	-	LEDOCPERR1	SWOCPERR1	LOD1	LSD1
Initial value	0	0	0	0	0	0	0	0

The register data is updated to the newest data immediately when the data (“LED open error”, “LED short to ground error”, “SW1 Over Current”, “LED Over Current”) is detected.

bit[0] LSD1

This register is “LED short to ground error” status for channel 1. LSD1 becomes “1” when “LED short to ground error” is detected, and LSD returns “0” when “LED short to ground error” is released.
There is filter for detecting (10 ms) and releasing (1 ms) each channel. This filter is shared for “LED short to ground protection” and “LED open protection”.

Table 31. “LED short to ground error” Status Register

LSD1	Status
0	Normal
1	Detects LED short to ground error

bit[1] LOD1

This register is “LED open error” status for channel 1. LOD1 becomes “1” when “LED open error” is detected, and LOD1 returns “0” when “LED open error” is released.
There is filter for detecting (10 ms) and releasing (1 ms) each channel. This filter is shared for “LED short to ground protection” and “LED open protection”.

Table 32. “LED open error” Status Register

LOD1	Status
0	Normal
1	Detects LED open error

bit[2] SWOCPERR1

This register is “SW Over Current error” status for channel 1. If SWOCPLAT = 0, SWOCPERR1 becomes “1” when “SW Over Current” is detected, and SWOCPERR1 returns “0” when “SW Over Current error” is released. If SWOCPLAT = 1, SWOCPERR1 becomes “1” when “SW over current error” is detected, and SWOCPERR1 becomes “0” by FLTRST = 1.

Table 33. SW Over Current Error Status

SWOCPERR1	Status
0	Normal
1	Detects SW Over Current error

bit[3] LEDOCPERR1

This register is “LED Over Current error” status for channel 1. If LEDOCPLAT = 0, LEDOCPERR1 becomes “1” when “LED Over Current” is detected, and LEDOCPERR1 returns “0” when “LED Over Current error” is released. If LEDOCPLAT = 1, LEDOCPERR1 becomes “1” when “LED over current error” is detected, and LEDOCPERR1 becomes “0” by FLTRST = 1.

Table 34. LED Over Current Error Status

LEDOCPERR1	Status
0	Normal
1	Detects LED Over Current error

●Address 0x1A to 0x1B: ERRSTx (x = 2 to 3)

These registers are error status for channel 2 and channel 3. These functions are the same as that for channel 1 with Address set to 0x19. ERRST3 is only used for the BD18398xxx-M.

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Sequence

1 Start-up and Turn-off Sequence

Normal Start-up (No SPI Communication)

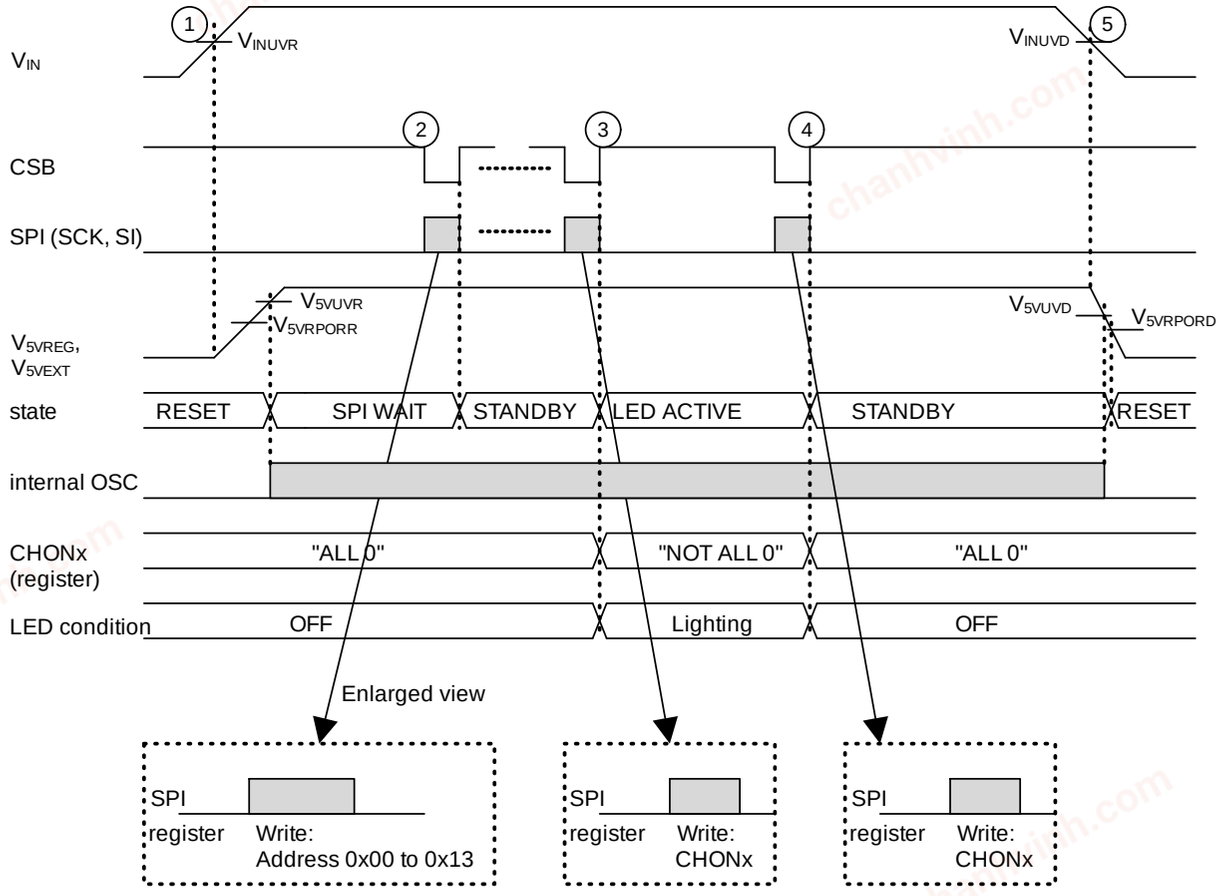


Figure 47. Start-up Sequence for Normal Operation

When you light the LED by general SPI control, follow the sequence below.

① Input the power supply of VIN.
② MCU starts communicating with SPI after waiting internal regulator to be stable.
③ Start dimming LED by CHONx = 1 (channel x).
④ Stop dimming LED by CHONx = 0.
⑤ Stop the input power supply of VIN.

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1 Start-up and Turn-off Sequence - continued

LIMP-HOME Start-up (No SPI Communication)

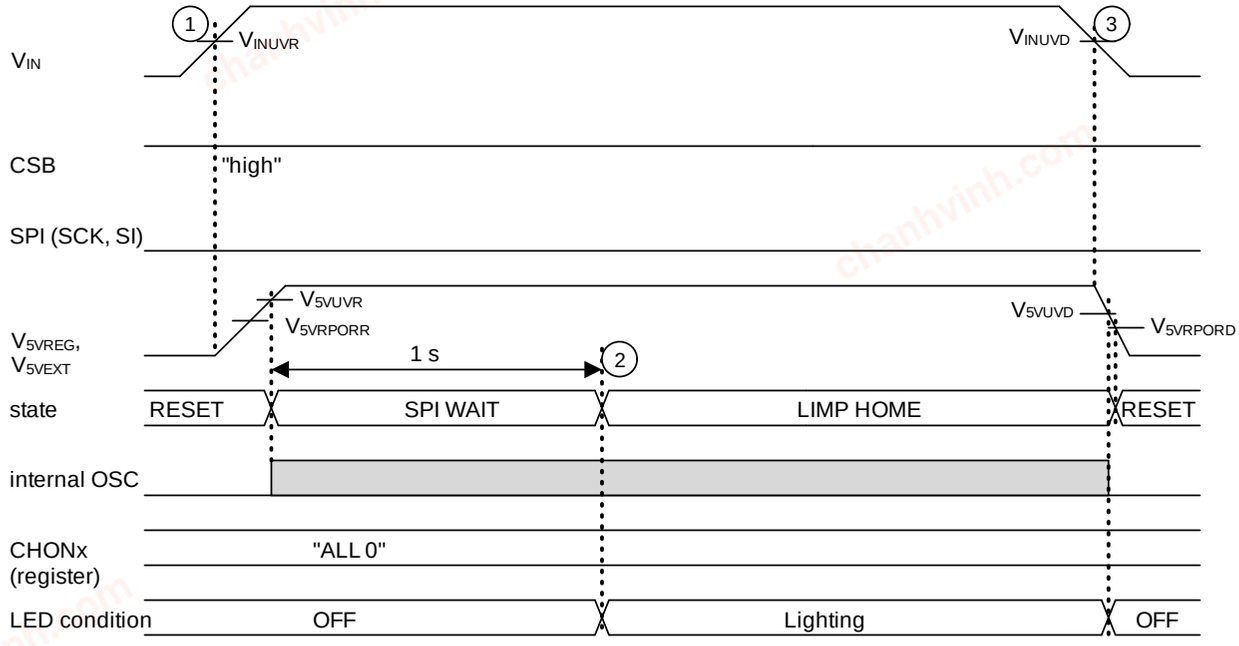


Figure 48. Start-up Sequence for LIMP-HOME

When you light the LED by LIMP-HOME mode, follow the sequence below.

① Input the power supply of VIN.
② Start lighting (by external resistor) after waiting 1 s from UVLO release.
③ Stop the input power supply of VIN.

STAND-ALONE Start-up (CSB = Low)

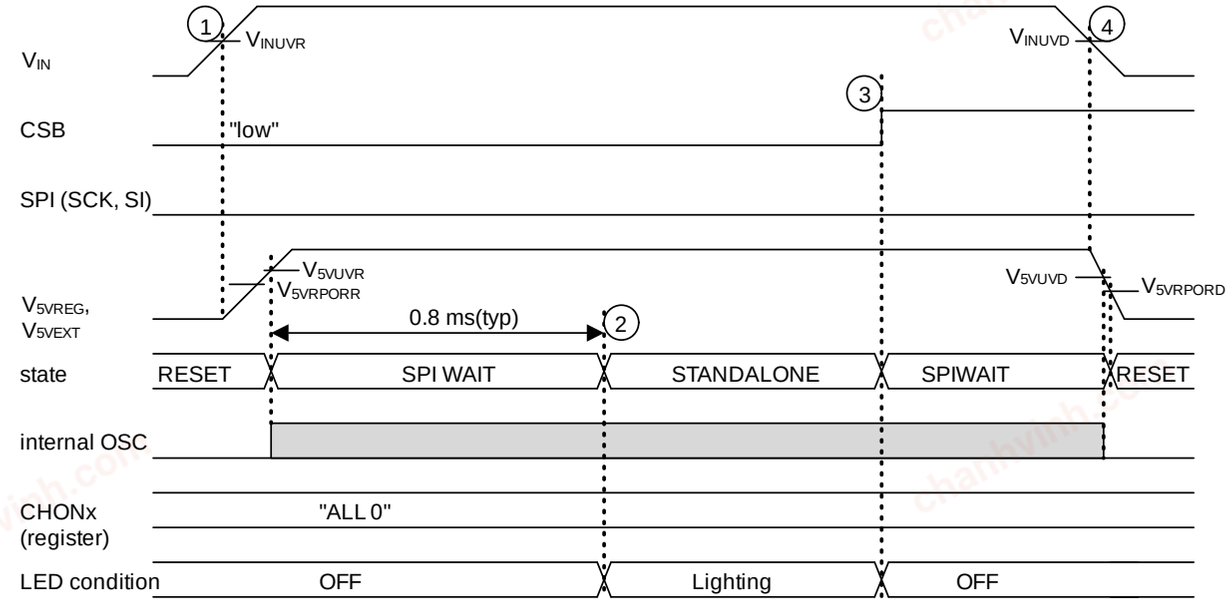


Figure 49. Start-up Sequence for STAND-ALONE

When you light the LED by STAND-ALONE mode, follow the sequence below.

① Input the power supply of VIN with CSB = low.
② Start lighting (by external resistor) after waiting 0.8 ms from UVLO release.
③ Input CSB = high and stop lighting. From this point, dimming can be operated by register setting.
④ Stop to input the power supply of VIN.

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1 Start-up and Turn-off Sequence - continued

LIMP-HOME during SPIWAIT (Release by SPI Communication)

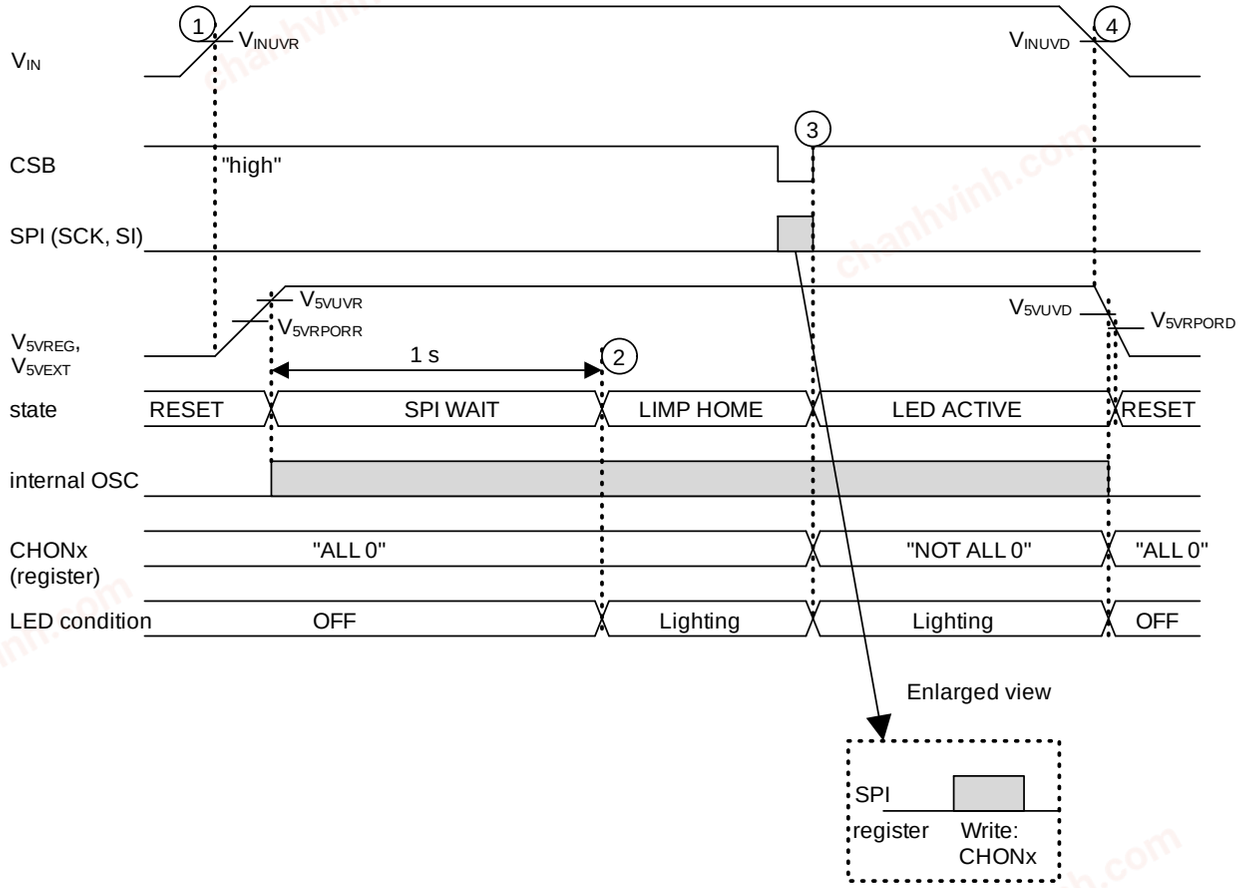


Figure 50. Start-up Sequence for LIMP-HOME

When you light the LED by LIMP-HOME mode then MCU sends SPI commands, follow the sequence below.

① Input the power supply of VIN.
② Start lighting based on external resistor after waiting 1 s from UVLO release.
③ After SPI Access (CRC OK), it triggers LIMP-HOME to LEDACTIVE. Lighting is changed from “based on external resistor” to SPI register controlled. If the previous state is SPIWAIT it returns to STANDBY or LEDACTIVE. In the case above it returns to LEDACTIVE after writing on CHONx register.
④ Stop the input power supply of VIN.

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1 Start-up and Turn-off Sequence - continued

LIMP-HOME during LEDACTIVE (Release by SPI Communication)

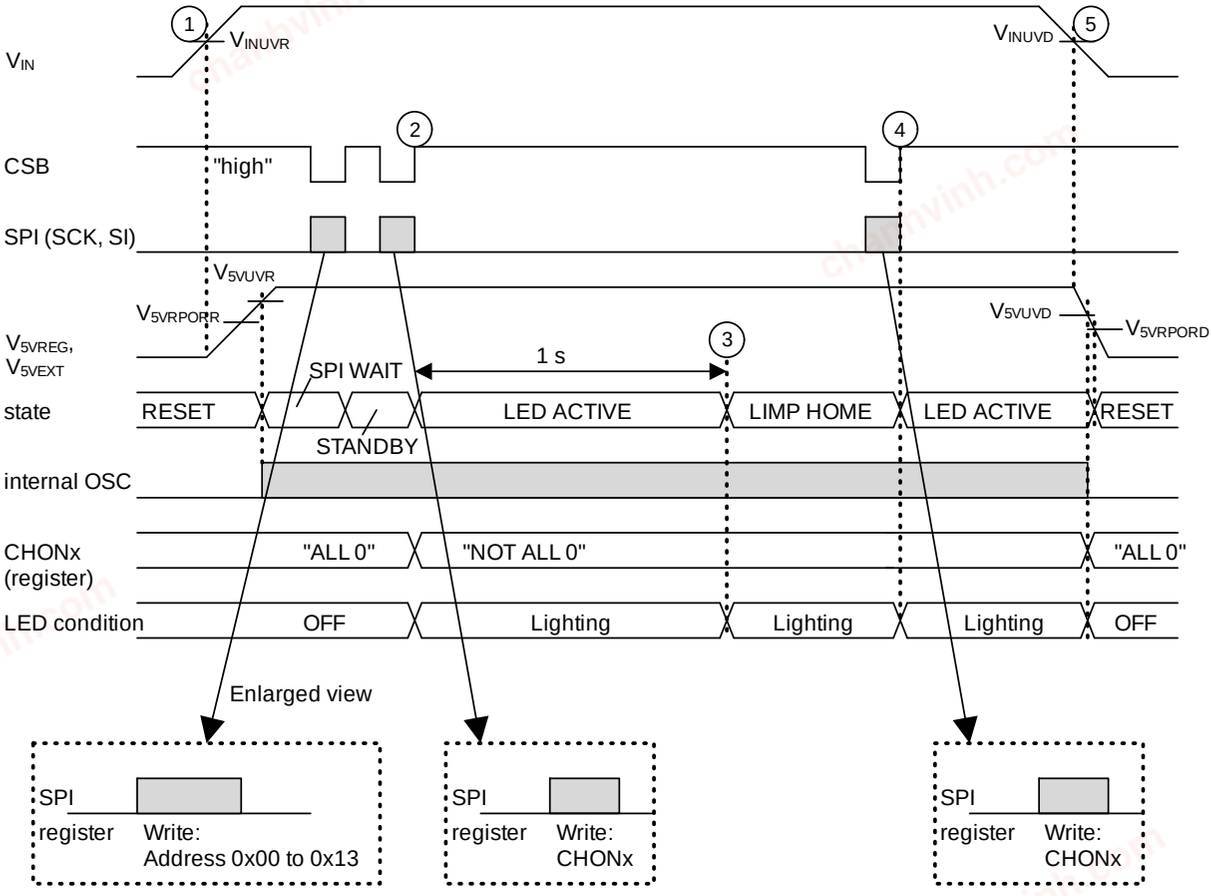


Figure 51. Start-up Sequence for LIMP-HOME

When you light the LED by LIMP-HOME mode, follow the sequence below.

① Input the power supply of VIN.

② MCU starts communicating with SPI after waiting internal regulator to be stable.
Start dimming LED by CHONx = 1 (channel x).

③ Start lighting based on external resistor after waiting 1 s from UVLO release.

④ After SPI Access (CRC OK), it triggers LIMP-HOME to LEDACTIVE. Lighting is changed from “based on external resistor” to SPI register controlled. If the previous state is LEDACTIVE, it returns to LEDACTIVE and continue dimming by Register Setting.

⑤ Stop the input power supply of VIN.

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1 Start-up and Turn-off Sequence - continued

Sleep Mode

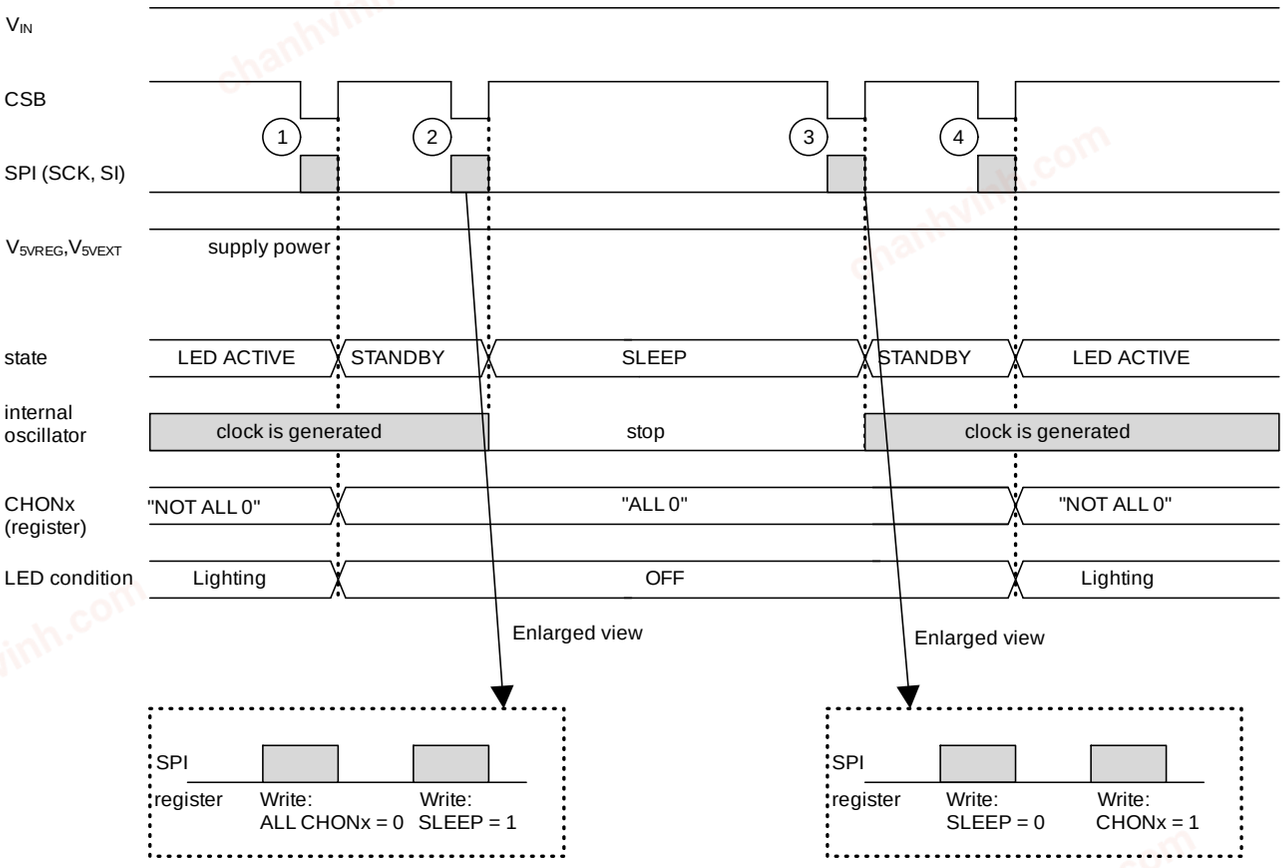


Figure 52. Sequence for SLEEP Mode

When you use SLEEP mode by SPI control, follow the sequence below.

① If ALL CHONx = 0, this IC stop lighting and go “STANDBY” state.
② If SLEEP = 1, internal oscillator stops. (Low quiescent current by stopping internal clock.)
③ If SLEEP = 0, internal oscillator starts.
④ If ANY CHONx = 1, this IC starts lighting and go “LEDACTIVE” state.

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1 Start-up and Turn-off Sequence - continued

Cold Cranking Mode (Sleep by UVLO)

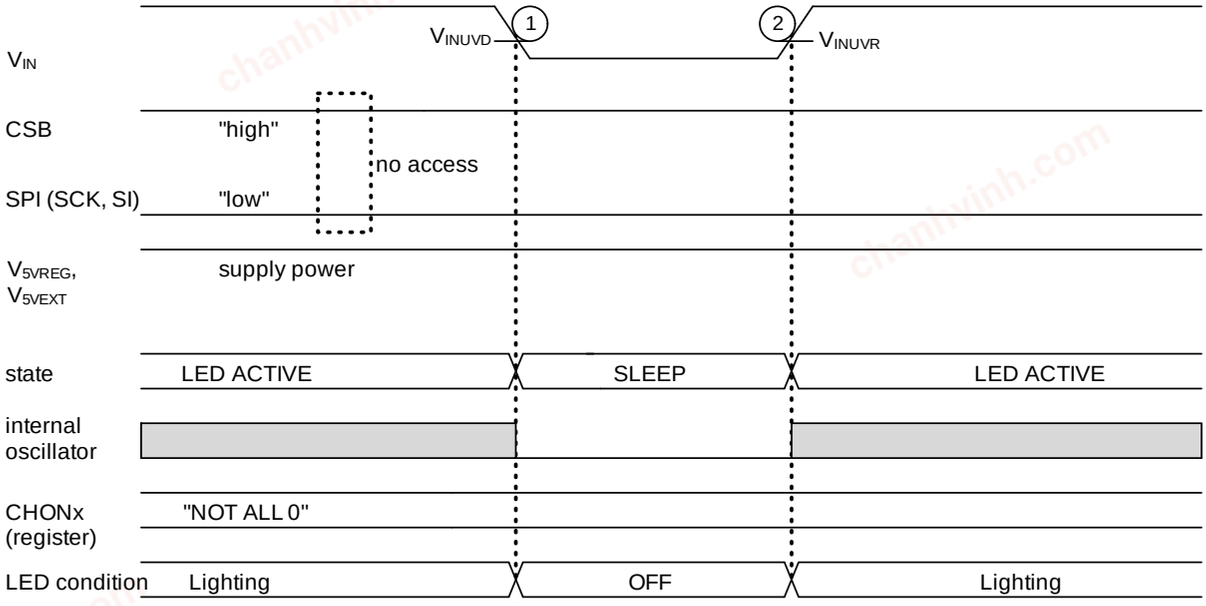


Figure 53. Start-up Sequence for Cold Cranking Mode

When this IC is in “cold cranking” condition, sequence of operation is as follows.

① If this IC detects “VIN UVLO”, internal oscillator is stop and stop lighting. (Low quiescent current condition.)

② When “VIN UVLO” is released, the internal oscillator starts, and this IC starts lighting with the same register settings as before detecting “VIN UVLO”. However, when this IC detects "POR", it is initialized.

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1 Start-up and Turn-off Sequence - continued

Error Sequence for “CRC Error”

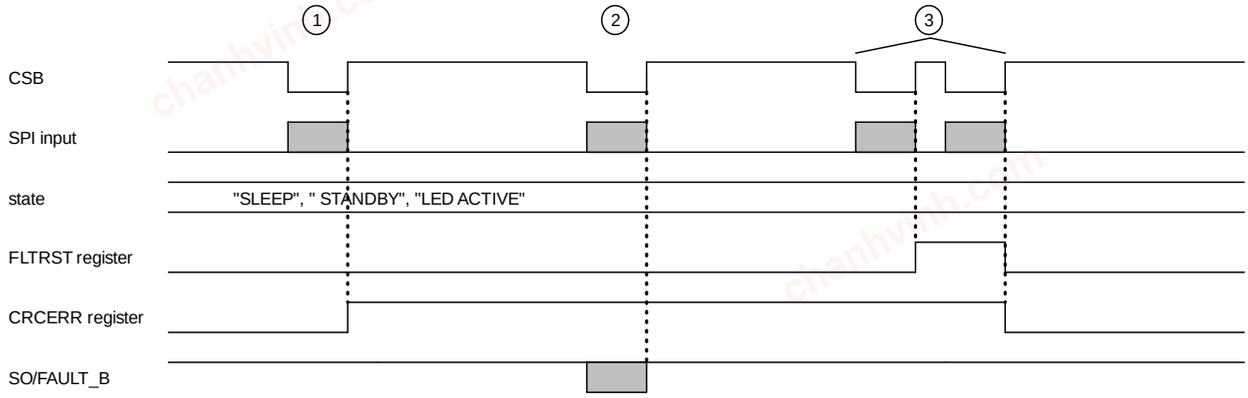


Figure 54. CRC Error Detection

① CRC error is detected when data sent does not match the CRC value in the SPI command. This mismatch can be caused by wrong data or noise in the SPI line. Write operation is not executed in the IC. Target Register is not updated. In this case, CRC Error status register is updated to High. Protection is latched automatically, sending SPI command with correct CRC does not clear CRCERR status register.

② MCU sends Read Command to status registers to confirm CRC status register.

③ MCU sends FLTRST and dummy SPI (data 0x00) to release the status register.

Error Sequence for “WDT Error”

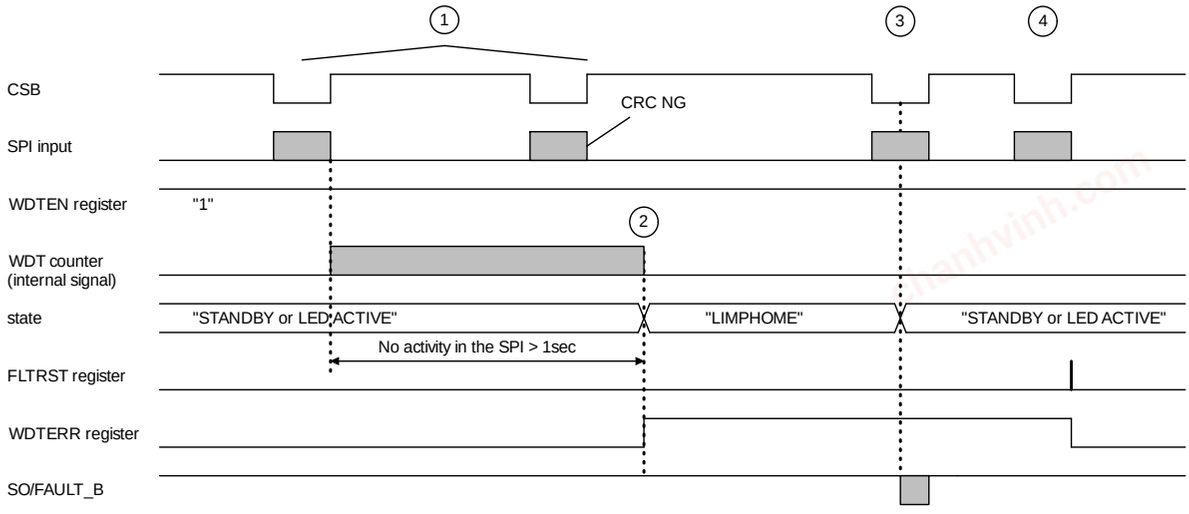


Figure 55. WDT Error Detection

① Watch Dog Timer starts to count at STANDBY or LEDACTIVE state. When there is no "CRC OK" detected in more than 1 s, IC detects WDT Error.

② WDT is detected, it sets the corresponding status register WDTERR to High and state changes from STANDBY/LEDACTIVE/SPIWAIT to LIMP-HOME.

③ MCU sends Read command to Status register to confirm WDT status. This event releases LIMP-HOME mode.

④ WDT detection is latches automatically, MCU must send FLTRST to clear the WDTERR status register and SO/FAULT_B output.

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Sequence - continued

2 A/D Control Sequence

ADMODE = 1 (Auto Mode)

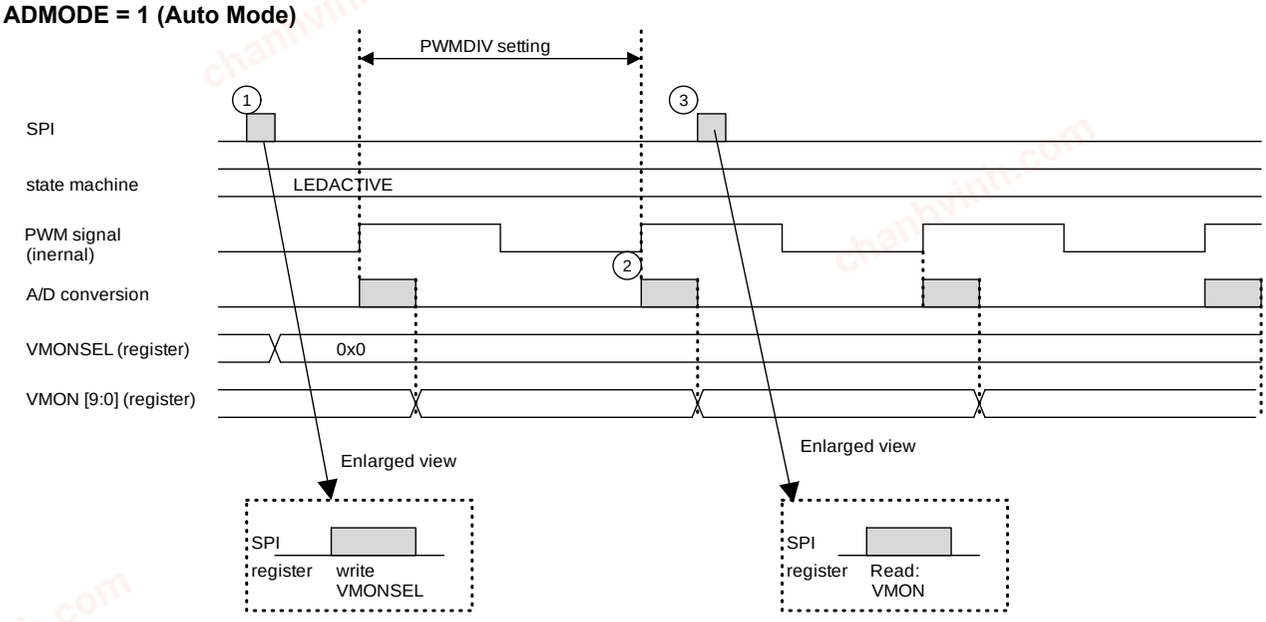


Figure 56. A/D Control (ADMODE = 1)

① If you want to know VIN voltage, VMON register is available by setting VMONSEL register.

② A/D conversion is executed every PWM timing (internal signal). This period is programmed by PWMDIV register. It is necessary to set CHONx = 1 to go to LEDACTIVE state to operate this.

③ You should wait to access register after this period.

ADMODE = 0 (Manual Mode)

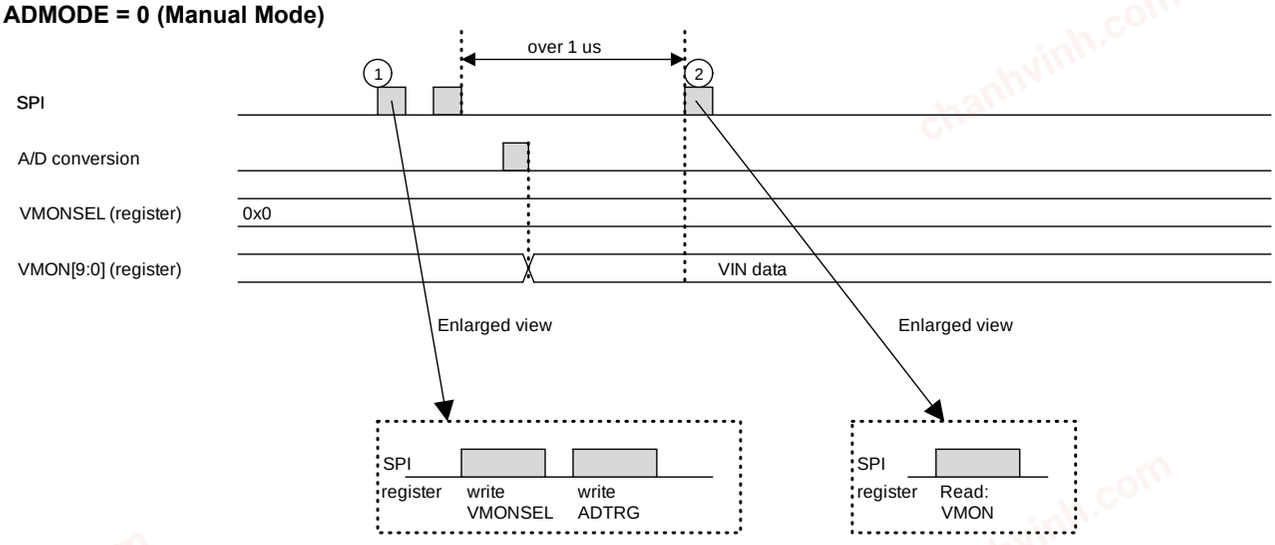


Figure 57. A/D Control (ADMODE = 0)

① If you want to know VIN voltage, VMON register is available by setting ADSEL register, and A/D starts to convert by ADTRG = 1.

② You should wait to access register after changing ADSEL. VMON register is available after 1 µs (include margin).

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Typical Performance Curves

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = 25 °C)

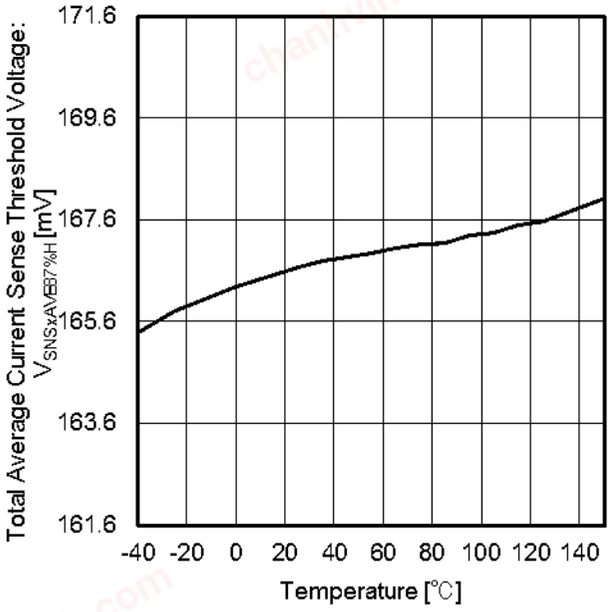


Figure 58. Total Average Current Sense Threshold Voltage vs Temperature

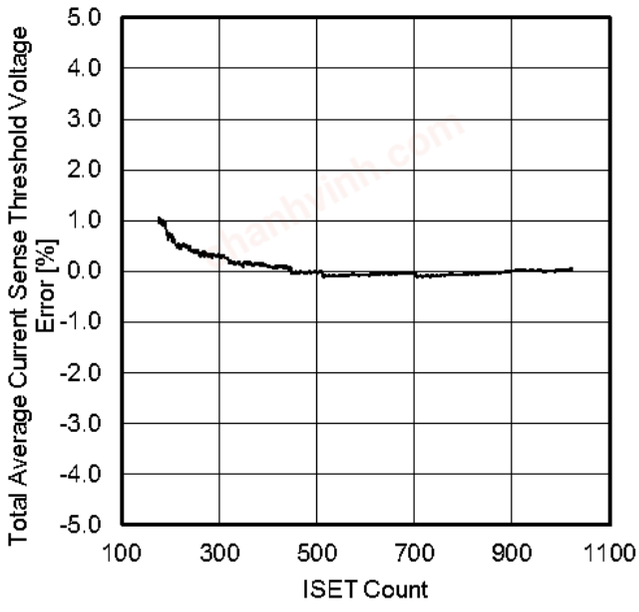


Figure 59. Total Average Current Sense Threshold Voltage Error vs ISET Count

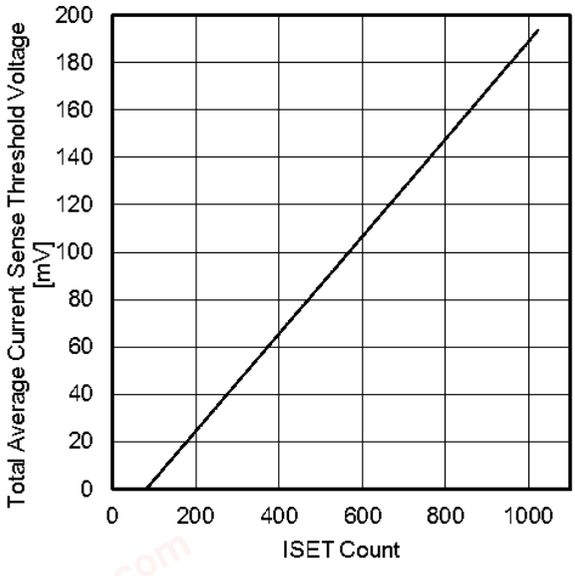


Figure 60. Total Average Current Sense Threshold Voltage vs ISET Count

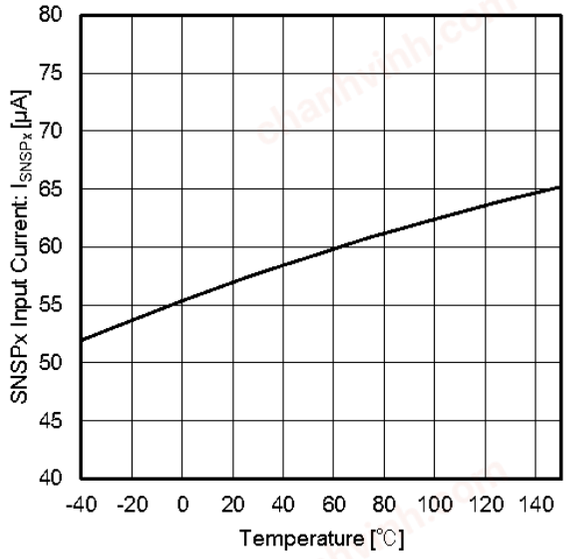


Figure 61. SNSPx Input Current vs Temperature

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = 25 °C)

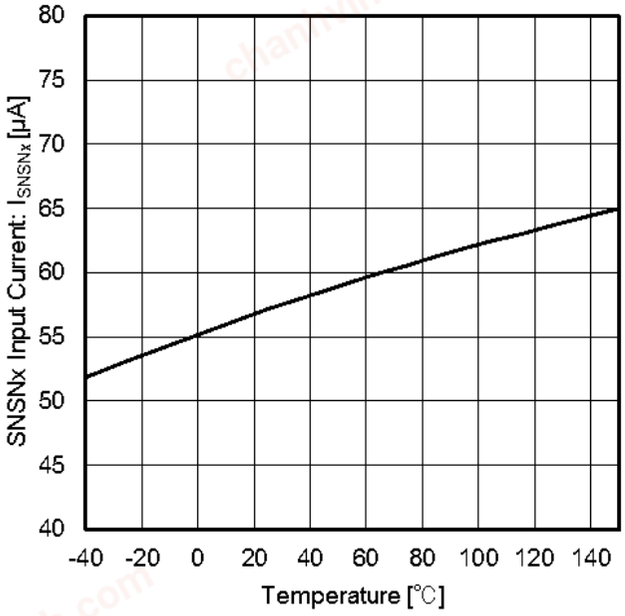


Figure 62. SNSNx Input Current vs Temperature

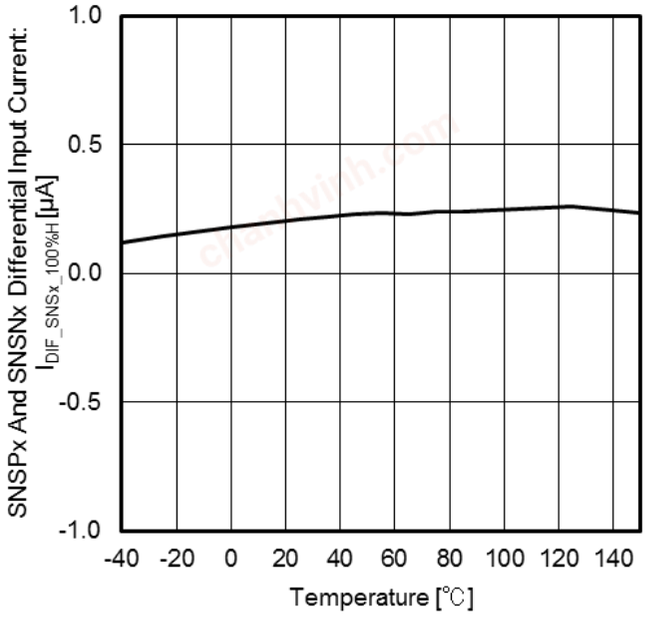


Figure 63. SNSPx And SNSNx Differential Input Current vs Temperature

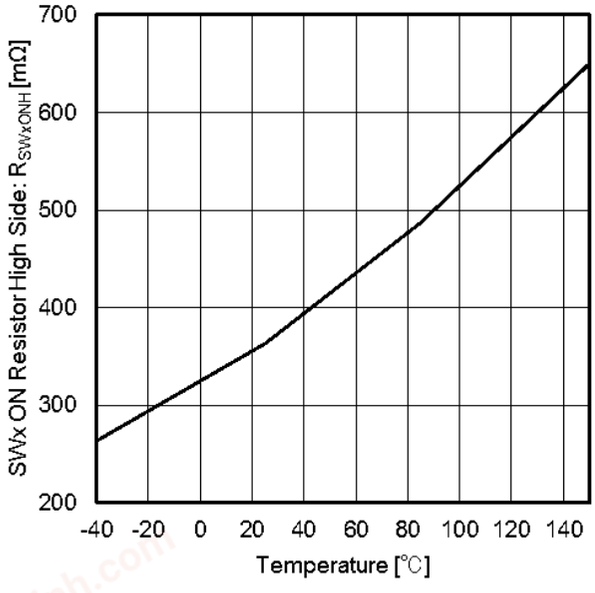


Figure 64. SWx ON Resistor High Side vs Temperature

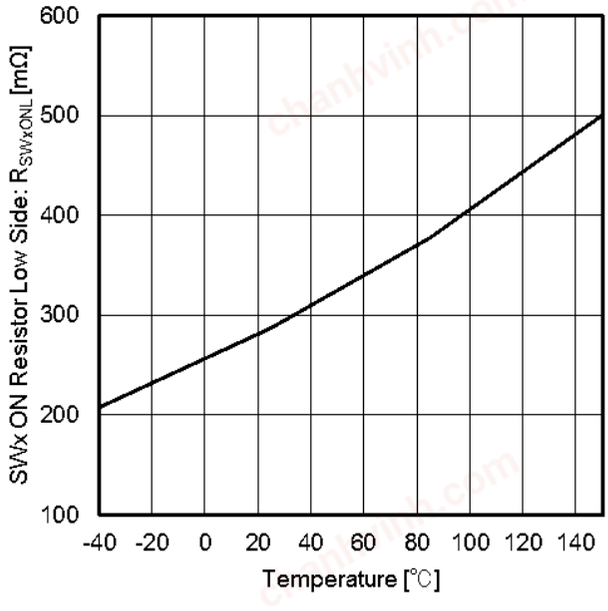


Figure 65. SWx ON Resistor Low Side vs Temperature

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = 25 °C)

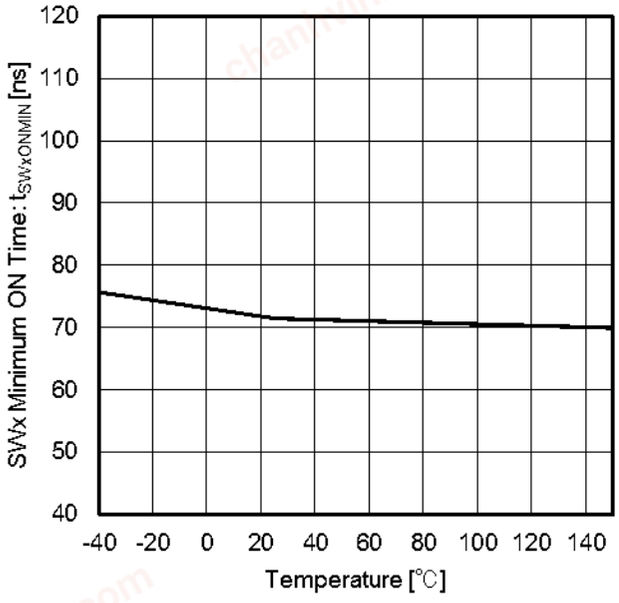


Figure 66. SWx Minimum ON Time vs Temperature

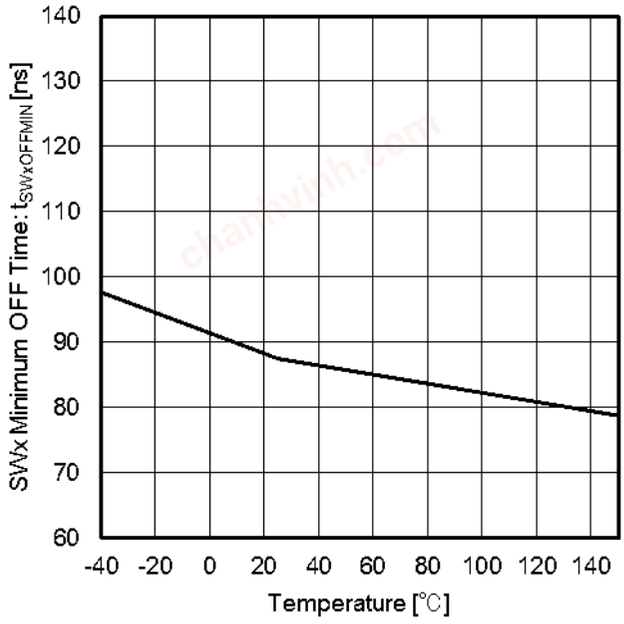


Figure 67. SWx Minimum OFF Time vs Temperature

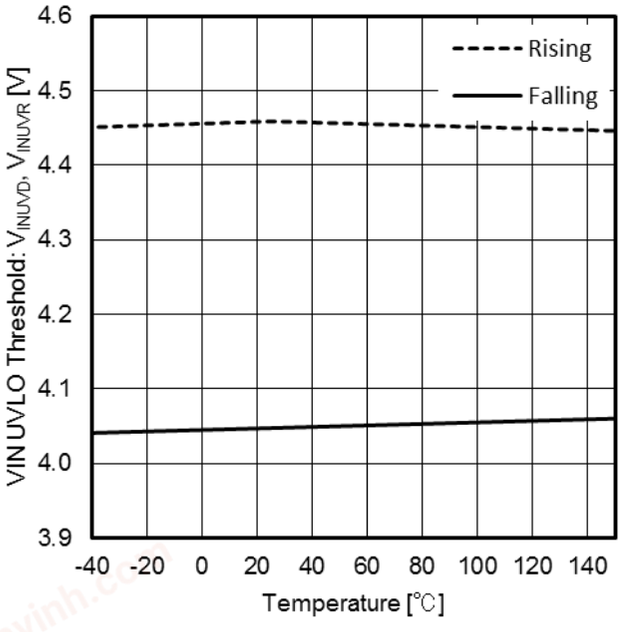


Figure 68. VIN UVLO Threshold vs Temperature

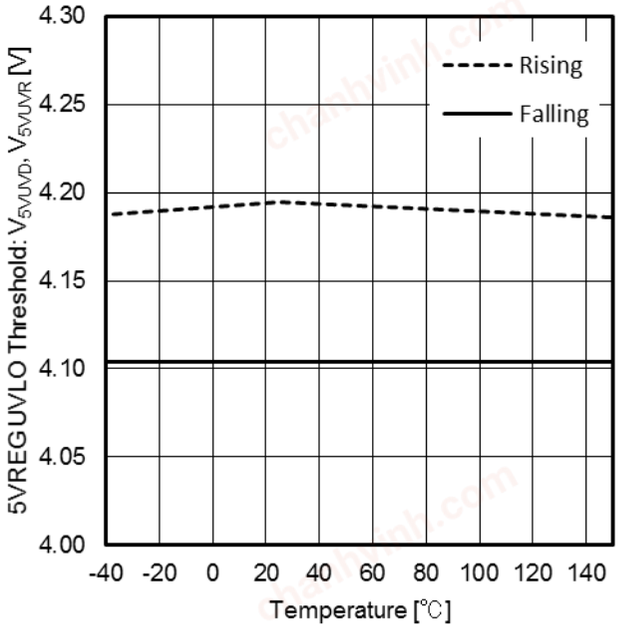


Figure 69. 5VREG UVLO Threshold vs Temperature

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = 25 °C)

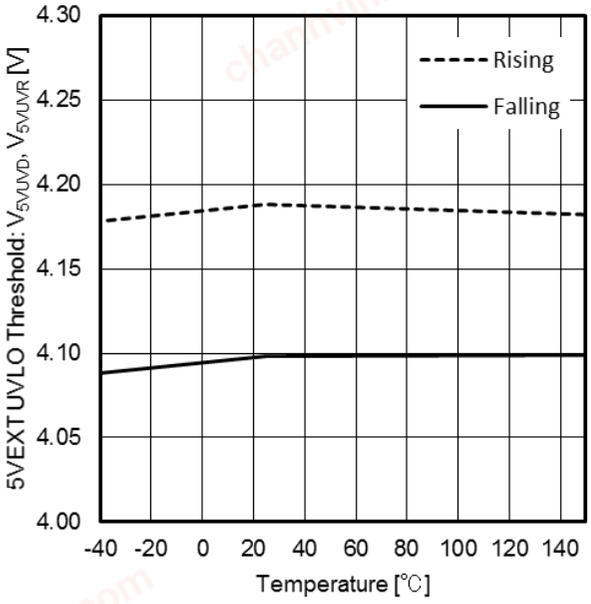


Figure 70. 5VEXT UVLO Threshold vs Temperature

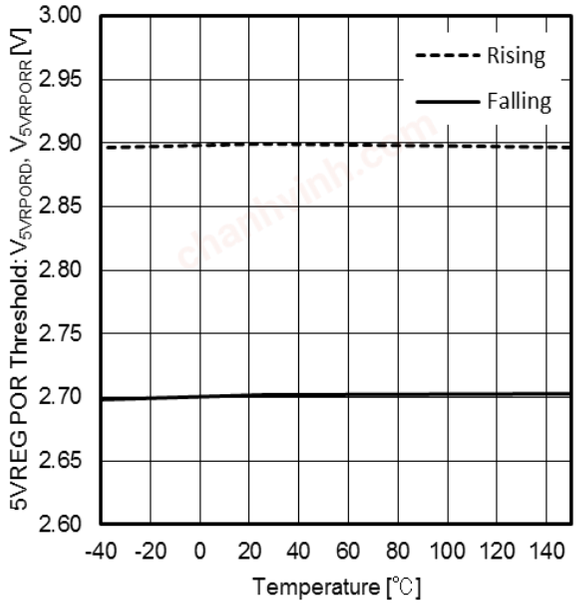


Figure 71. 5VREG POR Threshold vs Temperature

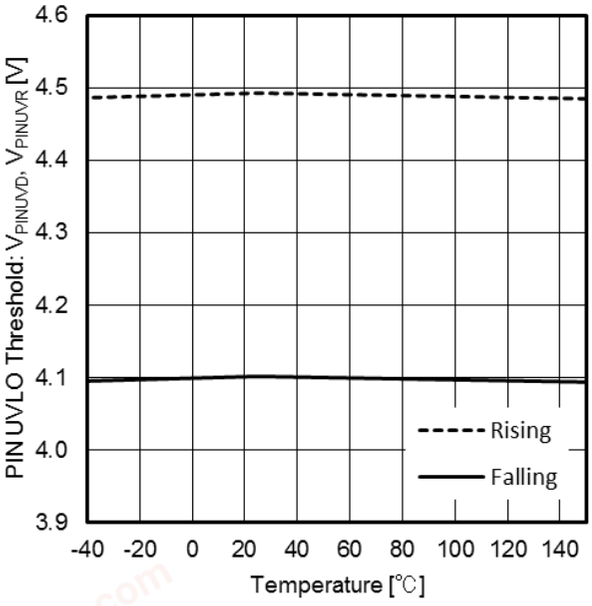


Figure 72. PIN UVLO Threshold vs Temperature

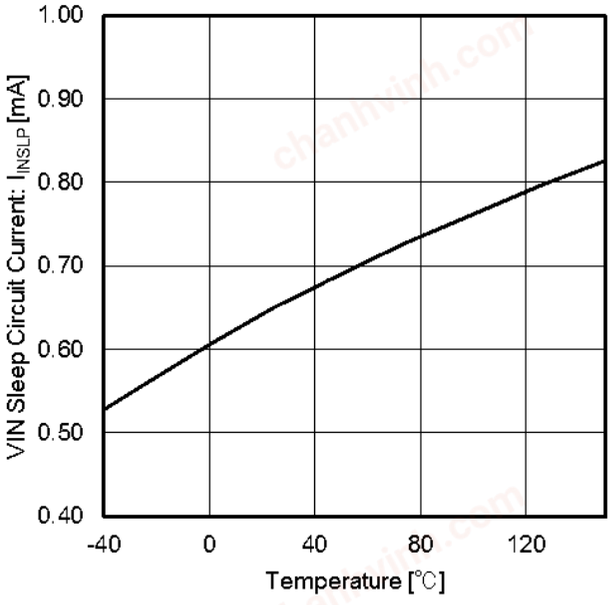


Figure 73. VIN Sleep Circuit Current vs Temperature

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = 25 °C)

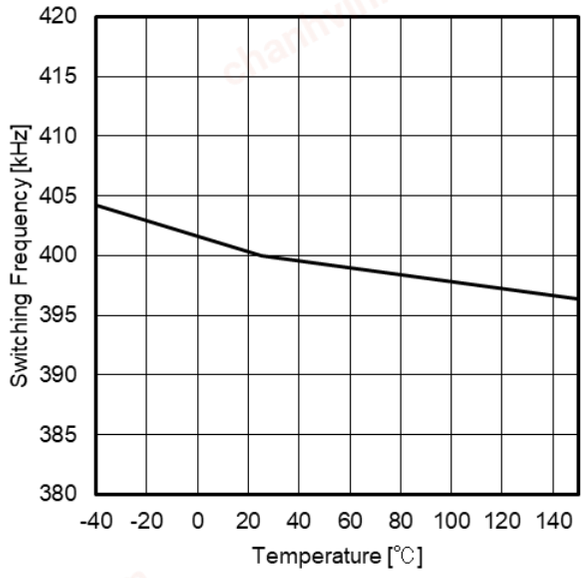


Figure 74. Switching Frequency vs Temperature
(D_{ONx} = 0.5, R_{TON} = 51 kΩ)

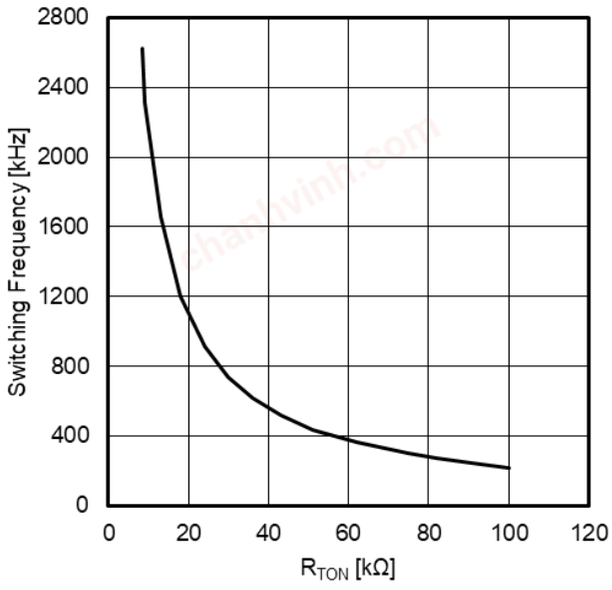


Figure 75. Switching Frequency vs R_{TON}
(D_{ONx} = 0.5)

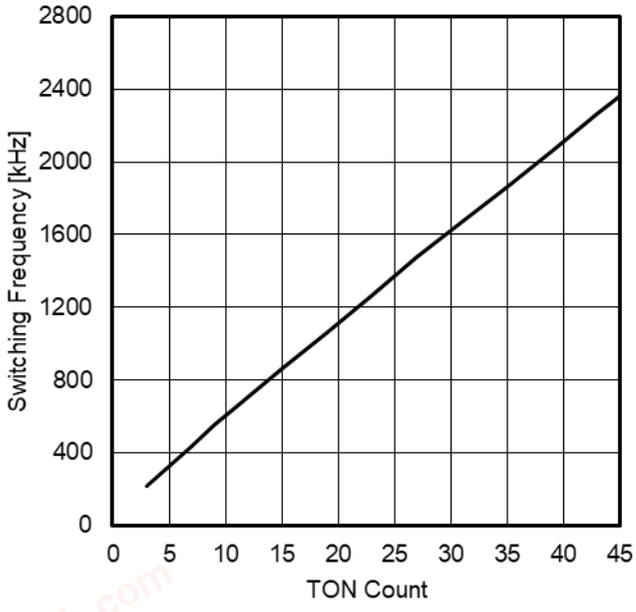


Figure 76. Switching Frequency vs TON Count
(D_{ONx} = 0.5, R_{TON} = 51 kΩ)

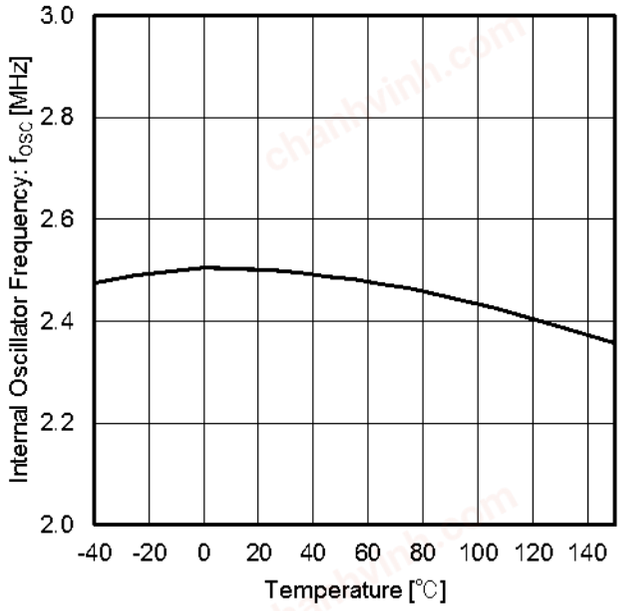


Figure 77. Internal Oscillator Frequency vs Temperature

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V, Tj = 25 °C)

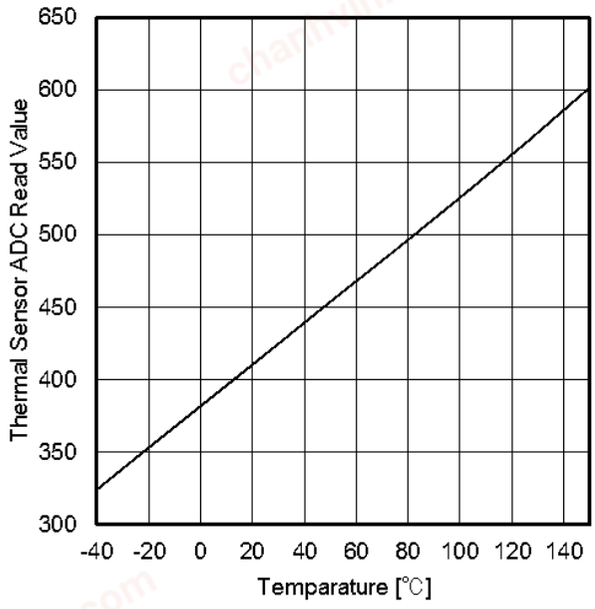


Figure 78. Thermal Sensor ADC Read Value vs Temperature

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Design Requirements

Parameter	Symbol	Min	Typ	Max	Unit
VIN Continuous Supply Voltage	V_{IN}	-	13	-	V
PIN Continuous Supply Voltage	V_{PIN}	58	60	62	V
SNSNx LED Output Voltage	V_{OUTx}	3	-	54	V
Continuous Average LED Current	I_{LEDx}	0.2	-	2.0	A
ΔPeak LED Current	ΔI_{LEDx_PEAK}	-	-	1	A
LED String Series Resister at V_{OUTx} = 30 V	R_{LEDx}	-	2.4	-	Ω
Setting Switching Frequency	f_{SWx}	-	400	-	kHz
Dynamic Voltage Changed of LEDs	ΔV_{LEDx}	-	54	-	V
Transition Time for Dynamic Voltage Change of LEDs	T_{LEDx}	-	25	-	µs
Ambient Temperature	Topr	-	25	-	°C

Design Procedure

1 Calculating Duty Cycle

Solve for the buck converter switching on-duty (D_{ONx}) and Max-on-duty (D_{ONx_MAX}) and Minimum-on-duty (D_{ONx_MIN}). SNSPx voltage is almost same with SNSNx voltage.

$$D_{ONx} = \frac{V_{SNSPx}}{V_{PIN}},$$

$$D_{ONx_{MAX}} = \frac{V_{SNSPx_{MAX}}}{V_{PIN_{MIN}}} = \frac{54}{58} = 0.931,$$

$$D_{ONx_MIN} = \frac{V_{SNSPx_MIN}}{V_{PIN_MAX}} = \frac{3}{62} = 0.0483$$

2 Calculating Minimum on-time and Minimum off-time

Solve for the buck converter switching on-time (T_{ONx}) and Minimum-on-time (T_{ONx_MIN}) and Minimum-off-time (T_{OFFx_MIN}).

$$T_{ONx} = \frac{D_{ONx}}{f_{SWx}},$$

$$T_{ONx_MIN} = \frac{D_{ONx_MIN}}{f_{SWx}} = \frac{0.0483}{400 \times 10^3} = 121 \times 10^{-9},$$

$$T_{OFFx_MIN} = \frac{1 - D_{ONx_MAX}}{f_{SWx}} = \frac{0.069}{400 \times 10^3} = 173 \times 10^{-9}$$

If $T_{ONx_MIN} \leq t_{SWxONMIN}$

Desired switching frequency (f_{SWx}) will be less than setting frequency and desired Average LED current ($I_{LEDxAVE}$) can be regulated.

If $T_{OFFx_MIN} \leq t_{SWxOFFMIN}$

Desired switching frequency (f_{SWx}) can be nearly fixed value and desired Average LED current ($I_{LEDxAVE}$) will be less than setting value.

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Design Procedure – continued

3 LED Current Setting

Average LED current setting ($I_{LEDxAVE}$) should be lower than maximum average LED current ($I_{LEDxAVE_MAX}$) 2 A.

$$I_{LEDxAVE} = \frac{V_{SNSxAVE100\%H}}{R_{SNSx}} = \frac{0.1915}{R_{SNSx}} \leq I_{LEDxAVE_MAX} = 2$$

$$R_{SNSx} \geq \frac{V_{SNSxAVE100\%H}}{I_{LEDxAVE_MAX}} = \frac{0.1915}{2} = 0.0958$$

Average LED current setting in the LIMP-HOME or STAND-ALONE mode should be lower than 2 A.

$$I_{LEDxAVE}(in\ the\ LIMP\text{-}HOME\ or\ the\ STAND\text{-}ALONE) = \frac{V_{SNSxAVE87\%H}}{R_{SNSx}} = \frac{0.1666}{R_{SNSx}} \leq I_{LEDxAVE_MAX} = 2$$

4 Total LED Current Setting

Recommended Average LED current setting is less than 1.6 A, so that recommended tola LED current ($I_{LEDxAVE_TOTAL}$) is less than 4.8 A for the BD18398RUV-M and 3.2 A for the BD18397RUV-M.
Recommended tola LED current ($I_{LEDxAVE_TOTAL}$) is less than 2.7 A for the BD18397/98EUV-M.

$$I_{LEDxAVE_TOTAL}(for\ the\ BD18397RUV\text{-}M) = I_{LED1AVE} + I_{LED2AVE} \leq 3.2$$
$$I_{LEDxAVE_TOTAL}(for\ the\ BD18398RUV\text{-}M) = I_{LED1AVE} + I_{LED2AVE} + I_{LED3AVE} \leq 4.8$$

$$I_{LEDxAVE_TOTAL}(for\ the\ BD18397EUV\text{-}M) = I_{LED1AVE} + I_{LED2AVE} \leq 2.7$$
$$I_{LEDxAVE_{TOTAL}}(for\ the\ BD18398EUV\text{-}M) = I_{LED1AVE} + I_{LED2AVE} + I_{LED3AVE} \leq 2.7$$

If Average LED current setting of the CH 1 for the BD18398RUV-M is 2.0 A, Average LED current setting of the CH 2 and CH 3 needs lower setting than 1.4 A/channel.

5 Inductor Selection

The inductor is selected to meet recommended inductor peak to peak ripple (ΔI_{LPP} / $I_{LEDxAVE_MAX}$) range (10 % to 100 %). For a stable LED current regulation, required minimum inductor ripple (ΔI_{LPP_MINx}) is more than 10 % (results in 19.1 mV ripple voltage between the SNSPx and SNSNx) to detect inductor bottom current, and required maximum inductor ripple current (ΔI_{LPP_MAX}) is less than 100 % (results in 200 mV ripple voltage between the SNSPx and the SNSNx) for nominal operation without detecting switch-overcurrent-protection (SWOCPx) and LED-current-protection (LOCPx).

$$\frac{\Delta I_{LPP_MAX}}{I_{LEDxAVE_MAX}} = \frac{V_{PIN_MAX}}{4 \times L \times f_{SWx} \times I_{LEDxAVE_MAX}} = \frac{62}{4 \times 33 \times 10^{-6} \times 400 \times 10^{3} \times 2} = 0.587 \leq 1$$

In case of the minimum off time.

$$\frac{\Delta I_{LPP_MIN1}}{I_{LEDxAVE_MAX}} = \frac{V_{SNSPx_MAX}}{L \times I_{LEDxAVE_MAX}} \times T_{OFFx_MIN} = \frac{54}{33 \times 10^{-6} \times 2} \times 173 \times 10^{-9} = 0.141 \geq 0.10$$

In case of the minimum on time.

$$\frac{\Delta I_{LPP_MIN2}}{I_{LEDxAVE_MAX}} = \frac{V_{PIN_MAX} - V_{SNSPx_MIN}}{L \times I_{LEDxAVE_MAX}} \times T_{ONx_MIN} = \frac{62 - 3}{33 \times 10^{-6} \times 2} \times 121 \times 10^{-9} = 0.108 \geq 0.10$$

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Design Procedure - continued

6 Output Capacitor Selection

The minimum output capacitor (C_{OUTx_MIN}) is selected to meet continuous LED current (I_{LEDx}) over LEDs itself to fulfill the LED peak to peak current (I_{LEDx_PP}) is not more than twice the minimum LED current (I_{LEDx_MIN}). The maximum output capacitor (C_{OUTx_MAX}) will be selected to reduce LED peak current (ΔI_{LEDx_PEAK}) into LEDs by discharged capacitor energy over dynamic LED voltage changed (ΔV_{LEDx}).

$$I_{LEDx_PP} \leq 2 \times I_{LEDx_MIN_} = 2 \times 0.2 = 0.4$$

$$C_{OUTx_MIN} = \frac{\Delta I_{LPP_MAX}}{8 \times f_{SWx} \times I_{LEDx_PP} \times R_{LEDx}} = \frac{0.587 \times 2}{8 \times 400 \times 10^3 \times 0.4 \times 2.4}$$

$$= 0.38 \times 10^{-6}$$

$$C_{OUTx_MAX} = \frac{\Delta I_{LEDx_PEAK}}{\Delta V_{LEDx}} \times T_{LEDx} = \frac{1}{54} \times 25 \times 10^{-6} = 0.46 \times 10^{-6}$$

$$\rightarrow C_{OUTx} = 0.47 \times 10^{-6}$$

7 Compensation Capacitor for Constant Current Mode (CC)

Recommended compensation capacitor (C_{COMPx}) and compensation network resister (R_{COMPx}) are selected for fast response against PWM dimming and dynamic voltage changed.

In case of 400 kHz switching frequency.

$$C_{COMPx} = 0.1 \times 10^{-6}$$
$$R_{COMPx} = 1 \times 10^3$$

In case of 2 MHz switching frequency, compensation network resister should not be used.

$$C_{COMPx} = 0.022 \times 10^{-6}$$
$$R_{COMPx} = 0$$

8 Compensation Capacitor for Constant Voltage Mode (CV)

Recommended compensation capacitor (C_{COMPx}) and compensation network resister (R_{COMPx}) are selected for fast response against load changed and total output capacitor (C_{OUTx}) should be increased to reduce voltage drop by load response.

In case of 400 kHz switching frequency.

$$C_{OUTx} = 10 \times 10^{-6}$$
$$C_{COMPx} = 0.1 \times 10^{-6}$$
$$R_{COMPx} = 1 \times 10^3$$

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Typical Application Examples

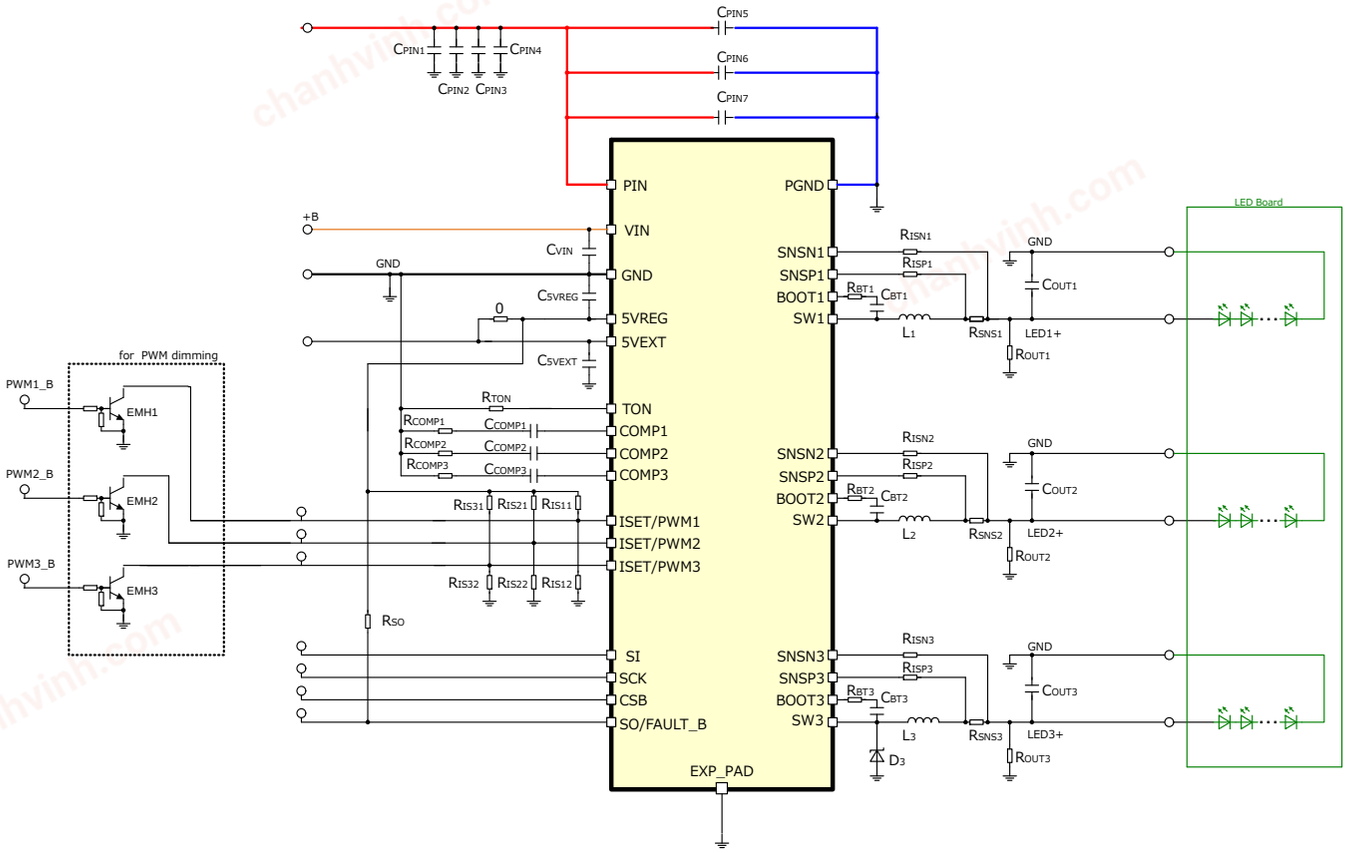


Figure 79. Application Circuit

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Application Parts Choice Examples

Component Name	Component Value	Product Name	Manufacturer
C_{PIN1}	4.7 µF	GCM32DC72A475KE02#_X7S_±10 %	Murata
C_{PIN2}	4.7 µF	GCM32DC72A475KE02#_X7S_±10 %	Murata
C_{PIN3}	4.7 µF	GCM32DC72A475KE02#_X7S_±10 %	Murata
C_{PIN4}	4.7 µF	GCM32DC72A475KE02#_X7S_±10 %	Murata
C_{PIN5}	0.1 µF	GCJ188R72A104KA01#_X7R_±10 %	Murata
C_{PIN6}	0.1 µF	GCJ188R72A104KA01#_X7R_±10 %	Murata
C_{PIN7}	0.1 µF	GCJ188R72A104KA01#_X7R_±10 %	Murata
C_{VIN}	1.0 µF	GCM21BR71H105KA01#_X7R_±10 %	Murata
C_{5VREG}	4.7 µF	GCM21BR71C475KA67#_X7R_±10 %	Murata
C_{5VEXT}	4.7 µF	GCM21BR71C475KA67#_X7R_±10 %	Murata
C_{COMPx}	0.1 µF	GCM188L81H104KA57#_X8L_±10 %	Murata
C_{BTx}	2.2 µF	GCM188C71A225KE01#_X7S_±10 %	Murata
C_{OUTx}	0.22 µF x 2 (CC mode)	GCM31MR72A224KA01#_X7R_±10 %	Murata
	4.7 µF x 2 (CV mode)	GCM32DC72A475KE02#_X7S_±10 %	Murata
R_{TON}	51 kΩ	MCR03	ROHM
R_{COMPx}	0 Ω (CC mode)	MCR03	ROHM
	4.7 kΩ (CV mode)	MCR03	ROHM
R_{SO}	4.7 kΩ	MCR03	ROHM
R_{ISNx}	1 kΩ	MCR03	ROHM
R_{ISPx}	1 kΩ	MCR03	ROHM
R_{SNSx}	0.091 Ω	LTR18	ROHM
R_{BTx}	4.7 Ω	MCR03	ROHM
R_{OUTx}	47 kΩ	MCR03	ROHM
R_{ISx1}	Open (CC mode)	-	-
	47 kΩ (CV mode)	MCR03	ROHM
R_{Isx2}	10 kΩ (CC mode)	MCR03	ROHM
	Open (CV mode)	-	-
L_x	22 µH	XAL5050-223ME	Coil Craft
D_3	100 V, 2A	RB068MM100TF	ROHM
EMHx	-	DTC144EE	ROHM

(x = 1, 2, 3)

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Application Typical Waveforms

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V)

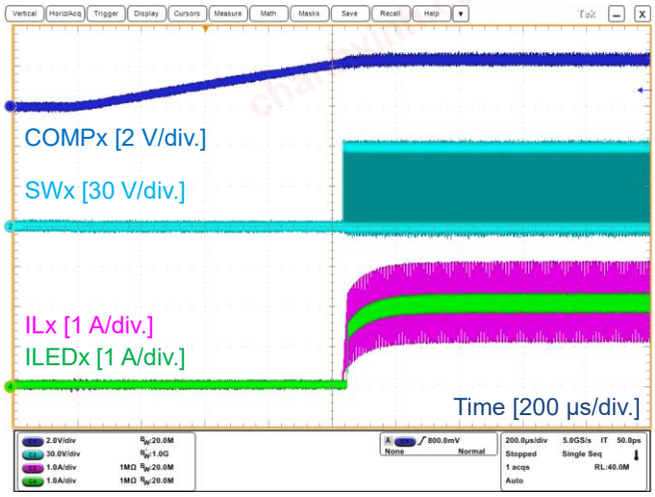


Figure 80. ON Sequence
(C_{COMPx} = 0.1 µF)

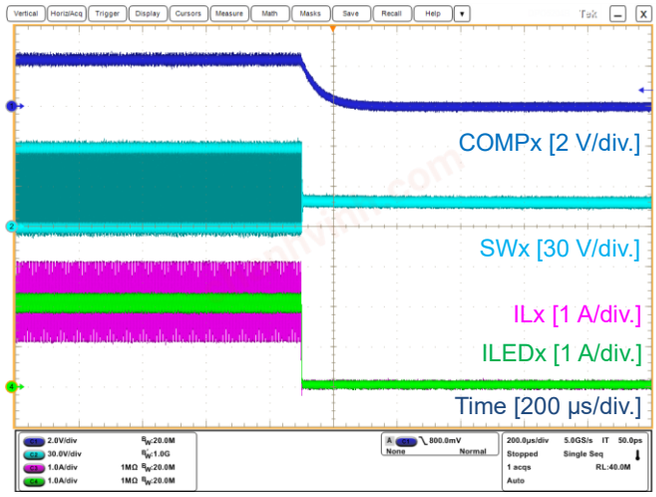


Figure 81. OFF Sequence
(C_{COMPx} = 0.1 µF)

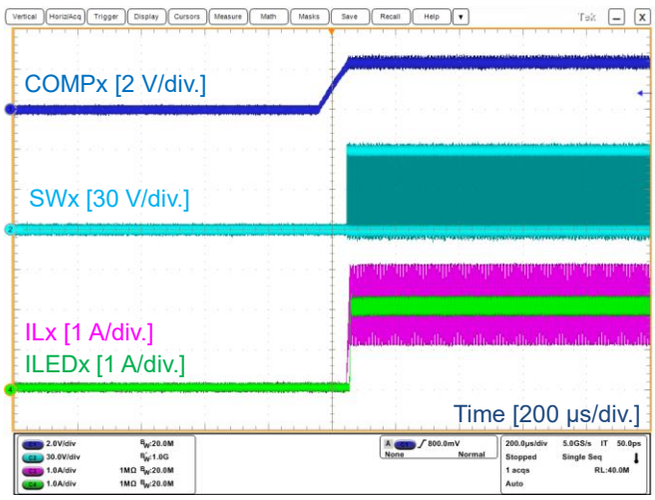


Figure 82. ON Sequence
(C_{COMPx} = 10 nF)

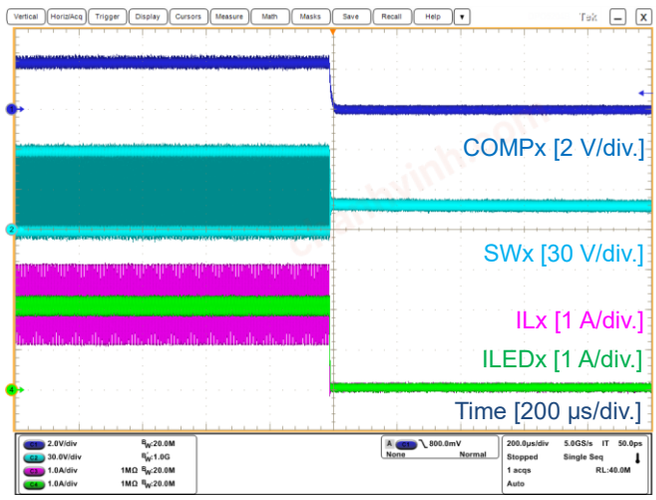


Figure 83. OFF Sequence
(C_{COMPx} = 10 nF)

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Application Typical Waveforms - continued

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V)

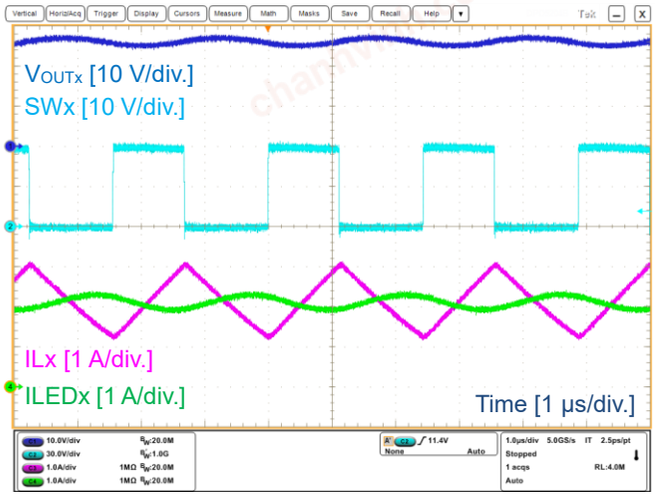


Figure 84. Normal Operation

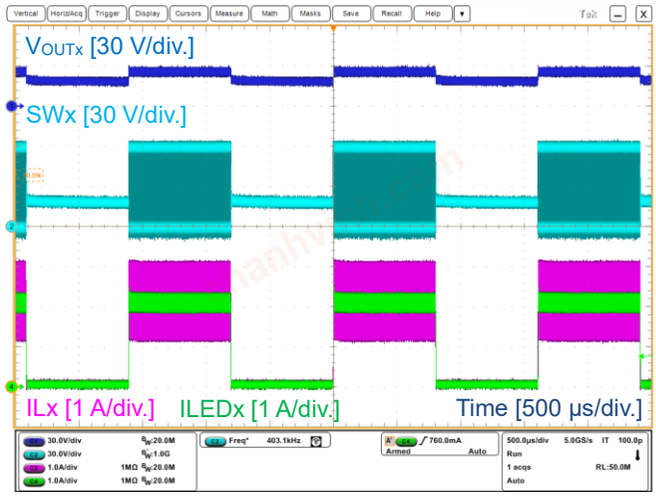


Figure 85. PWM Dimming Operation

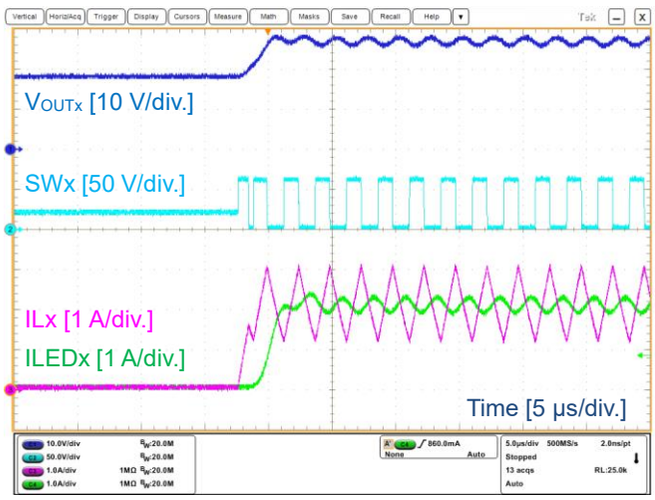


Figure 86. Internal PWM Dimming (Rising Edge)

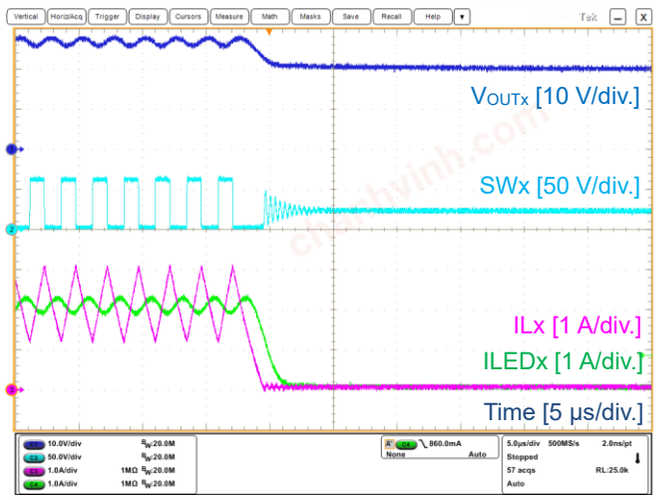


Figure 87. Internal PWM Dimming (Falling Edge)

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Application Typical Waveforms - continued

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V)

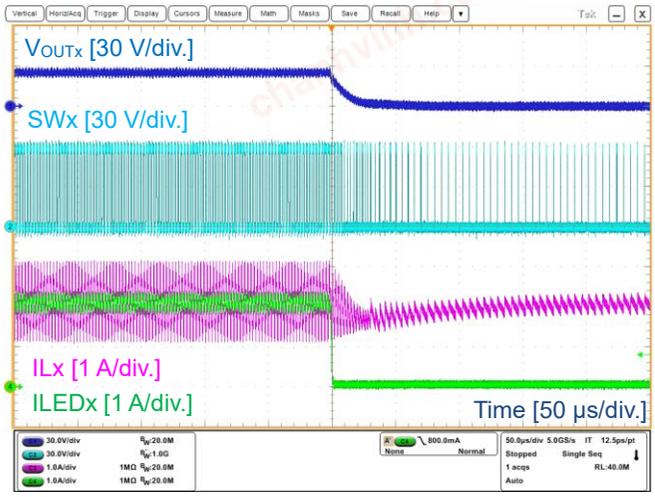


Figure 88. Output Short Circuit Fault
(C_{COMPx} = 0.1 µF)

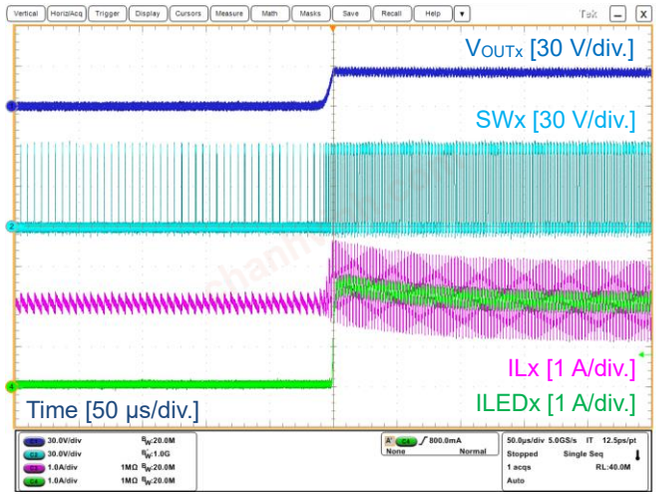


Figure 89. Output Short Circuit Fault Recovery
(C_{COMPx} = 0.1 µF)

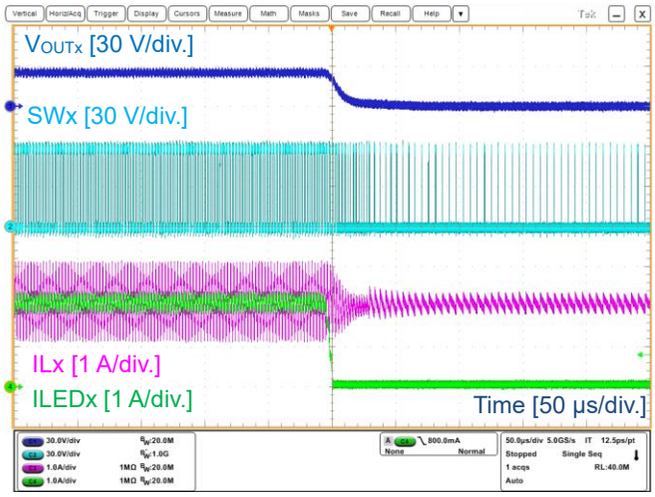


Figure 90. Output Short Circuit Fault
(C_{COMPx} = 10 nF)

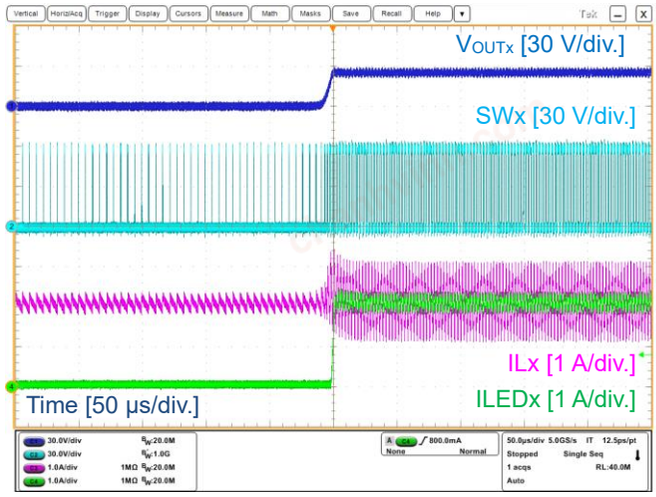


Figure 91. Output Short Circuit Fault Recovery
(C_{COMPx} = 10 nF)

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Application Typical Waveforms - continued

(Unless otherwise specified V_{IN} = 13 V, V_{PIN} = 60 V, V_{5VEXT} = 5 V)

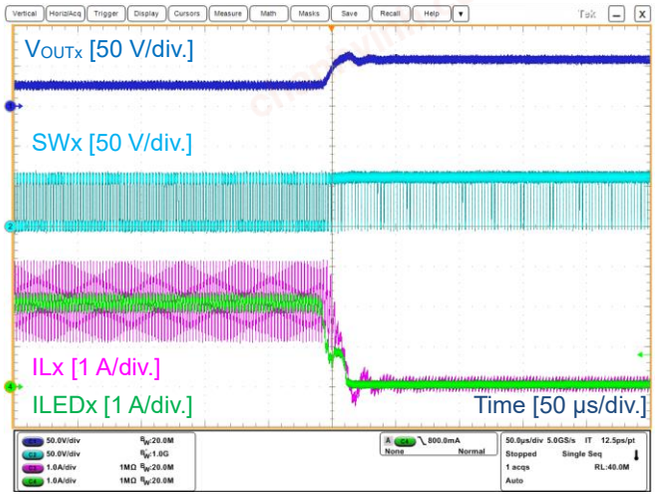


Figure 92. Output Open Circuit Fault
(C_{COMPx} = 0.1 µF)

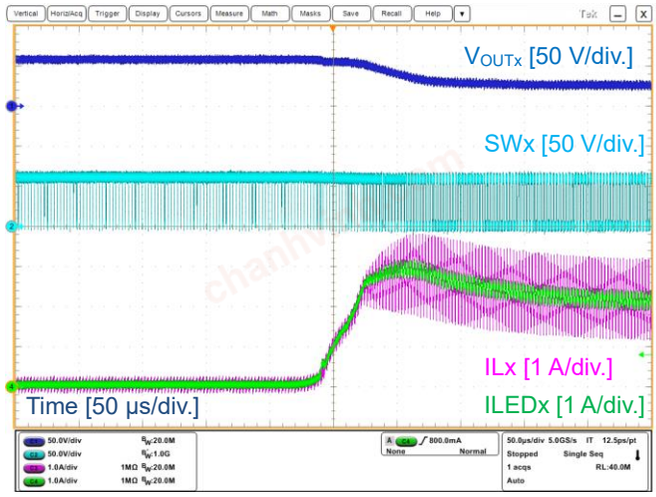


Figure 93. Output Open Circuit Fault Recovery
(C_{COMPx} = 0.1 µF)

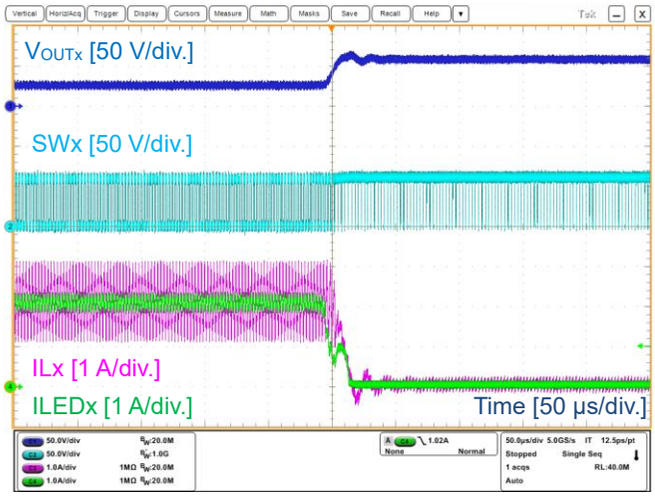


Figure 94. Output Open Circuit Fault
(C_{COMPx} = 10 nF)

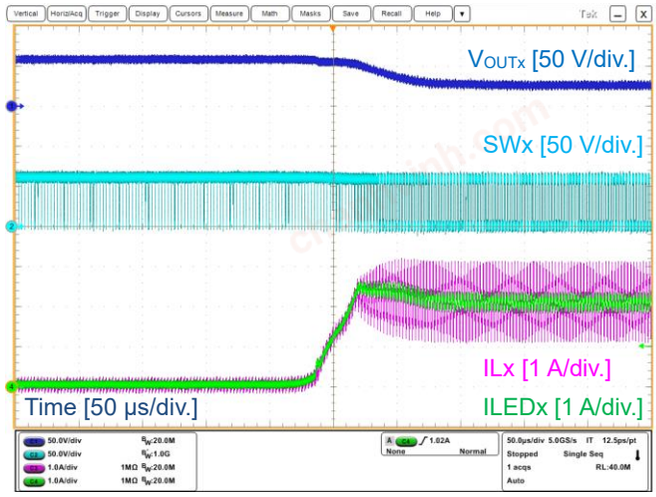
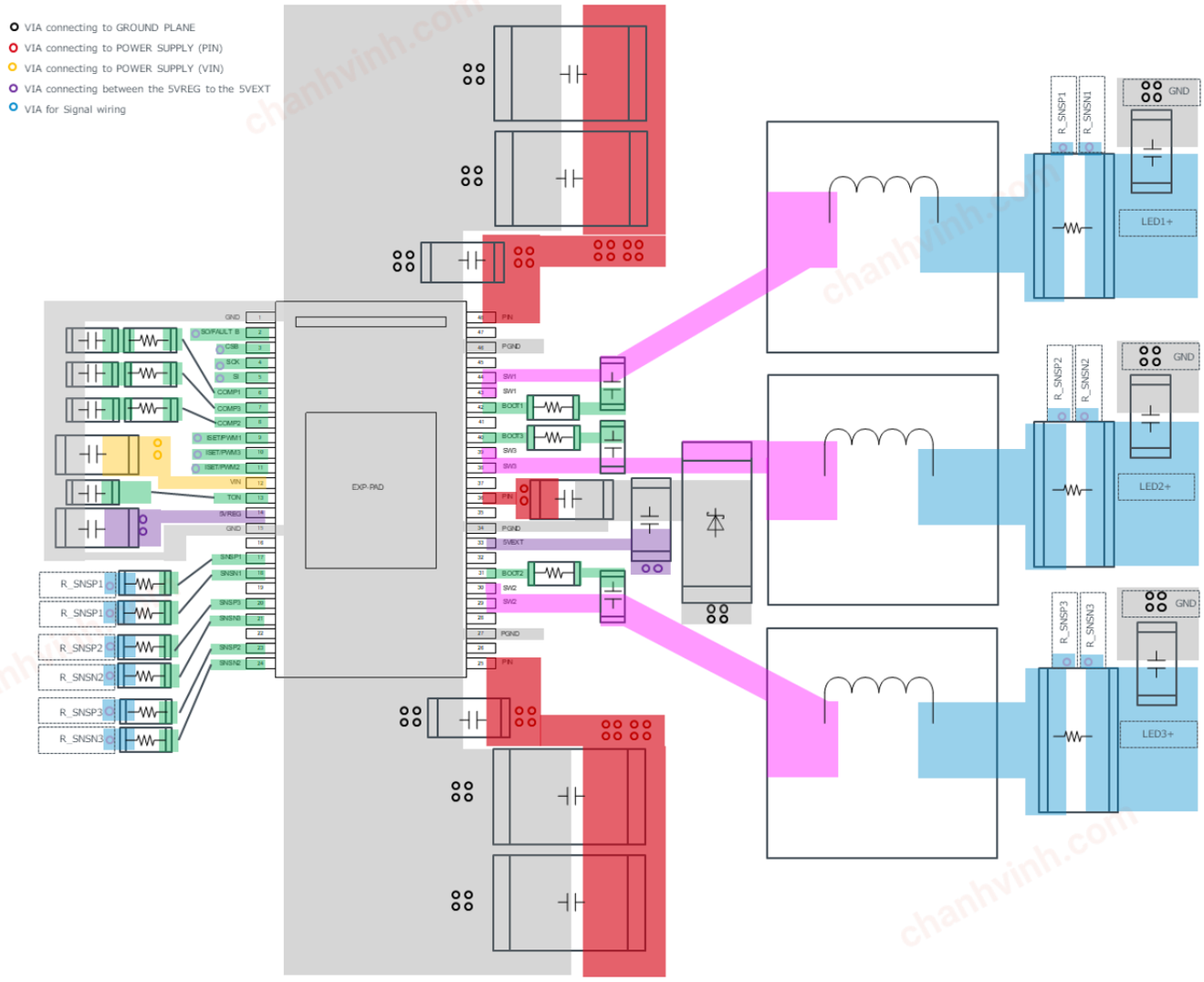


Figure 95. Output Open Circuit Fault Recovery
(C_{COMPx} = 10 nF)

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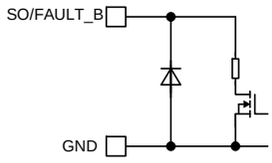
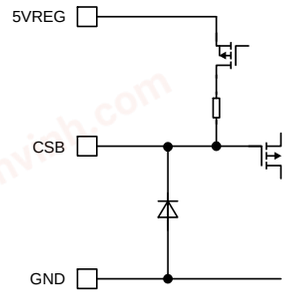
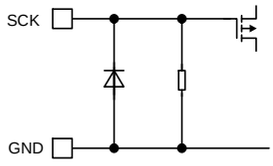
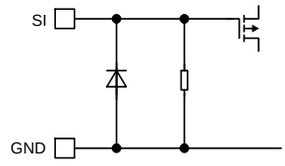
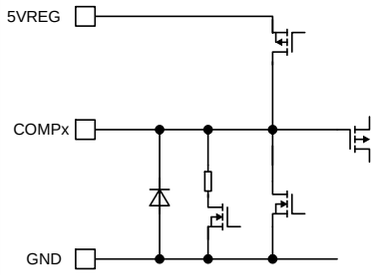
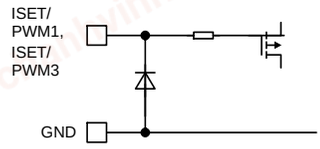
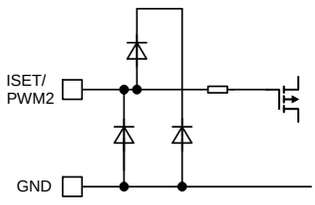
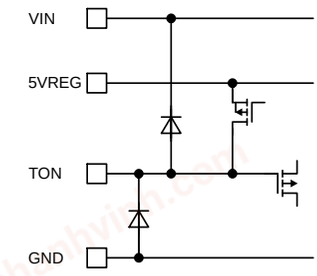
Layout Example



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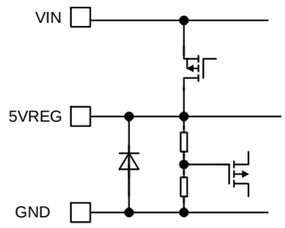
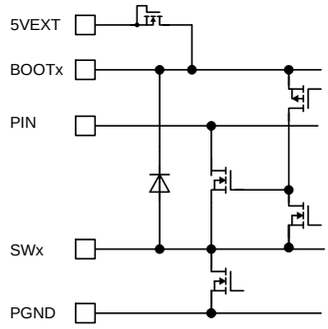
I/O Equivalence Circuits

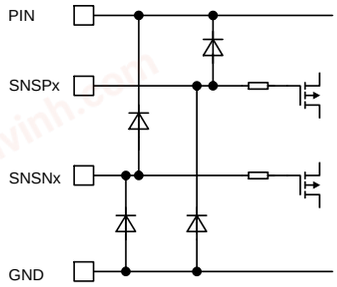
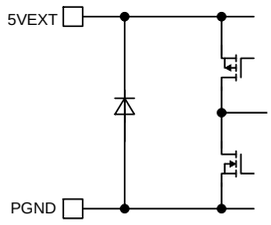
Pin No. HTSSOP-C48R	Pin No. HTSSOP-C48	Pin Name	I/O Equivalence Circuit	Pin No. HTSSOP-C48R	Pin No. HTSSOP-C48	Pin Name	I/O Equivalence Circuit
2	23	SO/ FAULT_ B		3	22	CSB	
4	21	SCK		5	20	SI	
6 7 8	19 18 17	COMP1 (Note 1) COMP3 COMP2		9 10	16 15	ISET/ PWM1 (Note 1) ISET/ PWM3	
11	14	ISET/ PWM2		13	12	TON	

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I/O Equivalence Circuits – continued

Pin No. HTSSOP-C48R	Pin No. HTSSOP-C48	Pin Name	I/O Equivalence Circuit
14	11	5VREG	
29,30	43,44	SW2	
38,39	34,35	SW3 (Note 1)	
43,44	29,30	SW1	
31	42	BOOT2	
40	33	BOOT3 (Note 1)	
42	31	BOOT1	

Pin No. HTSSOP-C48R	Pin No. HTSSOP-C48	Pin Name	I/O Equivalence Circuit
17	8	SNSP1 (Note 1)	
20	5	SNSP3	
23	2	SNSP2	
18	7	SNSN1	
21	4	SNSN3 (Note 1)	
24	1	SNSN2	
33	40	5VEXT	

(Note 1) BD18397: COMP3, ISET/PWM3, SNSP3, SNSN3, SW3, BOOT3 = N.C.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

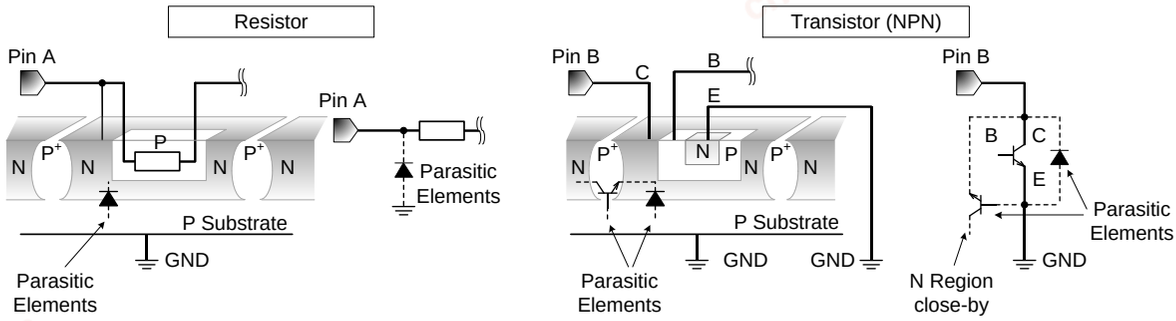


Figure 96. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

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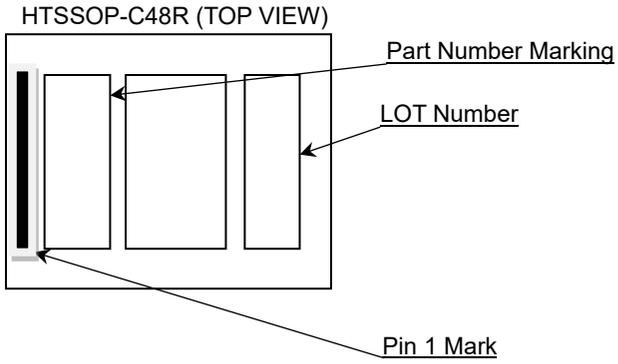
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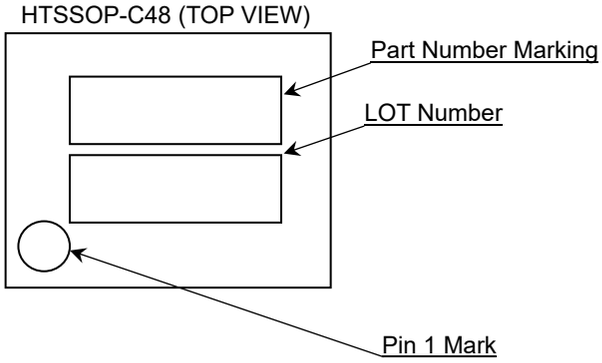
Ordering Information

B D 1 8 3 9 x x x x - M E 2

- Output Channel: 7: 2 channel; 8: 3 channel
- Package: RUV: HTSSOP-C48R; EUV: HTSSOP-C48
- Product Rank: M: for Automotive
- Packaging and forming specification: E2: Embossed tape and reel

Marking Diagrams





Lineup

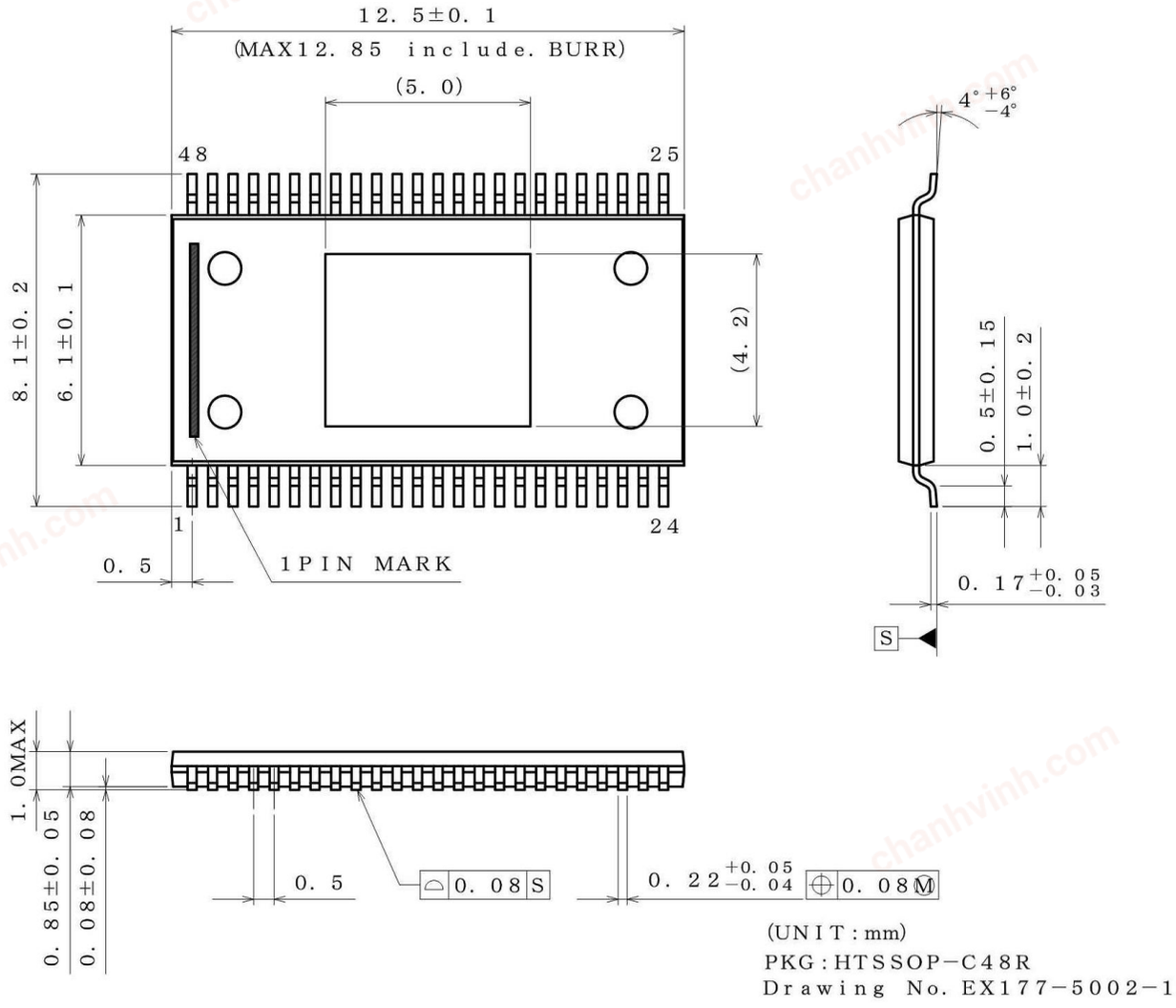
Output Channel	Part Number Marking	Package	Orderable Part Number
2 ch	BD18397	HTSSOP-C48R	BD18397RUV-ME2
	BD18397EUV	HTSSOP-C48	BD18397EUV-ME2
3 ch	BD18398	HTSSOP-C48R	BD18398RUV-ME2
	BD18398EUV	HTSSOP-C48	BD18398EUV-ME2

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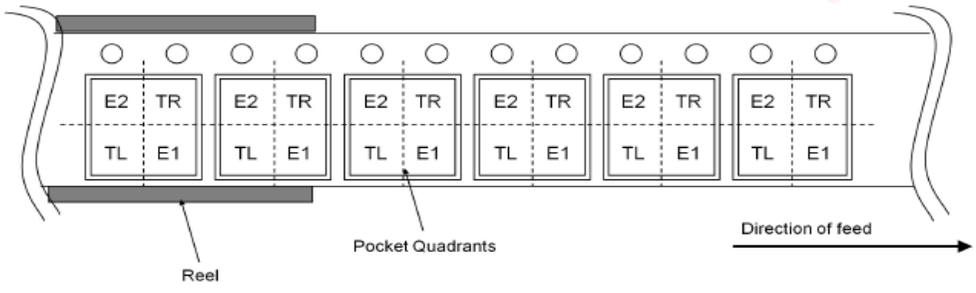
Physical Dimension and Packing Information

Package Name	HTSSOP-C48R



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand

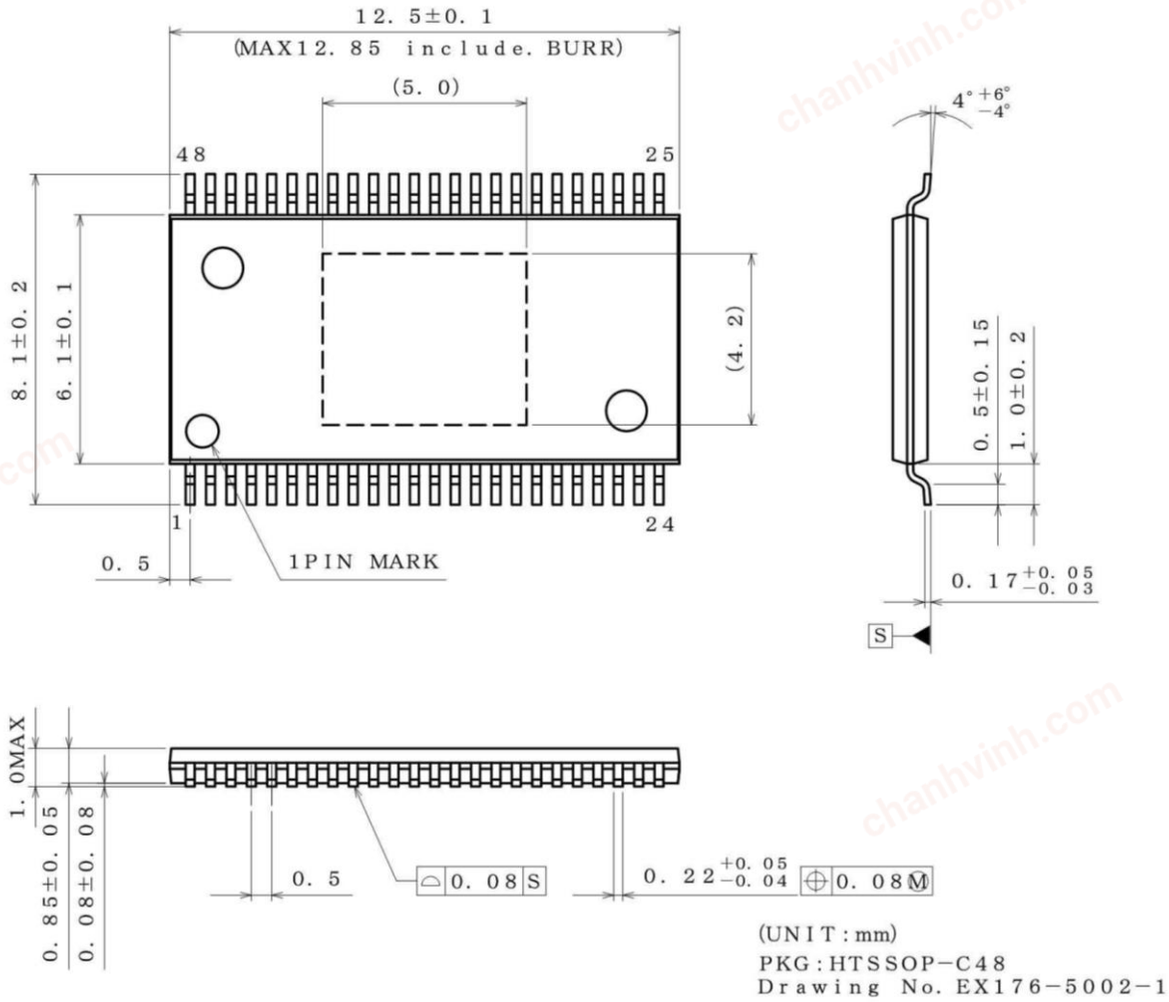


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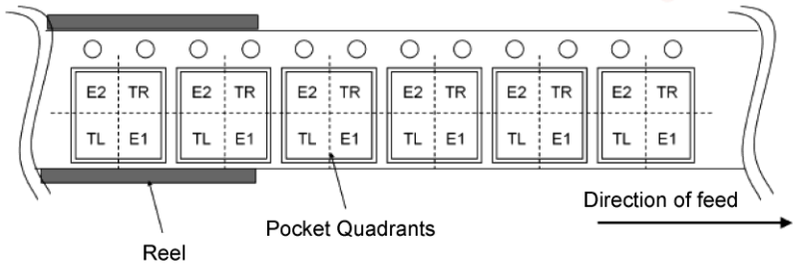
Physical Dimension and Packing Information – continued

Package Name	HTSSOP-C48



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
15.Feb.2022	001	New Release
01.Mar.2023	002	Adding Lineup Before: BD18397RUV-M, BD18398RUV-M After: BD18397RUV-M, BD18398RUV-M, BD18397EUV-M, BD18398EUV-M P1 updating Key Specification LED Output Voltage Range Before: 2 V to 60 V After: 2.5 V to 60 V P1 updating Typical Application Circuit Figure 1. Typical Application Circuit P3 updating Pin Descriptions BOOT1, BOOT2, BOOT3 Before: Connecting boot strap capacitor After: Connecting series resister and boot strap capacitor SW1, SW2, SW3 Adding description: Connecting schottky barrier diode to the SW3 pin. 5VREG Before: 2.2 µF After: 4.7 µF 5VEXT Before: 2.2 µF After: 4.7 µF P4 updating Bock Diagram Figure 4. Block Diagram P6 updating Thermal Resistance Adding item: HTSSOP-C48 for BD1839xEUV-M P7 updating Recommended Operating Conditions Note 2 Before: Schottky Barrier Diodes between After: Schottky Barrier Diodes should be needed between Adding item: PWM Dimming off Pulse Width and Note 6 Adding item: Continuous Total Average LED Current for BD1839xEUV-M P8 updating Recommended Setting Parts Range Adding item: R_{BTx} and Note 2 P14 updating Description of Blocks > Buck Converter LED Current Regulation Before: by the real time sensing V_{PIN} and V_{SNSNx} voltage. After: by the real time sensing V_{PIN} and V_{SNSPx} voltage. P15 updating Description of Blocks > LED Current Setting (Current Sense) Figure 7. LED Current Setting P16 updating Description of Blocks > DCDC Switching Frequency T_{ONx} Before: $k / (TONx[5:0] +1) \times R_{TON} \times V_{SNSPx} / V_{PIN} + 20 \times 10^{-9}$ After: $k / (TONx[5:0] +1) \times R_{TON} \times V_{SNSPx} / V_{PIN} \times 10^{-6} + 20 \times 10^{-9}$ f_{swx} Before: $1 / (k / (TONx[5:0] +1) \times R_{TON} \times V_{SNSPx} / V_{PIN} + 20 \times 10^{-9}) \times V_{SNSPx} / V_{PIN}$ After: $1 / (k / (TONx[5:0] +1) \times R_{TON} \times V_{SNSPx} / V_{PIN} \times 10^{-6} + 20 \times 10^{-9}) \times V_{SNSPx} / V_{PIN}$

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Revision History – continued

Date	Revision	Changes
01.Mar.2023	002	P20 updating Description of Blocks > Bootstrap Charge Adding description: When turning on the corresponding channel, the output voltage must be sufficiently discharged (V_{OUTx} < 1.5 V) before turning on the corresponding channel (CHONx = 1) to ensure that the bootstrap voltage is above the recommended operating voltage (V_{BTSWx} > 3.5 V). P24 updating Description of Blocks > Abnormal Detection/Protection Function 5VREG 5VEXT UVLO Before: V5VREG ≥ 4.5 V or V5VEXT ≥ 4.5 V After: V5VREG ≥ 4.2 V or V5VEXT ≥ 4.2 V P25 updating Description of Blocks > Under Voltage Locked Out (UVLO) Before: When detecting a UVLO by the V_{IN} or V_{5VREG} or V_{5VEXT}, After: When detecting a UVLO by the V_{IN} or V_{5VREG} or V_{5VEXT} or V_{PIN}, P26 updating Description of Blocks > SW Over Current Protection (SWOCPx) Figure 20. SW Over Current Protection Waveform P27 updating Description of Blocks > LED Open Detection Figure 21. LED Open Detection Waveform P28 updating Description of Blocks > LED Short to GND Detection Figure 22. LED Short to GND Detection Waveform P31 updating Description of Blocks > SPI Protocol and AC Electrical Characteristics Adding description: SI data is outputted with 24 bits shift from SO/FAULT_B. SO/FAULT_B keeps Hi-z when CSB = high. P33 updating Description of Blocks > SPI Protocol and AC Electrical Characteristics > SPI AC Timing Adding item: NOTE (Countermeasure of Noise) Adding item: Figure 29. Countermeasure of Noise P34 updating Description of Blocks > SPI Protocol and AC Electrical Characteristics > SPI Protocol > CRC Adding description: (It doesn't change value until '1' input because initial 0. (The result of "011111111111111111111111" (binary) is same as result of "111111111111111111111111".)) P41 updating Description of Blocks > Register > Description of Registers initial value of Address 0x00: SYSSET Before: initial value 0x00 After: initial value 0x40 P43 updating Description of Blocks > Register > Description of Registers Description of Address 0x03: DIMSET bit[7] PHEN Before: as shown in Figure 41. After: as shown in Figure 44. P44 updating Description of Blocks > Register > Description of Registers Description of Address 0x04 & 0x05 Removing description: If you want to change value during dimming, WLOCK function can be used.

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Revision History – continued

Date	Revision	Changes
01.Mar.2023	002	P45 updating Description of Blocks > Register > Description of Registers Table 15. DC/DC GM Amplifier Trans Conductance Setting GM1[1:0] = 0 Before: 1200 After: 1360 GM1[1:0] = 1 Before: 750 After: 870 GM1[1:0] = 2 Before: 430 After: 530 GM1[1:0] = 3 Before: 240 After: 300 P57 updating Sequence > Start-up and Turn-off Sequence > Error Sequence for “WDT Error” Description of Error Sequence for “WDT Error” ① Removing description: and SO/FAULT_B output is set to low P66 updating Design Procedure > Total LED Current Setting Adding description and formula for BD1839xEUV-M P66 updating Design Procedure >Inductor Selection Before: in case of the minimum on time After: in case of the minimum off time Before: in case of the maximum on time After: in case of the minimum on time P68 updating Typical Application Examples Figure 79. Application Circuit P69 updating Application Parts Choice Example C_{OUTx} Before: 10 µF, GCM31MR72A224KA01#_X7R_±10 % After: 4.7 µF x 2, GCM32DC72A475KE02#_X7S_±10 % Lx Before: XAL8050-223ME After: XAL5050-223M D_3 Before: RB068LAM100 After: RB068MM100TF Adding item: R_{BTx} P74 updating Layout Example P75 updating I/O Equivalence Circuits Adding item: New package Pin No. P79 updating Ordering Information and Marking Diagram and Lineup Adding item: HTSSOP-C48 for BD1839xEUV-M P81 updating Physical Dimension and Packing Information Adding item: HTSSOP-C48 for BD1839xEUV-M

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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