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ROHM SEMICONDUCTOR

Datasheet

Constant Current LED Drivers for Automotive

Constant Current Controller for Automotive LED Lamps

BD18340FV-M BD18341FV-M

General Description

BD18340FV-M/BD18341FV-M are 70V-withstanding Constant Current Controller for Automotive LED Lamps. It is able to drive at maximum 10 rows of PNP transistors. It can also contribute to reduction in the consumption power of the set as it has the integrated standby function., The IC also incorporates a highly reliable, in-built de-rating function, LED Open Detection, Short Circuit Protection and Over Voltage Mute function and LED failure input/output function.

Features

- ■AEC-Q100 Qualified(Note1)
- ■LED Constant-Current Controller
- ■PWM Dimming Function
- ■LED Current De-rating Function
- ■LED Open Detection
- ■Short Circuit Protection(SCP)
- ■Over Voltage Mute Function(OVM)
- ■Disable LED Open Detection Function at Reduced-Voltage
- ■Abnormal Output Detection and Output Functions

(Note1: Grade1)

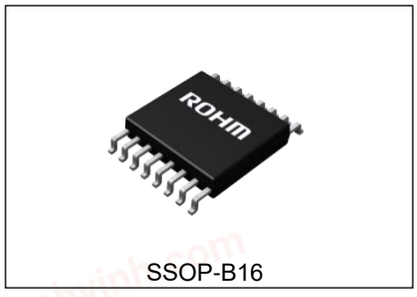
Applications

- ■ Automotive LED Exterior Lamp (Rear Lamp, Turn Lamp, DRL/Position Lamp, Fog Lamp etc.)
- ■ Automotive LED Interior Lamp (Air Conditioner Lamp, Interior Lamp, Cluster Light etc.)

Key Specifications

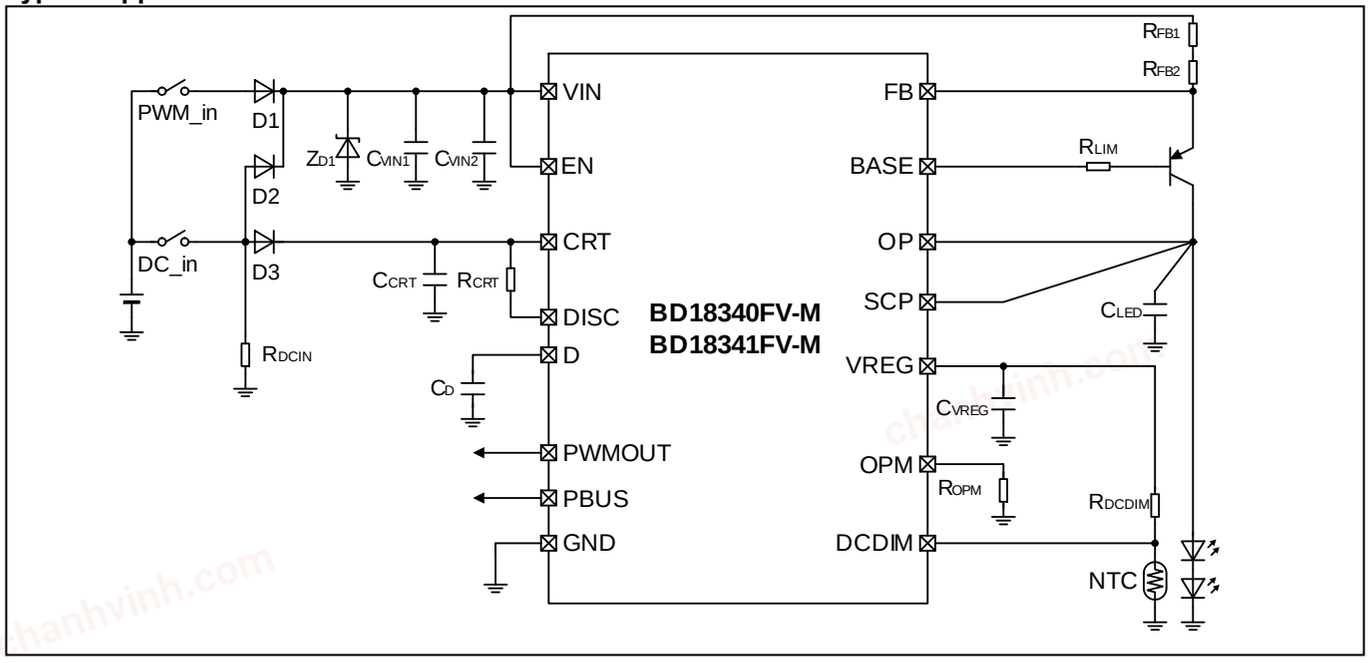
- ■Input Voltage Range: 4.5V to 19V
- ■FB Terminal Voltage Accuracy: 650mV ±3% @Ta = 25°C to 125°C
- ■Stand-by Current: 0μA(Typ)
- ■LED Current De-rating Accuracy:
  - BD18340FV-M: ±5% @V_{DCDIM}=0.5 to 0.75V
  - BD18341FV-M: ±12% @V_{DCDIM}=0.5 to 0.75V
- ■Operating Temperature Range: -40°C to +125°C

Package	W(Typ) x D(Typ) x H(Max)
SSOP-B16	5.00mm x 6.40mm x 1.35mm



SSOP-B16

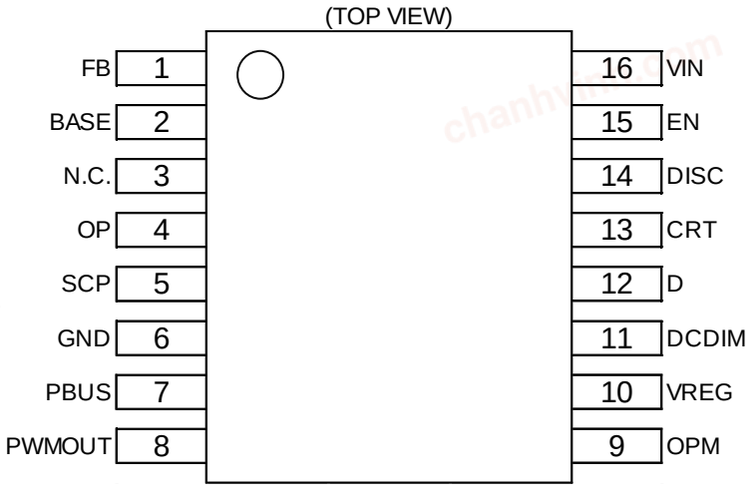
Typical Application Circuit



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Pin Configuration

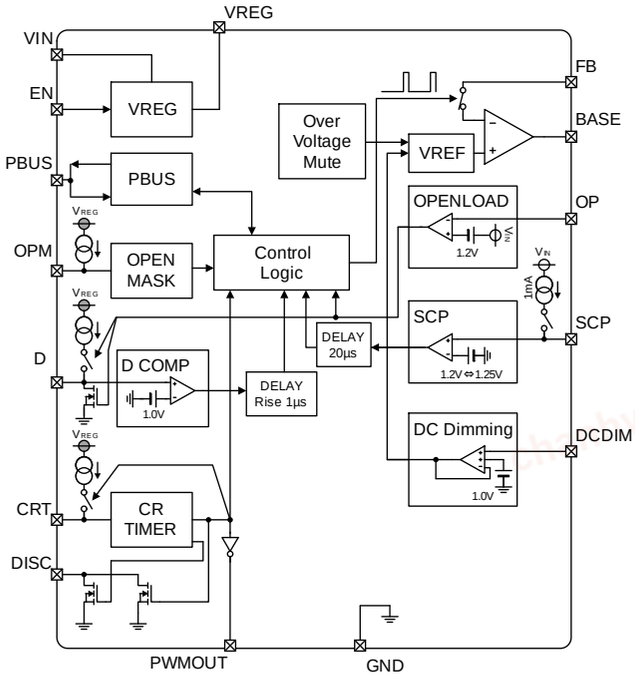


Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	FB	Input terminal for feedback voltage	9	OPM	The terminal to set Disable LED open detection voltage
2	BASE	The terminal for connecting PNP Tr. BASE	10	VREG	Internal reference voltage
3	N.C.	Pin not connected internally. (Note 1)	11	DCDIM	The terminal to set DC dimming
4	OP	The terminal for LED open detection	12	D	The terminal to set Disable LED open detection time
5	SCP	The terminal for short circuit protection	13	CRT	The terminal to set CR timer
6	GND	GND	14	DISC	Discharge terminal for CR timer
7	PBUS	The terminal Abnormal Output Detection and Output	15	EN	Enable input
8	PWMOUT	CR timer signal output	16	VIN	Power supply input

(Note 1) Please be sure to floating at N.C. pin

Block Diagram



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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{IN}	-0.3 to +70	V
EN,CRT, DISC Terminal Voltage	V_{EN}, V_{CRT}, V_{DISC}	-0.3 to +70	V
FB,BASE,OP,SCP Terminal Voltage	V_{FB}, V_{BASE}, V_{OP},V_{SCP}	-0.3 to V_{IN}+0.3V	V
VIN-FB, VIN-BASE Voltage across Terminals	V_{IN}-V_{FB},V_{IN}-V_{BASE}	-0.3 to +5.0	V
PBUS,VREG DCDIM Terminal Voltage	V_{PBUS}, V_{REG}, V_{DCDIM}	-0.3 to +7.0	V
PWMOUT, OPM, D Terminal Voltage	V_{PWMOUT}, V_{OPM}, V_D	-0.3 to V_{REG}+0.3	V
Operating Temperature Range	T_{opr}	-40 to 125	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C
Junction Temperature	T_{jmax}	150	°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance (Note2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note4)	2s2p(Note5)	
SSOP-B16				
Junction to Ambient	θ_{JA}	140.9	77.2	°C/W
Junction to Top Characterization Parameter (Note 3)	Ψ_{JT}	6	5	°C/W

(Note2) Based on JESD51-2A (Still-Air),
(Note3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note4) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note5) Using a PCB board based on JESD51-7

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

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Recommended Operating Conditions (Ta=-40°C to +125°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage(Note1) (Note2)	V_{IN}	4.5	13	19	V
CRTIMER Frequency Range	f_{PWM}	100	-	5000	Hz
PWM Minimum Pulse Width(Note3)	t_{MIN}	10	-	-	μs

(Note1) ASO should not be exceeded
(Note2) At start-up time, please apply a voltage above 5V once. The value is the voltage range after the temporary rise to 5V.
(Note3) At connecting the External PNP Tr.(2SAR573D3FRA(ROHM) ,1pcs), That is the same when the Pulse input to CRT terminal.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
The Capacitor connecting VIN Terminal1	C_{VIN1}	1.0	-	μF
The Capacitor connecting VIN Terminal2	C_{VIN2}(Note4)	0.047	-	μF
The Capacitor connecting VREG Terminal	C_{VREG}(Note5)	1.0	4.7	μF
The Capacitor connecting LED Anode	C_{LED}	0.1	0.68	μF
The Capacitor connecting CRT Terminal	C_{CRT}	0.01	0.22	μF
The Resistor connecting CRT Terminal	R_{CRT}	0.1	50	kΩ
The Resistor for setting LED Current LED	R_{FB1}, R_{FB2} (Note6)	0.8	6.5	Ω
The Resistor for setting Disable LED Open Detection Voltage	R_{OPM}	25	55	kΩ
The Resistor for setting DC Dimming	R_{DCDIM}	4.7	50	kΩ
The Resistor for DCIN pull-down	R_{DCIN}	-	10	kΩ
The Capacitor for setting Disable LED Open Detection Time	C_D(Note5)	0.001	0.1	μF
The Resistor for limiting Base Terminal Current	R_{LIM}	See Features Description 5		Ω
The External PNP Transistor	Q_1	(Note7)		-

(Note4) ROHM Recommended Value (0.1μF GCM155R71H104KE37 murata)
(Note5) Ceramic capacitor recommended. Please setting the Disable LED Open Detection Time less than PWM minimum pulse width.
(Note6) At connecting the External PNP Tr. (2SAR573D3FRA (ROHM), 1pcs)
(Note7) For external PNP transistor, please use the recommended device 2SAR573D3FRA for this IC.
While using non-recommended part device, validate the design on actual board.
Please check hfe of the part to design base current limit resistor. (See Features Description, section 5).
As for parasitic capacitance, please evaluate over shoot of I_{LED} on actual board. (See Features Description, Section 8 -Evaluation example, ILED pulse width at PWM Dimming operation).

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Electrical Characteristics1

(Unless otherwise specified Ta = -40 to +125°C, V_{IN} = 13V, C_{VREG} = 1.0µF, Transistor PNP = 2SAR573D3FRA)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Circuit Current I_{VIN}]						
Circuit Current at Stand-by Mode	I_{VIN1}	-	0	10	µA	V_{EN} = 0V V_{FB}=V_{IN}
Circuit Current at Normal Mode	I_{VIN2}	-	2.0	5.0	mA	V_{EN} = V_{IN}, V_{FB}=V_{IN}-1.0V Base current subtracted
Circuit Current at LED Open Detection	I_{VIN3}	-	2.0	5.0	mA	V_{EN} = V_{IN}, V_{FB}=V_{IN}-1.0V at LED Open Detection
Circuit Current at PBUS=Low	I_{VIN4}	-	2.0	5.0	mA	V_{EN} = V_{IN}, V_{FB}=V_{IN}-1.0V V_{PBUS} = 0V
[VREG Voltage]						
VREG Terminal Voltage	V_{REG}	4.85	5.00	5.15	V	I_{VREG} = -100µA
VREG Terminal Current Capability	I_{VREG}	-1.0	-	-	mA	
[DRV]						
FB Terminal Voltage	V_{FBREG}	630	650	670	mV	V_{FBREG} = V_{IN} - V_{FB} R_{FB1} = R_{FB2} = 1.8Ω, Ta = 25 to 125°C
		617	650	683	mV	V_{FBREG} = V_{IN} - V_{FB} R_{FB1} = R_{FB2} = 1.8Ω, Ta = -40 to 125°C
FB Terminal Input Current	I_{FB}	7.5	15	30	µA	V_{FB} = V_{IN}
BASE Terminal Sink Current Capability	I_{BASE}	10	-	-	mA	V_{FB} = V_{IN}, V_{BASE} = V_{IN} - 1.5V Ta = 25°C
BASE Terminal Pull-up Resistor	R_{BASE}	0.5	1.0	1.5	kΩ	V_{CRT} = 0V V_{FB} = V_{IN}, V_{BASE} = V_{IN} - 1.0V
[LED Current De-rating Function (DC Dimming Function)]						
DC Dimming Gain	D_{DG}	688	725	762	mV / V	ΔV_{FBREG} / ΔV_{DCDIM} V_{DCDIM}: 0.75V -> 0.35V
BD18340FV-M						
FB Terminal Voltage V_{DCDIM} = 0.75V	V_{FB_DC1}	443	466	489	mV	
FB Terminal Voltage V_{DCDIM} = 0.50V	V_{FB_DC2}	270	284	298	mV	
FB Terminal Voltage V_{DCDIM} = 0.35V	V_{FB_DC3}	161	175	189	mV	
BD18341FV-M						
FB Terminal Voltage V_{DCDIM} = 0.75V	V_{FB_DC1}	413	466	522	mV	
FB Terminal Voltage V_{DCDIM} = 0.50V	V_{FB_DC2}	250	284	318	mV	
FB Terminal Voltage V_{DCDIM} = 0.35V	V_{FB_DC3}	155	175	196	mV	
[Over Voltage Mute Function(OVM)]						
Over Voltage Mute Start Voltage	V_{OVMS}	20.0	22.0	24.0	V	ΔV_{FB} = 10.0mV ΔV_{FB} = V_{FB}(@V_{IN} = 13V) – V_{FB}(@V_{IN} = V_{OVM})
Over Voltage Mute Gain	V_{OVMG}	-	-25	-	mV / V	ΔV_{FB} / ΔV_{IN}

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Electrical Characteristics2

(Unless otherwise specified Ta = -40 to +125°C, V_{IN} = 13V, C_{VREG} = 1.0µF, Transistor PNP = 2SAR573D3FRA)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[CRTIMER]						
CRT Terminal Charge Current	I_{CRT}	36	40	44	µA	
CRT Terminal Charge Voltage	V_{CRT_CHA}	0.72	0.80	0.88	V	
CRT Terminal Discharge Voltage 1	V_{CRT_DIS1}	1.80	2.00	2.20	V	
CRT Terminal Discharge Voltage 2	V_{CRT_DIS2}	2.10	2.40	3.00	V	When $V_{CRT} > V_{CRT_DIS2}$, R_{D1} -> R_{D2}
CRT Terminal Charge Resistor	R_{CHA}	28.5	30.0	31.5	kΩ	R_{CHA}= (V_{CRT_DIS1}- V_{CRT_CHA})/ I_{CRT}
CR Timer Discharge Constant	V_{CRT_CHA} / V_{CRT_DIS1}	0.38	0.40	0.42	V / V	
DISC Terminal ON Resistor 1	R_{DISC1}	20	50	100	Ω	I_{DISC} = 10mA
DISC Terminal ON Resistor 2	R_{DISC2}	2.5	5.0	10	kΩ	I_{DISC} = 100µA
PWMOUT Terminal Output High Voltage	$V_{PWMOUTH}$	4.0	-	5.5	V	I_{PWMOUT} = -100µA
PWMOUT Terminal Output Low Voltage	$V_{PWMOUTL}$	-	-	0.5	V	I_{PWMOUT} = 100µA
PWMOUT Terminal Sink Current Capability	I_{PWMOUT_SINK}	-	-	0.5	mA	
PWMOUT Terminal Source Current Capability	I_{PWMOUT_SOURCE}	-0.5	-	-	mA	
CRT Terminal Leakage Current	I_{CRT_LEAK}	-	-	10	µA	V_{CRT} = 70V
[LED Open Detection]						
LED Open Detection Voltage	V_{OPD}	1.1	1.2	1.3	V	$V_{OPD} = V_{IN} - V_{OP}$
OP Terminal Input Current	I_{OP}	19	21	23	µA	$V_{OP} = V_{IN}$ - 0.5V
[Disable LED Open Detection Function at Reduced-Voltage]						
OPM Terminal Source Current	I_{OPM}	38	40	42	µA	
VIN Terminal Disable LED Open Detection Voltage at Reduced-Voltage	V_{IN_OPM}	V_{OPM} × 5.9	V_{OPM} × 6.0	V_{OPM} × 6.1	V	VIN terminal Voltage
OPM Terminal Input Voltage Range	V_{OPM_R}	1.0	-	2.2	V	
[Disable LED Open Detection Time Setting]						
Input Threshold Voltage	V_{DH}	0.9	1.0	1.1	V	
D Terminal Source Current	$I_{DSOURCE}$	100	230	400	µA	
D Terminal ON Resistor	R_D	-	-	950	Ω	I_{D_EXT} = 100µA

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Electrical Characteristics3

(Unless otherwise specified Ta = -40 to +125°C, V_{IN} = 13V, C_{VREG} = 1.0µF, Transistor PNP = 2SAR573D3FRA)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Short Circuit Protection(SCP)]						
Short Circuit Protection Voltage	V_{SCP1}	1.1	1.2	1.3	V	
Short Circuit Protection Release Voltage	V_{SCPR}	1.15	1.25	1.35	V	
Short Circuit Protection Hysteresis Voltage	V_{SCPHYS}	-	50	-	mV	
SCP Terminal Source Current	I_{SCP}	0.2	1.0	2.0	mA	
SCP Terminal Source Current ON Voltage	V_{SCP2}	1.15	1.30	1.45	V	
SCP Delay Time	t_{SCP2}	10	20	45	µs	
[PBUS]						
Input High Voltage	V_{PBUSH}	2.40	-	-	V	
Input Low Voltage	V_{PBUSL}	-	-	0.6	V	
Hysteresis Voltage	$V_{PBUSHYS}$	-	200	-	mV	
PBUS Terminal Source Current	I_{PBUS}	75	150	300	µA	V_{EN} = 5V
PBUS Terminal Output Low Voltage	R_{PBUS}	-	-	0.6	V	I_{PBUS_EXT} = 3mA
PBUS Terminal Output High Voltage	V_{PBUS_OH}	3.5	4.5	5.5	V	I_{PBUS_EXT} = -10µA
PBUS Terminal Leakage Current	I_{PBUS_LEAK}	-	-	10	µA	V_{PBUS} = 7V
[EN]						
Input High Voltage	V_{ENH}	2.4	-	-	V	
Input Low Voltage	V_{ENL}	-	-	0.6	V	
Hysteresis Voltage	V_{ENHYS}	-	60	-	mV	
Terminal Input Current	I_{EN}	-	7	15	µA	V_{EN} = 5V
[UVLO VIN]						
UVLO Detection Voltage	V_{UVLOD}	3.88	4.10	4.32	V	V_{IN}: Sweep down
UVLO Release Voltage	V_{UVLOR}	4.25	4.50	4.75	V	V_{IN}: Sweep up, V_{REG} > 3.75V
UVLO Hysteresis Voltage	V_{HYS}	-	0.4	-	V	

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Typical Performance Curves (Reference Data)

(Unless otherwise specified Ta = 25°C, V_{IN} = 13V, C_{VREG} = 1.0µF, Transistor PNP = 2SAR573D3FRA)

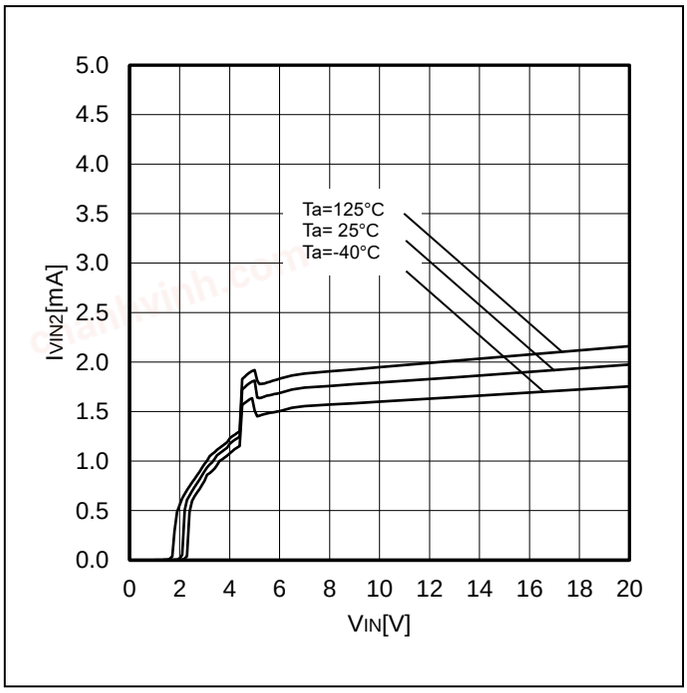


Figure 1. I_{VIN2} vs V_{IN}

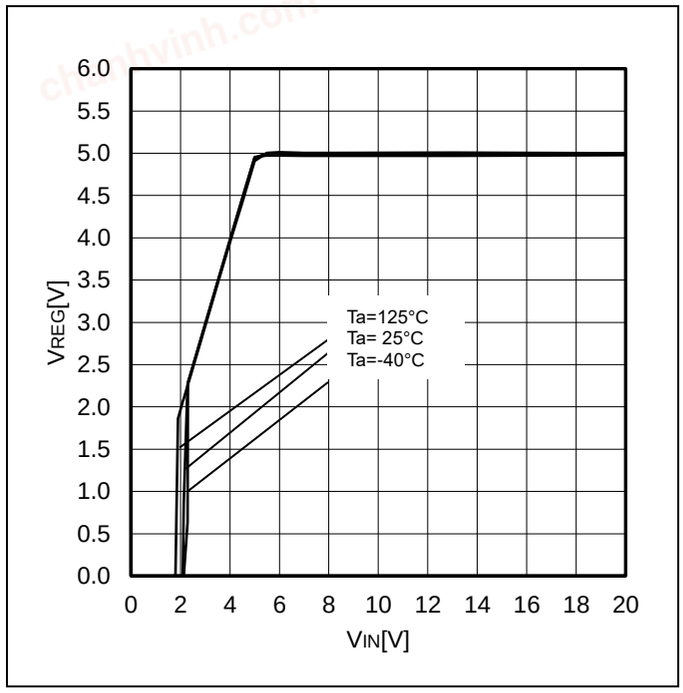


Figure 2. V_{REG} vs V_{IN}

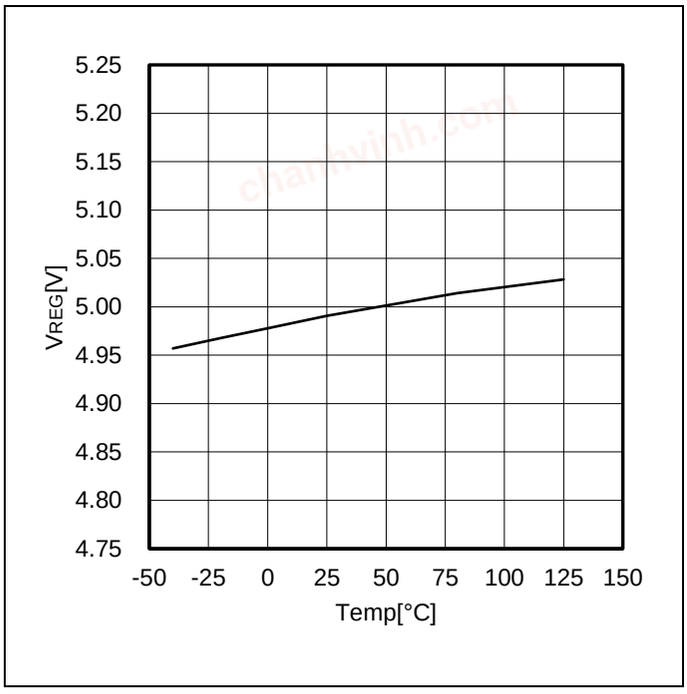


Figure 3. V_{REG} vs Temp

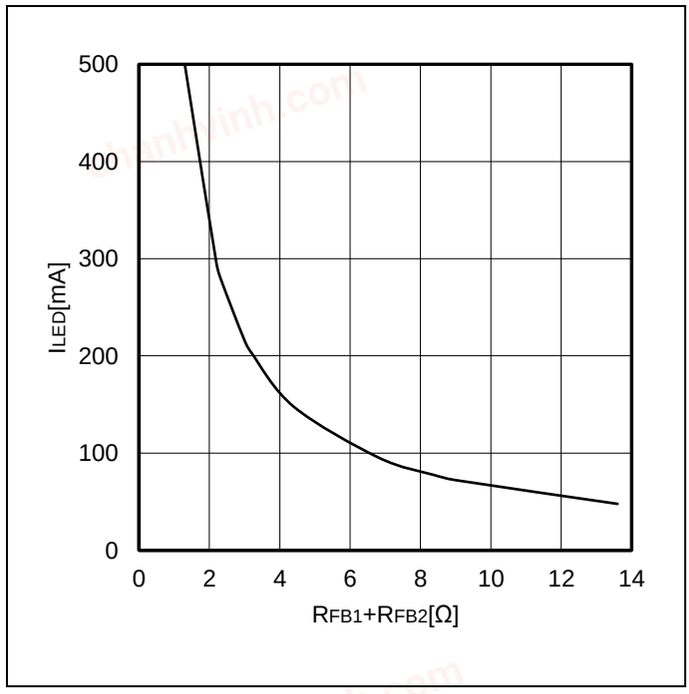


Figure 4. I_{LED} vs R_{FB1}+R_{FB2}

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Typical Performance Curves (Reference Data)

(Unless otherwise specified Ta = 25°C, V_{IN} = 13V, C_{VREG} = 1.0µF, Transistor PNP = 2SAR573D3FRA)

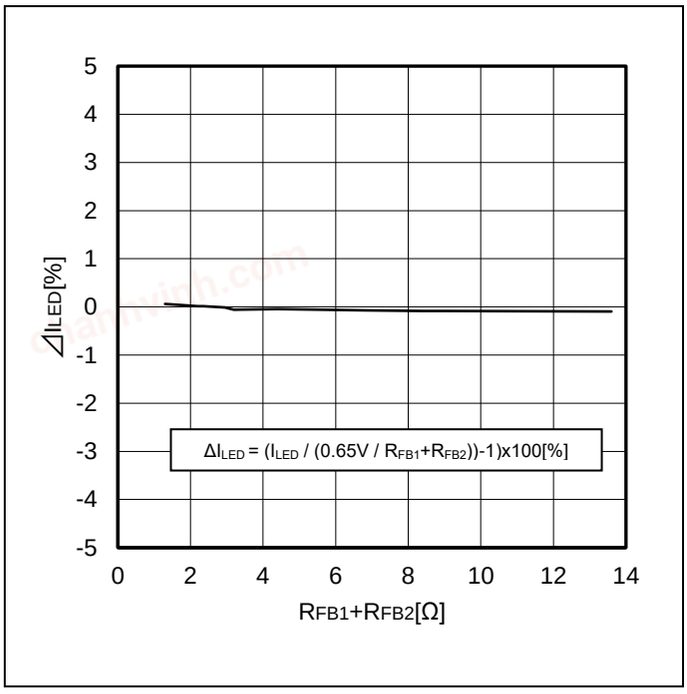


Figure 5. ΔI_{LED} vs $R_{FB1}+R_{FB2}$

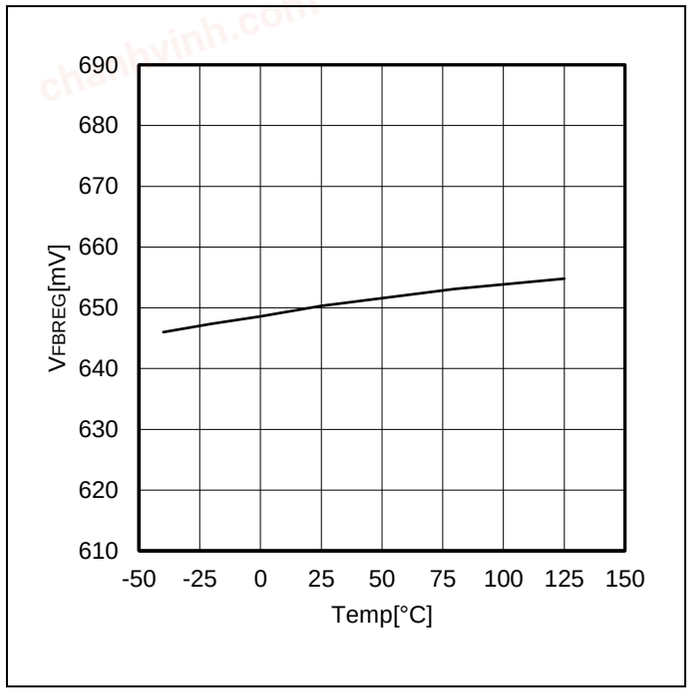


Figure 6. V_{FBREG} vs Temp

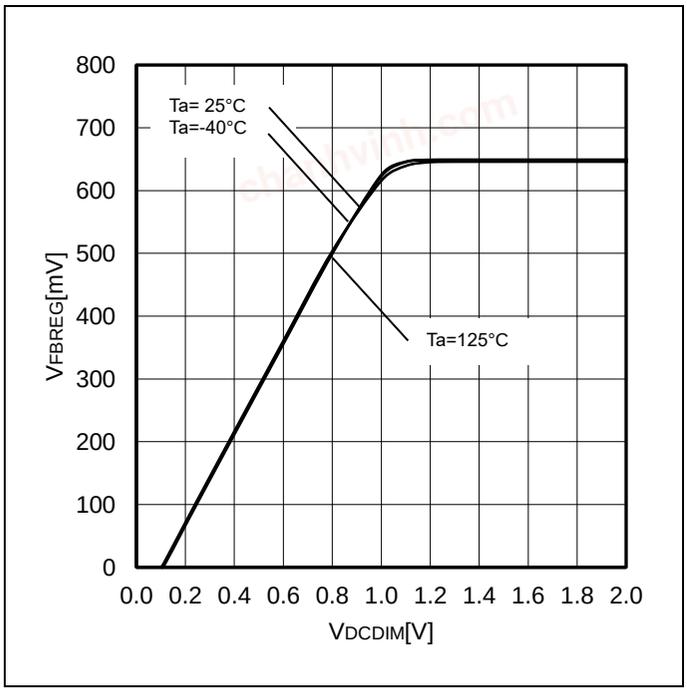


Figure 7. V_{FBREG} vs V_{DCDIM}

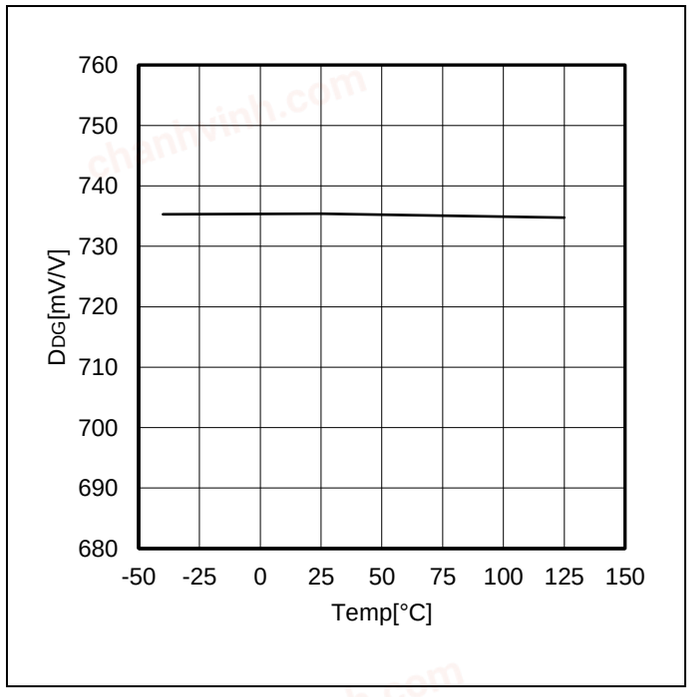


Figure 8. D_{DG} vs Temp

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Typical Performance Curves (Reference Data)
(Unless otherwise specified Ta = 25°C, V_{IN} = 13V, C_{VREG} = 1.0µF, Transistor PNP = 2SAR573D3FRA)

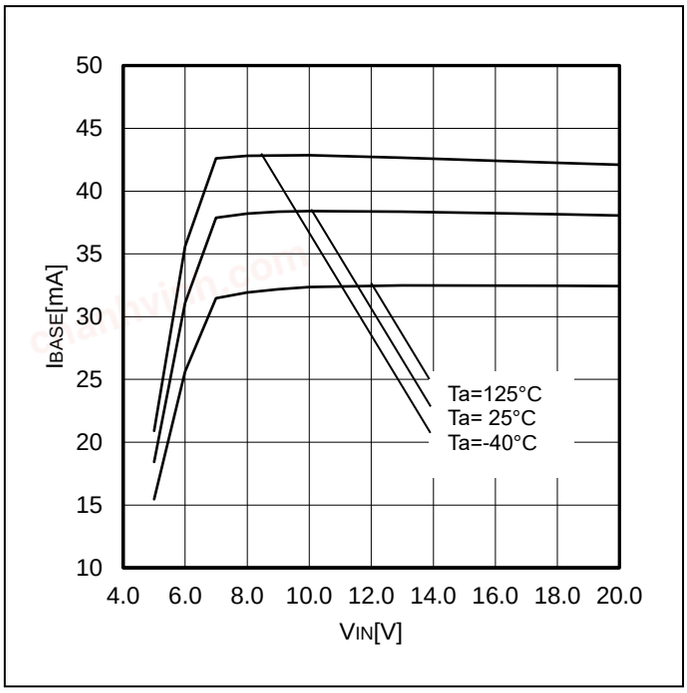


Figure 9. I_{BASE} vs V_{IN}

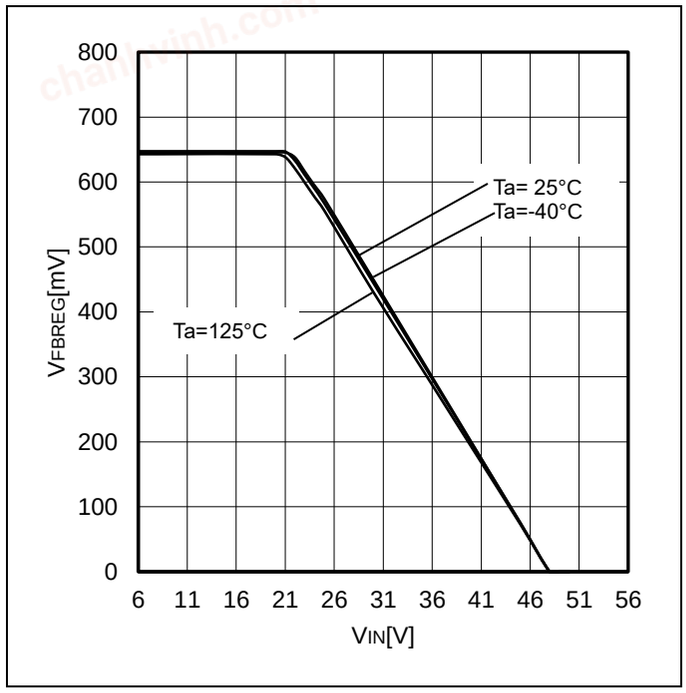


Figure 10. V_{FBREG} vs V_{IN}

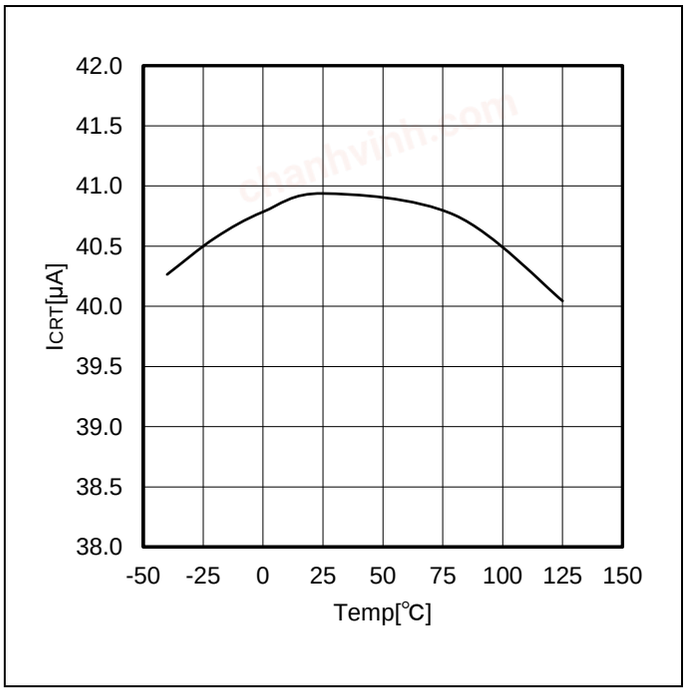


Figure 11. I_{CRT} vs Temp

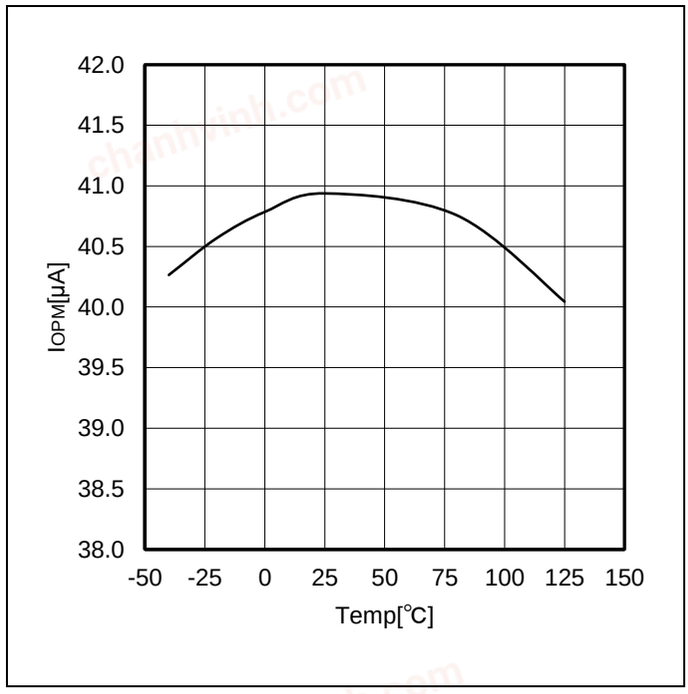


Figure 12. I_{OPM} vs Temp

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Features Description

(Unless otherwise specified, Ta=25°C, V_{IN}=13V, Transistor PNP = 2SAR573D3FRA, and numbers are “Typical” values.)

1. LED Current Setting

LED current I_{LED} can be defined by setting resistances R_{FB1} and R_{FB2}.

$$I_{LED} = \frac{V_{FBREG}}{R_{FB1} + R_{FB2}} \ [A]$$

where:
V_{FBREG} is the FB Terminal Voltage 650mV (Typ)

• How to connect LED current setting resistors

LED current setting resistors must always be connected at least in pair arranged in series as below.
If only one current setting resistor is used, then in case of a possible resistor short, the external PNP Tr. and LED may be broken due to large current flow.
PNP Tr. rating current, LED rating current, R_{FB1} and R_{FB2} must have the following relations:

$$I_{LED_Max} > I_{PNP_Max} > \frac{V_{FBREG}}{Min(R_{FB1}, R_{FB2})} \ [A]$$

where:
I_{LED_Max} is the LED Rating Current
I_{PNP_Max} is the PNP Tr. Rating Current
V_{FBREG} is the FB Terminal Voltage 650mV(Typ)
$Min(R_{FB1},R_{FB2})$ is the Lowest value of R_{FB1} and R_{FB2}

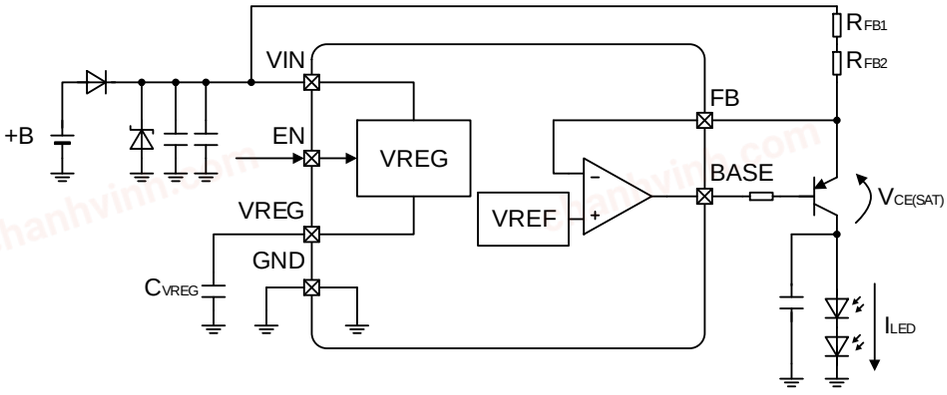


Figure 13. LED Current Setting

• Constant current control dynamic range

Constant current control dynamic range of LED current I_{LED} can be calculated as follows.

$$V_{IN} \geq V_{f_LED} \cdot N + V_{CE_PNP} + V_{FBREG} \ [V]$$

where:
V_{IN} is the VIN Terminal Voltage
V_{f_LED} is the LED Vf
N is the Number of Rows of LED
$V_{CE(sat)}$ is the External PNP Tr. Collector-Emitter Saturation Voltage
V_{FBREG} is the FB Terminal Voltage 650mV(Typ)

2. Reference-Voltage (VREG)
VIN terminal generates 5.0V (Typ). This voltage is used as power source for the internal circuit, and also used to fix the voltage of terminals outside LSI to HIGH side. VREG terminal must be connected with C_{VREG} = 1.0μF to 4.7μF to ensure capacity for the phase compensation. If C_{VREG} is not connected, the circuit behavior would become extraordinarily unstable, for example with the oscillation of the reference-voltage.
VREG terminal voltage must not be used as power source for other devices than this LSI.
VREG circuit has a built-in UVLO function. The IC is activated when the VREG terminal voltage rises to 4.0V (Typ) or higher, and shut down when the VREG terminal voltage drops to 3.75V(Typ) or lower.

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3. Table of Operations

The PWM dimming mode switches to DC control depending on CRT terminal voltage.
When V_{IN} > 22.0V (Typ), LED current is limited to reduce the heat dissipation of external PNP Tr.
Depending on OP/SCP terminal voltage status, output current is turned OFF. Output current is also turned OFF when Low signal is input to PBUS terminal.
In addition, UVLO, TSD further increases system reliability
For each functions, please refer to Features Description.

Operation Mode	CRT Terminal	Detecting Condition		LED Current (I_{LED})	PBUS Terminal
		[Detect]	[Release]		
Stand-by Mode(Note1)	-	$V_{EN} \leq 0.6V$	$V_{EN} \geq 2.4V$	OFF(Note3)	Hi-Z
DC	$V_{CRT} \geq$ 2.0V(Typ)	-	-	50mA to 400mA	High (4.5V(Typ))
PWM Dimming	See Features Description, 4.	-	-	See Features Description, 4.	High (4.5V(Typ))
DC Dimming	-	$V_{DCDIM} \leq$ 1.0V(Typ)	V_{DCDIM} > 1.25V	See Features Description, 9.	High (4.5V(Typ))
Over Voltage Mute	-	V_{IN} > 22.0V(Typ)	$V_{IN} \leq$ 22.0V(Typ)	See Features Description, 11.	High (4.5V(Typ))
LED Open Detection(Note2)	-	$V_{OP} \geq$ V_{IN} –1.2V(Typ)	V_{OP} < V_{IN} – 1.2V(Typ)	OFF(Note3)	Low
Short Circuit Protection (SCP)	-	$V_{SCP} \leq$ 1.2V(Typ)	$V_{SCP} \geq$ 1.25V(Typ)	OFF(Note3)	Low
PBUS Control OFF	-	$V_{PBUS} \leq 0.6V$	$V_{PBUS} \geq 2.4V$	OFF(Note3)	Input $V_{PBUS} \leq 0.6V$
UVLO	-	$V_{IN} \leq$ 4.1V(Typ) or $V_{REG} \leq$ 3.75V(Typ)	$V_{IN} \geq$ 4.5V(Typ) or $V_{REG} \geq$ 4.0V(Typ)	OFF(Note3)	High (4.5V(Typ))
TSD	-	Tj ≥ 175°C(Typ)	Tj ≤ 150°C(Typ)	OFF(Note3)	Hi-Z

(Note1) Circuit Current 0μA(Typ)
(Note2) In regard to the sequence of LED current OFF, see Features Description, 5.
(Note3) BASE Terminal Current: OFF, and LED Current (I_{LED}): OFF.

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4. PWM Dimming Operation using external RC network

PWM Dimming is performed with the following circuit.
The ramp up/down time of the CRT voltage, and therefore the dimming cycle and Duty, can be set by values of the external components **(C_{CRT}, R_{CRT})**.
Please connect CRT to VIN and DISC to GND or open if it is not used.

The CR timer function is activated if DC SW is OPEN. To perform PWM light control of LED current, a triangular waveform is generated at CRT terminal. The **LED current (I_{LED}) is turned OFF** while CRT voltage is ramping up, and **LED current(I_{LED}) is turned ON** while CRT voltage is ramping down.

When $V_{CRT} > V_{CRT_DIS1}$ (2.0V(Typ)), Dimming mode turns to DC Control. When $V_{CRT} > V_{CRT_DIS2}$ (2.4V(Typ)), discharge resistance of DISC terminal changes from R_{DISC1}(50Ω(Typ)) to R_{DISC2}(5kΩ(Typ)).

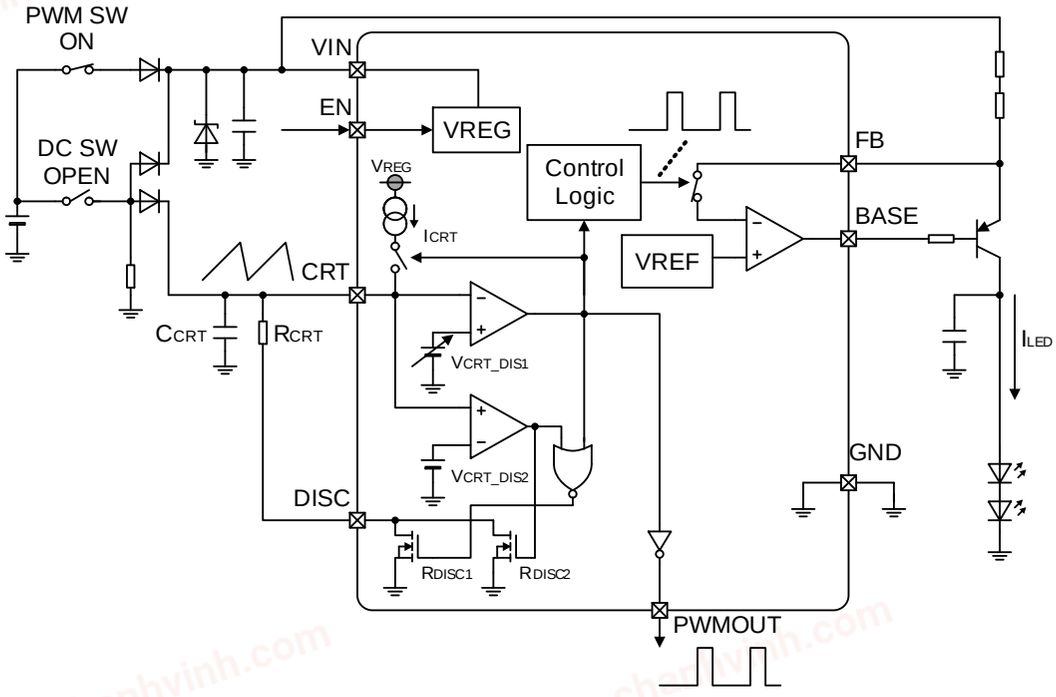


Figure 14. PWM Dimming Operation

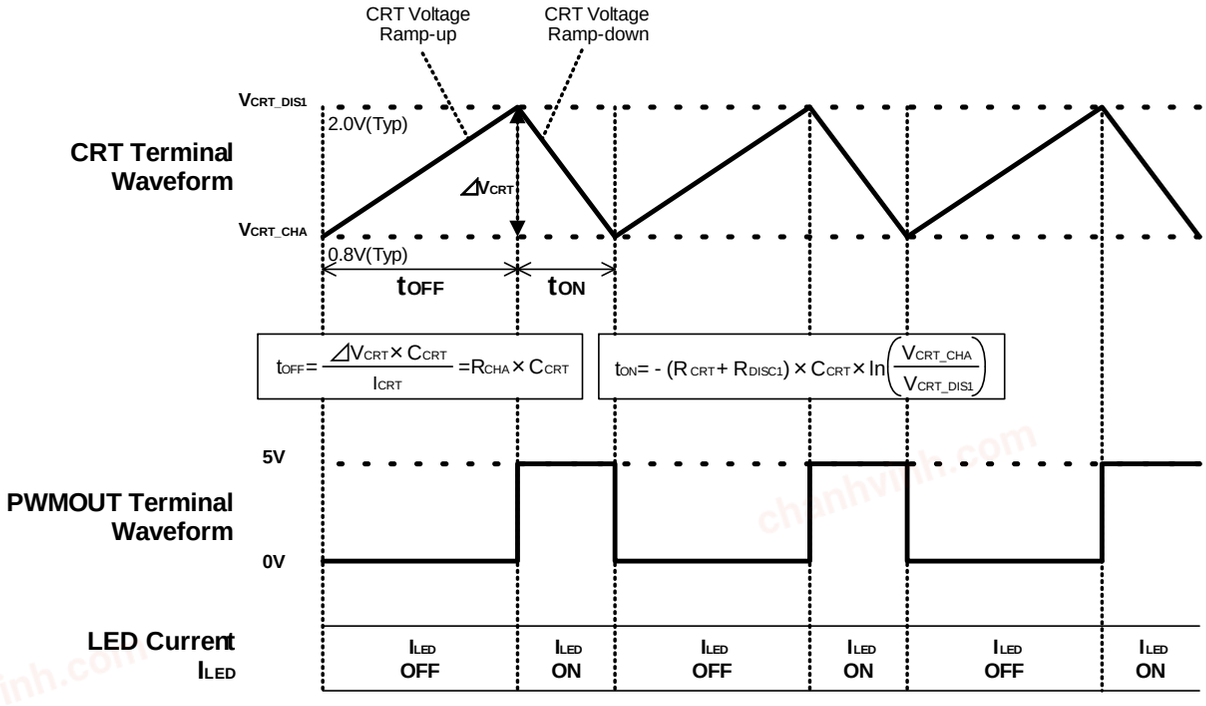


Figure 15. PWM Dimming Operation

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(1) CRT Ramp up Time t_{OFF} and CRT Ramp down Time t_{ON}
CRT Ramp up Time t_{OFF} and CRT Ramp down Time t_{ON} can be defined from the following equations.
Make sure that t_{ON} is set > PWM Minimum Pulse Width t_{MIN}:10μs (Min).

$$t_{OFF} = \frac{\Delta V_{CRT} \times C_{CRT}}{I_{CRT}} = R_{CHA} \times C_{CRT} \ [s]$$

$$t_{ON} = -(R_{CRT} + R_{DISC1}) \times C_{CRT} \times In\left(\frac{V_{CRT_CHA}}{V_{CRT_DIS1}}\right) \ [s]$$

where:

I_{CRT} is the CRT Terminal Charge Current	40μA(Typ)
R_{CHA} is the CRT Terminal Charge Resistor	30kΩ(Typ)
R_{DISC1} is the DISC Terminal ON Resistor1	50Ω(Typ)
V_{CRT_CHA} is the CRT Terminal Charge Voltage	0.8V(Typ)
V_{CRT_DIS1} is the CRT Terminal Discharge Voltage1	2.0V(Typ)

(2) PWM Dimming Frequency f_{PWM}
PWM frequency is defined by t_{ON} and t_{OFF}.

$$f_{PWM} = \frac{1}{t_{ON} + t_{OFF}} \ [Hz]$$

(3) ON Duty(D_{ON})
Like the above, PWM ON duty is defined by t_{ON} and t_{OFF}.

$$D_{ON} = \frac{t_{ON}}{t_{ON} + t_{OFF}} \ [\%]$$

(Example) In case of R_{CRT}=3.6kΩ, C_{CRT}=0.1μF (Typ)

$t_{OFF} = R_{CHA} \times C_{CRT}$ = 30kΩ × 0.1μF = **3.0ms**
$t_{ON} = -(R_{CRT} + R_{DISC1}) \times C_{CRT} \times \ln(V_{CRT_CHA} / V_{CRT_DIS1})$= - (3.6kΩ + 50Ω) × 0.1μF × ln(0.8V / 2.0V) = **0.334ms**

f_{PWM} = 1 / (t_{ON} + t_{OFF}) = 1 / (3.0ms + 0.334ms) = **300Hz**

D_{ON} = t_{ON} / (t_{ON} + t_{OFF}) = 0.334ms / (3.0ms + 0.334ms) =**10.0%**

[PWM Dimming Operation using external signal]
In case external PWM input to CRT terminal,
Make sure that input pulse High voltage >**2.2V** and pulse Low voltage<**0.72V**.
Also please open DISC terminal or connect to GND.

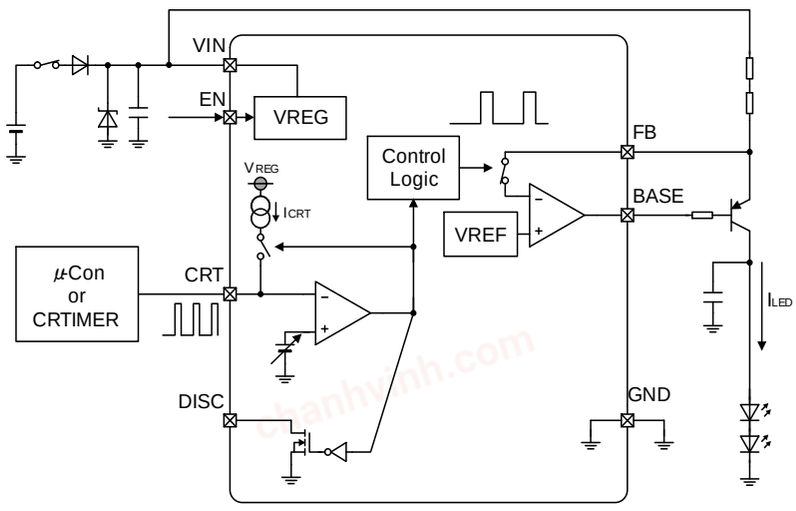


Figure 16. PWM Dimming Operation using external signal

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• About a reverse connection protection diode

Caution on using Reverse protection Diode

With temperature, reverse current I_r of diode (D2, D3) can affect the charge and discharge current to capacitance C1. It is recommended to choose a diode (D2, D3) with Ir value less than 1μA. To avoid High-Z at point A,a resistor R_{DCIN} of 10kΩ is also recommended between Point A and GND.

CRT rise / fall time deviation from set values

① During the PWM dimming operation mode, the A-point on Figure.17 becomes Hi-Z

↓

② Reverse current Ir of D2 and D3 goes to the A-point
(Power supply voltage is being input into the cathode of D2, so reverse current of D2 goes to mainly into C1)
⇒Reverse current Ir of D3 is added to the CRT terminal charge current and discharge current, so CRT start-up / fall time deviates from the settings.

↓

③ C1 gets charged, voltage at A-point rises

↓

④ Voltage at A-point exceeds voltage in CRT terminals of each IC

↓

⑤ Vf occurs in the diodes D3

↓

⑥ D3 circulate forward current If
⇒Forward current If of D3 is added to the CRT terminal charge current and discharge current, so CRT start-up / fall time deviates from the settings.

↓

⑦ Repetition ②-⑥

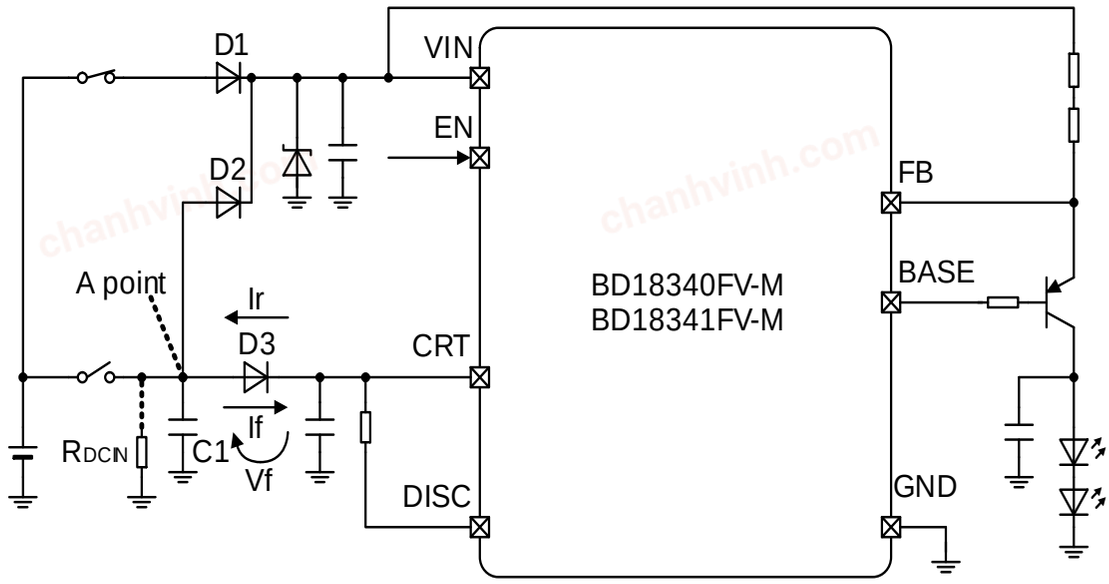


Figure 17. how reverse protection diode affects the CRT terminal rise/fall time

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5. LED Open Detection Function

The IC can detect LED open condition when the OP terminal voltage (V_{OP}) meets the following condition: $V_{OP} > V_{IN}$ - 1.2V (Typ). As soon as $V_{OP} > V_{IN}$ - 1.2 V (Typ) condition is achieved, D terminal source current (230μA (Typ)) turns on and starts charging the disable LED open detection time setting capacitor (C_D).
Once the D terminal voltage (V_D) becomes higher than 1.0 V (Typ) and 1μs (Typ) elapses, the BASE terminal sink current (I_{BASE}) is latched OFF and PBUS terminal voltage (V_{PBUS}) is switched to Low.

[Base Current Limit Resistance (R_{LIM})]
The OP terminal voltage V_{OP} is defined by the following formula:
(Note that the external PNP Tr. goes into the saturation mode when the collector is open)

$$V_{OP} = V_{IN} - \{(R_{FB1} + R_{FB2}) \times I_{BASE_Max} + V_{CE_PNP}\} \ [V]$$

$$I_{BASE_Max} = 6.0V/R_{LIM} \ [A]$$

$$\left(I_{BASE_Max} < 80mA\right)$$

where:
R_{FB1}, R_{FB2} is the LED Current Setting Resistance
I_{BASE_Max} is the Maximum BASE Terminal Sink Current
R_{LIM} is the BASE Terminal Sink Current Limit Resistance
V_{CE_PNP} is the External PNP Tr. Collector-Emitter Voltage (Note: I_{CE}=I_{OP} (23 μA (Max)))

Please determine the BASE current limit resistance R_{LIM} to ensure that the OP terminal voltage when the LED is open should meet the following condition: $V_{OP} > V_{IN}$ - 1.2 V (Typ).
Also note that the BASE current limit resistance must meet the following condition in order to obtain the BASE current to be needed during normal LED operation.

$$4.0/R_{LIM} > I_{LED}/hfe_{_MIN} \ [A]$$

where:
$hfe_{_MIN}$ is the Minimum External PNP Tr. hfe

Disable LED open detection time t_D, or the length of time from the moment the OP terminal voltage meets the condition "$V_{OP} > V_{IN}$ - 1.2 V (Typ)" until the moment the BASE terminal sink current (I_{BASE}) is latched OFF, can be defined by the following formula. **Note that the disable time must be shorter than the ON pulse width of the PWM dimming.**

$$t_{ON} > t_D = \frac{C_D \times V_{DH}}{I_D} \ [s]$$

where:
t_{ON} is the ON pulse width of the PWM dimming(CRT Ramp down Time)
C_D is the disable LED open detection time setting capacitor
V_{DH} is the D Terminal Input Threshold Voltage 1.0V (Typ)
I_D is the D Terminal Source Current 230μA (Typ)

To reset the latched off LED current, EN must be turned-on again (The time when EN Terminal is "L": more than 50μs) or the condition "UVLO (V_{IN} < 4.1 V or V_{REG} < 3.75 V)" must be fulfilled.

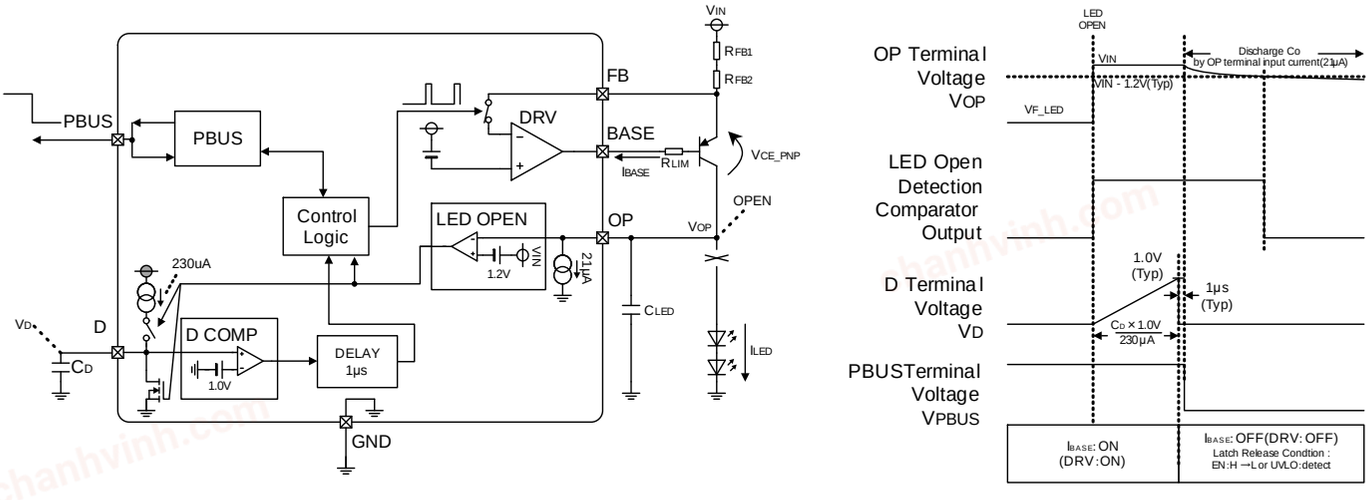


Figure 18. LED Open Detection Timing Chart

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6. Disable LED Open Detection Function at Reduced-Voltage

The disable LED open detection function serves to prevent false detection of LED open at the reduced-voltage during the ramp-up/ramp-down of the VIN terminal voltage. LED open will not be detected until the VIN terminal Disable Open Detection Voltage at Reduced-Voltage (V_{IN_OPM}). Once V_{IN_OPM} is surpassed, the LED current will be latched OFF (BASE terminal sink current (I_{BASE}) is latched OFF) and the PBUS voltage will be switched to Low following the sequence explained in Description of Functions 5.
V_{IN_OPM} must be defined by the following formula. (The OPM terminal voltage must be set between 1.0 V to 2.2 V.)

$$V_{IN_OPM} \geq V_{IN_OPERR} \quad [V]$$

where:
V_{IN_OPM} is the VIN Terminal Disable Open Detection Voltage at Reduced-Voltage
V_{IN_OPERR} is the VIN Terminal Open Erroneous Detection Voltage at Reduced-Voltage

$$V_{IN_OPM} = V_{OPM} \times 6.0(Typ) \quad [V]$$

$$V_{OPM} = I_{OPM} \times R_{OPM} \quad [V]$$

$$V_{IN_OPERR} = V_{f_LED} \times N + V_{OPD} \quad [V]$$

where:
V_{OPM} is the OPM Terminal Voltage
I_{OPM} is the Terminal Source Current 40 µA (Typ)
R_{OPM} is the OPM Terminal Connection Resistance
V_{f_LED} is the LED Vf
N is the Number of Rows of LED
V_{OPD} is the LED Open-Circuit Detection Voltage 1.2 V (Typ)

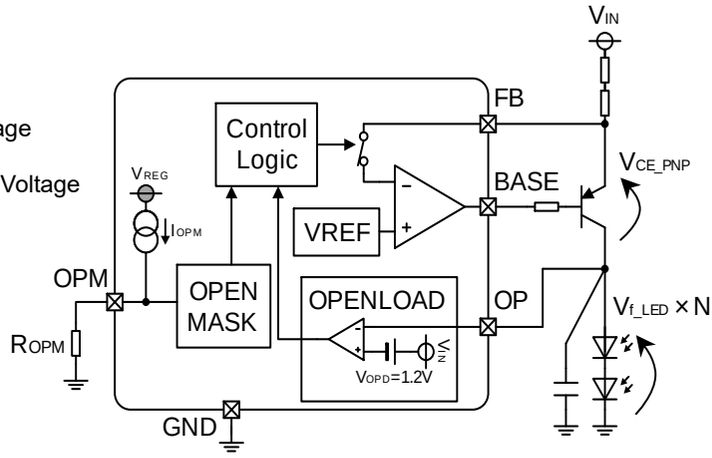


Figure 19. Disable LED Open Detection Function at Reduced-Voltage

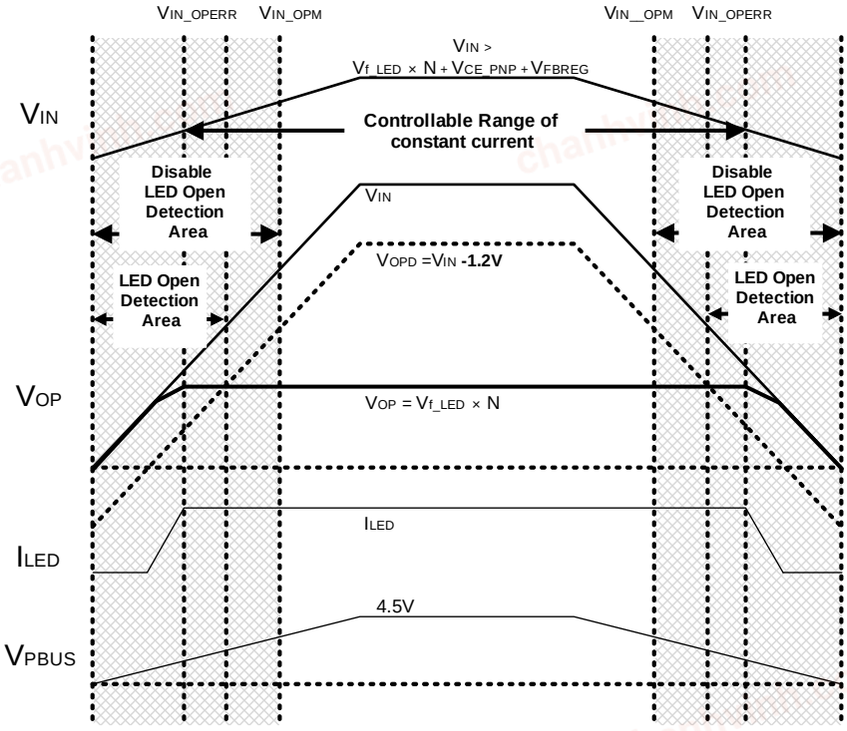


Figure 20. VIN Terminal Disable LED Open Detection Voltage and LED Open Erroneous Detection Voltage at Reduced-Voltage

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7. Short Circuit Protection (SCP)

Short Circuit Protection function lowers the SCP terminal voltage when the collector of the external PNP Tr. is grounded. After a lapse of the short circuit protection delay time (t_{SCP})(20µs(Typ)) following the drop of the SCP terminal voltage (V_{SCP}) under 1.2V(Typ), the external PNP Tr. is turned OFF to prevent its thermal destruction, and the PBUS terminal is switched to Low to communicate the faulty condition.
In order to avoid malfunction, the Short Circuit Protection function will not be activated until CRT > 2.0 V(Typ) after UVLO is reset.
In case where the short circuit (V_{SCP} < 1.2V(Typ)) is present from the beginning when the power is turned on, the short circuit protection function will be activated 60µs(Typ) after V_{CRT} > 2.0V(Typ) condition is reached.

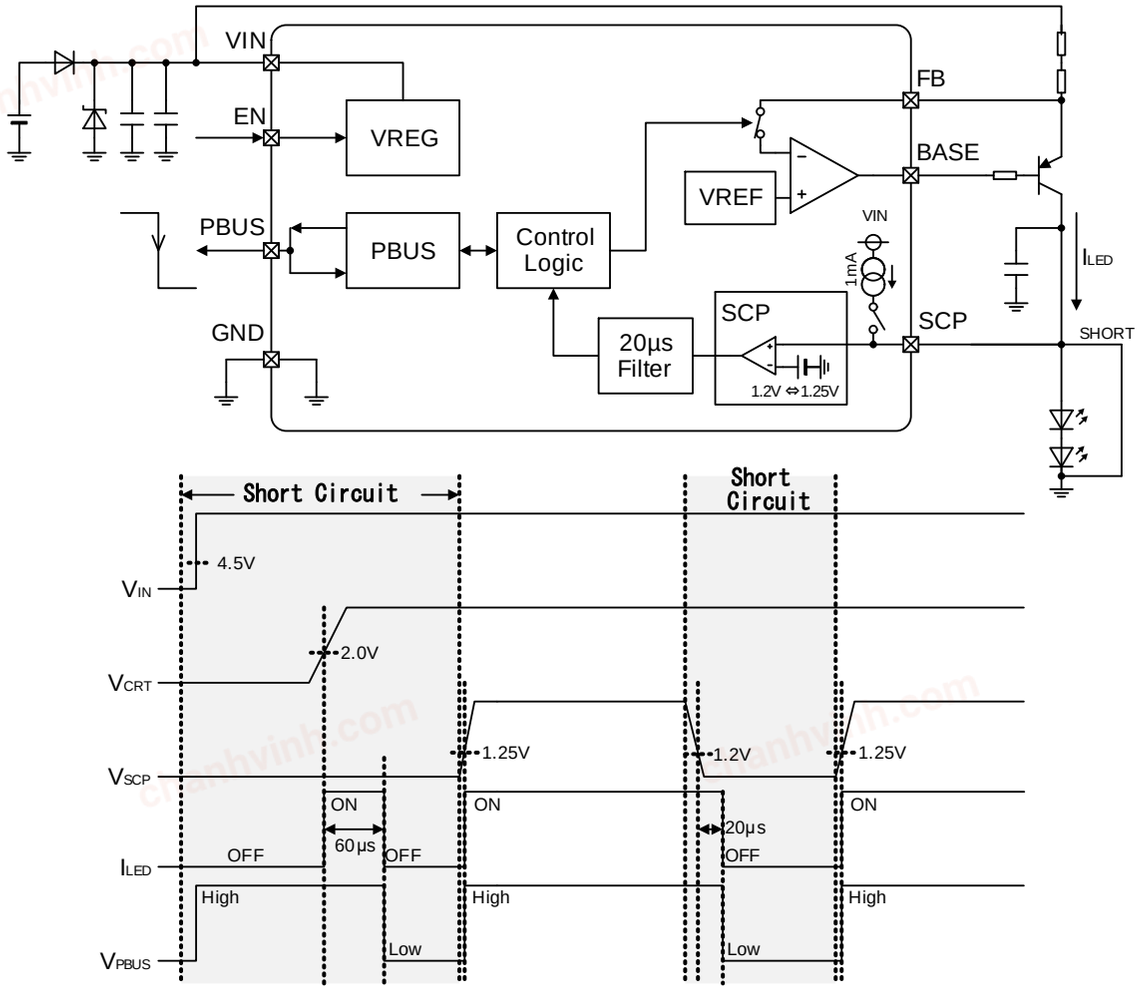


Figure 21. Short Circuit Protection (SCP)

• SCP Terminal Source Current
The SCP terminal sources the SCP terminal source current (1mA (Typ)) once its voltage (V_{SCP}) drops under 1.3V in order to prevent the malfunction of the short circuit protection.

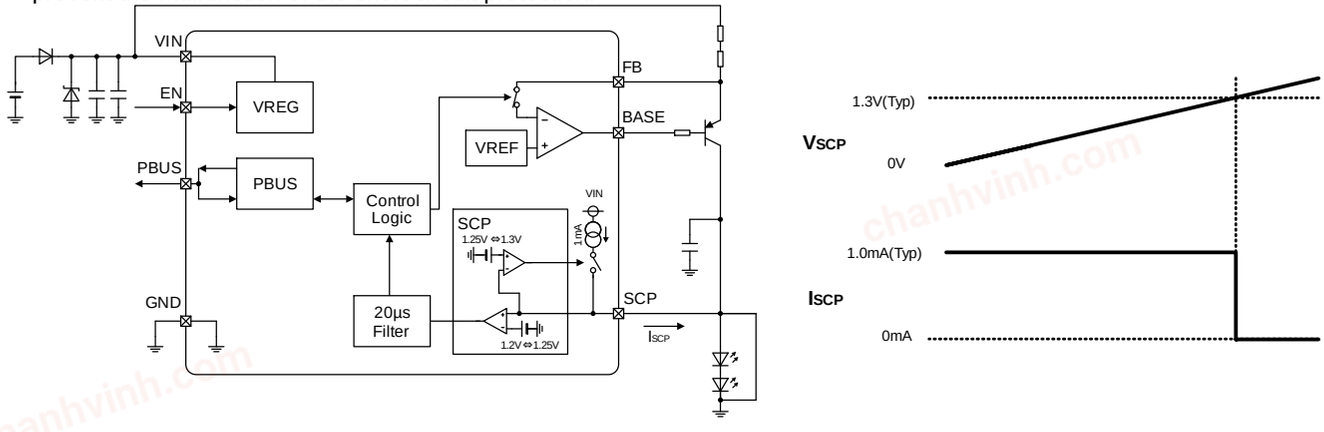


Figure 22. SCP Terminal Source Current

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8. About the capacitor of connecting LED anode

During PWM Mode, the output (LED anode) will be high impedance ('Hi-Z'). During this time noise (Note1) can couple on to this pin and cause false detection of SHORT condition.
To prevent this **it is necessary to connect a Capacitor (0.1μF to 0.68μF) between LED anode and GND terminal nearby terminal**

(Note1) Conducted noise, Radiated noise, Crosstalk of connecter and PCB pattern etc…

Make sure that the capacitor of connecting LED anode is the following equation:

$$0.1 \leq C_{LED} \leq 0.68 \ [\mu F]$$

In case above range is exceeded, the I_{LED} current becomes dull, so please evaluate I_{LED} waveform in PWM mode operation. (Please refer to the following waveform).

About the example of evaluation, please see to the following waveform.

In case a capacitor exceeding the recommended range (above 0.68μF) is connected to LED anode, there is a possibility that delay time of start-up will reach about several decades ms, so special attention is needed.

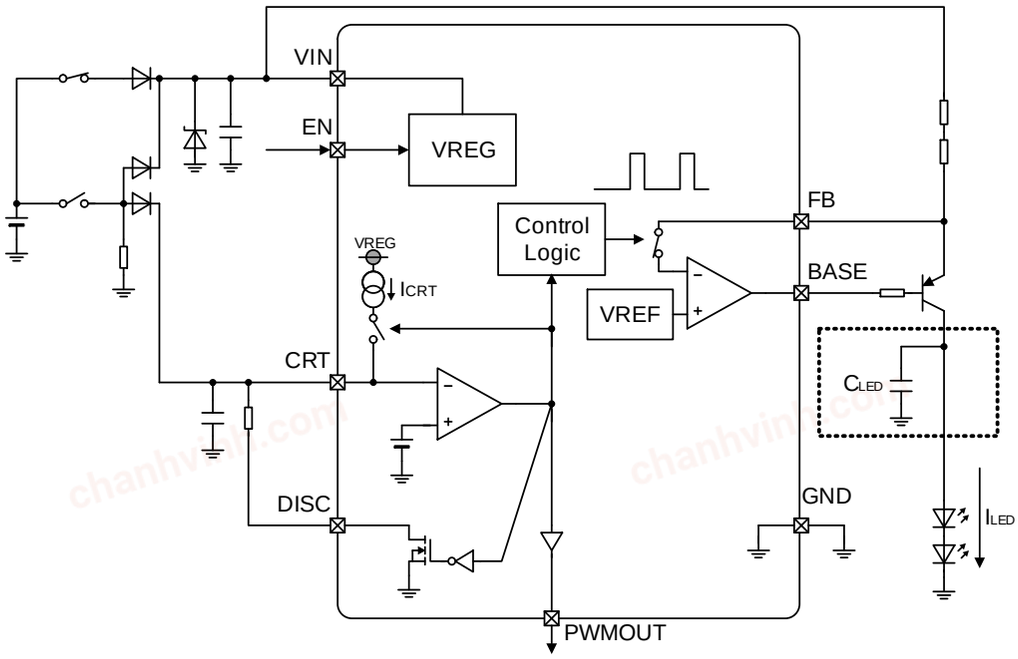


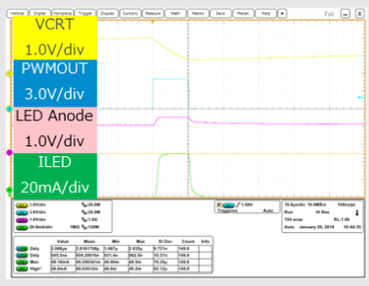
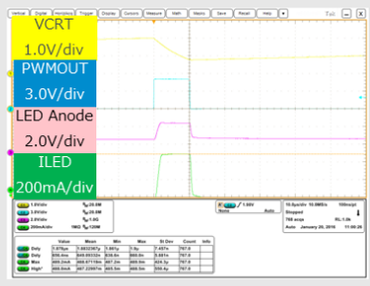
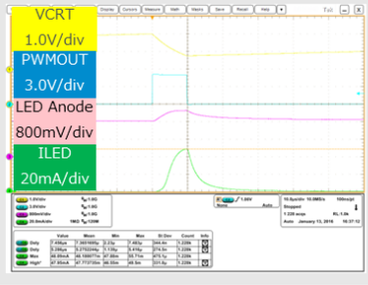
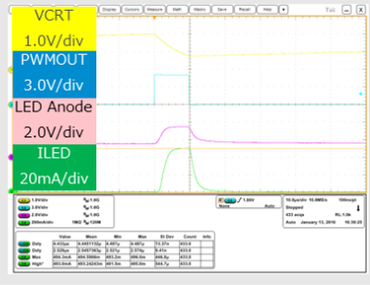
Figure 23. About the capacitor of connecting LED anode

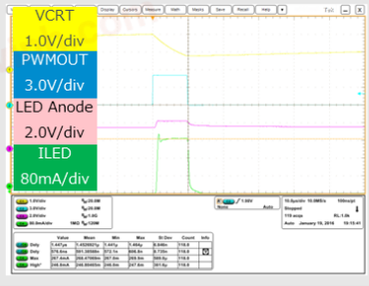
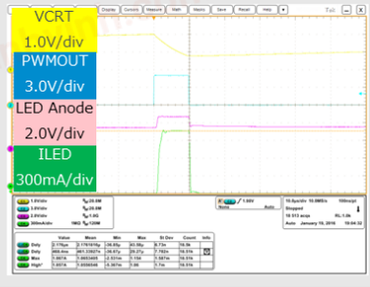
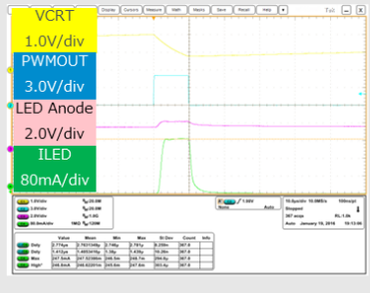
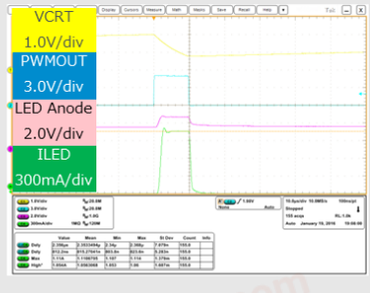
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Evaluation example (ILED pulse width at PWM Dimming operation)

Condition: +B = 13V
Ta = 25°C
LED = 1 Strings
C_{CRT} = 0.01µF
R_{DISC} = 1.0kΩ
PWM Dimming Mode

PNP Tr. : 1parallel	ILED=50mA		ILED=500mA	
CLED=0.1µF		Rise Time 2.0µs Fall Time 0.9µs OverShoot ≒ 0mA		Rise Time 1.9µs Fall Time 0.7µs OverShoot 1mA (0.2%)
CLED=0.47µF		Rise Time 7.4µs Fall Time 5.3µs OverShoot ≒ 0mA		Rise Time 4.4µs Fall Time 2.5µs OverShoot ≒ 0mA

PNP Tr. : 5parallel	ILED=50mA		ILED=200mA	
CLED=0.1µF		Rise Time 1.5µs Fall Time 0.6µs OverShoot 22mA (4.4%)		Rise Time 2.2µs Fall Time 0.5µs OverShoot 10mA (1%)
CLED=0.47µF		Rise Time 2.8µs Fall Time 1.4µs OverShoot ≒ 0mA		Rise Time 2.4µs Fall Time 0.8µs OverShoot 56mA (5.6%)

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9. LED Current De-rating Function (DC Dimming Function)

The LED current (I_{LED}) will be cut down once the DCDIM terminal voltage goes under 1.0 V (Typ).

If LED de-rating function is not used, please DCDIM terminal must be kept 1.25V or more always and as stable as possible. Any ripples at DCDIM terminal will cause oscillations in output current I_{LED} .It is recommended to insert a capacitor at DCDIM terminal.

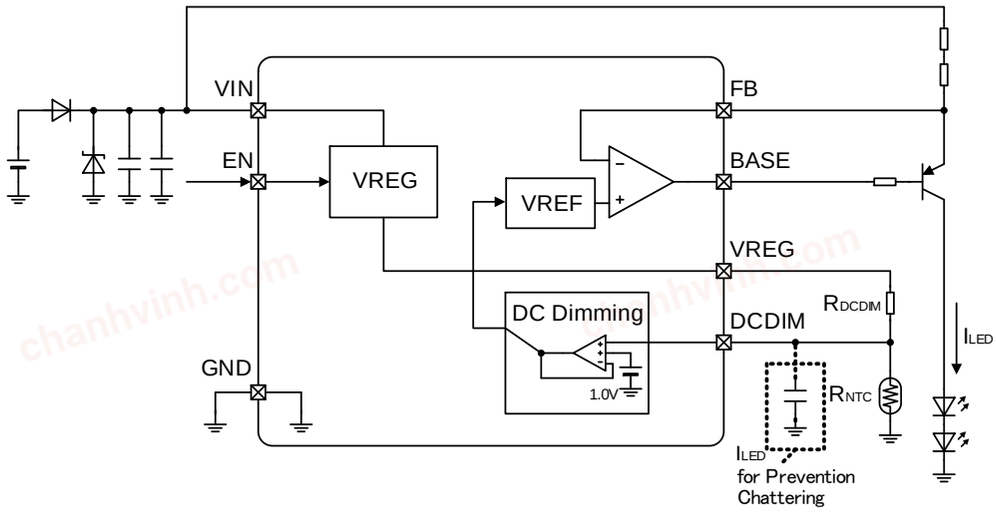
Steep changes in the DCDIM terminal voltage also might affect the ability of the output amplifier to keep up with the changes. So Please evaluate I_{LED} waveform on actual board.

The LED current de-rating function can be defined by the following formula:

$$V_{DCDIM} = V_{REG} \cdot \frac{R_{NTC}}{R_{NTC} + R_{DCDIM}} \quad [V]$$

$$V_{FBREG}(V_{DCDIM} < 1.0V) = V_{FBREG} - (1.0V - V_{DCDIM}) \times D_{DG} \quad [V]$$

where:
R_{DCDIM} is The Resistor for setting DC Dimming
R_{NTC} is the NTC Thermistor Resistance
V_{FBREG} is the FB Terminal Voltage VIN – 650 mV (Typ)
D_{DG} is the DCDIM Dimming Gain 725 mV/V (Typ)



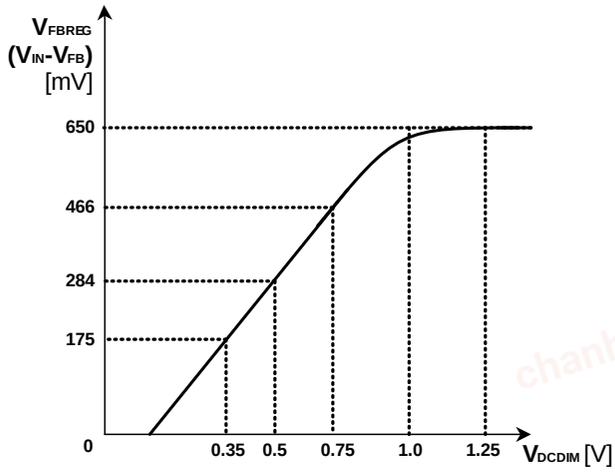


Figure 24. LED Current De-rating Function (DC Dimming Function)

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10. PBUS Function

The PBUS terminal has two functions. When the IC detects OPEN/SHORT of LED's the PBUS is pulled LOW.
It is also possible to turn OFF I_{LED} current by externally pulling the PBUS to LOW voltage. This feature is useful when multiple this IC's are used to drive LED loads. An OPEN/SHORT detection by one IC can be used to turn OFF current of other driver IC's. (Please refer connection diagram below)

Caution of using PBUS terminal

Do not connect to the PBUS terminal other than below items list due to the difference of ratings, internal threshold voltages, and so on. (BD18340FV-M, BD18341FV-M, BD18342FV-M, BD18343FV-M, BD18345EFV-M, BD18337EFV-M, BD18347EFV-M)

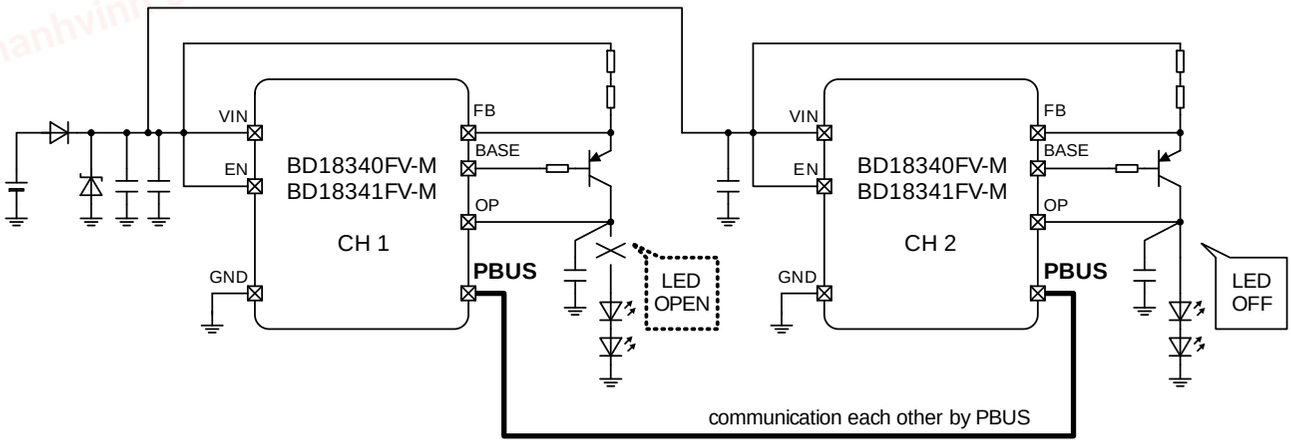


Figure 25. PBUS Function

▼Example of Protective Operation due to LED Open Circuit

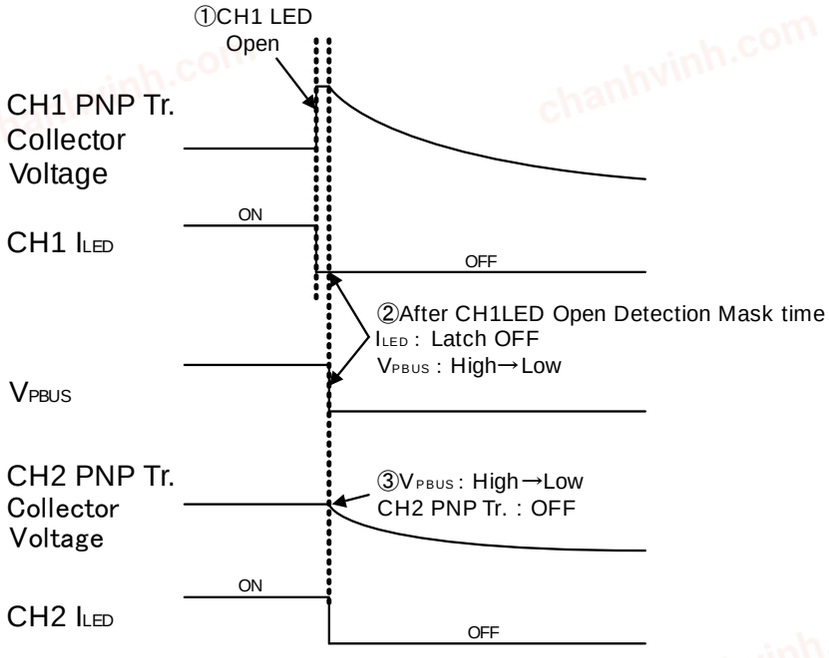


Figure 26. Example of Protective Operation

If LED OPEN occurs, PBUS of CH1 is switched from Hi-Z to Low output. As PBUS becomes Low, LED drivers of other CH detect the condition and turns OFF their own LEDs. LED anode clamps to 1.3V (Typ) during the OFF period, in order to prohibit ground fault detection.

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11. Over Voltage Mute Function (OVM)

Once the VIN terminal voltage (V_{IN}) goes above 22.0 V (Typ), the over voltage mute function is activated to decrease the LED current (I_{LED}) in order to suppress heat generation from the external PNP Tr.
The FB terminal voltage V_{FBREG} which controls the LED current (I_{LED}) will decay at -25 mV/V (Typ).

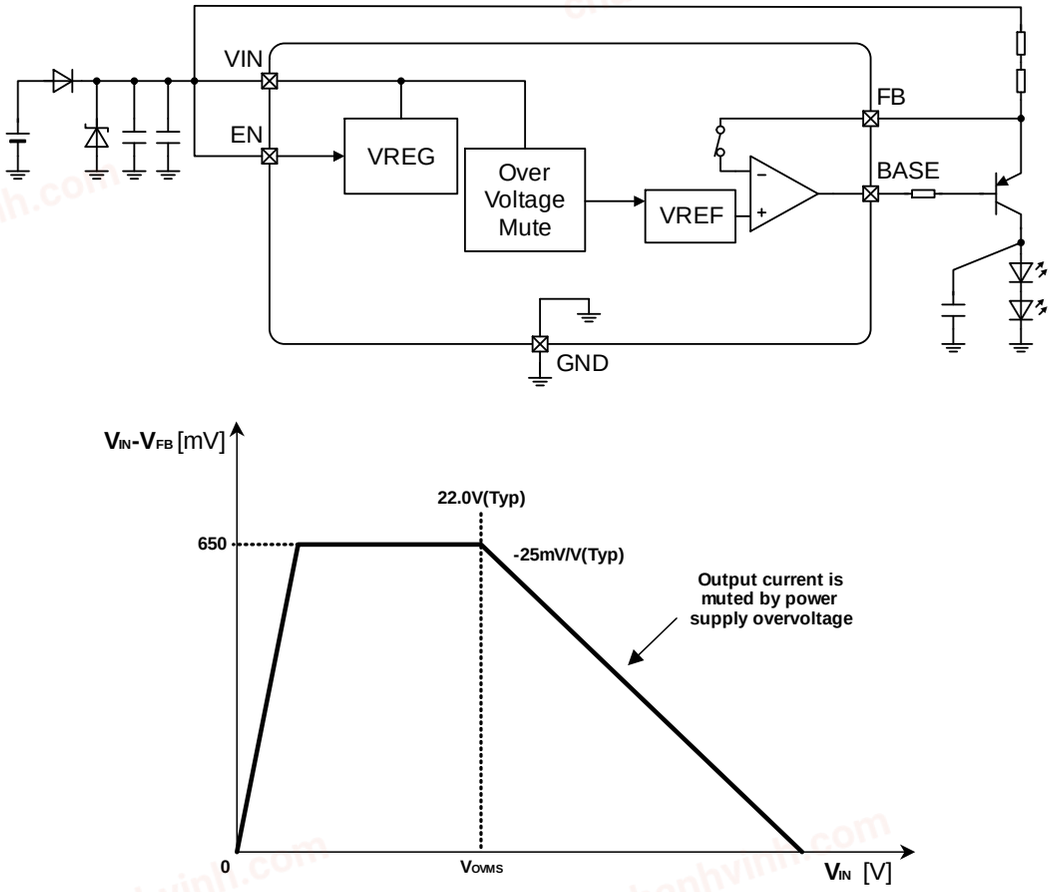


Figure 27. Overvoltage Mute Function (OVM)

12. Under voltage Lockout (UVLO)

UVLO is a protection circuit to prevent malfunction of the IC when the power is turned on or then the power is suddenly shut off.
This IC has two UVLO circuits; UVLO VIN for V_{IN} and UVLO VREG for V_{REG}.
As soon as UVLO status is detected, BASE terminal sink current will be turned off to switch OFF the LED current (I_{LED}).
The following shows the threshold conditions of both UVLO circuits.

Operating Mode	Detection Conditions		LED Current (I_{LED})	PBUS Terminal
	[Detect]	[Release]		
UVLO VIN	$V_{IN} \leq$ 4.1 V(Typ)	$V_{IN} \geq$ 4.5 V(Typ)	OFF(Note1)	High output (4.5 V (Typ))
UVLO VREG	$V_{REG} \leq$ 3.75V(Typ)	$V_{REG} \geq$ 4.0 V(Typ)	OFF(Note1)	High output (4.5 V (Typ))

(Note 1) BASE terminal sink current is turned OFF to switch OFF the LED current I_{LED}.

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Timing Chart

(Unless otherwise specified Ta=25°C, VIN=13V, Transistor PNP=2SAR573D3FRA, LED2strings, Value is Typical.)

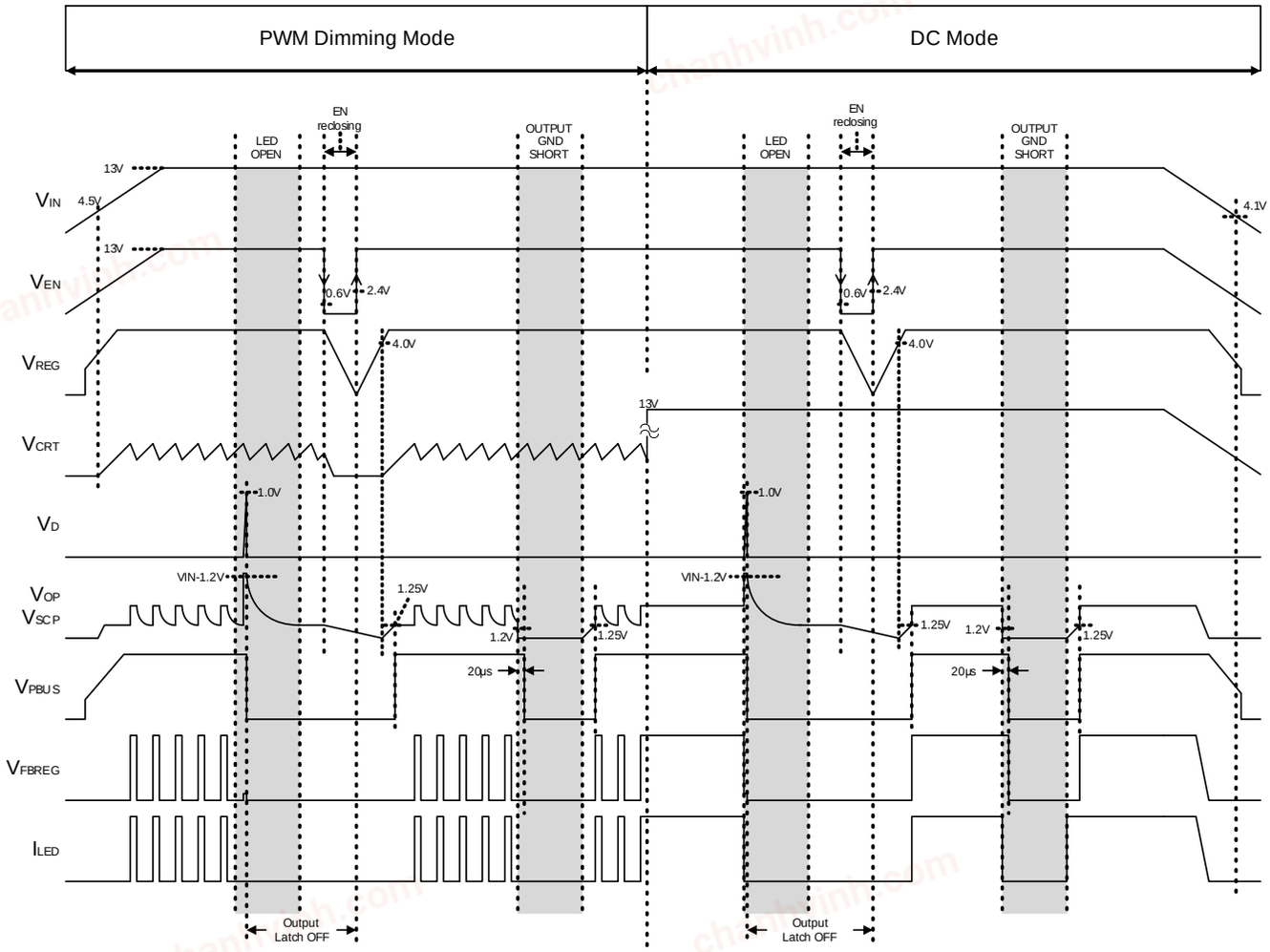


Figure 28. Timing Chart

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Recommended Application Circuit

(1) ILED=120mA

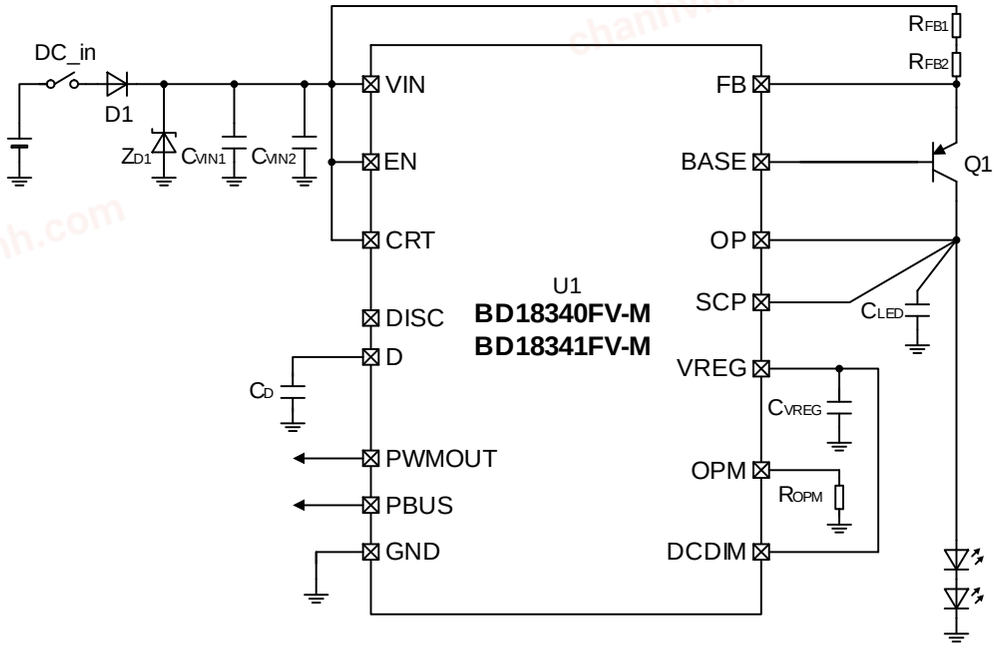


Figure 29. Recommended Application Circuit1 (I_{LED} 120mA, LED white 2strings)

Recommended Parts List1 (I_{LED} 120mA, LED white 2strings)

Parts	No	Parts Name	Value	UNIT	Product Maker
IC	U1	BD18340FV-M/BD18341FV-M	-	-	ROHM
Diode	D1	RFN2LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
PNP Tr.	Q1	2SAR573D3FRA	-	-	ROHM
Resistor	R_{FB1}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{FB2}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{OPM}	MCR03EZPFX3902	39	kΩ	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	μF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	μF	murata
	C_{VREG}	GCM188R71E105KA49	1.0	μF	murata
	C_D	GCM155R11H103KA40	0.01	μF	murata
	C_{LED}	GCM155R71H104KE37	0.1	μF	murata

(About Z_{D1}, please place according to Test Standard of Battery line.)

Please note the following

1. External PNP transistor

For external PNP transistor, please use the recommended device 2SAR573D3FRA for this IC.
While using non-recommended device, validate the design on actual board.
Please check hfe of the part to design base current limit resistor. (See Features Description, section 5). As for parasitic capacitance (C_{LED} connected at LED anode), The more it is small overshoot will be smaller. Please use devices that parasitic capacitance smaller than recommended device, also parasitic capacitance is possible to variation by PCB layout.
So please evaluate over shoot of I_{LED} on actual board. (See Features Description, Section 8 -Evaluation example, ILED pulse width at PWM Dimming operation).

2. Power supply steep variation

This IC is validated with test conditions as per ISO7637-2 standards.
There is possibility of unexpected LED regulation due to sudden transients outside the specification range standards in input power supply.Please check the maximum ratings of LED and evaluate on actual board for any unexpected LED regulation.

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(2) ILED=120mA, PWM ON Duty=10%

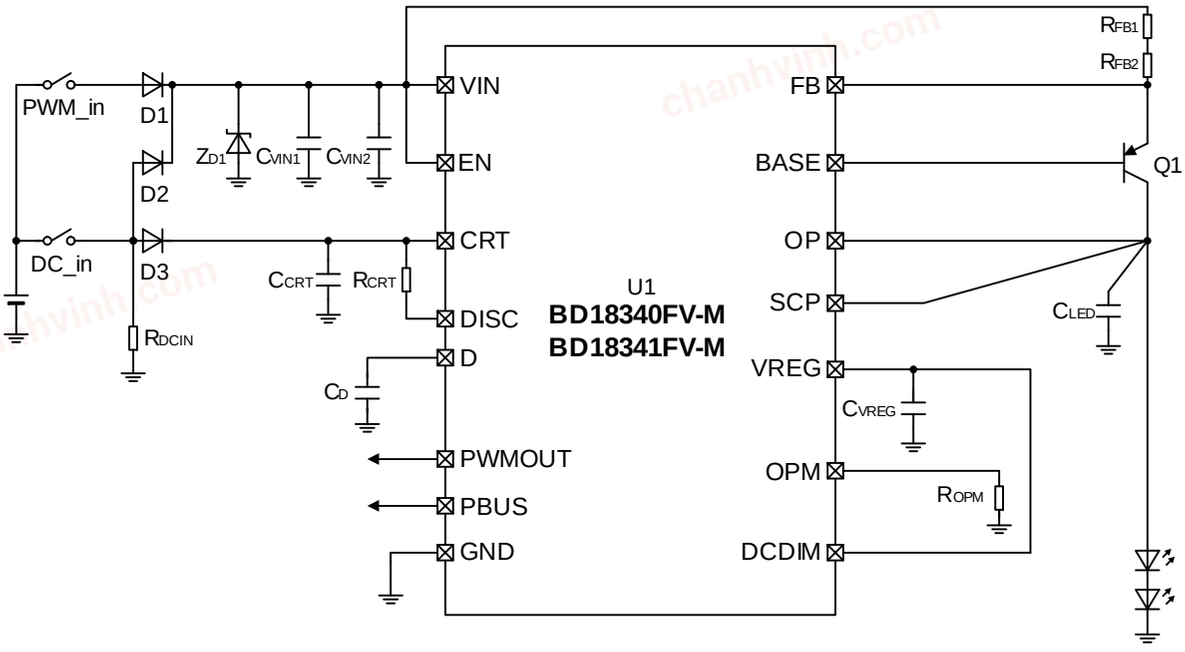


Figure 30. Recommended Application Circuit 2
(I_{LED} 120mA , LED white 2strings, PWM ON Duty: 10%(Pulse width: 0.334ms), PWM frequency: 300Hz)

Recommended Parts List 2
(I_{LED} 120mA, LED white 2strings, PWM ON Duty: 10%(Pulse width: 0.334ms),PWM frequency: 300Hz)

Parts	No	Parts Name	Value	UNIT	Product Maker
IC	U1	BD18340FV-M/BD18341FV-M	-	-	ROHM
Diode	D1,D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
PNP Tr.	Q1	2SAR573D3FRA	-	-	ROHM
Resistor	R_{FB1}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{FB2}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{CRT}	MCR03EZPFX3601	3.6	kΩ	ROHM
	R_{OPM}	MCR03EZPFX3902	39	kΩ	ROHM
	R_{DCIN}	ESR10EZPF2001	2	kΩ	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	μF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	μF	murata
	C_{VREG}	GCM188R71E105KA49	1.0	μF	murata
	C_{CRT}	GCM155R71H104KE37	0.1	μF	murata
	C_D	GCM155R11H103KA40	0.01	μF	murata
	C_{LED}	GCM155R71H104KE37	0.1	μF	murata

(About Z_{D1}, please place according to Test Standard of Battery line.)

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(3) ILED=542mA, PWM ON Duty=10%, LED Current De-rating function

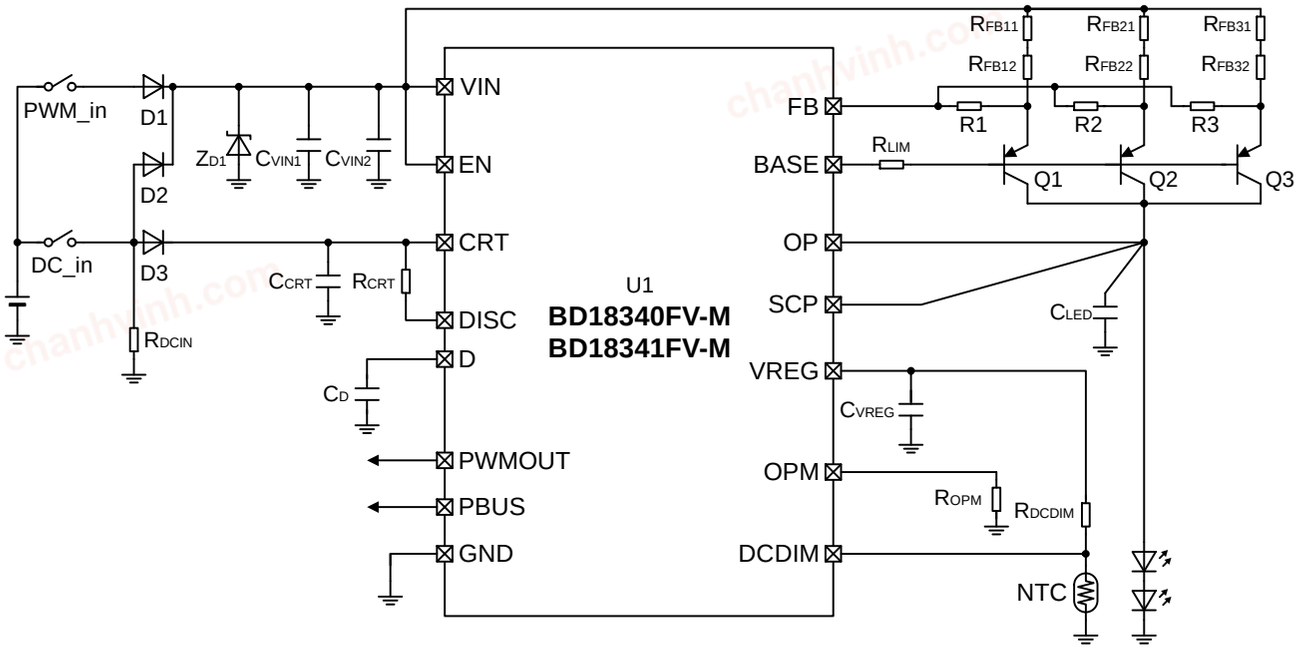


Figure 31. Recommended Application Circuit 3
(I_{LED} 542mA, LED white 2strings, PWM ON Duty: 10%(pulse width: 0.334ms), PWM frequency: 300Hz)

Recommended Parts List 3
(I_{LED} 542mA, LED white 2strings, PWM ON Duty: 10%(pulse width: 0.334ms), PWM frequency: 300Hz)

Parts	No	Parts Name	Value	Unit	Product Maker
IC	U1	BD18340FV-M/BD18341FV-M	-	-	ROHM
Diode	D1,D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
PNP Tr.	Q1 to Q3	2SAR573D3FRA	-	-	ROHM
Resistor	R_{LIM}	MCR03EZPFX1000	100	Ω	ROHM
	R_{FB11}, R_{FB21}, R_{FB31}	LTR10EVHFL1R80	1.8	Ω	ROHM
	R_{FB12}, R_{FB22}, R_{FB32}	LTR10EVHFL1R80	1.8	Ω	ROHM
	R_{CRT}	MCR03EZPFX3601	3.6	kΩ	ROHM
	R_{OPM}	MCR03EZPFX3902	39	kΩ	ROHM
	R_{DCDIM}	MCR03EZPFX4302	43	kΩ	ROHM
	NTC	NTCG104LH154JTDS	150	kΩ	TDK
	R_{DCIN}	ESR10EZPF2001	2	kΩ	ROHM
	R1 to R3	MCR03EZPFX51R0	51	Ω	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	μF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	μF	murata
	C_{VREG}	GCM188R71E105KA49	1.0	μF	murata
	C_{CRT}	GCM155R71H104KE37	0.1	μF	murata
	C_D	GCM155R11H103KA40	0.01	μF	murata
	C_{LED}	GCM155R71H104KE37	0.1	μF	murata

(About Z_{D1}, please place according to Test Standard of Battery line.)

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(4) ILED=120mA, Three rows drive, PWM ON Duty=10%, LED Current De-rating function

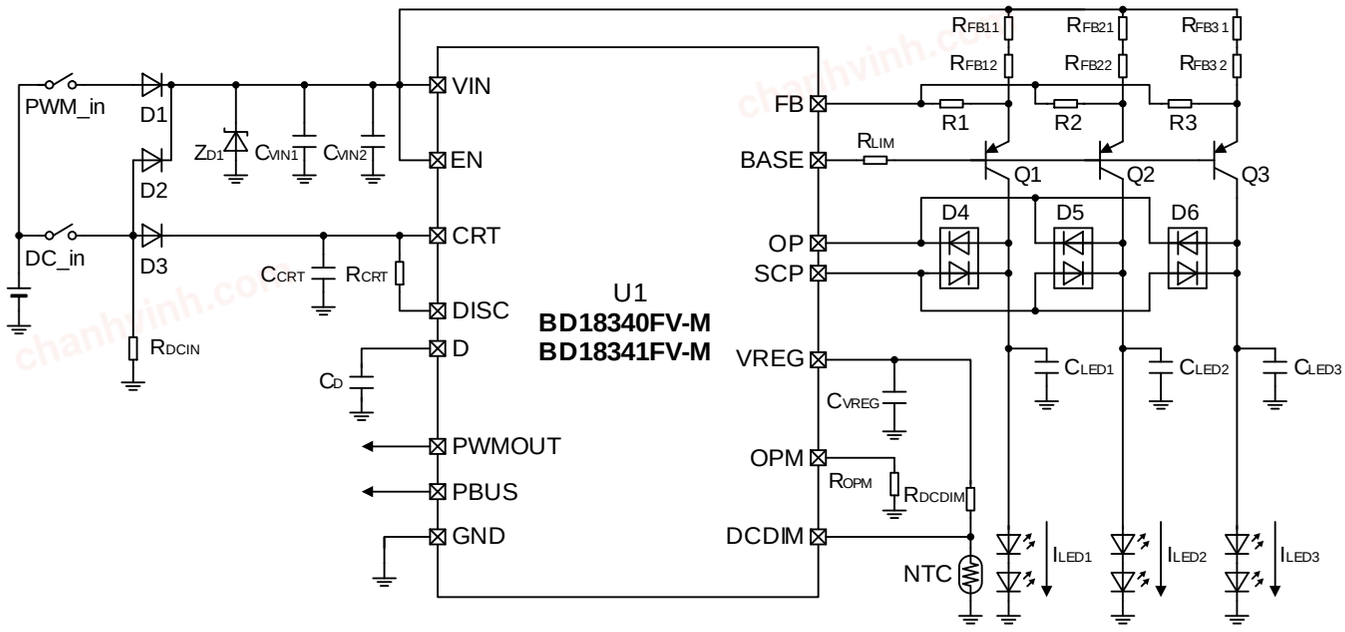


Figure 32. Recommended Application Circuit 4
($I_{LED1\sim3}$ 120mA, LED white 2strings×3, PWM ON Duty: 10%(pulse width: 0.334ms), PWM frequency: 300Hz)

Recommended Parts List 4
(I_{LED} 120mA, LED white 2strings, PWM ON Duty: 10%(pulse width: 0.334ms), PWM frequency: 300Hz)

Parts	No	Parts Name	Value	UNIT	Product Maker
IC	U1	BD18340FV-M/BD18341FV-M	-	-	ROHM
Diode	D1,D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	D4 to D6	DA228UFH			ROHM
PNP Tr.	Q1 to Q3	2SAR573D3FRA	-	-	ROHM
Resistor	R_{LIM}	MCR03EZPFX1000	100	Ω	ROHM
	R_{FB11}, R_{FB21}, R_{FB31}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{FB12}, R_{FB22}, R_{FB32}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{CRT}	MCR03EZPFX3601	3.6	kΩ	ROHM
	R_{OPM}	MCR03EZPFX3902	39	kΩ	ROHM
	R_{DCIN}	ESR10EZPF2001	2	kΩ	ROHM
	R1 to R3	MCR03EZPFX51R0	51	Ω	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	μF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	μF	murata
	C_{VREG}	GCM188R71E105KA49	1.0	μF	murata
	C_{CRT}	GCM155R71H104KE37	0.1	μF	murata
	C_D	GCM155R11H103KA40	0.01	μF	murata
	C_{LED1} to C_{LED3}	GCM155R71H104KE37	0.1	μF	murata

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Thermal Loss

Thermal design should meet the following equation:

$$P_d > P_C$$

$$P_d = (1/\theta_{JA}) \cdot (T_{jmax} - T_a) or (1/\Psi_{JT}) \cdot (T_{jmax} - T_T)$$

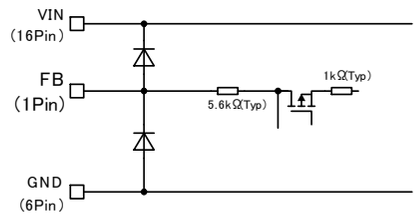
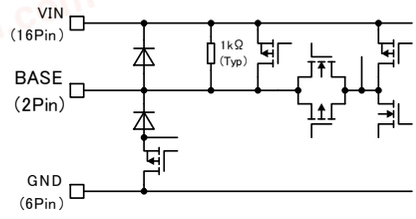
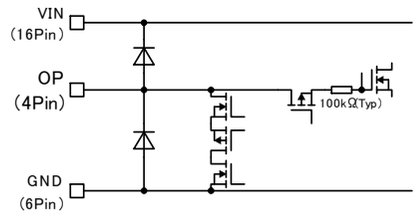
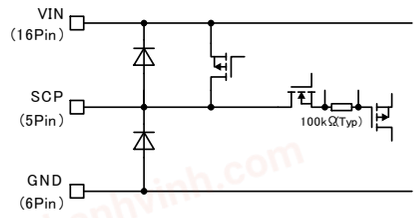
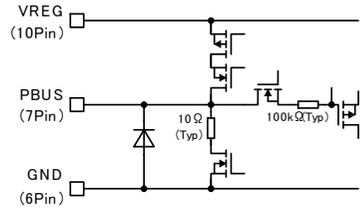
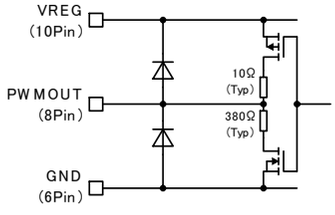
$$P_C = V_{IN} \cdot I_{VIN2} + V_{BASE} \cdot I_{BASE}$$

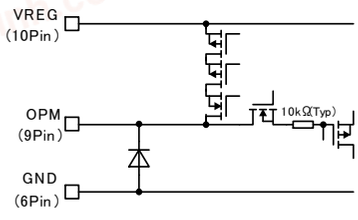
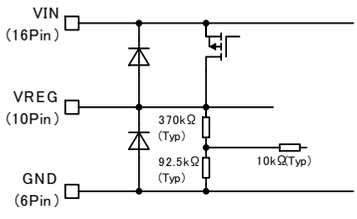
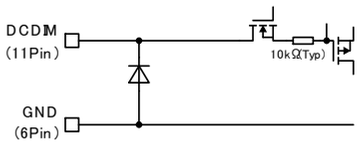
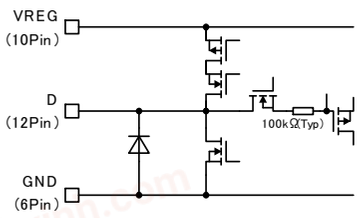
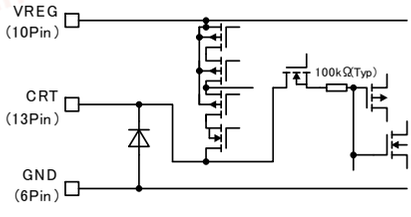
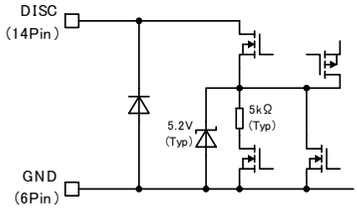
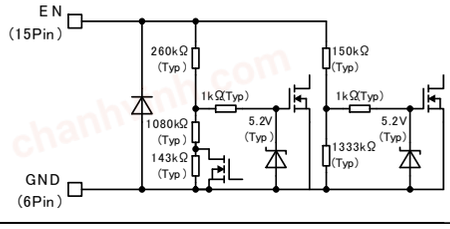
where:
P_d is the Power Dissipation
P_c is the Power Consumption
V_{IN} is the VIN Terminal Voltage
I_{VIN2} is the Circuit Current at Normal Mode
V_{BASE} is the BASE Terminal Voltage
I_{BASE} is the BASE Terminal Sink Current
Θ_{JA} is the Thermal Resistance of Junction to Ambient
Ψ_{JT} is the thermal Characterization Parameter of Junction to centerCase Surface
T_{jmax} is the Max Joint Temperature (150 °C)
T_a is the Ambient Temperature
T_T is the Case Surface Temperature

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I/O equivalence circuits

No.	Terminal Name	I/O Equivalent Circuit
1	FB	
2	BASE	
3	N.C	
4	OP	
5	SCP	
6	GND	-
7	PBUS	
8	PWM OUT	

No.	Terminal Name	I/O Equivalent Circuit
9	OPM	
10	VREG	
11	DCDIM	
12	D	
13	CRT	
14	DISC	
15	EN	
16	VIN	-

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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
OR

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

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Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

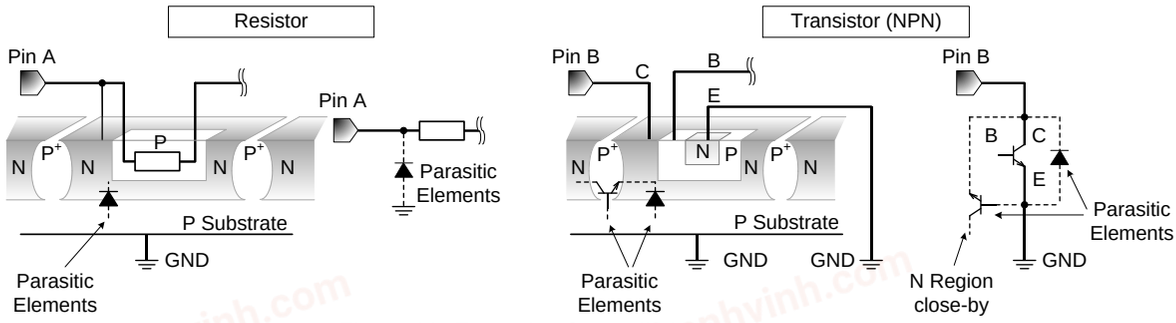


Figure 33. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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Ordering Information

B D 1 8 3 4 0 F V - ME2

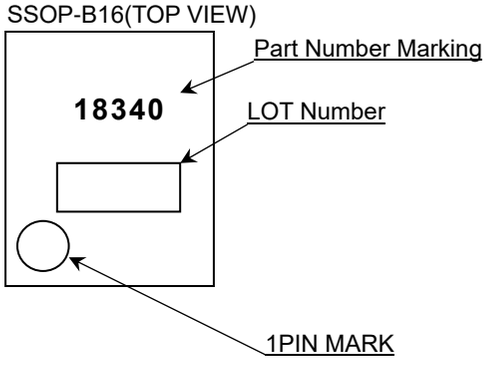
- Product Name
- Package FV: SSOP-B16
- Packaging and forming specification M: High Reliability Design E2: Embossed tape and reel

B D 1 8 3 4 1 F V - ME2

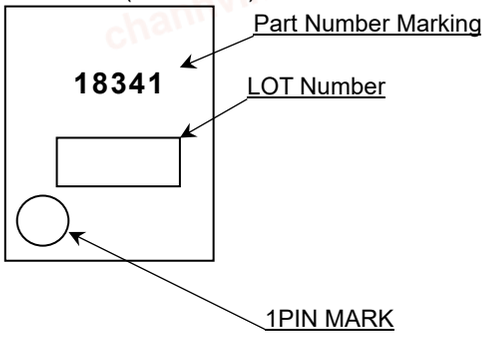
- Product Name
- Package FV: SSOP-B16
- Packaging and forming specification M: High Reliability Design E2: Embossed tape and reel

Marking Diagrams

SSOP-B16(TOP VIEW)



SSOP-B16(TOP VIEW)

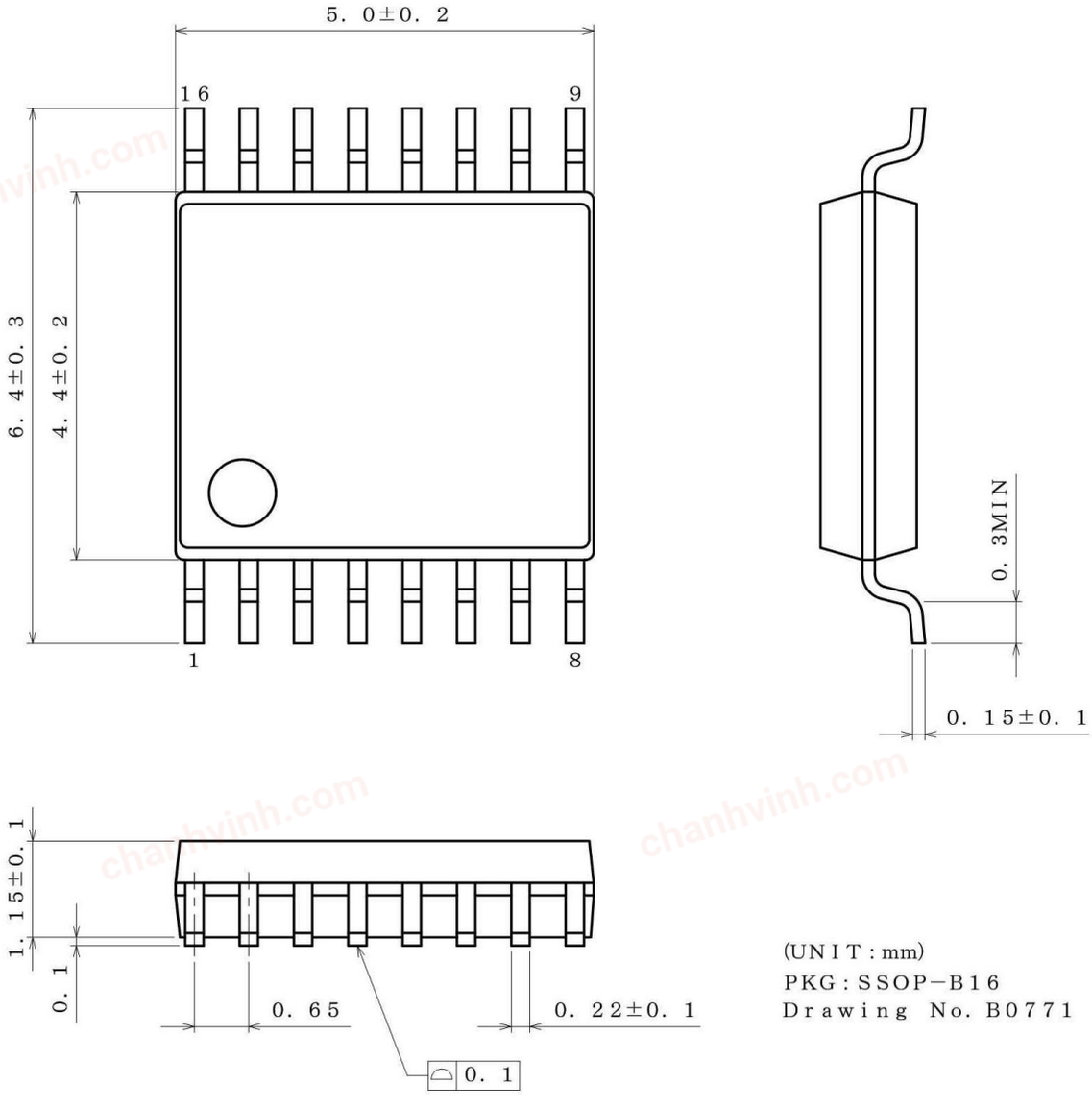


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Physical Dimension, Tape and Reel Information

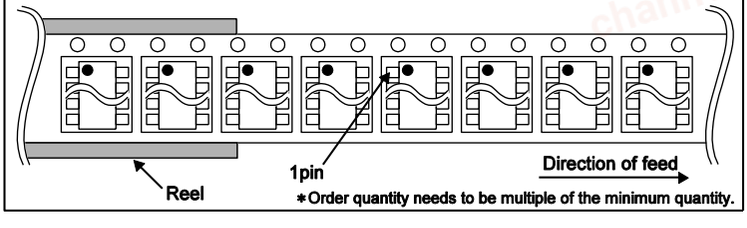
Package Name	SSOP-B16



(UNIT:mm)
PKG:SSOP-B16
Drawing No. B0771

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
2016.03.29	001	New Release
2016.04.21	002	Page.3 Footprints and Traces 74.2mm^2 (Square) ⇒ 74.2mm x 74.2mm Page.12 Table of Operations Operation Mode: TSD PBUS Terminal: High(4.5V(Typ)) to Hi-z
2019.02.28	003	Page.5 Electrical Characteristics1 VREG Terminal Voltage ±3%(Ta= 25 to 125°C) ⇒ ±3%(Ta=-40 to 125°C) ±5%(Ta=-40 to 125°C) Page.16 Formula $V_{OP} = (R_{FB1} + R_{FB2}) \times I_{BASE_Max} + V_{CE_PNP}\ [V]$ ↓ $V_{OP} = V_{IN} - \{(R_{FB1} + R_{FB2}) \times I_{BASE_Max} + V_{CE_PNP}\}\ [V]$ Page. 17 Delete the description of when installing heat sink resistor, or connecting resistor or diodes between OP terminal and LED anode Page. 21 DCDIM terminal must be kept below 1.25V ↓ DCDIM terminal must be kept 1.25V or more Page. 22 Caution of using PBUS terminal Revise the description and the items list Page.25, 26, 27 Recommended Parts List Update discontinued parts to latest parts number Page. 28 Recommended Application Circuit 4 I_{LED}: 150mA ⇒ 120mA Add recommended parts list 4 and delete the description
2023.12.13	004	Page.27 Modified application circuit example (3) Changed by modification of application circuit example (3) Changed the recommended parts list 3

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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