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Datasheet

Automotive LED Driver Series

16-channel Constant Current Driver Embedded Automotive Backlight LED Driver

BD12801MUF-M

General Description

BD12801MUF-M is 16-channel constant current driver with 13 bit PWM dimming and 8 bit local DC dimming individual channels. Communication with µController via SPI is feasible.

Features

- ■AEC-Q100 Qualified*(Note 1)*
- ■Integrated 16-channel 20 V LED Constant Current Driver
- ■SPI Interface
- ■Independent 13 bit PWM Dimming Function
- ■Independent 8 bit Local DC Dimming Function
- ■Independent 8 bit Phase Shift Function
- ■LSI Protection Function (UVLO, TSD, ISETSCP)
- ■LED Abnormality Detection Function (Open/Short)
- ■Integrated Abnormality Output FAIL Pin
- ■Cascade Connection Feasible

(Note 1) Grade 1

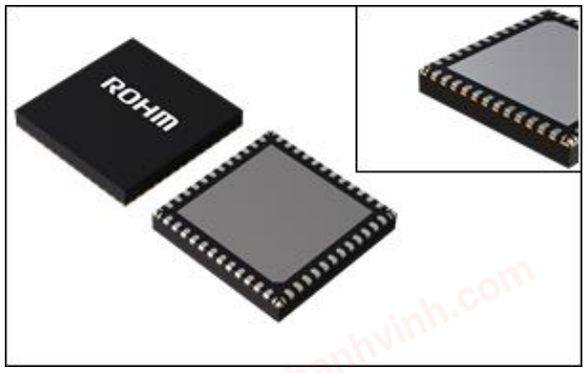
Applications

- ■Cluster, Center Infotainment Display
- ■Other Automotive Backlights

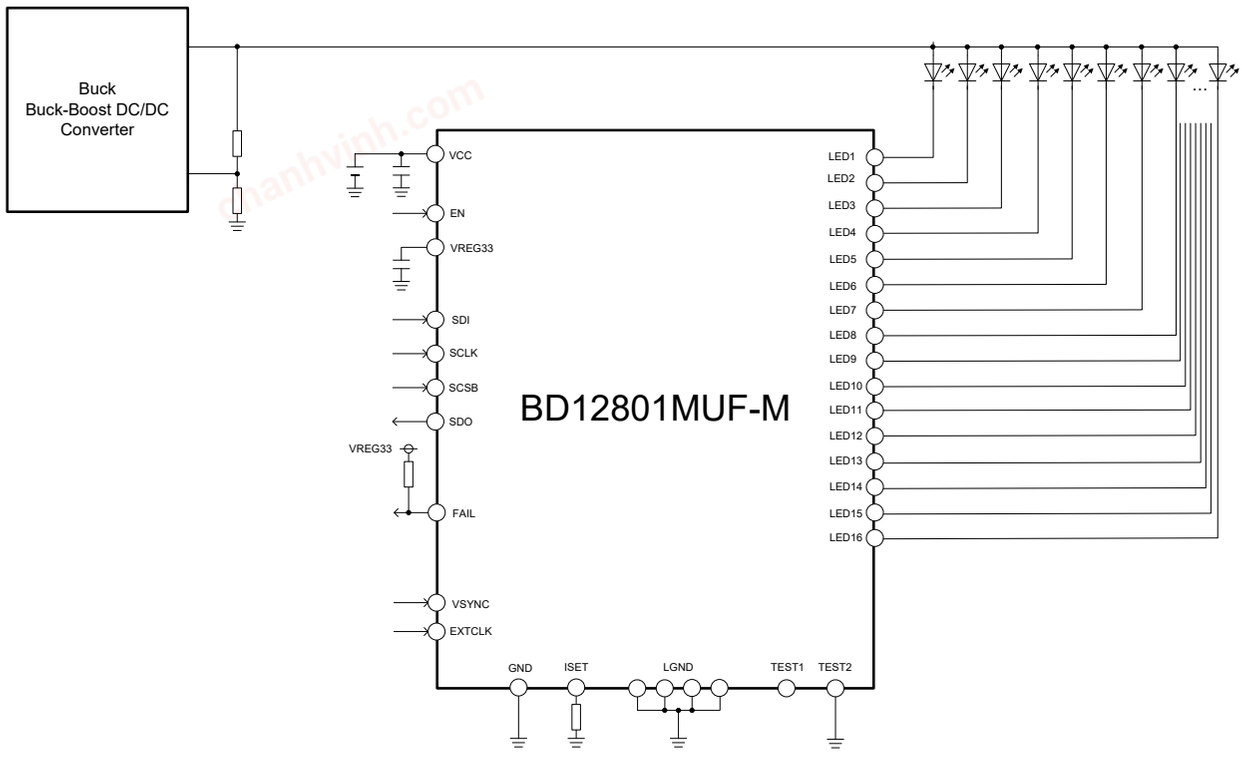
Key Specifications

- ■Power Supply Voltage Range: 3.0 V to 5.5 V
- ■LED Output Current Range: 20 mA to 130 mA
- ■Operating Temperature Range: -40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN48FAV070	7.0 mm x 7.0 mm x 1.0 mm



Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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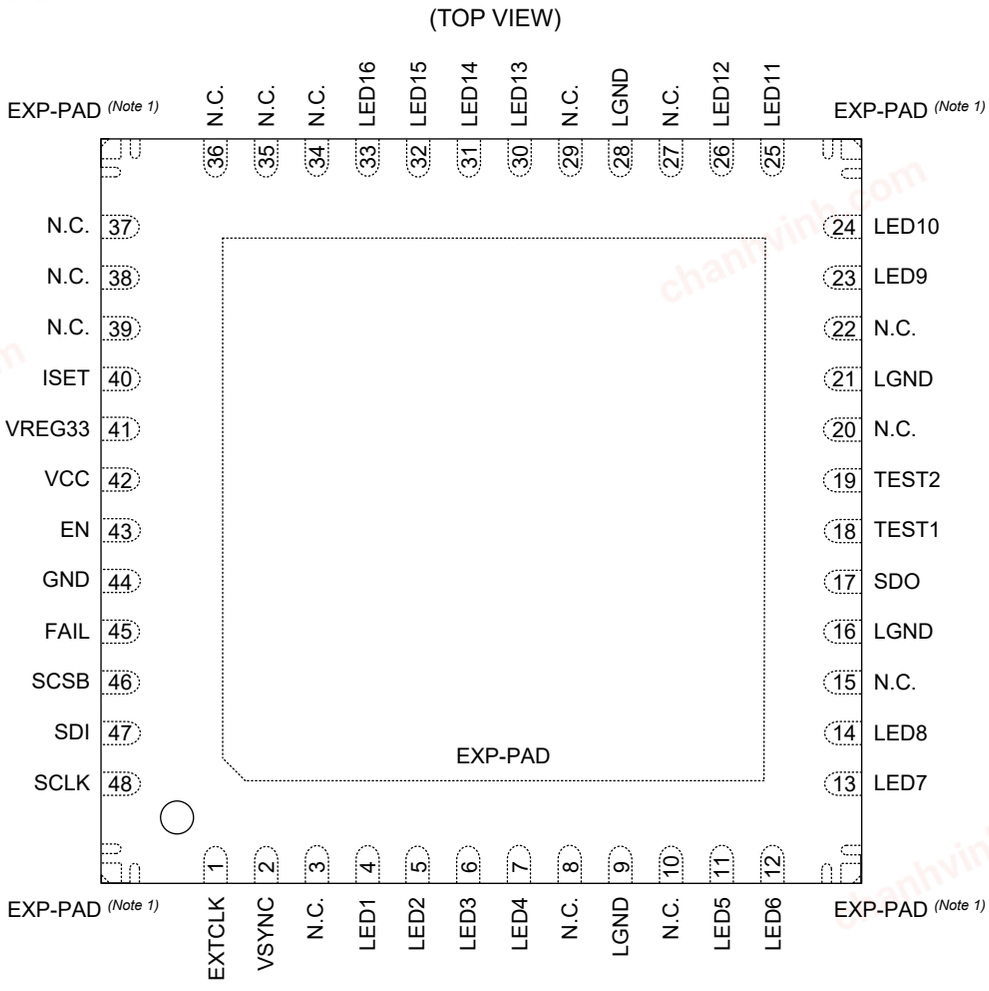
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Pin Configuration



(Note 1) EXP-PAD on the corner is comprised of three electrodes and is short-circuited inside.

Pin Descriptions

Pin No.	Pin Name	Function
1	EXTCLK	EXTCLK signal pin. Input the frequency 8,192 times of VSYNC (PWMFREQ[1:0] = 0).
2	VSYNC	VSYNC signal pin
3	N.C.	-
4	LED1	Constant current output pin. Connect to LED cathode.
5	LED2	Constant current output pin. Connect to LED cathode.
6	LED3	Constant current output pin. Connect to LED cathode.
7	LED4	Constant current output pin. Connect to LED cathode.
8	N.C.	-
9	LGND	Analog GND for constant current driver block
10	N.C.	-
11	LED5	Constant current output pin. Connect to LED cathode.
12	LED6	Constant current output pin. Connect to LED cathode.
13	LED7	Constant current output pin. Connect to LED cathode.
14	LED8	Constant current output pin. Connect to LED cathode.
15	N.C.	-
16	LGND	Analog GND for constant current driver block

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Pin Descriptions - continued

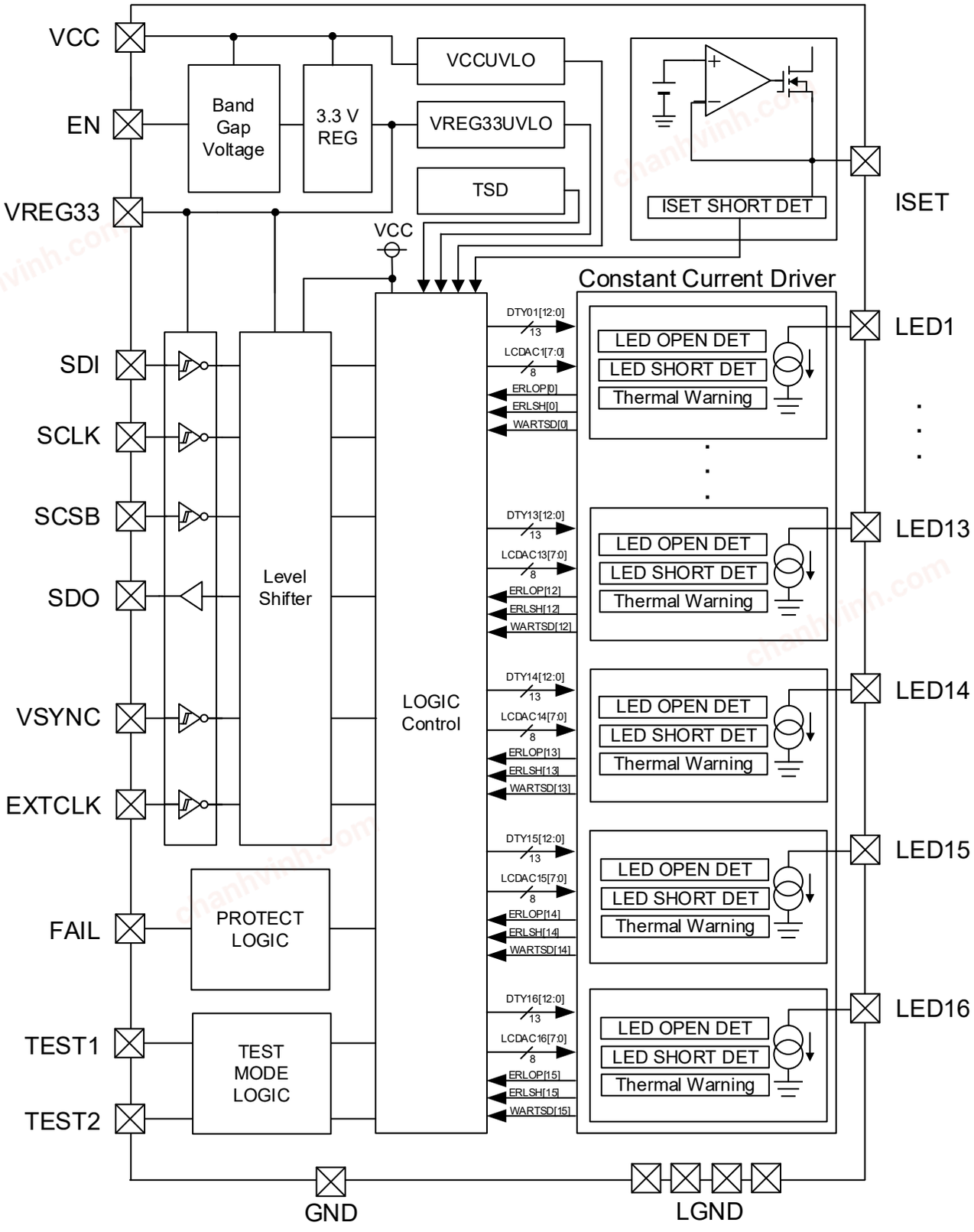
Pin No.	Pin Name	Function
17	SDO	Data output pin.
18	TEST1	TEST mode output pin. Set this pin open.
19	TEST2	TEST mode input pin. Connect to GND.
20	N.C.	-
21	LGND	Analog GND for constant current driver block
22	N.C.	-
23	LED9	Constant current output pin. Connect to LED cathode.
24	LED10	Constant current output pin. Connect to LED cathode.
25	LED11	Constant current output pin. Connect to LED cathode.
26	LED12	Constant current output pin. Connect to LED cathode.
27	N.C.	-
28	LGND	Analog GND for constant current driver block
29	N.C.	-
30	LED13	Constant current output pin. Connect to LED cathode.
31	LED14	Constant current output pin. Connect to LED cathode.
32	LED15	Constant current output pin. Connect to LED cathode.
33	LED16	Constant current output pin. Connect to LED cathode.
34	N.C.	-
35	N.C.	-
36	N.C.	-
37	N.C.	-
38	N.C.	-
39	N.C.	-
40	ISET	LED current setting pin. LED current is set by resistor connected to GND.
41	VREG33	Output 3.3 V constant voltage
42	VCC	Power supply pin
43	EN	Engage Standby-mode with V_{EN} = Low. Operation mode with V_{EN} = High.
44	GND	Small signal GND
45	FAIL	Abnormal detection output pin
46	SCSB	Chip select setting pin
47	SDI	Data input pin
48	SCLK	CLK input pin
-	EXP-PAD	Exposed Pad. Connect center EXP-PAD to the internal PCB ground plane using multiple via, it will provide excellent heat dissipation characteristics.

(Note) LED1 to LED16 are defined as LEDn (n = 1 to 16) from this page.
If there is no use LEDn channel, set open for the pin. If LEDn pin connects to GND, standby current isn't 0 μA (Typ) because there is a current path.

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Block Diagram



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Description of Blocks

If there is no description, the mentioned values are typical value.

1. Reference Voltage (3.3V REG)

3.3V REG Block generates 3.3 V at EN = High, and outputs to the VREG33 pin. This voltage (V_{VREG33}) is used as I/O interface power supply for internal circuit. The VREG33 pin has UVLO function, and it starts operation at $V_{CC} \geq 2.8$ V and $V_{VREG33} \geq 2.7$ V and stops when at $V_{CC} \leq 2.7$ V or $V_{VREG33} \leq 2.6$ V. About the condition to release/detect V_{VREG33} voltage, refer to Table 1. Protection Table. Connect a ceramic capacitor (C_{VREG33}) to the VREG33 pin for phase margin. C_{VREG33} range is 1.0 µF to 4.7 µF and recommended value is 2.2 µF. If the C_{VREG33} is not connected, it might occur unstable operation e.g. oscillation. In addition, VREG33 pin has the over current protection function. If the load current of VREG33 pin exceeds 15 mA, the voltage drops. The following diagram shows the power supply system of MCU and LED Driver. Select the suitable connection in accord with application structure.

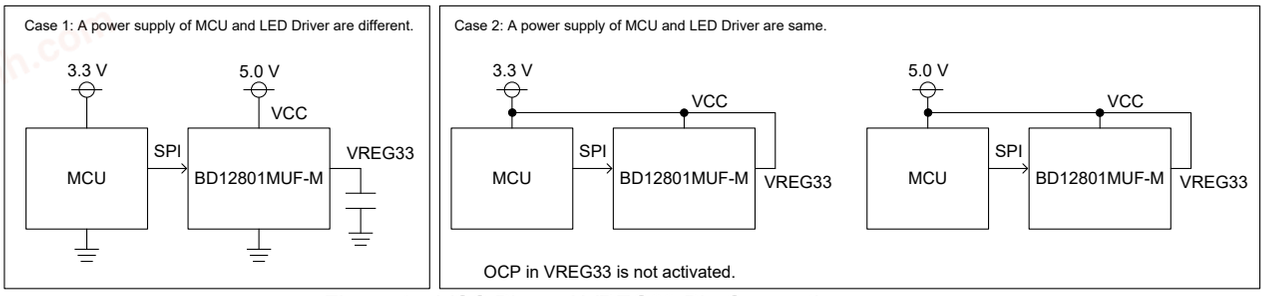


Figure 1. VCC Pin and VREG33 Pin Connection

2. Constant Current Driver

This device integrates 16-channel constant current driver. Constant current drivers capability is defined by supply voltage thus with $V_{CC} \geq 4.2$ V will be 130 mA/ch and with 3.0 V ≤ V_{CC} < 4.2 V will be 100 mA/ch. Also 13 bit PWM dimming function, 8 bit DC dimming function, 8 bit phase shift function are built in for independent channel.

(1) Maximum LED Output Current Setting (R_{ISET})

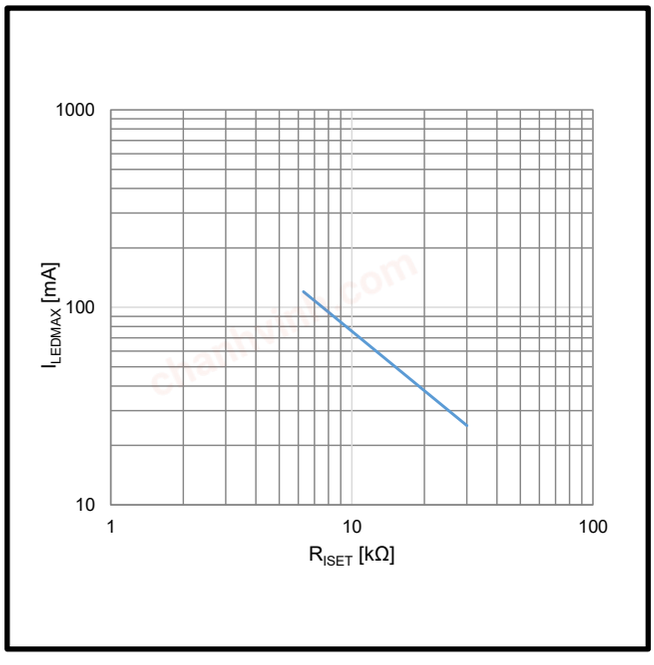


Figure 2. I_{LEDMAX} vs R_{ISET}

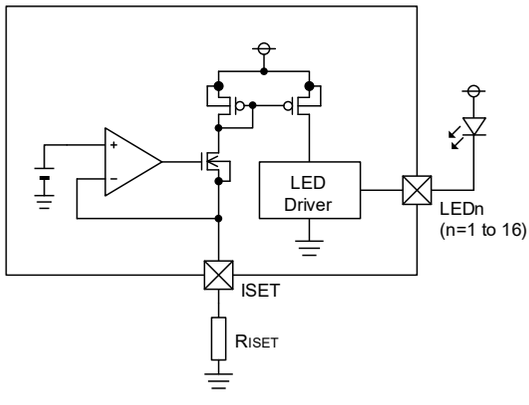


Figure 3. ISET Block Diagram

The Maximum LED Output Current I_{LEDMAX} can be obtained by the following equation.

$$I_{LEDMAX} = 757/R_{ISET} \quad [A]$$

The operating range of the R_{ISET} value is from 6.3 kΩ to 30 kΩ. Additionally, the R_{ISET} value could not be changed during operation. In this IC, ISET SHORT protection is built-in to protect an LED element from excess current when the ISET pin and GND are shorted. If the $R_{ISETSCP}$ is 2.2 kΩ (Typ) or less, the IC detects ISET SHORT protection and LED current is turned off.

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2. Constant Current Driver - continued

(2) Local DC Dimming Control

Integrates 8 bit DC dimming function LCDACn[7:0], which controls LED current of each channel by SPI input from the defined LED current by R_{ISET}. LED current under DC dimming can be calculated in below equation.

$$I_{LEDn} = I_{LEDMAX} \times \{(LCDACn[7:0] + 1)/256\} \quad > \quad 0.02 \quad [A] \quad (n = 1\ to\ 16)$$

In instance when R_{ISET} = 6.3 kΩ and LCDACn[7:0] = 0xFF, LED current will be 120 mA. As minimum LED current of the device is minimum 20 mA, LCDACn[7:0] should be set from 0x2A to 0xFF. Note that LCDACn[7:0] minimum bit cannot be set due to minimum current 20 mA. Step width will be 0.47 mA (= 120 mA / 256). On the other hand R_{ISET} = 19 kΩ and LCDACn[7:0] = 0xFF will set LED current as 40 mA, LCDACn[7:0] should be set from 0x80 to 0xFF. Step width will be 0.156 mA (= 40 mA / 256). LCDACn[7:0] setting range will differ by R_{ISET}.

(3) Local PWM Dimming Control

PWM dimming frequency, pulse width, and phase shift can be controlled by SPI input. Constant current driver can be controlled synchronized to PWM for independent channel set by SPI.

However constant current driver's minimum pulse width depends on LED current value. When LED current value is 80 mA or more, set the minimum pulse width to more than 0.6 µs. If LED current value is less than 80 mA, set the minimum pulse width to more than 2 µs. For example with PWM frequency 200 Hz at LED current of 100 mA setting, it's possible to set with 13 bit full range of PWM duty. Average LED current under PWM dimming can be calculated in below equation.

$$I_{LEDn_AVE} = I_{LEDn} \times \{(DTYn[12:0] + 1)/\ 8{,}192\} \qquad [A] \quad (n = 1\ to\ 16)$$

(4) Local Phase Shift Control

This device integrates 8 bit Phase Shift function. Control by independent channel based on set PWM cycle is feasible. In case PWM frequency is 200 Hz, shift rate per channel can be set by about 20 µs steps. Refer to Figure 4.

To summarize (1) to (3), the LED current setting, PWM dimming, DC dimming are schematically shown as Figure 5.

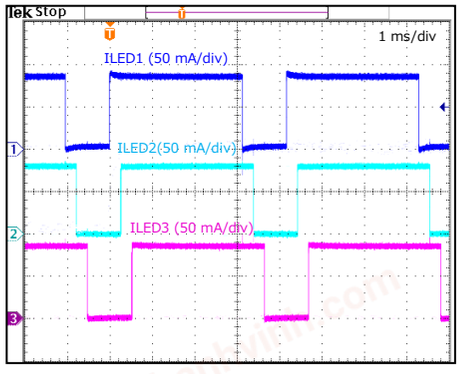


Figure 4. Local Phase Shift Control

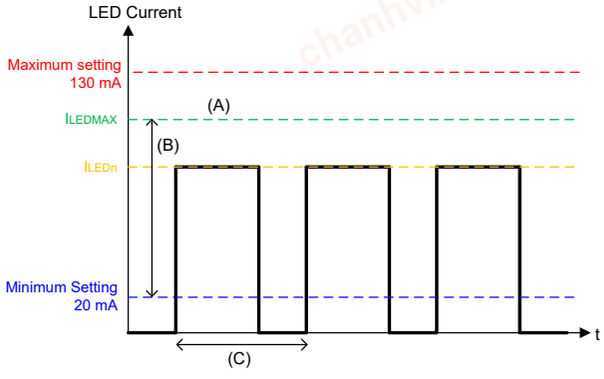


Figure 5. Setting Range by Dimming Method

(A) I_{LEDMAX} is set to the maximum LED current value from 20 mA to 130 mA by R_{ISET}.
(B) When I_{LEDMAX} is set to 80 mA by R_{ISET}, DC dimming range is limited from 64 to 256 because of minimum LED current setting 20 mA.
(C) PWM dimming can be controlled by 13 bit range.

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Description of Blocks - continued

3. Protection Feature

Table 1. Protection Table

Protection Name	Protection			Error Setting(Note 4)				Error Flag			Recommend Operation
	Pin	Detection Condition	Release Condition	Error Enable	SSMASK	ERRMASK	ERRLAT	Error Register	FAIL(Note 6)	Clear Condition	
LED OPEN	LEDn(Note 3)	DTYENn = 1 and LEDOPEN = 1 and [PWMn = High and V_{LEDn}(Note 3) ≤ 0.2 V]	DTYENn = 0 or LEDOPEN = 0 or [PWMn = High and V_{LEDn}(Note 3) > 0.2 V]	LEDOPEN	O	O	O	ERLOP[15:0]	Low	Protection released (ERRLAT = 0) or ERRCLR (ERRLAT = 1)	target LEDn(Note 3) OFF (DTYENn(Note 3) = 0)
LED SHORT	LEDn(Note 3)	DTYENn = 1 and LEDSHEN = 1 and [PWMn = High and V_{LEDn}(Note 3) ≥ register setting]	DTYENn = 0 or LEDSHEN = 0 or [PWMn = High and V_{LEDn}(Note 3) < register setting]	LEDSHEN	O	O	O	ERLSH[15:0]	Low	Protection released (ERRLAT = 0) or ERRCLR (ERRLAT = 1)	target LEDn(Note 3) OFF (DTYENn(Note 3) = 0)
LED SCP(Note 1)	LEDn(Note 3)	DTYENn = 0 and LEDOPEN = 1 and V_{LEDn}(Note 3) ≤ 0.2 V during SCP setting time (after detecting LED Open Error)	TSD detect or EN detect or VCCUVLO detect or VREG33UVLO detect	LEDOPEN	O	-	-	WARSCP	VSYNC	TSD detect or EN detect or VCCUVLO detect or VREG33UVLO detect	All LEDn(Note 3) OFF
ISET SHORT	ISET	R_{SETSCP} ≤ 2.2 kΩ	R_{SETSCP} > 2.2 kΩ	-	O	-	O	WARISET	Low	Protection released (ERRLAT = 0) or ERRCLR (ERRLAT = 1)	LED1 to 16 OFF (automaticaly)
Thermal Warning	-	Tj ≥ 135 °C	Tj ≤ 125 °C	TSDWEN	O	-	O	WARTSD[15:0] (Note 2)	Low	Protection released (ERRLAT = 0) or ERRCLR (ERRLAT = 1)	target LEDn OFF (DTYENn(Note 3) = 0)
TSD(Note 5)	-	Tj ≥ 175 °C	Tj ≤ 150 °C	-	-	-	-	-	Low	Protection released	All block initialized (automaticaly)
VCCUVLO(Note 5)	VCC	V_{CC} ≤ 2.7 V	V_{CC} ≥ 2.8 V	-	-	-	-	-	High (Hi-z)	-	All block initialized (automaticaly)
VREG33UVLO(Note 5)	VREG33	V_{VREG33} ≤ 2.6 V	V_{VREG33} ≥ 2.7 V	-	-	-	-	-	High (Hi-z)	-	All block initialized (automaticaly)

(Note 1) It can't detect "SCP error" if LEDn (n = 1 to 16) pin shorts GND before setting DTYEN = 1 and detecting "LED open error". This function is available after detecting "LED open error".
(Note 2) WARTSD[n-1]: monitor LEDn
(Note 3) n = 1 to 16
(Note 4) O: It has this function. -: It doesn't have this function.
(Note 5) When it detects "VREG33UVLO" or "VCCUVLO" or "TSD" or "EN", it can't detect other protection.
(Note 6) The FAIL pin is recommended to pull up to V_{VREG33}. Recommended value for pull up resistance is 20 kΩ to 100 kΩ.
When above failure is detected, the FAIL pin voltage becomes Low. If the FAIL pin is not used pin, it shall be kept open or short to GND.

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Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	-0.3 to +7.0	V
EN Pin Voltage	V_{EN}	-0.2 to +7.0	V
LED1 to LED16 Pin Voltage	V_{LED1} to V_{LED16}	-0.2 to +20.0	V
FAIL Pin Voltage	V_{FAIL}	-0.3 to +7.0	V
VREG33, SCSB, SCLK, SDI, SDO, VSYNC, EXTCLK, TEST1, TEST2, ISET Pin Voltage	V_{VREG33}, V_{SCSB}, V_{SCLK}, V_{SDI}, V_{SDO}, V_{VSYNC}, V_{EXTCLK}, V_{TEST1}, V_{TEST2}, V_{ISET}	-0.2 to +7.0	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN48FAV070				
Junction to Ambient	θ_{JA}	71.4	24.2	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	6.0	3.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power Supply Voltage	V_{CC}	3.0	5.0	5.5	V	
VREG33 Pin Connect Capacitance	C_{VREG33}	1.0	2.2	4.7	µF	
ISET Pin Connection Resistance	R_{ISET}	6.3	-	30.0	kΩ	
FAIL Pin Connection Resistance	R_{FAIL}	20	-	100	kΩ	
EXTCLK Frequency	f_{EXTCLK}	409.6	-	5,000.0	kHz	
EXTCLK Duty	D_{EXTCLK}	40	-	60	%	
VSYNC Frequency	$f_{VSYNCCLK}$	50	-	600	Hz	
VSYNC Minimum Pulse Width	$t_{VSYNCMIN}$	50	-	-	µs	
LEDn Output Current 1	$I_{LEDMAX1}$	20	-	100	mA	3.0 V ≤ V_{CC} < 4.2 V
LEDn Output Current 2	$I_{LEDMAX2}$	20	-	130	mA	V_{CC} ≥ 4.2 V
Operating Temperature	Topr	-40	+25	+125	°C	

(Note) Above operation range is referring to IC independently. Thorough verification of the coefficient setting in actual application shall be practiced.

Electrical Characteristics

(Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC} = 3.0 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Device Overview]						
Circuit Current	I_{CC}	-	5.5	15.0	mA	V_{EN} = High, All Current drivers are OFF
Standby Current	I_{STB}	-	0	300	µA	V_{EN} = Low
[VREG33 Block]						
VREG33 Pin Output Voltage	V_{VREG33}	3.1	3.3	3.5	V	V_{CC} = 3.5 V to 5.5 V, I_{VREG33} = 0 mA
VREG33 Pin Load Regulation Voltage	ΔV_{VREG33}	-	30	80	mV	V_{CC} = 3.5 V to 5.5 V, I_{VREG33} = -5 mA
VREG33 Pin Over Current Protection	$I_{VREG33OCP}$	10	-	-	mA	V_{CC} = 5.0 V
[PROTECT LOGIC Block]						
VCCUVLO Detection Voltage	$V_{VCCUVLO}$	2.55	2.70	2.85	V	V_{CC}: SWEEP DOWN
VCCUVLO Hysteresis Voltage	$V_{VCCUHYS}$	-	100	-	mV	
VREG33UVLO Detection Voltage	$V_{VREG33UVLO}$	2.40	2.60	2.80	V	V_{VREG33}: SWEEP DOWN
VREG33UVLO Hysteresis Voltage	$V_{VREG33UHYS}$	-	100	-	mV	
LED OPEN Detection Voltage	V_{OPDET}	0.1	0.2	0.3	V	V_{LEDn}: SWEEP UP
LED SHORT Detection Voltage	V_{SHDET}	4.5	4.8	5.1	V	LEDSH = 0xF
ISET GND Short Detection Resistance	R_{SETSCP}	0.7	2.2	4.3	kΩ	
Thermal Warning Monitor Detection Temperature	t_{MON}	-	135	-	°C	
Thermal Warning Monitor Hysteresis Width	t_{MONHYS}	-	10	-	°C	

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Electrical Characteristics - continued

(Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC} = 3.0 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Constant Current Driver Block]						
ISET Pin Reference Voltage	V_{ISET}	-	0.606	-	V	
LEDn Pin ON Resistance	R_{LED1}	-	-	6.5	Ω	
LEDn Pin Output Current1 *(Note 1)*	I_{OUT1}	94	100	106	mA	
LEDn Pin Output Current Absolute Error1 *(Note 1)*	ΔI_{OUTA1}	-4	-	+4	%	Ta = 25 °C, V_{CC} = 5 V
		-6	-	+6	%	
LEDn Pin Output Current Relative Error1 *(Note 1)*	ΔI_{OUTR1}	-4	-	+4	%	Ta = 25 °C, V_{CC} = 5 V
		-6	-	+6	%	
LEDn Pin Output Current2 *(Note 2)*	I_{OUT2}	45	50	55	mA	
LEDn Pin Output Current Absolute Error2 *(Note 2)*	ΔI_{OUTA2}	-6	-	+6	%	Ta = 25 °C, V_{CC} = 5 V
		-7.5	-	+7.5	%	
LEDn Pin Output Current Relative Error2 *(Note 3)*	ΔI_{OUTR2}	-6	-	+6	%	Ta = 25 °C, V_{CC} = 5 V
		-7.5	-	+7.5	%	
[EN Input Pin]						
EN Pin Input Current	I_{EN}	18	30	50	µA	V_{EN} = 3.0 V
EN Pin Input High Voltage	V_{ENH}	0.8 x V_{VREG33}	-	V_{VREG33} + 0.2	V	
EN Pin Input Low Voltage	V_{ENL}	-0.2	-	+0.2 x V_{VREG33}	V	
[LOGIC Input (SCSB, SCLK, SDI, EXTCLK, VSYNC)]						
LOGIC Pin Input Current	I_{IN}	-1	0	+1	µA	V_{IN} = V_{CC}
LOGIC Pin Input High Voltage	V_{INH}	0.8 x V_{VREG33}	-	V_{VREG33} + 0.2	V	
LOGIC Pin Input Low Voltage	V_{INL}	-0.2	-	+0.2 x V_{VREG33}	V	
[LOGIC Output Block (SDO)]						
SDO Pin Output High Voltage	V_{SDOH}	V_{VREG33} -0.2	-	V_{VREG33} +0.2	V	I_{SDO} = -1 mA
SDO Pin Output Low Voltage	V_{SDOL}	-	-	0.2	V	I_{SDO} = +1 mA
[FAIL Output Block]						
FAIL Pin ON Resistance	R_{FAIL}	0.5	1.0	2.0	kΩ	I_{FAIL} = +1 mA
FAIL Pin Leak Current	$I_{LEAKFAIL}$	-	-	0.1	µA	V_{FAIL} = 5.0 V

(Note 1) R_{ISET} = 7.5 kΩ, V_{LEDn} = 0.65 V, SDI = w(0x18,0xFF), w(0x19,0x3F)
(Note 2) R_{ISET} = 15 kΩ, V_{LEDn} = 0.65 V, SDI = w(0x18,0xFF), w(0x19,0x3F)
(Note 3) V_{LEDn} describes either pin of LED1 to LED16 voltage.
I_{LEDn} describes either pin of LED1 to LED16 current.
$\Delta I_{OUTA1} = (I_{LEDn}/0.1 - 1) \times 100$
$\Delta I_{OUTR1} = (I_{LEDn}/I_{LED_AVE} - 1) \times 100$
I_{LED_AVE} describes the average current of LED1 to LED16.

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Typical Performance Curves

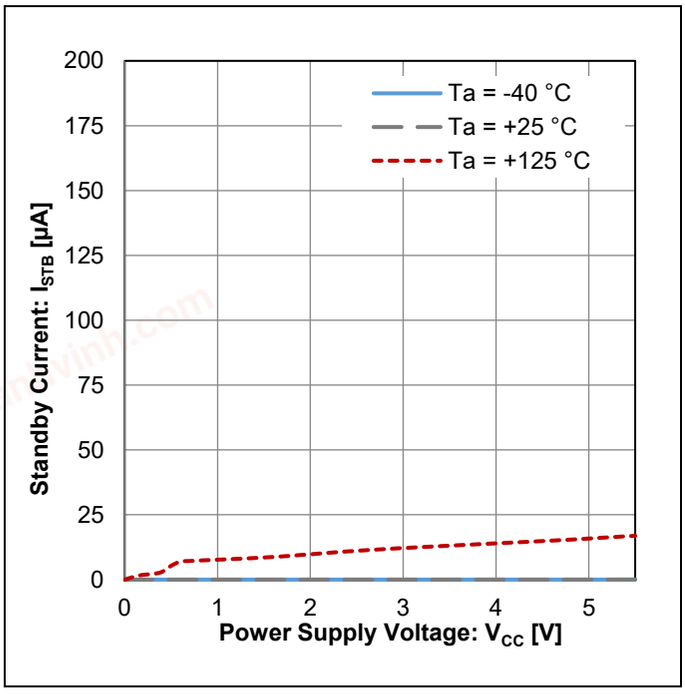


Figure 6. Standby Current vs Power Supply Voltage

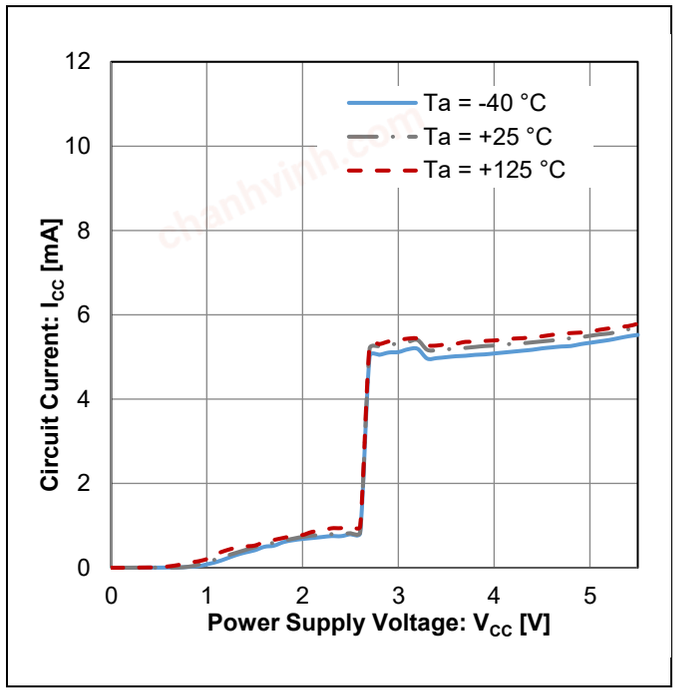


Figure 7. Circuit Current vs Power Supply Voltage (V_{EN} = High)

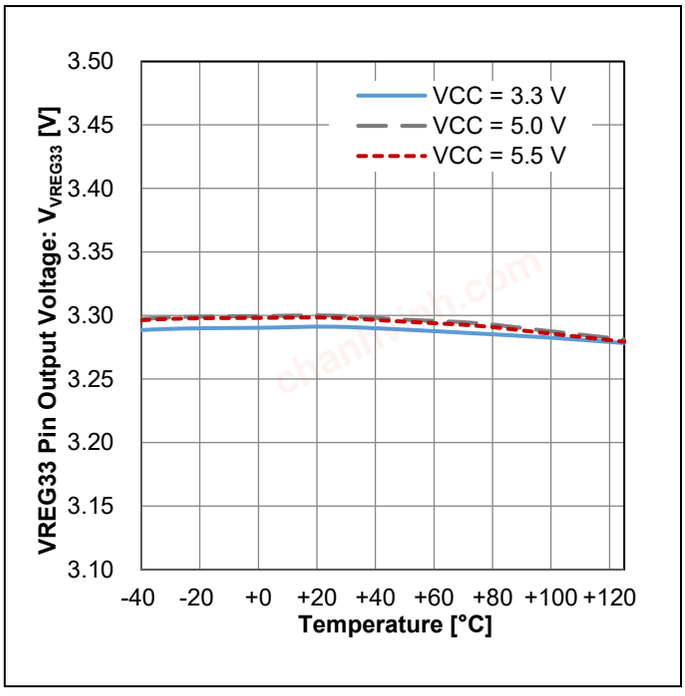


Figure 8. VREG33 Pin Output Voltage vs Temperature

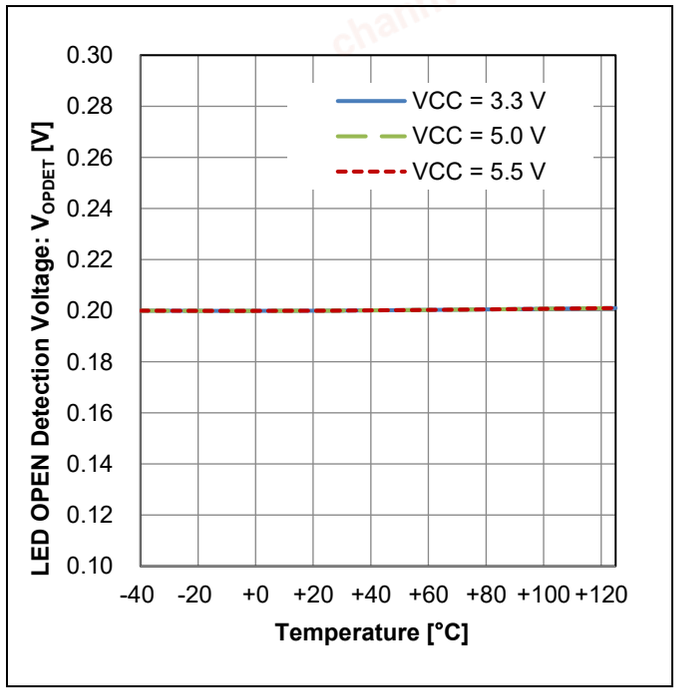


Figure 9. LED OPEN Detection Voltage vs Temperature

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Typical Performance Curves - continued

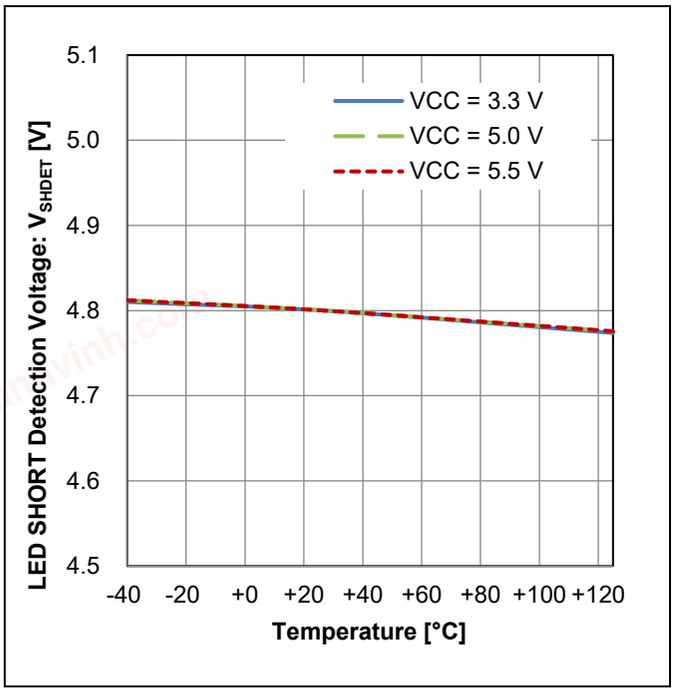


Figure 10. LED SHORT Detection Voltage vs Temperature

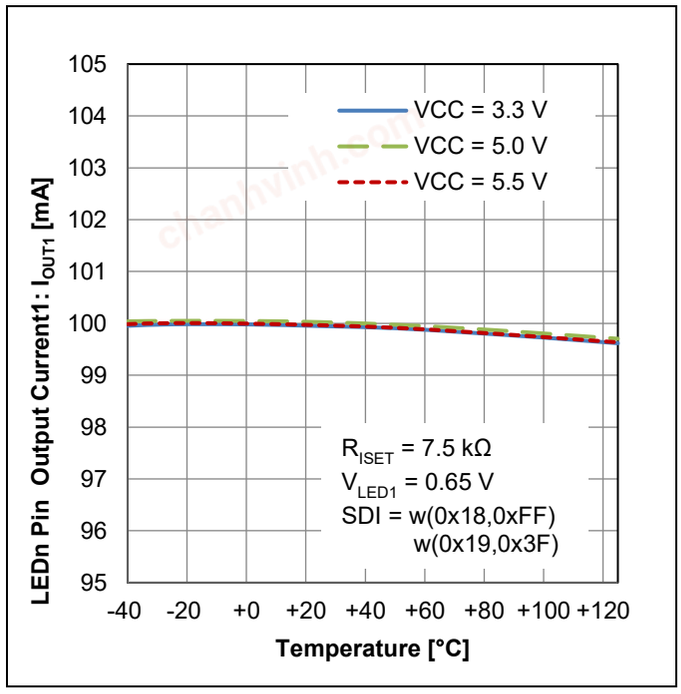


Figure 11. LEDn Pin Output Current1 vs Temperature

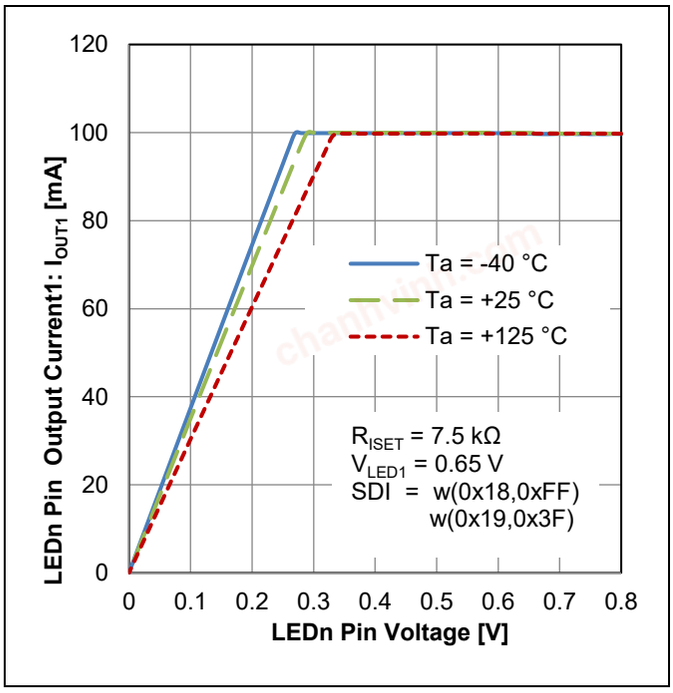


Figure 12. LEDn Pin Output Current1 vs LED Pin Voltage (VCC = 3.3 V)

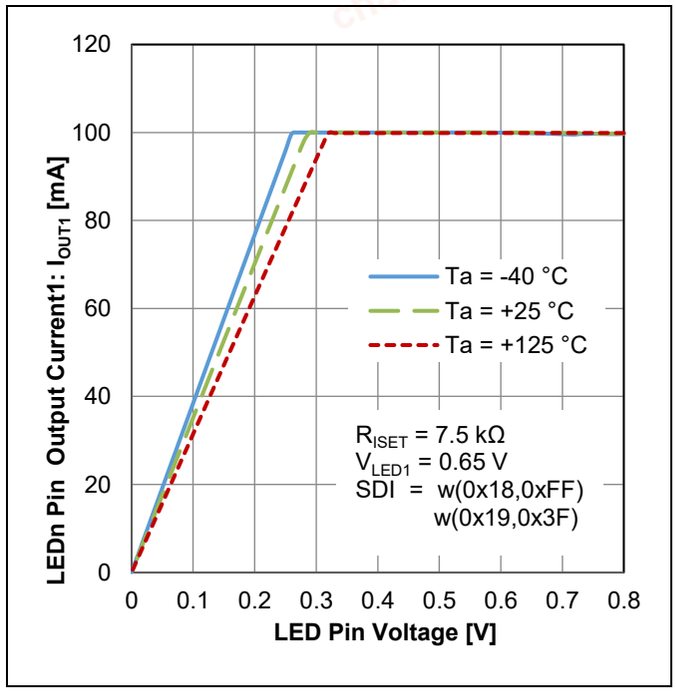


Figure 13. LEDn Pin Output Current1 vs LED Pin Voltage (VCC = 5.0 V)

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Functions of Logic Blocks

1. Serial Interface and AC Electrical Characteristics

Serial Peripheral Interface (SPI) controls the IC with SCSB, SCLK, SDI, and SDO signals.
Start the SPI communication with the initial value of SCSB is 'High', and that of SCLK and SDI is 'Low'.
When using several devices, connect the SDO pin to the SDI pin of the next device to make cascade connection.
SDO signal is output after SDI input from 8 datas. Example of the n byte Write is shown in the following.
SDO is in the state of output the signals. (initial value is 'Low')

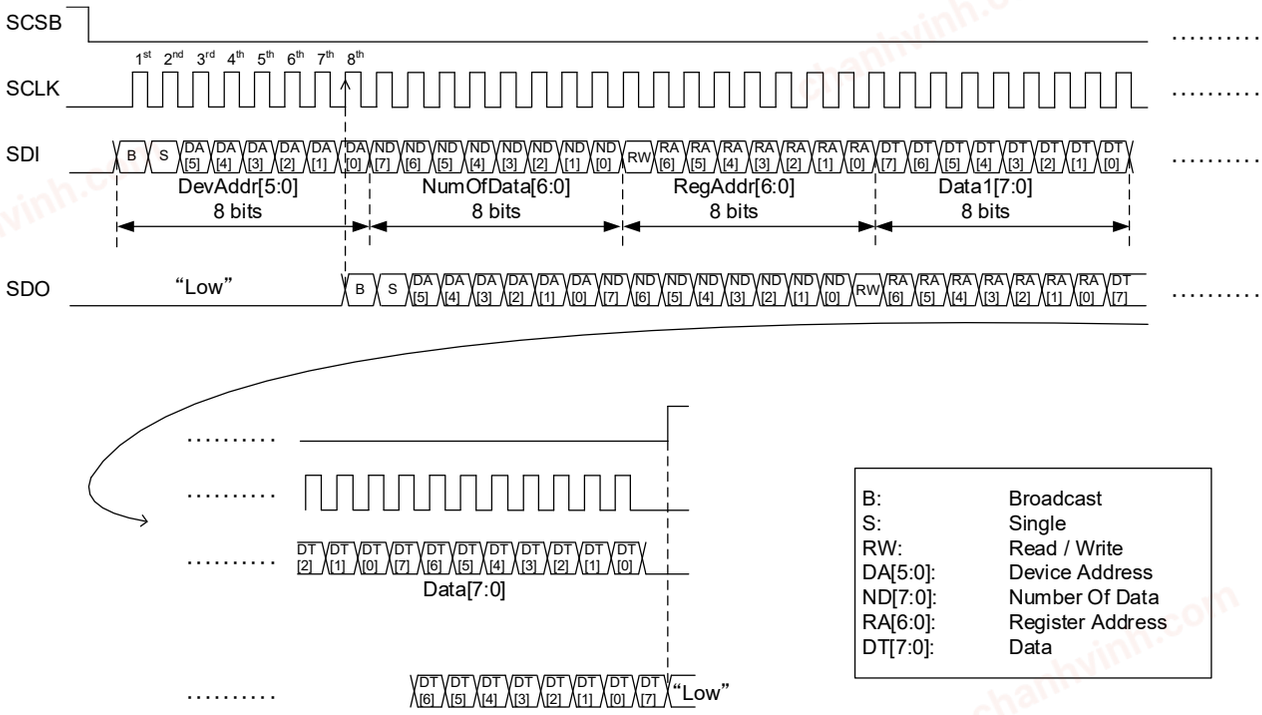


Figure 14. SPI Protocol (Write)

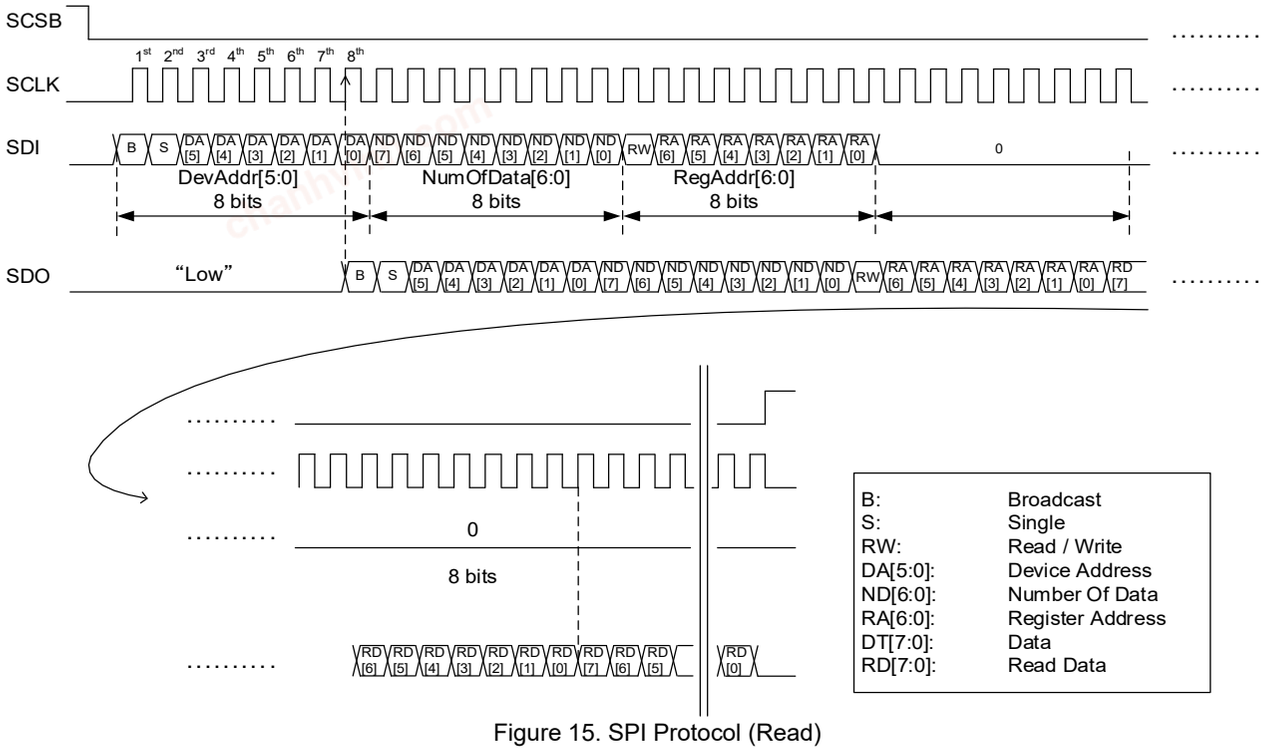


Figure 15. SPI Protocol (Read)

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Functions of Logic Blocks - continued

2. SPI AC Timing

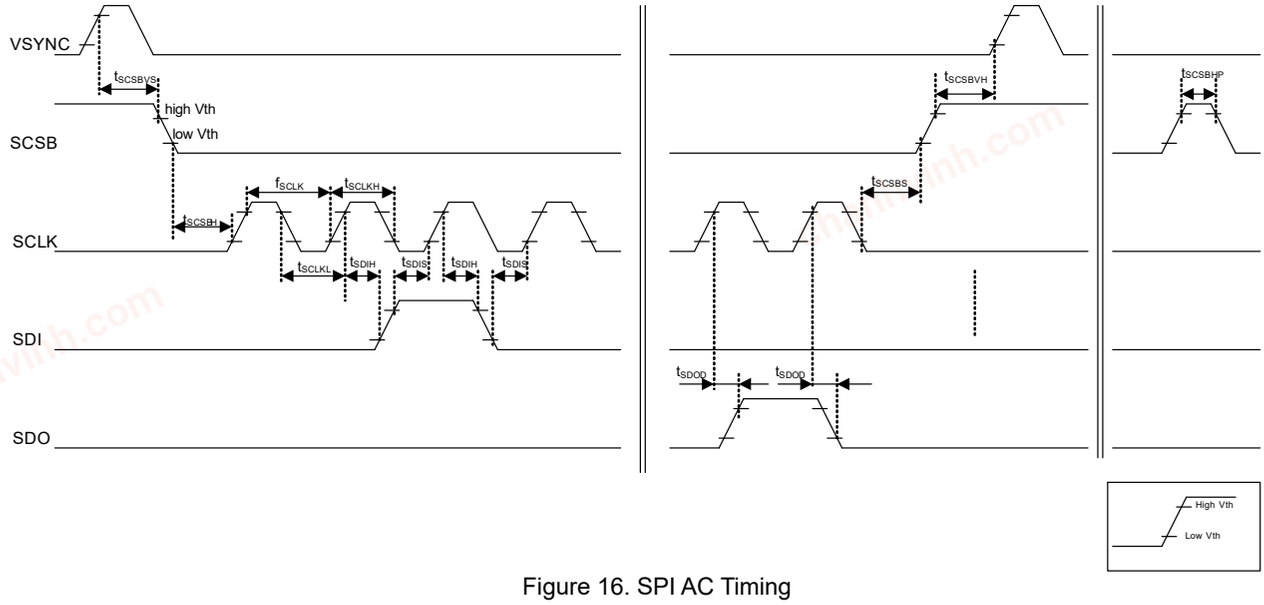


Figure 16. SPI AC Timing

Table 2. SPI AC Timing

Recommended Operation Condition (Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC} = 3.0 V to 5.5 V)

Parameter	Symbol	Rating			Unit	Comments
		Min	Typ	Max		
SCLK Frequency	f_{SCLK}	0.1	-	5	MHz	
SCLK Duty	D_{SCLK}	40	-	60	%	
SCLK High Level Range	t_{SCLKH}	70	-	-	ns	
SCLK Low Level Range	t_{SCLKL}	70	-	-	ns	
SDI Input Setup Time	t_{SDIS}	40	-	-	ns	
SDI Input Hold Time	t_{SDIH}	25	-	-	ns	
SCSB Input Setup Time	t_{SCSBS}	100	-	-	ns	
SCSB Input Hold Time	t_{SCSBH}	100	-	-	ns	
SDO Output Delay Time	t_{SDOD}	25	-	140	ns	V_{CC} = V_{VREG33}: 3.0 V to 3.6 V
		15	-	100	ns	V_{CC} = V_{VREG33}: 4.5 V to 5.5 V
		15	-	140	ns	V_{CC} = V_{VREG33}: 3.0 V to 5.5 V
SCSB High Pulse Width	t_{SCSBHP}	1000	-	-	ns	
SCSB Setup Time for VSYNC	t_{SCSBVS}	10	-	-	µs	
SCSB Hold Time for VSYNC	t_{SCSBVH}	10	-	-	µs	

(Output load capacitance: 15 pF)

(Note) It is not available to input VSYNC during SCSB = L.

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Functions of Logic Blocks - continued

3. Cascade Connection

Each device can be controlled by connecting the SCLK and SCSB pins to all devices in parallel, and by connecting each SDO to the SDI of the next device in series. The maximum number of devices that can be cascaded is 16.

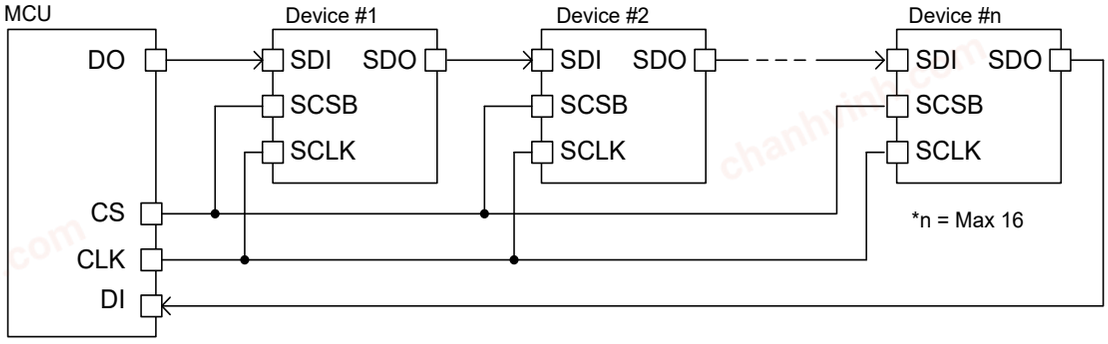


Figure 17. Image of Cascade Connection

4. SPI Data Flow

MCU Write and Read as following flow. This IC has 3 timing for update analog control data.

Type A (immediately):	It updates data after SPI access.
Type B (VSYNC):	It updates data after SPI access and VSYNC rising edge.
Type C (PWM):	It updates data after SPI access and VSYNC and PWM rising edge. (PWM is internal signal set by SPI)

So, there is mismatch between “Read data” and “Control data”.

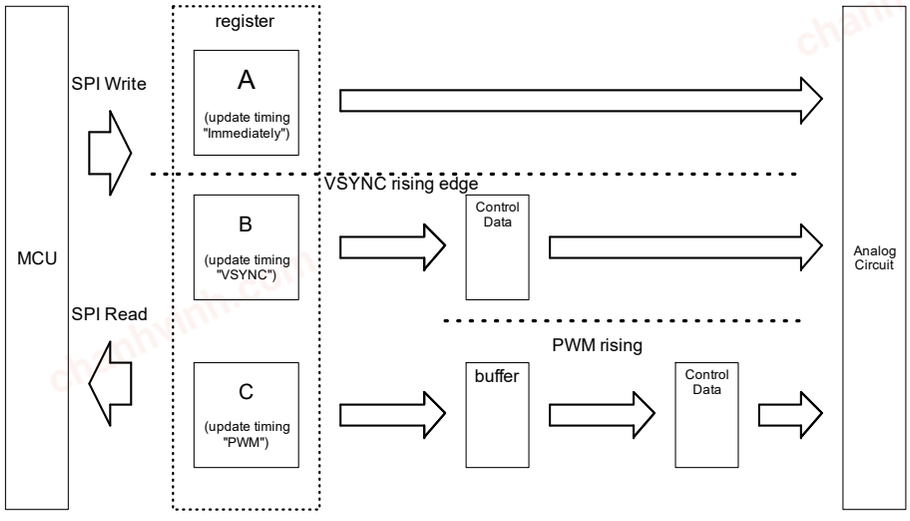


Figure 18. SPI Data Flow

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Functions of Logic Blocks - continued

5. SPI Protocol

(1) Device Address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
B	S	DevAddr [5:0]					

Bit	Parameter	Function
B	Broadcast	B = 1: All chips receive the data (Write only/No Read) B = 0: Write/Read to the chip that assigned by DevAddr [5:0]
S	Single byte	S = 1: 1 byte Write/Read mode S = 0: block Write/Read mode
DevAddr [5:0]	Device Address	0x00: Write the same data to the same RegAddr of all devices (Provided, B = 1) 0x01 to 0x3E: Each Device Address 0x3F: Write the different data to the same RegAddr of all devices (Provided, B = 1)

DevAddr of each device will be calculated by counting the number of byte of 0x00 data after the fall-edge of SCSB. When matching the received DevAddr and calculated DevAddr of the device, Write/Read function will occur. When unmatching the received DevAddr and calculated DevAddr of the chip, not taking in the data and output to SDO. Refer to the each protocol for the details.

(2) Number of transferred byte when block Write/Read

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	NumOfData [6:0]						

Bit	Parameter	Function
NumOfData [6:0]	Number of transferred byte for one device	0x02 to 0x48

When S = 0 (Block Write/Read) of DevAddr, set the number of transferred byte (NumOfData) after DevAddr.
When S = 1, it skip this packet. (“Device Address” ->“Register Address” ->….)
Transferred byte number = NumOfData

Table 3. Access Table for Write (RW = 0)

SPI setting				Access to devices			Acceptable *(Note 1)*
					For All device		
B	S	DevAddr	NumOfData	For single device	Same data	Different data	
0	0	0x00	0x02 to 0x48	-	-	-	X
		0x01 to 0x3E		O	-	-	O
		0x3F		-	-	-	X
	1	0x00	Not sending this data	-	-	-	X
		0x01 to 0x3E		O	-	-	O
		0x3F		-	-	-	X
1	0	0x00	0x02 to 0x48	-	O	-	O
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	O	O
	1	0x00	Not sending this data	-	O	-	O
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	O	O

(Note 1) X: This setting isn’t acceptable. Don’t set this condition.

Table 4. Access Table for Read (RW = 1)

SPI setting				Access to devices			Acceptable *(Note 1)*
					For All device		
B	S	DevAddr	NumOfData	For single device	Same data	Different data	
0	0	0x00	0x02 to 0x48	-	-	-	X
		0x01 to 0x3E		O	-	-	O
		0x3F		-	-	-	X
	1	0x00	Not sending this data	-	-	-	X
		0x01 to 0x3E		O	-	-	O
		0x3F		-	-	-	X
1	0/1	0x00	0x02 to 0x48	-	-	-	X
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	-	X

(Note 1) X: This setting isn’t acceptable. Don’t set this condition.

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5. SPI Protocol - continued

(3) Register Address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RW	RegAddr [6:0]						

Bit	Parameter	Function
RW	Read/Write	RW = 0: Write the registers RW = 1: Read the registers
RegAddr [6:0]	Register Address	0x00 to 0x4F

(4) Data

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Data [7:0]							

Bit	Parameter	Value
Data [7:0]	Data	0x00 to 0xFF

(5) Single device, 1 byte Write (Write to Device #1)

B:	0	Target Device receives the data
S:	1	Single byte
DevAddr[5:0]:	0x01	Target Device Address
NumOfData[6:0]:	-	1 byte Write mode
RW:	0	Write
RegAddr[6:0]:	0x02	Address

SDI : Transfer in the order of DevAddr, RegAddr, and Data.
SDO : The data input to SDI is output with a 1 byte shift.

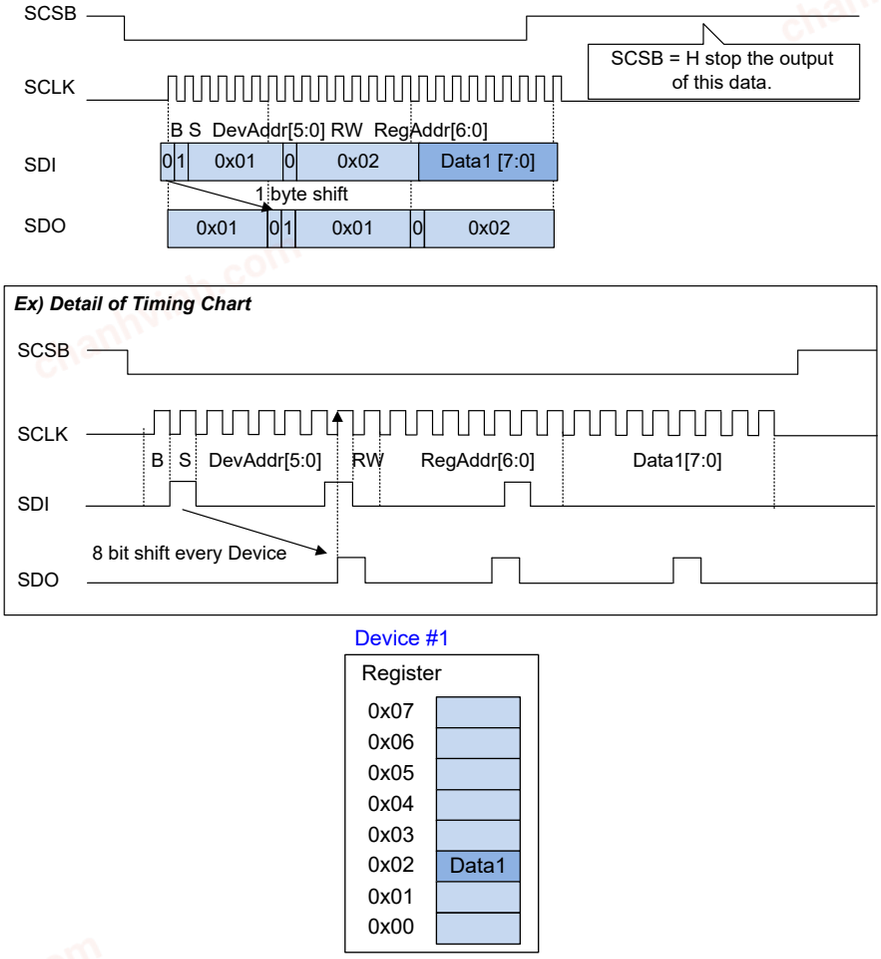


Figure 19. SPI Protocol of the 1 Byte Write to Device #1

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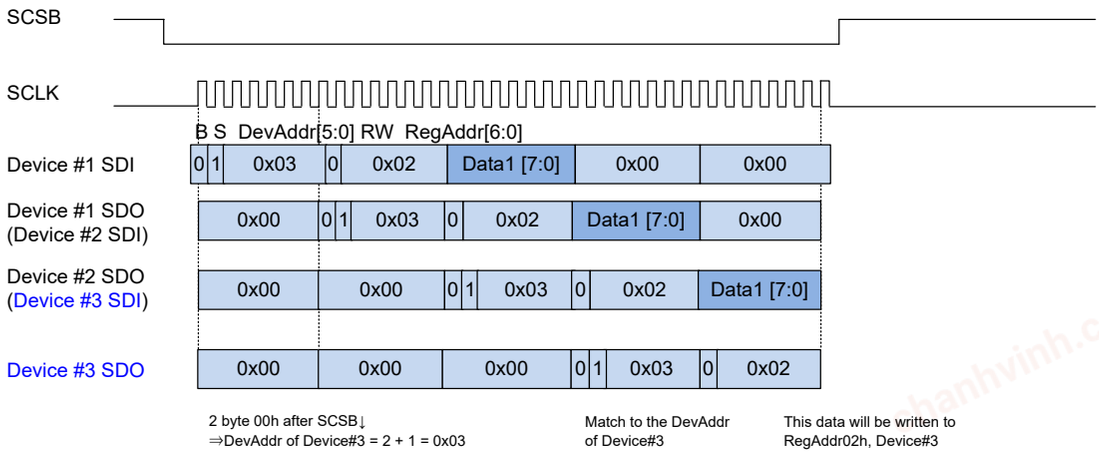
5. SPI Protocol - continued

(6) Single device, 1 byte Write (Write to Device #3)

B:	0	Target Device receives the data
S:	1	Single byte
DevAddr[5:0]:	0x03	Target Device Address
NumOfData[6:0]:	-	1 byte Write mode
RW:	0	Write
RegAddr[6:0]:	0x02	Address

SDI : Transfer in the order of DevAddr, RegAddr, and Data.
SDO : Output the transferred data to the next device after SDI input by 1 byte.

DevAddr of each device will be calculated by counting the number of byte of 0x00 data after the fall-edge of SCSB.
DevAddr = (Number of byte of 0x00 data) + 1



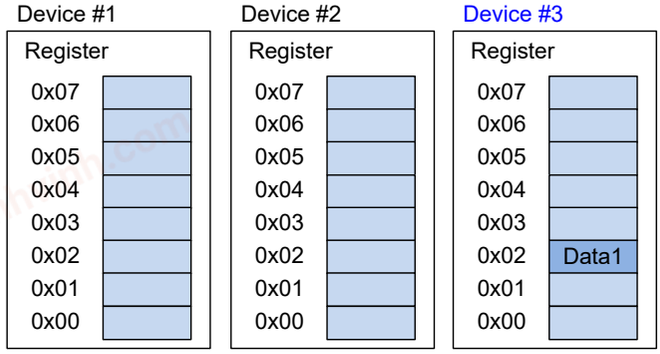


Figure 20. SPI Protocol of the 1 Byte Write to Device #3

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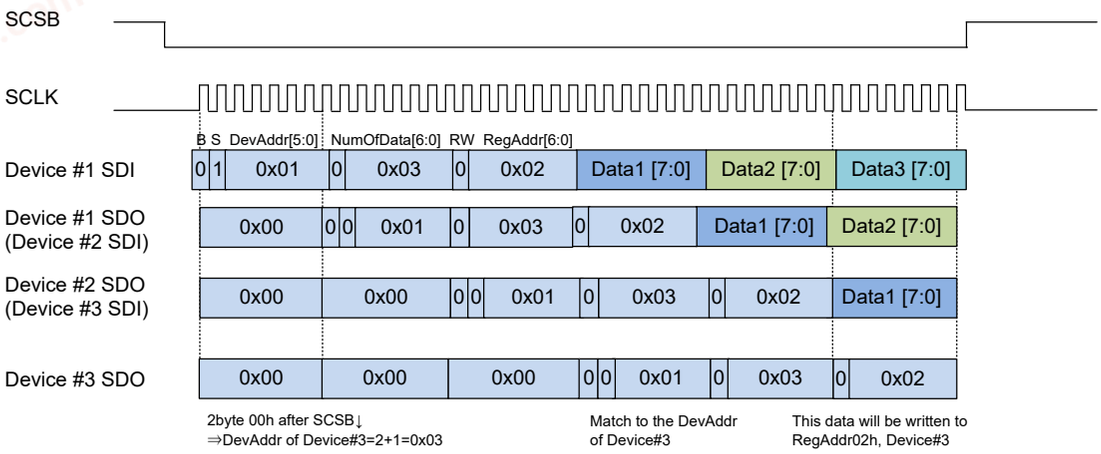
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5. SPI Protocol - continued

(7) Single device, “n byte” Write (Write to the consecutive register of Device #1)

B:	0	Target Device receives the data
S:	0	Single byte
DevAddr[5:0]:	0x01	Target Device Address
NumOfData[6:0]:	0x03	3 byte Write mode
RW:	0	Write
RegAddr[6:0]:	0x02	Address

SDI : Transfer in the order of DevAddr, NumOfData, RegAddr, and Data.
SDO : Output the transferred data to the next device after SDI input by 1 byte.



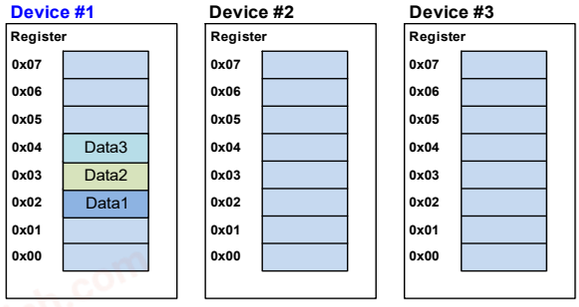


Figure 21. SPI Protocol of the n Byte Write to Device #1

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5. SPI Protocol - continued

(8) All device, different “1 byte” Write (Write the same 1 byte data to the same RegAddr of all Devices)

B:	1	All device receive data
S:	1	Single byte
DevAddr[5:0]:	0x3F	All device different data
NumOfData[6:0]:	-	1 byte Write mode
RW:	0	Write
RegAddr[6:0]:	0x02	Address

SDI : Transfer in the order of DevAddr, RegAddr, and Data.
SDO : Output the transferred data to the next device after SDI input by 1 byte.

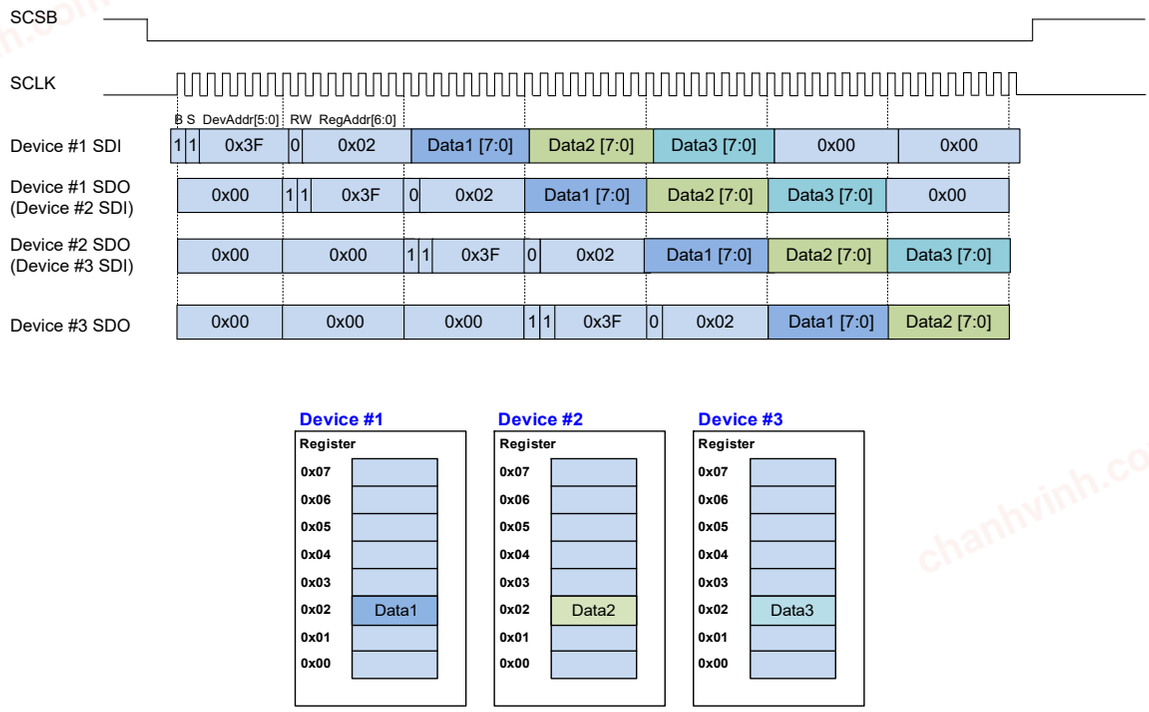


Figure 22. SPI Protocol of the 1 Byte Distinct Data Write to All Devices

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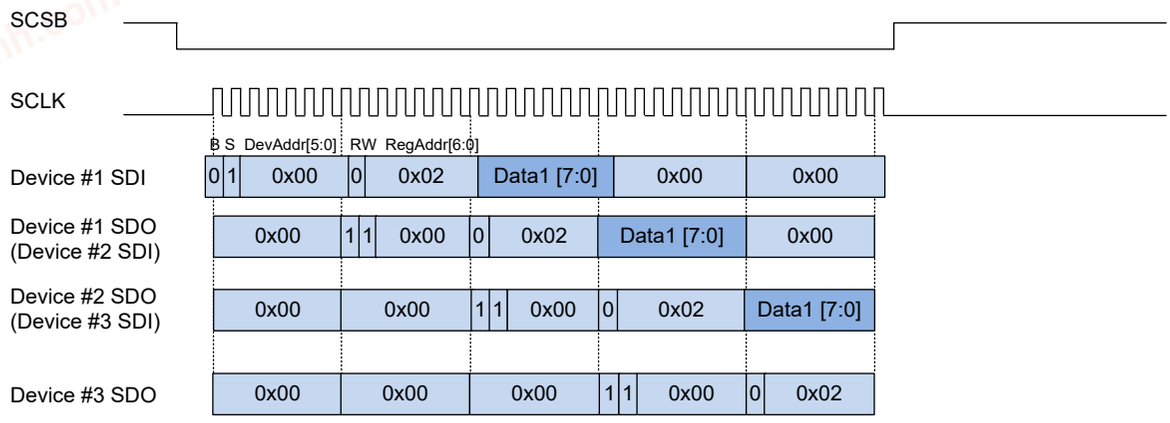
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5. SPI Protocol - continued

(9) All device, same “1 byte” Write (Write the same 1 byte data to the same RegAddr of all Devices)

B:	1	All device receive data
S:	1	Single byte
DevAddr[5:0]:	0x00	All device same data
NumOfData[6:0]:	-	1 byte Write mode
RW:	0	Write
RegAddr[6:0]:	0x02	Address

SDI : Transfer in the order of DevAddr, RegAddr, and Data.
SDO : Output the transferred data to the next device after SDI input by 1 byte.



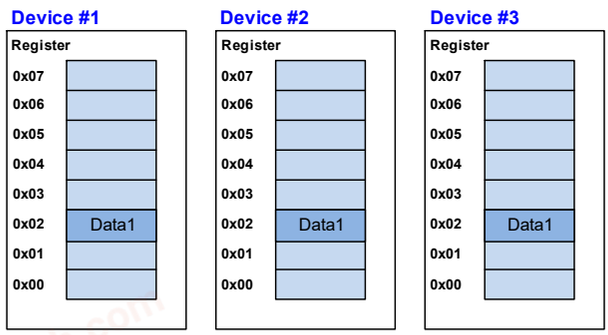


Figure 23. SPI Protocol of the 1 Byte Distinct Data Write to All Devices

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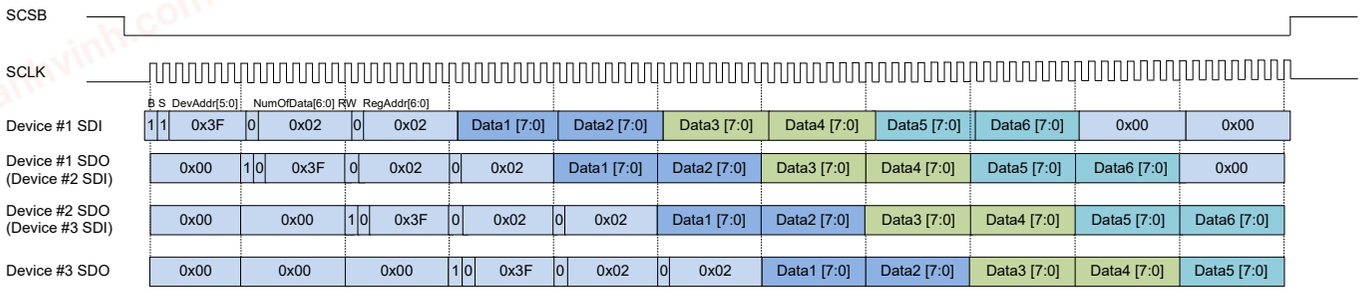
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5. SPI Protocol - continued

(10) All device, different “n byte” Write (Write the different n byte data to the same RegAddr of all Devices)

B:	1	All device receive data
S:	0	multi byte
DevAddr[5:0]:	0x3F	All device different data
NumOfData[6:0]:	0x02	2 byte Write mode
RW:	0	Write
RegAddr[6:0]:	0x02	Address

SDI : Transfer in the order of DevAddr, NumOfData, RegAddr, and Data.
SDO : Output the transferred data to the next device after SDI input by 1 byte.



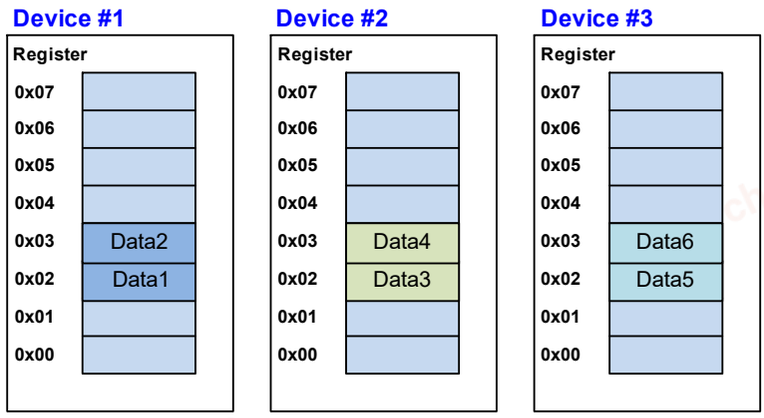


Figure 24. SPI Protocol of the n Byte Distinct Data Write to All Devices

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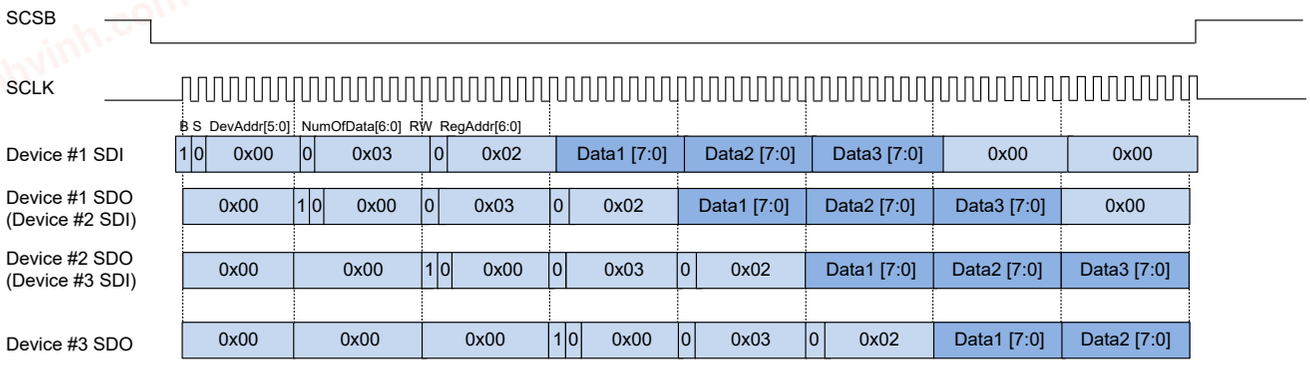
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5. SPI Protocol - continued

(11) All device, same “n byte” Write (Write the same n byte data to the same RegAddr of all Devices)

B:	1	All device receive data
S:	0	multi byte
DevAddr[5:0]:	0x00	All device same data
NumOfData[6:0]:	0x03	3 byte Write mode
RW:	0	Write
RegAddr[6:0]:	0x02	Address

SDI : Transfer in the order of DevAddr, NumOfData, RegAddr, and Data.
SDO : Output the transferred data to the next device after SDI input by 1 byte.



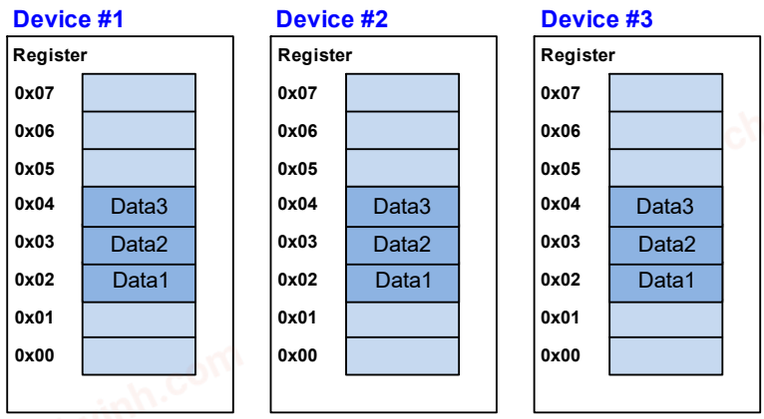


Figure 25. SPI Protocol of the n Byte Same Data Write to All Devices

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5. SPI Protocol - continued

(12) Single device, “1 byte” Read (Read the 1 byte data from Device #2)

B:	0	Target device receive each data
S:	1	single byte
DevAddr[5:0]:	0x02	Target Device Address
NumOfData[6:0]:	-	1 byte Read mode
RW:	1	Read
RegAddr[6:0]:	0x03	Address

SDI : Transfer in the order of DevAddr and RegAddr.
SDO : Output the transferred data to the next device after SDI input by 1 byte.

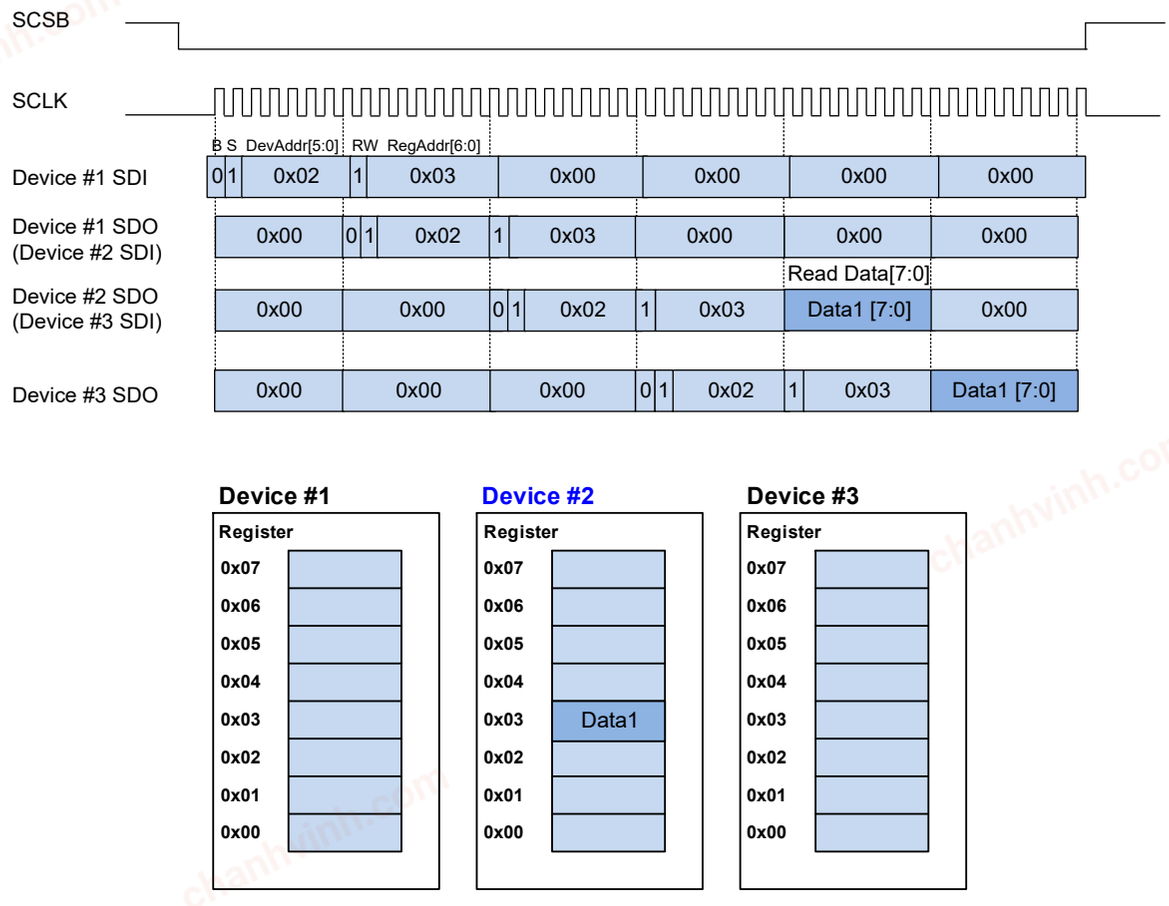


Figure 26. SPI Protocol of the 1 Byte Read from Device #2

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5. SPI Protocol - continued

(13) Single device, “n byte” Read (Read the n byte data from Device #2)

B:	0	Target device receive each data
S:	0	multi byte
DevAddr[5:0]:	0x02	Target Device Address
NumOfData:	0x02	1 byte Read mode
RW:	1	Read
RegAddr[6:0]:	0x03	Address

SDI : Transfer in the order of DevAddr, NumOfData, and RegAddr.
SDO : Output the transferred data to the next device after SDI input by 1 byte.

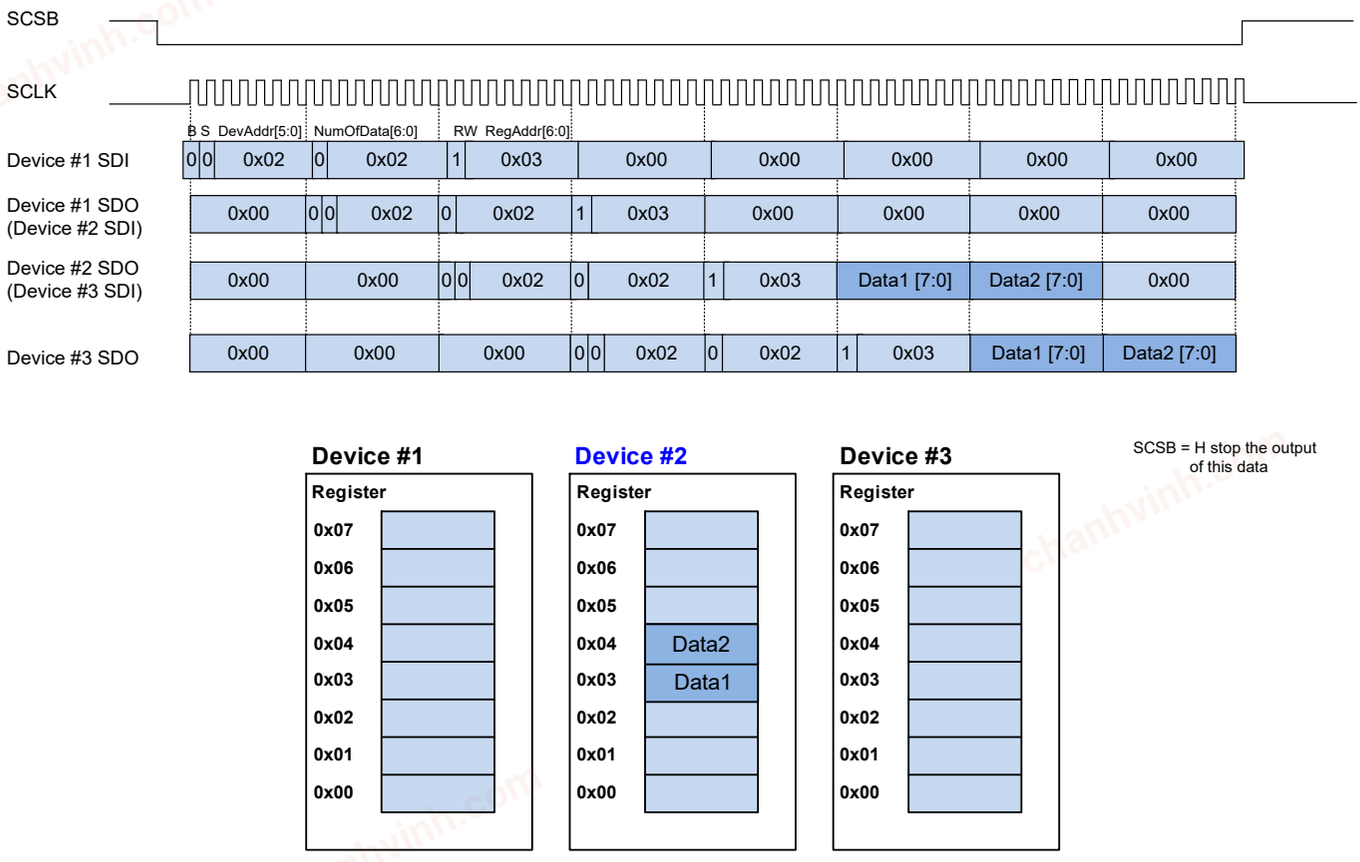


Figure 27. SPI Protocol of the n Byte Read from Device #2

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5. SPI Protocol - continued

(14) Example of n byte Write (Write the n byte data to Device #1 and #2)

Example of the transfer of 2 device Cascade Connection.

Transfer setting	DevAddr	1 byte
	Number of transferred byte	1 byte
	RegAddr	1 byte
Data	Data for the duty setting of Duty	2 byte x 16 channel x 2 device = 64 byte
Dummy clock	for multi device transfer	1 byte
SUM		68 byte

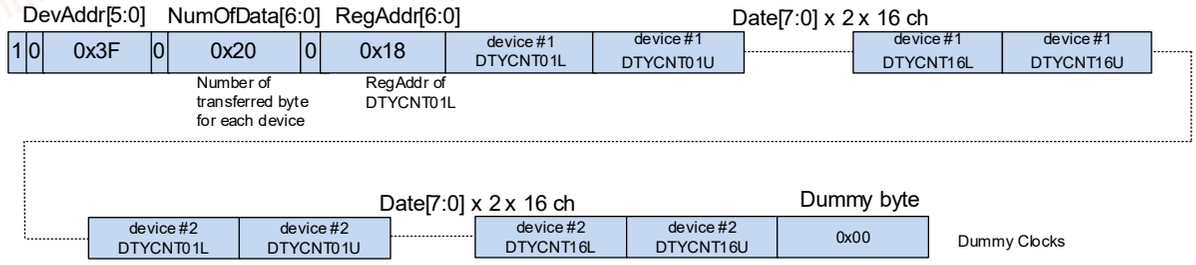


Figure 28. Transfer Byte Number for Multi Access

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Functions of Logic Blocks - continued

6. Register Map

Each registers is updated at the 3 timings.
Provided for Type B and Type C, the registers are not updated when the update timing and SCSB = 'Low' are the same, and wait for the next update timing when SCSB = 'High'.
Reset Condition: "UVLO" condition = VREG33UVLO or VCCUVLO or TSD or EN is detected.

Register Update timing for control data
Type A : Updated to the newest data immediately when the data is written.
Type B : Updated to the newest data when the next VSYNC timing.
(rise-edge trigger) after the data is written.)
Type C : Updated to the newest data when the next VSYNC and PWM (PWM is internal signal) timing.
(rise-edge trigger of VSYNC, then rise-edge trigger of PWM (first PWM pulse when PWMFREQ[1:0] = 01h to 11h) after the data is written.

Note: Don't access (Write) register except for following register and write '0' in '-'.

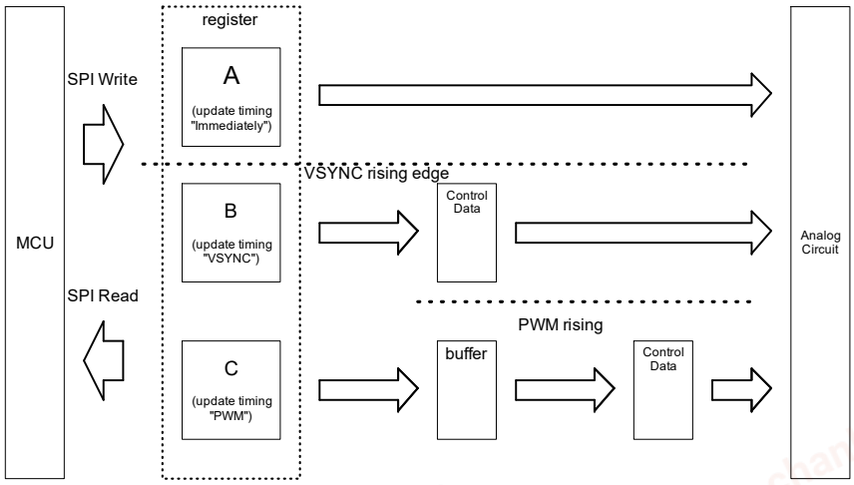


Figure 29. SPI Data Flow

Address 0x01 to 0x16 (1/3)

Register Name	Address	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Register Access	Initial	Reset Condition	Update Timing	Comments
-	0x00	-	-	-	-	-	-	-	-	R/W	0x00	UVLO	Type A	Blank
PWMFREQ	0x01	-	-	-	-	-	-	PWMFREQ[1:0]		R/W	0x00	UVLO	Type A	PWM output frequency setting
ERRSET1	0x02	-	-	SCPTIME[1:0]		LEDSH[3:0]				R/W	0x0F	UVLO	Type A	LED short voltage setting
SSMASK	0x03	SSMASK[7:0]								R/W	0x3C	UVLO	Type B	SS mask time
ERRMASK	0x04	ERRMASK[7:0]								R/W	0x29	UVLO	Type B	error mask time
ERREN	0x05	-	-	-	-	-	TSDWEN	LEDSHEN	LEDOPEN	R/W	0x07	UVLO	Type B	error enable setting
ERRSET2	0x06	FAILTEST	FAILCNT	-	ERRCLR	-	-	-	ERRLAT (Note 1)	R/W	0x00	UVLO	Type A	Error controlling
DLYCNT01	0x07	DLY01[7:0]								R/W	0x00	UVLO	Type B	LED1 PWM Delay setting upper 8bit
DLYCNT02	0x08	DLY02[7:0]								R/W	0x00	UVLO	Type B	LED2 PWM Delay setting upper 8bit
DLYCNT03	0x09	DLY03[7:0]								R/W	0x00	UVLO	Type B	LED3 PWM Delay setting upper 8bit
DLYCNT04	0x0A	DLY04[7:0]								R/W	0x00	UVLO	Type B	LED4 PWM Delay setting upper 8bit
DLYCNT05	0x0B	DLY05[7:0]								R/W	0x00	UVLO	Type B	LED5 PWM Delay setting upper 8bit
DLYCNT06	0x0C	DLY06[7:0]								R/W	0x00	UVLO	Type B	LED6 PWM Delay setting upper 8bit
DLYCNT07	0x0D	DLY07[7:0]								R/W	0x00	UVLO	Type B	LED7 PWM Delay setting upper 8bit
DLYCNT08	0x0E	DLY08[7:0]								R/W	0x00	UVLO	Type B	LED8 PWM Delay setting upper 8bit
DLYCNT09	0x0F	DLY09[7:0]								R/W	0x00	UVLO	Type B	LED9 PWM Delay setting upper 8bit
DLYCNT10	0x10	DLY10[7:0]								R/W	0x00	UVLO	Type B	LED10 PWM Delay setting upper 8bit
DLYCNT11	0x11	DLY11[7:0]								R/W	0x00	UVLO	Type B	LED11 PWM Delay setting upper 8bit
DLYCNT12	0x12	DLY12[7:0]								R/W	0x00	UVLO	Type B	LED12 PWM Delay setting upper 8bit
DLYCNT13	0x13	DLY13[7:0]								R/W	0x00	UVLO	Type B	LED13 PWM Delay setting upper 8bit
DLYCNT14	0x14	DLY14[7:0]								R/W	0x00	UVLO	Type B	LED14 PWM Delay setting upper 8bit
DLYCNT15	0x15	DLY15[7:0]								R/W	0x00	UVLO	Type B	LED15 PWM Delay setting upper 8bit
DLYCNT16	0x16	DLY16[7:0]								R/W	0x00	UVLO	Type B	LED16 PWM Delay setting upper 8bit

(Note) WO: Write Only, RO: Read Only, R/W: Read and Write
(Note 1) Update timing of ERRLAT is Type B.

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6. Register Map – continued
Address 0x17 to 0x47 (2/3)

Register Name	Address	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Register Access	Initial	Reset Condition	Update Timing	Comments
PWMPLS	0x17	-	-	-	PLSSET	-	-	PLSNUM[1:0]		R/W	0x00	UVLO	Type C	PWM pulse number setting
DTYCNT01L	0x18	DTY01[7:0]								R/W	0x00	UVLO	Type C	LED1 PWM ON duty Lower 8bit
DTYCNT01U	0x19	-	-	DTYEN01	DTY01[12:8]					R/W	0x00	UVLO	Type C	LED1 PWM ON duty Upper 5bit
DTYCNT02L	0x1A	DTY02[7:0]								R/W	0x00	UVLO	Type C	LED2 PWM ON duty Lower 8bit
DTYCNT02U	0x1B	-	-	DTYEN02	DTY02[12:8]					R/W	0x00	UVLO	Type C	LED2 PWM ON duty Upper 5bit
DTYCNT03L	0x1C	DTY03[7:0]								R/W	0x00	UVLO	Type C	LED3 PWM ON duty Lower 8bit
DTYCNT03U	0x1D	-	-	DTYEN03	DTY03[12:8]					R/W	0x00	UVLO	Type C	LED3 PWM ON duty Upper 5bit
DTYCNT04L	0x1E	DTY04[7:0]								R/W	0x00	UVLO	Type C	LED4 PWM ON duty Lower 8bit
DTYCNT04U	0x1F	-	-	DTYEN04	DTY04[12:8]					R/W	0x00	UVLO	Type C	LED4 PWM ON duty Upper 5bit
DTYCNT05L	0x20	DTY05[7:0]								R/W	0x00	UVLO	Type C	LED5 PWM ON duty Lower 8bit
DTYCNT05U	0x21	-	-	DTYEN05	DTY05[12:8]					R/W	0x00	UVLO	Type C	LED5 PWM ON duty Upper 5bit
DTYCNT06L	0x22	DTY06[7:0]								R/W	0x00	UVLO	Type C	LED6 PWM ON duty Lower 8bit
DTYCNT06U	0x23	-	-	DTYEN06	DTY06[12:8]					R/W	0x00	UVLO	Type C	LED6 PWM ON duty Upper 5bit
DTYCNT07L	0x24	DTY07[7:0]								R/W	0x00	UVLO	Type C	LED7 PWM ON duty Lower 8bit
DTYCNT07U	0x25	-	-	DTYEN07	DTY07[12:8]					R/W	0x00	UVLO	Type C	LED7 PWM ON duty Upper 5bit
DTYCNT08L	0x26	DTY08[7:0]								R/W	0x00	UVLO	Type C	LED8 PWM ON duty Lower 8bit
DTYCNT08U	0x27	-	-	DTYEN08	DTY08[12:8]					R/W	0x00	UVLO	Type C	LED8 PWM ON duty Upper 5bit
DTYCNT09L	0x28	DTY09[7:0]								R/W	0x00	UVLO	Type C	LED9 PWM ON duty Lower 8bit
DTYCNT09U	0x29	-	-	DTYEN09	DTY09[12:8]					R/W	0x00	UVLO	Type C	LED9 PWM ON duty Upper 5bit
DTYCNT10L	0x2A	DTY10[7:0]								R/W	0x00	UVLO	Type C	LED10 PWM ON duty Lower 8bit
DTYCNT10U	0x2B	-	-	DTYEN10	DTY10[12:8]					R/W	0x00	UVLO	Type C	LED10 PWM ON duty Upper 5bit
DTYCNT11L	0x2C	DTY11[7:0]								R/W	0x00	UVLO	Type C	LED11 PWM ON duty Lower 8bit
DTYCNT11U	0x2D	-	-	DTYEN11	DTY11[12:8]					R/W	0x00	UVLO	Type C	LED11 PWM ON duty Upper 5bit
DTYCNT12L	0x2E	DTY12[7:0]								R/W	0x00	UVLO	Type C	LED12 PWM ON duty Lower 8bit
DTYCNT12U	0x2F	-	-	DTYEN12	DTY12[12:8]					R/W	0x00	UVLO	Type C	LED12 PWM ON duty Upper 5bit
DTYCNT13L	0x30	DTY13[7:0]								R/W	0x00	UVLO	Type C	LED13 PWM ON duty Lower 8bit
DTYCNT13U	0x31	-	-	DTYEN13	DTY13[12:8]					R/W	0x00	UVLO	Type C	LED13 PWM ON duty Upper 5bit
DTYCNT14L	0x32	DTY14[7:0]								R/W	0x00	UVLO	Type C	LED14 PWM ON duty Lower 8bit
DTYCNT14U	0x33	-	-	DTYEN14	DTY14[12:8]					R/W	0x00	UVLO	Type C	LED14 PWM ON duty Upper 5bit
DTYCNT15L	0x34	DTY15[7:0]								R/W	0x00	UVLO	Type C	LED15 PWM ON duty Lower 8bit
DTYCNT15U	0x35	-	-	DTYEN15	DTY15[12:8]					R/W	0x00	UVLO	Type C	LED15 PWM ON duty Upper 5bit
DTYCNT16L	0x36	DTY16[7:0]								R/W	0x00	UVLO	Type C	LED16 PWM ON duty Lower 8bit
DTYCNT16U	0x37	-	-	DTYEN16	DTY16[12:8]					R/W	0x00	UVLO	Type C	LED16 PWM ON duty Upper 5bit
LCDAC1	0x38	LCDAC1[7:0]								R/W	0xFF	UVLO	Type C	LED1 local DAC setting
LCDAC2	0x39	LCDAC2[7:0]								R/W	0xFF	UVLO	Type C	LED2 local DAC setting
LCDAC3	0x3A	LCDAC3[7:0]								R/W	0xFF	UVLO	Type C	LED3 local DAC setting
LCDAC4	0x3B	LCDAC4[7:0]								R/W	0xFF	UVLO	Type C	LED4 local DAC setting
LCDAC5	0x3C	LCDAC5[7:0]								R/W	0xFF	UVLO	Type C	LED5 local DAC setting
LCDAC6	0x3D	LCDAC6[7:0]								R/W	0xFF	UVLO	Type C	LED6 local DAC setting
LCDAC7	0x3E	LCDAC7[7:0]								R/W	0xFF	UVLO	Type C	LED7 local DAC setting
LCDAC8	0x3F	LCDAC8[7:0]								R/W	0xFF	UVLO	Type C	LED8 local DAC setting
LCDAC9	0x40	LCDAC9[7:0]								R/W	0xFF	UVLO	Type C	LED9 local DAC setting
LCDAC10	0x41	LCDAC10[7:0]								R/W	0xFF	UVLO	Type C	LED10 local DAC setting
LCDAC11	0x42	LCDAC11[7:0]								R/W	0xFF	UVLO	Type C	LED11 local DAC setting
LCDAC12	0x43	LCDAC12[7:0]								R/W	0xFF	UVLO	Type C	LED12 local DAC setting
LCDAC13	0x44	LCDAC13[7:0]								R/W	0xFF	UVLO	Type C	LED13 local DAC setting
LCDAC14	0x45	LCDAC14[7:0]								R/W	0xFF	UVLO	Type C	LED14 local DAC setting
LCDAC15	0x46	LCDAC15[7:0]								R/W	0xFF	UVLO	Type C	LED15 local DAC setting
LCDAC16	0x47	LCDAC16[7:0]								R/W	0xFF	UVLO	Type C	LED16 local DAC setting

(Note) WO: Write Only, RO: Read Only, R/W: Read and Write

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6. Register Map - continued
Address 0x48 to 0x4F (3/3)

Register Name	Address	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Register Access	Initial	Reset Condition	Update Timing	Comments
-	0x48	-	-	-	-	-	-	-	-	-	-	-	-	blank
ERRLEDOPA	0x49	ERLOP[7:0] (Note 2)								RO	0x00	UVLO	Type A	error flag LEDn open (n = 1 to 8)
ERRLEDOPB	0x4A	ERLOP[15:8] (Note 2)								RO	0x00	UVLO	Type A	error flag LEDn open (n = 9 to 16)
ERRLEDSHA	0x4B	ERLSH[7:0] (Note 2)								RO	0x00	UVLO	Type A	error flag LEDn short (n = 1 to 8)
ERRLEDSHB	0x4C	ERLSH[15:8] (Note 2)								RO	0x00	UVLO	Type A	error flag LEDn short (n = 9 to 16)
ERRISETSCP	0x4D	-	-	-	-	-	-	WARSCP (Note 3)	WARISET (Note 2)	RO	0x00	UVLO	Type A	error flag ISET short and SCP
ERRTSDA	0x4E	WARTSD[7:0] (Note 2)								RO	0x00	UVLO	Type A	error flag TSD warning (n = 1 to 8)
ERRTSDB	0x4F	WARTSD[15:8] (Note 2)								RO	0x00	UVLO	Type A	error flag TSD warning (n = 9 to 16)

(Note) WO: Write Only, RO: Read Only, R/W: Read and Write
(Note 2) Released condition is referred in description of register.
(Note 3) Released condition is only reset.

7. Description of Registers

Address 0x01: PWMFREQ Output PWM frequency setting [Read/Write] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	-	-	-	-	PWMFREQ[1:0]	
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

Regarding EXTCLK frequency, refer to the following list.
If it is different from relation of PWMFREQ and EXTCLK frequency, it can't control LED normally.
Don't change value during dimming. (only initial setting before PWM setting)

PWMFREQ[1:0]	PWM Frequency	EXTCLK Frequency
0	VSYNC x 1	VSYNC x 8,192
1	VSYNC x 2	VSYNC x 16,384
2	VSYNC x 4	VSYNC x 32,768
3	VSYNC x 8	VSYNC x 65,536

Example of EXTCLK setting is referred. This IC can be acceptable to input EXTCLK under 5 MHz.
(Refer to frequency range of electric characteristics)

(Example) EXTCLK frequency and PWM frequency

PWMFREQ[1:0]	VSYNC Frequency [Hz]			
	60	120	240	480
0	491,520	983,040	1,966,080	3,932,160
	60	120	240	480
1	983,040	1,966,080	3,932,160	-
	120	240	480	-
2	1,966,080	3,932,160	-	-
	240	480	-	-
3	3,932,160	-	-	-
	480	-	-	-

[Hz]

Upper: EXTCLK frequency
Lower: PWM frequency

'-' is not acceptable to set this value in PWMFREQ register.

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7. Description of Registers - continued

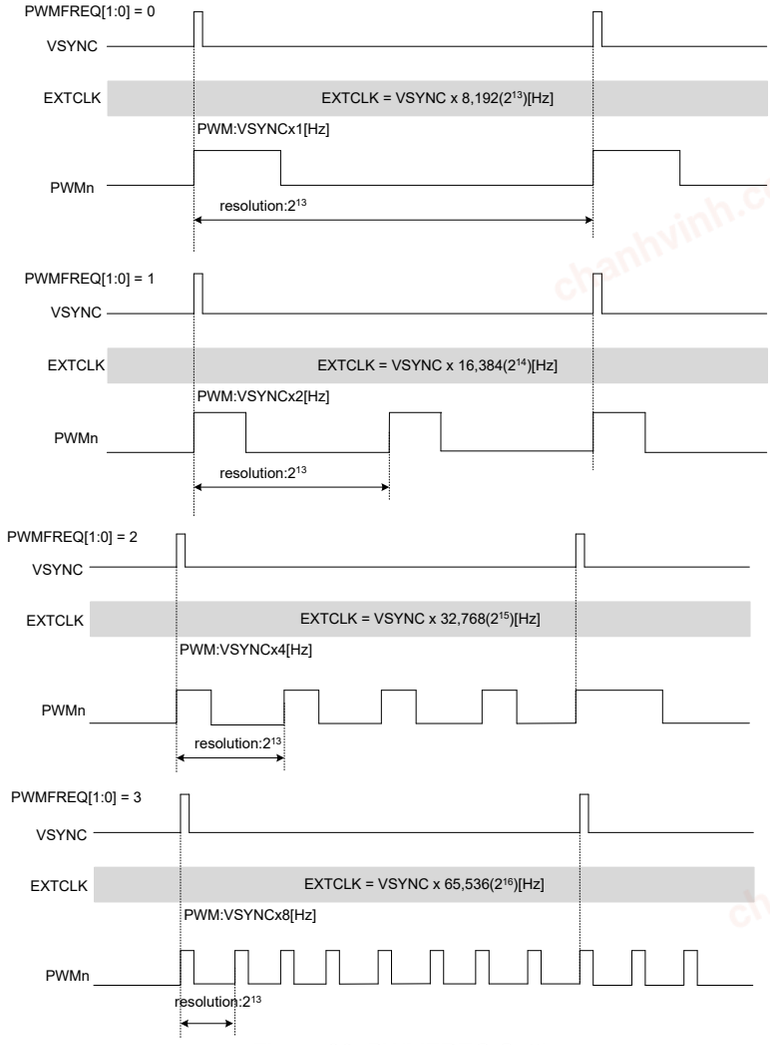


Figure 30. PWMFREQ Setting

Address 0x02: ERRSET1 LED short detection voltage setting [Read/Write] Initial value 0x0F

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	SCPTIME[1:0]		LEDSH[3:0]			
Initial value	0	0	0	0	1	1	1	1

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

Bit[5:4] SCPTIME

This register controls MASK time for SCP detected.

SCPTIME[1:0]	MASK Time
0	1 VSYNC cycle
1	2 VSYNC cycle
2	4 VSYNC cycle
3	8 VSYNC cycle

Bit[3:0] LEDSH[3:0]

This register controls detection voltage LED short protection.

LEDSH[3:0]	Detection Voltage [V]
0x0 to 0x8	Not available
0x9	3.00
0xA	3.30
0xB	3.60
0xC	3.90
0xD	4.20
0xE	4.50
0xF	4.80

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7. Description of Registers – continued

Address 0x03: SSMASK Soft start mask register [Read/Write] Initial value 0x3C

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	SSMASK[7:0]							
Initial value	0	0	1	1	1	1	0	0

Update: VSYNC

The register data is updated to the newest data when the next VSYNC signal rises up after the data is written.
Set value more than 0x02.

It controls protect function (LED open protection, LED short protection, SCP, ISET short warning, TSD warning) after SSMASK time. So, it is not available to operate protection function during SSMASK time.

The time of mask of ERROR detection is set by counting the number of VSYNC.

Time of mask = SSMASK x VSYNC
(except for waiting time until 1st VSYNC pulse)

VSYNC [Hz]	60	120	240	480
Max Mask time [ms]	4,250	2,125	1,062.5	531.3

Address 0x04: ERRMASK ERROR output mask time setting register [Read/Write] Initial value 0x29

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERRMASK[7:0]							
Initial value	0	0	1	0	1	0	0	1

Update: VSYNC

The register data is updated to the newest data when the next VSYNC signal rises up after the data is written.

When 0 to 2 is written to this register, the register value becomes 3.
When over 3 is written to this register, writing value becomes register value.

This IC has mask function for “LED open protection” and “LED short protection”. It can’t detect these errors during this time.

ERROR mask time is set by counting the number of EXTCLK.

Mask time = ERRMASK x EXTCLK
Example) ERRMASK = 3: mask 3 clock to 4 clock (PWM = H and error signal (after synchronizing))

‘-’ column is not acceptable setting.

VSYNC/EXTCLK condition vs “Maximum Mask time” (Default 0x29 (41))

PWMFREQ[1:0]	VSYNC [Hz]			
	60	120	240	480
0	519	259	130	65
1	259	130	65	-
2	130	65	-	-
3	65	-	-	-

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7. Description of Registers – continued

Address 0x05: ERREN Error enable setting [Read/Write] Initial value 0x07

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	-	-	-	TSDWEN	LEDSHEN	LEDOPEN
Initial value	0	0	0	0	0	1	1	1

Update: VSYNC

This register is updated to the newest data when the next VSYNC signal rises up after the data is written.

Bit[2]: TSDWEN
0: disable (error register and error output (FAIL) is initial condition if “TSD warning” is occurred
1: enable (135 deg (Typ))

Bit[1] LEDSHEN
0: disable (error register and error output (FAIL) is initial condition if “LED short protection” is occurred
1: enable

Bit[0] LEDOPEN
0: disable (error register and error output (FAIL) is initial condition if “LED open protection” is occurred
1: enable

“LED open function” effects SCP detection. So, it is not available to change this enable during operation.

Address 0x06: ERRSET2 Error Latch mode setting [Read/Write] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	FAILTEST	FAILCNT	-	ERRCLR	-	-		ERRLAT
Initial value	0	0	0	0	0	0	0	0

Update: FAILTEST, FAILCNT, ERRCLR: Immediately, ERRLAT: VSYNC

The data (ERRCLR) in register is updated to the newest data immediately when the new data is written.
The register data (ERRLAT) is updated to the newest data when the next VSYNC signal rises up after the data is written.

Bit[7] FAILTEST
0: normal operation
1: It available to control the FAIL pin output by FAILCNT register.

Bit[4] FAILCNT
0: It outputs Low from the FAIL pin when FAILTEST = 1
1: It outputs High from the FAIL pin when FAILTEST = 1

Bit[4] ERRCLR
0: no operation
1: clear error register and return Hi-Z in FAIL output when ERRLAT = 1
ERRCLR return ‘0’ automatically. So, it can’t read ‘1’.

Bit[0] ERRLAT
0: error register and FAIL output are returned to initial condition when error is released.
1: error register and FAIL output are kept until writing ‘1’ in ERRCLR.

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7. Description of Registers - continued

Address 0x07: DLYCNT01 (LED1 PWM Delay setting register) [Read/Write] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	DLY01[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: VSYNC

The register data is updated to the newest data when the next VSYNC signal rises up after the data is written.

This register is used to make setting of delay width for PWM light modulation in a total of 8 bits, i.e., Bit[7:0] when Address = 0x07.

DLY01[7:0]	LED Delay Width (clock width@EXTCLK)			
	PWMFREQ[1:0] = 0	PWMFREQ[1:0] = 1	PWMFREQ[1:0] = 2	PWMFREQ[1:0] = 3
0x00	4 clock to 5 clock width@EXTCLK from posedge of VSYNC (*)			
0x01	(*) + 0x01 x 2^5	(*) + 0x01 x 2^6	(*) + 0x01 x 2^7	(*) + 0x01 x 2^8
0x02	(*) + 0x02 x 2^5	(*) + 0x02 x 2^6	(*) + 0x02 x 2^7	(*) + 0x02 x 2^8
0x03	(*) + 0x03 x 2^5	(*) + 0x03 x 2^6	(*) + 0x03 x 2^7	(*) + 0x03 x 2^8
…	…	…	…	…
0xXX	(*) + 0xXX x 2^5	(*) + 0xXX x 2^6	(*) + 0xXX x 2^7	(*) + 0xXX x 2^8
…	…	…	…	…
0xFC	(*) + 0xFC x 2^5	(*) + 0xFC x 2^6	(*) + 0xFC x 2^7	(*) + 0xFC x 2^8
0xFD	(*) + 0xFD x 2^5	(*) + 0xFD x 2^6	(*) + 0xFD x 2^7	(*) + 0xFD x 2^8
0xFE	(*) + 0xFE x 2^5	(*) + 0xFE x 2^6	(*) + 0xFE x 2^7	(*) + 0xFE x 2^8
0xFF	(*) + 0xFF x 2^5	(*) + 0xFF x 2^6	(*) + 0xFF x 2^7	(*) + 0xFF x 2^8

Decide “DLY01 setting” in VSYNC and EXTCLK jitter of MCU. Refer to “PWM behavior at close VSYNC interval”.

Address 0x08 to 0x16: DLYCNTn (n = 2 to 16)
This register is used to make PWM delay width setting for LED2 to LED16. The setting procedure is the same as that for LED1 with Address set to 0x07.

The register data is updated to the newest data when the next VSYNC signal rises up after the data is written.

Address 0x17: PWMPLS (PWM pulse number setting) [Read/Write] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	-	PLSSET	-	-	PLSNUM[1:0]	
Initial value	0	0	0	0	0	0	0	0

Update: PWM

The register data is updated to the newest data when the next PWM signal rises up after the data is written.

PWMFREQ[1:0]	PLSNUM (PWM pulse number)			
	0	1	2	3
0	1			
1	2		1	
2	4	3	2	1
3	8	6	4	2

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7. Description of Registers - continued

It outputs PWM pulse in Head position When PLSSET = 0
Example) PWMFREQ[1:0] = 3, PLSSET = 0

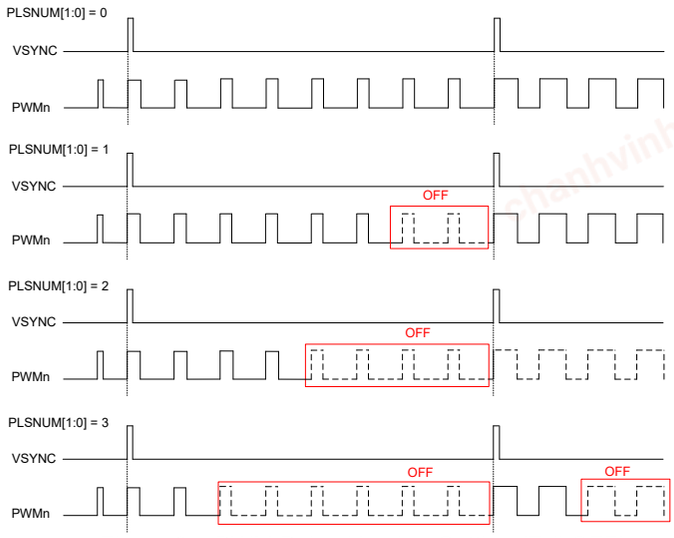


Figure 31. PWM Pulse Number Setting (Tail OFF)

It outputs PWM pulse in Tail position When PLSSET = 1.
Example) PWMFREQ[1:0] = 3, PLSSET = 1

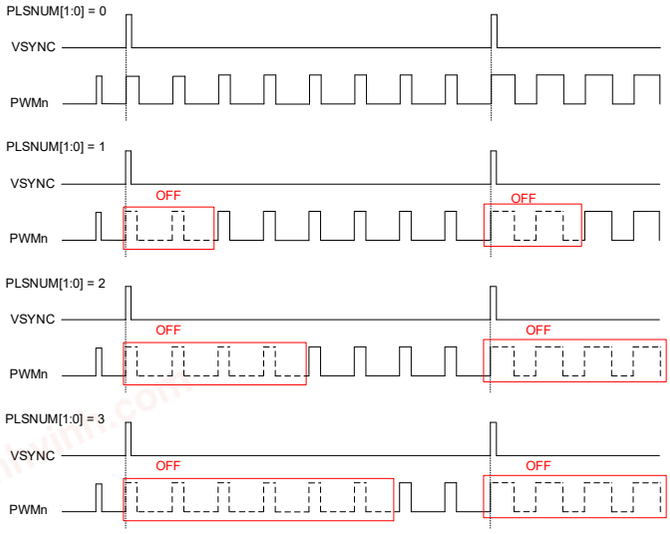


Figure 32. PWM Pulse Number Setting (Head OFF)

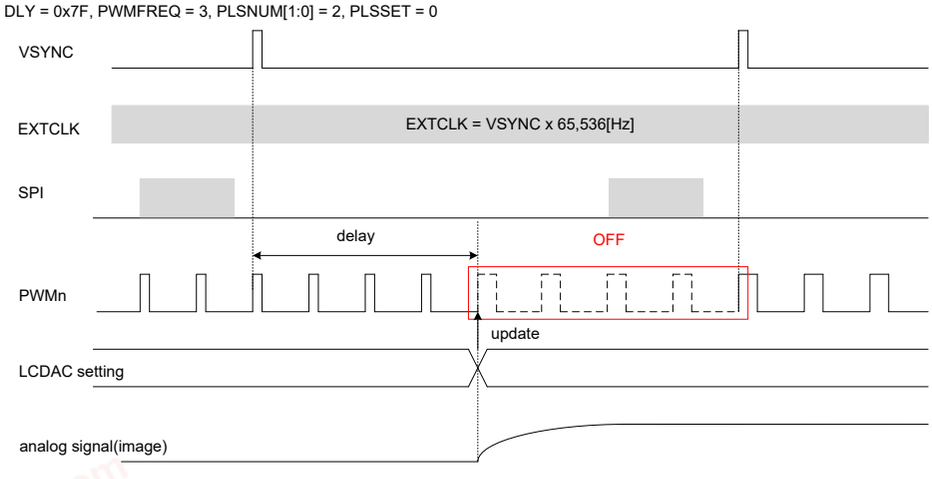


Figure 33. PWM Pulse Number Setting

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7. Description of Registers - continued

Address 0x18: DTYCNT01L (LED1 PWM duty setting register - lower 8 bits) [Read/Write] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	DTY01[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: PWM

The register data is updated to the newest data when the next PWM signal rises up after the data is written.

Address 0x19: DTYCNT01U (LED1 PWM duty setting register - upper 5 bits) [Read/Write] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	DTYEN01	DTY01[12:8]				
Initial value	0	0	0	0	0	0	0	0

Update: PWM

The register data is updated to the newest data when the next PWM signal rises up after the data is written.

This register is used to make setting of pulse duty for PWM light modulation in a total of 13 bits, i.e., Bit[7:0] when Address = 0x18 and Bit[4:0] when Address = 0x19.

DTYEN01	DTY01[12:0]	LED Pulse Width
0	0x000 to 0x1FFF	0 clock width@EXTCLK
1	0x0000	1 clock width@EXTCLK
1	0x0001	2 clock width@EXTCLK
1	0x0002	3 clock width@EXTCLK
1	0x0003	4 clock width@EXTCLK
1	...	...
1	0x1FFC	8189 clock width@EXTCLK
1	0x1FFD	8190 clock width@EXTCLK
1	0x1FFE	8191 clock width@EXTCLK
1	0x1FFF	Normally set to High (Duty 100 %)

If DTYEN01 = 0 is set when it detects LED open/LED short in channel 1, Error register (ERLOP[0]/ERLSH[0]) and FAIL turn normal condition.

Address 0x1A to 0x37: DTYCNTn (n = 2 to 16)
This register is used to make setting of PWM pulse width for LED2 to LED16. The setting procedure is the same as that for LED1 with Address set to 0x1A and 0x37.

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7. Description of Registers - continued

Address 0x38: LCDAC1 (Analog light modulation setting for LED1) [Read/Write] Initial value 0xFF

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	LCDAC1[7:0]							
Initial value	1	1	1	1	1	1	1	1

Update: PWM

The register data is updated to the newest data when the next PWM signal rises up after the data is written.

Address 0x39 to 0x47: LCDACn (n = 2 to 16)
This register is used to make setting of PWM pulse width for LED2 to LED16. The setting procedure is the same as that for LED1 with Address set to 0x38.

This register can be written 0x00 to 0xFF value.
The DAC setting is possible, but the guarantee levels become more than 20 mA.

LCDACn[7:0] (Write value)	I_{LEDn}
0x00	I_{LEDMAX} x 1/256
0x01	I_{LEDMAX} x 2/256
…	…
0xXX	I_{LEDMAX} x (LCDACn +1)/256
…	…
0xFF	I_{LEDMAX} x 256/256

(n = 1 to 16)

$$I_{LEDMAX} = 757/R_{ISET} \quad [A]$$

$$I_{LEDn} = I_{LEDMAX} \times \{(LCDACn[7:0] + 1)/256\} > 0.02 \quad [A] \quad (n = 1\ to\ 16)$$

$$I_{LEDn_AVE} = I_{LEDn} \times \{(DTYn[12:0] + 1)/ 8{,}192\} \quad [A] \quad (n = 1\ to\ 16)$$

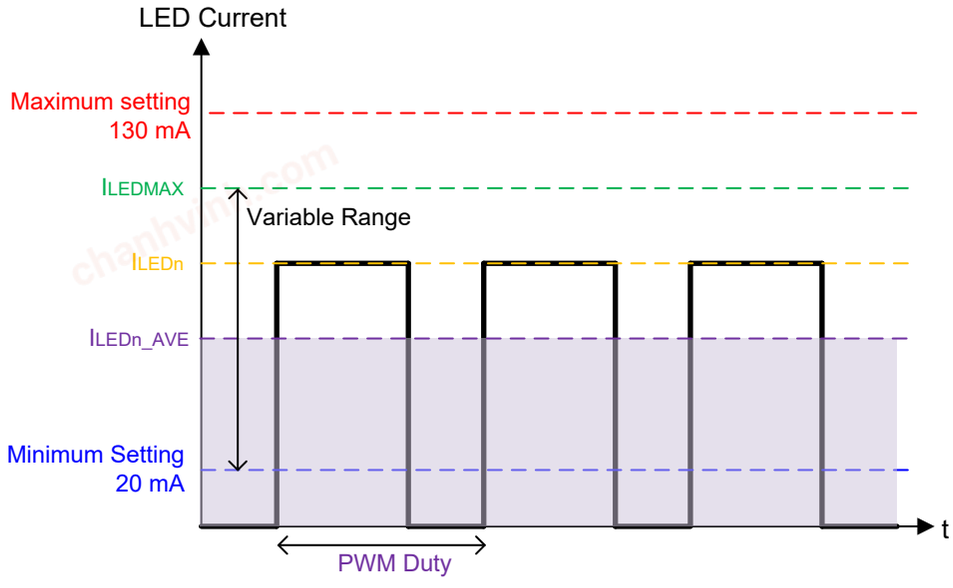


Figure 34. Current Setting Image

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7. Description of Registers - continued

Address 0x49: ERRLEDOPA (LED1 to LED8 pin open ERROR monitor) [Read] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLOP[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The register data is updated to the newest data immediately when the data (“LED open protection”) is detected.

Address 0x4A: ERRLEDOPB (LED8 to LED16 pin open ERROR monitor) [Read] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLOP[15:8]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The register data is updated to the newest data immediately when the data (“LED open protection”) is detected.

ERLOP[n-1]	Status
0	Normal
1	Detect protection *(Note 1)*

(n = 1 to 16 channel)

(Note 1) ERRLAT = 0: ERLOP[n-1] turns 0, if Error is released or “DTYENn = 0” is set or “LEDOPEN = 0” is set.
ERRLAT = 1: ERLOP[n-1] turns 0, if “ERRCLR = 1” is set.

Address 0x4B: ERRLEDSHA (LED1 to LED8 short ERROR monitor) [Read] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSH[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The register data is updated to the newest data immediately when the data (“LED short protection”) is detected.

Address 0x4C: ERRLEDSHB (LED8 to LED16 short ERROR monitor) [Read] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSH[15:8]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The register data is updated to the newest data immediately when the data (“LED short protection”) is detected.

ERLSH[n-1]	Status
0	Normal
1	Detect protection *(Note 2)*

(n = 1 to 16 channel)

(Note 2) ERRLAT = 0: ERLSH[n-1] turns 0, if Error is released or “DTYENn = 0” is set or “LEDSHEN = 0” is set.
ERRLAT = 1: ERLSH[n-1] turns 0, if “ERRCLR = 1” is set.

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7. Description of Registers - continued

Address 0x4D: ERRISETSCP (ISET short warning and SCP) [Read] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	-	-	-	-	WARSCP	WARISET
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

Bit[1]
The register data is updated to the newest data immediately when the data (“SCP”) are detected.

WARSCP	Status
0	Normal
1	Detect SCP*(Note 1)*

(Note 1) WARSCP turns 0 by only reset. It operates SCP circuit using “LED open circuit”.
Don’t change LEDOPEN = 0.

Bit[0]
The register data is updated to the newest data immediately when the data (“ISET short warning”) are detected.

WARISET	Status
0	Normal
1	Detect ISET short (ISET resistor is under 2.5 kΩ)*(Note 2)*

(Note 2) ERRLAT = 0: WARISET turns 0, if Error is released.
ERRLAT = 1: WARISET turns 0, if “ERRCLR = 1” is set.

Address 0x4E: ERRTSDA (TSD warning) [Read] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	WARTSD[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The register data is updated to the newest data immediately when the data (“TSD warning”) are detected.

Address 0x4F: ERRTSDB (TSD warning) [Read] Initial value 0x00

Bit No	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	WARTSD[15:8]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The register data is updated to the newest data immediately when the data (“TSD warning”) are detected.

WARTSD[n-1]	Status
0	Normal
1	Detect protection*(Note 3)*

(n = 1 to 16 channel)

(Note 3) ERRLAT = 0: WARTSD[n-1] turns 0, if Error is released or “TSDWEN = 0” is set.
ERRLAT = 1: WARTSD[n-1] turns 0, if “ERRCLR = 1” is set.

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Timing Chart

1. PWM Delay and ON Duty Setting Procedure Each Dimming Mode

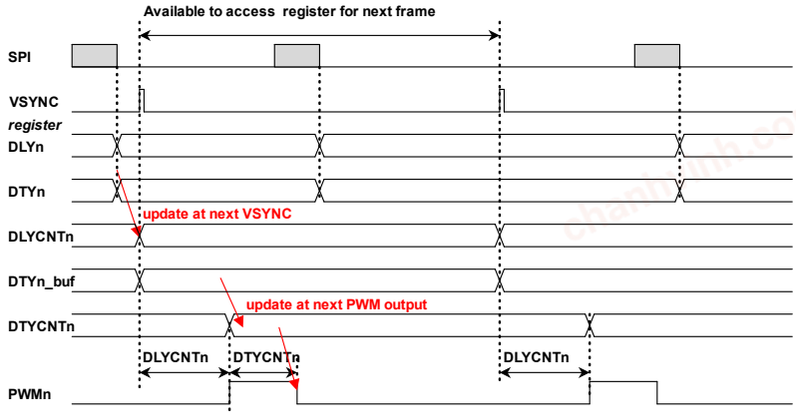


Figure 35. Head Control(PWMFREQ[1:0] = 0)

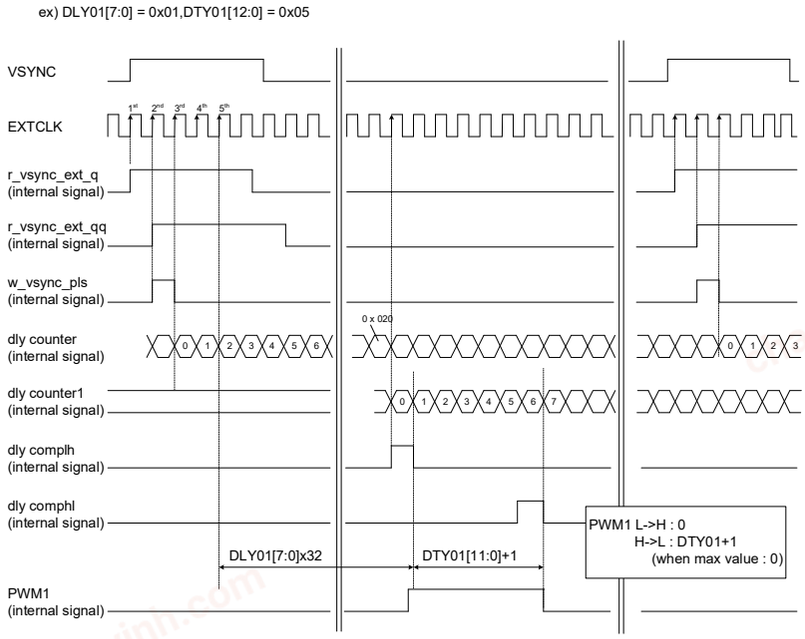


Figure 36. Setting for PWM Delay and ON Duty for Head Control

By making register setting, PWM output delay and ON duty time counts of LED1 to LED16 can be controlled.
The above timing chart shows an example for LED1.
(Example) To make delay time count setting, write “delay time” in Address 0x07.
To make ON duty time count setting, write “duty time” in Address 0x18 and 0x19.

The delay counter starts counting after 4 to 5 EXTCLKs from the rise-edge of VSYNC signal due to internal signal’s timing.
When the counter reaches the set delay value (0x07), the duty counter starts counting, also PWM1 signal is set to ‘High’.
Subsequently, when the duty counter reaches the set duty value (0x18 and 0x19), PWM1 signal is set to ‘Low’.
The sequence is continuously repeated. The procedure for LED2 to LED16 is the same as LED1.
It can set delay of 256 resolution of VSYNC period.

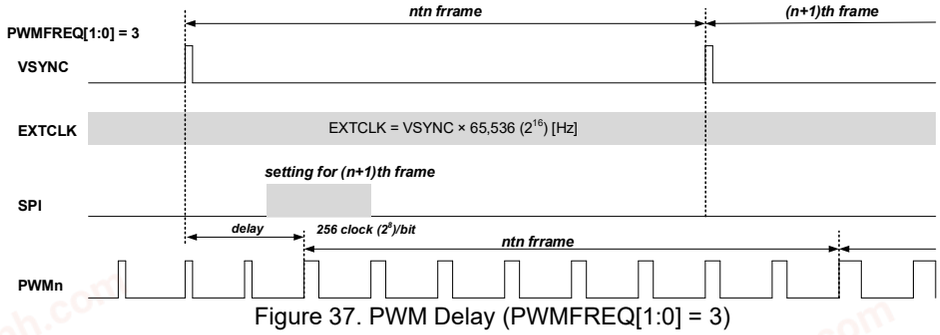


Figure 37. PWM Delay (PWMFREQ[1:0] = 3)

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Timing Chart - continued

2. PWM Behavior at Close VSYNC Interval

Basically, the frequency of EXTCLK pulse is 8,192(PWMFREQ[1:0] = 0) times of that of VSYNC.
Close-interval VSYNC up to 8,192 can make the stick to 'High'/'Low' of PWM signals.
Example of PWM behavior for LED1 is shown as follows.

(1) Stick to High of PWM

Example: Delay = 0, Duty = 75 %

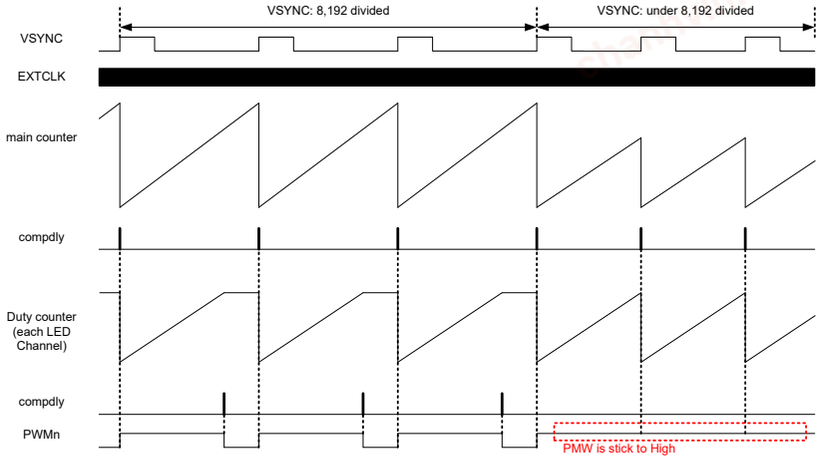


Figure 38. Waveform Function when PWM is Fixed to High

PWM is sets to 'High' at the trigger of compdly (internal signal that shows the arrival of Delay set value) = 'High', also is set to 'Low' at the trigger of compdty (internal signal that shows the arrival of Duty set value) = 'Low'.
"Main counter" is reset and starts counting up at the rise-edge of VSYNC. If it counts up until 8,191, it keeps 8,191 until VSYNC pulse.
"duty counter" is reset and starts counting up at trigger of compdly. If trigger of compdty is generated, it keeps counter value until next trigger of compdly.

For this example, compdly just after the rise-edge of VSYNC sets PWM = 'High' because Delay = 0 %.
"Duty counter" is reset and starts counting up at the pulse of compdly. For this example, as long as VSYNC is divided by 8,192 EXTCLK, PWM is set to 'Low' at the trigger of compdty after the arrival of Duty set value. While, If VSYNC is less than 8,192 EXTCLK, PWM is stick to 'High'. Because the counter is reset since VSYNC is input before the arrival of Duty set value, and the trigger compdty to set PWM to 'Low' is not provided.

(2) Stick to Low of PWM

Example: Delay = 75 %, Duty = 50 %

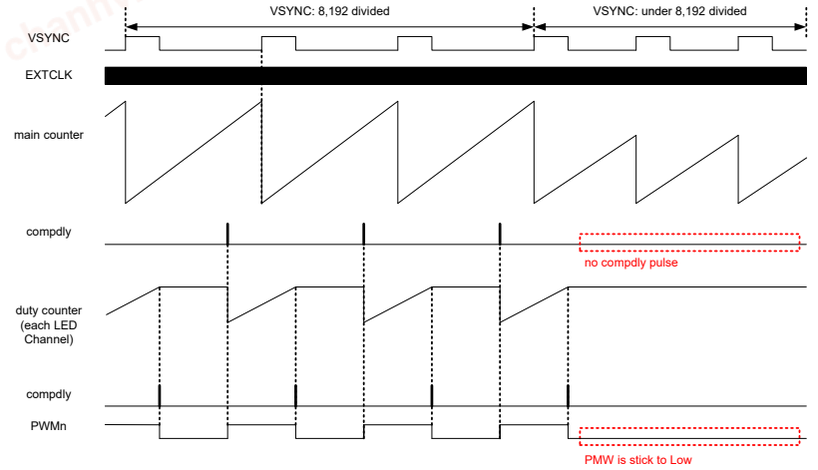


Figure 39. Waveform Function when PWM is Fixed to Low

When the setting of Delay is not 0, PWM is also set to 'High' at the trigger of compdly and is set to L at the trigger of compdty. When VSYNC is divided by up to 8,192 EXTCLK, PWM is also set to L after the arrival of Duty set value. But when the interval of VSYNC is less than the setting of Delay, PWM is stick to 'Low'. Because the counter is reset since VSYNC is input before the arrival of Delay set value, and the trigger compdly to set PWM to 'High' is not provided.

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2. PWM Behavior at Close VSYNC Interval - continued

(3) Lower PWM duty

Example: Delay = 0, Duty = 75 %

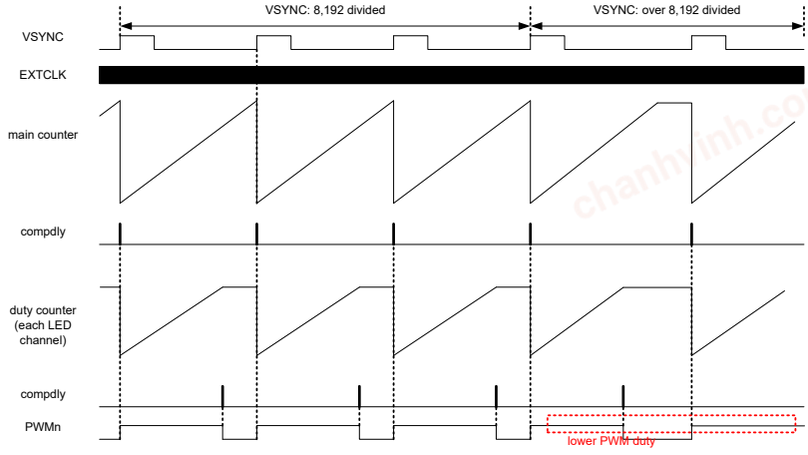


Figure 40. Waveform Function when PWM Duty is Low

For this example, compdly just after the rise-edge of VSYNC sets PWM = ‘High’ because Delay = 0 %.
“Duty counter” is reset and starts counting up at the pulse of compdly. For this example, If VSYNC is more than 8,192 EXTCLK, PWM is set to ‘Low’ at the trigger of compdty after the arrival of Duty set value. Counter keep 8,191 after count = 8,191 until next rise-edge of VSYNC. So PWM is lower than target duty in this case.

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Timing Chart - continued

3. ERROR Control

There are the following internal signals on timing chart:

PWM_OH[n-1] (n = 1 to 16)	PWM signal for LEDn (high: LED ON, low: LED OFF)
LOPDET_ID[n-1] (n = 1 to 16)	LED open error signal (low: error)
LSPDET_ID[n-1] (n = 1 to 16)	LED short error signal (low: error)
WARTSD_ID[n-1] (n = 1 to 16)	TSD warning signal (low: error)
WARISET_IL	ISET short warning (low: error)
SSEND	Soft start mask signal (low: mask)
r_lopdet, r_lspdet, r_vsync	retiming signal
r_wartsd, r_wariset	retiming signal
err_mskcnt	error mask counter

Timing chart of each ERROR detection is as follows

(1) LED Short Protection

It operates as following when it detects (The LED pin voltage is over setting value) or released “LED short Error“.
(Example) Register setting: DLY02[7:0] = 0x00, ERRMASK[7:0] = 0x03, ERRLAT = 0

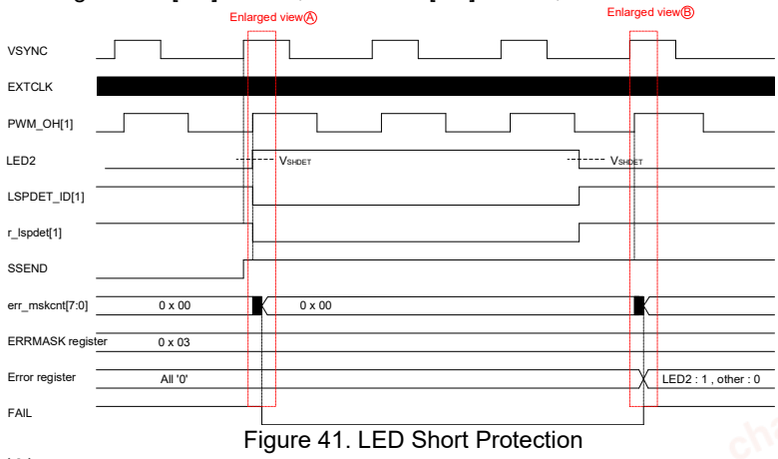


Figure 41. LED Short Protection

(a) Enlarged chart (A)

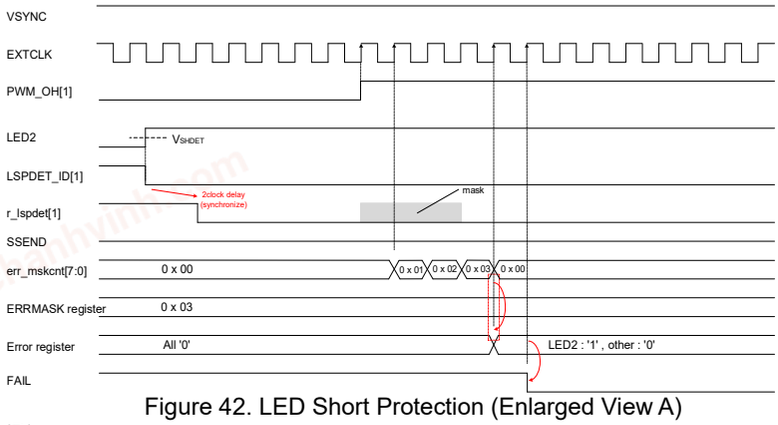


Figure 42. LED Short Protection (Enlarged View A)

(b) Enlarged chart (B)

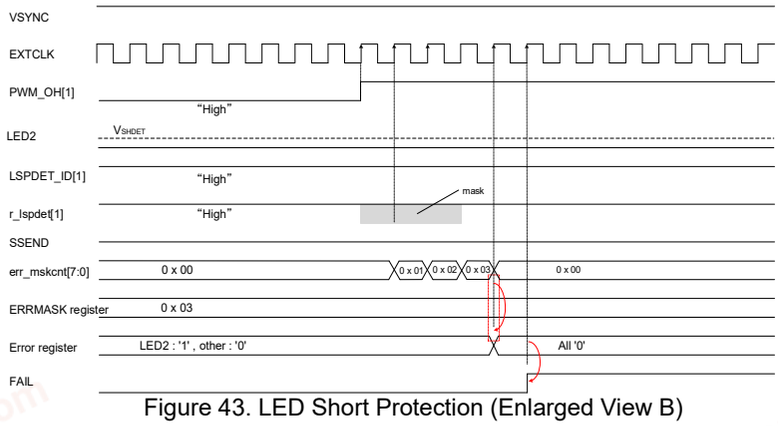


Figure 43. LED Short Protection (Enlarged View B)

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3. ERROR Control – continued

(2) LED Open Protection

It operates as following when it detects (The LED pin voltage is under 0.2 V) or released “LED open Error“.
(Example) Register setting: DLY02[7:0] = 0x00, ERRMASK[7:0] = 0x03, ERRLAT = 0

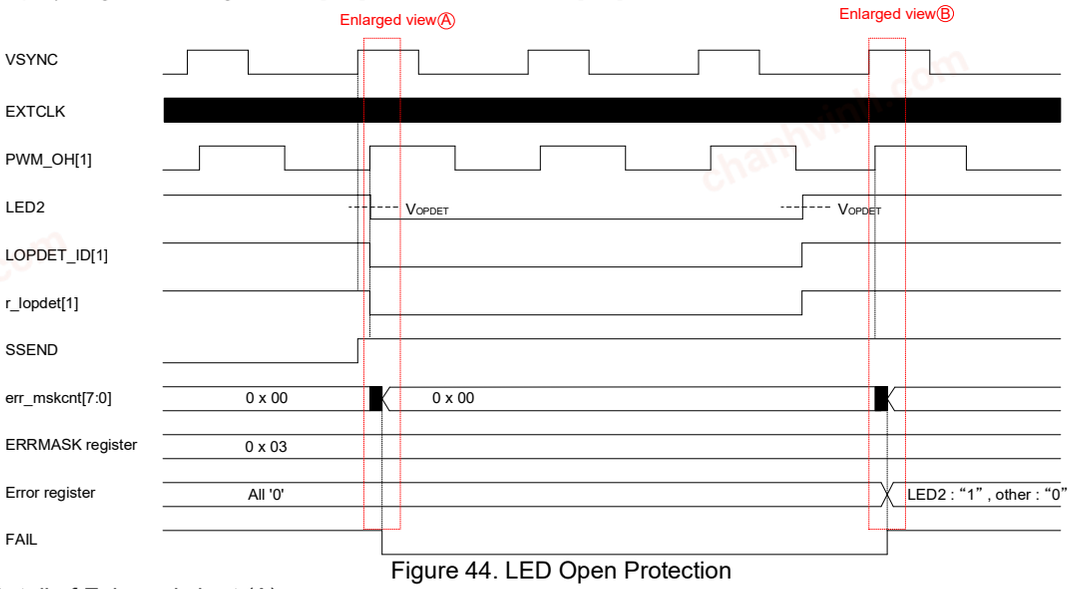


Figure 44. LED Open Protection

(a) Detail of Enlarged chart (A)

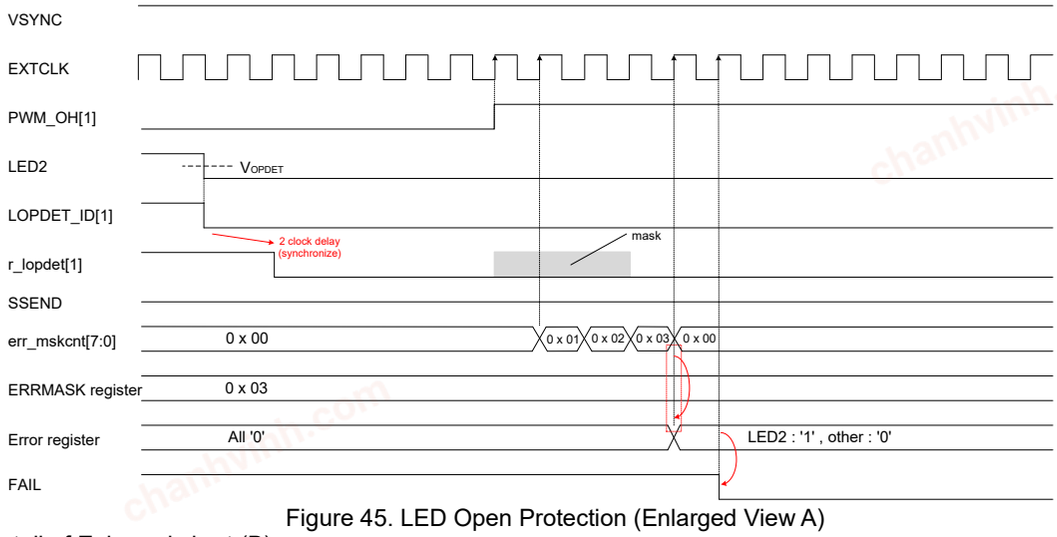


Figure 45. LED Open Protection (Enlarged View A)

(b) Detail of Enlarged chart (B)

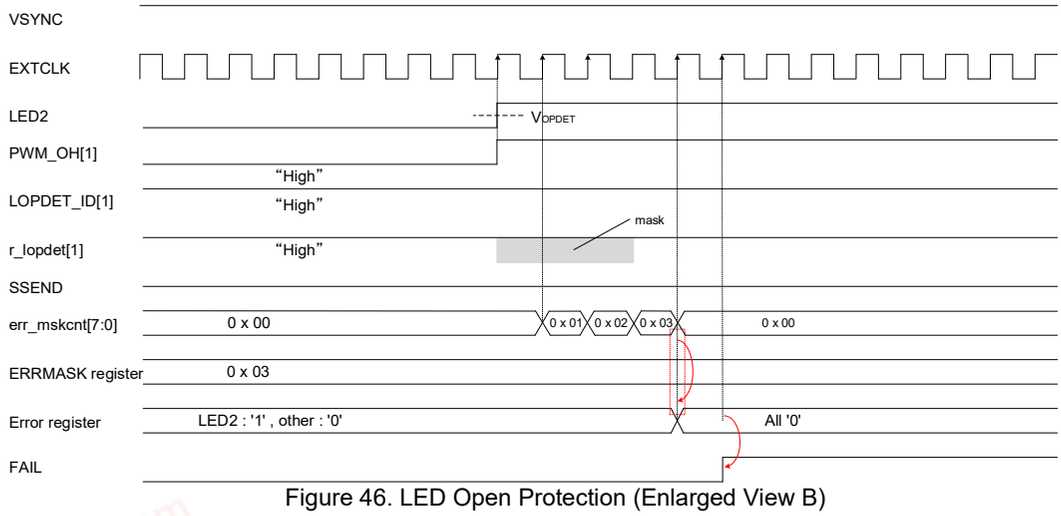


Figure 46. LED Open Protection (Enlarged View B)

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(2) LED Open Protection – continued

[Operation]

When PWM_OH[1] = 'High' and LOPDET_ID[1] = 'Low' with SSEND = 'High' (Soft Start end), ERRMASK starts counting with EXTCLK (err_mskcnt_r) from the rise-edge of PWM_OH[1]. At the arriving to the set value (0x03), FAIL is set to 'Low', i.e. ERROR is started to be detected. When ERROR is detected and PWM_OH[1] = 'High' and LOPDET_ID[1] = High, ERRMASK starts counting with EXTCLK (err_mskcnt_r) from the rise-edge of PWM_OH[1]. At the arriving to the set value (0x03), FAIL is set to 'High', i.e. It released ERROR condition.

(Example) low width error case,
Register setting: DLY02[7:0] = 0x00, ERRMASK[7:0] = 0x03, ERRLAT = 0

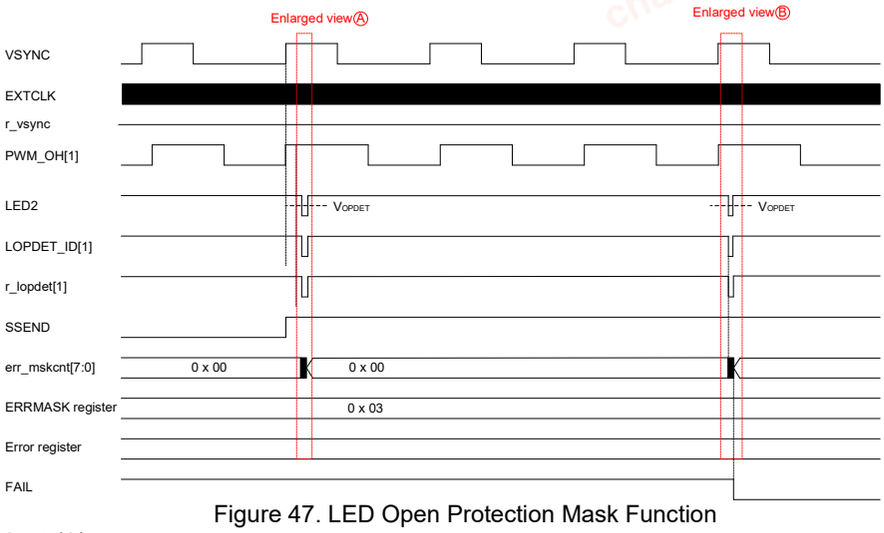


Figure 47. LED Open Protection Mask Function

(a) Enlarged chart (A)

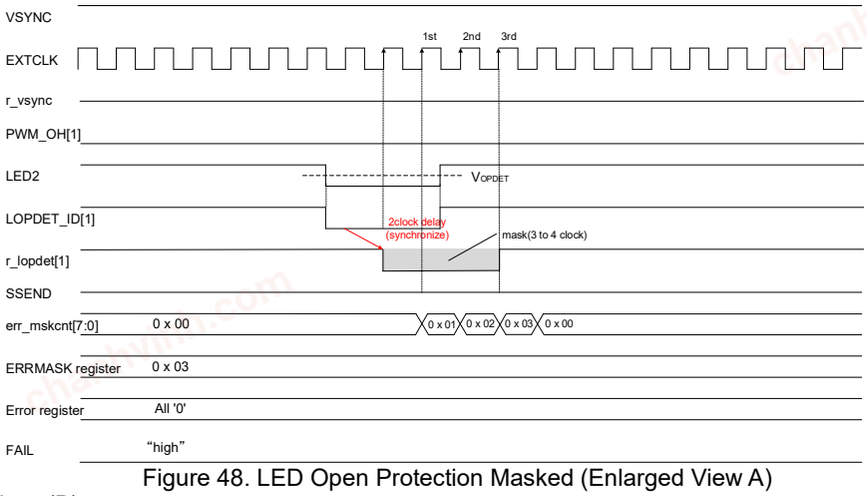


Figure 48. LED Open Protection Masked (Enlarged View A)

(b) Enlarged chart (B)

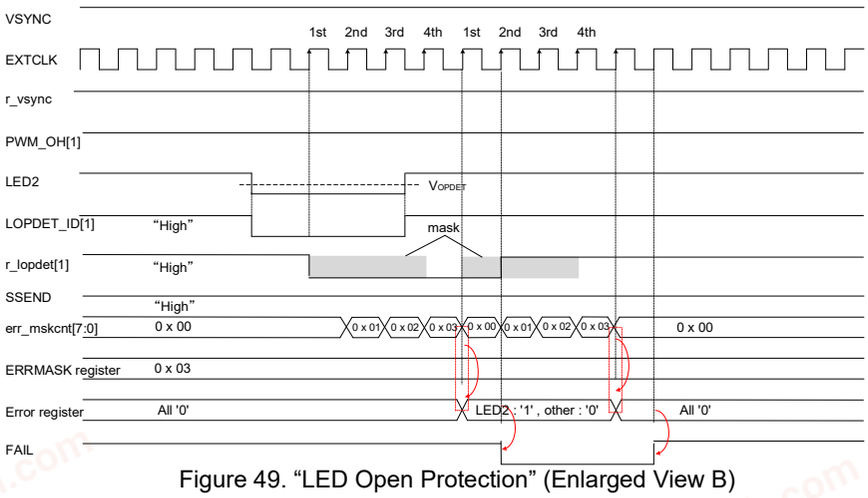


Figure 49. "LED Open Protection" (Enlarged View B)

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3. ERROR Control – continued

(3) TSD Warning

If It heats over 135 deg, it detects “TSD warning” (WARTSD_ID[1] = Low).
It update error register (WARTSD[1] = 1) and FAIL = Low after detection.
If it releases error condition, it updates error register (WARTSD[1] = 0) and FAIL = High.
This function has enabled (TSDWEN). If TSDWEN = 0, it doesn’t detect “TSD warning protection”
PWM_OH[n-1] signal don’t effect “TSD warning protection”.

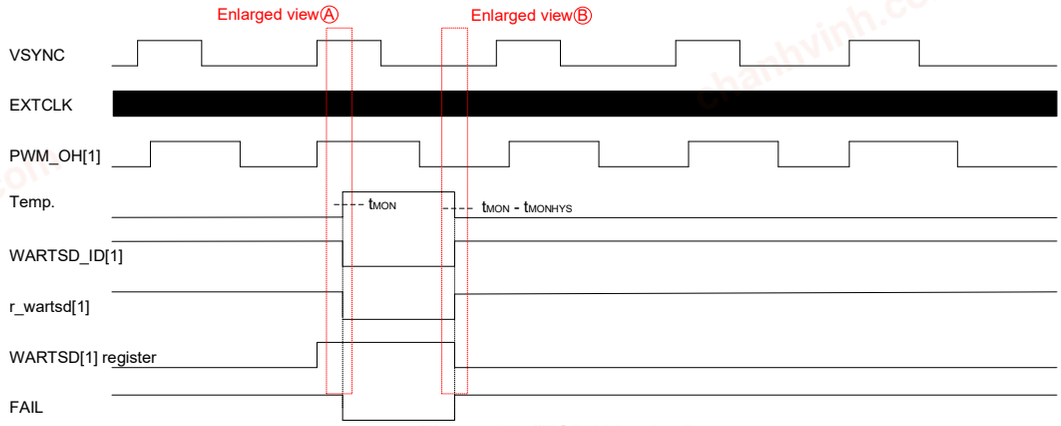


Figure 50. “TSD Warning”

(a) Enlarged chart (A)

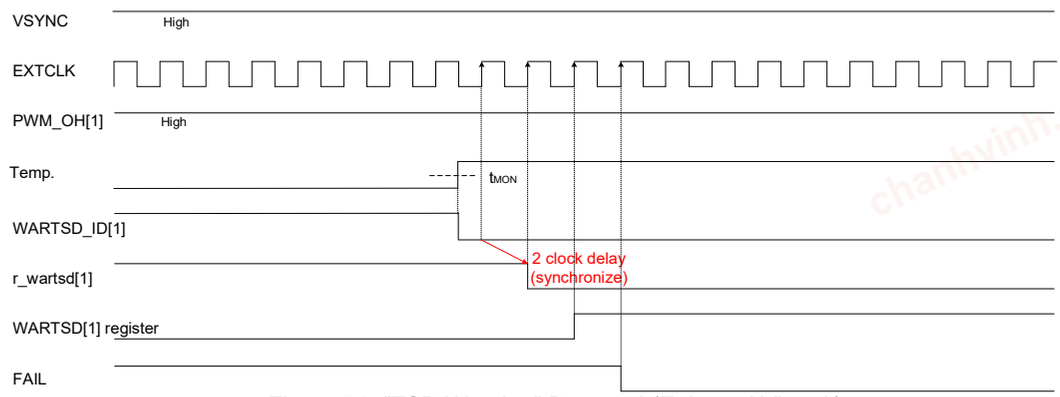


Figure 51. “TSD Warning” Detected (Enlarged View A)

(b) Enlarged chart (B)

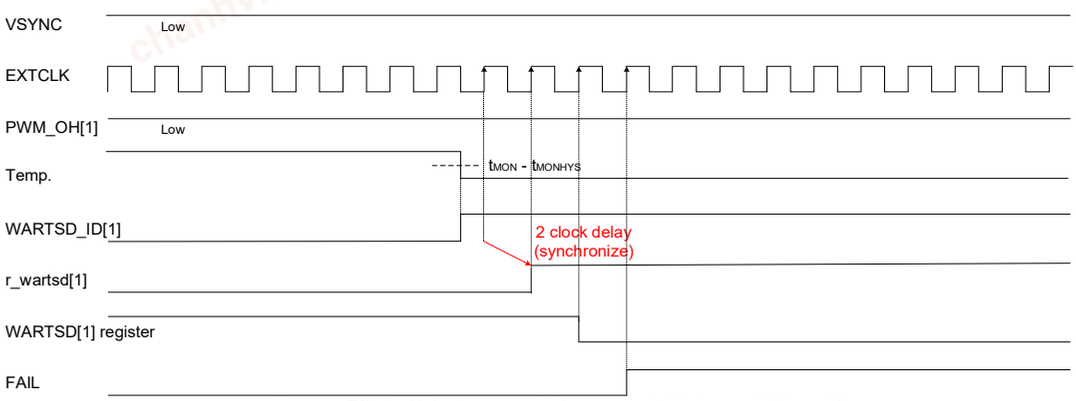


Figure 52. “TSD Warning” Released (Enlarged View B)

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3. ERROR Control – continued

(4) ISET Short Warning

If It set ISET resistor under 2.5 kΩ, it detect “ISET short warning” (WARISET_IL = Low).
It update error register (WARISET = 1) and FAIL = Low after detection.
If it release error condition, it update error register (WARISET = 0) and FAIL = High.

ERRMASK doesn’t effect this protection.

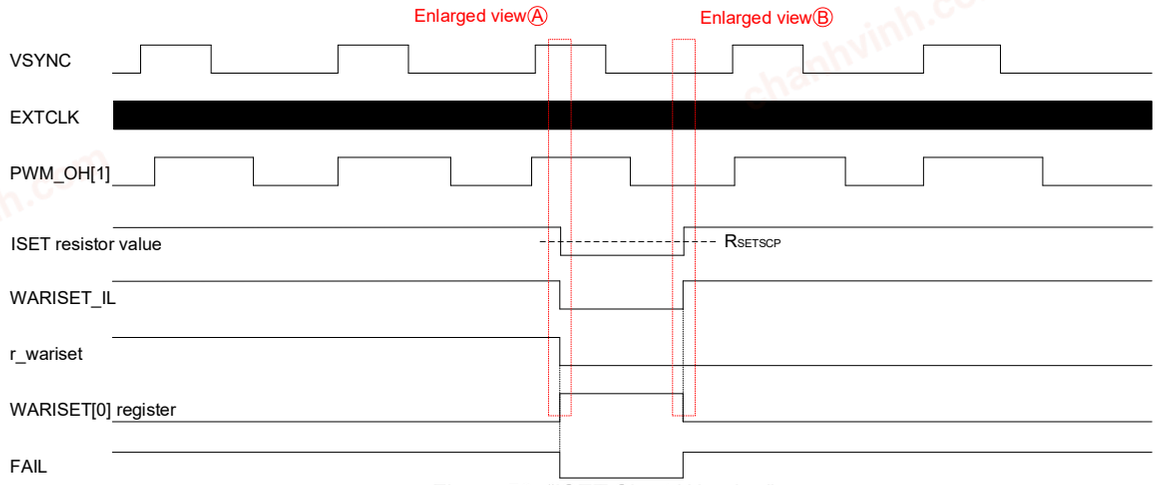


Figure 53. “ISET Short Warning”

(a) Enlarged chart (A)

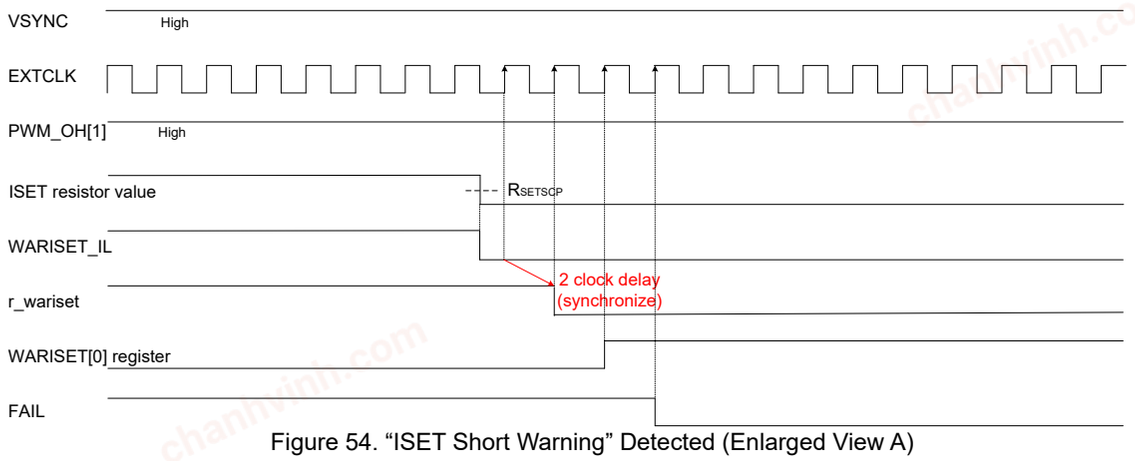


Figure 54. “ISET Short Warning” Detected (Enlarged View A)

(b) Enlarged chart (B)

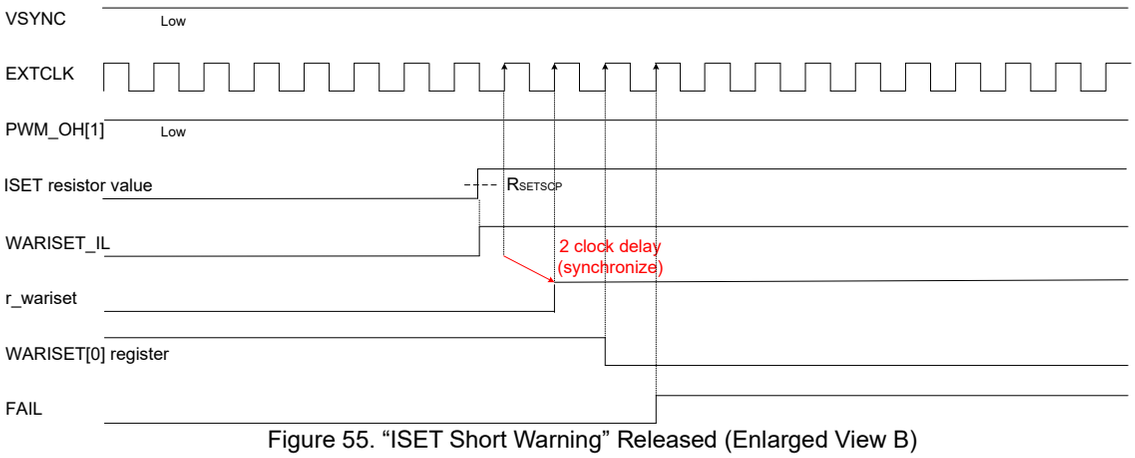


Figure 55. “ISET Short Warning” Released (Enlarged View B)

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3. ERROR Control – continued

(5) TSD

If It heat over 175 deg, it detect “TSD” (TSD_IL = Low).
It update FAIL = Low and initialized all circuit after detection.
It update FAIL = High after released.

ERRMASK and SSMASK don’t effect this protection.

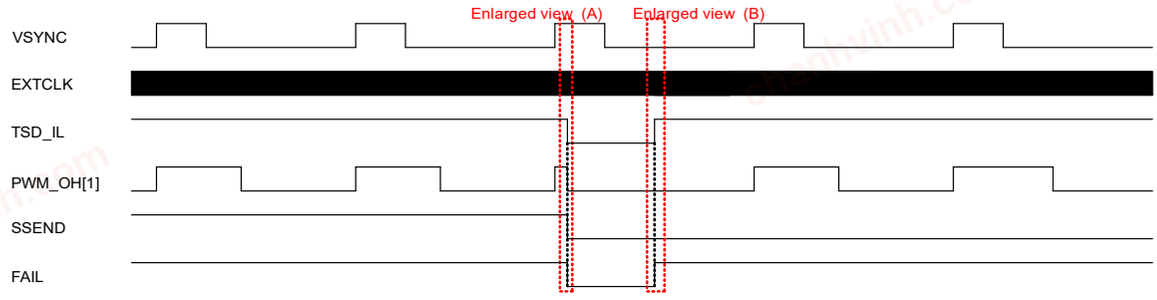


Figure 56. TSD

(a) Enlarged chart (A)

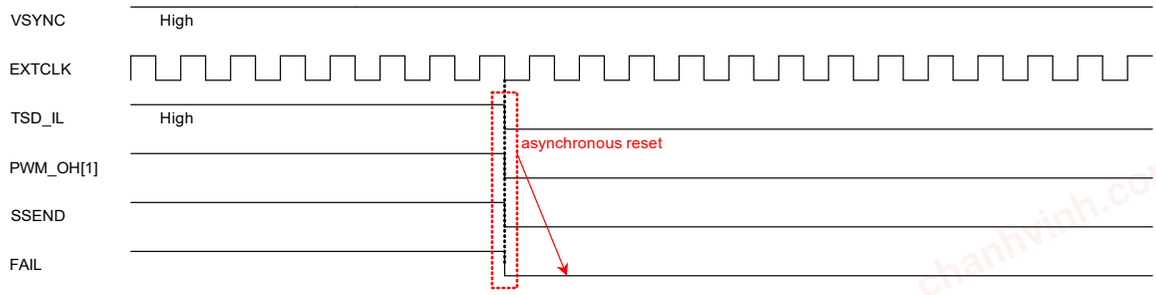


Figure 57. “TSD” Detected (Enlarged View A)

(b) Enlarged chart (B)

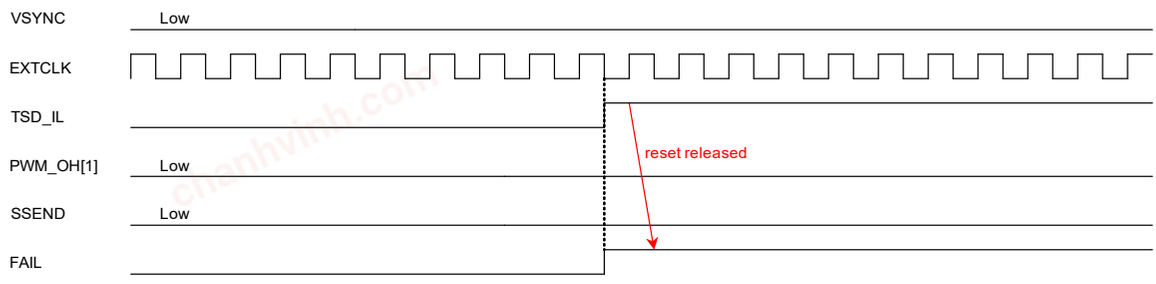


Figure 58. “TSD” Released (Enlarged View B)

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3. ERROR Control – continued

(6) Soft-Start Masking Function

The time of mask of ERROR detection at starting of IC is set by counting the number of VSYNC.

Time of mask = set value x VSYNC

(Example) Address = 0x03(SSMASK), DATA = 0x3C:

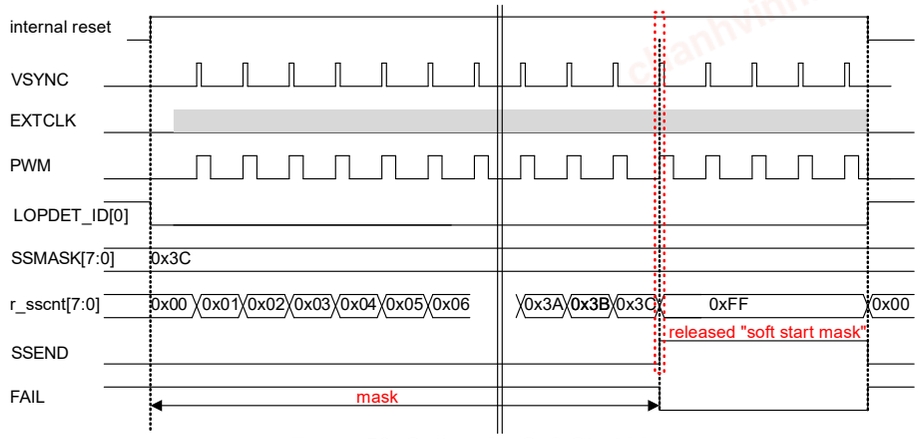


Figure 59. Setting for Soft Start Mask

(7) LED SCP

LED SCP is operated after detecting “LED open error” and writing DTYENn = 0.
MASK time can be controlled by SCPTIME register.
FAIL outputs VSYNC pulse after the MASK time.

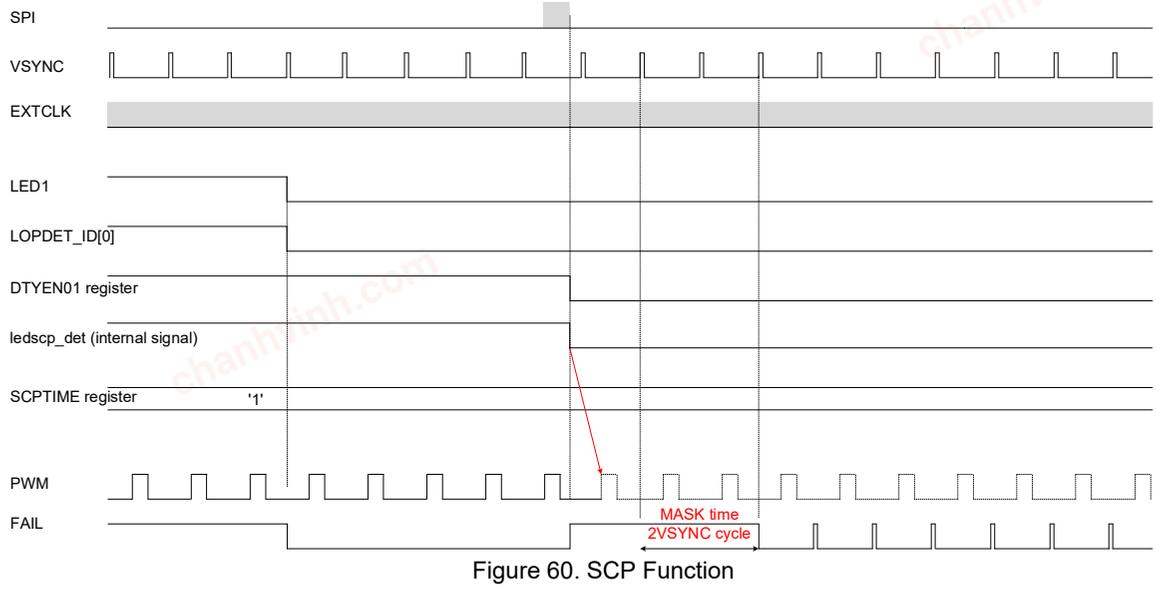


Figure 60. SCP Function

(Note) It can’t detect “SCP error” if LEDn (n = 1 to 16) pin shorts GND before setting DTYEN = 1 and detecting LED open error”. This function is available after detecting “LED open error”.

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Timing Chart - continued

4. Boot Sequence

(1) Normal Boot

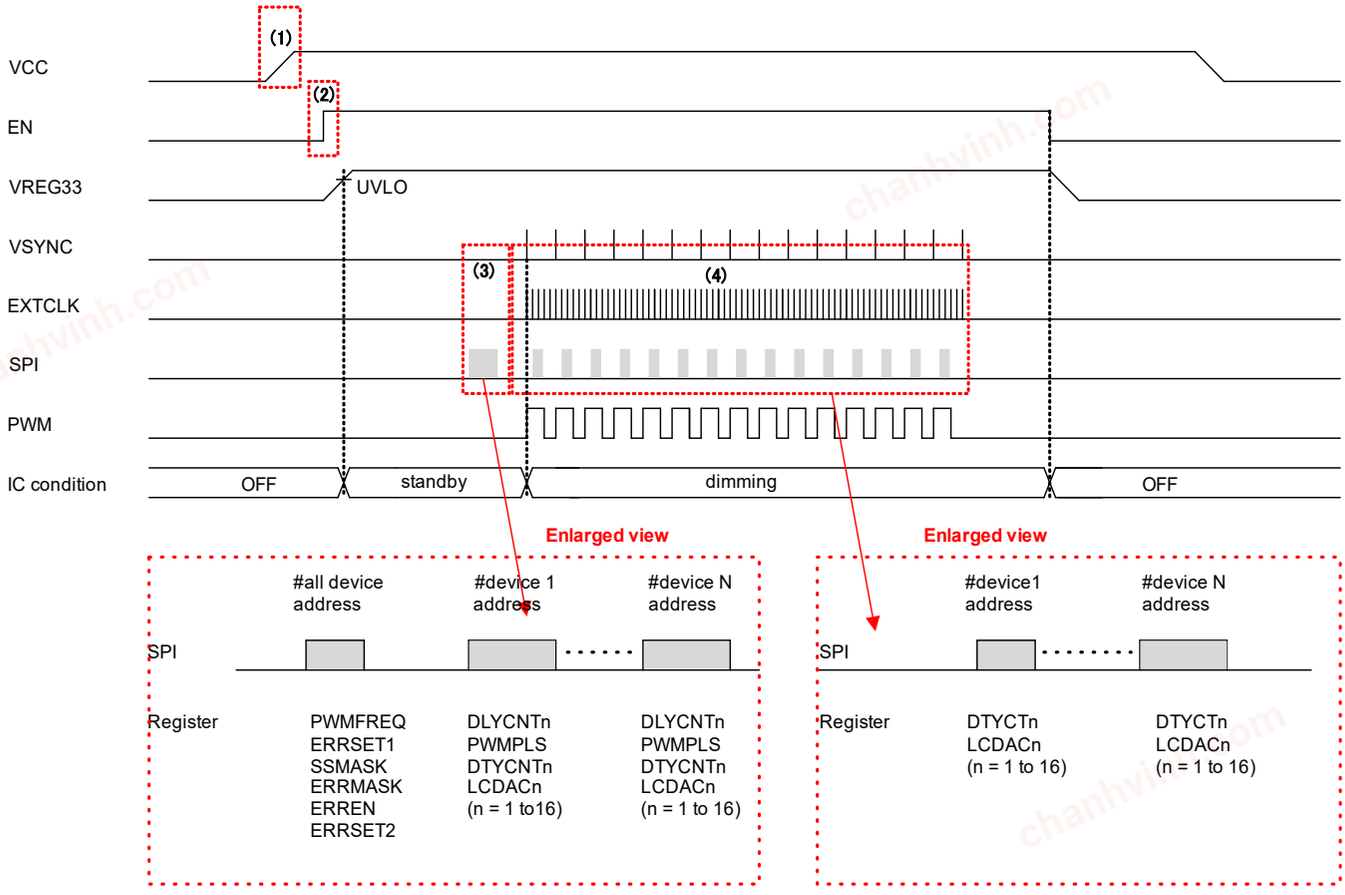


Figure 61. Starting Sequence for Normal Operation

When you light the LED by general SPI control, follow the sequence below.

(1) Input the power supply of VCC.
(2) Launch the EN from ‘Low’ to ‘High’.
(3) Write the data to the register by SPI control, then set the LED driver.
(4) Input the VSYNC, EXTCLK signal and set register for PWM dimming.

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Timing Chart - continued

5. PWM Dimming Sequence

It has “register”, “buffer” and “control data” for DTYCNTn and LCDACn. 1st “register” are updated by SPI. 2nd “buffer” are updated at VSYNC pulse, 3rd “control data” are updated at PWM timing as following for keeping data until finishing output.

(1) PWM Duty (DTYCNTn)/Local DAC (LCDACn) Control

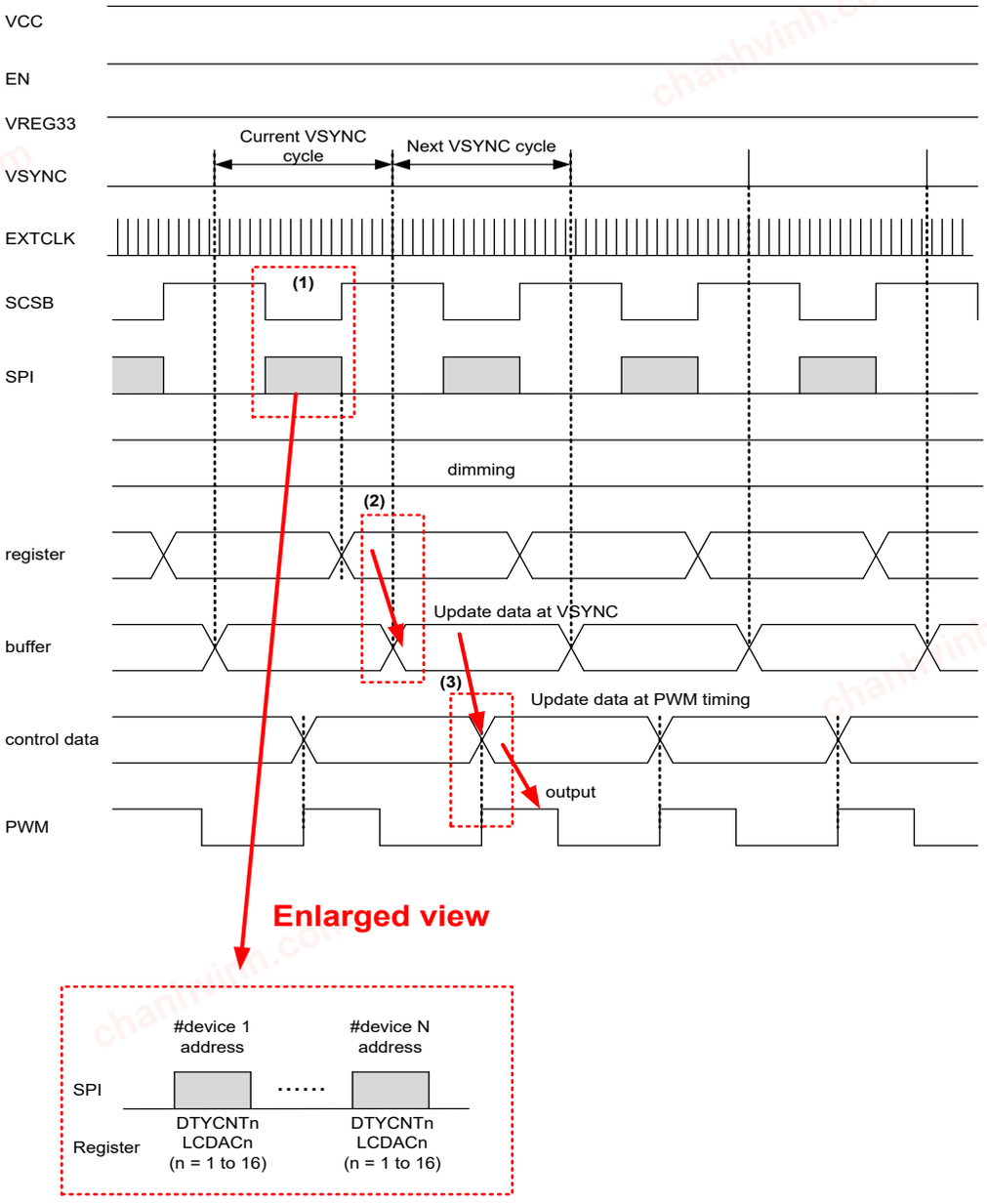


Figure 62. Dimming Sequence for Normal Operation

When the LEDs are controlled by general SPI control, the sequence is the following.
(1) “SPI write sequence” should be finished in “current VSYNC cycle” until next VSYNC pulse.
(2) The buffer value is updated at VSYNC timing.
(3) The control data (DTYCNTn, LCDACn) are updated and PWM is updated at the same time.

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5. PWM Dimming Sequence – continued

(2) PWM Duty (DTYCNTn)/Local DAC (LCDACn) Control (Wrong SPI Access)

If MCU access at VSYNC pulse, it don't update buffer data for any register (update timing VSYNC, PWM)

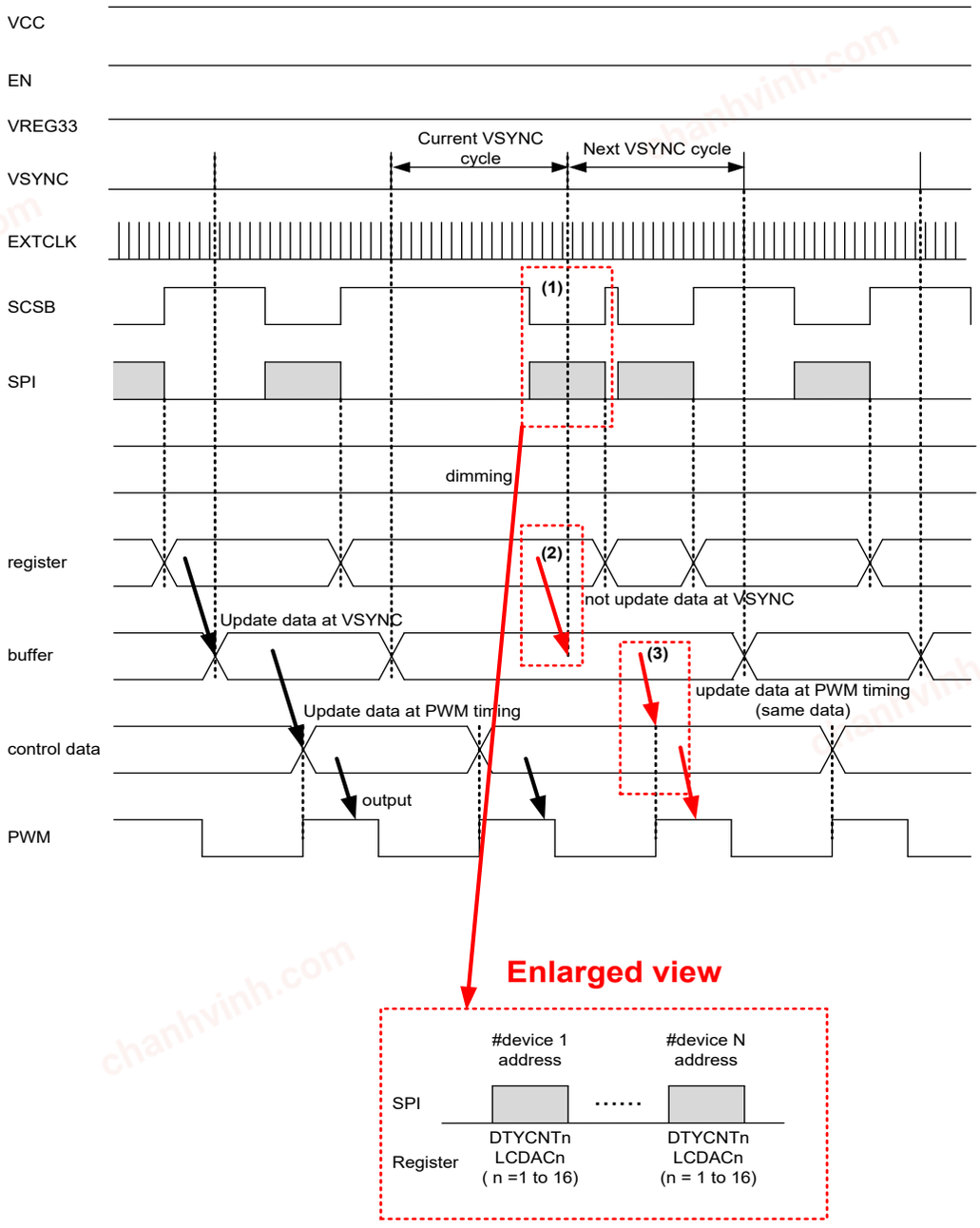


Figure 63. Dimming Sequence for Normal Operation (Wrong SPI Access)

When the LEDs are controlled by general SPI control, the sequence is the following.
(1) "SPI write sequence" is not finished in "current VSYNC cycle" until next VSYNC pulse.
(2) The buffer value is not updated at VSYNC timing. (because it occurred SCSB = Low and VSYNC pulse condition)
(3) The control data (DTYCNTn, LCDACn) are not updated, because buffer value is not updated.

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Timing Chart - continued

6. Error Sequence

(1) Error Sequence for “LED Open Protection” without ERRLAT

Example) It detects “LED open error” in LED1

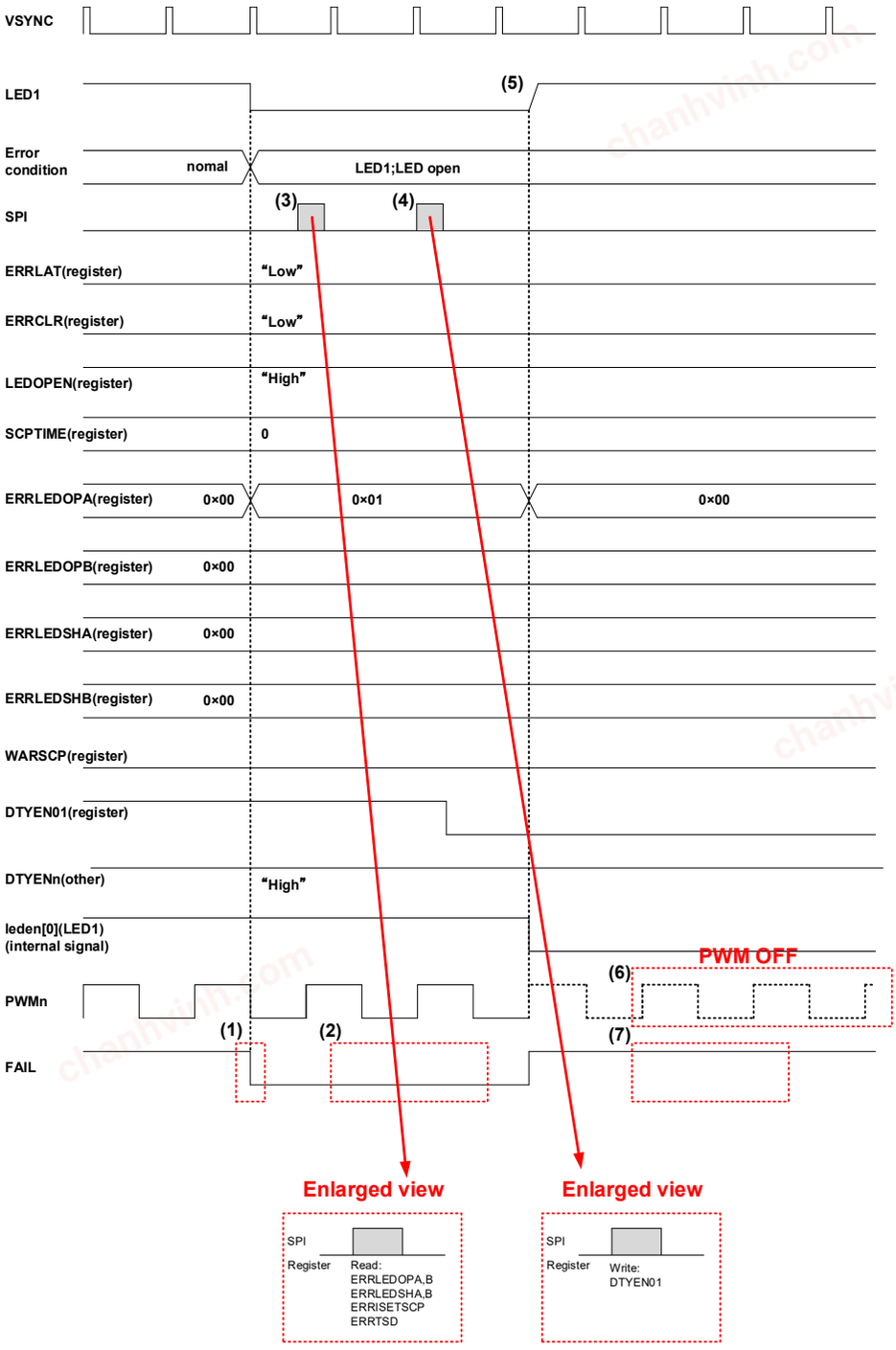


Figure 64. Error Sequence for “LED OPEN Error” without ERRLAT

(1) If it detects “LED OPEN error”, it outputs Low from FAIL after ERRMASK time.
(2) If Error condition is released in this timing, it outputs high from FAIL after ERRMASK.
(3) MCU read “Error register” after MCU receiving FAIL = Low condition.
(4) MCU write “DTYEN01 = 0” of “Error Channel” for protection.
(5) It pulls up the LED1 pin after DTYEN01 = 0. So LED1 voltage is over 0.2 V for LED1 open.
(6) PWM output is OFF after next VSYNC and PWM timing.
(7) “Error register” and FAIL return normal condition after next VSYNC and PWM timing.

MCU can’t detect Error condition if “error condition” is cleared before reading “error register”.

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6. Error Sequence – continued

(2) Error Sequence for SCP without ERRLAT

Example) It detects “SCP Error” in LED1.

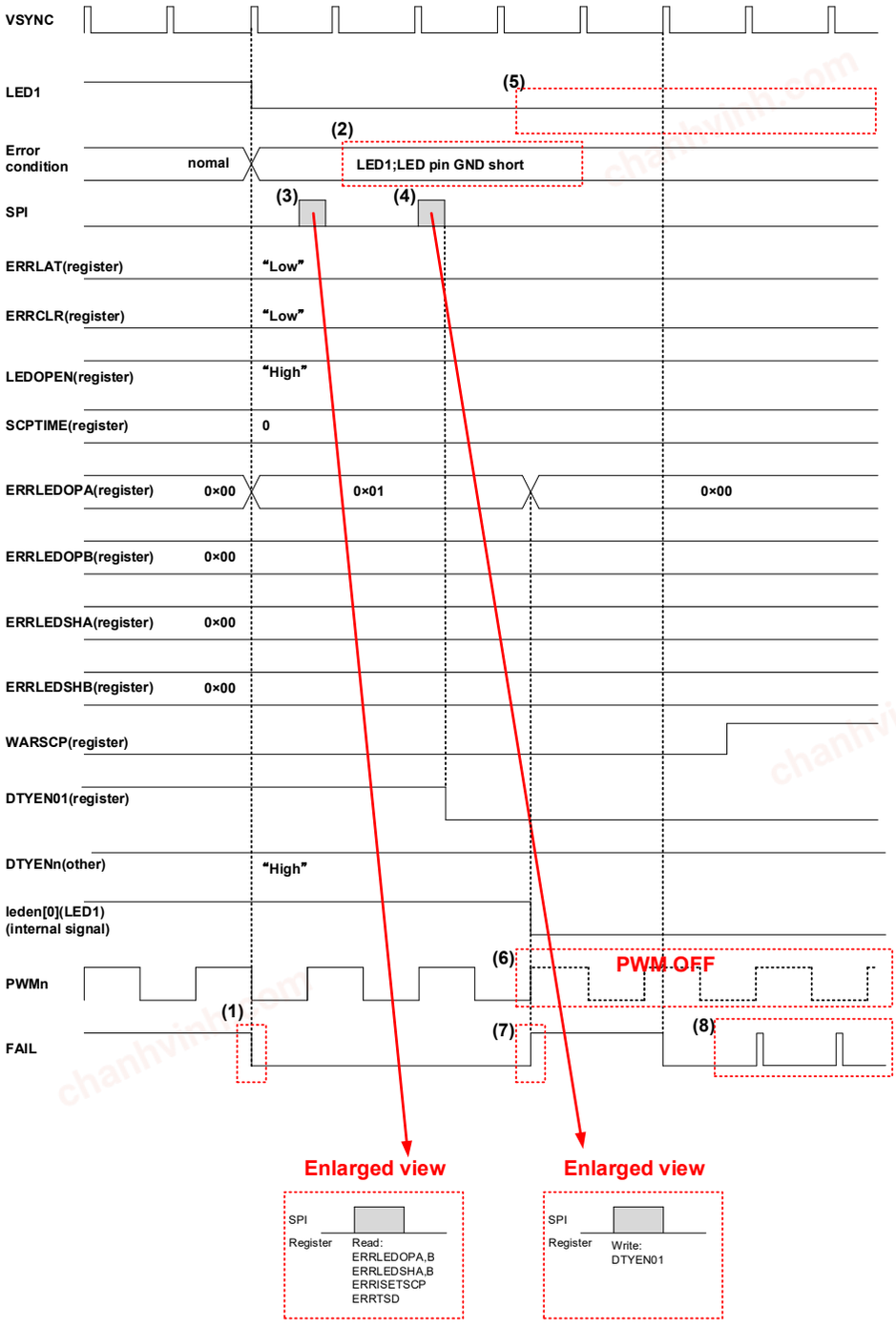


Figure 65. Error Sequence for SCP without ERRLAT

(1) If it detecs “LED OPEN error” after ERRMASK time, it outputs Low from FAIL.
(2) If Error condition is released in this timing, it outputs high from FAIL after ERRMASK.
(3) MCU read “Error register” after MCU receiving FAIL = Low condition.
(4) MCU write “DTYEN01 = 0” of “Error Channel” for protection.
(5) It pulls up the LED1 pin after DTYEN01 = 0. But it can’t be over 0.3 V because LED1 shorts to GND.
(6) It doesn’t outputs PWM after next VSYNC and PWM timing.
(7) It releases “Error register” and FAIL after next VSYNC and PWM timing.
(8) It outputs VSYNC pulse from the FAIL pin after detecting SCP.

MCU can’t detect Error condition if “error condition” is cleared before reading “error register”.

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6. Error Sequence – continued

(3) Error Sequence for “LED Open Protection” with ERRLAT

Example) It detects “LED open error” in LED1

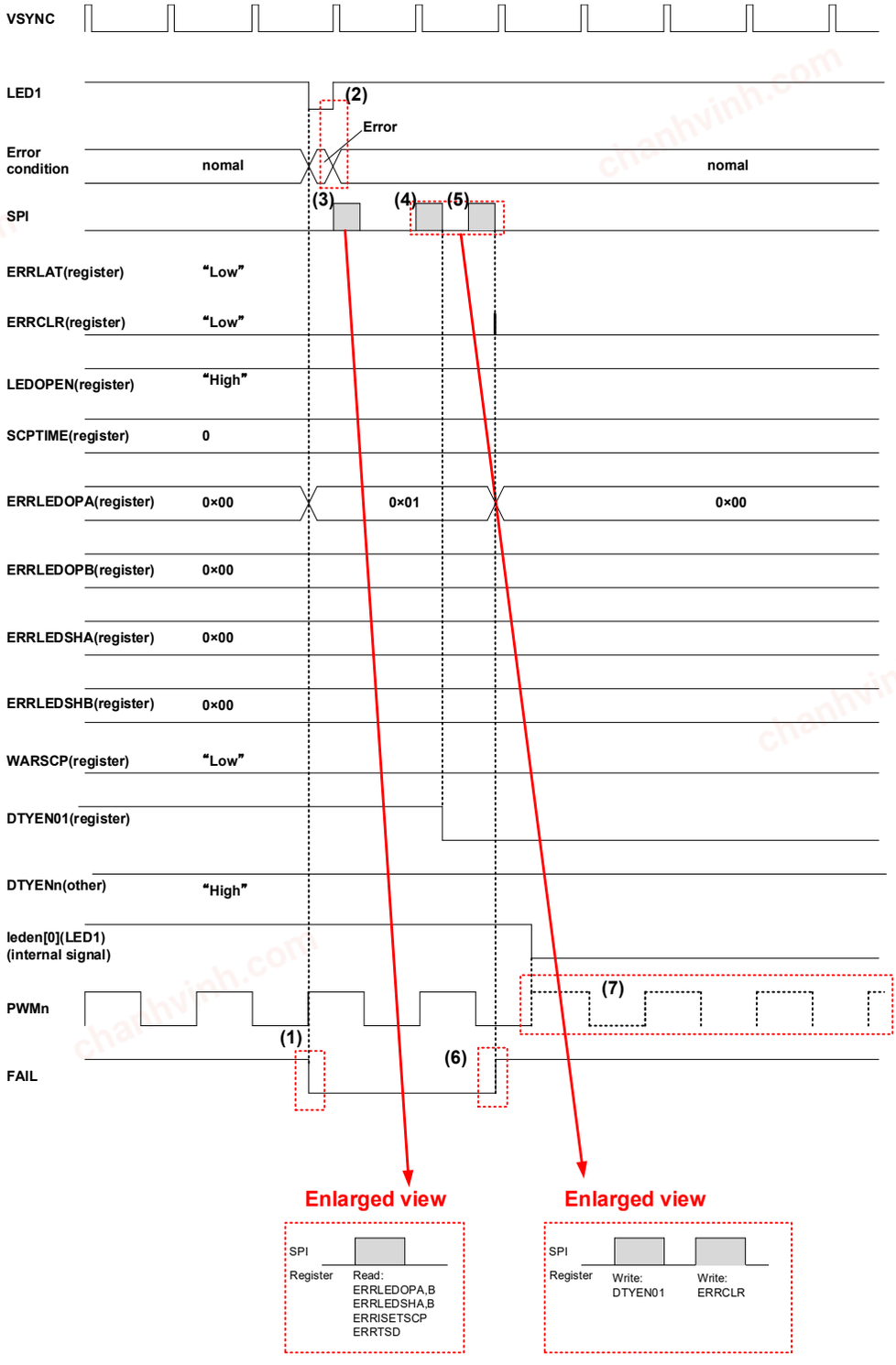


Figure 66. Error Sequence for “LED Open Protection” with ERRLAT

(1) If it detects “LED open error”, it outputs Low from FAIL after ERRMASK time.
(2) If Error condition is released in this timing, it keeps Low in FAIL and “Error register”.
(3) MCU read “Error register” after MCU receiving FAIL = Low condition.
(4) MCU write “DTYEN01 = 0” of “Error Channel” for protection condition released.
(5) MCU write “ERRCLR = 1” for releasing “Latch condition”.
(6) “Error register” and FAIL return normal condition after ERRCLR = 1.
(7) PWM is OFF after next VSYNC and PWM timing.

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6. Error Sequence – continued

(4) Error Sequence SCP with ERRLAT

Example) It detects “SCP Error” in LED1.

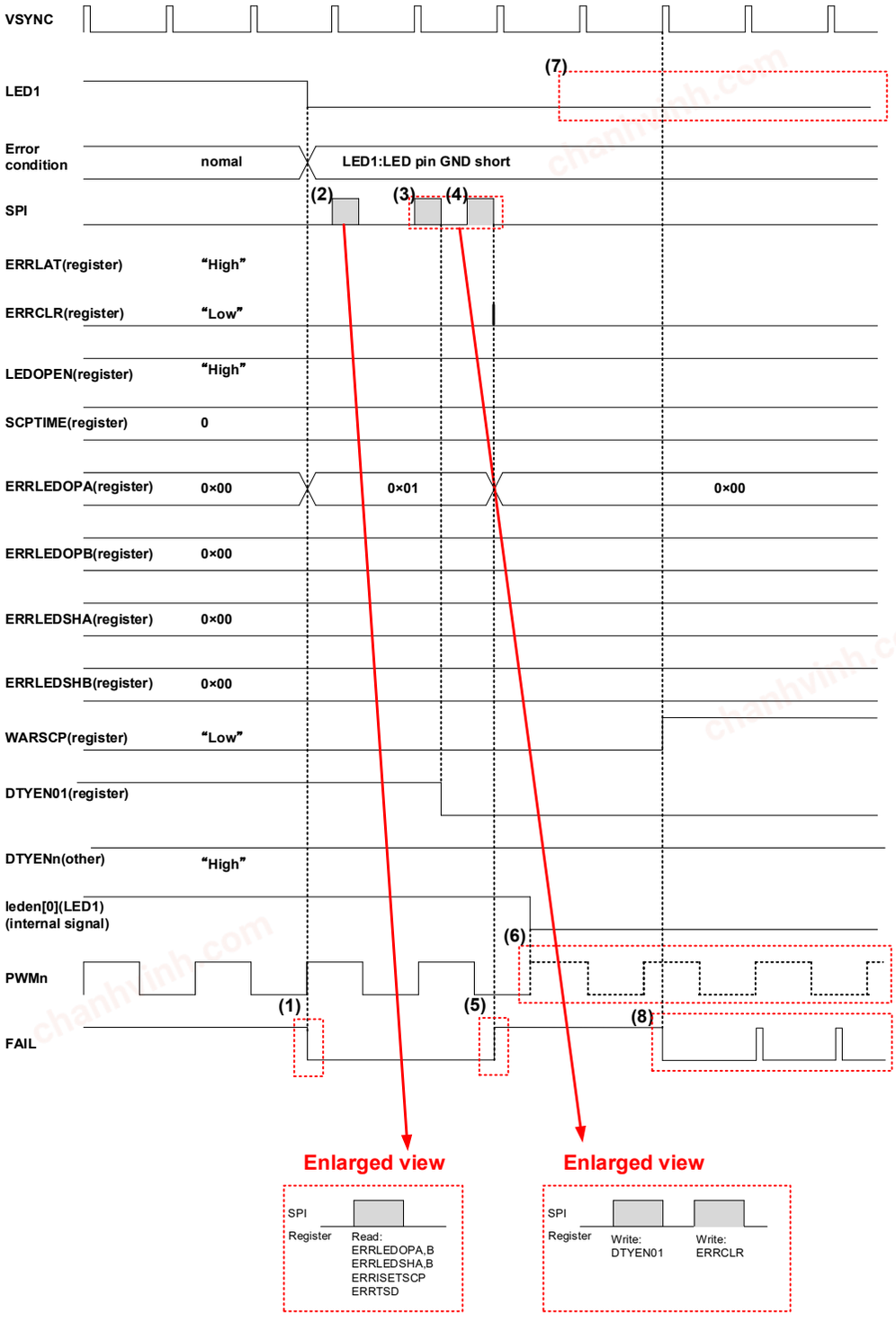


Figure 67. Error Sequence for SCP with ERRLAT

(1) If it detects “LED open error”, it outputs Low from FAIL after ERRMASK time.
(2) MCU read “Error register” after MCU receiving FAIL = Low condition.
(3) MCU write “DTYEN01 = 0” of “Error Channel” for protection condition released.
(4) MCU write “ERRCLR = 1” for releasing “Latch condition”.
(5) “Error register” and FAIL return normal condition after ERRCLR = 1
(6) PWM is OFF after next VSYNC and PWM timing.
(7) It pulls up LED1 pin. But it can’t be over 0.3 V because LED1 shorts to GND.
(8) It detects SCP. So output VSYNC input from the FAIL pin.

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Timing Chart - continued

7. FAIL Control Sequence

FAIL output can be controlled by register setting.

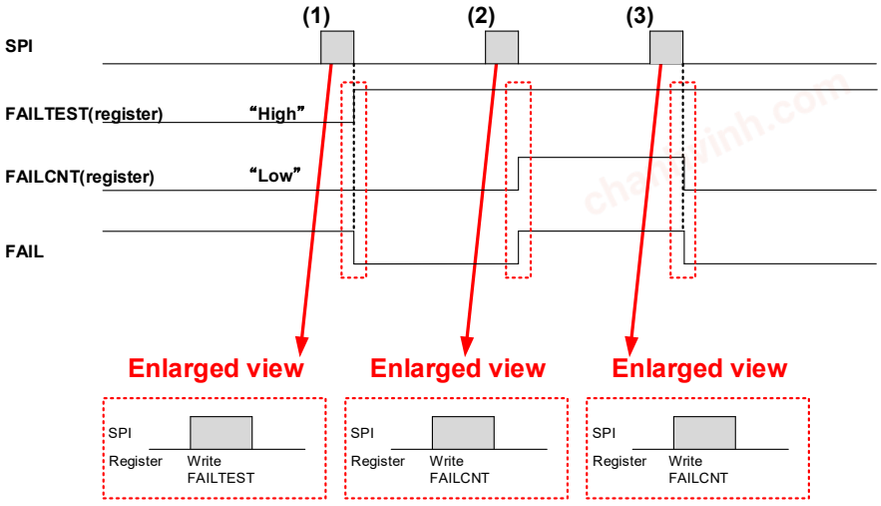


Figure 68. FAIL Control Sequence

(1) It is available to control FAIL output by FAILTEST = 1
(2) FAILCNT = High, so it outputs High from the FAIL pin.
(3) FAILCNT = Low, so it outputs Low from the FAIL pin.

(1) LED Open Protection

When PWMn = high, If the LEDn pin becomes 0.1 V (Typ) or lower, FAIL = 'Low' is outputted and "LED open error" will be detected. (n = 1 to 16)

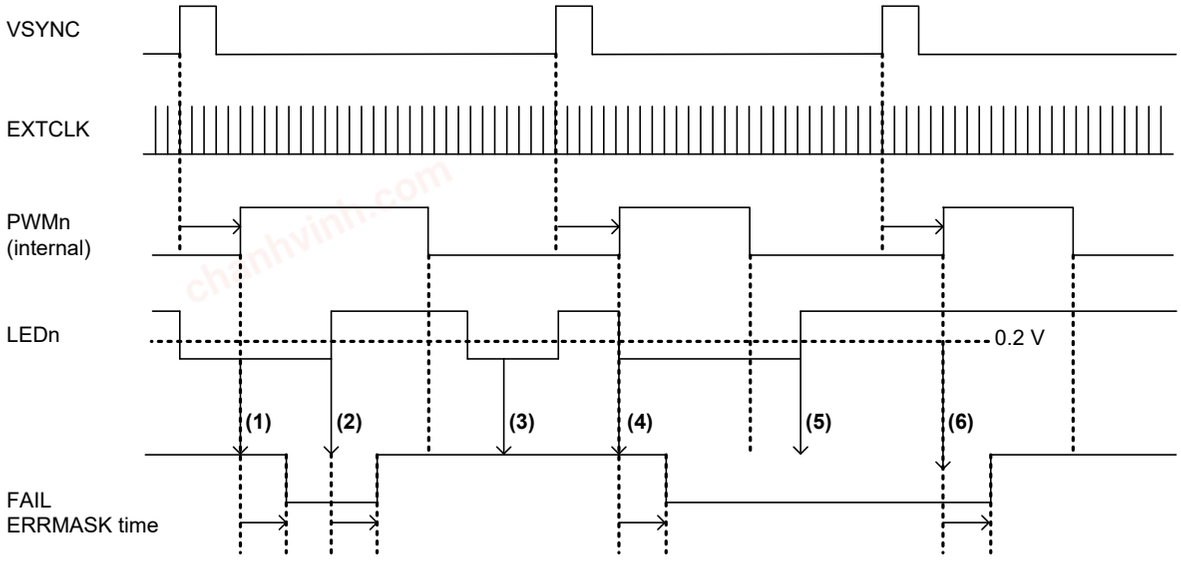


Figure 69. LED Open Protection

(1) When PWMn = 'High', "LED open error" is detected. FAIL outputs 'Low' after ERRMASK time.
(2) If LEDn pin voltage is release condition, FAIL outputs 'High' after ERRMASK.
(3) If LEDn pin voltage is release condition when PWMn = 'Low', it keeps FAIL condition (High).
(4) When PWMn = 'High', "LED open error" is detected. FAIL outputs 'Low' after ERRMASK time.
(5) If LEDn pin voltage is release condition when PWMn = 'Low', it keeps FAIL condition (Low).
(6) If LEDn pin voltage is release condition, FAIL outputs 'High' after ERRMASK.

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7. FAIL Control Sequence – continued

(2) LED Short Protection

If LEDn pin becomes LEDSH[3:0](Address 0x02) when PWMn = high, FAIL = ‘Low’ is outputted and “LED short error” will be detected. (n = 1 to 16)

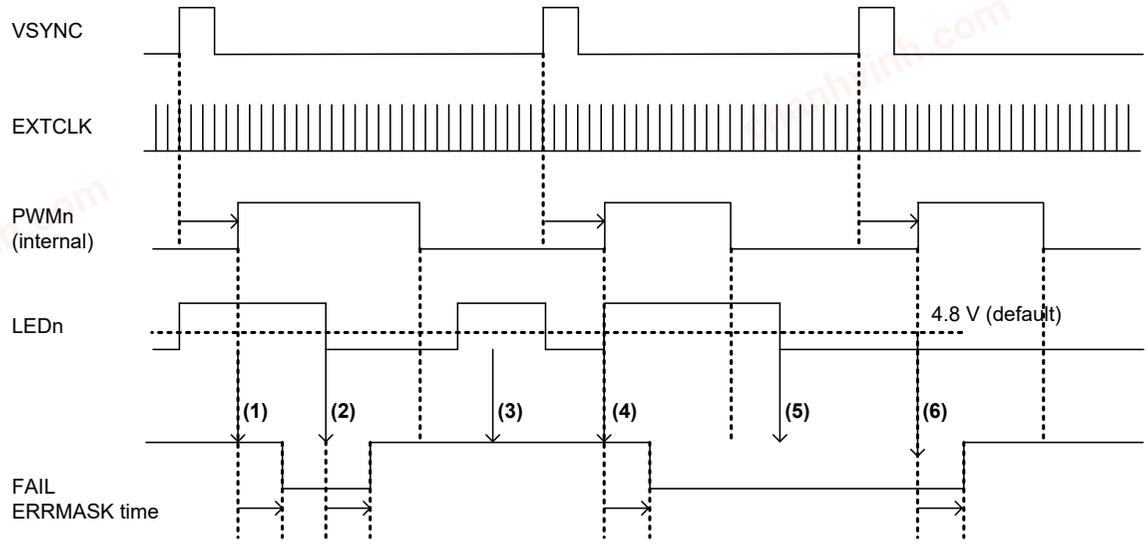


Figure 70. LED Short Protection

(1) When PWMn = ‘High’, “LED short error” is detected. FAIL outputs ‘Low’ after ERRMASK time.
(2) If LEDn pin voltage is release condition, FAIL outputs ‘High’ after ERRMASK.
(3) If LEDn pin voltage is release condition when PWMn = ‘Low’, it keeps FAIL condition (High).
(4) When PWMn = ‘High’, “LED short error” is detected. FAIL outputs ‘Low’ after ERRMASK time.
(5) If LEDn pin voltage is release condition when PWMn = ‘Low’, it keeps FAIL condition (Low).
(6) If LEDn pin voltage is release condition, FAIL outputs ‘High’ after ERRMASK.

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Application Examples

1. External Component Setting Example

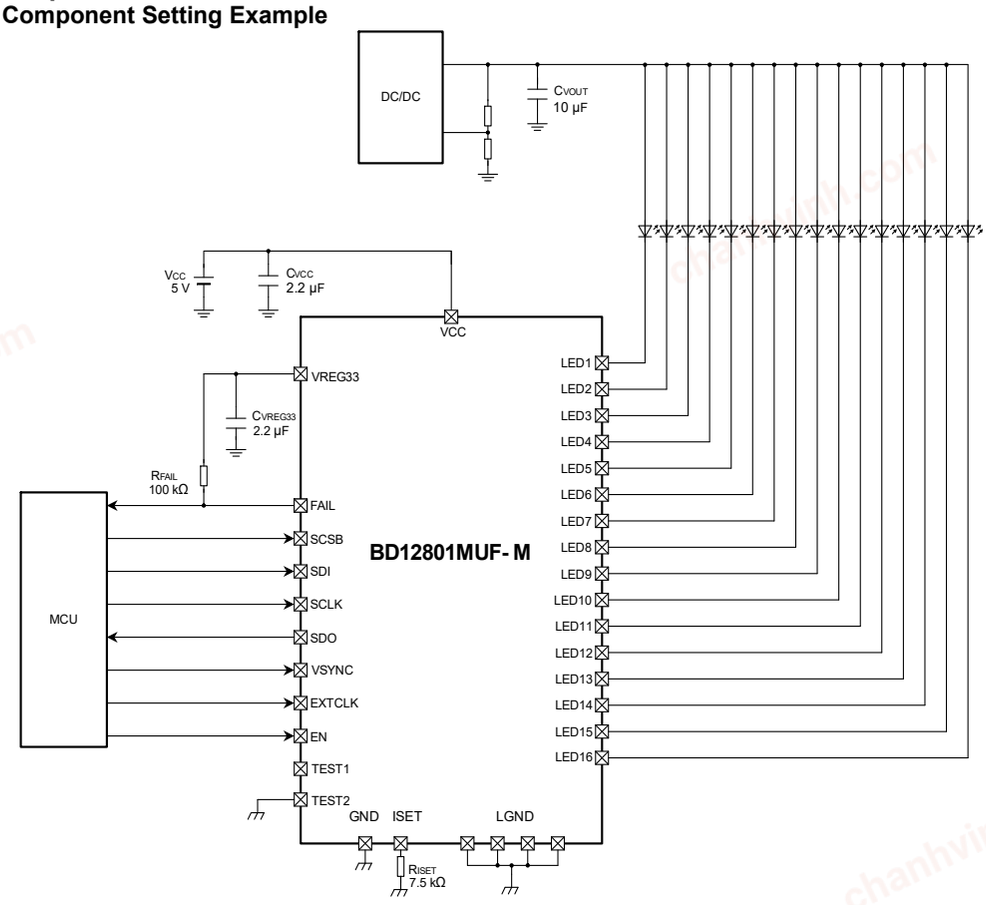


Figure 71. External Component Setting Example

2. Cascade Connection Application

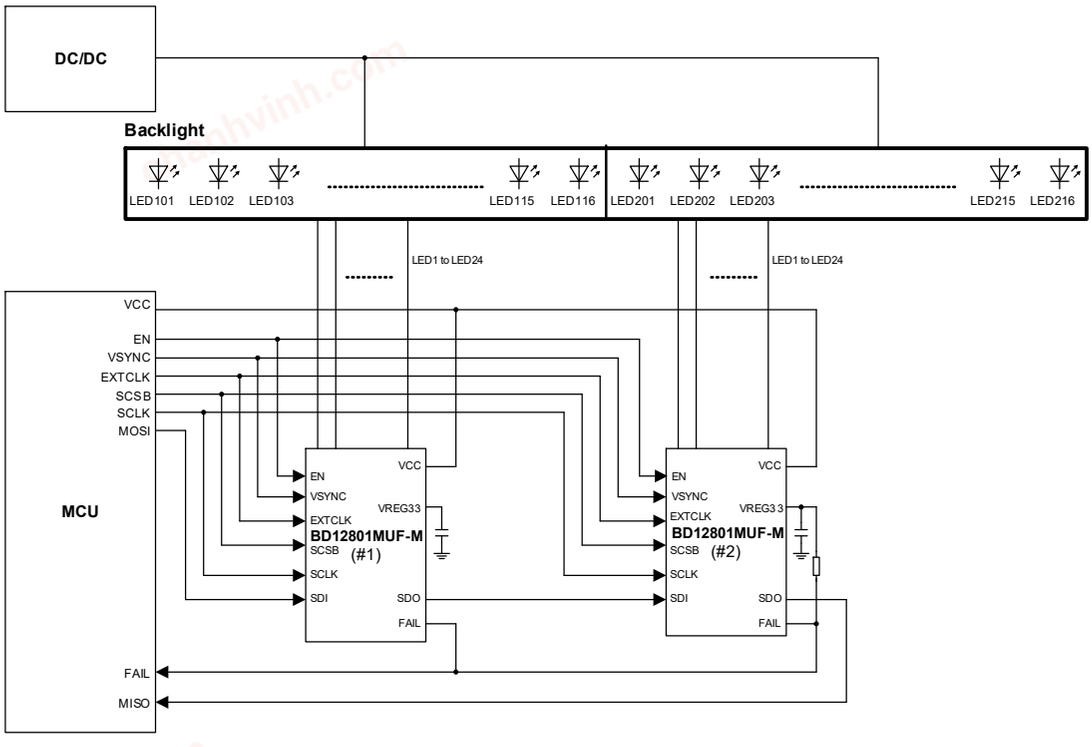
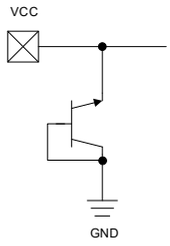
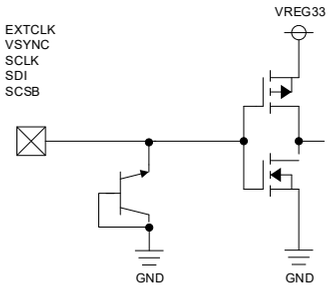
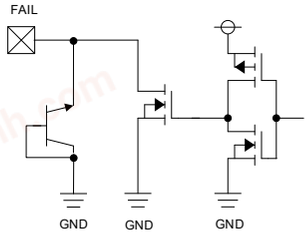
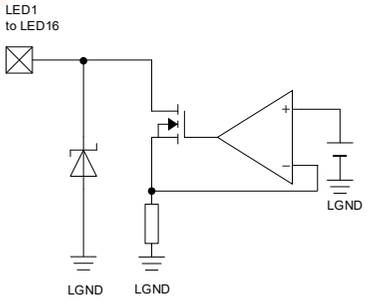
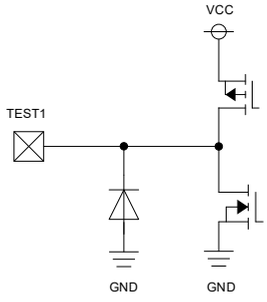
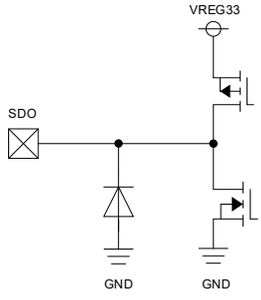
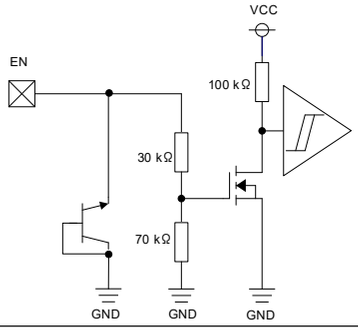
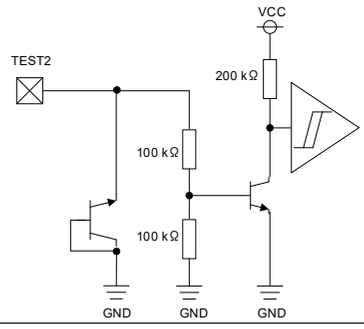
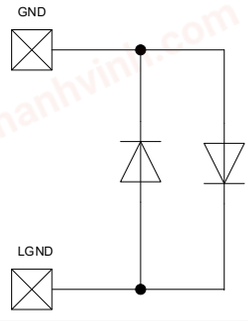
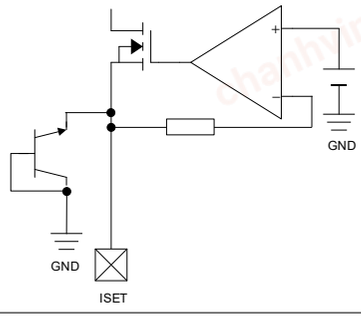
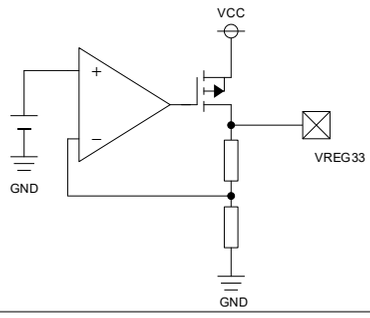


Figure 72. Cascade Connection Application

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I/O Equivalence Circuit

VCC	EXTCLK, VSYNC, SCLK, SDI, SCSB	FAIL
		
LED1 to LED16	**TEST1**	**SDO**
		
EN	**TEST2**	**GND,LGND**
		
ISET	**VREG33**	
		

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Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

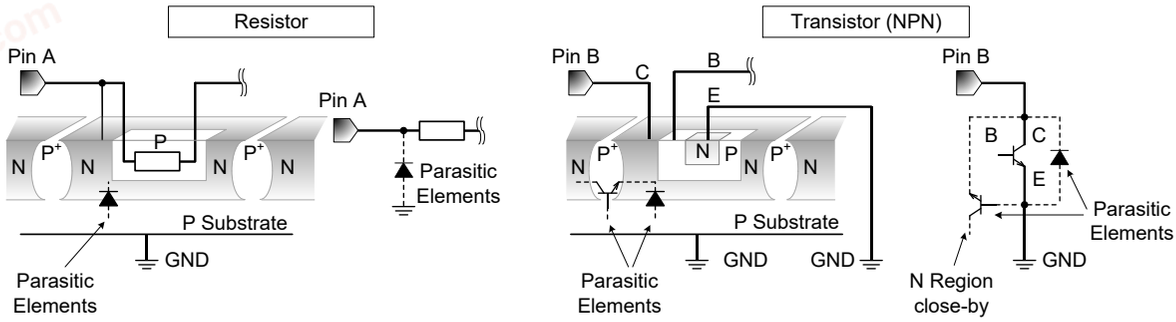


Figure 73. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information

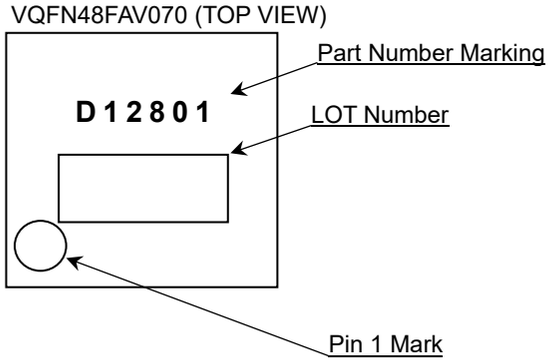
B	D	1	2	8	0	1	M	U	F	-	ME2

Package
MUF: VQFN48FAV070

Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram

VQFN48FAV070 (TOP VIEW)

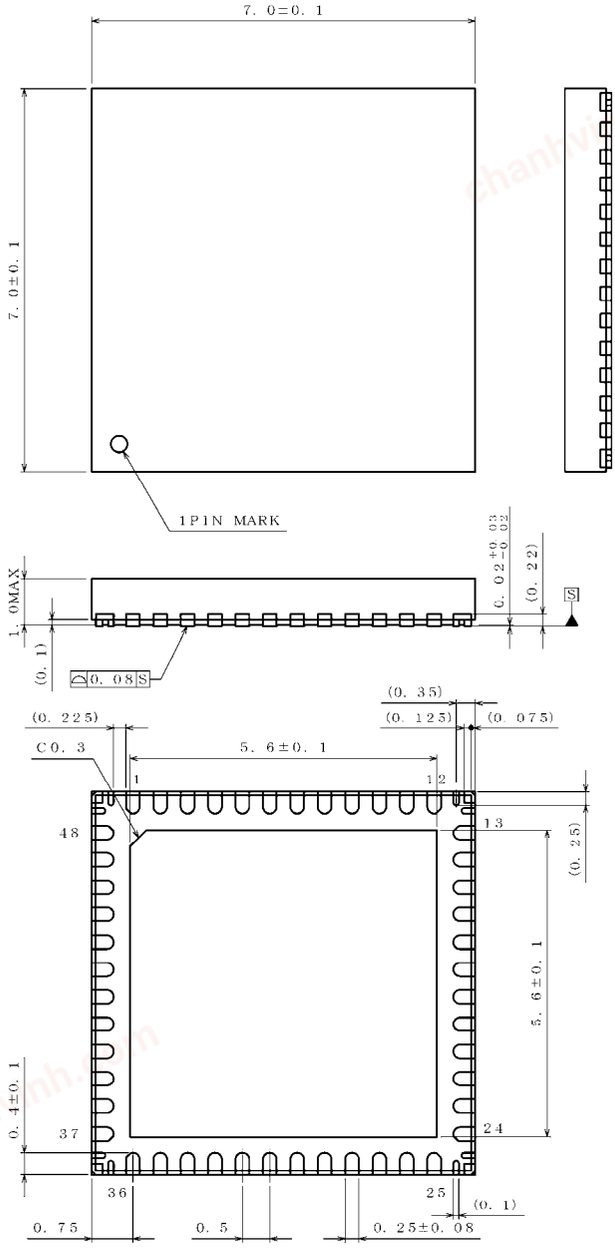


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Physical Dimension and Packing Information

Package Name	VQFN48FAV070



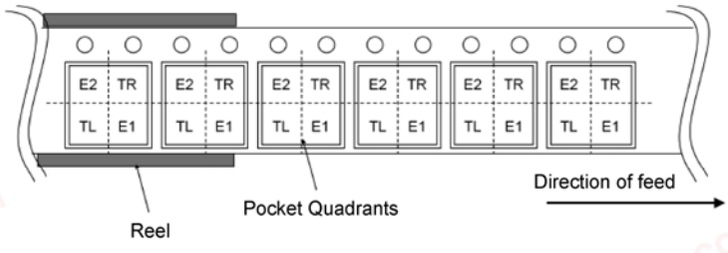
(UNIT : mm)

NOTE : Dimensions in ( ) for reference only.

PKG : VQFN48FAV070
Drawing No. EX405 5001 1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
10.May.2021	001	New Release

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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General Precaution

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