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XT Family of Ultra-low Phase Noise Quartz-based PLL Oscillators

XT Datasheet

Description

The XT devices are ultra-low phase noise quartz-based PLL oscillators supporting a large range of frequencies and output interface types.

The XT devices can be programmed to generate an output frequency from 15MHz to 2100MHz with a resolution as low as 1Hz accuracy. The configurability of this family of devices provides fast delivery times for both sample and large production orders.

Parts may be factory programmed for fixed frequency applications, or may be field configured using the I2C interface.

Features

- Output types: LVDS, LVPECL, CML
  - Frequency range: 15MHz to 2100MHz
- Output type: HCSL
  - Frequency range: 15MHz to 725MHz
- Supply voltage options: 1.8V, 2.5V, 3.3V
- Phase jitter (12kHz to 20MHz): 135 fs typical
- Package options:
  - 3.2 × 2.5 × 0.85 mm
- Operating temperature and stability:
  - -40°C to +85°C, ±3ppm
- Frequency stability for life:
  - -40°C to +85°C, ±13ppm

Pin Assignments

Figure 1. 3.2 × 2.5 mm Package – Top View

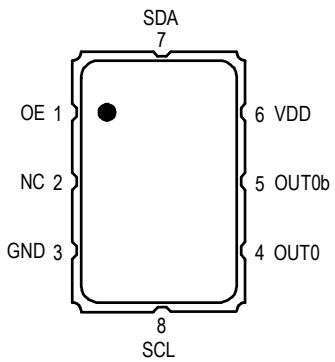


Table 1. Pin Descriptions

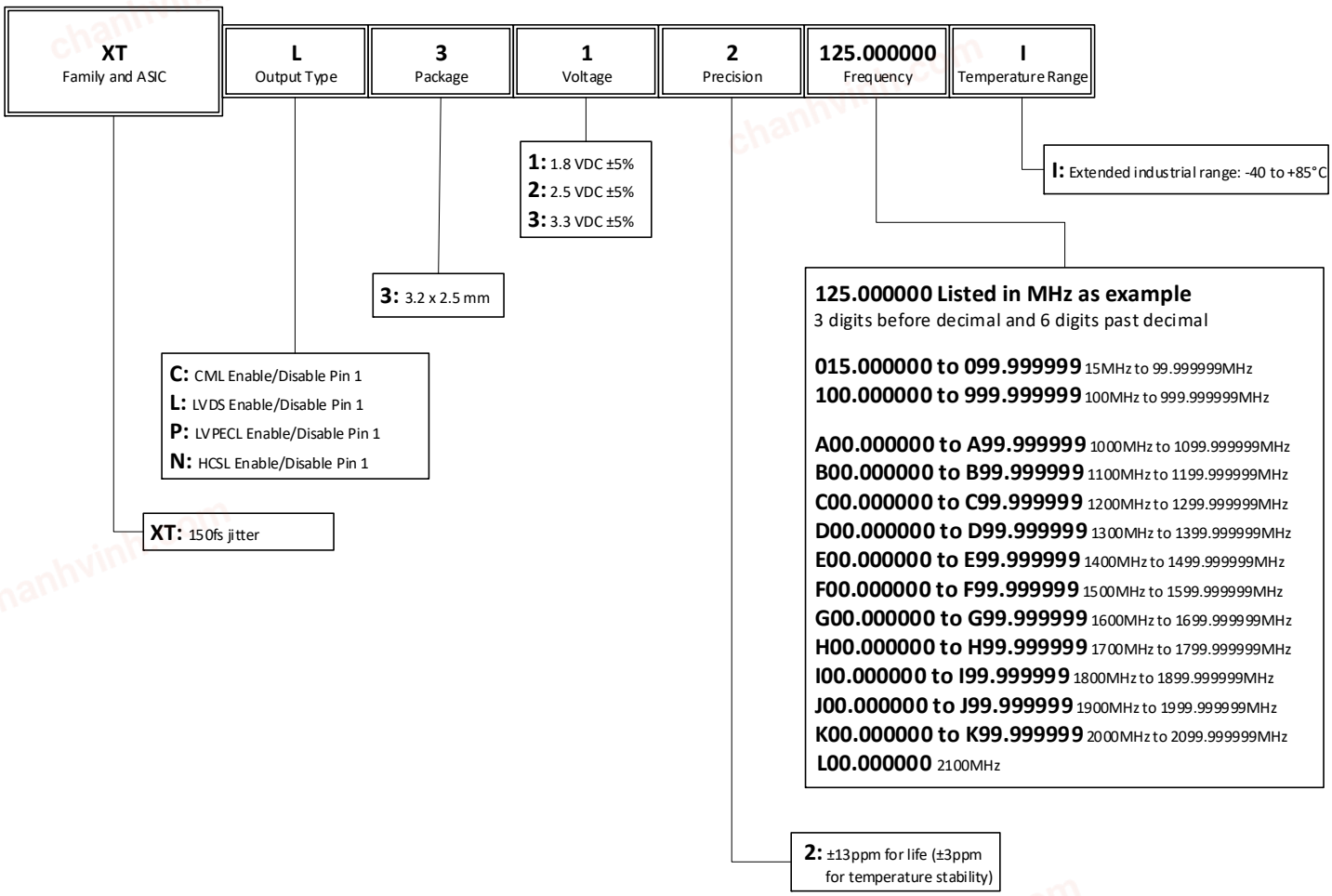
Pin #	Pin Name	Description
1	OE	Output Enable (0 = output disabled, pulled high internally)
2	NC	No connect
3	GND	Connect to ground
4	OUT0	Output
5	OUT0b	Complementary output
6	V_{DD}	Supply voltage
7	SDA [1]	Serial data
8	SCL [1]	Serial clock

[1] Pins 7 and 8 are no connect for non-I2C applications.

See Ordering Information for more details.

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Ordering Information



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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range. Thermal characteristics, in actual applications, should be assessed case by case to guarantee junction temperature does not exceed 125°C.

Table 2. Absolute Maximum Ratings

Item	Rating	
V_{DD}	-0.5V to +3.8V	
OE	-0.5V to +3.8V	
Storage Temperature	-55°C to 125°C	
Maximum Junction Temperature	125°C	
Theta J_A [1]	LNG8	131.47 °C/W
Theta J_B [1]		92.89 °C/W

[1] Thermal characteristics are based on simulation in standard condition.

ESD Compliance

Table 3. ESD Compliance

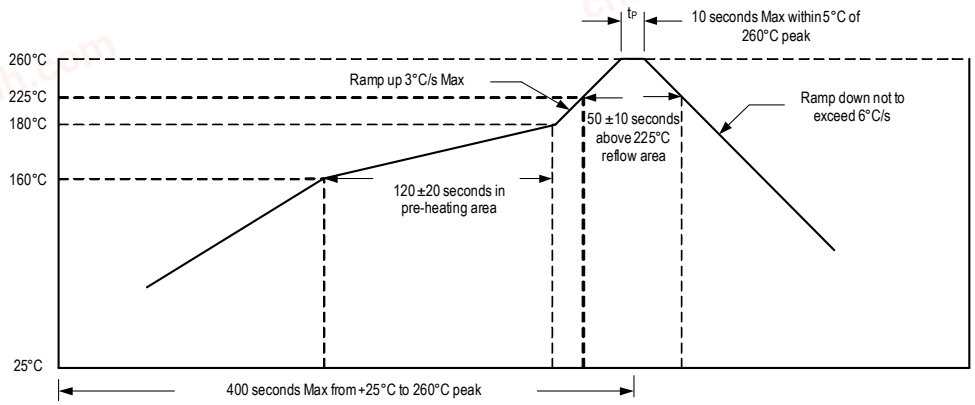
Human Body Model (HBM)	2000V

Mechanical Testing

Table 4. Mechanical Testing

Parameter	Test Method
Mechanical Shock	Half-sine wave with 0.3ms 3000G. X, Y, Z each direction 1 time.
Mechanical Vibration	Frequency: 10 to 55MHz amplitude: 1.5mm. Frequency: 55–2000Hz peak value: 20G. Duration time: 4H for each X, Y, Z axis; total 12hours.
High Temp Operating Life (HTOL)	1000 hours at 125°C (under power).
MSL Level 3	J-STD-020E, Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices, December 2014.

Solder Reflow Profile



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DC Electrical Characteristics

Table 5. 3.3V IDD DC Electrical Characteristics

V_{DD} = 3.3V ± 5%, T_A = -40°C to +85°C, typical at 156.25MHz.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Current Consumption	LVDS	15MHz to 400MHz.	—	59	67	mA
			400MHz to 2.1GHz.	—	—	85	
		LVPECL	15MHz to 212.5MHz.	—	84	94	
			212.5MHz to 400MHz.	—	—	110	
			212.5MHz to 2.1GHz.	—	—	110	
		HCSL	15MHz to 400MHz.	—	—	95	
			400MHz to 725MHz.	—	74	83	
		CML	15MHz to 2.1GHz.	—	54	61	

Table 6. 2.5V IDD DC Electrical Characteristics

V_{DD} = 2.5V ± 5%, T_A = -40°C to +85°C, typical at 156.25MHz.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Current Consumption	LVDS	15MHz to 400MHz.	—	59	66	mA
			400MHz to 2.1GHz.	—	—	85	
		LVPECL	15MHz to 156.25MHz.	—	84	94	
			156.25MHz to 400MHz.	—	—	110	
			400MHz to 2.1GHz.	—	—	110	
		HCSL	15MHz to 400MHz.	—	—	95	
			400MHz to 725MHz.	—	74	82	
		CML	15MHz to 2.1GHz.	—	54	61	

Table 7. 1.8V DD DC Electrical Characteristics

V_{DD} = 1.8V ± 5%, T_A = -40°C to +85°C, typical at 156.25MHz.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Current Consumption	LVDS	15MHz to 400MHz.	—	59	66	mA
			400MHz to 2.1GHz.	—	—	85	
		LVPECL	15MHz to 250MHz.	—	84	93	
			250MHz to 2.1GHz.	—	—	110	
		HCSL	15MHz to 400MHz.	—	—	95	
			400MHz to 725MHz.	—	74	81	
		CML	15MHz to 2.1GHz.	—	54	61	

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Table 8. LVCMOS DC Electrical Characteristics

V_{DD} = 1.8V, 2.5V, 3.3V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage (OE pin only)	V_{DD} = 1.8V, 2.5V, 3.3V ± 5%.	0.7 × V_{DD}	—	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage (OE pin only)	V_{DD} = 1.8V, 2.5V, 3.3V ± 5%.	GND - 0.3	—	0.3 × V_{DD}	V

Table 9. LVDS DC Electrical Characteristics

V_{DD} = 1.8V, 2.5V, 3.3V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	V_{DD} = 1.8V, 2.5V, 3.3V ± 5%.	0.30	0.44	0.60	V
V_{OS}	Output Offset Voltage	V_{DD} = 1.8V ± 5%	0.75	0.88	1.01	
		V_{DD} = 2.5V ± 5%	1.08	1.25	1.41	
		V_{DD} = 3.3V ± 5%	1.11	1.26	1.41	

Table 10. LVPECL DC Electrical Characteristics

V_{DD} = 1.8V, 2.5V, 3.3V ± 5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	V_{DD} = 1.8V ± 5%.	0.83	0.96	1.11	V
		V_{DD} = 2.5V ± 5%.	1.52	1.69	1.87	
		V_{DD} = 3.3V ± 5%.	2.28	2.49	2.72	
V_{OL}	Output Low Voltage	V_{DD} = 1.8V ± 5%.	0.19	0.30	0.42	
		V_{DD} = 2.5V ± 5%.	0.92	1.04	1.17	
		V_{DD} = 3.3V ± 5%.	1.68	1.84	2.01	

Table 11. HCSL DC Electrical Characteristics

V_{DD} = 1.8V, 2.5V, 3.3V ± 5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	V_{DD} = 1.8V ± 5%.	0.67	0.81	0.95	V
		V_{DD} = 2.5V ± 5%.	0.74	0.88	1.03	
		V_{DD} = 3.3V ± 5%.	0.78	0.92	1.07	
V_{OL}	Output Low Voltage	—	-0.06	0.07	0.20	

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Table 12. CML DC Electrical Characteristics

V_{DD} = 1.8V, 2.5V, 3.3V ± 5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	V_{DD} = 1.8V ± 5%.	1.61	1.76	1.91	V
		V_{DD} = 2.5V ± 5%.	2.33	2.46	2.59	
		V_{DD} = 3.3V ± 5%.	3.09	3.26	3.43	
V_{OL}	Output Low Voltage	V_{DD} = 1.8V ± 5%.	1.24	1.37	1.52	
		V_{DD} = 2.5V ± 5%.	1.95	2.06	2.17	
		V_{DD} = 3.3V ± 5%.	2.70	2.85	3.00	

Table 13. DC Electrical Characteristics – Leakage Current

V_{DD} = 1.8V, 2.5V, 3.3V ± 5%, T_A = -40°C to +85°C, typical at 156.25MHz.

Symbol	Parameter	Conditions	Input	Minimum	Typical	Maximum	Units
I_{IH}	Input Leakage High	V_{DD} = 3.3V ±5%.	OE	-5	0.8	5	µA
			SCLK	-5	1.4	5	
			SDATA	-5	1.4	5	
I_{IL}	Input Leakage Low	V_{DD} = 3.3V ±5%.	OE	-20	-17.4	-14	µA
			SCLK	-37	-33.5	-30	
			SDATA	-20	-17	-14	
I_{IH}	Input Leakage High	V_{DD} = 1.8V ±5%.	OE	-5	0.8	5	µA
			SCLK	-5	1.4	5	
			SDATA	-5	1.4	5	
I_{IL}	Input Leakage Low	V_{DD} = 1.8V ±5%.	OE	-11.5	-9.5	-7.5	µA
			SCLK	-20.8	-18.3	-15.7	
			SDATA	-11.5	-9.3	-7.5	

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AC Electrical Characteristics

Note for all AC Electrical Characteristics tables:

1. Installation should include a 0.01µF bypass capacitor placed between V_{DD} and GND to minimize power supply line noise.

Table 14. 3.3V AC Electrical Characteristics

V_{DD} = 3.3V ± 5%, T_A = -40°C to +85°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS, LVPECL, CML.		15	—	2100	MHz
		HCSL.		15	—	725	
	Frequency Stability	Temperature = -40°C to +85°C.		—	—	±3	PPM
	Frequency Tolerance (25°C)	T_A = 25°C.		—	—	±2	
	Aging (1 year)	T_A = 25°C.		—	—	±1	
	Aging (10 years)	T_A = 25°C.		—	—	±7	
	Output Load	LVDS.	Differential.	—	100	—	Ω
		LVPECL.	Thevenin equivalent.	—	50	—	
		HCSL.	To GND.	—	50	—	
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		—	5	—	ms
t_R	Output Rise Time	LVDS.	20% – 80%, 156.25MHz	—	299	400	ps
		LVPECL.		—	287	400	
		HCSL.		—	306	400	
		CML		—	301	400	
t_F	Output Fall Time	LVDS.	80% – 20%, 156.25MHz	—	279	400	ps
		LVPECL.		—	274	400	
		HCSL.		—	284	400	
		CML		—	279	400	
O_{DC}	Output Clock Duty Cycle	LVDS.	156.25MHz	45	—	55	%
		LVPECL.	156.25MHz	45	—	55	
		HCSL.	156.25MHz	45	—	55	
		CML	156.25MHz	45	—	55	
T_{OE}	Output Enable/Disable Time	—	—	—	1	—	ms

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Table 15. 2.5V AC Electrical Characteristics

V_{DD} = 2.5V ± 5%, T_A = -40°C to +85°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS, LVPECL, CML.		15	—	2100	MHz
		HCSL.		15	—	725	
	Frequency Stability	Temperature = -40°C to +85°C.		—	—	±3	ppm
	Frequency Tolerance (25°C)	T_A = 25°C.		—	—	±2	
	Aging (1 year)	T_A = 25°C.		—	—	±1	
	Aging (10 years)	T_A = 25°C.		—	—	±7	
	Output Load	LVDS.	Differential.	—	100	—	Ω
		LVPECL.	Thevenin equivalent.	—	50	—	
		HCSL.	To GND.	—	50	—	
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		—	5	—	ms
t_R	Output Rise Time	LVDS.	20% – 80%, 156.25MHz	—	303	400	ps
		LVPECL.		—	292	400	
		HCSL.		—	310	400	
		CML		—	304	400	
t_F	Output Fall Time	LVDS.	80% – 20%, 156.25MHz	—	282	400	ps
		LVPECL.		—	278	400	
		HCSL.		—	288	400	
		CML		—	281	400	
O_{DC}	Output Clock Duty Cycle	LVDS.	156.25MHz	45	—	55	%
		LVPECL.	156.25MHz	45	—	55	
		HCSL.	156.25MHz	45	—	55	
		CML	156.25MHz	45	—	55	
T_{OE}	Output Enable/Disable Time	—	—	—	1	—	ms

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Table 16. 1.8V AC Electrical Characteristics

V_{DD} = 1.8V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS, LVPECL, CML.		15	—	2100	MHz
		HCSL.		15	—	725	
	Frequency Stability	Temperature = -40°C to +85°C.		—	—	±3	PPM
	Frequency Tolerance (25°C)	T_A = 25°C.		—	—	±2	
	Aging (1 year)	T_A = 25°C.		—	—	±1	
	Aging (10 years)	T_A = 25°C.		—	—	±7	
	Output Load	LVDS.	Differential.	—	100	—	Ω
		LVPECL.	Thevenin equivalent.	—	50	—	
		HCSL.	To GND.	—	50	—	
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		—	5	—	ms
t_R	Output Rise Time	LVDS.	20% – 80%, 312.5MHz	—	300	450	ps
		LVPECL.		—	260	450	
		HCSL.		—	260	450	
		CML		—	270	450	
t_F	Output Fall Time	LVDS.	80% – 20%, 312.5MHz	—	280	450	ps
		LVPECL.		—	250	450	
		HCSL.		—	250	450	
		CML		—	270	450	
O_{DC}	Output Clock Duty Cycle	LVDS.	312.5MHz	45	—	55	%
		LVPECL.	312.5MHz	45	—	55	
		HCSL.	312.5MHz	45	—	55	
		CML	312.5MHz	45	—	55	
T_{OE}	Output Enable/Disable Time	—	—	—	1	—	ms

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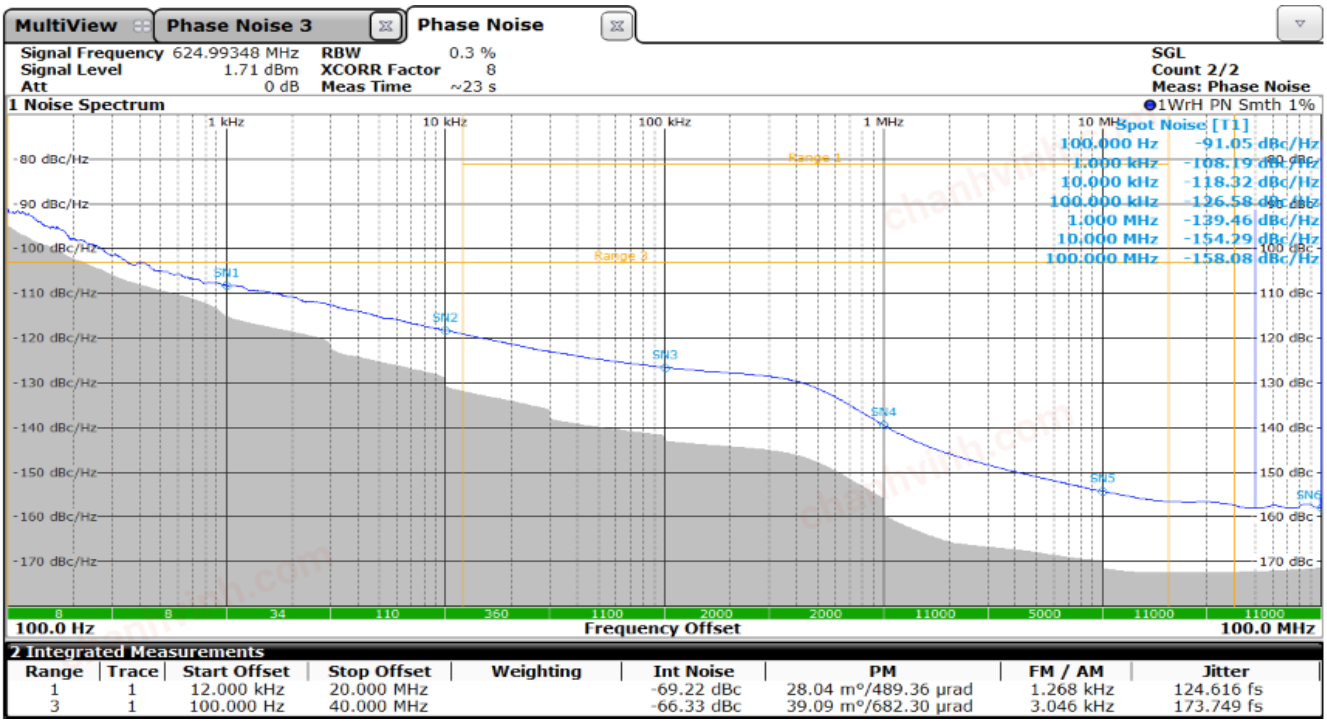
Table 17. Phase Jitter Characteristics

V_{DD} = 1.8V, 2.5V, 3.3V ± 5%, T_A = -40°C to +85°C.

Symbol	Parameter	Conditions	Typical (LVPECL)	Typical (LVDS)	Typical (CML)	Typical (HSCL)	Units
f_{JITTER}	Phase Jitter (12kHz – 20MHz)	312.50MHz	124	159	131	126	fsec
		625.00MHz	130	132	133	131	fsec
		644.53MHz	134	137	133	130	fsec
		779.215MHz	140	140	139	—	fsec
		818.991MHz	143	144	140	—	fsec
		822.128MHz	164	167	164	—	fsec
		840.759MHz	146	152	151	—	fsec
		1588.430MHz	147	144	143	—	fsec
		1681.518MHz	156	153	151	—	fsec
		1644.256MHz	157	154	155	—	fsec
		1637.982MHz	147	148	148	—	fsec

Output Phase Noise

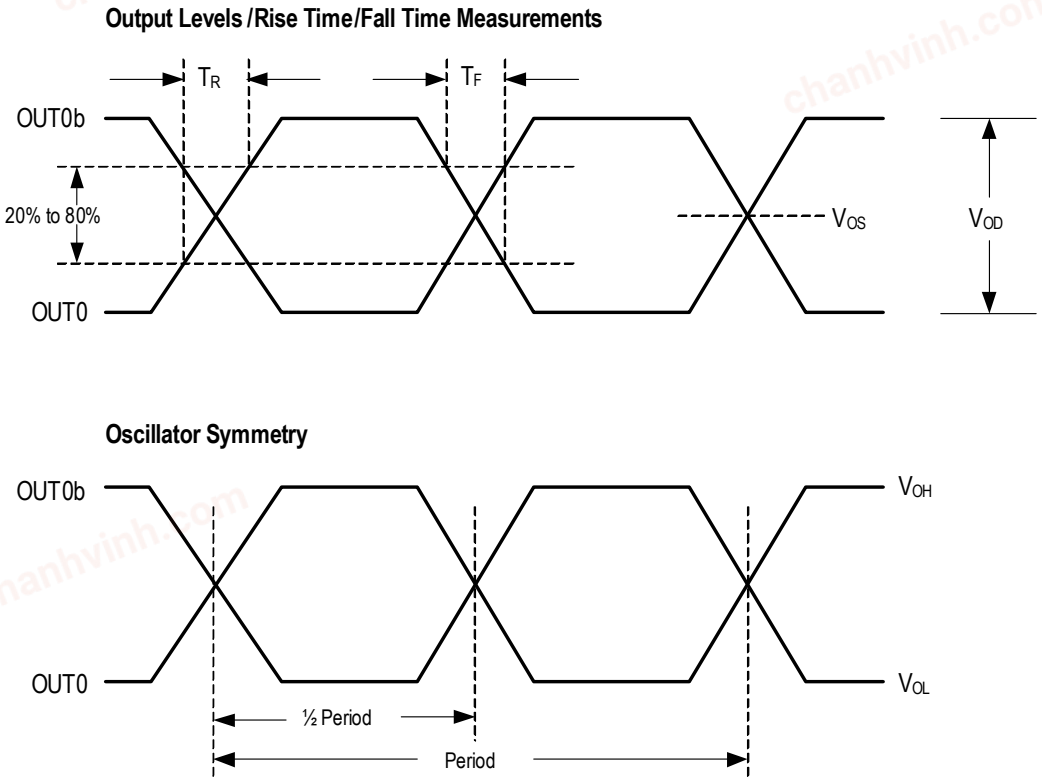
Figure 2. 625MHz LVDS Output



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Output Waveforms

Figure 3. LVDS/LVPECL/HCSL/CML Output Waveforms

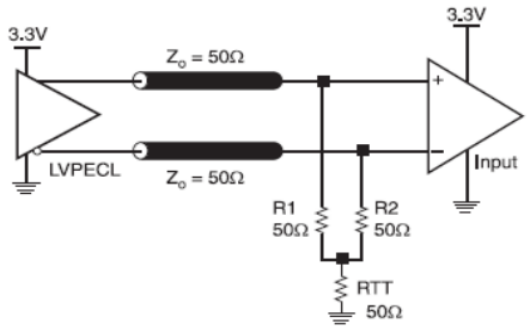


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3.3V LVPECL Output Termination

Figure 4 shows an example of termination for 3.3V LVPECL driver.

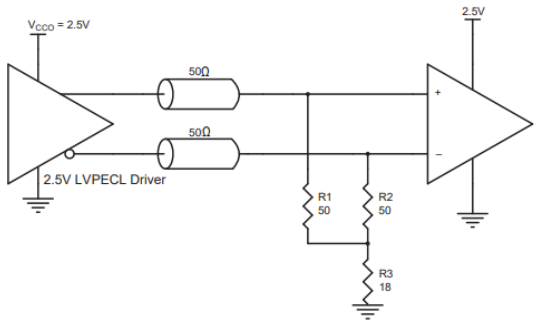
Figure 4. 3.3V LVPECL Driver Termination Example



2.5V LVPECL Output Termination

Figure 5 shows an example of termination for 2.5V LVPECL driver.

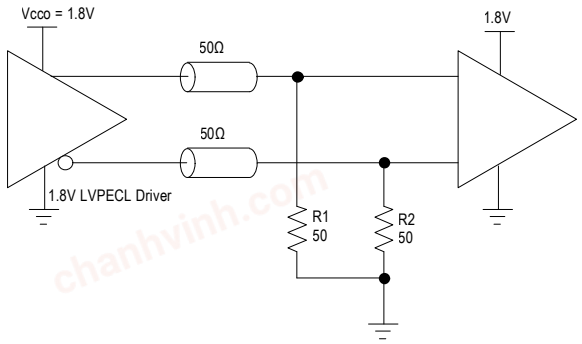
Figure 5. 2.5V LVPECL Driver Termination Example



1.8V LVPECL Output Termination

Figure 6 shows an example of termination for 1.8V LVPECL driver.

Figure 6. 1.8V LVPECL Driver Termination Example



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LVDS Output Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 7 can be used with either type of output structure. Figure 8, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 7. Standard LVDS Termination

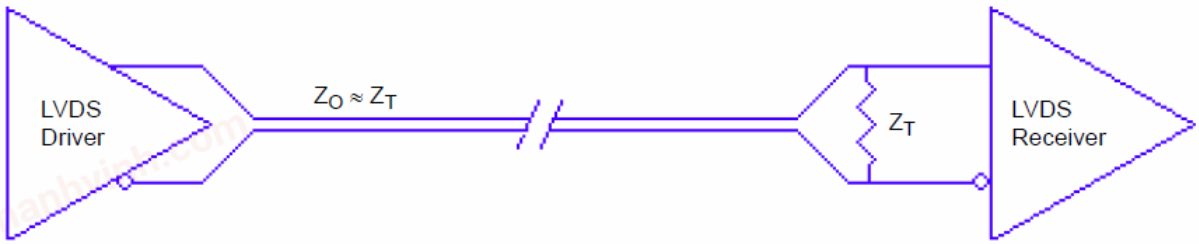
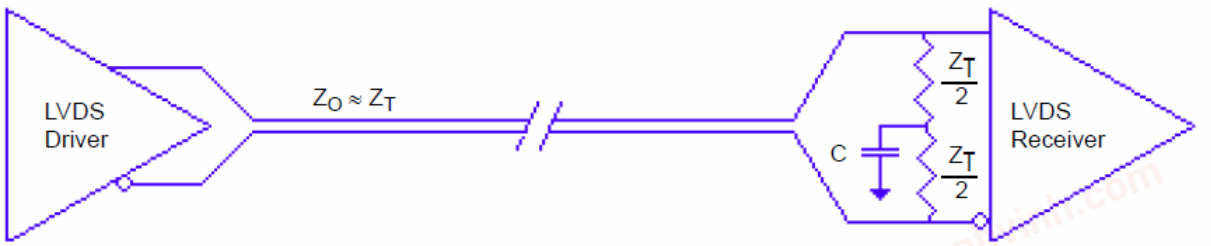


Figure 8. Optional LVDS Termination



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HCSL Output Termination

Figure 9 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential. Figure 10 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 9. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

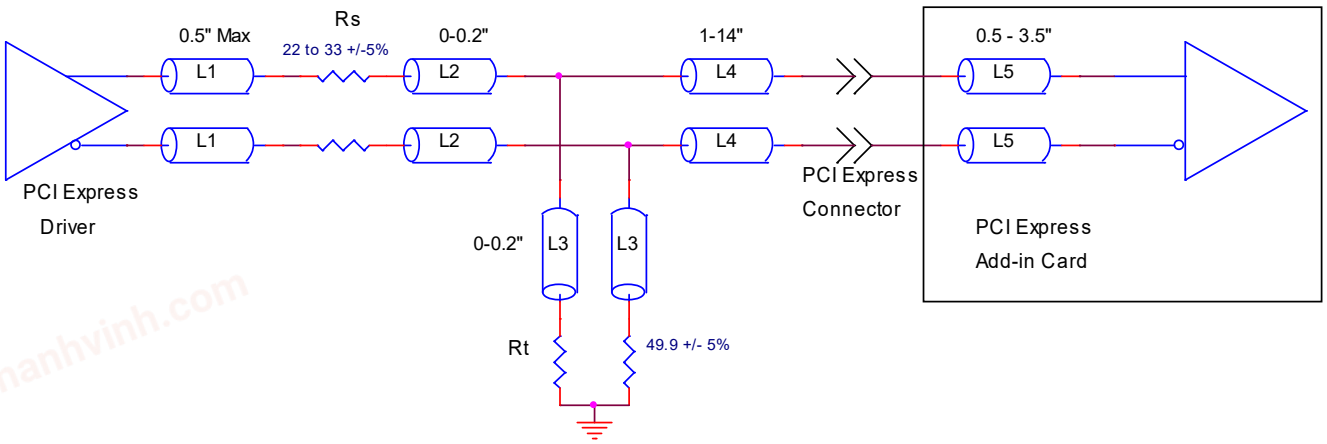
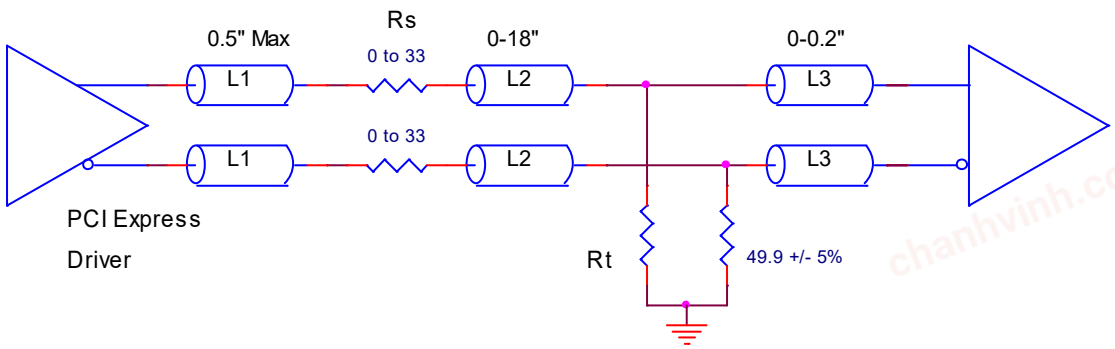


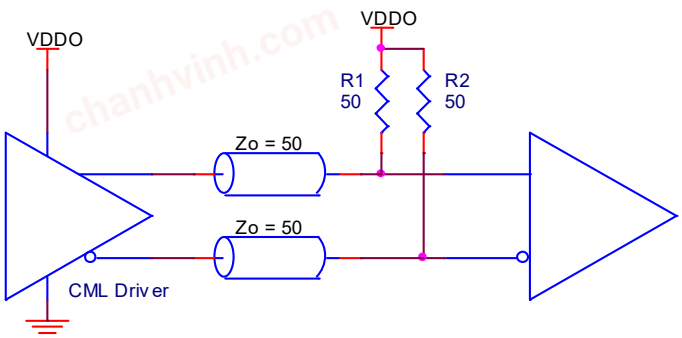
Figure 10. Recommended Termination (where a point-to-point connection can be used)



CML Output Termination

Figure 11 shows an example of the termination for a CML driver. In this example, the transmission line characteristic impedance is 50Ω. The R1 and R2 50Ω matched load terminations are pulled up to VDDO. The matched loads are located close to the receiver.

Figure 11. CML Driver Termination Example



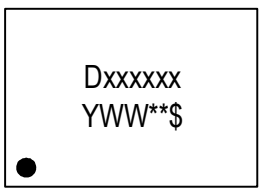
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Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram

Figure 12. Marking Configuration for the 3.2 × 2.5 mm (LNG8) Package (example based on XTL312625.000000I)



- Line 1 denotes the truncated part number as follows:
  - "D" = a combination of the 3rd digit (output type, e.g. "**L**") and the 5th digit (voltage supply, e.g. "**3**"), in accordance with the mapping key as follows:
    - C1 = A, C2 = B, C3 = C, **L1 = D**, L2 = E, L3 = F, N1 = G, N2 = H, N3 = J, P1 = K, P2 = L, P3 = M
  - "xxxxxx" = the first three digits to the left of the decimal point and the last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number. (e.g. 625000).
- Line 2 indicates the following:
  - "YWW" denotes the last digit of the year and week when the part was assembled.
  - "**" denotes the sequential lot number.
  - "$" denotes the mark location.

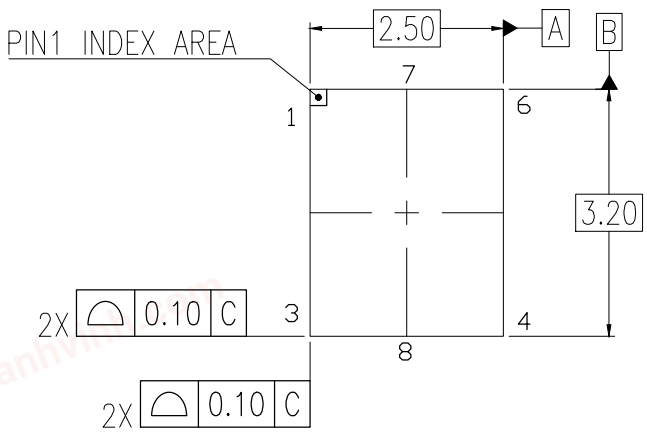
Revision History

Revision Date	Description of Change
April 8, 2021	Initial release.

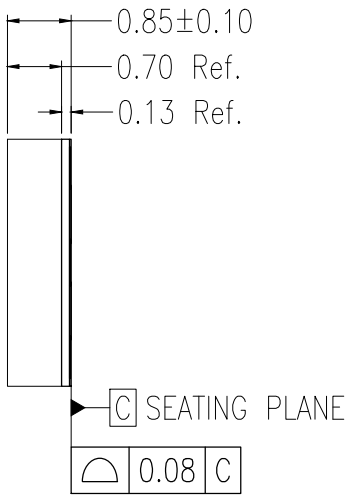
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8-LGA, Package Outline Drawing

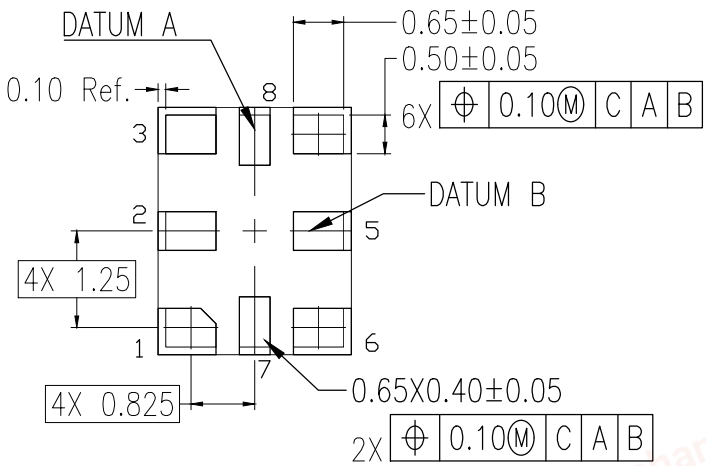
2.50 x 3.20 x 0.85 mm Body, 1.25mm Pitch



TOP VIEW



SIDE VIEW

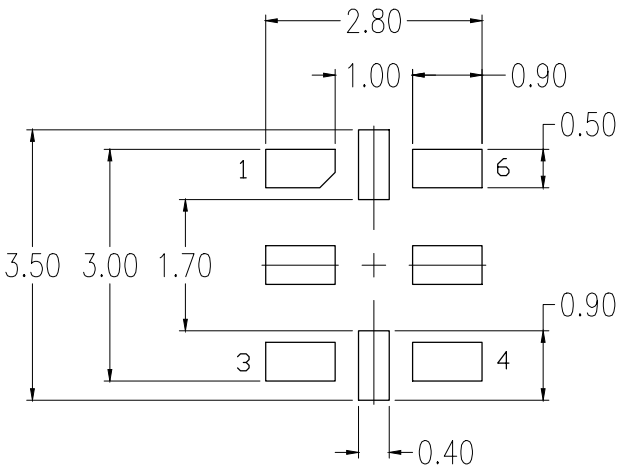


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5–2009
2. ALL DIMENSIONS ARE IN MILLIMETERS

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES
2. TOP DOWN VIEW. AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN
4. NSMD PATTERN ASSUMED

Package Revision History		
Date Created	Rev No.	Description
Nov. 12, 2019	00	Initial Release
Jun. 21, 2021	01	Update to Renesas Logo

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