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RENESAS

User's Manual

μPD179327 Subseries

8-Bit Single-Chip Microcontrollers

μPD179322
μPD179322A
μPD179324
μPD179324A
μPD179326
μPD179327
μPD78F9328

Document No. U16995EJ2V0UD00 (2nd edition)
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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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INTRODUCTION

Target Readers

This manual is intended for users who wish to understand the functions of the μPD179327 Subseries and to design and develop application systems and programs using these microcontrollers.

Target products:

- μPD179327 Subseries: μPD179322, 179322A, 179324, 179324A, 179326, 179327

The μPD78F9328 is used as the flash memory version of the μPD179327 Subseries.

Purpose

This manual is intended to give users an understanding of the functions described in the Organization below.

Organization

The μPD179327 Subseries User's Manual is divided into two parts: this manual and instructions (common to the 78K/0S Series).

μPD179327 Subseries User's Manual	78K/0S Series User's Manual Instructions
• Pin functions • Internal block functions • Interrupt functions • Other on-chip peripheral functions • Electrical specifications	• CPU function • Instruction set • Explanation of each instruction

How to Use This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

- To understand the functions in general:
  → Read this manual in the order of the contents. The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.
- How to interpret the register format:
  → Where the bit number is enclosed in angle brackets (<>), the bit name is reserved for the assembler and is defined as an sfr variable by the #pragma sfr directive for the C compiler.
- When you know a register name and want to confirm its details:
  → Read **APPENDIX B REGISTER INDEX**.
- To know the 78K/0S Series instruction function in detail:
  → Read **78K/0S Series Instructions User's Manual (U11047E)**.
- To know the μPD179322, 179322A, 179324, 179324A, 179326, and 179327 electrical specification in details:
  → Read **CHAPTER 18 ELECTRICAL SPECIFICATIONS (μPD179322, 179322A, 179324, 179324A, 179326, AND 179327)**.
- To know the μPD78F9328 electrical specification in details:
  → Read **CHAPTER 19 ELECTRICAL SPECIFICATIONS (μPD78F9328)**.

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Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD179327 Subseries User's Manual	This manual
78K/0S Series Instructions User's Manual	U11047E

Documents Related to Development Software Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U16656E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U16654E
	Language	U14872E
SM78K Series Ver. 2.52 System Simulator	Operation	U16768E
	External Part User Open Interface Specification	U15802E
ID78K0S-NS Ver. 2.52 Integrated Debugger	Operation	U16584E
PM plus Ver.5.10		U16569E

Document Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
IE-789468-NS-EM1 Emulation Board	To be prepared

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Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products and Packages -	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (http://www.necel.com/pkg/en/mount/index.html)

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CHAPTER 1 GENERAL

1.1 Features

- ROM and RAM capacities

Item / Part Number	Program Memory (ROM)		Data Memory	
			Internal High-Speed RAM	LCD Display RAM
μPD179322	Mask ROM	4 KB	256 bytes	24 × 4 bits
μPD179322A				
μPD179324		8 KB		
μPD179324A				
μPD179326		16 KB	512 bytes	
μPD179327		24 KB		
μPD78F9328	Flash memory	32 KB		

- Minimum instruction execution time can be changed from high-speed (0.4 μs: @ 5.0 MHz operation with main system clock) to ultra-low-speed (122 μs: @ 32.768 kHz operation with subsystem clock)
- I/O ports: 21
- Serial interface (3-wire serial I/O mode): 1 channel
- Timer: 4 channels
  - 8-bit timer: 2 channels
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- LCD controller/driver
  Segment signals: 24, common signals: 4
- Vectored interrupt sources
  - Mask ROM versions: 8
  - Flash memory version: 9
- On-chip power-on clear circuit (mask option for mask ROM versions)
- Power supply voltage
  - Mask ROM versions: V_{DD} = 1.8 to 3.6 V[Note]
  - Flash memory version: V_{DD} = 1.8 to 5.5 V[Note]
- Operating ambient temperature: T_A = –40 to +85°C

Note For mask ROM version when the use of the POC circuit is selected or for flash memory versions, the minimum value of the operation power supply voltage is the POC detection voltage (1.9±0.1 V).

1.2 Applications

Remote controllers for air conditioners, AV equipments, and water flow (in toilets, baths, etc.), etc.

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1.3 Ordering Information

Part Number	Package	Internal ROM
μPD179322GB-×××-8ET	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179322AGB-×××-8ET	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179324GB-×××-8ET	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179324AGB-×××-8ET	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179326GB-×××-8ET	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179327GB-×××-8ET	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179322GB-×××-8ET-A	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179322AGB-×××-8ET-A	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179324GB-×××-8ET-A	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179324AGB-×××-8ET-A	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179326GB-×××-8ET-A	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD179327GB-×××-8ET-A	52-pin plastic LQFP (10 × 10)	Mask ROM
μPD78F9328GB-8ET	52-pin plastic LQFP (10 × 10)	Flash memory
μPD78F9328GB-8ET-A	52-pin plastic LQFP (10 × 10)	Flash memory

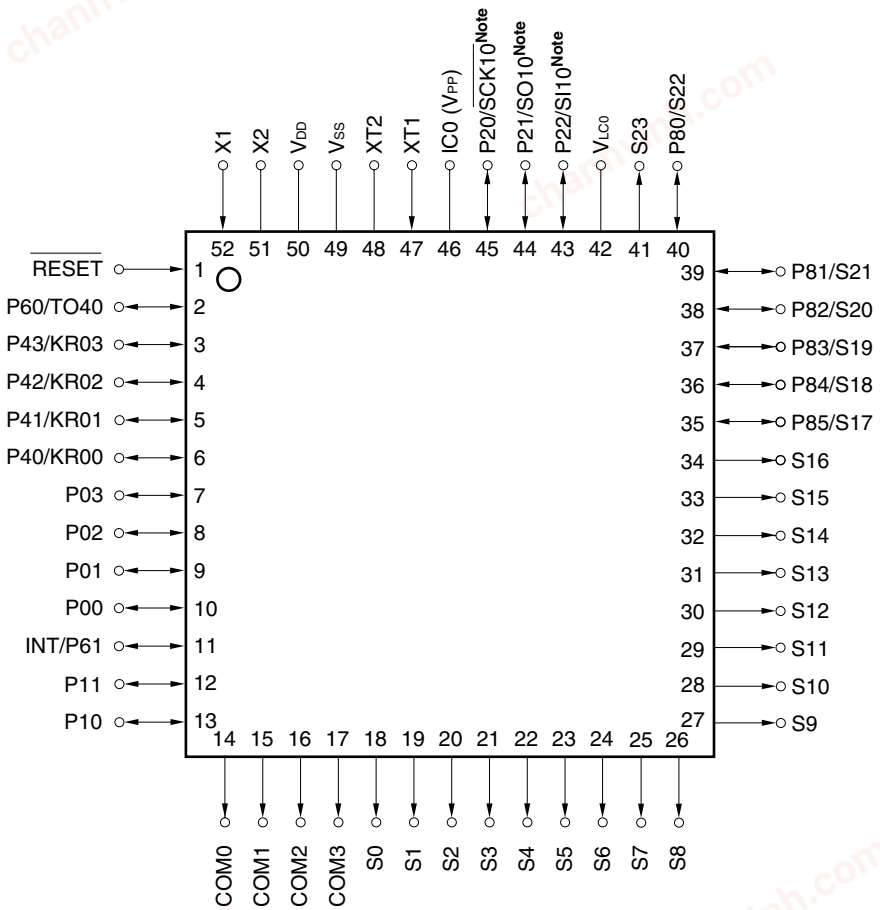
Remarks 1. ××× indicates ROM code suffix.

2. Products that have the part numbers suffixed by "-A" are lead-free products.

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1.4 Pin Configuration (Top View)

52-pin plastic LQFP (10 × 10)



Note $\overline{\text{SCK10}}$, SO10, and SI10 are provided in the μPD78F9328 only.

Caution Connect the IC0 (Internally Connected) pin directly to V_{SS}.

Remark The parenthesized values apply to the μPD78F9328.

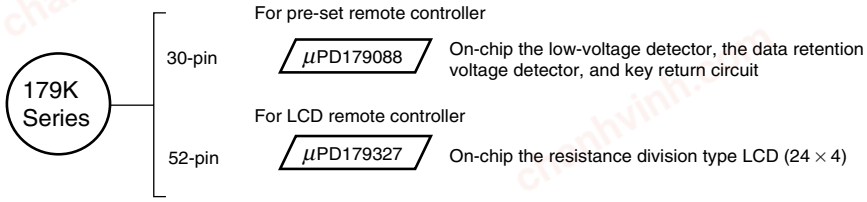
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COM0 to COM3:	Common output	S0 to S23:	Segment output
IC0:	Internally connected	$\overline{\text{SCK10}}$:	Serial clock input/output
INT:	Interrupt from peripherals	SI10:	Serial data input
KR00 to KR03:	Key return	SO10:	Serial data output
P00 to P03:	Port 0	TO40:	Timer output
P10, P11:	Port 1	V_{DD}:	Power supply
P20 to P22:	Port 2	V_{LC0}:	Power supply for LCD
P40 to P43:	Port 4	V_{PP}:	Programming power supply
P60, P61:	Port 6	V_{SS}:	Ground
P80 to P85:	Port 8	X1, X2:	Crystal (main system clock)
$\overline{\text{RESET}}$:	Reset	XT1, XT2:	Crystal (subsystem clock)

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1.5 179K Series Lineup

The products in the 179K Series are listed below. The names enclosed in boxes are subseries names.

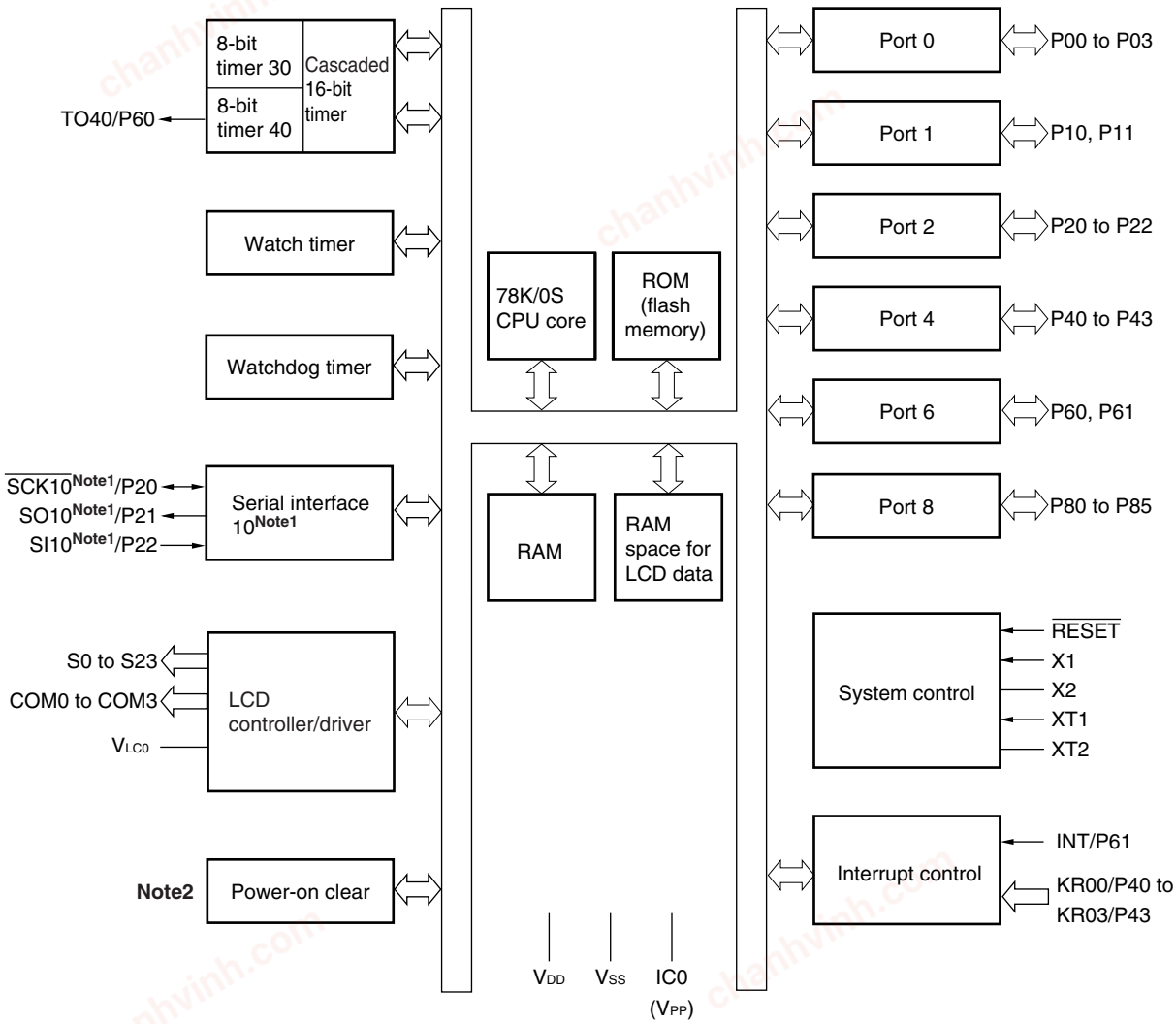


The major differences between subseries are shown below.

Subseries \ Function		ROM Capacity (Bytes)	Timer				I/O	V_{DD} MIN.Value	Remarks
			8-Bit	16-Bit	Watch	WDT			
For pre-set remote controller	μPD179088	16 K-32 k	3 ch	1 ch	1 ch	1 ch	24	1.8 V	–
For LCD remote controller	μPD179327	4 K to 24 K	2 ch	–	1 ch	1 ch	21	1.8 V	–

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1.6 Block Diagram



Notes 1. The serial interface 10 is provided in the μPD78F9328 only.

2. Only when use of the POC circuit is selected by a mask option in the case of mask ROM versions (μPD179322, 179322A, 179324, 179324A, 179326, and 179327).

Remarks 1. The internal ROM and RAM capacities vary depending on the product.

2. The parenthesized values apply to the μPD78F9328.

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1.7 Overview of Functions

Item \ Part Number		μPD179327 Subseries				μPD789327 Subseries
		μPD179322 μPD179322A	μPD179324 μPD179324A	μPD179326	μPD179327	μPD78F9328
Internal memory	ROM	Mask ROM				Flash memory
		4 KB	8 KB	16 KB	24 KB	32 KB
	High-speed RAM	256 bytes		512 bytes		
	LCD display RAM	24 × 4 bits				
Main system clock (oscillation frequency)		Ceramic/crystal oscillation (1.0 to 5.0 MHz)				
Subsystem clock (oscillation frequency)		Crystal oscillation (32.768 kHz)				
Minimum instruction execution time		0.4 μs/1.6 μs (@ 5.0 MHz operation with main system clock)				
		122 μs (@ 32.768 kHz operation with subsystem clock)				
General-purpose registers		8 bits × 8 registers				
Instruction set		• 16-bit operations • Bit manipulations (such as set, reset, and test)				
I/O ports		CMOS I/O: 21 Note 1				
Timers		• 8-bit timer: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel				
Timer outputs		1				
Serial interface		–				3-wire serial I/O mode: 1 channel
LCD controller/driver		• Segment signal outputs: 24 Note 1 • Common signal outputs: 4 • Mode: Static mode and 1/3 bias mode				
Vectored interrupt sources	Maskable	Internal: 5 external: 2				Internal: 6 external: 2
	Non-maskable	Internal: 1				
Reset		• Reset by $\overline{\text{RESET}}$ input • Internal reset by watchdog timer • Reset by power-on-clear circuit Note 2				
Power supply voltage		V_{DD} = 1.8 to 3.6 V Note 3				V_{DD} = 1.8 to 5.5 V Note 3
Operating ambient temperature		T_A = −40 to +85°C				
Package		52-pin plastic LQFP (10 × 10)				

Notes 1. Six among these pins are used to select either port function or LCD segment output via the port function register.

2. For mask ROM versions (μPD179322, 179322A, 179324, 179324A, 179326, 179327), this is available only when the use of POC circuit is selected by mask option.

3. For mask ROM versions when the use of the POC circuit is selected or for flash memory versions, the minimum value of the operation power supply voltage is the POC detection voltage (1.9 ±0.1 V).

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An outline of the timer is shown below.

		8-Bit Timer 30	8-Bit Timer 40	Watch Timer	Watchdog Timer
Operation mode	Interval timer	1 channel	1 channel	1 channel[Note 1]	1 channel[Note 2]
	External event counter	–	–	–	–
Function	Timer outputs	–	1 output	–	–
	Square-wave outputs	–	1 output	–	–
	Capture	–	–	–	–
	Interrupt sources	1	1	2	2

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer has the watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or interval timer function.

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CHAPTER 2 PIN FUNCTIONS

2.1 List of Pin Functions

(1) Port pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	Input/ output	Port 0. This is a 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified in port units using pull-up resistor option register 0 (PU0).	Input	–
P10, P11	Input/ output	Port 1. This is a 2-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified in port units using pull-up resistor option register 0 (PU0).	Input	–
P20	Input/ output	Port 2. This is a 3-bit I/O port. Input/output can be specified in 1-bit units. On-chip pull-up resistors can be specified in 1-bit units using pull-up resistor option register 2 (PUB2).	Input	$\overline{\text{SCK10}}$[Note]
P21				SO10[Note]
P22				SI10[Note]
P40 to P43	Input/ output	Port 4. This is a 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified in port units using pull-up resistor option register 0 (PU0), or key return mode register 00 (KRM00).	Input	KR00 to KR03
P60	Input/ output	Port 6. This is a 2-bit I/O port. Input/output can be specified in 1-bit units.	Input	TO40
P61				INT
P80 to P85	Input/ output	Port 8. This is a 6-bit I/O port. Input/output can be specified in 1-bit units.	Input	S22 to S17

Note $\overline{\text{SCK10}}$, SO10, and SI10 are provided in μPD78F9328 only.

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(2) Non-port pins

Pin Name	I/O	Function	After Reset	Alternate Function
INT	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P61
KR00 to KR03	Input	Key return signal detection	Input	P40 to P43
TO40	Output	8-bit timer 40 output	Input	P60
$\overline{\text{SCK10}}$ Note	Input/ output	Serial clock input/output of serial interface 10	Input	P20
SI10 Note	Input	Serial data input of serial interface 10	Input	P22
SO10 Note	Output	Serial data output of serial interface 10	Input	P21
S0 to S16	Output	LCD controller/driver segment signal outputs	Low-level output	–
S17 to S22			Input	P85 to P80
S23			Low-level output	–
COM0 to COM3	Output	LCD controller/driver common signal outputs	Low-level output	–
V_{LC0}	–	LCD drive voltage	–	–
X1	Input	Connecting crystal/ceramic resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–
IC0	–	Internally connected. Connect directly to V_{SS}.	–	–
V_{PP}	–	Sets flash memory programming mode. Applies high voltage when a program is written or verified.	–	–

Note $\overline{\text{SCK10}}$, SO10, and SI10 are provided in μPD78F9328 only.

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2.2 Description of Pin Functions

2.2.1 P00 to P03 (Port 0)

These pins constitute a 4-bit I/O port and can be set in the input or output port mode in 1-bit units by port mode register 0 (PM0). When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0) in port units.

2.2.2 P10, P11 (Port 1)

These pins constitute a 2-bit I/O port and can be set in the input or output port mode in 1-bit units by port mode register 1 (PM1). When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0) in port units.

2.2.3 P20 to P22 (Port 2)

These pins constitute a 3-bit I/O port. In addition, these pins enable serial interface data I/O and clock I/O in μPD78F9328 only.

Port 2 can be specified in the following operation modes in 1-bit units.

(1) Port mode

In this mode, P20 to P22 function as a 3-bit I/O port. Port 2 can be set in the input or output port mode in 1-bit units by port mode register 2 (PM2). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register B2 (PUB2) in 1-bit units.

(2) Control mode

In this mode, P20 to P22 function as the serial interface data I/O and clock I/O.

(a) SI10 Note, SO10 Note

These are the serial data I/O pins of the serial interface.

(b) $\overline{\text{SCK10}}$ Note

This is the serial clock I/O pin of the serial interface.

Note $\overline{\text{SCK10}}$, SO10, and SI10 are provided in μPD78F9328 only.

Caution When using P20 to P22 as serial interface pins, the I/O mode and output latch must be set according to the functions to be used. For the details of the setting, refer to Table 9-2 Settings of Serial Interface 10 Operating Mode.

2.2.4 P40 to P43 (Port 4)

These pins constitute a 4-bit I/O port. In addition, they also function as key return signal detection.

Port 4 can be specified in the following operation mode in 1-bit units.

(1) Port mode

In this mode, port 4 functions as a 4-bit I/O port. Port 4 can be set in the input or output port mode in 1-bit units by port mode register 4 (PM4). When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0) or key return mode register 00 (KRM00) in port units.

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(2) Control mode

In this mode, the pins function as key return signal detection (KR00 to KR03).

2.2.5 P60, P61 (Port 6)

These pins constitute a 2-bit I/O port. In addition, they also function as timer output and external interrupt input. Port 6 can be specified in the following operation mode in 1-bit units.

(1) Port mode

In this mode, port 6 functions as a 2-bit I/O port. Port 6 can be set in the input or output port mode in 1-bit units by port mode register 6 (PM6).

(2) Control mode

In this mode, the pins function as timer output and external interrupt input.

(a) TO40

This is the timer output pin to timer 40.

(b) INT

This is the external interrupt input pin for which valid edges (rising edge, falling edge, or both rising and falling edges) can be specified.

2.2.6 P80 to P85 (Port 8)

These pins constitute a 6-bit I/O port. In addition, they also function as LCD controller/driver segment signal output. Port 8 can be specified in the following operation mode in 1-bit units by port function register 8 (PF8).

(1) Port mode

In this mode, port 8 functions as a 6-bit I/O port. Port 8 can be set in the input or output port mode in 1-bit units by port mode register 8 (PM8).

(2) Control mode

In this mode, the pins function as LCD controller/driver segment signal output (S17 to S22).

2.2.7 S0 to S16, S23

These pins are segment signal output pins for the LCD controller/driver.

2.2.8 COM0 to COM3

These pins are common signal output pins for the LCD controller/driver.

2.2.9 V_{LC0}

This pin is the power supply voltage pin to drive the LCD.

2.2.10 $\overline{\text{RESET}}$

This pin inputs an active-low system reset signal.

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2.2.11 X1, X2

These pins are used to connect a crystal/ceramic resonator for main system clock oscillation.

To supply an external clock, input the clock to X1 and input the inverted signal to X2.

2.2.12 XT1, XT2

These pins are used to connect a crystal resonator for subsystem clock oscillation.

To supply an external clock, input the clock to XT1 and input the inverted signal to XT2.

2.2.13 V_{DD}

This is the positive power supply pin.

2.2.14 V_{SS}

This is the ground pin.

2.2.15 V_{PP} (μPD78F9328 only)

A high voltage should be applied to this pin when the flash memory programming mode is set and when the program is written or verified.

Perform either of the following.

- Independently connect a 10 kΩ pull-down resistor to V_{PP}.
- Use the jumper on the board to connect V_{PP} to the dedicated flash programmer or V_{SS}, in programming mode or normal operation mode, respectively.

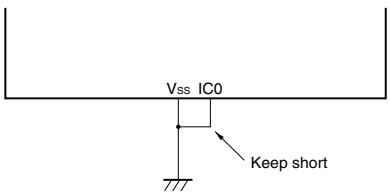
If the wiring between the V_{PP} and V_{SS} pins is long or external noise is superimposed on the V_{PP} pin, the userprogram may not run correctly.

2.2.16 IC0 (mask ROM version only)

The IC0 (Internally Connected) pin is used to set the μPD179322, 179322A, 179324, 179324A, 179326, and 179327 in the test mode before shipment. In the normal operation mode, directly connect this pin to the V_{SS} pin with as short a wiring length as possible.

If a potential difference is generated between the IC0 pin and V_{SS} pin due to a long wiring length, or an external noise superimposed on the IC0 pin, the user program may not run correctly.

- Directly connect the IC0 pin to the V_{SS} pin.



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2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output circuit configuration of each type, see Figure 2-1.

Table 2-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

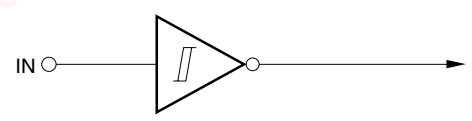
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P03	5-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P10, P11			
P20/$\overline{SCK10}$ Note1	8-A		
P21/SO10 Note1			
P22/SI10 Note1			
P40/KR00 to P43/KR03			
P60/TO40	5		
P61/INT	8		Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P80/S22 to P85/S17	17-N		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
S0 to S16, S23	17-D	Output	Leave open.
COM0 to COM3	18-B		
V_{LC0}	–	–	Connect to V_{DD} Note2.
XT1		Input	Connect to V_{SS}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
IC0 (mask ROM version)	–	–	Connect directly to V_{SS}.
V_{PP} (μPD78F9328)			Independently connect V_{PP} to a 10 kΩ pull-down resistor or directly connect to V_{SS}.

Notes 1. $\overline{SCK10}$, SO10, and SI10 are provided in μPD78F9328 only.

2. The current flows from V_{LC0} to V_{SS} via the LCD division resistors.

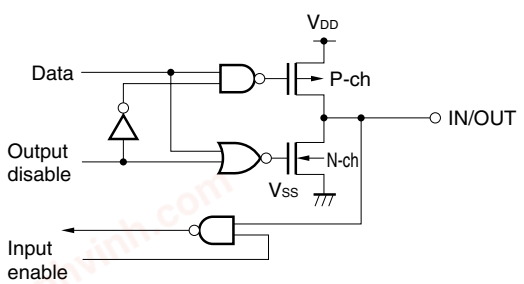
Figure 2-1. I/O Circuit Type (1/2)

Type 2



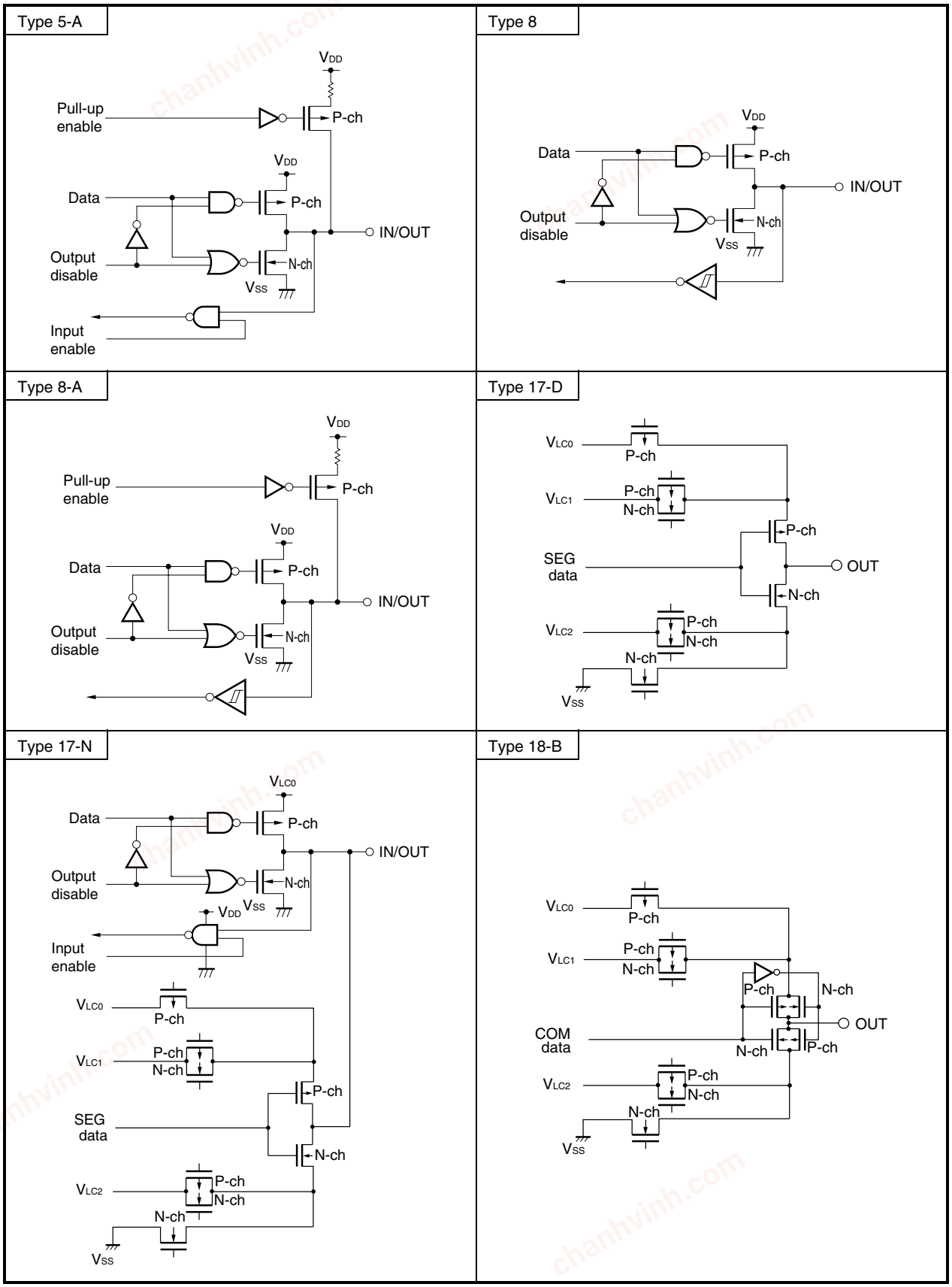
Schmitt-triggered input with hysteresis characteristics.

Type 5



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Figure 2-1. I/O Circuit Type (2/2)



Remark V_{LC1}: $V_{LC0} \times 2/3$, V_{LC2}: $V_{LC0}/3$

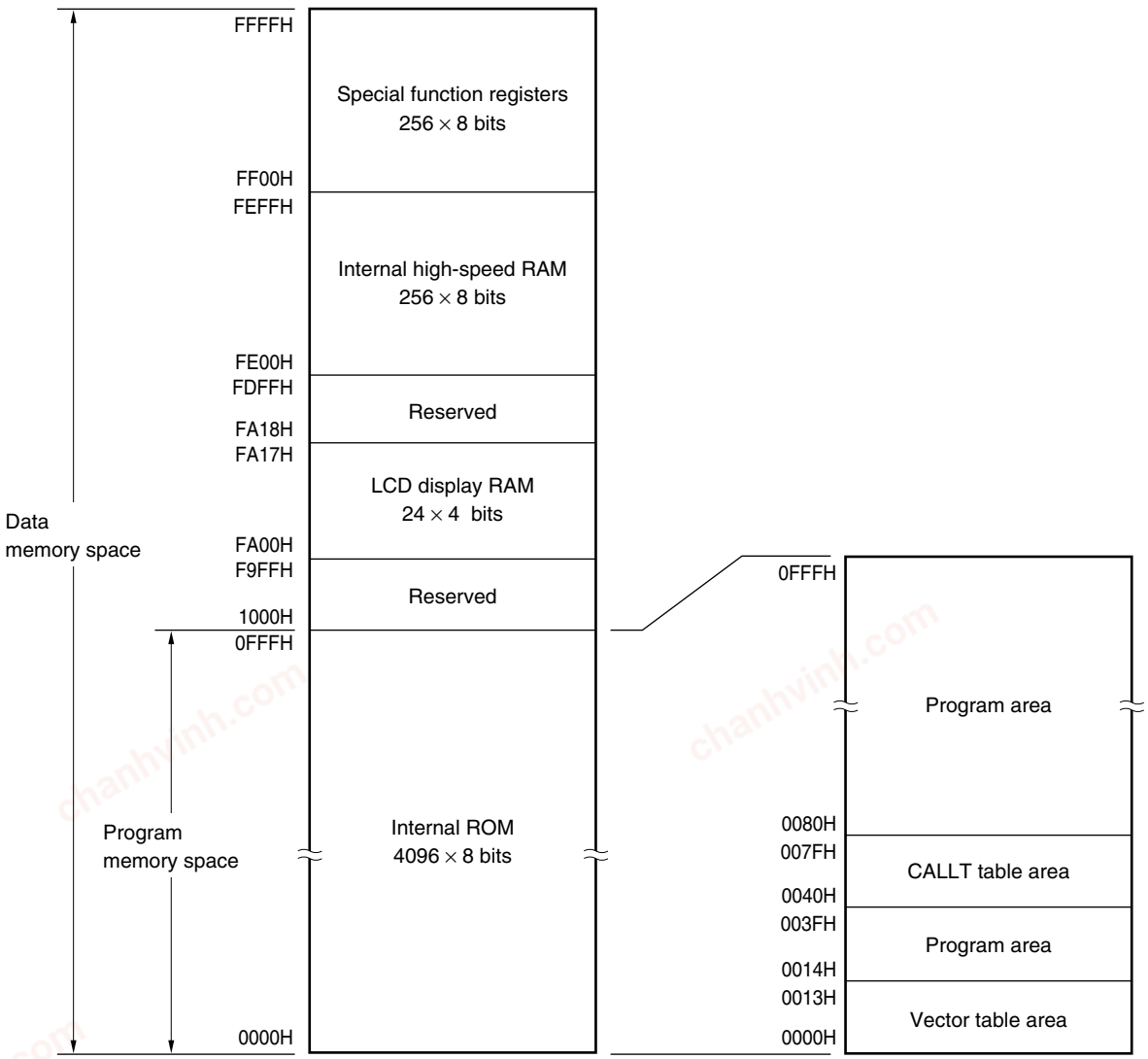
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CHAPTER 3 CPU ARCHITECTURE

3.1 Memory Space

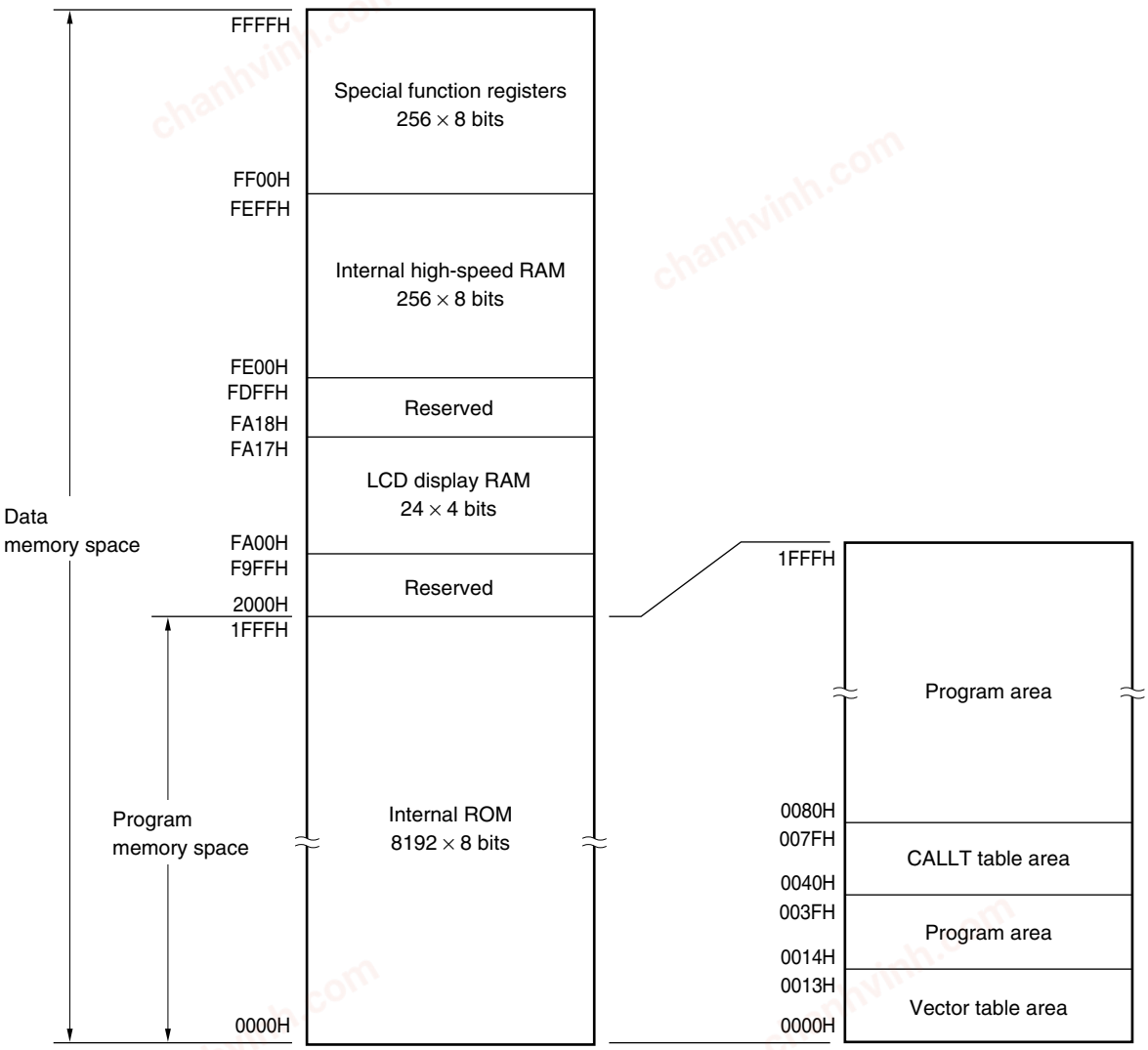
The μPD179327 Subseries can access 64 KB of memory space. Figures 3-1 through 3-5 show the memory maps.

Figure 3-1. Memory Map (μPD179322 and 179322A)



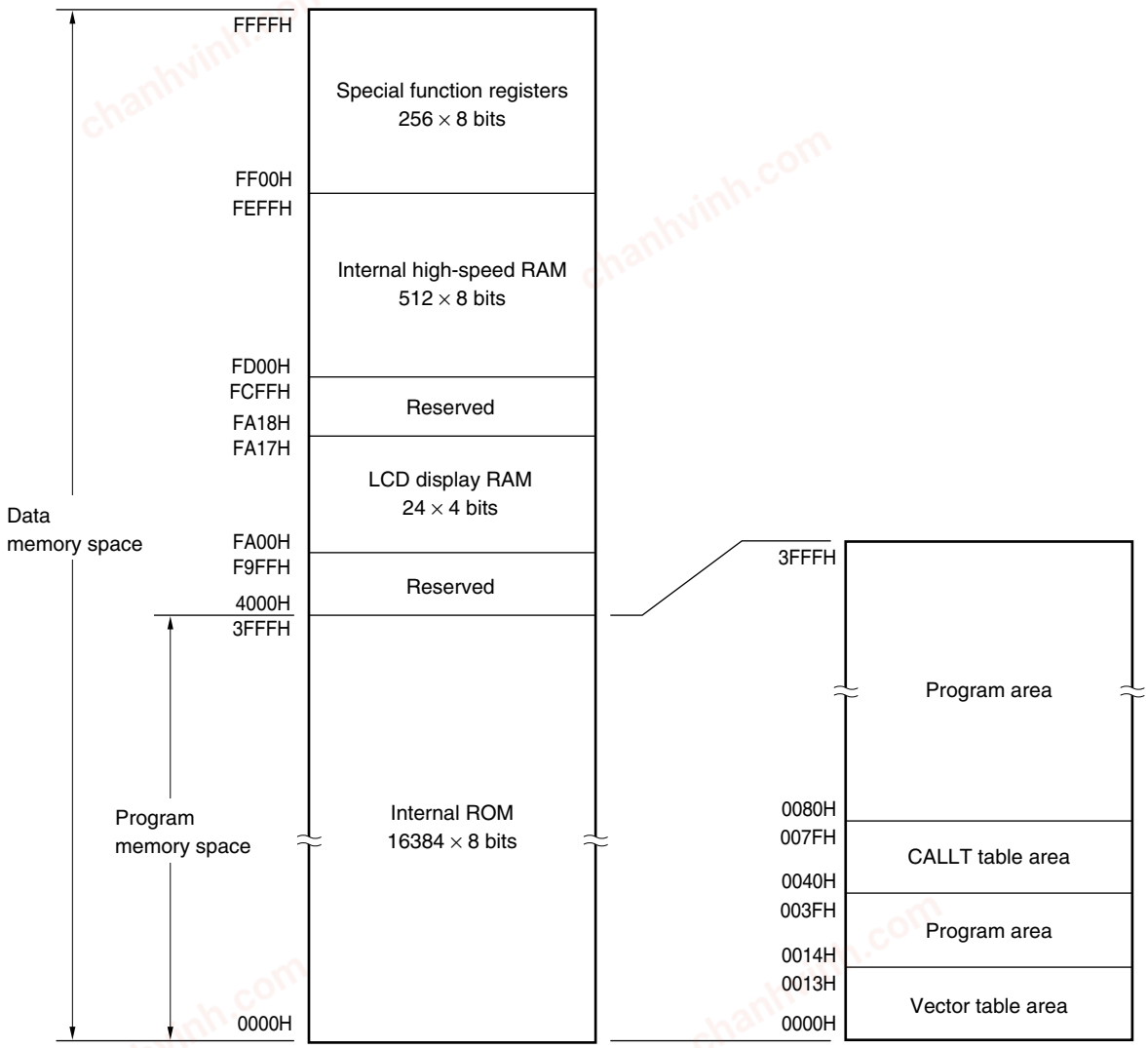
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Figure 3-2. Memory Map (μPD179324 and 179324A)



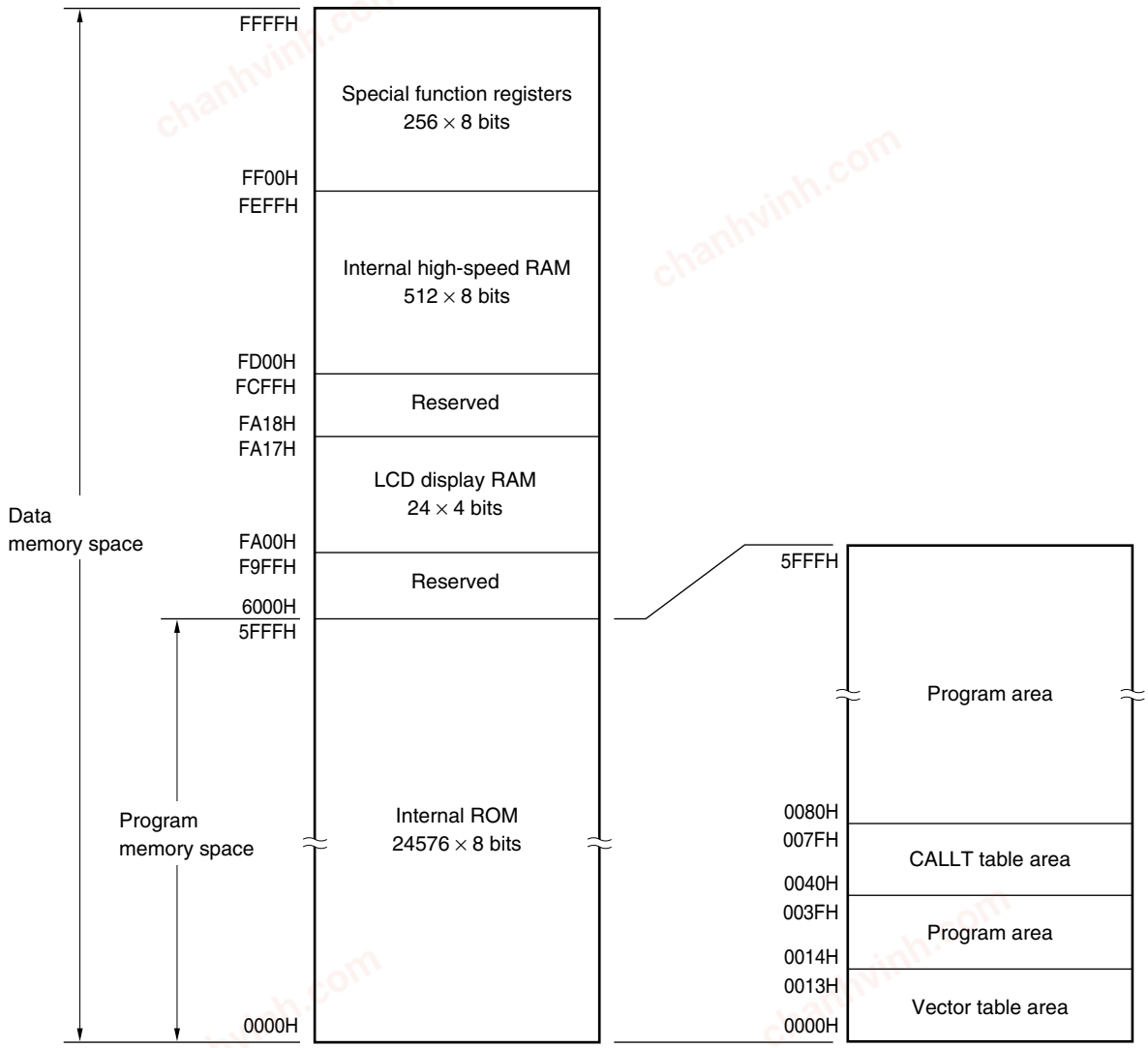
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Figure 3-3. Memory Map (μPD179326)



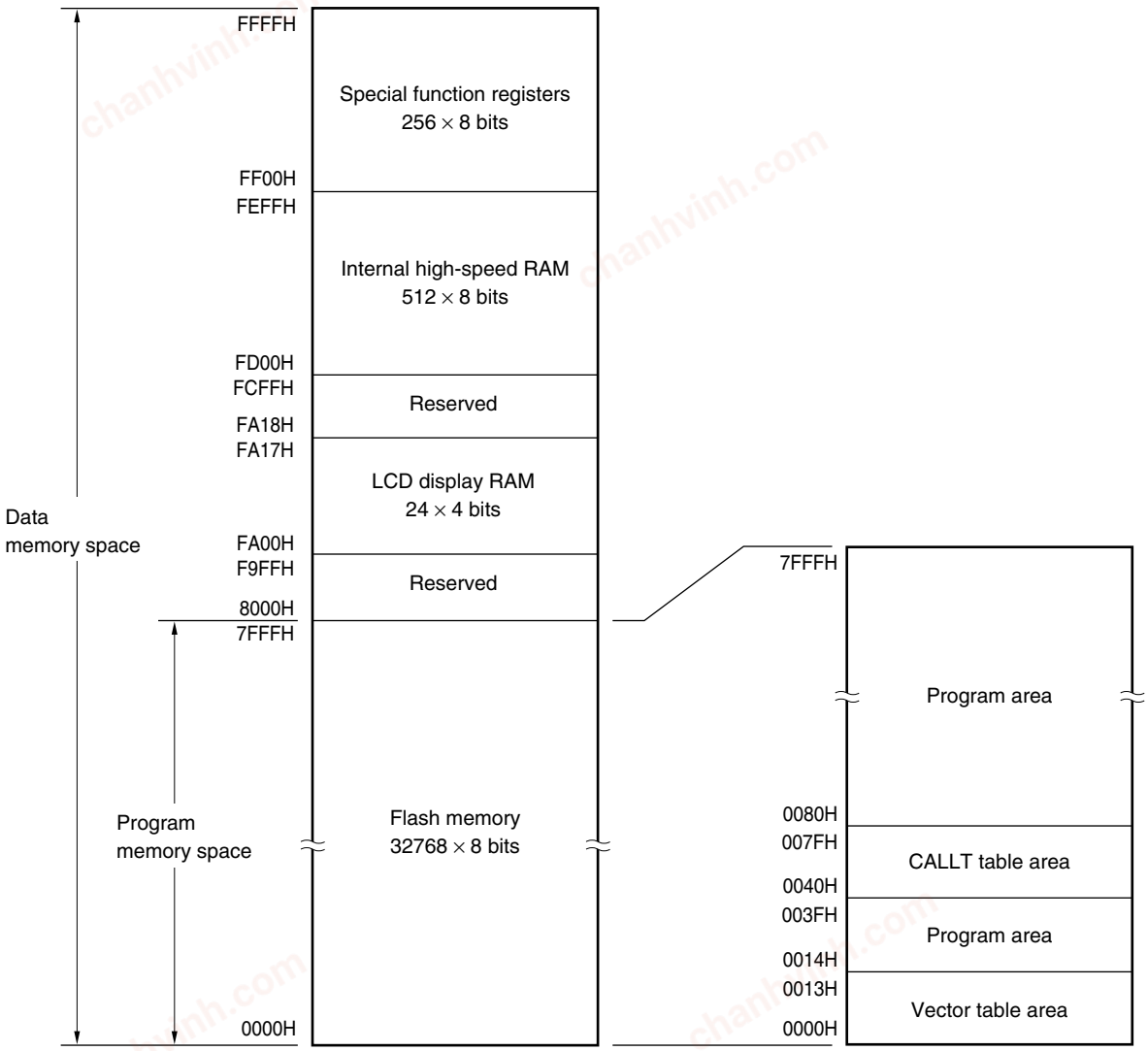
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Figure 3-4. Memory Map (μPD179327)



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Figure 3-5. Memory Map (μPD78F9328)



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3.1.1 Internal program memory space

The internal program memory space stores programs and table data. This space is usually addressed by the program counter (PC).

The μPD179327 Subseries provide internal ROM (or flash memory) with the following capacity for each product.

Table 3-1. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD179322 and 179322A	Mask ROM	4096 × 8 bits
μPD179324 and 179324A		8192 × 8 bits
μPD179326		16384 × 8 bits
μPD179327		24576 × 8 bits
μPD78F9328	Flash memory	32768 × 8 bits

The following areas are allocated to the internal program memory space.

(1) Vector table area

The 20-byte area of addresses 0000H to 0013H is reserved as a vector table area. This area stores program start addresses to be used when branching by the $\overline{\text{RESET}}$ input or an interrupt request generation. Of a 16-bit program address, the lower 8 bits are stored in an even address, and the higher 8 bits are stored in an odd address.

Table 3-2. Vector Table

Vector Table Address	Interrupt Request	Vector Table Address	Interrupt Request
0000H	$\overline{\text{RESET}}$ input	000CH	INTTM30
0004H	INTWDT	000EH	INTTM40
0006H	INTP0	0010H	INTKR00
0008H[Note]	INTCSI10[Note]	0012H	INTWTI
000AH	INTWT		

Note The μPD78F9328 only

(2) CALLT instruction table area

The subroutine entry address of a 1-byte call instruction (CALLT) can be stored in the 64-byte area of addresses 0040H to 007FH.

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3.1.2 Internal data memory (internal high-speed RAM) space

The μPD179327 Subseries products incorporate the following RAM.

(1) Internal high-speed RAM

Internal high-speed RAM is incorporated in the area between FE00H and FEFFH in the μPD179322, 179322A, 179324 and 179324A, and in the area between FD00H and FEFFH in the μPD179326, 179327, and 78F9328.

Instructions cannot be written to this on-chip high-speed RAM as a program area for execution.

The internal high-speed RAM is also used as a stack.

(2) LCD display RAM

LCD display RAM is allocated in the area between FA00H and FA17H. The LCD display RAM can also be used as ordinary RAM.

3.1.3 Special function register (SFR) area

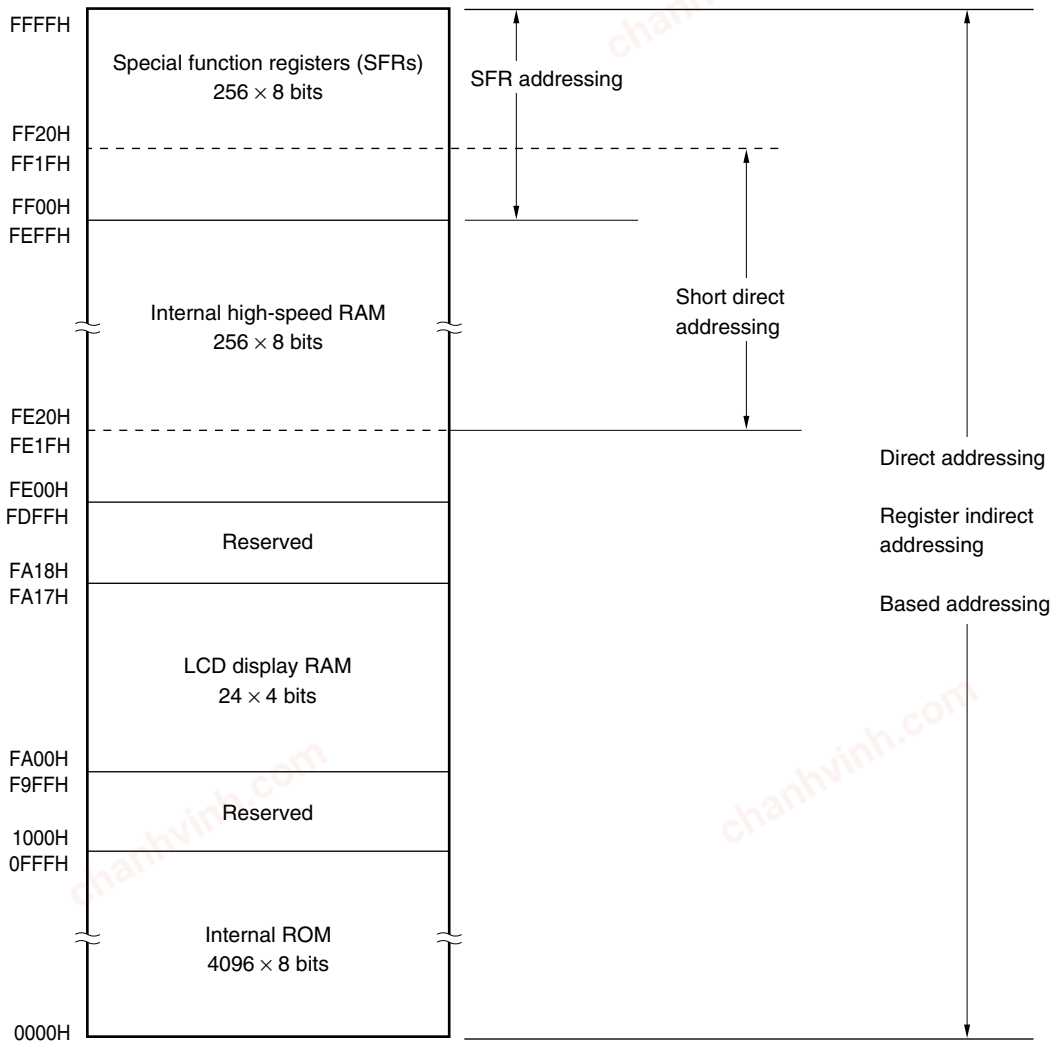
Special function registers (SFRs) of on-chip peripheral hardware are allocated in the area between FF00H and FFFFH (see **Table 3-3**).

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3.1.4 Data memory addressing

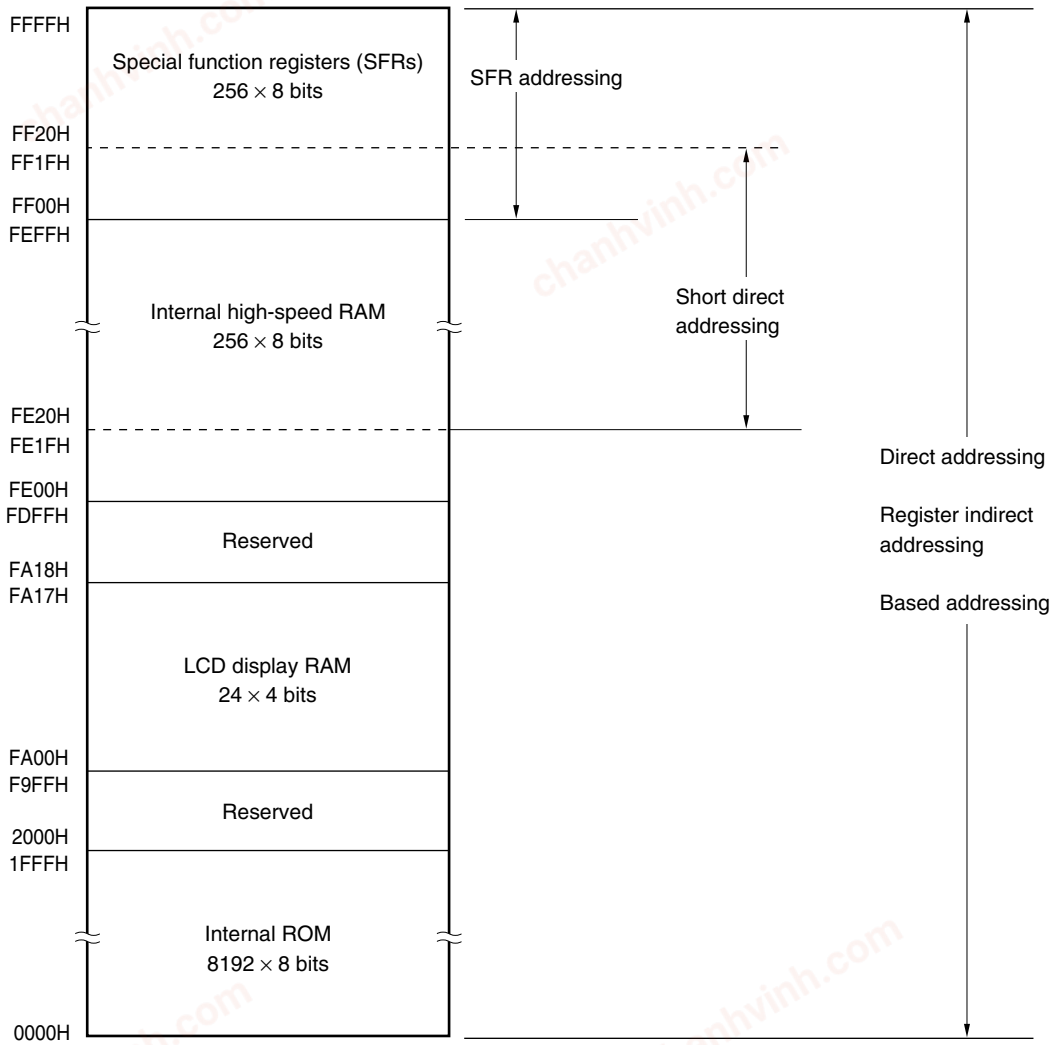
The μPD179327 Subseries are provided with a variety of addressing modes to make memory manipulation as efficient as possible. At the addresses corresponding to data memory area especially, specific addressing modes that correspond to the particular function an area, such as the special function registers are available. Figures 3-6 through 3-10 show the data memory addressing modes.

Figure 3-6. Data Memory Addressing (μPD179322 and 179322A)



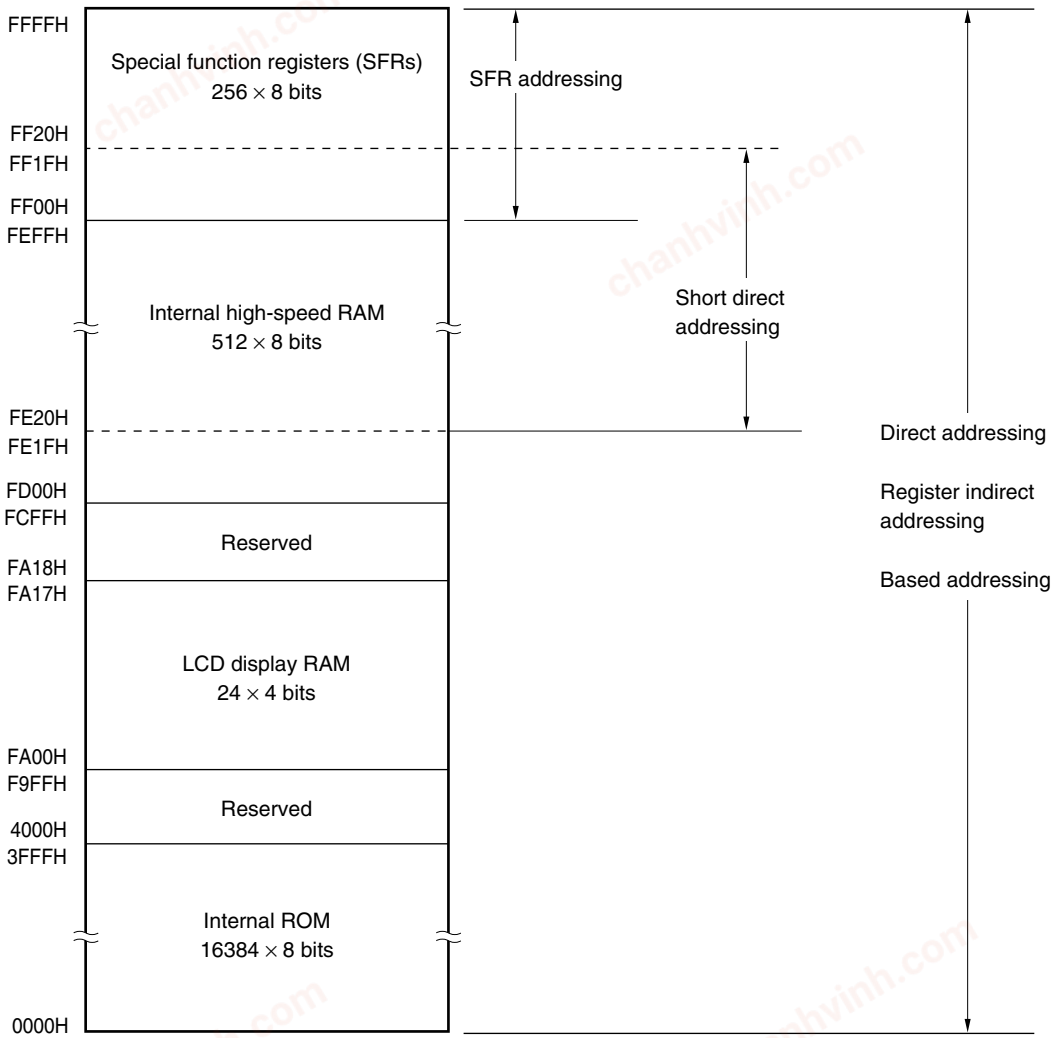
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Figure 3-7. Data Memory Addressing (μPD179324 and 179324A)



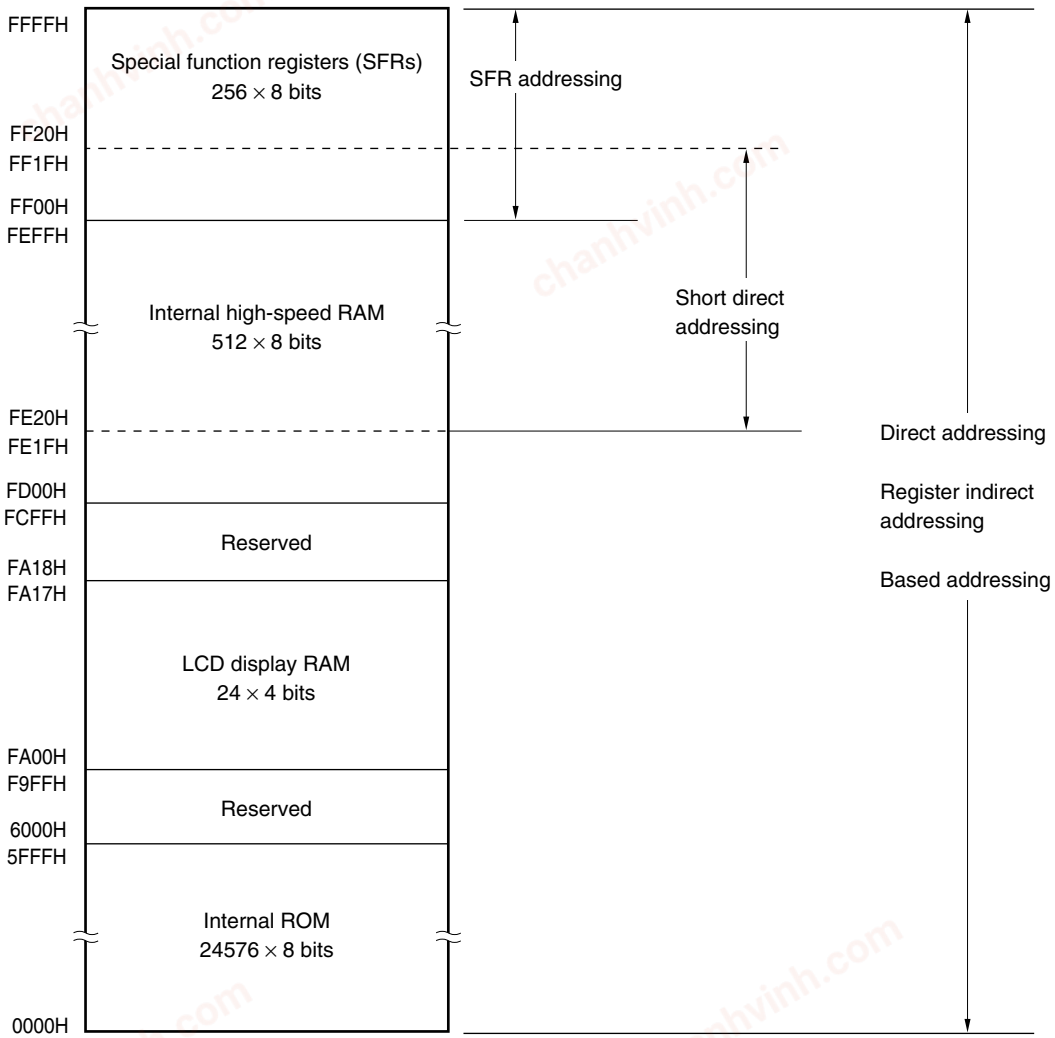
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Figure 3-8. Data Memory Addressing (μPD179326)



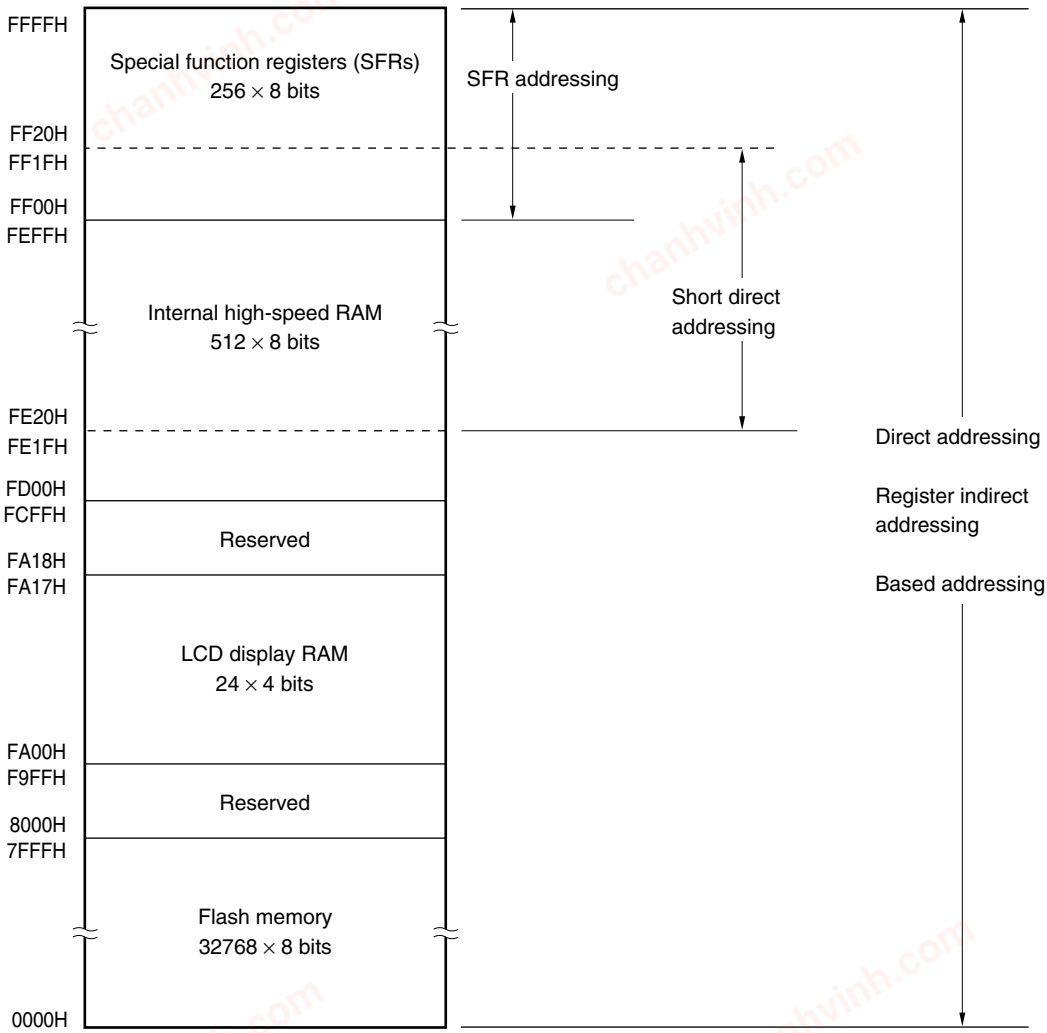
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Figure 3-9. Data Memory Addressing (μPD179327)



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Figure 3-10. Data Memory Addressing (μPD78F9328)



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3.2 Processor Registers

The μPD179327 Subseries provide the following on-chip processor registers.

3.2.1 Control registers

The control registers contain special functions to control the program sequence statuses and stack memory. The program counter, program status word, and stack pointer are control registers.

(1) Program counter (PC)

The program counter is a 16-bit register that holds the address information of the next program to be executed.

In normal operation, the PC is automatically incremented according to the number of bytes of the instruction to be fetched. When a branch instruction is executed, immediate data or register contents are set.

$\overline{\text{RESET}}$ input sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-11. Program Counter Configuration

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags to be set/reset by instruction execution.

The program status word contents are automatically stacked upon interrupt request generation or PUSH PSW instruction execution and are automatically restored upon execution of the RETI and POP PSW instructions.

$\overline{\text{RESET}}$ input sets PSW to 02H.

Figure 3-12. Program Status Word Configuration

	7							0
PSW	IE	Z	0	AC	0	0	1	CY

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(a) Interrupt enable flag (IE)

This flag controls interrupt request acknowledgement operations of the CPU.

When 0, IE is set to the interrupt disable status (DI), and interrupt requests other than non-maskable interrupt are all disabled.

When 1, IE is set to the interrupt enable status (EI). Interrupt request acknowledgement enable is controlled with an interrupt mask flag for various interrupt sources.

IE is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

(c) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(d) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit manipulation instruction execution.

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(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal high-speed RAM area can be set as the stack area.

Figure 3-13. Stack Pointer Configuration

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restore) from the stack memory.

Each stack operation saves/restores data as shown in Figures 3-14 and 3-15.

Caution Since $\overline{\text{RESET}}$ input makes the SP contents undefined, be sure to initialize the SP before instruction execution.

Figure 3-14. Data to Be Saved to Stack Memory

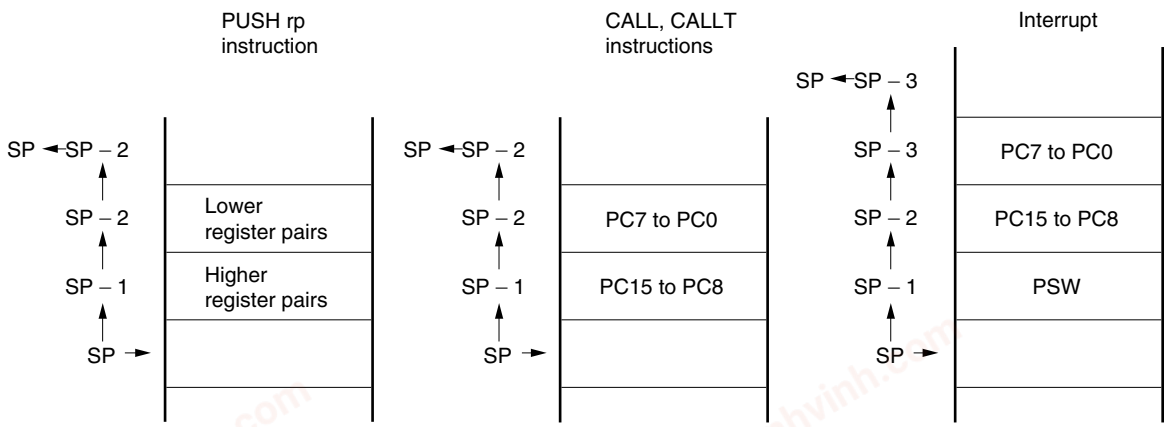
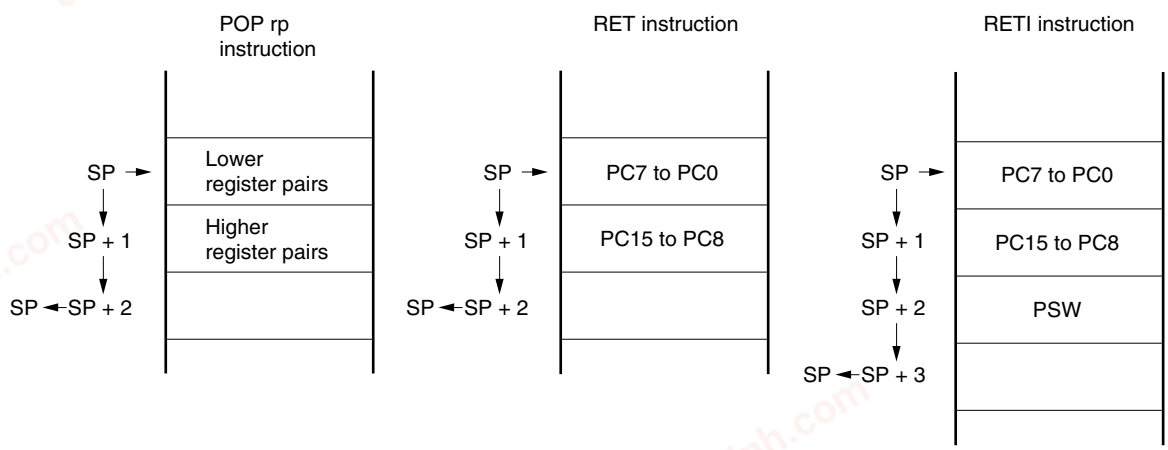


Figure 3-15. Data to Be Restored from Stack Memory



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3.2.2 General-purpose registers

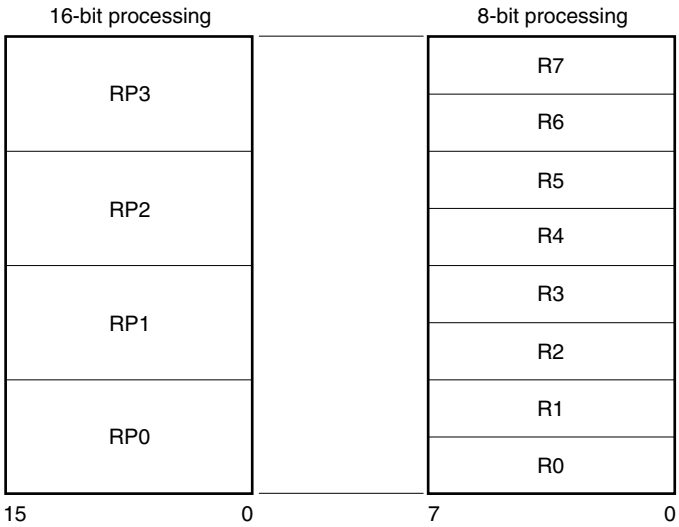
The general-purpose registers consist of eight 8-bit registers (X, A, C, B, E, D, L, and H).

Each register can be used as an 8-bit register, or two 8-bit registers in pairs can be used as a 16-bit register (AX, BC, DE, and HL).

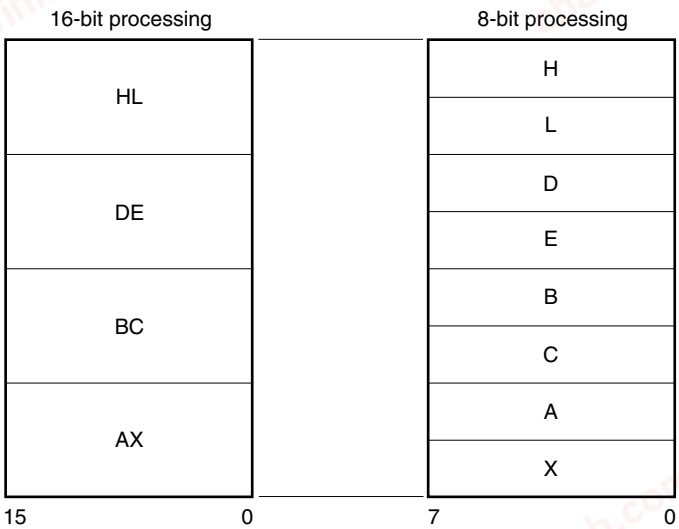
General-purpose registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, or HL) or absolute names (R0 to R7 and RP0 to RP3).

Figure 3-16. General-Purpose Register Configuration

(a) Absolute names



(b) Function names



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3.2.3 Special function registers (SFRs)

Unlike a general-purpose register, each special function register has a special function.

The special function registers are allocated in the 256-byte area of FF00H to FFFFH.

Special function registers can be manipulated, like general-purpose registers, by operation, transfer, and bit manipulation instructions. The manipulatable bit units (1, 8, and 16) differ depending on the special function register type.

The manipulatable bits can be specified as follows.

- 1-bit manipulation
  Describes a symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address.

- 8-bit manipulation
  Describes a symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.

- 16-bit manipulation
  Describes a symbol reserved by the assembler for the 16-bit manipulation instruction operand. When addressing an address, describe an even address.

Table 3-3 lists the special function registers. The meanings of the symbols in this table are as follows:

- Symbol
  Indicates the addresses of the implemented special function registers. The symbols shown in this column are reserved for the assembler and are defined as an sfr variable by the #pragma sfr directive for the C compiler. Therefore, these symbols can be used as instruction operands if an assembler or integrated debugger is used.

- R/W
  Indicates whether the special function register in question can be read or written.
  R/W: Read/write
  R: Read only
  W: Write only

- Bit unit for manipulation
  Indicates the bit units (1, 8, 16) in which the special function register in question can be manipulated.

- After reset
  Indicates the status of the special function register when the $\overline{\text{RESET}}$ signal is input.

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Table 3-3. Special Function Registers (1/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit Unit for Manipulation			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0	R/W	√	√	–	00H
FF01H	Port 1	P1		√	√	–	
FF02H	Port 2	P2		√	√	–	
FF04H	Port 4	P4		√	√	–	
FF06H	Port 6	P6		√	√	–	
FF08H	Port 8	P8		√	√	–	
FF20H	Port mode register 0	PM0		√	√	–	FFH
FF21H	Port mode register 1	PM1		√	√	–	
FF22H	Port mode register 2	PM2		√	√	–	
FF24H	Port mode register 4	PM4		√	√	–	
FF26H	Port mode register 6	PM6		√	√	–	
FF28H	Port mode register 8	PM8		√	√	–	3FH
FF32H	Pull-up resistor option register B2	PUB2		√	√	–	00H
FF42H	Watchdog timer clock selection register	TCL2		–	√	–	
FF4AH	Watch timer mode control register	WTM		√	√	–	
FF58H	Port function register 8	PF8		√	√	–	
FF63H	8-bit compare register 30	CR30	W	–	√	–	Undefined
FF64H	8-bit timer counter 30	TM30	R	–	√	–	00H
FF65H	8-bit timer mode control register 30	TMC30	R/W	√	√	–	
FF66H	8-bit compare register 40	CR40	W	–	√	–	Undefined
FF67H	8-bit H width compare register 40	CRH40		–	√	–	
FF68H	8-bit timer counter 40	TM40	R	–	√	–	00H
FF69H	8-bit timer mode control register 40	TMC40	R/W	√	√	–	
FF6AH	Carrier generator output control register 40	TCA40	W	–	√	–	
FF72H	Serial operation mode register 10[Note1]	CSIM10[Note1]	R/W	√	√	–	
FF74H	Transmission/reception shift register 10[Note1]	SIO10[Note1]		√	√	–	Undefined
FFB0H	LCD display mode register 0	LCDM0		√	√	–	00H
FFB2H	LCD clock control register 0	LCDC0		√	√	–	
FFDDH	Power-on-clear register 1	POCF1		√	√	–	00H[Note2]

Notes 1. Provided in μPD78F9328 only. Do not access this address for a mask ROM version.

2. This value is 04H only after a power-on-clear reset.

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Table 3-3. Special Function Registers (2/2)

Address	Special Function Register (SFR) Name	Symbol	R/W	Bit Unit for Manipulation			After Reset
				1 Bit	8 Bits	16 Bits	
FFE0H	Interrupt request flag register 0	IF0	R/W	√	√	–	00H
FFE4H	Interrupt mask flag register 0	MK0		√	√	–	FFH
FFECH	External interrupt mode register 0	INTM0		√	√	–	00H
FFF0H	Suboscillation mode register	SCKM		√	√	–	
FFF2H	Subclock control register	CSS		√	√	–	
FFF5H	Key return mode register 00	KRM00		√	√	–	
FFF7H	Pull-up resistor option register 0	PU0		√	√	–	
FFF9H	Watchdog timer mode register	WDTM		√	√	–	
FFFAH	Oscillation stabilization time selection register	OSTS		√	√	–	04H
FFFBH	Processor clock control register	PCC		√	√	–	02H

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3.3 Instruction Address Addressing

An instruction address is determined by the program counter (PC) contents. The PC contents are normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to the PC and branched by the following addressing (for details of each instruction, refer to **78K/0S Series Instructions User's Manual (U11047E)**).

3.3.1 Relative addressing

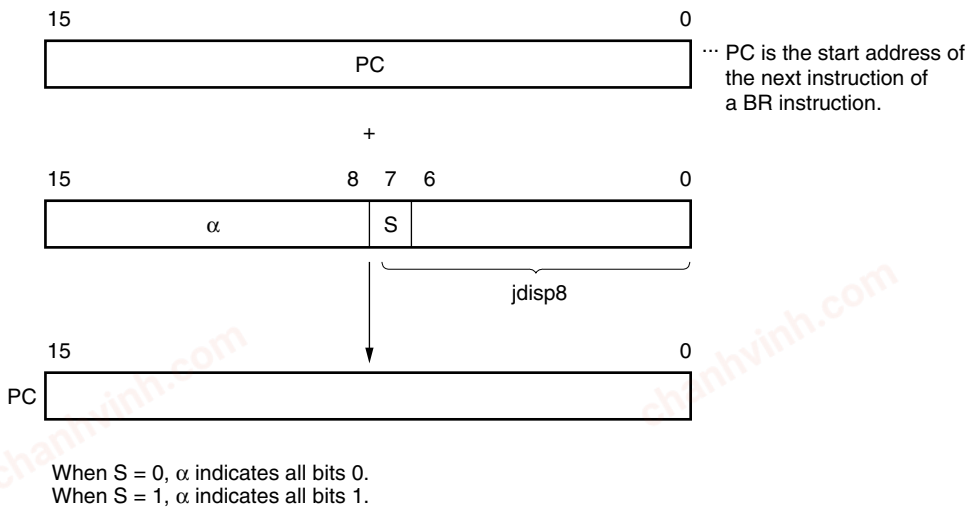
[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (–128 to +127) and bit 7 becomes a sign bit.

This means that information is relatively branched to a location between –128 and +127, from the start address of the next instruction when relative addressing is used.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, α indicates all bits 0.
When S = 1, α indicates all bits 1.

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3.3.2 Immediate addressing

[Function]

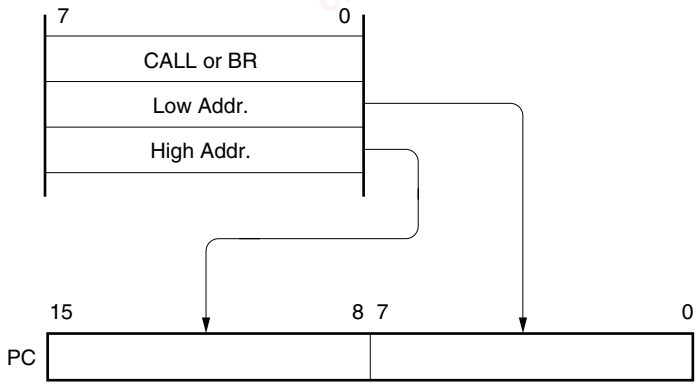
Immediate data in the instruction word is transferred to the program counter (PC) and branched.

This function is carried out when the CALL !addr16 or BR !addr16 instruction is executed.

CALL !addr16 and BR !addr16 instructions can be branched to any location in the memory space.

[Illustration]

In case of CALL !addr16 and BR !addr16 instructions



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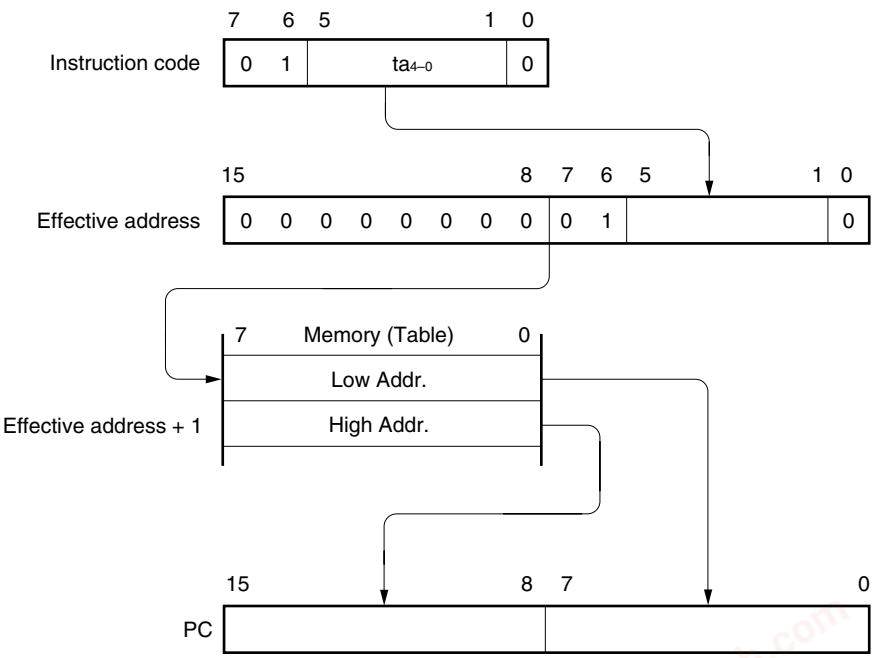
3.3.3 Table indirect addressing

[Function]

Table contents (branch destination address) of the particular location to be addressed by the lower 5-bit immediate data of an instruction code from bit 1 to bit 5 are transferred to the program counter (PC) and branched.

This function is carried out when the CALLT [addr5] instruction is executed. The instruction enables a branch to any location in the memory space by referring to the addresses stored in the memory table at 40H to 7FH.

[Illustration]



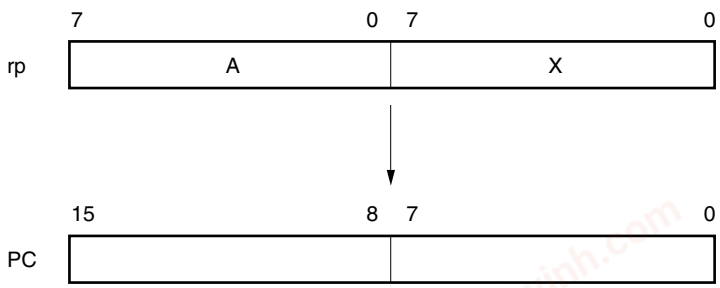
3.3.4 Register addressing

[Function]

The register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) and branched.

This function is carried out when the BR AX instruction is executed.

[Illustration]



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3.4 Operand Address Addressing

The following various methods are available to specify the register and memory (addressing) which undergo manipulation during instruction execution.

3.4.1 Direct addressing

[Function]

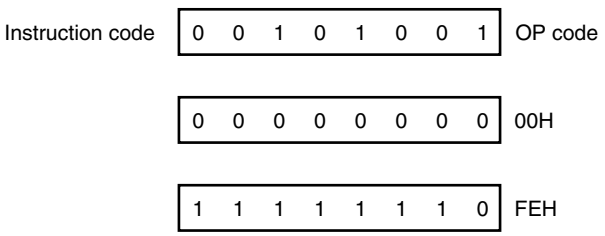
The memory indicated with immediate data in an instruction word is directly addressed.

[Operand format]

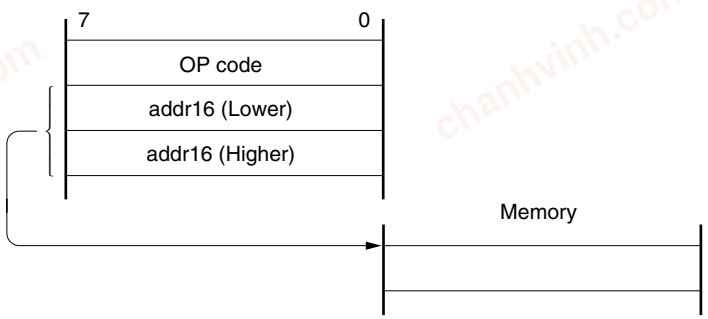
Identifier	Description
addr16	Label or 16-bit immediate data

[Description example]

MOV A, !FE00H; When setting !addr16 to FE00H



[Illustration]



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3.4.2 Short direct addressing

[Function]

The memory to be manipulated in the fixed space is directly addressed with 8-bit data in an instruction word.

The fixed space is the 256-byte space FE20H to FF1FH where the addressing is applied. Internal high-speed RAM and special function registers (SFRs) are mapped at FE20H to FEFFH and FF00H to FF1FH, respectively.

The SFR area (FF00H to FF1FH) where short direct addressing is applied is a part of the whole SFR area. Ports that are frequently accessed in a program and the compare register of the timer counter are mapped in this area, and these SFRs can be manipulated with a small number of bytes and clocks.

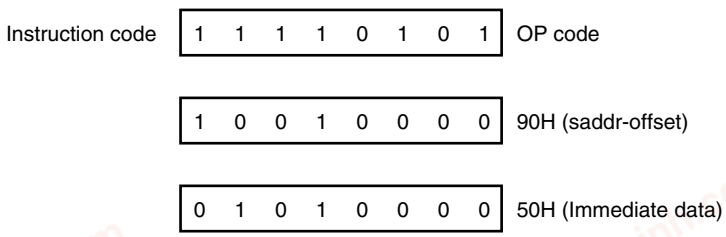
When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is set to 0. When it is at 00H to 1FH, bit 8 is set to 1. See **[Illustration]** below.

[Operand format]

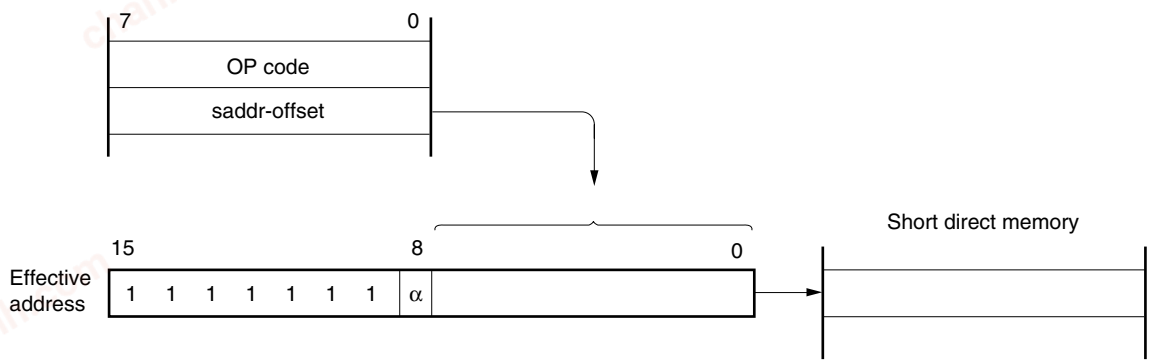
Identifier	Description
saddr	Label or FE20H to FF1FH immediate data
saddrp	Label or FE20H to FF1FH immediate data (even address only)

[Description example]

MOV FE90H, #50H; When setting saddr to FE90H and the immediate data to 50H



[Illustration]



When 8-bit immediate data is 20H to FFH, α = 0.
When 8-bit immediate data is 00H to 1FH, α = 1.

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3.4.3 Special function register (SFR) addressing

[Function]

The memory-mapped special function registers (SFRs) are addressed with 8-bit immediate data in an instruction word.

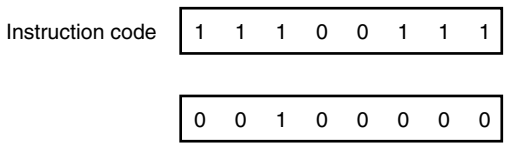
This addressing is applied to the 256-byte space FF00H to FFFFH. However, the SFRs mapped at FF00H to FF1FH can also be accessed with short direct addressing.

[Operand format]

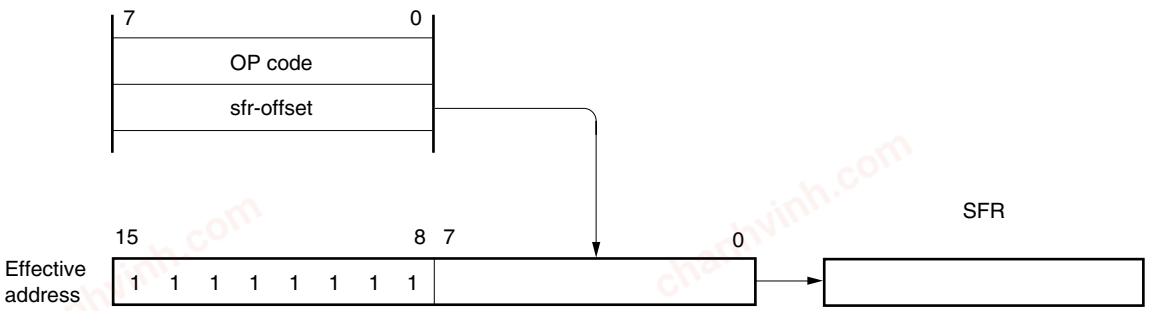
Identifier	Description
sfr	Special function register name

[Description example]

MOV PM0, A; When selecting PM0 for sfr



[Illustration]



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3.4.4 Register addressing

[Function]

In the register addressing mode, general-purpose registers are accessed as operands. The general-purpose register to be accessed is specified by a register specification code or functional name in the instruction code. Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the instruction code.

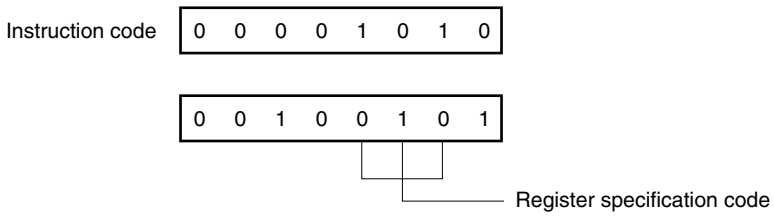
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

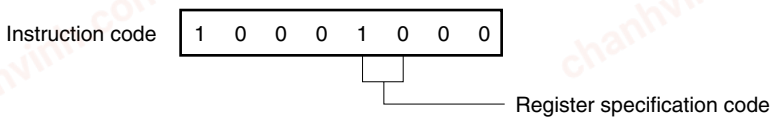
r and rp can be described with absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; When selecting the C register for r



INCW DE; When selecting the DE register pair for rp



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3.4.5 Register indirect addressing

[Function]

In the register indirect addressing mode, memory is manipulated according to the contents of a register pair specified as an operand. The register pair to be accessed is specified by the register pair specification code in an instruction code. This addressing can be carried out for all the memory spaces.

[Operand format]

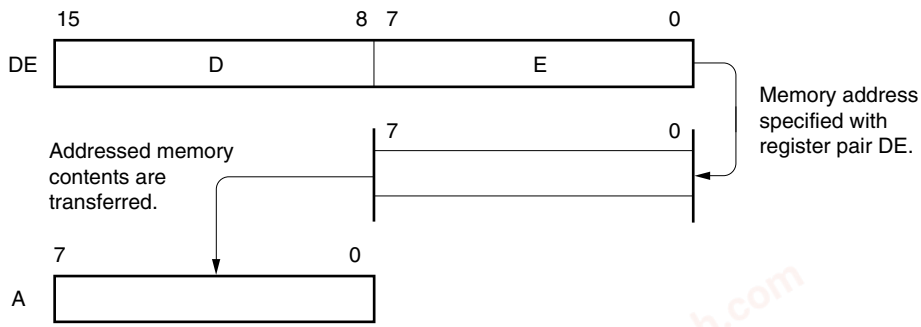
Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; When selecting register pair [DE]

Instruction code | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

[Illustration]



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3.4.6 Based addressing

[Function]

8-bit immediate data is added to the contents of the base register, that is, the HL register pair, and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all the memory spaces.

[Operand format]

Identifier	Description
–	[HL+byte]

[Description example]

MOV A, [HL+10H]; When setting byte to 10H

Instruction code	0	0	1	0	1	1	0	1
	0	0	0	1	0	0	0	0

3.4.7 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon generation of an interrupt request.

Only the internal high-speed RAM area can be addressed using stack addressing.

[Description example]

In the case of PUSH DE

Instruction code	1	0	1	0	1	0	1	0

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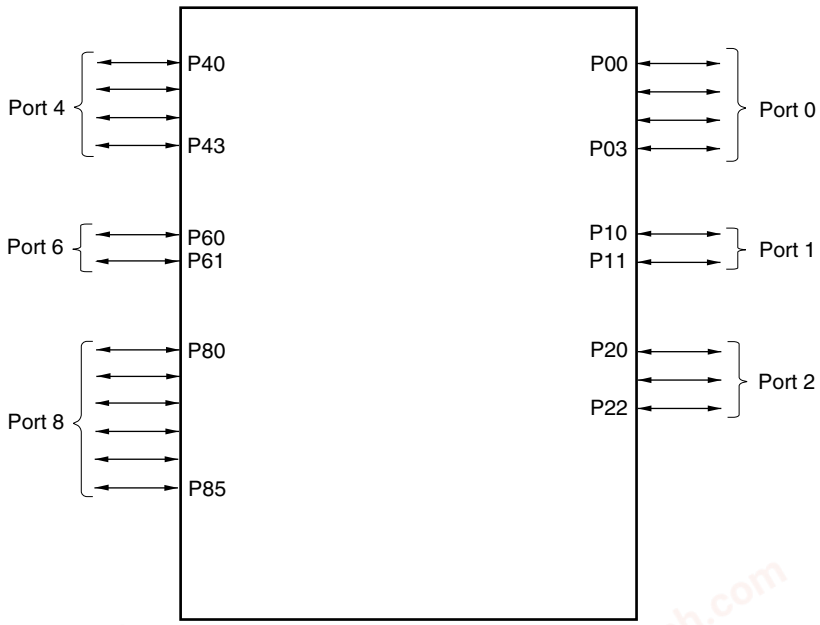
CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

The μPD179327 Subseries provide the ports shown in Figure 4-1, enabling various methods of control.

Numerous other functions are provided that can be used in addition to the digital I/O port functions. For more information on these additional functions, see **CHAPTER 2 PIN FUNCTIONS**.

Figure 4-1. Port Types



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Table 4-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P03	This is an I/O port for which input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0).
Port 1	P10, P11	This is an I/O port for which input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0).
Port 2	P20 to P22	This is an I/O port for which input and output can be specified in 1-bit units. On-chip pull-up resistors can be specified using pull-up resistor option register B2 (PUB2).
Port 4	P40 to P43	This is an I/O port for which input and output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified using pull-up resistor option register 0 (PU0), or key return mode register 00 (KRM00).
Port 6	P60, P61	This is an I/O port for which input and output can be specified in 1-bit units.
Port 8	P80 to P85	This is an I/O port for which input and output can be specified in 1-bit units.

4.2 Port Configuration

The ports include the following hardware.

Table 4-2. Configuration of Port

Item	Configuration
Control registers	Port mode registers (PMm: m = 0 to 2, 4, 6, 8) Pull-up resistor option registers (PU0, PUB2) Port function register 8 (PF8)
Ports	Total: 21 (CMOS I/O: 21)
Pull-up resistors	Total: 13 (software control: 13)

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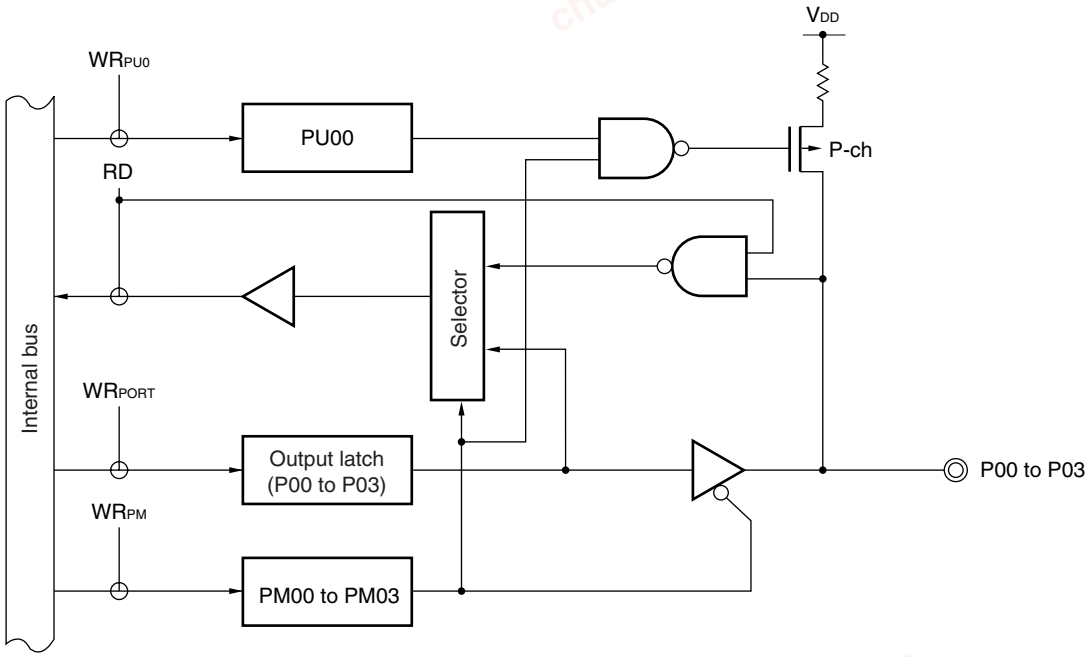
4.2.1 Port 0

Port 0 is a 4-bit I/O port with an output latch. It can be specified in the input or output mode in 1-bit units by using the port mode register 0 (PM0). When the P00 to P03 pins are used as input port pins, on-chip pull-up resistors can be connected in 4-bit units by using pull-up resistor option register 0 (PU0).

$\overline{\text{RESET}}$ input sets port 0 in the input mode.

Figure 4-2 shows a block diagram of port 0.

Figure 4-2. Block Diagram of P00 to P03



PU0: Pull-up resistor option register 0
PM: Port mode register
RD: Port 0 read signal
WR: Port 0 write signal

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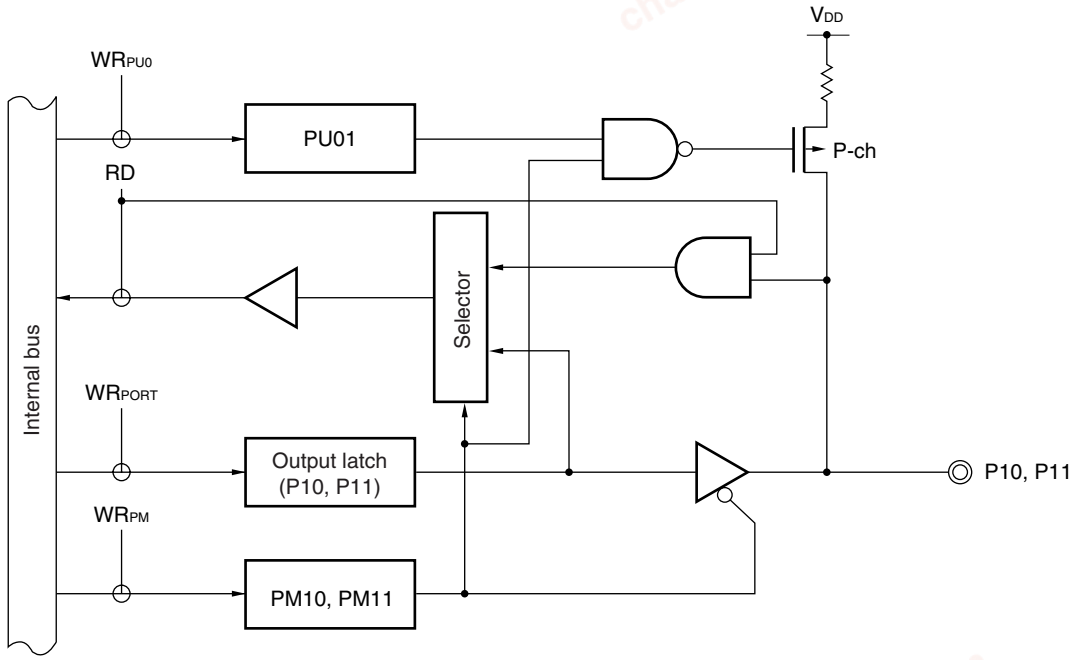
4.2.2 Port 1

Port 1 is a 2-bit I/O port with an output latch. It can be specified in the input or output mode in 1-bit units by using port mode register 1 (PM1). When using the P10 and P11 pins as input port pins, on-chip pull-up resistors can be connected in 2-bit units by using pull-up resistor option register 0 (PU0).

$\overline{\text{RESET}}$ input sets port 1 in the input mode.

Figure 4-3 shows a block diagram of port 1.

Figure 4-3. Block Diagram of P10 and P11



PU0: Pull-up resistor option register 0
PM: Port mode register
RD: Port 1 read signal
WR: Port 1 write signal

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4.2.3 Port 2

Port 2 is a 3-bit I/O port with an output latch. It can be specified in the input or output mode in 1-bit units by using port mode register 2 (PM2). On-chip pull-up resistors can be connected in 1-bit units by using pull-up resistor option register B2 (PUB2) regardless of whether the port is in the input or output mode.

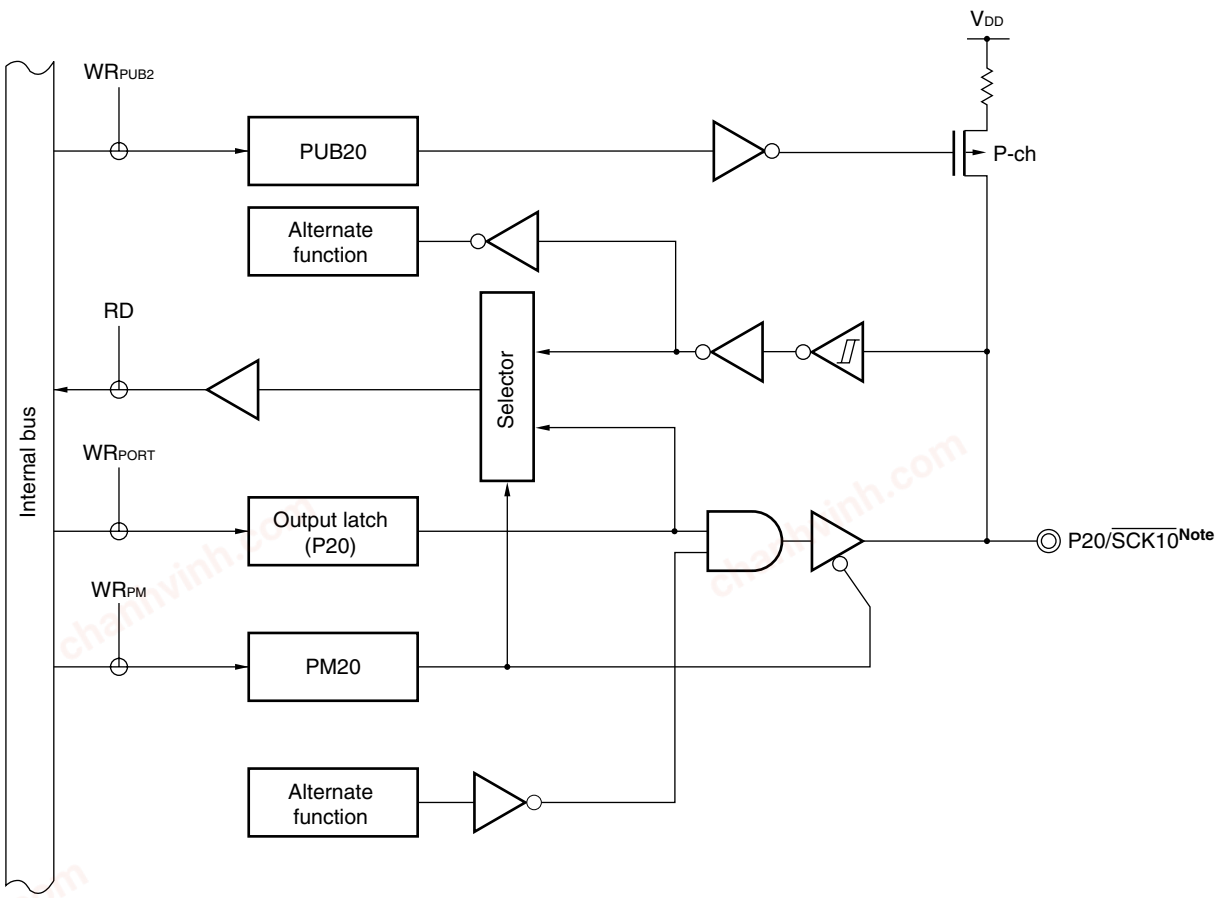
This port can also be used as serial interface data I/O in the μPD78F9328.

$\overline{\text{RESET}}$ input sets port 2 in the input mode.

Figures 4-4 to 4-6 show block diagrams of port 2.

Caution When using the pins of port 2 as the serial interface, the I/O or output latch must be set according to the function to be used. For how to set the latches, see Table 9-2 Settings of Serial Interface 10 Operating Mode.

Figure 4-4. Block Diagram of P20

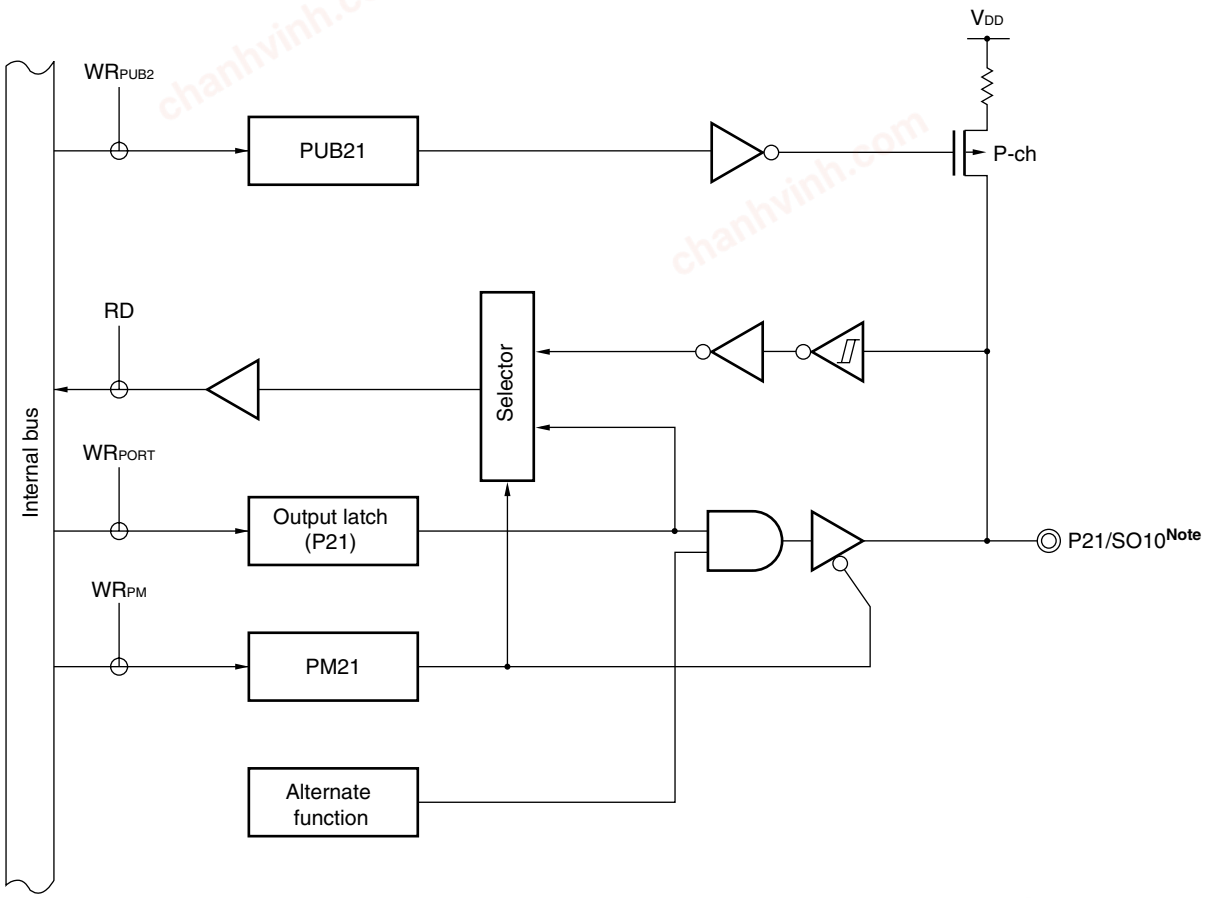


PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Note $\overline{\text{SCK10}}$ is provided in the μPD78F9328 only.

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Figure 4-5. Block Diagram of P21

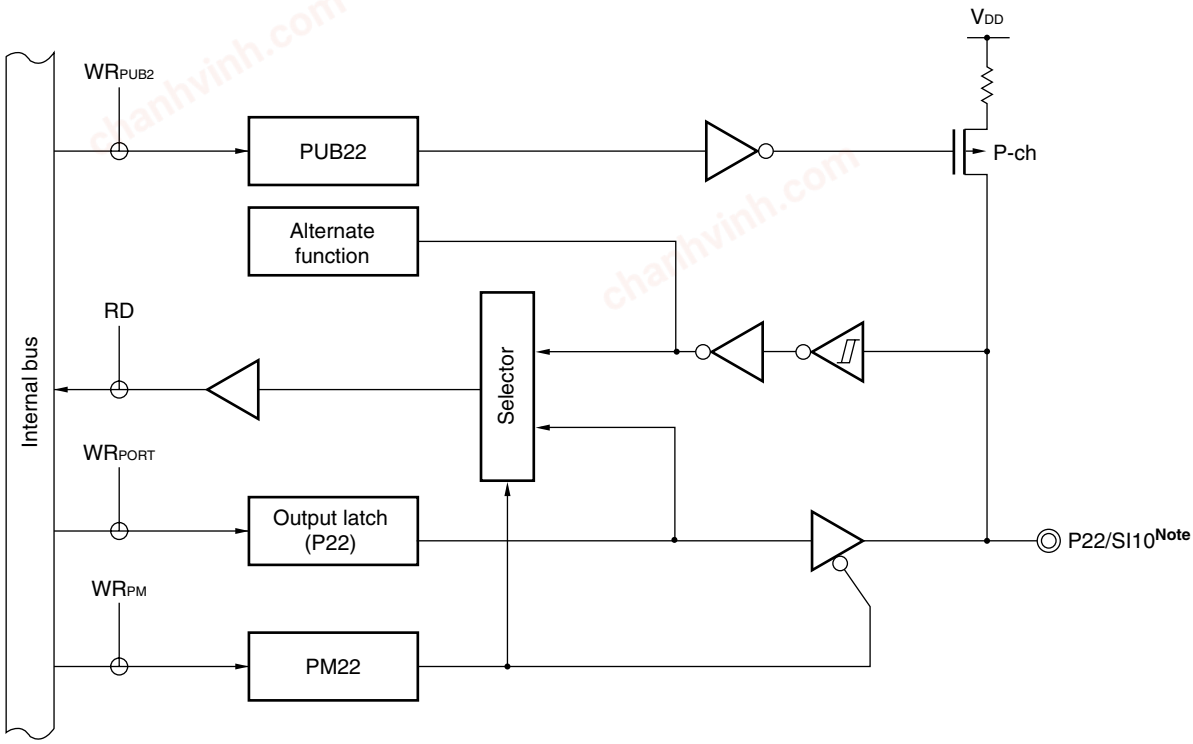


PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Note SO10 is provided in the μPD78F9328 only.

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Figure 4-6. Block Diagram of P22



PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Note SI10 is provided in the μPD78F9328 only.

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4.2.4 Port 4

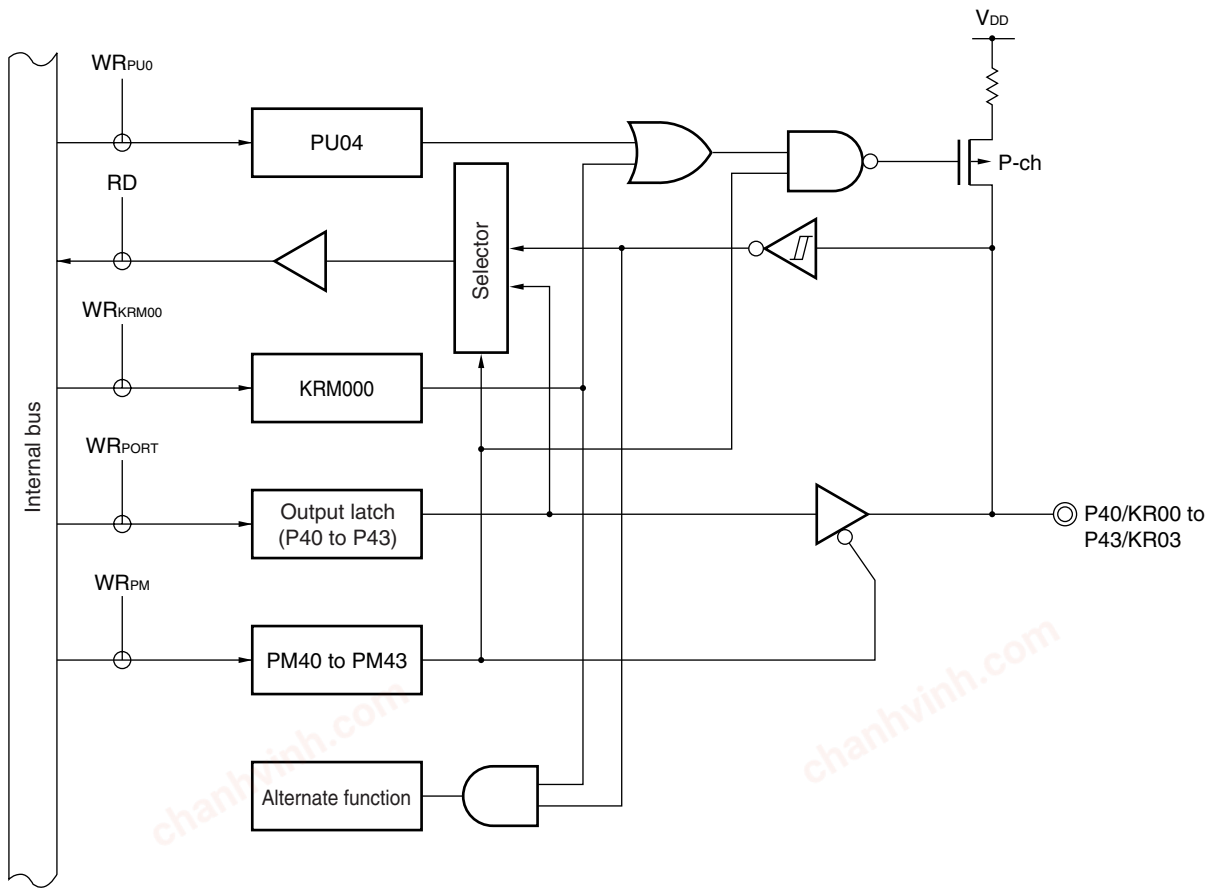
Port 4 is a 4-bit I/O port with an output latch. It can be specified in the input or output mode in 1-bit units by using port mode register 4 (PM4). When using the P40 to P43 pins as input port pins, on-chip pull-up resistors can be connected in 4-bit units by using pull-up resistor option register 0 (PU0).

This port is also used as a key return.

$\overline{\text{RESET}}$ input sets port 4 in the input mode.

Figure 4-7 shows block diagram of port 4.

Figure 4-7. Block Diagram of P40 to P43



KRM00: Key return mode register 00
PU0: Pull-up resistor option register 0
PM: Port mode register
RD: Port 4 read signal
WR: Port 4 write signal

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4.2.5 Port 6

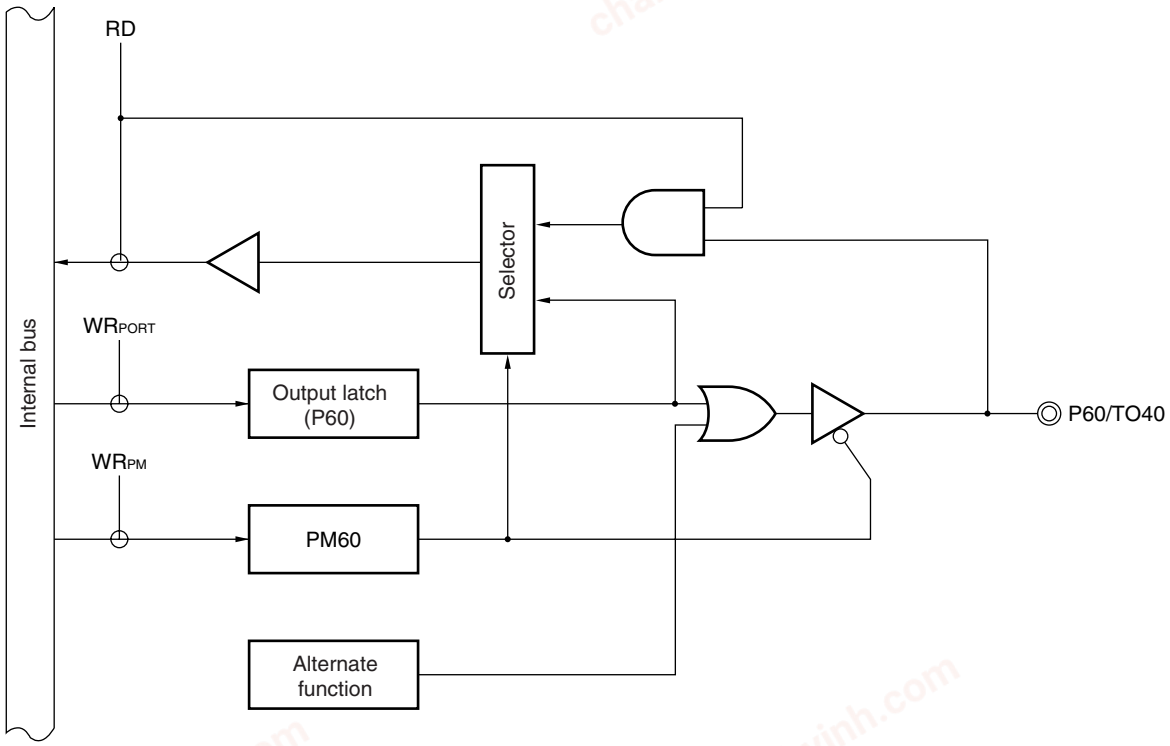
Port 6 is a 2-bit I/O port with an output latch. It can be specified in the input or output mode in 1-bit units by using port mode register 6 (PM6).

This port is also used as a timer output and external interrupt input.

$\overline{\text{RESET}}$ input sets port 6 in the input mode.

Figures 4-8 and 4-9 show block diagrams of port 6.

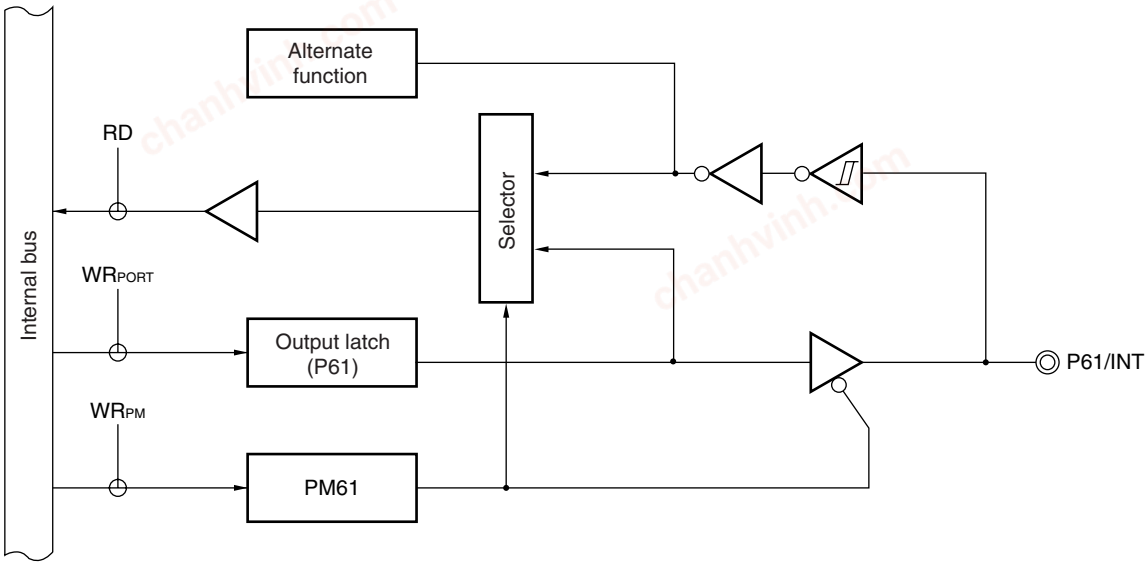
Figure 4-8. Block Diagram of P60



PM: Port mode register
RD: Port 6 read signal
WR: Port 6 write signal

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Figure 4-9. Block Diagram of P61



PM: Port mode register
RD: Port 6 read signal
WR: Port 6 write signal

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4.2.6 Port 8

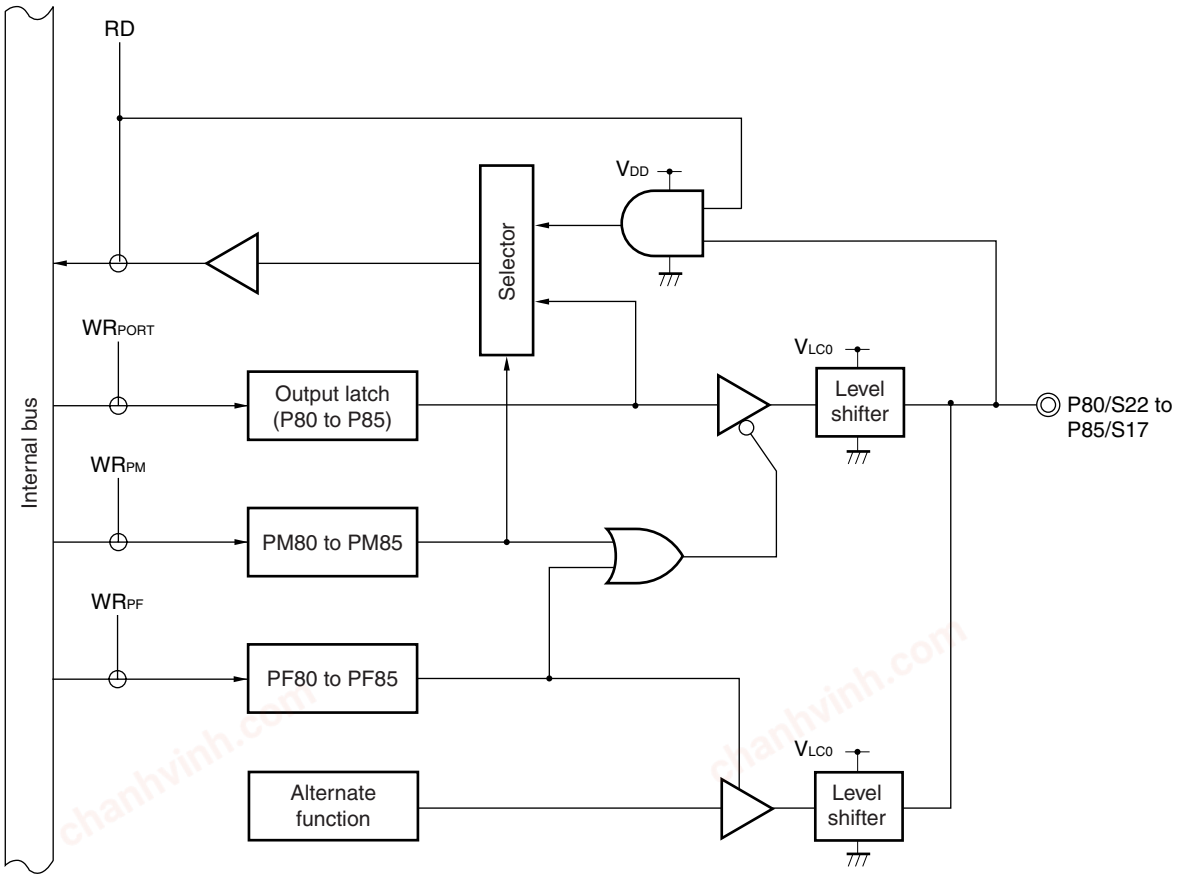
Port 8 is a 6-bit I/O port with an output latch. It can be specified in the input or output mode in 1-bit units by using port mode register 8 (PM8).

This port is also used as a segment output, and can be switched to the port function or segment output function in 1-bit units by port function register 8 (PF8).

$\overline{\text{RESET}}$ input sets port 8 in the input mode.

Figure 4-10 shows a block diagram of port 8.

Figure 4-10. Block Diagram of P80 to P85



PF: Port function register
RD: Port 8 read signal
WR: Port 8 write signal

Caution When using port 8 as an output port, the high-level output voltage is V_{LC0}, not V_{DD}. When a high level is output from the output port, pay attention to the current capacity.

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4.3 Registers Controlling Port Function

The ports are controlled by the following three types of registers.

- Port mode registers (PM0 to PM2, PM4, PM6, PM8)
- Pull-up resistor option registers (PU0, PUB2)
- Port function register 8 (PF8)

(1) Port mode registers (PM0 to PM2, PM4, PM6, PM8)

PM0 to PM2, PM4, PM6 and PM8 are used to set port input/output in 1-bit units.

The port mode registers are independently set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PM0, PM1, PM2, PM4, and PM6 to FFH, and PM8 to 3FH.

When port pins are used as alternate-function pins, set the port mode register and output latch according to Table 4-3.

Caution As P61 has an alternate function as external interrupt input, when the port function output mode is specified and the output level is changed, the interrupt request flag is set. When the output mode is used, therefore, the interrupt mask flag (PMK0) should be preset to 1.

Figure 4-11. Format of Port Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM1	1	1	1	1	1	1	PM11	PM10	FF21H	FFH	R/W
PM2	1	1	1	1	1	PM22	PM21	PM20	FF22H	FFH	R/W
PM4	1	1	1	1	PM43	PM42	PM41	PM40	FF24H	FFH	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FF26H	FFH	R/W
PM8	0	0	PM85	PM84	PM83	PM82	PM81	PM80	FF28H	3FH	R/W

PMmn	Pmn pin input/output mode selection (m = 0 to 2, 4, 6, 8 n = 0 to 5)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Cautions 1. Bits 4 to 7 of PM0, bits 2 to 7 of PM1, bits 3 to 7 of PM2, bits 4 to 7 of PM4, and bits 2 to 7 of PM6 must be set to 1.

2. Bits 6 and 7 of PM8 must be set to 0.

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Table 4-3. Port Mode Registers and Output Latch Settings When Using Alternate Functions

Pin Name	Alternate Function		PM××	P××
	Name	I/O		
P20	$\overline{SCK10}$ Note1	Input	1	×
		Output	0	1
P21	SO10 Note1	Output	0	1
P22	SI10 Note1	Input	1	×
P40 to P43	KR00 to KR03	Input	1	×
P60	TO40	Output	0	0
P61	INT	Input	1	×
P80 to P85	S22 to S17 Note2	Output	×	×

Notes 1. The μPD78F9328 only

2. When using P80 to P85 pins as S22 to S17, set port function register 8 (PF8) to 3FH.

Caution When port 2 is used as a serial interface pin, the I/O latch or output latch must be set according to its function. For the setting method, see Table 9-2 Settings of Serial Interface 10 Operating Mode.

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

(2) Pull-up resistor option register 0 (PU0)

PU0 sets whether an on-chip pull-up resistor on ports 0, 1, and 4 is used or not in port units. On the port specified to use an on-chip pull-up resistor by PU0, the pull-up resistor can be internally used only for the bits set in the input mode. No on-chip pull-up resistors can be used for the bits set in the output mode regardless of the setting of PU0. This also applies to cases when the pins are used for alternate functions.

PU0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears PU0 to 00H.

Figure 4-12. Format of Pull-up Resistor Option Register 0

Symbol	7	6	5	<4>	3	2	<1>	<0>	Address	After reset	R/W
PU0	0	0	0	PU04	0	0	PU01	PU00	FFF7H	00H	R/W

PU0m	Pm on-chip pull-up resistor selection (m = 0, 1, 4)
0	On-chip pull-up resistor not used
1	On-chip pull-up resistor used

Caution Bits 2, 3, and 5 to 7 must be set to 0.

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(3) Pull-up resistor option register B2 (PUB2)

PUB2 sets whether on-chip pull-up resistors on P20 to P22 are used or not in bit units. A pin for which use of an on-chip pull-up resistor is specified by PUB2 can be connected to the pull-up resistor regardless of whether the pin is in the input or output mode. The same applies when the alternate function of the pin is used.

PUB2 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears PUB2 to 00H.

Figure 4-13. Format of Pull-up Resistor Option Register B2

Symbol	7	6	5	4	3	<2>	<1>	<0>	Address	After reset	R/W
PUB2	0	0	0	0	0	PUB22	PUB21	PUB20	FF32H	00H	R/W

PUB2n	P2n on-chip pull-up resistor selection (n = 0 to 2)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Cautions 1. Bits 3 to 7 must be set to 0.

2. Clear PUB2n to 0 when using P2n in the output mode or using it as an alternate function output pin. Otherwise, it always outputs a high level.

(4) Port function register 8 (PF8)

PF8 sets the port function of port 8 in 1-bit units.

The pins of port 8 are selected as either LCD segment signal outputs or general-purpose port pins according to the setting of PF8.

PF8 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears PF8 to 00H.

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Figure 4-14. Format of Port Function Register 8

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PF8	0	0	PF85	PF84	PF83	PF82	PF81	PF80	FF58H	00H	R/W

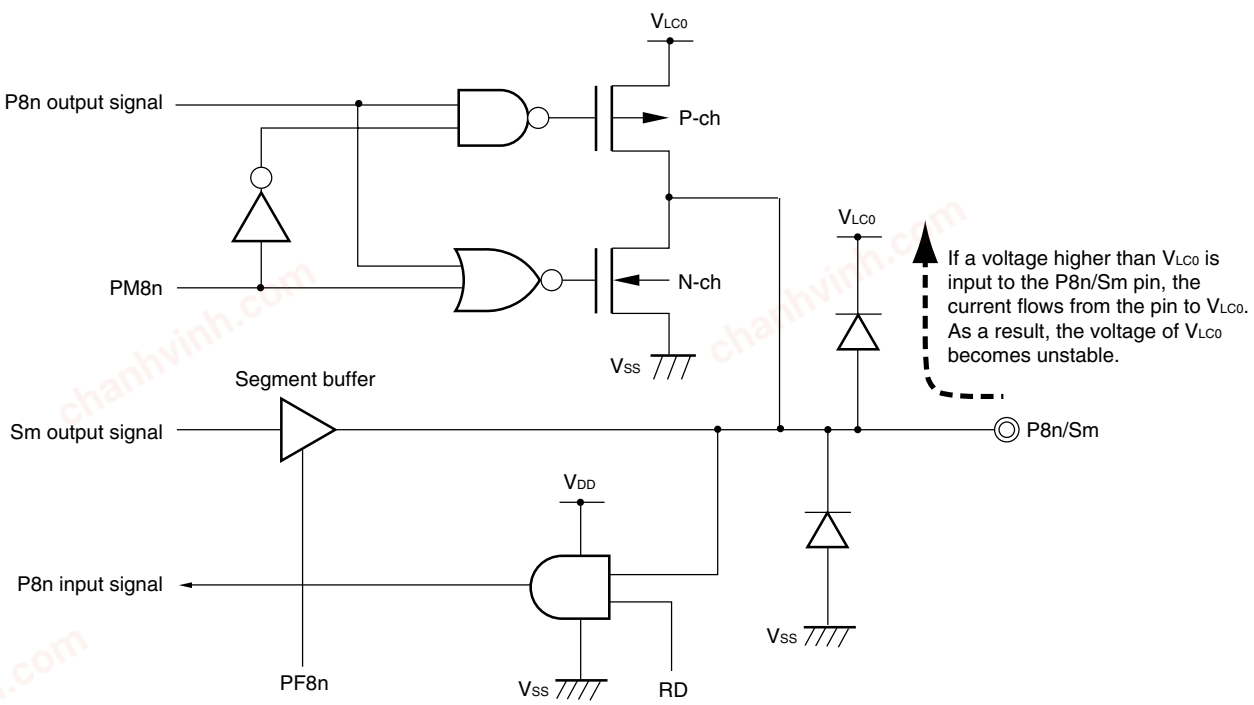
PF8n	P8n port function (n = 0 to 5)
0	Operates as a general-purpose port
1	Operates as an LCD segment signal output

Cautions 1. Bits 6 and 7 must be set to 0.

2. When port 8 is used as a general-purpose port, observe the following restriction (because an ESD protection circuit for LCD pins (on the high-level side of port 8) is connected to V_{LC0}).

- **When any one of pins P80/S22 to P85/S17 is used as a general-purpose input port pin, use the microcontroller at $V_{DD} = V_{LC0}$ or $V_{DD} < V_{LC0}$.**

There is no restriction when all of pins P80/S22 to P85/S17 are used as LCD segment pins or general-purpose output port pins.



Remark Sm: LCD segment output (m = 22 to 17)
P8n: Bit n of Port 8 (n = 0 to 5)
PF8n: Bit n of Port function register 8 (n = 0 to 5)
RD: Port 8 read signal

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4.4 Port Function Operation

The operation of a port differs depending on whether the port is set in the input or output mode, as described below.

4.4.1 Writing to I/O port

(1) In output mode

A value can be written to the output latch of a port by using a transfer instruction. The contents of the output latch can be output from the pins of the port.

Data once written to the output latch is retained until new data is written to the output latch.

(2) In input mode

A value can be written to the output latch by using a transfer instruction. However, the status of the port pin is not changed because the output buffer is OFF.

Data once written to the output latch is retained until new data is written to the output latch.

Caution A 1-bit memory manipulation instruction is executed to manipulate 1 bit of a port. However, this instruction accesses the port in 8-bit units. When this instruction is executed to manipulate a bit of an input/output port, therefore, the contents of the output latch of the pin that is set in the input mode and not subject to manipulation become undefined.

4.4.2 Reading from I/O port

(1) In output mode

The status of an output latch can be read by using a transfer instruction. The contents of the output latch are not changed.

(2) In input mode

The status of a pin can be read by using a transfer instruction. The contents of the output latch are not changed.

4.4.3 Arithmetic operation of I/O port

(1) In output mode

An arithmetic operation can be performed with the contents of the output latch. The result of the operation is written to the output latch. The contents of the output latch are output from the port pins.

Data once written to the output latch is retained until new data is written to the output latch.

(2) In input mode

The contents of the output latch become undefined. However, the status of the pin is not changed because the output buffer is OFF.

Caution A 1-bit memory manipulation instruction is executed to manipulate 1 bit of a port. However, this instruction accesses the port in 8-bit units. When this instruction is executed to manipulate a bit of an input/output port, therefore, the contents of the output latch of the pin that is set in the input mode and not subject to manipulation become undefined.

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CHAPTER 5 CLOCK GENERATOR

5.1 Clock Generator Functions

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following two types of system clock oscillators are used.

- **Main system clock (ceramic/crystal) oscillator**
  This circuit oscillates at 1.0 to 5.0 MHz. Oscillation can be stopped by executing the STOP instruction or setting the processor clock control register (PCC).
- **Subsystem clock oscillator**
  This circuit oscillates at 32.768 kHz. Oscillation can be stopped by the suboscillation mode register (SCKM).

5.2 Clock Generator Configuration

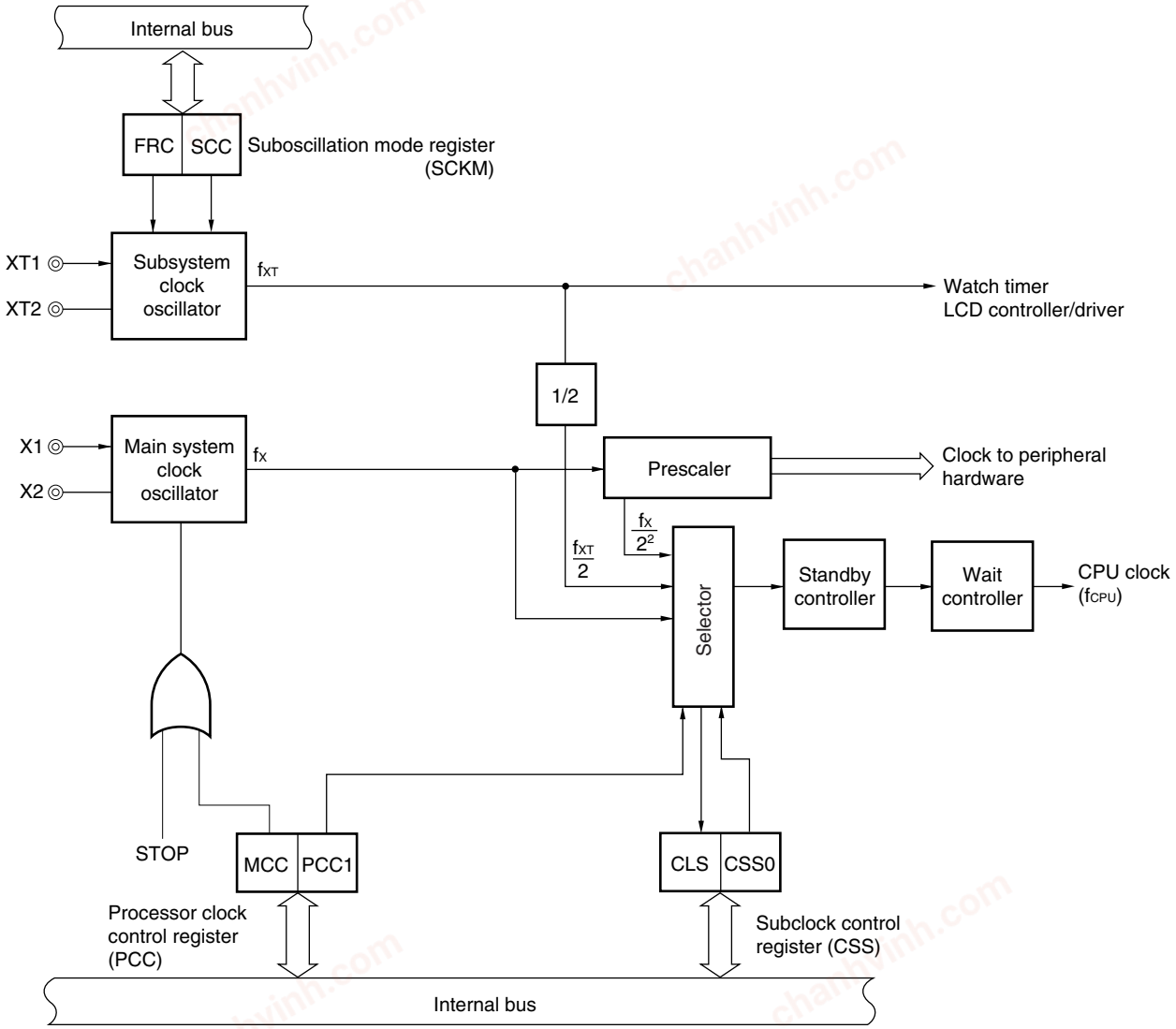
The clock generator includes the following hardware.

Table 5-1. Configuration of Clock Generator

Item	Configuration
Control registers	Processor clock control register (PCC) Suboscillation mode register (SCKM) Subclock control register (CSS)
Oscillators	Main system clock oscillator Subsystem clock oscillator

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Figure 5-1. Block Diagram of Clock Generator



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5.3 Registers Controlling Clock Generator

The clock generator is controlled by the following three registers.

- Processor clock control register (PCC)
- Suboscillation mode register (SCKM)
- Subclock control register (CSS)

(1) Processor clock control register (PCC)

PCC sets CPU clock selection and the division ratio.

PCC is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PCC to 02H.

Figure 5-2. Format of Processor Clock Control Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
PCC	MCC	0	0	0	0	0	PCC1	0	FFFBH	02H	R/W

MCC	Control of main system clock oscillator operation
0	Operation enabled
1	Operation disabled

CSS0	PCC1	CPU clock (f_{CPU}) selection[Note]	Maximum instruction execution time: $2/f_{CPU}$
			f_X = 5.0 MHz or f_{XT} = 32.768 kHz operation
0	0	f_X	0.4 μs
0	1	$f_X/2^2$	1.6 μs
1	×	$f_{XT}/2$	122 μs

Note The CPU clock is selected according to a combination of the PCC1 flag in the processor clock control register (PCC) and the CSS0 flag in the subclock control register (CSS) (Refer to **5.3 (3) Subclock control register (CSS)**).

Cautions 1. Bits 0 and 2 to 6 must be set to 0.

2. The MCC can be set only when the subsystem clock has been selected as the CPU clock.

Setting MCC to 1 while the main system clock is operating is invalid.

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. ×: Don't care

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(2) Suboscillation mode register (SCKM)

SCKM selects a feedback resistor for the subsystem clock, and controls the oscillation of the clock.

SCKM is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears SCKM to 00H.

Figure 5-3. Format of Suboscillation Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
SCKM	0	0	0	0	0	0	FRC	SCC	FFF0H	00H	R/W

FRC	Feedback resistor selection[Note]
0	On-chip feedback resistor used
1	On-chip feedback resistor not used

SCC	Control of subsystem clock oscillator operation
0	Operation enabled
1	Operation disabled

Note The feedback resistor is necessary to adjust the bias point of the oscillation waveform to close to the mid point of the supply voltage. Only when the subclock is not used, the power consumption in STOP mode can be further reduced by setting FRC = 1.

Caution Bits 2 to 7 must be set to 0.

(3) Subclock control register (CSS)

CSS specifies whether the main system or subsystem clock oscillator is to be selected. It also specifies the CPU clock operation status.

CSS is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSS to 00H.

Figure 5-4. Format of Subclock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
CSS	0	0	CLS	CSS0	0	0	0	0	FFF2H	00H	R/W[Note]

CLS	CPU clock operation status
0	Operation based on the output of the divided main system clock
1	Operation based on the subsystem clock

CSS0	Selection of the main system or subsystem clock oscillator
0	Divided output from the main system clock oscillator
1	Output from the subsystem clock oscillator

Note Bit 5 is read only.

Caution Bits 0 to 3, 6, and 7 must be set to 0.

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5.4 System Clock Oscillators

5.4.1 Main system clock oscillator

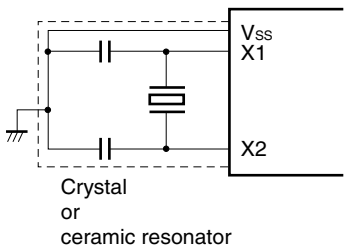
The main system clock oscillator is oscillated by the crystal or ceramic resonator (5.0 MHz TYP.) connected across the X1 and X2 pins.

An external clock can also be input to the circuit. In this case, input the clock signal to the X1 pin, and input the inverted signal to the X2 pin.

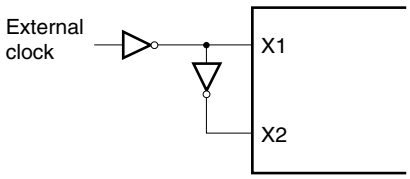
Figure 5-5 shows the external circuit of the main system clock oscillator.

Figure 5-5. External Circuit of Main System Clock Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



Caution When using the main system or subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in Figures 5-5 and 5-6 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

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5.4.2 Subsystem clock oscillator

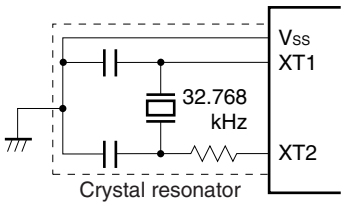
The subsystem clock oscillator is oscillated by the crystal resonator (32.768 kHz TYP.) connected across the XT1 and XT2 pins.

An external clock can also be input to the circuit. In this case, input the clock signal to the XT1 pin, and input the inverted signal to the XT2 pin.

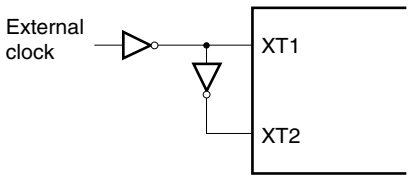
Figure 5-6 shows the external circuit of the subsystem clock oscillator.

Figure 5-6. External Circuit of Subsystem Clock Oscillator

(a) Crystal oscillation



(b) External clock



Caution When using the main system or subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in Figures 5-5 and 5-6 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

When using the subsystem clock, particular care is required because the subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption.

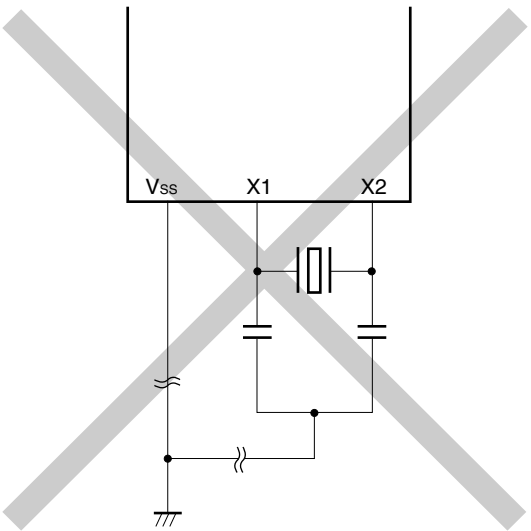
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5.4.3 Example of incorrect resonator connection

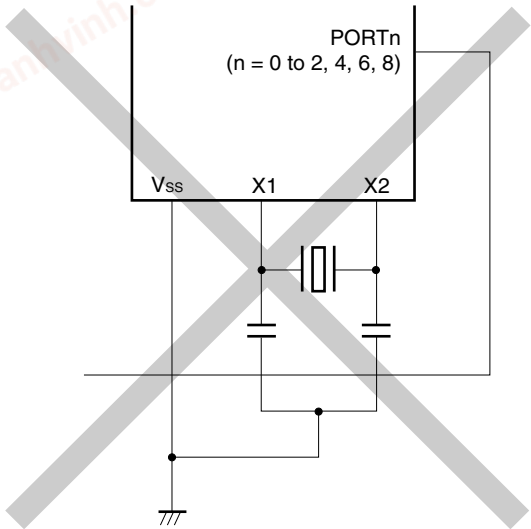
Figure 5-7 shows examples of incorrect resonator connection.

Figure 5-7. Examples of Incorrect Resonator Connection (1/2)

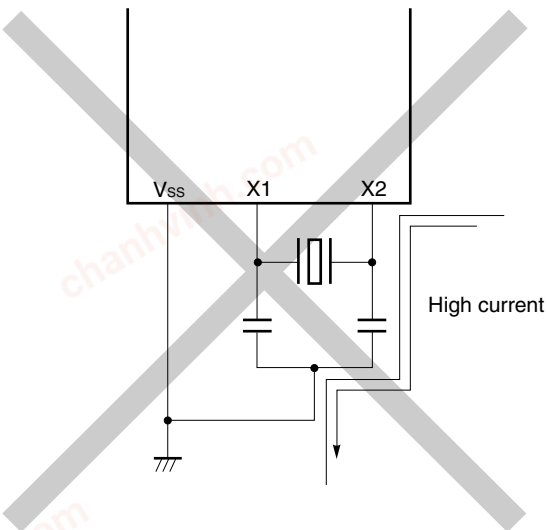
(a) Too long wiring



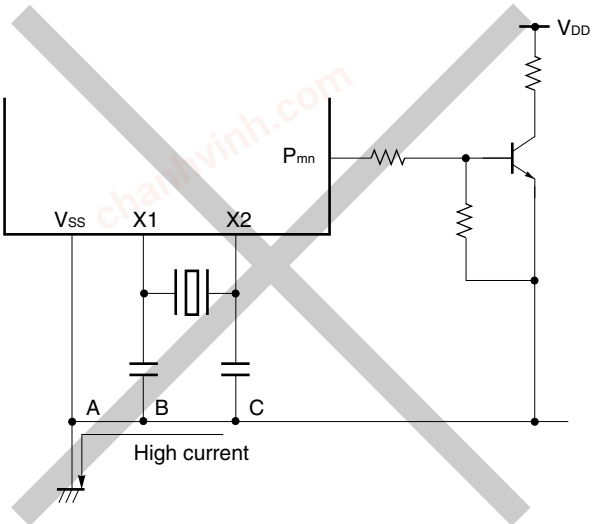
(b) Crossed signal line



(c) Wiring near high fluctuating current



(d) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)

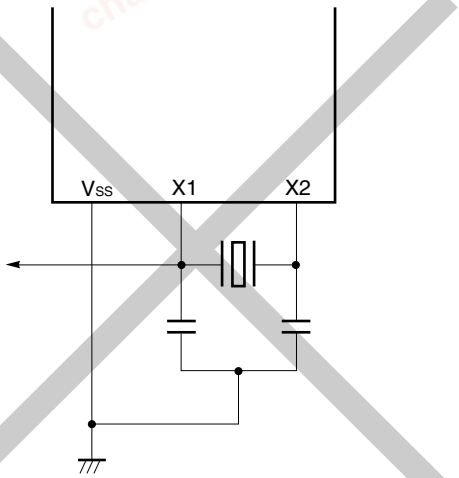


Remark When using the subsystem clock, read X1 and X2 as XT1 and XT2, respectively, and connect a resistor to the XT2 in series.

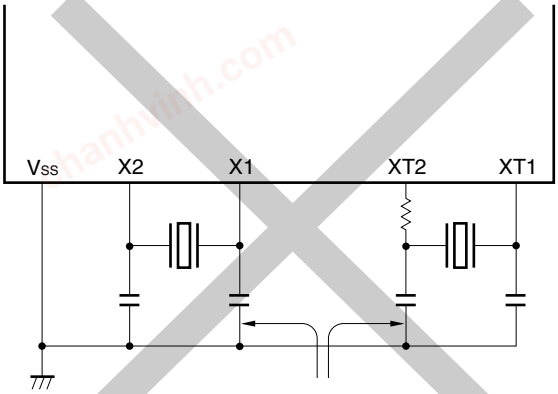
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Figure 5-7. Examples of Incorrect Resonator Connection (2/2)

(e) Signal is fetched



(f) Parallel and near signal lines of main system clock and subsystem clock



XT2 is wired parallel to X1.

Remark When using the subsystem clock, read X1 and X2 as XT1 and XT2, respectively, and connect a resistor to the XT2 in series.

Caution If the X1 wire is in parallel with the XT2 wire, crosstalk noise may occur between the X1 and XT2, resulting in a malfunction.
To avoid this, do not lay the X1 and XT2 wires in parallel.

5.4.4 Divider circuit

The divider circuit divides the output of the main system clock oscillator (fx) to generate various clocks.

5.4.5 When no subsystem clock is used

If a subsystem clock is not necessary, for example, for low-power consumption operation or clock operation, handle the XT1 and XT2 pins as follows:

XT1: Connect to VSS
XT2: Leave open

In this case, however, a small current leaks via the on-chip feedback resistor in the subsystem clock oscillator when the main system clock is stopped. To avoid this, set bit 1 (FRC) of the suboscillation mode register (SCKM) so that the on-chip feedback resistor will not be used. Also in this case, handle the XT1 and XT2 pins as stated above.

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5.5 Clock Generator Operation

The clock generator generates the following clocks and controls the operation modes of the CPU, such as the standby mode.

- Main system clock f_X
- Subsystem clock f_{XT}
- CPU clock f_{CPU}
- Clock to peripheral hardware

The operation and function of the clock generator is determined by the processor clock control register (PCC), suboscillation mode register (SCKM), and subclock control register (CSS), as follows.

(a) The low-speed mode (1.6 μs: at 5.0 MHz operation) of the main system clock is selected when the $\overline{\text{RESET}}$ signal is generated (PCC = 02H). While a low level is input to the $\overline{\text{RESET}}$ pin, oscillation of the main system clock is stopped.

(b) Three types of minimum instruction execution time (0.4 μs and 1.6 μs: main system clock (at 5.0 MHz operation), 122 μs: subsystem clock (at 32.768 kHz operation)) can be selected by the PCC, SCKM, and CSS settings.

(c) Two standby modes, STOP and HALT, can be used with the main system clock selected. In a system where no subsystem clock is used, setting bit 1 (FRC) of the SCKM so that the on-chip feedback resistor cannot be used reduces current consumption in STOP mode. In a system where a subsystem clock is used, setting SCKM bit 0 to 1 can cause the subsystem clock to stop oscillation.

(d) CSS bit 4 (CSS0) can be used to select the subsystem clock so that low current consumption operation is used (122 μs: at 32.768 kHz operation).

(e) With the subsystem clock selected, it is possible to cause the main system clock to stop oscillating using bit 7 (MCC) of PCC. The HALT mode can be used, but the STOP mode cannot.

(f) The clock pulse for the peripheral hardware is generated by dividing the frequency of the main system clock, but the subsystem clock pulse is only supplied to the watch timer and LCD controller/driver. The watch timer and LCD controller/driver can therefore keep running even during standby. The other hardware stops when the main system clock stops because it runs based on the main system clock (except for external input clock operations).

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5.6 Changing Setting of System Clock and CPU Clock

5.6.1 Time required for switching between system clock and CPU clock

The CPU clock can be selected by using bit 1 (PCC1) of the processor clock control register (PCC) and bit 4 (CSS0) of the subclock control register (CSS).

The maximum time indicated in Table 5-2 is required until the CPU clock actually switches (i.e. switching does not occur immediately after the PCC register is rewritten). Until this time has elapsed, therefore, it is impossible to ascertain whether the clock before or after the switch is operating.

Table 5-2. Maximum Time Required for Switching CPU Clock

Set Value Before Switching		Set Value After Switching					
CSS0	PCC1	CSS0	PCC1	CSS0	PCC1	CSS0	PCC1
		0	0	0	1	1	×
0	0			4 clocks		$2f_X/f_{XT}$ clocks (306 clocks)	
	1	2 clocks				$f_X/2f_{XT}$ clocks (76 clocks)	
1	×	2 clocks		2 clocks			

Remarks 1. Two clocks are the minimum instruction execution time of the CPU clock before switching.

2. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

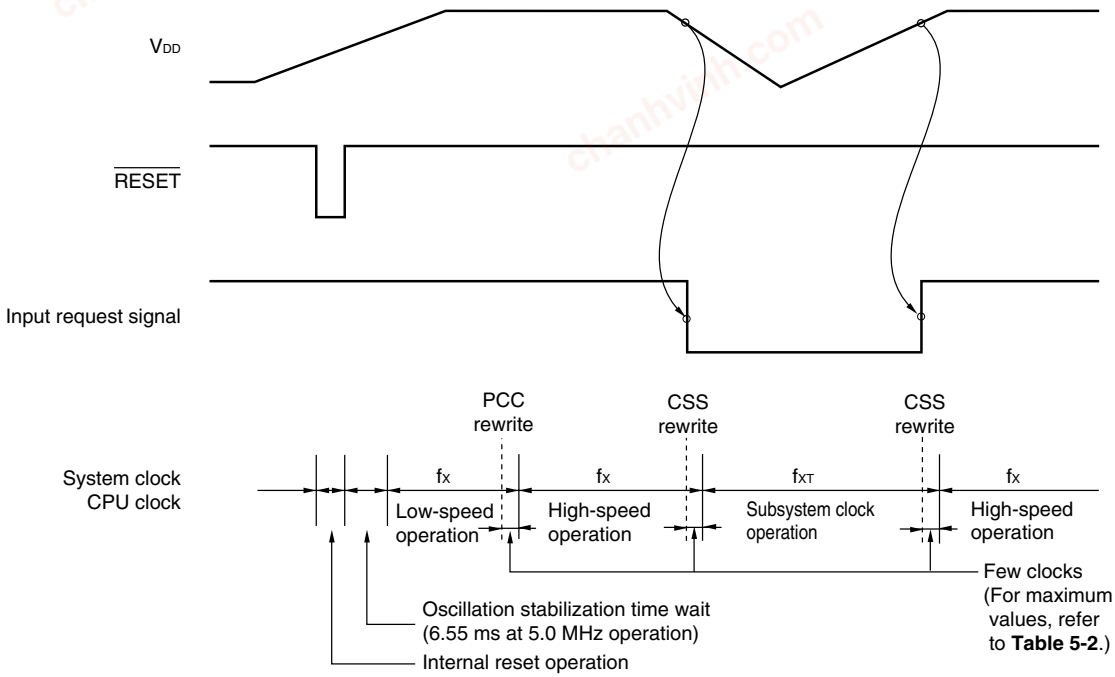
3. ×: don't care

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5.6.2 Switching between system clock and CPU clock

The following figure illustrates how the CPU clock and system clock switch.

Figure 5-8. Example of Switching Between System Clock and CPU Clock



<1> The CPU is reset when the $\overline{\text{RESET}}$ pin is made low on power application. The effect of resetting is released when the $\overline{\text{RESET}}$ pin is later made high, and the main system clock starts oscillating. At this time, the oscillation stabilization time (2^{15}/fx) is automatically secured.
After that, the CPU starts instruction execution at the slow speed of the main system clock (1.6 μs at 5.0 MHz operation).

<2> After the time required for the V_{DD} voltage to rise to the level at which the CPU can operate at high speed has elapsed, bit 1 (PCC1) of the processor clock control register (PCC) is rewritten.

<3> After a few clocks have elapsed, the CPU clock is switched to high-speed (0.4 μs at 5.0 MHz operation), and the CPU starts the high-speed operation.

<4> A drop of the V_{DD} voltage is detected by an interrupt request signal. Bit 4 (CSS0) of the subclock control register (CSS) is rewritten so that the clock is switched to the subsystem clock (at this moment, the subsystem clock must be in the oscillation stabilized status).

<5> After a few clocks have elapsed, the CPU clock is switched to the subsystem clock operation (122 μs at 32.768 kHz operation). (At this time, bit 7 (MCC) of PCC can be set to 1 to stop the main system clock.)

<6> When a recover of the V_{DD} voltage is detected by an interrupt request signal, CSS0 is written so that the CPU clock is switched to the main system clock. (If the main system clock is stopped, set bit 7 (MCC) of PCC to 0 so that the main system clock starts oscillating. After the time required for the oscillation to stabilize has elapsed, rewrite CSS0.)

<7> After a few clocks, the CPU clock is switched to high speed (0.4 μs at 5.0 MHz operation), and the CPU returns to high-speed operation.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

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CHAPTER 6 8-BIT TIMERS 30 AND 40

6.1 8-Bit Timers 30 and 40 Functions

The 8-bit timer in the μPD179327 Subseries has 2 channels (timer 30 and timer 40). The operation modes listed in the following table can be set via mode register settings.

Table 6-1. Operation Modes

Mode \ Channel	Timer 30	Timer 40
8-bit timer counter mode (Discrete mode)	Available	Available
16-bit timer counter mode (Cascade connection mode)	Available	
Carrier generator mode	Available	
PWM output mode	Not available	Available

(1) 8-bit timer counter mode (discrete mode)

The following functions can be used in this mode.

- Interval timer with 8-bit resolution
- Square-wave output with 8-bit resolution (timer 40 only)

(2) 16-bit timer counter mode (cascade connection mode)

Operation as a 16-bit timer is enabled during cascade connection mode.
The following functions can be used in this mode.

- Interval timer with 16-bit resolution
- Square-wave output with 16-bit resolution

(3) Carrier generator mode

The carrier clock generated by timer 40 is output in cycles set by timer 30.

(4) PWM output mode (timer 40 only)

Pulses are output using any duty factor set by timer 40.

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6.2 8-Bit Timers 30 and 40 Configuration

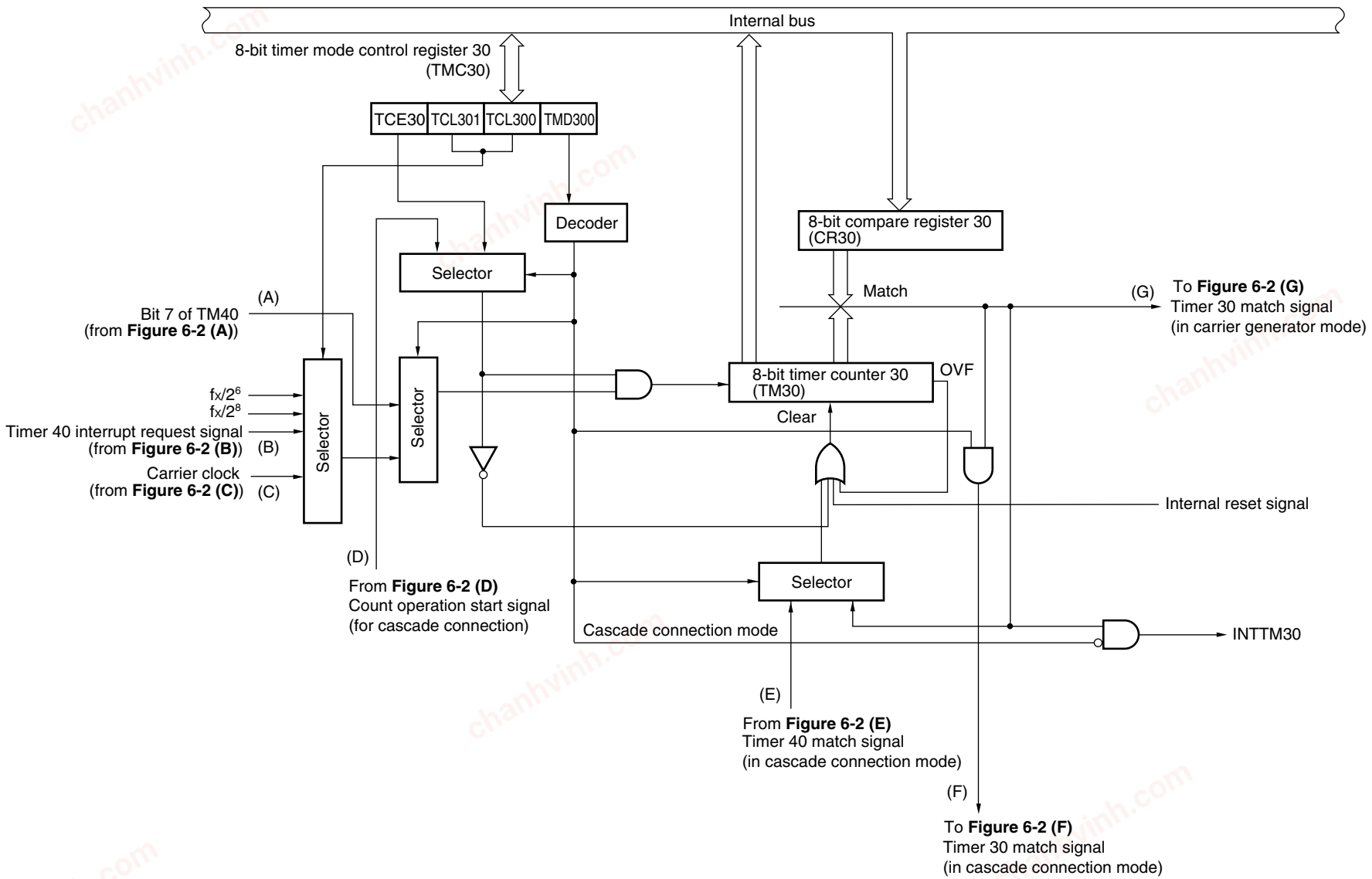
The 8-bit timers 30 and 40 include the following hardware.

Table 6-2. Configuration of 8-Bit Timers 30 and 40

Item	Configuration
Timer counters	8 bits × 2 (TM30, TM40)
Registers	Compare registers: 8 bits × 3 (CR30, CR40, CRH40)
Timer outputs	1 (TO40)
Control registers	8-bit timer mode control register 30 (TMC30) 8-bit timer mode control register 40 (TMC40) Carrier generator output control register 40 (TCA40) Port mode register 6 (PM6) Port 6 (P6)

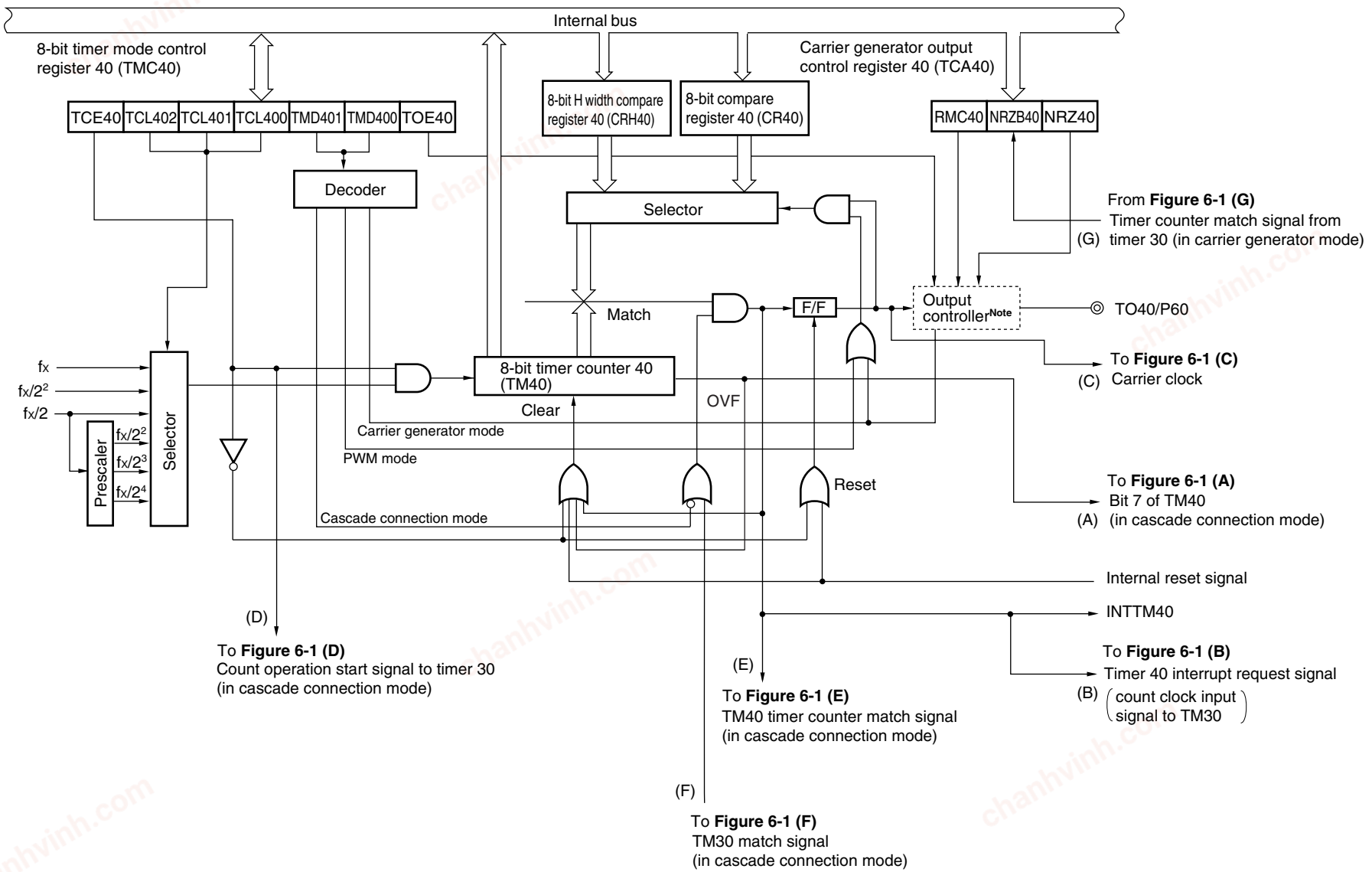
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Figure 6-1. Block Diagram of Timer 30



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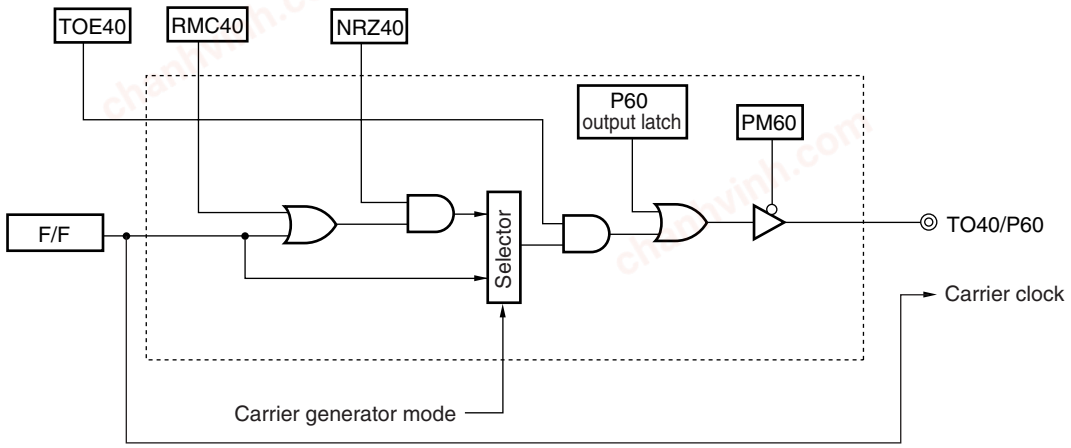
Figure 6-2. Block Diagram of Timer 40



Note Refer to **Figure 6-3** for details.

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Figure 6-3. Block Diagram of Output Controller (Timer 40)



(1) 8-bit compare register 30 (CR30)

This 8-bit register is used to continually compare the value set to CR30 with the count value in 8-bit timer counter 30 (TM30) and to generate an interrupt request (INTTM30) when a match occurs.

CR30 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes CR30 undefined.

Caution CR30 cannot be used in PWM output mode.

(2) 8-bit compare register 40 (CR40)

This 8-bit register is used to continually compare the value set to CR40 with the count value in 8-bit timer counter 40 (TM40) and to generate an interrupt request (INTTM40) when a match occurs. When connected to TM30 via a cascade connection and used as a 16-bit timer, the interrupt request (INTTM40) occurs only when matches occur simultaneously between CR30 and TM30 and between CR40 and TM40 (INTTM30 does not occur).

In carrier generator mode or PWM output mode, CR40 sets the timer output low-level width.

CR40 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes CR40 undefined.

(3) 8-bit H width compare register 40 (CRH40)

In carrier generator mode or PWM output mode, the high-level width of timer output is set by writing a value to CRH40.

The set value of CRH40 is always compared with the TM40 count value, and when they match, an interrupt request (INTTM40) is generated.

CRH40 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes CRH40 undefined.

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(4) 8-bit timer counters 30 and 40 (TM30 and TM40)

These are 8-bit registers that are used to count the count pulse.

TM30 and TM40 are read with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets TM30 and TM40 to 00H.

TM30 and TM40 are cleared to 00H under the following conditions.

(a) Discrete mode

(i) TM30

- After reset
- When TCE30 (bit 7 of 8-bit timer mode control register 30 (TMC30)) is cleared to 0
- When a match occurs between TM30 and CR30
- When the TM30 count value overflows

(ii) TM40

- After reset
- When TCE40 (bit 7 of 8-bit timer mode control register 40 (TMC40)) is cleared to 0
- When a match occurs between TM40 and CR40
- When the TM40 count value overflows

(b) Cascade connection mode (TM30 and TM40 are simultaneously cleared to 00H)

- After reset
- When the TCE40 flag is cleared to 0
- When matches occur simultaneously between TM30 and CR30 and between TM40 and CR40
- When the TM30 and TM40 count values overflow simultaneously

(c) Carrier generator mode/PWM output mode (TM40 only)

- After reset
- When the TCE40 flag is cleared to 0
- When a match occurs between TM40 and CR40
- When a match occurs between TM40 and CRH40
- When the TM40 count value overflows

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6.3 Registers Controlling 8-Bit Timers 30 and 40

8-bit timer 30 and 40 are controlled by the following five registers.

- 8-bit timer mode control register 30 (TMC30)
- 8-bit timer mode control register 40 (TMC40)
- Carrier generator output control register 40 (TCA40)
- Port mode register 6 (PM6)
- Port 6 (P6)

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(1) 8-bit timer mode control register 30 (TMC30)

8-bit timer mode control register 30 (TMC30) is used to control the timer 30 count clock setting and the operation mode setting.

TMC30 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets TMC30 to 00H.

Figure 6-4. Format of 8-Bit Timer Mode Control Register 30

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
TMC30	TCE30	0	0	TCL301	TCL300	0	TMD300	0	FF65H	00H	R/W

TCE30	Control of TM30 count operation[Note 1]
0	Clear TM30 count value and stop operation
1	Start count operation

TCL301	TCL300	Selection of timer 30 count clock
0	0	$f_X/2^6$ (78.1 kHz)
0	1	$f_X/2^8$ (19.5 kHz)
1	0	Timer 40 match signal
1	1	Carrier clock created for timer 40

TMD300	TMD401	TMD400	Selection of operation mode for timer 30 and timer 40[Note 2]
0	0	0	8-bit timer counter mode (discrete mode)
1	0	1	16-bit timer counter mode (cascade connection mode)
0	1	1	Carrier generator mode
0	1	0	Timer 40: PWM output mode Timer 30: 8-bit timer counter mode
Other than above			Setting prohibited

Notes 1. Since the count operation is controlled by TCE40 (bit 7 of TMC40) in cascade connection mode, any setting for TCE30 is ignored.

2. The operation mode selection is set to both the TMC30 register and TMC40 register.

Cautions 1. In cascade connection mode, the timer 40 output signal is forcibly selected for the count clock.

2. Be sure to clear bits 0, 2, 5, and 6 to 0.

Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

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(2) 8-bit timer mode control register 40 (TMC40)

8-bit timer mode control register 40 (TMC40) is used to control the timer 40 count clock setting and the operation mode setting.

TMC40 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets TMC40 to 00H.

Figure 6-5. Format of 8-Bit Timer Mode Control Register 40

Symbol	<7>	6	5	4	3	2	1	<0>	Address	After reset	R/W
TMC40	TCE40	0	TCL402	TCL401	TCL400	TMD401	TMD400	TOE40	FF69H	00H	R/W

TCE40	Control of TM40 count operation[Note 1]
0	Clear TM40 count value and stop operation (the count value is also cleared for TM30 during cascade connection mode)
1	Start count operation (the count operation is also started for TM30 during cascade connection mode)

TCL402	TCL401	TCL400	Selection of timer 40 count clock
0	0	0	f_X (5 MHz)
0	0	1	$f_X/2^2$ (1.25 MHz)
0	1	0	$f_X/2$ (2.5 MHz)
0	1	1	$f_X/2^2$ (1.25 MHz)
1	0	0	$f_X/2^3$ (625 kHz)
1	0	1	$f_X/2^4$ (313 kHz)
Other than above			Setting prohibited

TMD300	TMD401	TMD400	Selection of operation mode for timer 30 and timer 40[Note 2]
0	0	0	8-bit timer counter mode (discrete mode)
1	0	1	16-bit timer counter mode (cascade connection mode)
0	1	1	Carrier generator mode
0	1	0	Timer 40: PWM output mode Timer 30: 8-bit timer counter mode
Other than above			Setting prohibited

TOE40	Control of timer output
0	Output disabled (port mode)
1	Output enabled

Notes 1. Since the count operation is controlled by TCE40 in cascade connection mode, any setting for TCE30 (bit 7 of TMC30) is ignored.

2. The operation mode selection is set to both the TMC30 register and TMC40 register.

Caution Be sure to clear bit 6 to 0.

Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

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(3) Carrier generator output control register 40 (TCA40)

This register is used to set the timer output data in carrier generator mode.

TCA40 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets TCA40 to 00H.

Figure 6-6. Format of Carrier Generator Output Control Register 40

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
TCA40	0	0	0	0	0	RMC40	NRZB40	NRZ40	FF6AH	00H	R/W

RMC40	Control of remote control output
0	When NRZ40 = 1, carrier pulse is output to TO40/P60 pin
1	When NRZ40 = 1, high-level signal is output to TO40/P60 pin

NRZB40	This is the bit that stores the next data to be output to NRZ40. Data is transferred to NRZ40 at the rising edge of the timer 30 match signal. Input the necessary value in NRZB40 in advance by program.

NRZ40	No return zero data
0	Output low-level signal (carrier clock is stopped)
1	Output carrier pulse or high-level signal

Cautions 1. Bits 3 to 7 must be set to 0.

2. TCA40 cannot be set with a 1-bit memory manipulation instruction. Be sure to use an 8-bit memory manipulation instruction to set TCA40.

3. The NRZ40 flag can be written only when carrier generator output is stopped (TOE40 = 0). The data cannot be overwritten when TOE40 = 1.

4. When the carrier generator is stopped once and then started again, NRZB40 does not hold the previous data. Re-set data to NRZB40. At this time, a 1-bit memory manipulation instruction must not be used. Be sure to use an 8-bit memory manipulation instruction.

5. To enable operation in the carrier generator mode, set a value to the compare registers (CR30, CR40, and CRH40), and input the necessary value to the NRZB40 and NRZ40 flags in advance. Otherwise, the signal of the timer match circuit will become unstable and the NRZ40 flag will be undefined.

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(4) Port mode register 6 (PM6)

This register is used to set the I/O mode of port 6 in 1-bit units.

When using the P60/TO40 pin as a timer output, set the PM60 and P60 output latch to 0.

PM6 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PM6 to FFH.

Figure 6-7. Format of Port Mode Register 6

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FF26H	FFH	R/W

PM6n	I/O mode of P6n pin (n = 0, 1)
0	Output mode (output buffer is on)
1	Input mode (output buffer is off)

Caution Bits 2 to 7 must be set to 1.

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6.4 8-Bit Timers 30 and 40 Operation

6.4.1 Operation as 8-bit timer counter

Timers 30 and 40 can be independently used as 8-bit timer counters.
The following modes can be used for the 8-bit timer counters.

- Interval timer with 8-bit resolution
- Square-wave output with 8-bit resolution (timer 40 only)

(1) Operation as interval timer with 8-bit resolution

The interval timer with 8-bit resolution repeatedly generates an interrupt at a time interval specified by the count value preset in 8-bit compare register n0 (CRn0).
To operate 8-bit timer n0 as an interval timer, settings must be made in the following sequence.

<1> Disable operation of 8-bit timer counter n0 (TMn0) (TCEn0 = 0).
<2> Disable timer output of TOn0 (TOEn0 = 0).
<3> Set a count value in CRn0.
<4> Set the operation mode of timer n0 to 8-bit timer counter mode (see **Figures 6-4** and **6-5**).
<5> Set the count clock for timer n0 (see **Tables 6-3** and **6-4**).
<6> Enable the operation of TMn0 (TCEn0 = 1).

When the count value of 8-bit timer counter n0 (TMn0) matches the value set in CRn0, TMn0 is cleared to 00H and continues counting. At the same time, an interrupt request signal (INTTMn0) is generated.
Tables 6-3 and 6-4 show the interval time, and Figures 6-8 to 6-12 show the timing of the interval timer operation.

Caution Be sure to stop the timer operation before overwriting the count clock with different data.

Remark n = 3, 4

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Table 6-3. Interval Time of Timer 30 (at fx = 5.0 MHz Operation)

TCL301	TCL300	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	2^6/fx (12.8 μs)	2^{14}/fx (3.28 ms)	2^4/fx (12.8 μs)
0	1	2^8/fx (51.2 μs)	2^{16}/fx (13.1 ms)	2^8/fx (51.2 μs)
1	0	Input cycle of timer 40 match signal	Input cycle of timer 40 match signal $\times 2^8$	Input cycle of timer 40 match signal
1	1	Carrier clock cycle created with timer 40	Carrier clock cycle created with timer 40 $\times 2^8$	Carrier clock cycle created with timer 40

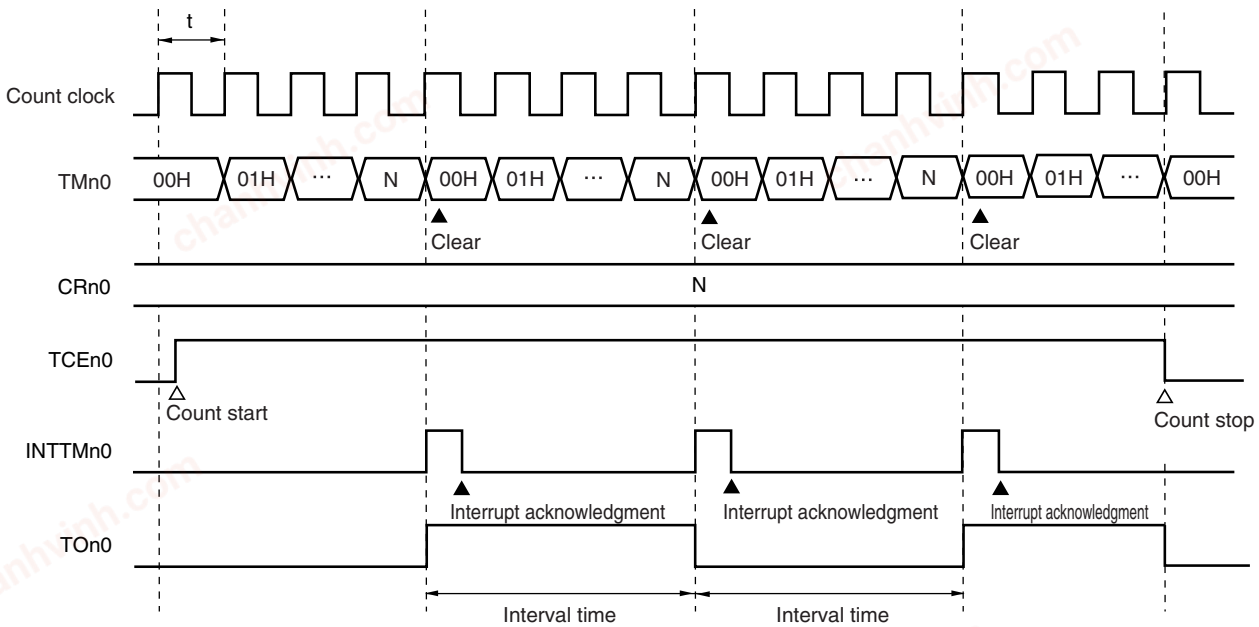
Remark fx: Main system clock oscillation frequency

Table 6-4. Interval Time of Timer 40 (at fx = 5.0 MHz Operation)

TCL402	TCL401	TCL400	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	0	1/fx (0.2 μs)	2^8/fx (51 μs)	1/fx (0.2 μs)
0	0	1	2^2/fx (0.8 μs)	2^{10}/fx (205 μs)	2^2/fx (0.8 μs)
0	1	0	2/fx (0.4 μs)	2^9/fx (102 μs)	2/fx (0.4 μs)
0	1	1	2^2/fx (0.8 μs)	2^{10}/fx (205 μs)	2^2/fx (0.8 μs)
1	0	0	2^3/fx (1.6 μs)	2^{11}/fx (410 μs)	2^3/fx (1.6 μs)
1	0	1	2^4/fx (3.2 μs)	2^{12}/fx (819 μs)	2^4/fx (3.2 μs)

Remark fx: Main system clock oscillation frequency

Figure 6-8. Timing of Interval Timer Operation with 8-Bit Resolution (Basic Operation)

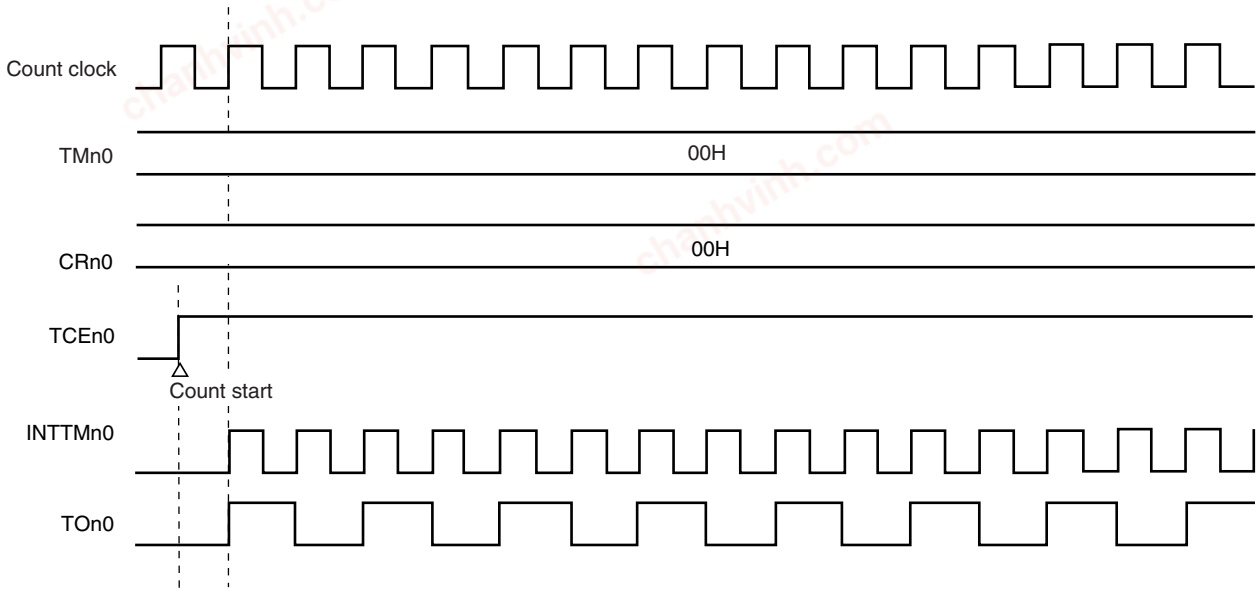


Remarks 1. Interval time = (N + 1) × t: N = 00H to FFH

2. n = 3, 4

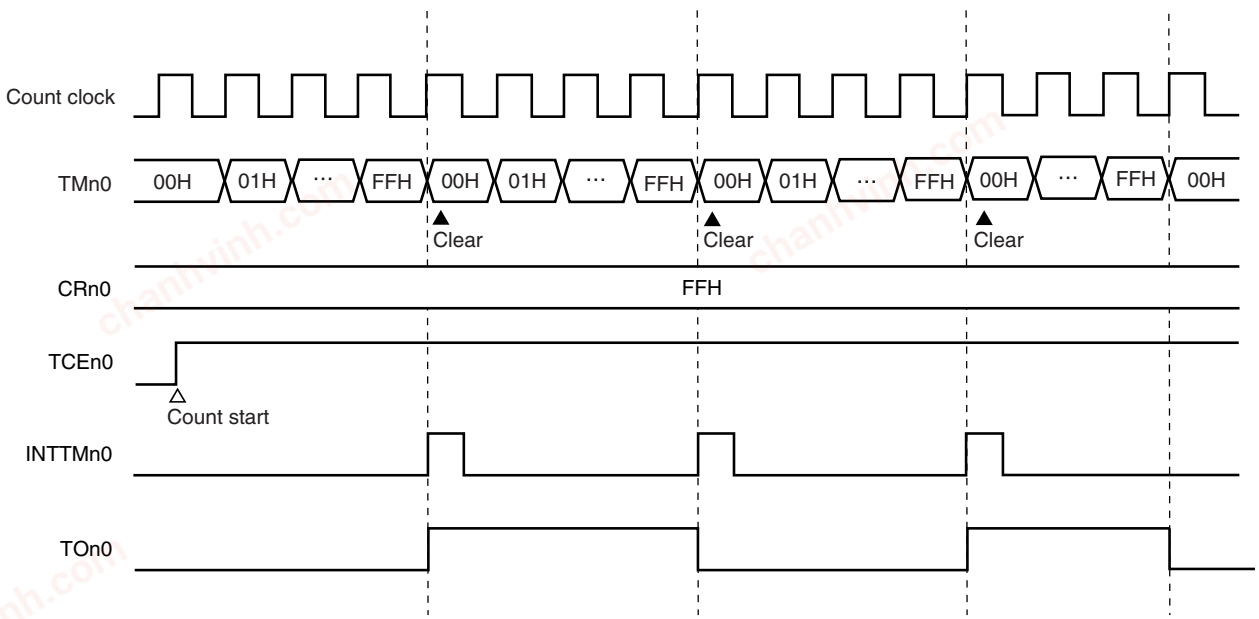
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Figure 6-9. Timing of Interval Timer Operation with 8-Bit Resolution (When CRn0 Is Set to 00H)



Remark n = 3, 4

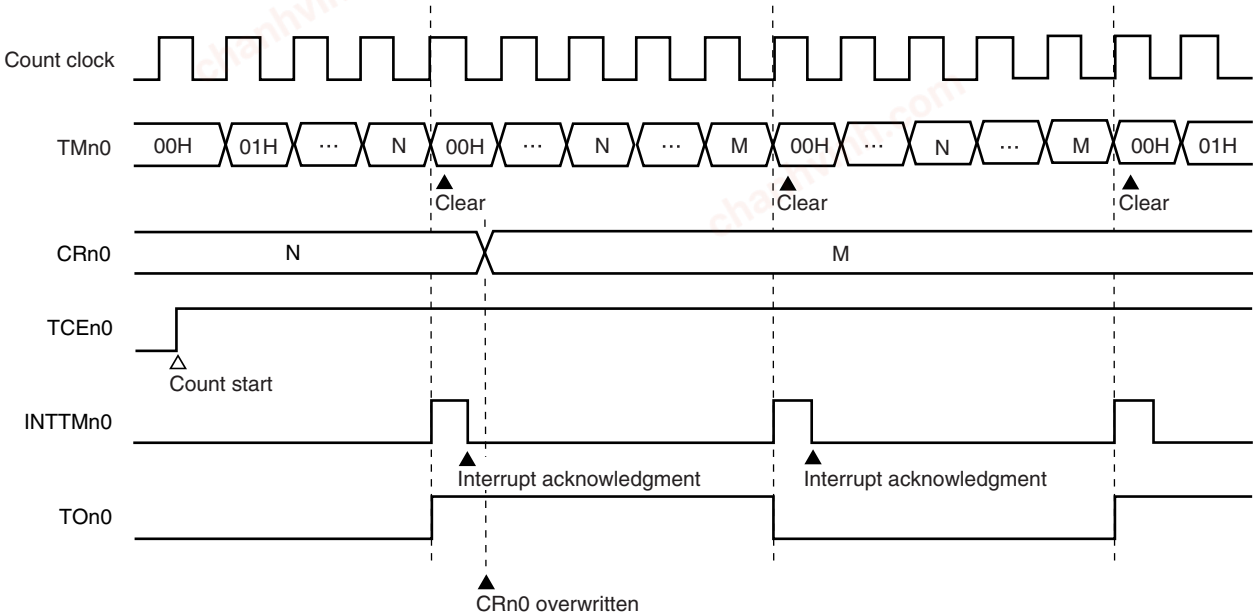
Figure 6-10. Timing of Interval Timer Operation with 8-Bit Resolution (When CRn0 Is Set to FFH)



Remark n = 3, 4

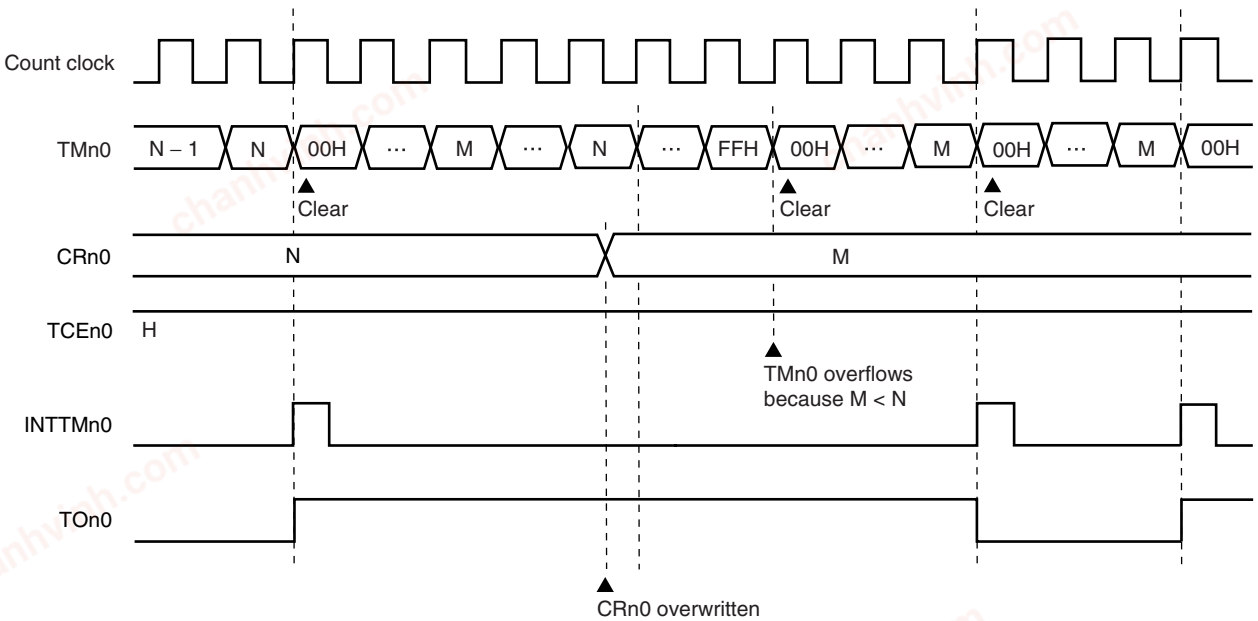
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Figure 6-11. Timing of Interval Timer Operation with 8-Bit Resolution (When CRn0 Changes from N to M (N < M))



Remark n = 3, 4

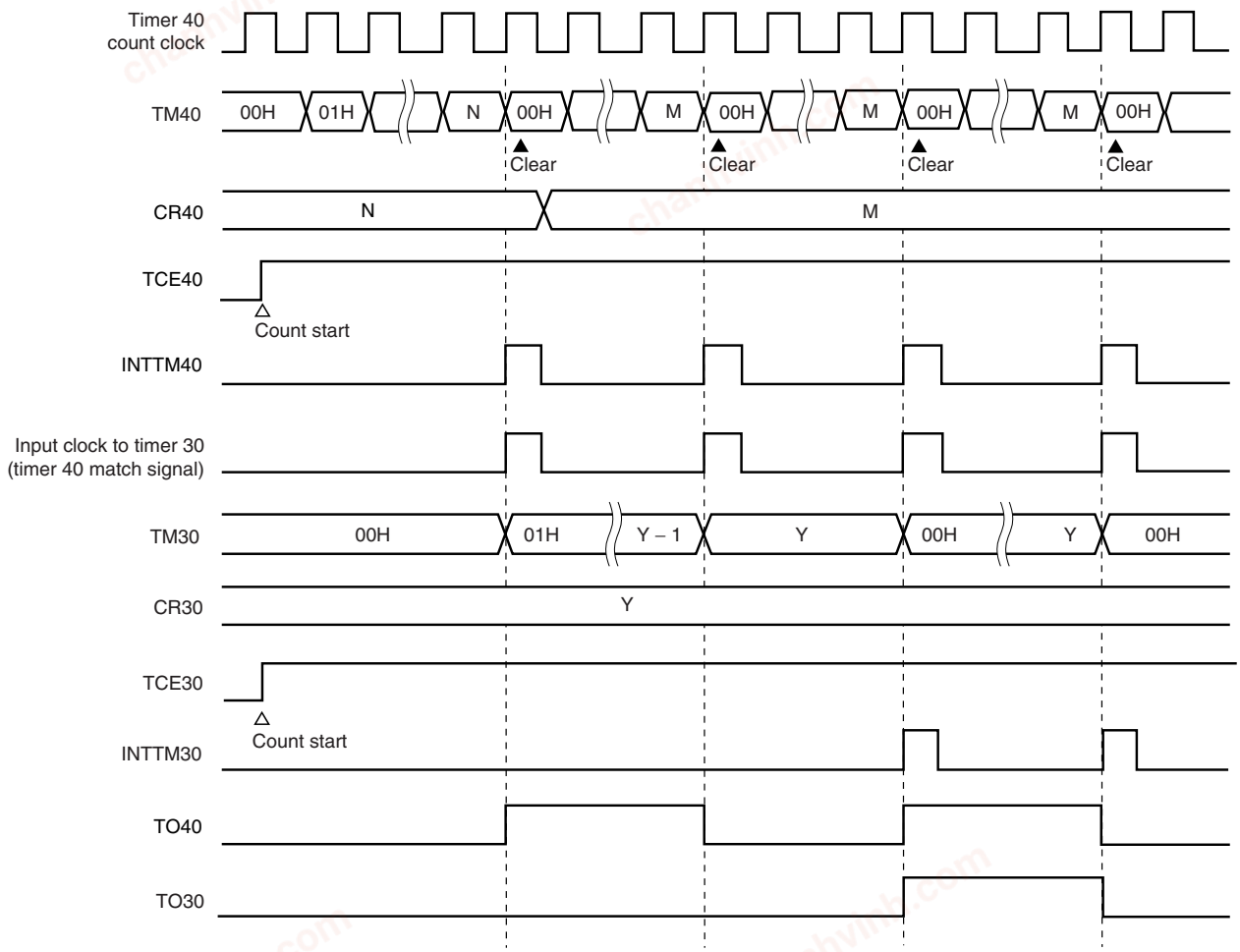
Figure 6-12. Timing of Interval Timer Operation with 8-Bit Resolution (When CRn0 Changes from N to M (N > M))



Remark n = 3, 4

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Figure 6-13. Timing of Interval Timer Operation with 8-Bit Resolution (When Timer 40 Match Signal Is Selected for Timer 30 Count Clock)



Remark n = 3, 4

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(2) Operation as square-wave output with 8-bit resolution (timer 40 only)

Square waves of any frequency can be output at an interval specified by the value preset in 8-bit compare register 40 (CR40).

To operate timer 40 for square-wave output, settings must be made in the following sequence.

<1> Set P60 to output mode (PM60 = 0).
<2> Set the output latch of P60 to 0.
<3> Disable operation of timer counter 40 (TM40) (TCE40 = 0).
<4> Set a count clock for timer 40 and enable output of TO40 (TOE40 = 1).
<5> Set a count value in CR40.
<6> Enable the operation of TM40 (TCE40 = 1).

When the count value of TM40 matches the value set in CR40, the TO40 pin output will be inverted. Through application of this mechanism, square waves of any frequency can be output. As soon as a match occurs, TM40 is cleared to 00H and continues counting. At the same time, an interrupt request signal (INTTM40) is generated.

The square-wave output is cleared to 0 by setting TCE40 to 0.

Table 6-5 shows the square-wave output range, and Figure 6-14 shows the timing of square-wave output.

Caution Be sure to stop the timer operation before overwriting the count clock with different data.

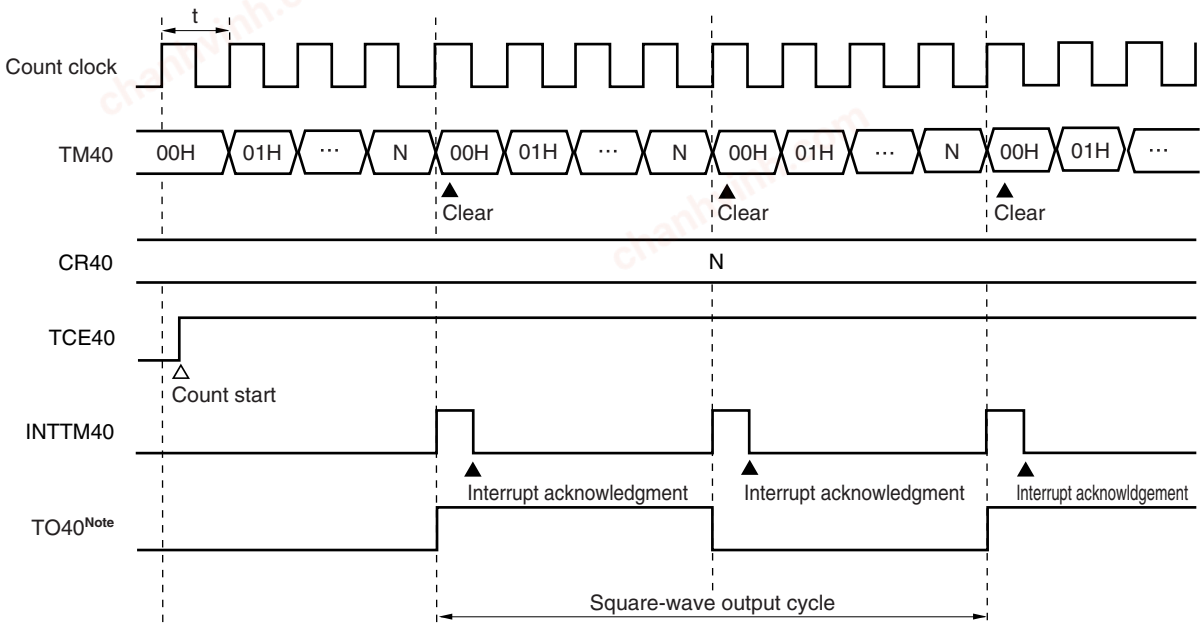
Table 6-5. Square-Wave Output Range of Timer 40 (at f_X = 5.0 MHz Operation)

TCL402	TCL401	TCL400	Minimum Pulse Width	Maximum Pulse Width	Resolution
0	0	0	$1/f_X$ (0.2 μs)	$2^8/f_X$ (51 μs)	$1/f_X$ (0.2 μs)
0	0	1	$2^2/f_X$ (0.8 μs)	$2^{10}/f_X$ (205 μs)	$2^2/f_X$ (0.8 μs)
0	1	0	$2/f_X$ (0.4 μs)	$2^9/f_X$ (102 μs)	$2/f_X$ (0.4 μs)
0	1	1	$2^2/f_X$ (0.8 μs)	$2^{10}/f_X$ (205 μs)	$2^2/f_X$ (0.8 μs)
1	0	0	$2^3/f_X$ (1.6 μs)	$2^{11}/f_X$ (410 μs)	$2^3/f_X$ (1.6 μs)
1	0	1	$2^4/f_X$ (3.2 μs)	$2^{12}/f_X$ (819 μs)	$2^4/f_X$ (3.2 μs)

Remark f_X: Main system clock oscillation frequency

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Figure 6-14. Timing of Square-Wave Output with 8-Bit Resolution



Note The initial value of TO40 is low level when output is enabled (TOE40 = 1).

Remark Square-wave output cycle = 2 (N + 1) × t: N = 00H to FFH

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6.4.2 Operation as 16-bit timer counter

Timers 30 and 40 can be used as 16-bit timer counters via a cascade connection. In this case, 8-bit timer counter 30 (TM30) is the higher 8 bits and 8-bit timer counter 40 (TM40) is the lower 8 bits. 8-bit timer 40 controls reset and clear.

The following modes can be used for the 16-bit timer counter.

- Interval timer with 16-bit resolution
- Square-wave output with 16-bit resolution

(1) Operation as interval timer with 16-bit resolution

The interval timer with 16-bit resolution repeatedly generates an interrupt at a time interval specified by the count value preset in 8-bit compare register 30 (CR30) and 8-bit compare register 40 (CR40).

To operate as an interval timer with 16-bit resolution, settings must be made in the following sequence.

<1> Disable operation of 8-bit timer counter 30 (TM30) and 8-bit timer counter 40 (TM40) (TCE30 = 0, TCE40 = 0).
<2> Disable timer output of TO40 (TOE40 = 0).
<3> Set the count clock for timer 40 (see **Table 6-4**).
<4> Set the operation mode of timer 30 and timer 40 to 16-bit timer counter mode (see **Figures 6-4** and **6-5**).
<5> Set a count value in CR30 and CR40.
<6> Enable the operation of TM30 and TM40 (TCE40 = 1[Note]).

Note Start and clear of the timer in the 16-bit timer counter mode are controlled by TCE40 (the value of TCE30 is invalid).

When the count values of TM30 and TM40 match the values set in CR30 and CR40 respectively, both TM30 and TM40 are simultaneously cleared to 00H and counting continues. At the same time, an interrupt request signal (INTTM40) is generated (INTTM30 is not generated).

Table 6-6 shows interval time, and Figure 6-15 shows the timing of the interval timer operation.

Caution Be sure to stop the timer operation before overwriting the count clock with different data.

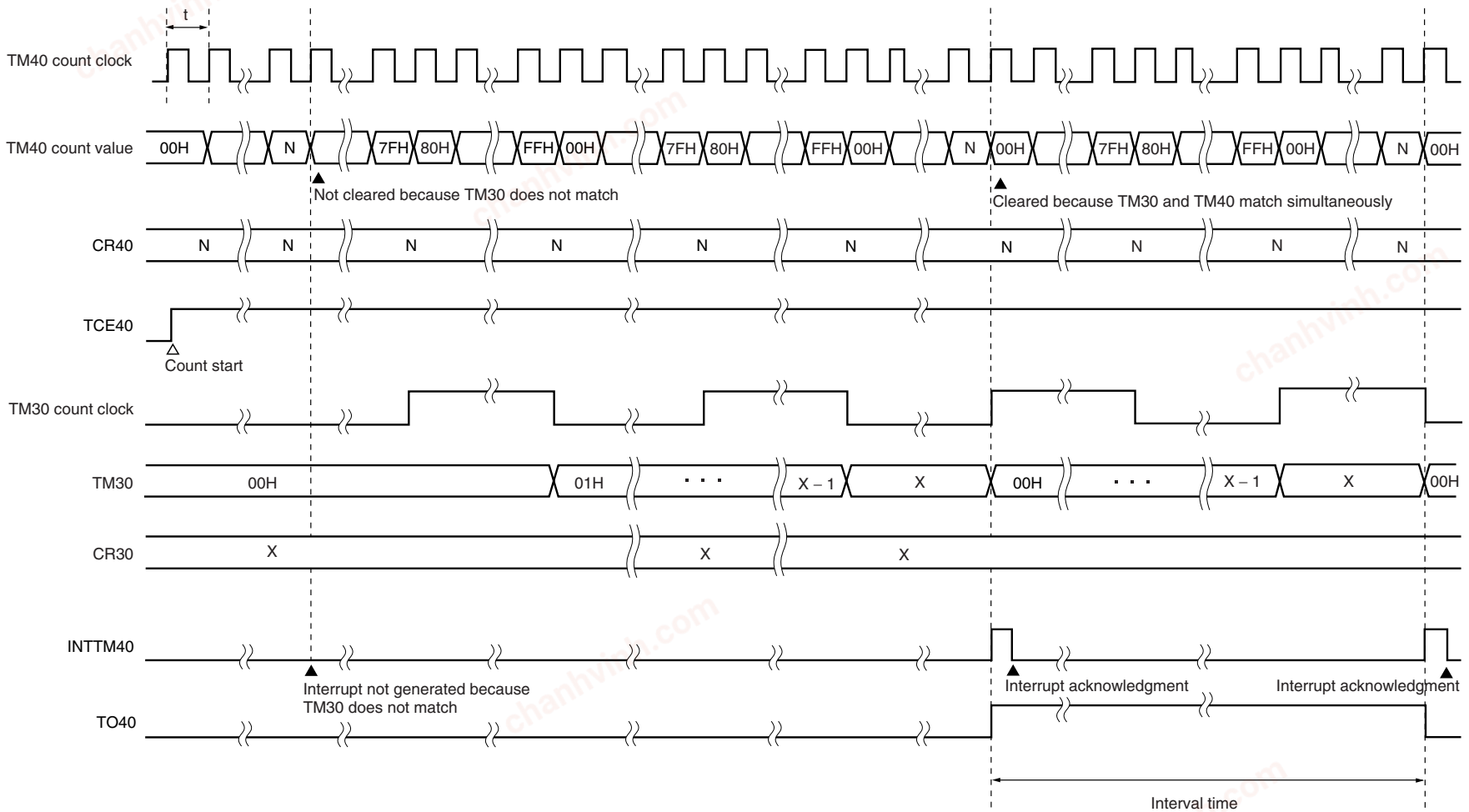
Table 6-6. Interval Time with 16-Bit Resolution (at fx = 5.0 MHz Operation)

TCL402	TCL401	TCL400	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	0	1/fx (0.2 μs)	2^{16}/fx (13.1 ms)	1/fx (0.2 μs)
0	0	1	2^2/fx (0.8 μs)	2^{18}/fx (52.4 ms)	2^2/fx (0.8 μs)
0	1	0	2/fx (0.4 μs)	2^{17}/fx (26.2 ms)	2/fx (0.4 μs)
0	1	1	2^2/fx (0.8 μs)	2^{18}/fx (52.4 ms)	2^2/fx (0.8 μs)
1	0	0	2^3/fx (1.6 μs)	2^{19}/fx (105 ms)	2^3/fx (1.6 μs)
1	0	1	2^4/fx (3.2 μs)	2^{20}/fx (210 ms)	2^4/fx (3.2 μs)

Remark fx: Main system clock oscillation frequency

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Figure 6-15. Timing of Interval Timer Operation with 16-Bit Resolution



Remark Interval time = $(256X + N + 1) \times t$: X = 00H to FFH, N = 00H to FFH

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(2) Operation as square-wave output with 16-bit resolution

Square waves of any frequency can be output at an interval specified by the count value preset in CR30 and CR40.

To operate as a square-wave output with 16-bit resolution, settings must be made in the following sequence.

<1> Disable operation of TM30 and TM40 (TCE30 = 0, TCE40 = 0).
<2> Disable output of TO40 (TOE40 = 0).
<3> Set a count clock for timer 40.
<4> Set P60 to output mode (PM60 = 0) and P60 output latch to 0 and enable TO40 output (TOE40 = 1).
<5> Set count values in CR30 and CR40.
<6> Enable the operation of TM40 (TCE40 = 1[Note]).

Note Start and clear of the timer in the 16-bit timer counter mode are controlled by TCE40 (the value of TCE30 is invalid).

When the count values of TM30 and TM40 simultaneously match the values set in CR30 and CR40 respectively, the TO40 pin output will be inverted. Through application of this mechanism, square waves of any frequency can be output. As soon as a match occurs, TM30 and TM40 are cleared to 00H and counting continues. At the same time, an interrupt request signal (INTTM40) is generated (INTTM30 is not generated).

The square-wave output is cleared to 0 by setting TCE40 to 0.

Table 6-7 shows the square wave-output range, and Figure 6-16 shows timing of square-wave output.

Caution Be sure to stop the timer operation before overwriting the count clock with different data.

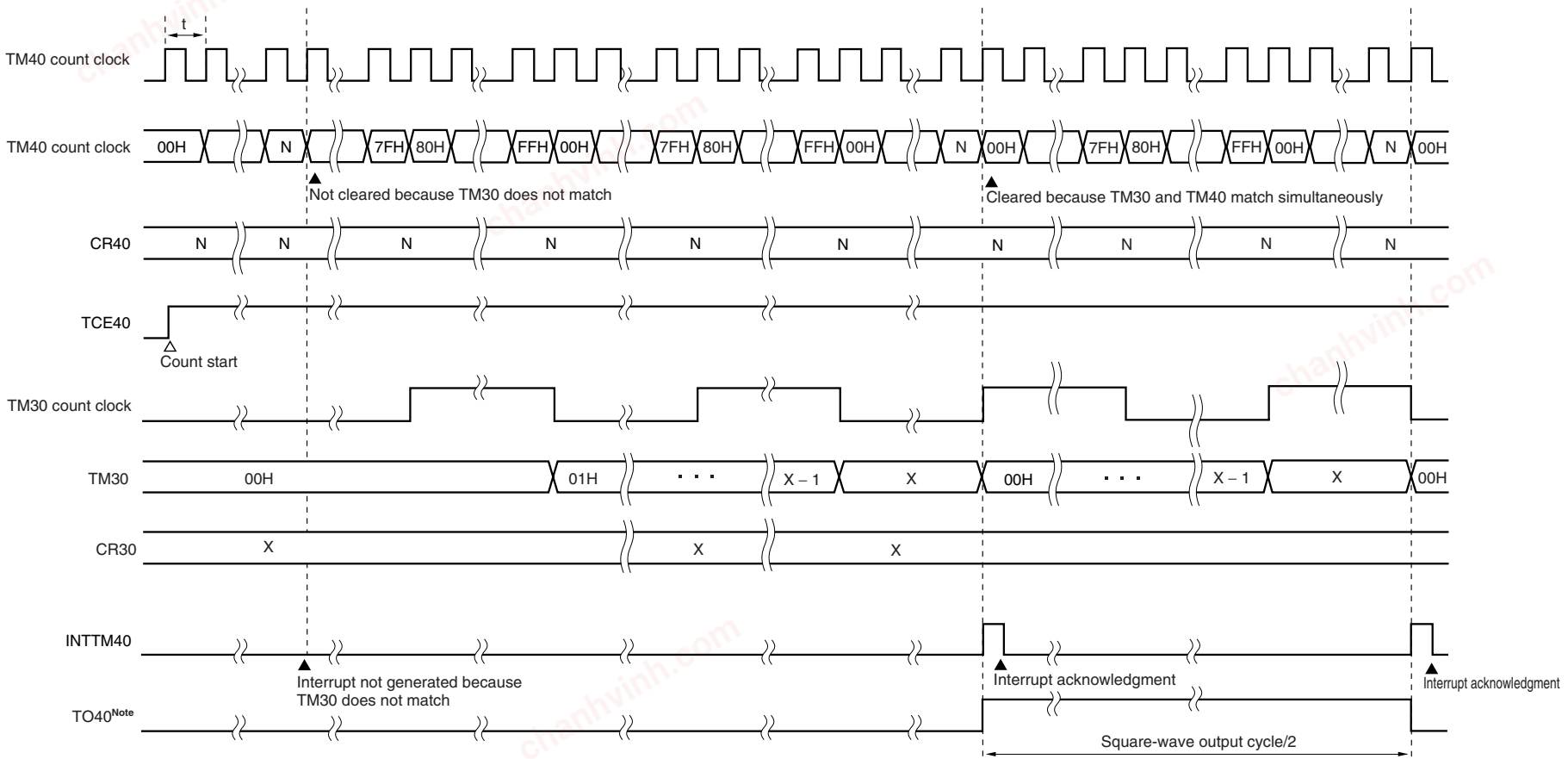
Table 6-7. Square-Wave Output Range with 16-Bit Resolution (at fx = 5.0 MHz Operation)

TCL402	TCL401	TCL400	Minimum Pulse Width	Maximum Pulse Width	Resolution
0	0	0	1/fx (0.2 μs)	2^{16}/fx (13.1 ms)	1/fx (0.2 μs)
0	0	1	2^2/fx (0.8 μs)	2^{18}/fx (52.4 ms)	2^2/fx (0.8 μs)
0	1	0	2/fx (0.4 μs)	2^{17}/fx (26.2 ms)	2/fx (0.4 μs)
0	1	1	2^2/fx (0.8 μs)	2^{18}/fx (52.4 ms)	2^2/fx (0.8 μs)
1	0	0	2^3/fx (1.6 μs)	2^{19}/fx (105 ms)	2^3/fx (1.6 μs)
1	0	1	2^4/fx (3.2 μs)	2^{20}/fx (210 ms)	2^4/fx (3.2 μs)

Remark fx: Main system clock oscillation frequency

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Figure 6-16. Timing of Square-Wave Output with 16-Bit Resolution



Note The initial value of TO40 is low level when output is enabled (TOE40 = 1).

Remark Square-wave output cycle = 2 (256X + N + 1) × t: X = 00H to FFH, N = 00H to FFH

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6.4.3 Operation as carrier generator

An arbitrary carrier clock generated by TM40 can be output in the cycle set in TM30.

To operate timers 30 and 40 as carrier generators, settings must be made in the following sequence.

<1> Disable operation of TM30 and TM40 (TCE30 = 0, TCE40 = 0).
<2> Disable timer output of TO40 (TOE40 = 0).
<3> Set count values in CR30, CR40, and CRH40.
<4> Set the operation mode of timer 30 and timer 40 to carrier generator mode (see **Figures 6-4** and **6-5**).
<5> Set the count clock for timer 30 and timer 40.
<6> Set remote control output to carrier pulse (RMC40 (bit 2 of carrier generator output control register 40 (TCA40)) = 0).
Input the required value to NRZB40 (bit 1 of TCA40) by program.
Input a value to NRZ40 (bit 0 of TCA40) before it is reloaded from NRZB40.
<7> Set P60 to output mode (PM60 = 0) and the P60 output latch to 0 and enable TO40 output by setting TOE40 to 1.
<8> Enable the operation of TM30 and TM40 (TCE30 = 1, TCE40 = 1).
<9> Save the NRZB40 value to a general-purpose register.
<10> When INTTM30 rises, the NRZB40 value is transferred to NRZ40. After that, rewrite TCA40 using an 8-bit memory manipulation instruction. Input the value to be transferred next to NRZ40 to NRZB40, and input the value saved in step <9> to NRZ40.
<11> Generate the desired carrier signal by repeating steps <9> and <10>.

The operation of the carrier generator is as follows.

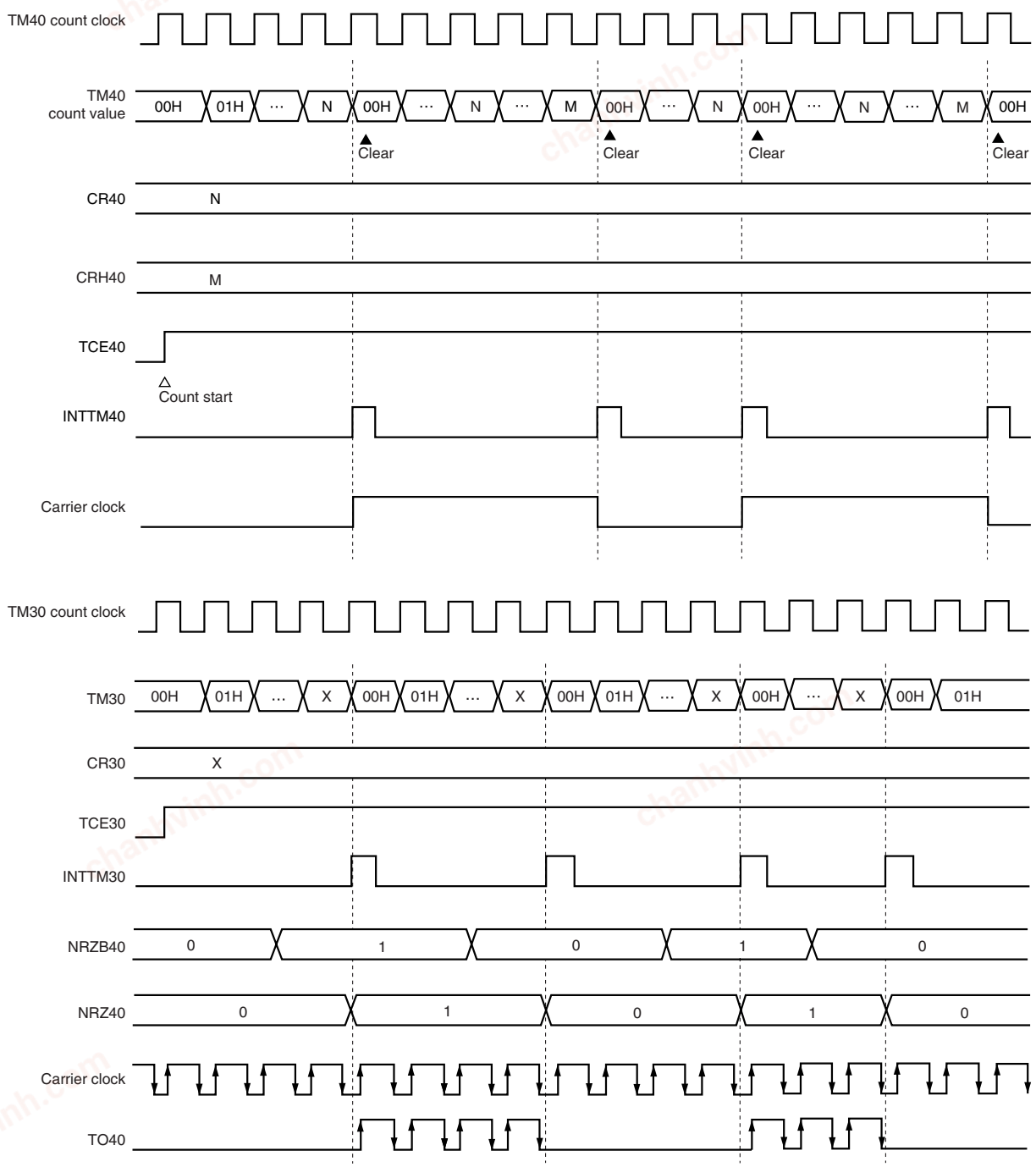
<1> When the count the value of TM40 matches the value set in CR40, an interrupt request signal (INTTM40) is generated and the output of timer 40 is inverted, which makes the compare register switch from CR40 to CRH40.
<2> After that, when the count the value of TM40 matches the value set in CRH40, an interrupt request signal (INTTM40) is generated and the output of timer 40 is inverted again, which makes the compare register switch from CRH40 to CR40.
<3> The carrier clock is generated by repeating <1> and <2> above.
<4> When the count value of TM30 matches the value set in CR30, an interrupt request signal (INTTM30) is generated. The rising edge of INTTM30 is the data reload signal of NRZB40 and is transferred to NRZ40.
<5> When NRZ40 is 1, a carrier clock is output from TO40 pin.

Cautions
1. **TCA40 cannot be set with a 1-bit memory manipulation instruction. Be sure to use an 8-bit memory manipulation instruction.**
2. **The NRZ40 flag can be rewritten only when the carrier generator output is stopped (TOE40 = 0). The data of the flag is not changed even if a write instruction is executed while TOE40 = 1.**
3. **When the carrier generator is stopped once and then started again, NRZB40 does not hold the previous data. Re-set data to NRZB40. At this time, a 1-bit memory manipulation instruction must not be used. Be sure to use an 8-bit memory manipulation instruction.**
4. **To enable operation in the carrier generator mode, set a value to the compare registers (CR30, CR40, and CRH40), and input the necessary value to the NRZB40 and NRZ40 flags in advance. Otherwise, the signal of the timer match circuit will become unstable and the NRZ40 flag will be undefined.**

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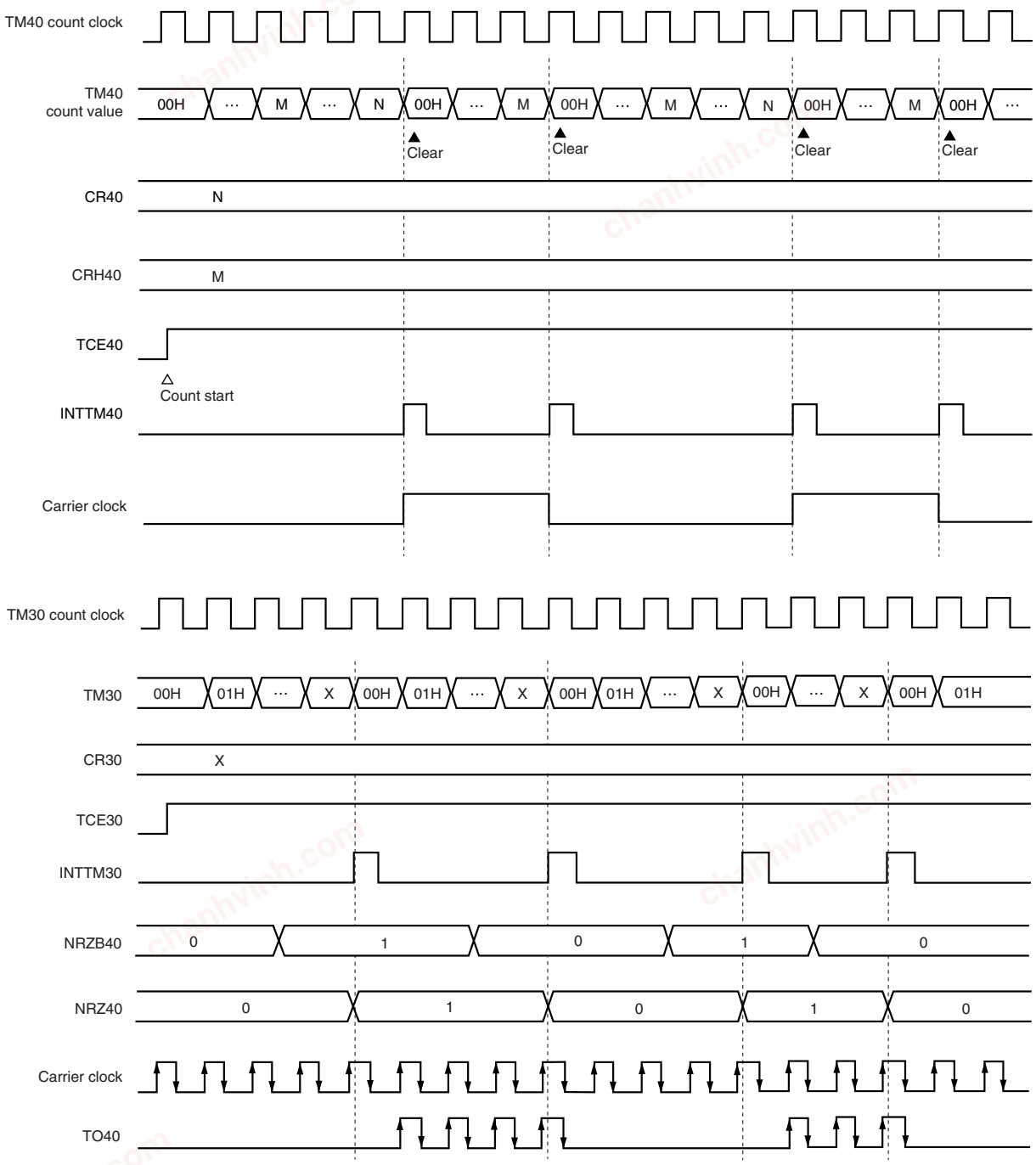
Figures 6-17 to 6-19 show the operation timing of the carrier generator.

Figure 6-17. Timing of Carrier Generator Operation (When CR40 = N, CRH40 = M (M > N))



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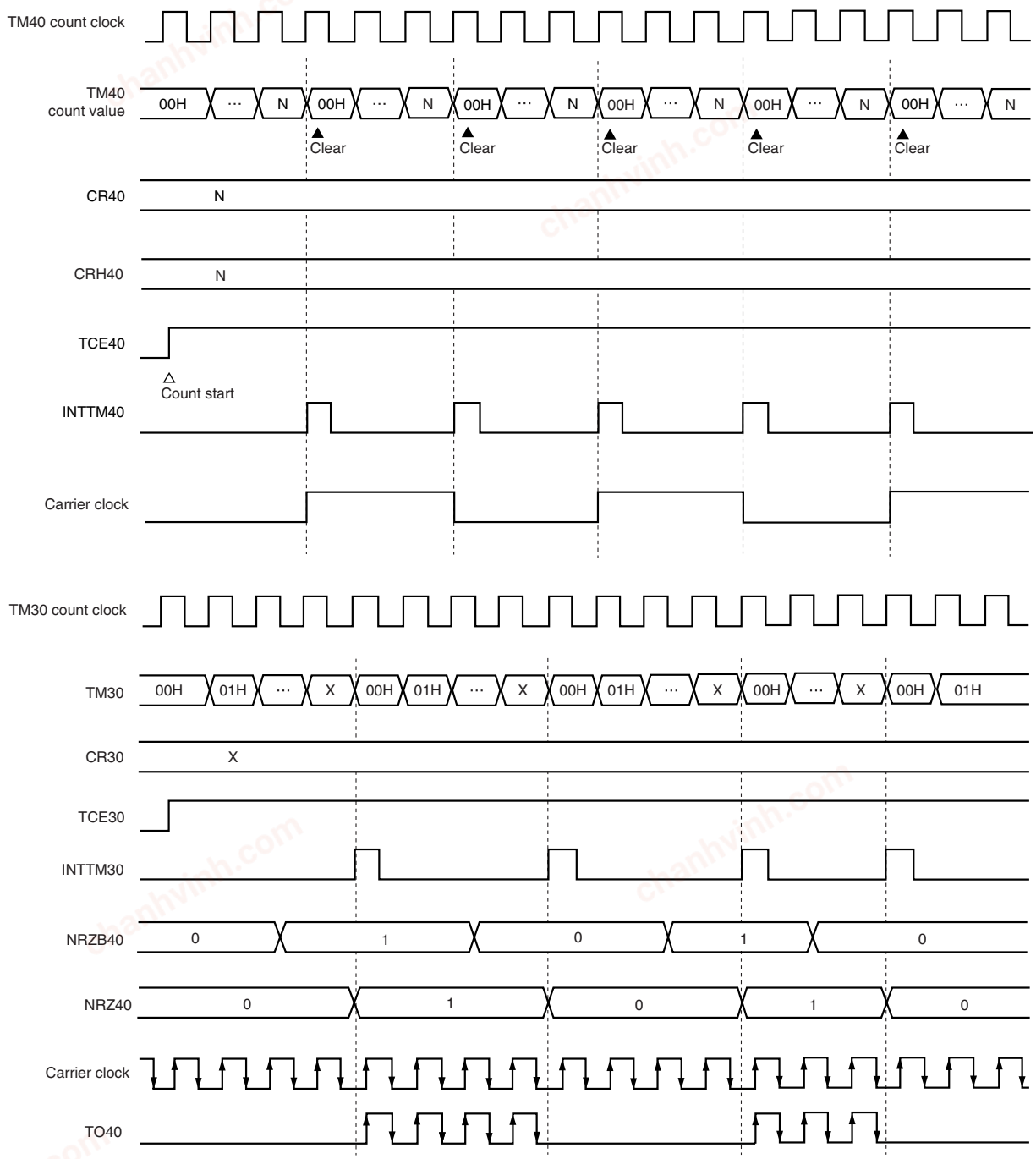
Figure 6-18. Timing of Carrier Generator Operation (When CR40 = N, CRH40 = M (M < N))



Remark This figure shows an example of when the NRZ40 value is changed while the carrier clock is high level.

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Figure 6-19. Timing of Carrier Generator Operation (When CR40 = CRH40 = N)



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6.4.4 Operation as PWM output (timer 40 only)

In the PWM output mode, a pulse of any duty ratio can be output by setting a low-level width using CR40 and a high-level width using CRH40.

To operate timer 40 in PWM output mode, settings must be made in the following sequence.

<1> Disable operation of TM40 (TCE40 = 0).
<2> Disable timer output of TO40 (TOE40 = 0).
<3> Set count values in CR40 and CRH40.
<4> Set the operation mode of timer 40 to carrier generator mode (see **Figure 6-5**).
<5> Set the count clock for timer 40.
<6> Set P60 to output mode (PM60 = 0) and the P60 output latch to 0 and enable timer output of TO40 (TOE40 = 1).
<7> Enable the operation of TM40 (TCE40 = 1).

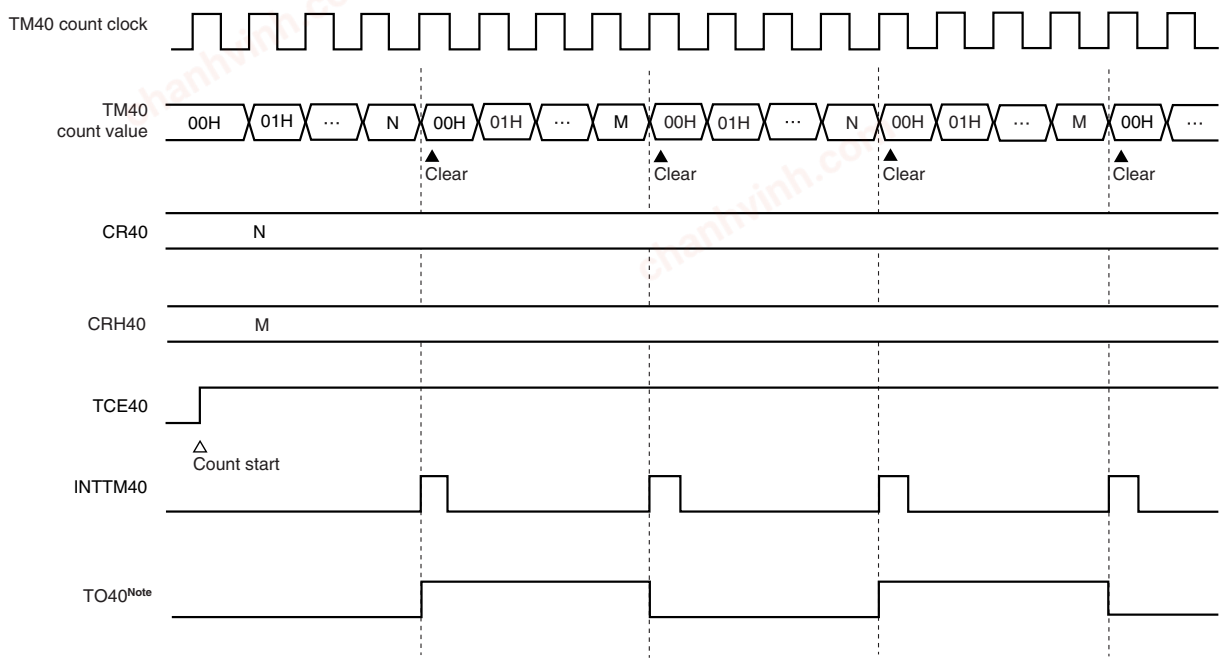
The operation in the PWM output mode is as follows.

<1> When the count value of TM40 matches the value set in CR40, an interrupt request signal (INTTM40) is generated and the output of timer 40 is inverted, which makes the compare register switch from CR40 to CRH40.
<2> A match between TM40 and CR40 clears the TM40 value to 00H and then counting starts again.
<3> After that, when the count value of TM40 matches the value set in CRH40, an interrupt request signal (INTTM40) is generated and the output of timer 40 is inverted again, which makes the compare register switch from CRH40 to CR40.
<4> A match between TM40 and CRH40 clears the TM40 value to 00H and then counting starts again.

A pulse of any duty ratio is output by repeating <1> to <4> above. Figures 6-20 and 6-21 show the operation timing in the PWM output mode.

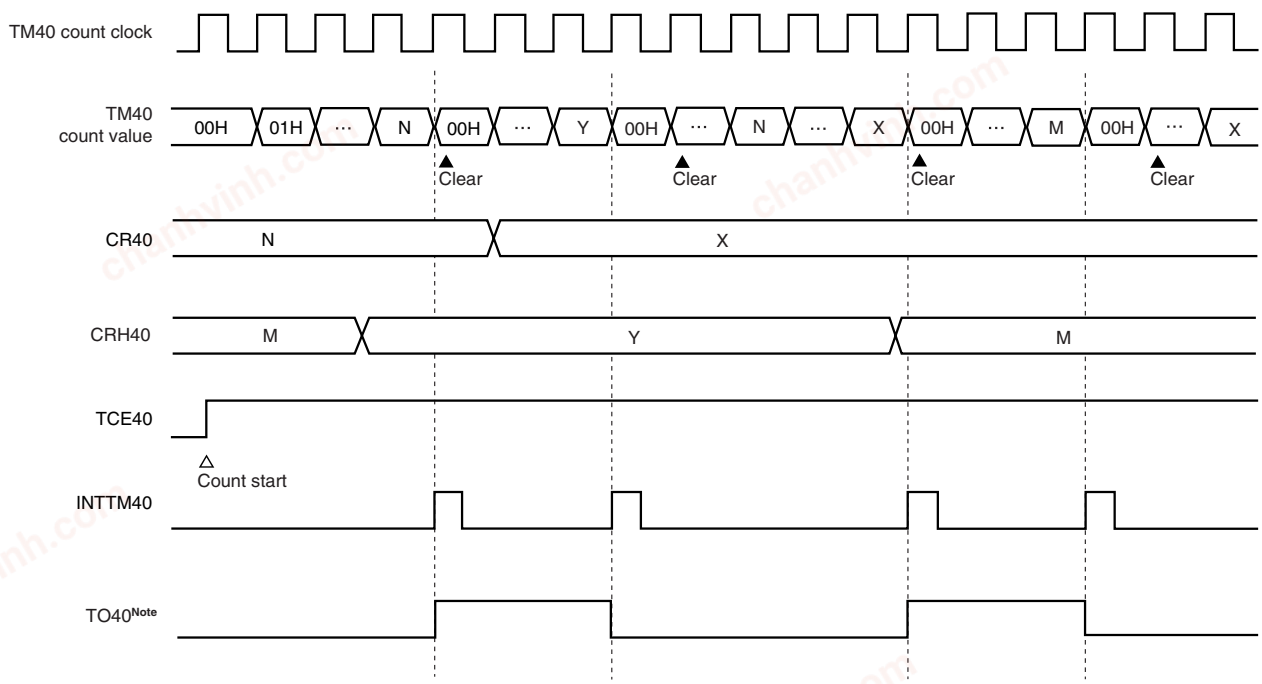
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Figure 6-20. PWM Output Mode Timing (Basic Operation)



Note The initial value of TO40 is low level when output is enabled (TOE40 = 1).

Figure 6-21. PWM Output Mode Timing (When CR40 and CRH40 Are Overwritten)



Note The initial value of TO40 is low level when output is enabled (TOE40 = 1).

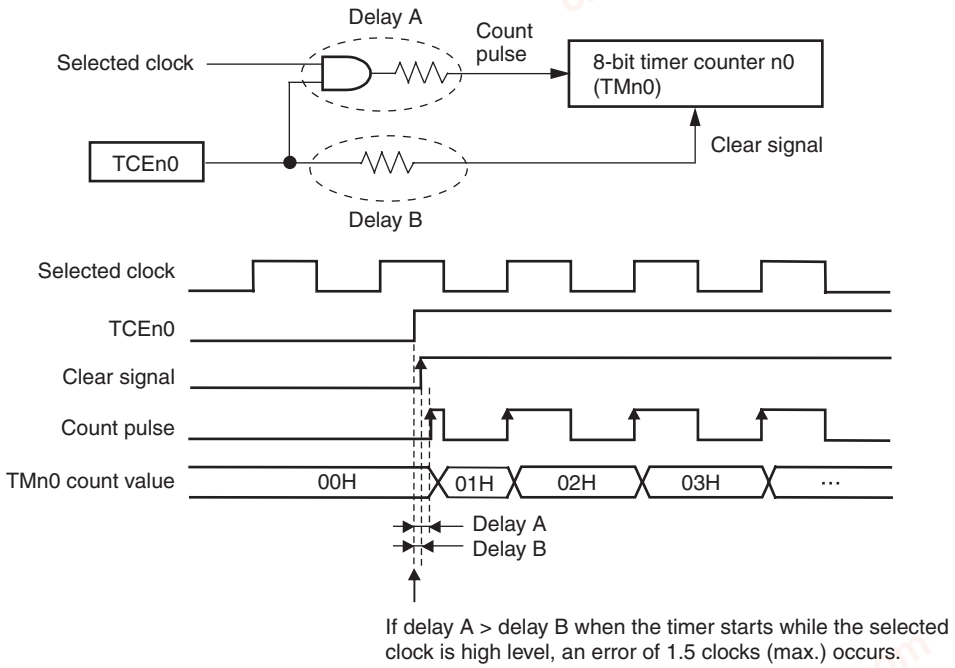
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6.5 Notes on Using 8-Bit Timers 30 and 40

(1) Error on starting timer

An error of up to 1.5 clocks is included in the time between when the timer is started and a match signal is generated. This is because the counter may be incremented by detecting a rising edge at the timing at which the timer starts while the count clock is high level (see **Figure 6-22**).

Figure 6-22. Case in Which Error of 1.5 Clocks (Max.) Occurs



If delay A > delay B when the timer starts while the selected clock is high level, an error of 1.5 clocks (max.) occurs.

Remark n = 3, 4

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CHAPTER 7 WATCH TIMER

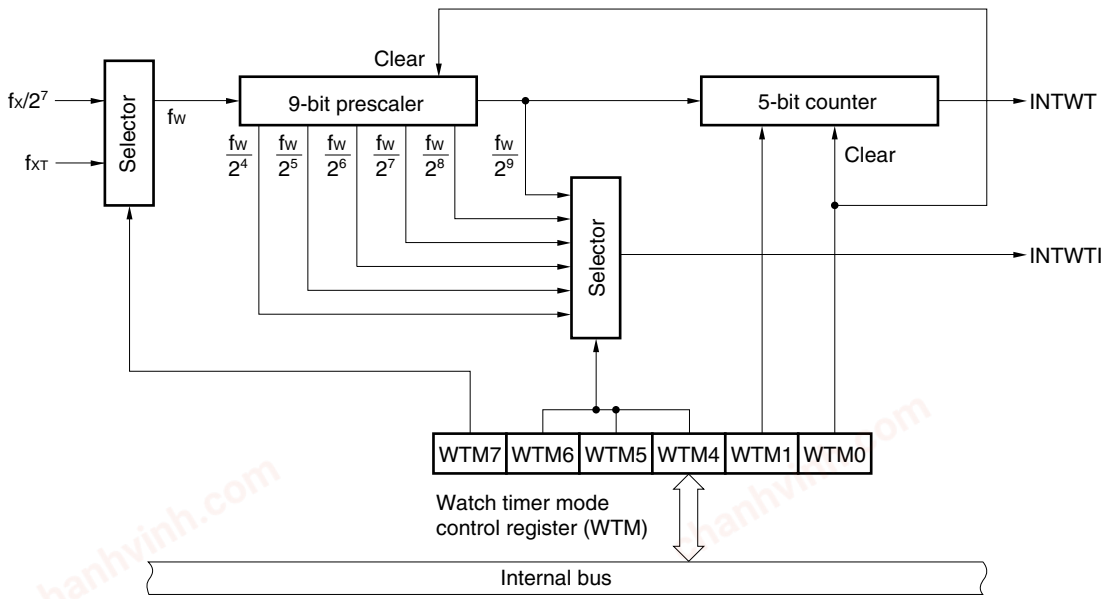
7.1 Watch Timer Functions

The watch timer has the following functions.

- Watch timer
- Interval timer

The watch and interval timers can be used at the same time.
Figure 7-1 shows a block diagram of the watch timer.

Figure 7-1. Block Diagram of Watch Timer



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(1) Watch timer

The 4.19 MHz main system clock or 32.768 kHz subsystem clock is used to generate an interrupt request (INTWT) at 0.5-second intervals.

Caution When the main system clock is operating at 5.0 MHz, it cannot be used to generate a 0.5-second interval. In this case, the subsystem clock, which operates at 32.768 kHz, should be used instead.

(2) Interval timer

The interval timer is used to generate an interrupt request (INTWT) at specified intervals.

Table 7-1. Interval Time of Interval Timer

Interval	At f_X = 5.0 MHz Operation	At f_X = 4.19 MHz Operation	At f_{XT} = 32.768 kHz Operation
$2^4 \times 1/f_W$	409.6 μs	488 μs	488 μs
$2^5 \times 1/f_W$	819.2 μs	977 μs	977 μs
$2^6 \times 1/f_W$	1.64 ms	1.95 ms	1.95 ms
$2^7 \times 1/f_W$	3.28 ms	3.91 ms	3.91 ms
$2^8 \times 1/f_W$	6.55 ms	7.81 ms	7.81 ms
$2^9 \times 1/f_W$	13.1 ms	15.6 ms	15.6 ms

Remarks 1. f_W: Watch timer clock frequency ($f_X/2^7$ or f_{XT})
2. f_X: Main system clock oscillation frequency
3. f_{XT}: Subsystem clock oscillation frequency

7.2 Watch Timer Configuration

The watch timer includes the following hardware.

Table 7-2. Configuration of Watch Timer

Item	Configuration
Counter	5 bits × 1
Prescaler	9 bits × 1
Control register	Watch timer mode control register (WTM)

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7.3 Register Controlling Watch Timer

The watch timer mode control register (WTM) is used to control the watch timer.

- Watch timer mode control register (WTM)
  WTM selects a count clock for the watch timer and specifies whether to enable clocking of the timer. It also specifies the prescaler interval and how the 5-bit counter is controlled.
  This register is set with a 1-bit or 8-bit memory manipulation instruction.
  $\overline{\text{RESET}}$ input clears WTM to 00H.

Figure 7-2. Format of Watch Timer Mode Control Register

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After reset	R/W
WTM	WTM7	WTM6	WTM5	WTM4	0	0	WTM1	WTM0	FF4AH	00H	R/W

WTM7	Watch timer count clock (f_W) selection
0	$f_X/2^7$ (39.1 kHz)
1	f_{XT} (32.768 kHz)

WTM6	WTM5	WTM4	Prescaler interval selection
0	0	0	$2^4/f_W$
0	0	1	$2^5/f_W$
0	1	0	$2^6/f_W$
0	1	1	$2^7/f_W$
1	0	0	$2^8/f_W$
1	0	1	$2^9/f_W$
Other than above			Setting prohibited

WTM1	Control of 5-bit counter operation
0	Cleared after stop
1	Started

WTM0	Watch timer operation
0	Operation stopped (both prescaler and timer cleared)
1	Operation enabled

Caution Bits 2 and 3 must be set to 0.

Remarks 1. f_W: Watch timer clock frequency ($f_X/2^7$ or f_{XT})
2. f_X: Main system clock oscillation frequency
3. f_{XT}: Subsystem clock oscillation frequency
4. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

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7.4 Watch Timer Operation

7.4.1 Operation as watch timer

The main system clock (4.19 MHz) or subsystem clock (32.768 kHz) is used as a watch timer which generates 0.5-second intervals.

The watch timer is used to generate an interrupt request at specified intervals.

By setting bits 0 and 1 (WTM0 and WTM1) of the watch timer mode control register (WTM) to 1, the watch timer starts counting. By setting them to 0, the 5-bit counter is cleared and the watch timer stops counting.

When the interval timer also operates at the same time, only the watch timer can be started from 0 seconds by setting WTM1 to 0. However, an error of up to $2^9 \times 1/f_W$ seconds may occur for the first overflow of the watch timer (INTWT) after a 0-second start because the 9-bit prescaler is not cleared in this case.

7.4.2 Operation as interval timer

The interval timer is used to repeatedly generate an interrupt request at the interval specified by a preset count value.

The interval time can be selected by bits 4 to 6 (WTM4 to WTM6) of the watch timer mode control register (WTM).

Table 7-3. Interval Time of Interval Timer

Interval	At f_X = 5.0 MHz Operation	At f_X = 4.19 MHz Operation	At f_{XT} = 32.768 kHz Operation
$2^4 \times 1/f_W$	409.6 μs	488 μs	488 μs
$2^5 \times 1/f_W$	819.2 μs	977 μs	977 μs
$2^6 \times 1/f_W$	1.64 ms	1.95 ms	1.95 ms
$2^7 \times 1/f_W$	3.28 ms	3.91 ms	3.91 ms
$2^8 \times 1/f_W$	6.55 ms	7.81 ms	7.81 ms
$2^9 \times 1/f_W$	13.1 ms	15.6 ms	15.6 ms

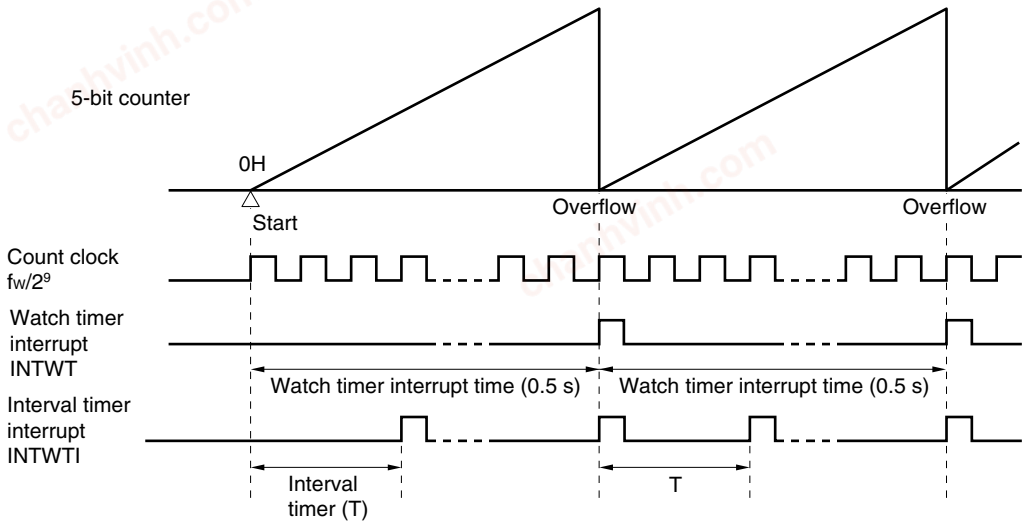
Remarks 1. f_W: Watch timer clock frequency ($f_X/2^7$ or f_{XT})

2. f_X: Main system clock oscillation frequency

3. f_{XT}: Subsystem clock oscillation frequency

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Figure 7-3. Watch Timer/Interval Timer Operation Timing



Caution When operation of the watch timer and 5-bit counter has been enabled by setting the watch timer mode control register (WTM) (setting WTM0 (bit 0 of WTM) to 1), the time until the first interrupt request after this setting will not be exactly the same as the watch timer interrupt time (0.5 s). This is because the 5-bit counter starts counting one cycle after the output of the 9-bit prescaler. The INTWT signal will be generated at the set time from its second generation.

Remarks 1. fw: Watch timer clock frequency

2. The parenthesized values apply to operation at fw = 32.768 kHz.

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CHAPTER 8 WATCHDOG TIMER

8.1 Watchdog Timer Functions

The watchdog timer has the following functions.

- Watchdog timer
- Interval timer

Caution Select the watchdog timer mode or interval timer mode by using the watchdog timer mode register (WDTM).

(1) Watchdog timer

The watchdog timer is used to detect inadvertent program loop. When the inadvertent program loop is detected, a non-maskable interrupt or the $\overline{\text{RESET}}$ signal can be generated.

Table 8-1. Inadvertent Program Loop Detection Time of Watchdog Timer

Inadvertent Program Loop Detection Time	At fx = 5.0 MHz Operation
$2^{11} \times 1/f_x$	410 μs
$2^{13} \times 1/f_x$	1.64 ms
$2^{15} \times 1/f_x$	6.55 ms
$2^{17} \times 1/f_x$	26.2 ms

Remark fx: Main system clock oscillation frequency

(2) Interval timer

The interval timer generates an interrupt at any preset intervals.

Table 8-2. Interval Time of Watchdog Timer

Interval Time	At fx = 5.0 MHz Operation
$2^{11} \times 1/f_x$	410 μs
$2^{13} \times 1/f_x$	1.64 ms
$2^{15} \times 1/f_x$	6.55 ms
$2^{17} \times 1/f_x$	26.2 ms

Remark fx: Main system clock oscillation frequency

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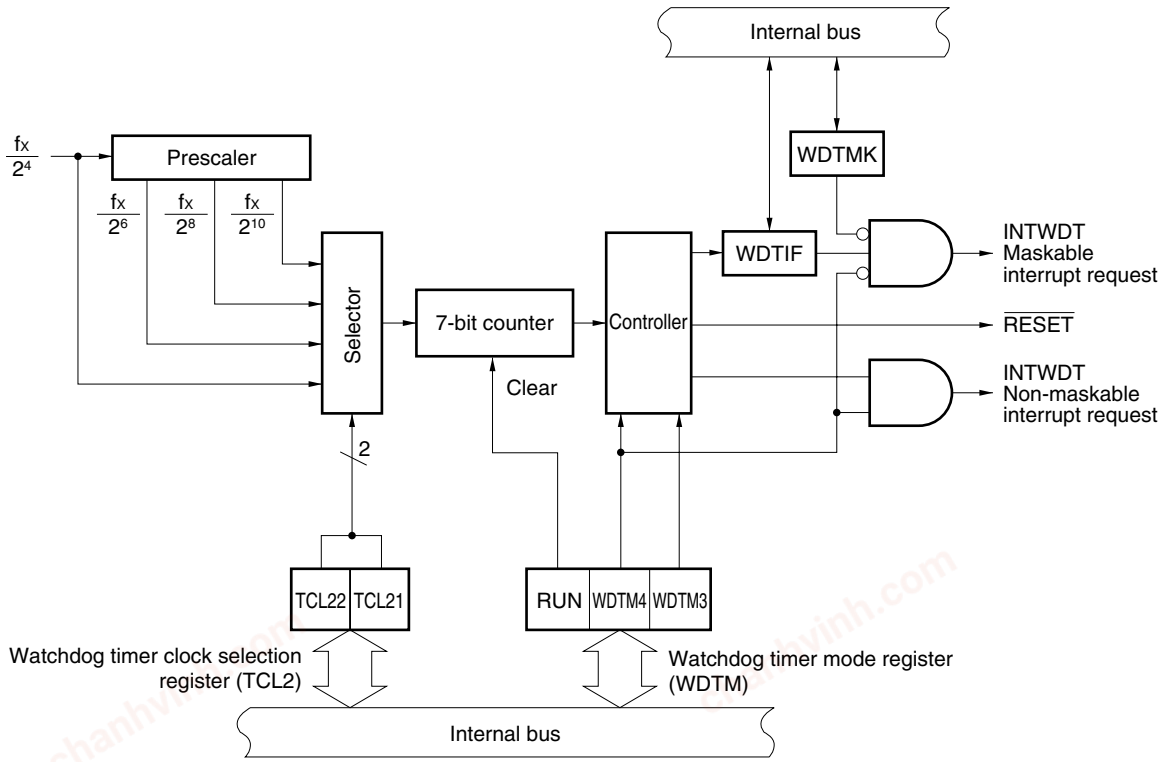
8.2 Watchdog Timer Configuration

The watchdog timer includes the following hardware.

Table 8-3. Configuration of Watchdog Timer

Item	Configuration
Control registers	Watchdog timer clock selection register (TCL2) Watchdog timer mode register (WDTM)

Figure 8-1. Block Diagram of Watchdog Timer



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8.3 Registers Controlling Watchdog Timer

The watchdog timer is controlled by the following two registers.

- Watchdog timer clock selection register (TCL2)
- Watchdog timer mode register (WDTM)

(1) Watchdog timer clock selection register (TCL2)

TCL2 sets the watchdog timer count clock.

This register is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TCL2 to 00H.

Figure 8-2. Format of Watchdog Timer Clock Selection Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
TCL2	0	0	0	0	0	TCL22	TCL21	0	FF42H	00H	R/W

TCL22	TCL21	Watchdog timer count clock selection	Inadvertent program loop detection or interval time
0	0	$f_X/2^4$ (313 kHz)	$2^{11}/f_X$ (410 μs)
0	1	$f_X/2^6$ (78.1 kHz)	$2^{13}/f_X$ (1.64 ms)
1	0	$f_X/2^8$ (19.5 kHz)	$2^{15}/f_X$ (6.55 ms)
1	1	$f_X/2^{10}$ (4.88 kHz)	$2^{17}/f_X$ (26.2 ms)

Caution Bits 0, 3 to 7 must be set to 0.

Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

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(2) Watchdog timer mode register (WDTM)

WDTM sets an operation mode of the watchdog timer, and enables/disables counting of the watchdog timer. This register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears WDTM to 00H.

Figure 8-3. Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

RUN	Selection of operation of watchdog timer[Note 1]
0	Stops counting
1	Clears counter and starts counting

WDTM4	WDTM3	Selection of operation mode of watchdog timer[Note 2]
0	0	Operation stopped
0	1	Interval timer mode (when overflow occurs, a maskable interrupt occur)[Note 3]
1	0	Watchdog timer mode 1 (when overflow occurs, a non-maskable interrupt occurs)
1	1	Watchdog timer mode 2 (when overflow occurs, reset operation starts)

Notes 1. Once RUN has been set (1), it cannot be cleared (0) by software. Therefore, when counting is started, it cannot be stopped by any means other than $\overline{\text{RESET}}$ input.

2. Once WDTM3 and WDTM4 have been set (1), they cannot be cleared (0) by software.

3. The watchdog timer starts operations as an interval timer when RUN is set to 1.

Cautions 1. When the watchdog timer is cleared by setting RUN to 1, the actual overflow time is up to 0.8% shorter than the time set by the watchdog timer clock selection register (TCL2).

2. In watchdog timer mode 1 or 2, set WDTM4 to 1 after confirming that the WDTIF (bit 0 of interrupt request flag register 0 (IF0)) is set to 0. While WDTIF is 1, a non-maskable interrupt is generated upon write completion if watchdog timer mode 1 or 2 is selected.

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8.4 Watchdog Timer Operation

8.4.1 Operation as watchdog timer

The watchdog timer detects an inadvertent program loop when bit 4 (WDTM4) of the watchdog timer mode register (WDTM) is set to 1.

The count clock (inadvertent program loop detection time interval) of the watchdog timer can be selected by bits 1 and 2 (TCL21 and TCL22) of the watchdog timer clock selection register (TCL2). By setting bit 7 (RUN) of WDTM to 1, the watchdog timer is started. Set RUN to 1 within the set inadvertent program loop detection time interval after the watchdog timer has been started. By setting RUN to 1, the watchdog timer can be cleared and start counting. If RUN is not set to 1, and the inadvertent program loop detection time is exceeded, the system is reset or a non-maskable interrupt is generated by the value of bit 3 (WDTM3) of WDTM.

The watchdog timer continues operation in the HALT mode, but stops in the STOP mode. Therefore, set RUN to 1 before entering the STOP mode to clear the watchdog timer, and then execute the STOP instruction.

Cautions 1. The actual inadvertent program loop detection time may be up to 0.8% shorter than the set time.

2. When the subsystem clock is selected as the CPU clock, the watchdog timer stops counting. In this case, therefore, the watchdog timer stops operation even though the main system clock is oscillating.

Table 8-4. Inadvertent Program Loop Detection Time of Watchdog Timer

TCL22	TCL21	Inadvertent Program Loop Detection Time	At fx = 5.0 MHz Operation
0	0	$2^{11} \times 1/fx$	410 μs
0	1	$2^{13} \times 1/fx$	1.64 ms
1	0	$2^{15} \times 1/fx$	6.55 ms
1	1	$2^{17} \times 1/fx$	26.2 ms

Remark fx: Main system clock oscillation frequency

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8.4.2 Operation as interval timer

When bit 4 (WDTM4) and bit 3 (WDTM3) of the watchdog timer mode register (WDTM) are set to 0 and 1, respectively, the watchdog timer also operates as an interval timer that repeatedly generates an interrupt at time intervals specified by a preset count value.

Select a count clock (or interval time) by setting bits 1 and 2 (TCL21 and TCL22) of the watchdog timer clock selection register (TCL2). The watchdog timer starts operation as an interval timer when the RUN bit (bit 7 of WDTM) is set to 1.

In the interval timer mode, the interrupt mask flag (WDTMK) is valid, and a maskable interrupt (INTWDT) can be generated. The priority of INTWDT is set as the highest of all the maskable interrupts.

The interval timer continues operation in the HALT mode, but stops in the STOP mode. Therefore, set RUN to 1 before entering the STOP mode to clear the interval timer, and then execute the STOP instruction.

Cautions 1. Once bit 4 (WDTM4) of WDTM is set to 1 (when the watchdog timer mode is selected), the interval timer mode is not set, unless the $\overline{\text{RESET}}$ signal is input.

2. The interval time immediately after the setting by WDTM may be up to 0.8% shorter than the set time.

Table 8-5. Interval Time of Watchdog Timer

TCL22	TCL21	Interval Time	At fx = 5.0 MHz Operation
0	0	$2^{11} \times 1/fx$	410 μs
0	1	$2^{13} \times 1/fx$	1.64 ms
1	0	$2^{15} \times 1/fx$	6.55 ms
1	1	$2^{17} \times 1/fx$	26.2 ms

Remark fx: Main system clock oscillation frequency

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CHAPTER 9 SERIAL INTERFACE 10 (μPD78F9328 ONLY)

Caution Serial interface 10 is not available for mask ROM versions. Do not access the registers used for Serial interface 10 when using a mask ROM version.

9.1 Serial Interface 10 Functions

Serial interface 10 has the following two modes.

- Operation stop mode
- 3-wire serial I/O mode

(1) Operation stop mode

This mode is used when serial transfer is not carried out. It enables a reduction in power consumption.

(2) 3-wire serial I/O mode (MSB/LSB-first switchable)

In this mode, 8-bit data transfer is carried out-first with three lines, one for the serial clock ($\overline{\text{SCK10}}$) and two for serial data (SI10 and SO10).

The 3-wire serial I/O mode supports simultaneous transmit and receive operations, reducing data transfer processing time.

It is possible to switch the start bit of 8-bit data to be transmitted between the MSB and the LSB, thus allowing connection to devices with either start bit.

The 3-wire serial I/O mode is effective for connecting display controllers and peripheral I/O such as the 75XL Series, 78K Series, and 17K Series, which have internal conventional clocked serial interfaces.

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9.2 Serial Interface 10 Configuration

Serial interface 10 includes the following hardware.

Table 9-1. Configuration of Serial Interface 10

Item	Configuration
Register	Transmit/receive shift register 10 (SIO10)
Control register	Serial operation mode register 10 (CSIM10) Port mode register 2 (PM2) Port 2 (P2)

(1) Transmit/receive shift register 10 (SIO10)

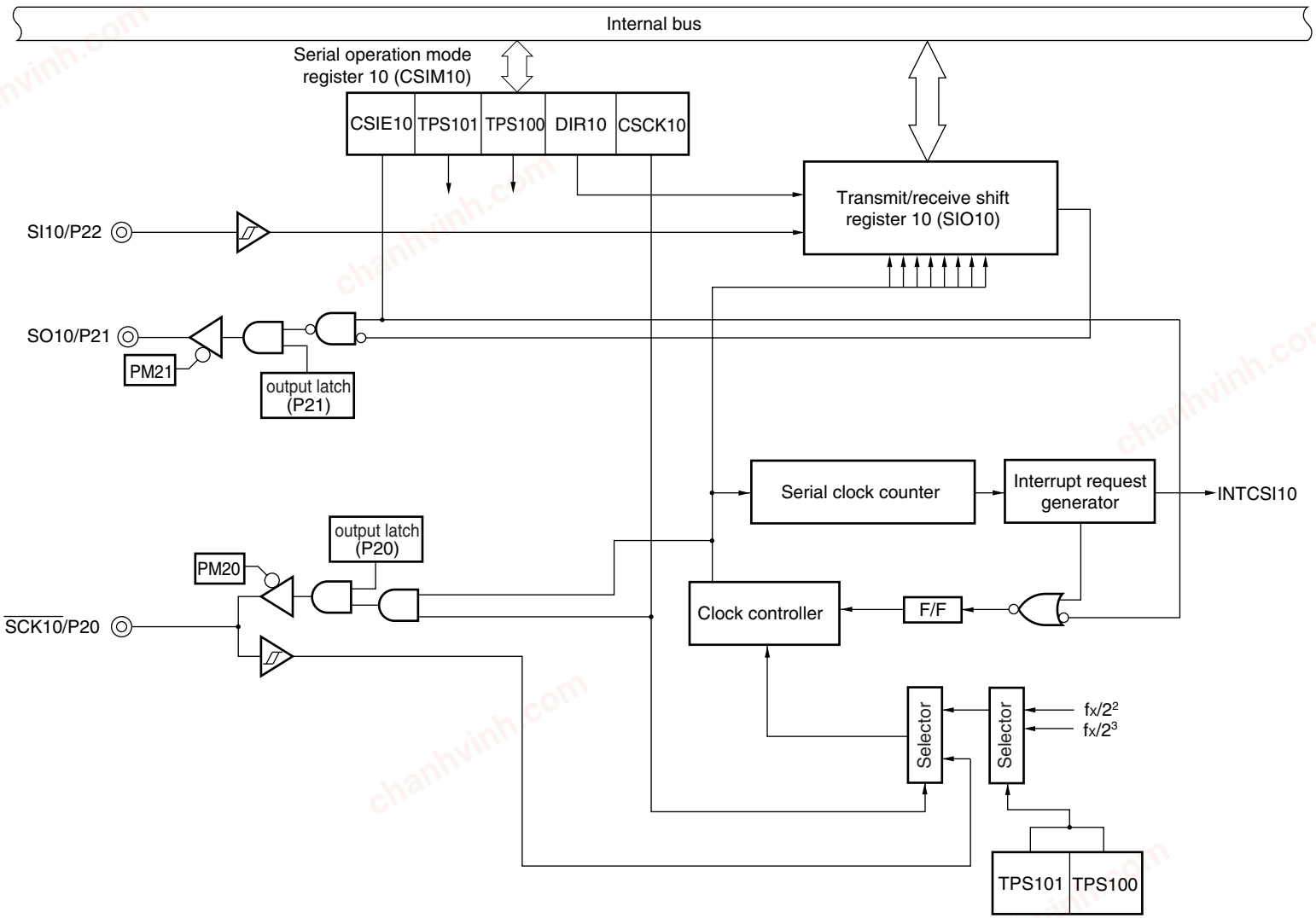
SIO10 is an 8-bit register used for parallel-to-serial conversion and to perform serial data transmission/reception in synchronization with serial clocks.

This register is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes SIO10 undefined.

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Figure 9-1. Block Diagram of Serial Interface 10



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9.3 Registers Controlling Serial Interface 10

Serial interface 10 is controlled by the following three registers.

- Serial operation mode register 10 (CSIM10)
- Port mode register 2 (PM2)
- Port 2 (P2)

(1) Serial operation mode register 10 (CSIM10)

CSIM10 is used to control serial interface 10 and set the serial clock and start bit.

This register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM10 to 00H.

Figure 9-2. Format of Serial Operation Mode Register 10

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM10	CSIE10	0	TPS101	TPS100	0	DIR10	CSCK10	0	FF72H	00H	R/W

CSIE10	Operation control in 3-wire serial I/O mode
0	Operation stopped
1	Operation enabled

TPS101	TPS100	Count clock selection when internal clock is selected
0	0	$f_X/2^2$ (1.25 MHz)
0	1	$f_X/2^3$ (625 kHz)
Other than above		Setting prohibited

DIR10	Start bit specification
0	MSB
1	LSB

CSCK10	SIO10 clock selection
0	Input clock to $\overline{\text{SCK10}}$ pin from external
1	Internal clock selected by TPS100, TPS101

Cautions 1. Bits 0, 3, and 6 must be set to 0.

2. Switch operation mode after stopping the serial transmit/receive operation.

Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

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(2) Port mode register 2 (PM2)

This register is used to set the I/O mode of port 2 in 1-bit units.

PM2 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PM2 to FFH.

Figure 9-3. Format of Port Mode Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	1	1	1	1	1	PM22	PM21	PM20	FF22H	FFH	R/W

PM2n	I/O mode of P2n pin (n = 0 to 2)
0	Output mode (output buffer is on)
1	Input mode (output buffer is off)

Caution Bits 3 to 7 must be set to 1.

Table 9-2. Settings of Serial Interface 10 Operating Mode

(1) Operation stop mode

CSIM10			PM22	P22	PM21	P21	PM20	P20	Start Bit	Shift Clock	P22/SI10 Pin Function	P21/SO10 Pin Function	P20/$\overline{\text{SCK10}}$ Pin Function
CSIE10	DIR10	CSCK10											
0	×	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	—	—	P22	P21	P20
Other than above									Setting prohibited				

(2) 3-wire serial I/O mode

CSIM10			PM22	P22	PM21	P21	PM20	P20	Start Bit	Shift Clock	P22/SI10 Pin Function	P21/SO10 Pin Function	P20/$\overline{\text{SCK10}}$ Pin Function
CSIE10	DIR10	CSCK10											
1	0	0	1Note 2	×Note 2	0	1	1	×	MSB	External clock	SI10Note 2	SO10 (CMOS output)	$\overline{\text{SCK10}}$ input
		1					0	1		Internal clock			$\overline{\text{SCK10}}$ output
1	1	0					1	×	LSB	External clock			$\overline{\text{SCK10}}$ input
		1					0	1		Internal clock			$\overline{\text{SCK10}}$ output
Other than above									Setting prohibited				

Notes 1. Can be used as port function.

2. If used only for transmission, can be used as P22 (CMOS I/O).

Remark ×: don't care

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9.4 Serial Interface 10 Operation

Serial interface 10 provides the following two types of modes.

- Operation stop mode
- 3-wire serial I/O mode

9.4.1 Operation stop mode

In the operation stop mode, serial transfer is not executed, therefore enabling a reduction in the power consumption.

The P20/$\overline{SCK10}$, P21/SO10, and P22/SI10 pins can be used as normal I/O ports.

(1) Register setting

Operation stop mode is set by serial operation mode register 10 (CSIM10).

(a) Serial operation mode register 10 (CSIM10)

CSIM10 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears CSIM10 to 00H.

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM10	CSIE10	0	TPS101	TPS100	0	DIR10	CSCK10	0	FF72H	00H	R/W

CSIE10	Operation control in 3-wire serial I/O mode
0	Operation stopped
1	Operation enabled

Caution Bits 0, 3, and 6 must be set to 0.

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9.4.2 3-wire serial I/O mode

The 3-wire serial I/O mode is useful for connection of peripheral I/O and display controllers, etc., which incorporate a conventional clocked serial interface, such as the 75XL Series, 78K Series, 17K Series.

Communication is performed using three lines: a serial clock line ($\overline{SCK10}$), serial output line (SO10), and serial input line (SI10).

(1) Register setting

3-wire serial I/O mode settings are performed using serial operation mode register 10 (CSIM10).

(a) Serial operation mode register 10 (CSIM10)

CSIM10 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears CSIM10 to 00H.

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM10	CSIE10	0	TPS101	TPS100	0	DIR10	CSCK10	0	FF72H	00H	R/W

CSIE10	Operation control in 3-wire serial I/O mode
0	Operation stopped
1	Operation enabled

TPS101	TPS100	Count clock selection when internal clock is selected
0	0	$f_X/2^2$ (1.25 MHz)
0	1	$f_X/2^3$ (625 kHz)
Other than above		Setting prohibited

DIR10	Start bit specification
0	MSB
1	LSB

CSCK10	SIO10 clock selection
0	Input clock to $\overline{SCK10}$ pin from external
1	Internal clock selected by TPS100, TPS101

Cautions 1. Bits 0, 3, and 6 must be set to 0.

2. Switch operation mode after stopping the serial transmit/receive operation.

Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

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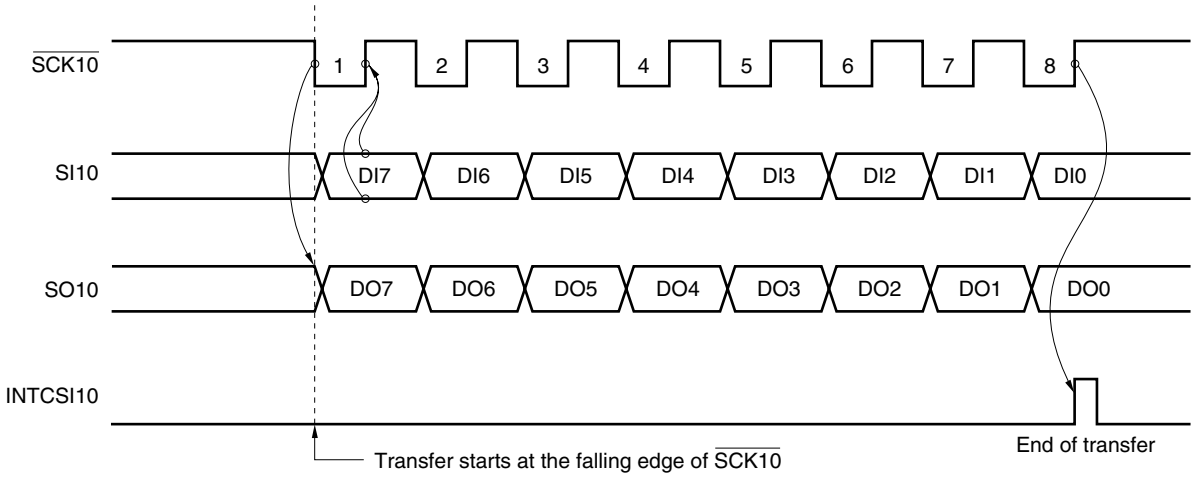
(2) Communication operation

In the 3-wire serial I/O mode, data transmission/reception is performed in 8-bit units. Data is transmitted/received bit by bit in synchronization with the serial clock.

Transmit shift register 10 (SIO10) shift operations are performed in synchronization with the fall of the serial clock ($\overline{SCK10}$). Transmit data is then held in the SO10 latch and output from the SO10 pin. Also, receive data input to the SI10 pin is latched in the input bits of SIO10 on the rise of $\overline{SCK10}$.

At the end of an 8-bit transfer, the operation of SIO10 stops automatically, and the interrupt request signal (INTCSI10) is generated.

Figure 9-4. 3-Wire Serial I/O Mode Timing



Cautions

1. **When data is written to SIO10 in the serial operation disabled status (CSIE10 = 0), the data cannot be transmitted or received.**
2. **When data is written to SIO10 in the serial operation disabled status (CSIE10 = 0) and then serial operation is enabled (CSIE10 = 1), the data cannot be transmitted or received.**
3. **Once data has been written to SIO10 with the external serial clock selected (CSCK10 = 0), overwriting the data does not update the contents of SIO10.**
4. **When CSIM10 is operated during data transmission/reception, data cannot be transmitted or received normally.**
5. **When SIO10 is operated during data transmission/reception, the data cannot be transmitted or received normally.**

(3) Transfer start

Serial transfer is started by setting transfer data to the transmit shift register 10 (SIO10) when the following two conditions are satisfied.

- Bit 7 (CSIE10) of serial operation mode register 10 (CSIM10) = 1
- Internal serial clock is stopped or $\overline{SCK10}$ is a high level after 8-bit serial transfer.

Termination of 8-bit transfer stops the serial transfer automatically and generates the interrupt request signal (INTCSI10).

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CHAPTER 10 LCD CONTROLLER/DRIVER

10.1 LCD Controller/Driver Functions

The functions of the LCD controller/driver of the μPD179327 Subseries are as follows.

(1) Automatic output of segment and common signals based on automatic display data memory read
(2) Two different display modes:
- Static
- 1/4 duty (1/3 bias)

(3) Four different frame frequencies, selectable in each display mode
(4) Up to 24 segment signal outputs (S0 to S23) and four common signal outputs (COM0 to COM3)
(5) Operation with a subsystem clock

Table 10-1 lists the maximum number of pixels that can be displayed in each display mode.

Table 10-1. Maximum Number of Pixels

Bias Mode	Number of Time Slices	Common Signals Used	Maximum Number of Pixels
–	Static	COM0 (COM1 to COM3)	24 (24 segments × 1 common)[Note 1]
1/3	4	COM0 to COM3	96 (24 segments × 4 commons)[Note 2]

Notes 1. 3-digit LCD panel, each digit having an 8-segment 8. configuration.
2. 12-digit LCD panel, each digit having a 2-segment 8. configuration.

10.2 LCD Controller/Driver Configuration

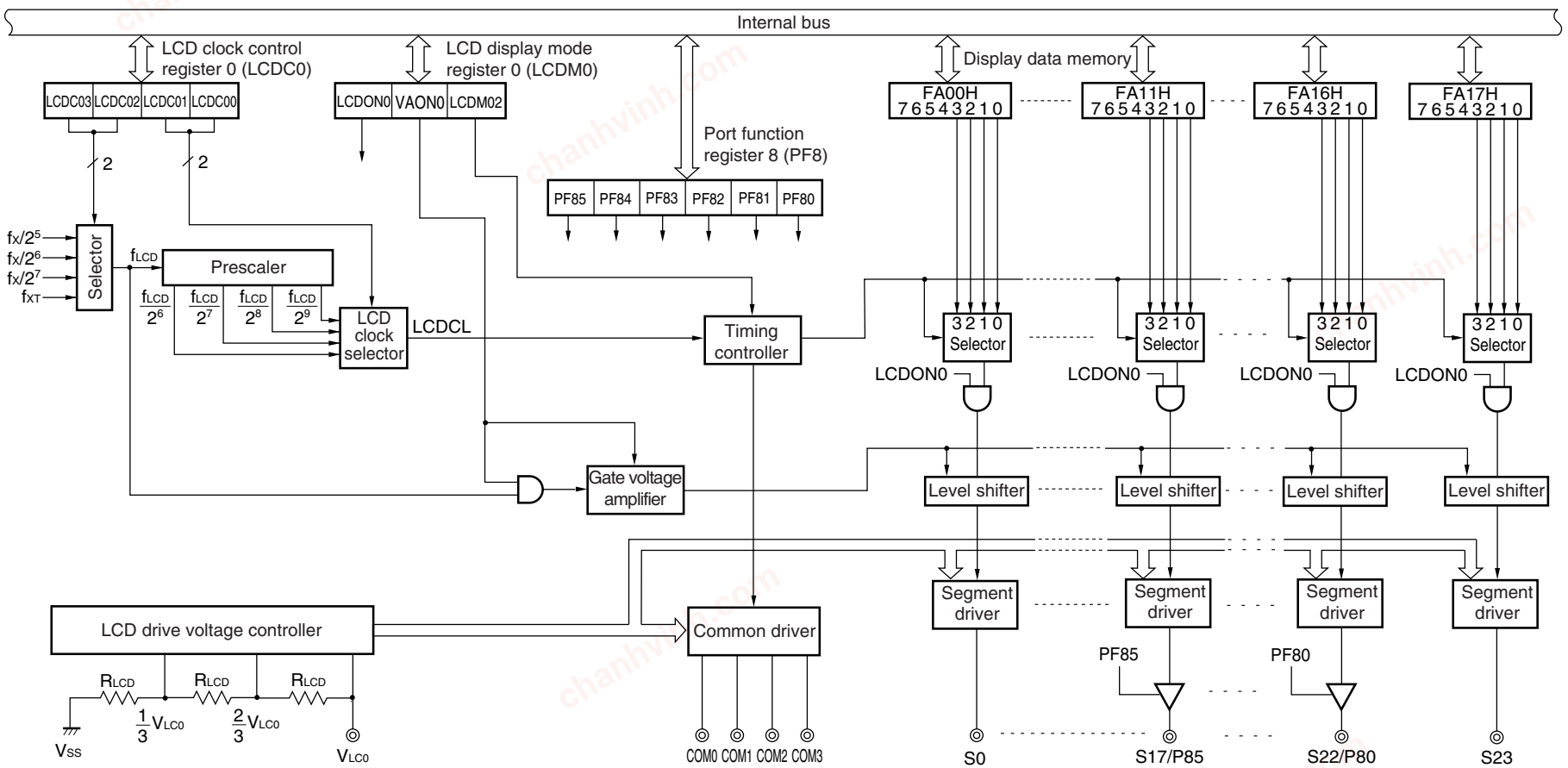
The LCD controller/driver consists of the following hardware.

Table 10-2. Configuration of LCD Controller/Driver

Item	Configuration
Display outputs	Segment signals: 24 Common signals: 4
Control registers	LCD display mode register 0 (LCDM0) LCD clock control register 0 (LCDC0) Port function register 8 (PF8)

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Figure 10-1. Block Diagram of LCD Controller/Driver



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10.3 Registers Controlling LCD Controller/Driver

- LCD display mode register 0 (LCDM0)
- LCD clock control register 0 (LCDC0)
- Port function register 8 (PF8)

(1) LCD display mode register 0 (LCDM0)

LCDM0 specifies whether to enable display operation. It also specifies the operation mode and display mode.

This register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears LCDM0 to 00H.

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Figure 10-2. Format of LCD Display Mode Register 0

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
LCDM0	LCDON0	VAON0	0	0	0	LCDM02	0	0	FFB0H	00H	R/W

LCDON0	LCD display enable/disable
0	Display off (all segment outputs are unselected for signal output)
1	Display on

VAON0	LCD controller/driver operation mode[Note 1]
0	No gate voltage amplification (for V_{LC0} = 2.7 to 5.5 V display)
1	Gate voltage amplification enabled (for V_{LC0} = 1.8 to 5.5 V display)

LCDM02	Display mode selection[Note 2]
0	Four-time slot, 1/3 bias mode
1	Static mode

Notes 1. When LCD display is not performed, the power consumption can be lowered by clearing VAON0 to 0.

2. To set the STOP mode while the main system clock is selected as the LCD source clock, select the static mode (LCDM02 = 1).

Cautions 1. Bits 0,1, 3 to 5 must be set to 0.

2. When operating VAON0, follow the procedure described below.

A. To stop gate voltage amplification after switching display status from on to off:

1) Set to display off status by setting LCDON0 = 0.

2) Stop gate voltage amplification by setting VAON0= 0.

B. To stop gate voltage amplification during display on status:

Setting prohibited. Be sure to stop gate voltage amplification after setting display off.

C. To set display on from gate voltage amplification stop status:

1) Start gate voltage amplification by setting VAON0 = 1, then wait for about 500 ms.

2) Set display on by setting LCDON0 = 1.

D. To start voltage amplification during display on status:

Setting prohibited. Be sure to setting display off, and follow the procedure in C.

3. When the main system clock is selected as the LCD source clock, If the STOP mode is selected, an abnormal display may occur. Before selecting the STOP mode, disable display and select the static mode (LCDON0 = 0 and LCDM02 = 1). If the subsystem clock is selected as the LCD source clock, a normal operation is performed in the STOP mode.

4. The LCD may momentarily light for 1 cycle immediately after the display has been turned on/off because the waveform has not become stabilized.

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(2) LCD clock control register 0 (LCDC0)

LCDC0 specifies the LCD source clock and LCD clock. The frame frequency is determined by the LCD clock and the number of time divisions.

This register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears LCDC0 to 00H.

Figure 10-3. Format of LCD Clock Control Register 0

Symbol	7	6	5	4	3	2	1	<0>	Address	After reset	R/W
LCDC0	0	0	0	0	LCDC03	LCDC02	LCDC01	LCDC00	FFB2H	00H	R/W

LCDC03	LCDC02	LCD source clock (f_{LCD}) selection[Note]
0	0	f_{XT} (32.768 kHz)
0	1	$f_X/2^5$ (156.3 kHz)
1	0	$f_X/2^6$ (78.1 kHz)
1	1	$f_X/2^7$ (39.1 kHz)

LCDC01	LCDC00	LCD clock (LCDCL) selection
0	0	$f_{LCD}/2^6$
0	1	$f_{LCD}/2^7$
1	0	$f_{LCD}/2^8$
1	1	$f_{LCD}/2^9$

Note Specify an LCD source clock (f_{LCD}) frequency of at least 32 kHz.

Remarks 1. f_X: Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

Cautions 1. Bits 4 to 7 must be set to 0.

2. Be sure to turn off the display (LCDON = 0) and stop the voltage amplifier (VAON0 = 0) before changing the LCDC0 settings.

For example, Table 10-3 lists the frame frequencies used when f_{XT} (32.768 kHz) is supplied to the LCD source clock (f_{LCD}).

Table 10-3. Frame Frequencies (Hz)

LCD Clock (LCDCL) / Time Division	$f_{XT}/2^9$ (64 Hz)	$f_{XT}/2^8$ (128 Hz)	$f_{XT}/2^7$ (256 Hz)	$f_{XT}/2^6$ (512 Hz)
Static	64	128	256	512
4	16	32	64	128

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(3) Port function register 8 (PF8)

PF8 specifies whether S17/P85 to S22/P80 are used as LCD segment signal outputs or general-purpose ports in 1-bit units.

This register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears PF8 to 00H.

Figure 10-4. Format of Port Function Register 8

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PF8	0	0	PF85	PF84	PF83	PF82	PF81	PF80	FF58H	00H	R/W

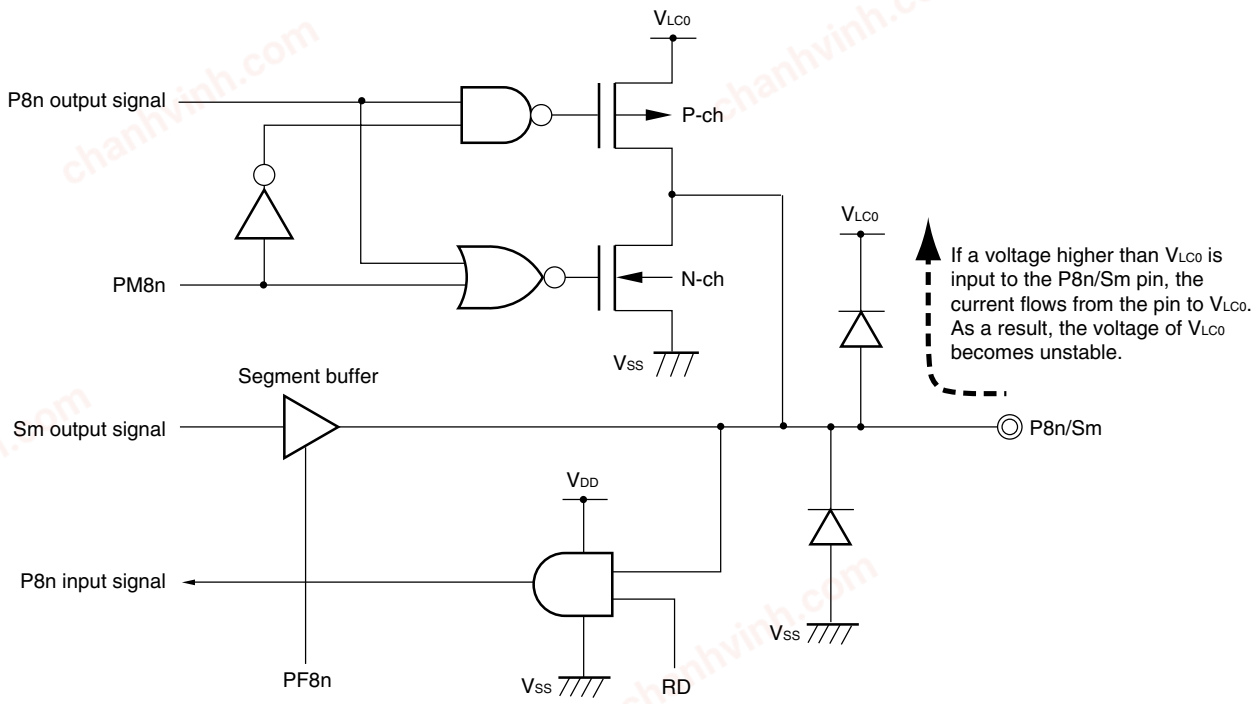
PF8n	Port function of P8n (n = 0 to 5)
0	Operates as a general-purpose port
1	Operates as an LCD segment signal output

Cautions 1. Bits 6 and 7 must be set to 0.

2. When port 8 is used as a general-purpose port, observe the following restriction (because an ESD protection circuit for LCD pins (on the high-level side of port 8) is connected to V_{LC0}).

- **When any one of pins P80/S22 to P85/S17 is used as a general-purpose input port pin, use the microcontroller at $V_{DD} = V_{LC0}$ or $V_{DD} < V_{LC0}$.**

There is no restriction when all of pins P80/S22 to P85/S17 are used as LCD segment pins or general-purpose output port pins.



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Remark Sm: LCD segment output (m = 22 to 17)
P8n: Bit n of Port 8 (n = 0 to 5)
PF8n: Bit n of Port function register 8 (n = 0 to 5)
RD: Port 8 read signal

10.4 Setting LCD Controller/Driver

Set the LCD controller/driver using the following procedure.

<To enable gate voltage amplification>

<1> Set the frame frequency using LCD clock control register 0 (LCDC0).
<2> Set VAON0 (bit 6 of LCDM0) (VAON0 = 1).
Wait for 500 ms or more after setting VAON0.
<3> Start output corresponding to each display data memory by setting LCDON0 (bit 7 of LCDM0) (LCDON0 =1).

<When gate voltage is not amplified>

<1> Set the frame frequency using LCD clock control register 0 (LCDC0).
<2> Start output corresponding to each display data memory by setting LCDON0 (bit 7 of LCDM0) (LCDON0 =1).

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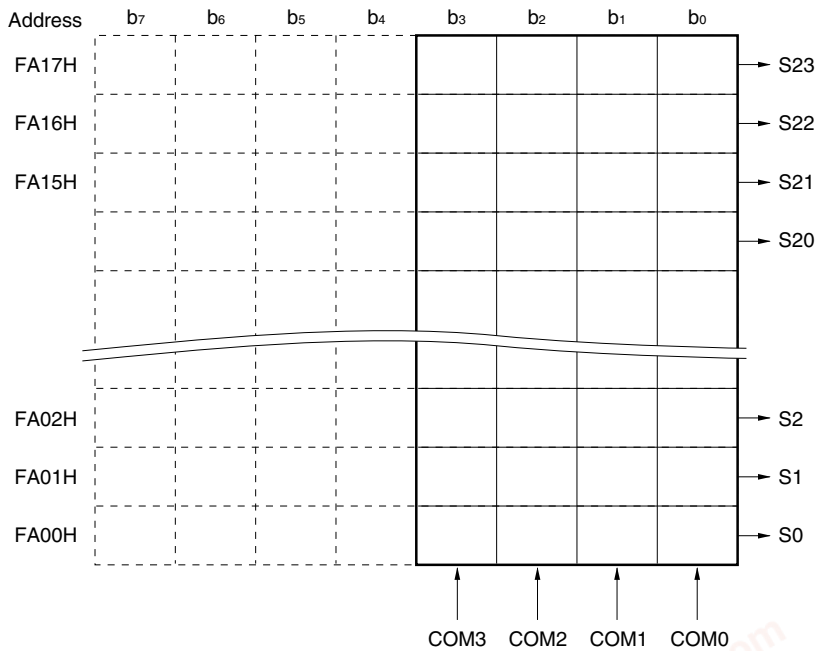
10.5 LCD Display Data Memory

The LCD display data memory is mapped at addresses FA00H to FA17H. Data in the LCD display data memory can be displayed on the LCD panel using the LCD controller/driver.

Figure 10-5 shows the relationship between the contents of the LCD display data memory and the segment/common outputs.

That part of the display data memory which is not used for display can be used as ordinary RAM.

Figure 10-5. Relationship Between LCD Display Data Memory Contents and Segment/Common Outputs



Caution No memory has been installed as the higher 4 bits of the LCD display data memory. Be sure to set 0 to them.

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10.6 Common and Segment Signals

Each pixel of the LCD panel turns on when the potential difference between the corresponding common and segment signals becomes higher than a specific voltage (LCD drive voltage, V_{LCD}). It turns off when the potential difference becomes lower than V_{LCD}.

Applying DC voltage to the common and segment signals for an LCD panel would deteriorate it. To avoid this problem, this LCD panel is driven with AC voltage.

(1) Common signals

Each common signal is selected sequentially according to a specified number of time slots at the timing listed in Table 10-4.

Table 10-4. COM Signals

COM Signal / Number of Time Slots	COM0	COM1	COM2	COM3
Static display mode				
Four-time slot mode				

(2) Segment signals

The segment signals correspond to 24 bytes of LCD display data memory (FA00H to FA17H). Bits 0, 1, 2, and 3 of each byte are read in synchronization with COM0, COM1, COM2, and COM3, respectively. If the contents of each bit are 1, it is converted to the select voltage, and if 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (S0 to S23).

Check, with the information given above, what combination of the front-surface electrodes (corresponding to the segment signals) and the rear-surface electrodes (corresponding to the common signals) forms display patterns in the LCD display data memory, and write the bit data that corresponds to the desired display pattern on a one-to-one basis.

LCD display data memory bits 1 to 3 are not used for LCD display in the static display. So these bits can be used for purposes other than display.

LCD display data memory bits 4 to 7 are fixed to 0.

(3) Output waveforms of common and segment signals

The voltages listed in Table 10-5 are output as common and segment signals.

When both common and segment signals are at the select voltage, a display on-voltage of $\pm V_{LCD}$ is obtained. The other combinations of the signals correspond to the display off-voltage.

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Table 10-5. LCD Drive Voltage

(a) Static display mode

Segment Signal / Common Signal	Select Signal Level	Deselect Signal Level
	V_{SS0}/V_{LC0}	V_{LC0}/V_{SS0}
V_{LC0}/V_{SS0}	$-V_{LCD}/+V_{LCD}$	0 V/0 V

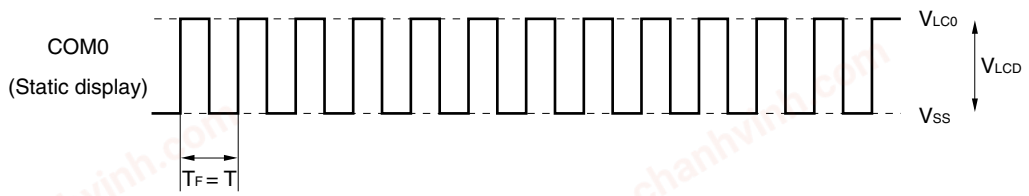
(b) 1/3 bias method

Segment Signal / Common Signal		Select Signal Level	Deselect Signal Level
		V_{SS0}/V_{LC0}	V_{LC1}/V_{LC2}
Select signal level	V_{LC0}/V_{SS0}	$-V_{LCD}/+V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$
Deselect signal level	V_{LC2}/V_{LC1}	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$

Figure 10-6 shows the common signal waveforms, and Figure 10-7 shows the voltages and phases of the common and segment signals.

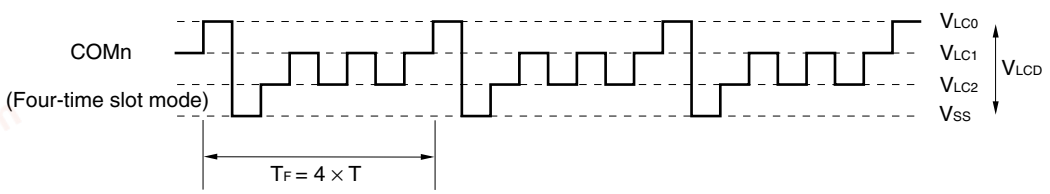
Figure 10-6. Common Signal Waveforms

(a) Static display mode



T: One LCD clock period TF: Frame frequency

(b) 1/3 bias method

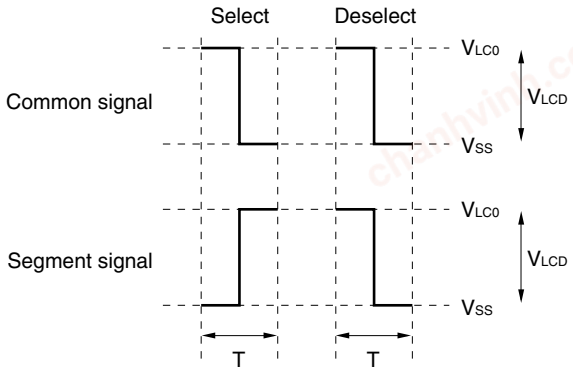


T: One LCD clock period TF: Frame frequency

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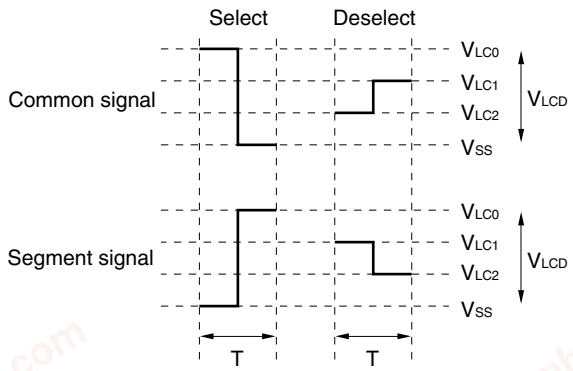
Figure 10-7. Voltages and Phases of Common and Segment Signals

(a) Static display mode



T: One LCD clock period

(b) 1/3 bias method



T: One LCD clock period

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10.7 Display Modes

10.7.1 Static display example

Figure 10-9 shows how the three-digit LCD panel having the display pattern shown in Figure 10-8 is connected to the segment signals (S0 to S23) and the common signal (COM0) of the μPD179327 Subseries chip. This example displays data "12.3" in the LCD panel. The contents of the display data memory (addresses FA00H to FA17H) correspond to this display.

The following description focuses on numeral "2." (2.) displayed in the second digit. To display "2." in the LCD panel, it is necessary to apply the select or deselect voltage to the S8 to S15 pins according to Table 10-6 at the timing of the common signal COM0; see Figure 10-8 for the relationship between the segment signals and LCD segments.

Table 10-6. Select and Deselect Voltages (COM0)

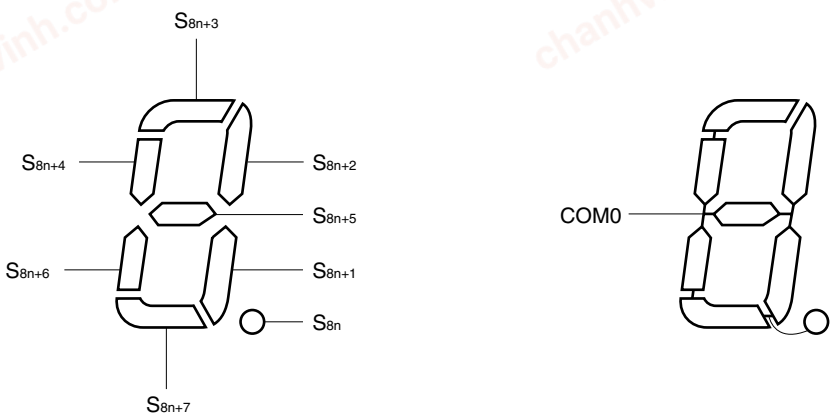
Segment / Common	S8	S9	S10	S11	S12	S13	S14	S15
COM0	Select	Deselect	Select	Select	Deselect	Select	Select	Select

According to Table 10-6, it is determined that the bit-0 pattern of the display data memory locations (FA08H to FA0FH) must be 10110111.

Figure 10-10 shows the LCD drive waveforms of S11 and S12, and COM0. When the select voltage is applied to S11 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

COM1 to COM3 are supplied with the same waveform as for COM0. So, COM0 to COM3 may be connected together to increase the driving capacity.

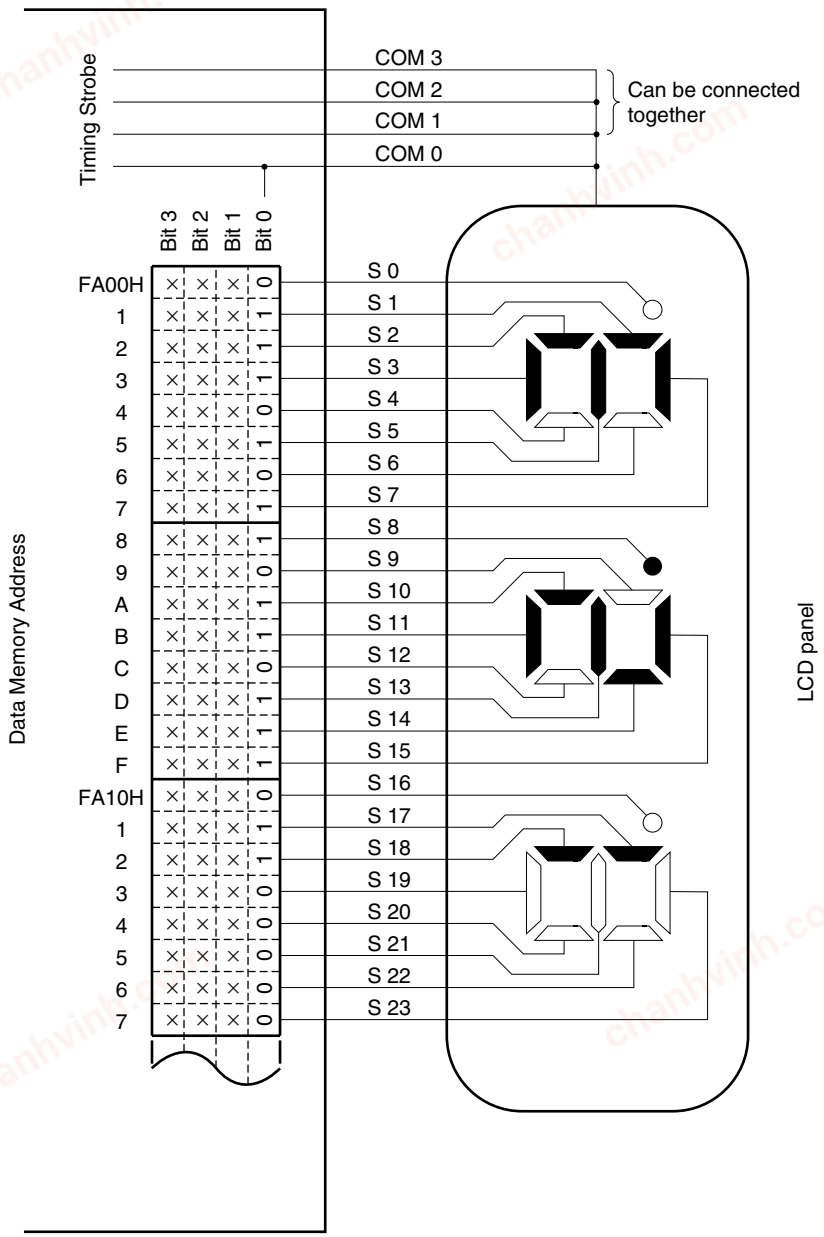
Figure 10-8. Static LCD Display Pattern and Electrode Connections



Remark n = 0 to 2

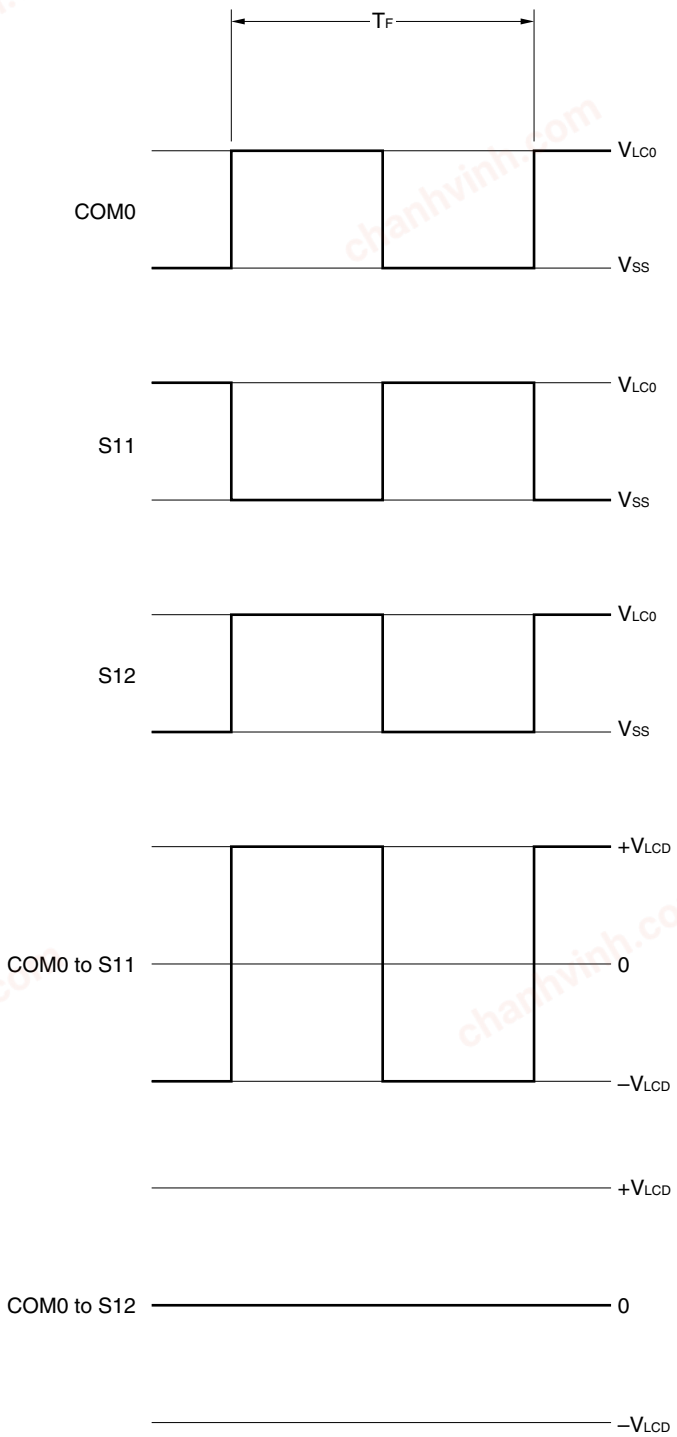
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Figure 10-9. Example of Connecting Static LCD Panel



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Figure 10-10. Static LCD Drive Waveform Examples



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10.7.2 Four-time slot display example

Figure 10-12 shows how the 12-digit LCD panel having the display pattern shown in Figure 10-11 is connected to the segment signals (S0 to S23) and the common signals (COM0 to COM3) of the μPD179327 Subseries chip. This example displays data “123456.789012” in the LCD panel. The contents of the display data memory (addresses FA00H to FA17H) correspond to this display.

The following description focuses on numeral “6.” (6.) displayed in the seventh digit. To display “6.” in the LCD panel, it is necessary to apply the select or deselect voltage to the S12 and S13 pins according to Table 10-7 at the timing of the common signals COM0 to COM3; see Figure 10-11 for the relationship between the segment signals and LCD segments.

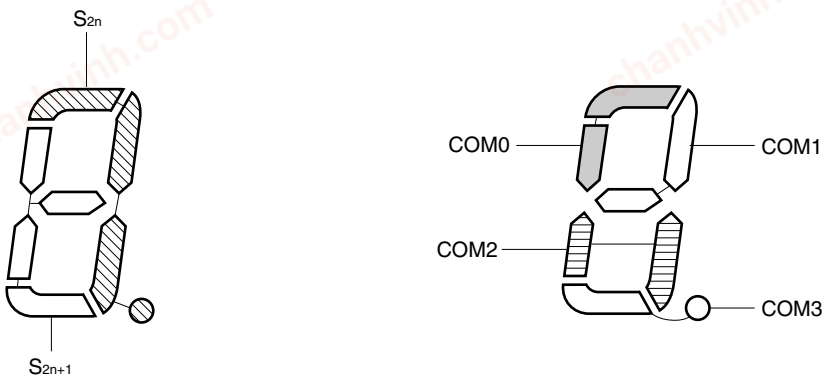
Table 10-7. Select and Deselect Voltages (COM0 to COM3)

Segment / Common	S12	S13
COM0	Select	Select
COM1	Deselect	Select
COM2	Select	Select
COM3	Select	Select

According to Table 10-7, it is determined that the display data memory location (FA0CH) that corresponds to S12 must contain 1101.

Figure 10-13 shows examples of LCD drive waveforms between the S12 signal and each common signal. When the select voltage is applied to S12 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

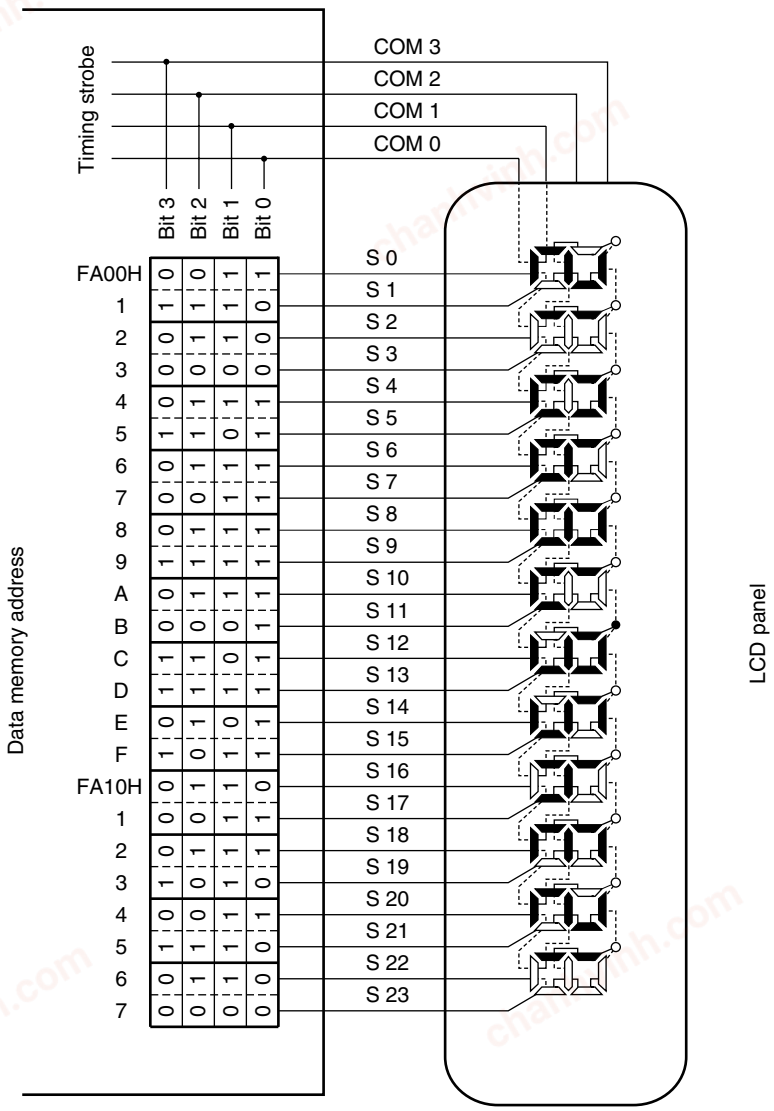
Figure 10-11. Four-Time Slot LCD Display Pattern and Electrode Connections



Remark n = 0 to 11

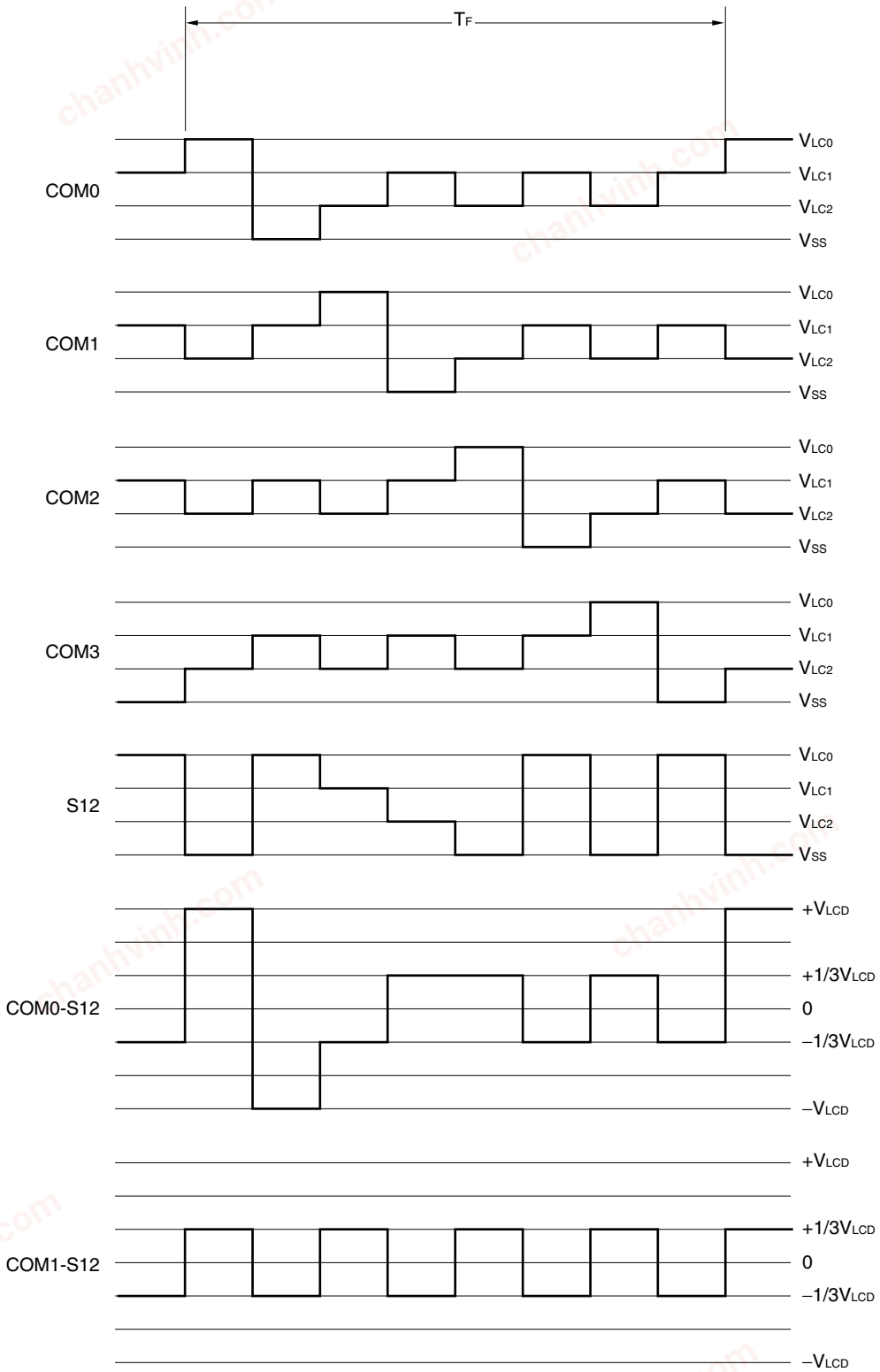
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Figure 10-12. Example of Connecting Four-Time Slot LCD Panel



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Figure 10-13. Four-Time Slot LCD Drive Waveform Examples



Remark The waveforms of COM2-S12 and COM3-S12 are not shown in the above chart.

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CHAPTER 11 POWER-ON-CLEAR CIRCUITS

μPD179327 Subseries provides a power-on-clear (POC) circuit.

In the flash memory version (μPD78F9328), the POC circuit is always operating. However, it can only be used when selected by a mask option in mask ROM versions (μPD179322, 179322A, 179324, 179324A, 179326, and 179327) (see **CHAPTER 16 MASK OPTIONS**).

11.1 Power-on-Clear Circuit Functions

The power-on-clear circuits include the following function.

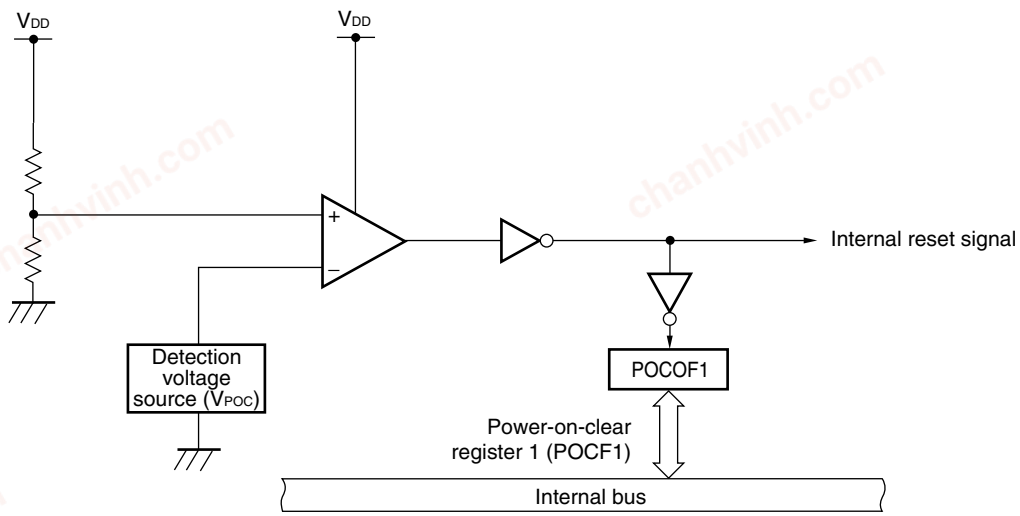
(1) Power-on-clear (POC) circuit

- Compares the detection voltage (V_{POC}) with the power supply voltage (V_{DD}) and generates an internal reset signal if $V_{DD} < V_{POC}$.
- This circuit can operate even in STOP mode.

11.2 Power-on-Clear Circuit Configuration

Figure 11-1 shows the block diagram of the power-on-clear circuits.

Figure 11-1. Block Diagram of Power-on-Clear Circuit



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11.3 Register Controlling Power-on-Clear Circuit

The power-on-clear circuits are controlled by the following register.

- Power-on-clear register 1 (POCF1)

(1) Power-on-clear register 1 (POCF1)

POCF1 controls POC circuit operation.

This register is set with a 1-bit or 8-bit memory manipulation instruction.

Figure 11-2. Format of Power-on-Clear Register 1

Symbol	7	6	5	4	3	<2>	1	0	Address	After reset	R/W
POCF1	0	0	0	0	0	POCOF1	0	0	FFDDH	00H[Note]	R/W

POCOF1	POC output detection flag
0	Non-generation of reset signal by POC or in cleared state due to a write operation to POCF1
1	Generation of reset signal by POC

Note This value is 04H only after a power-on-clear reset.

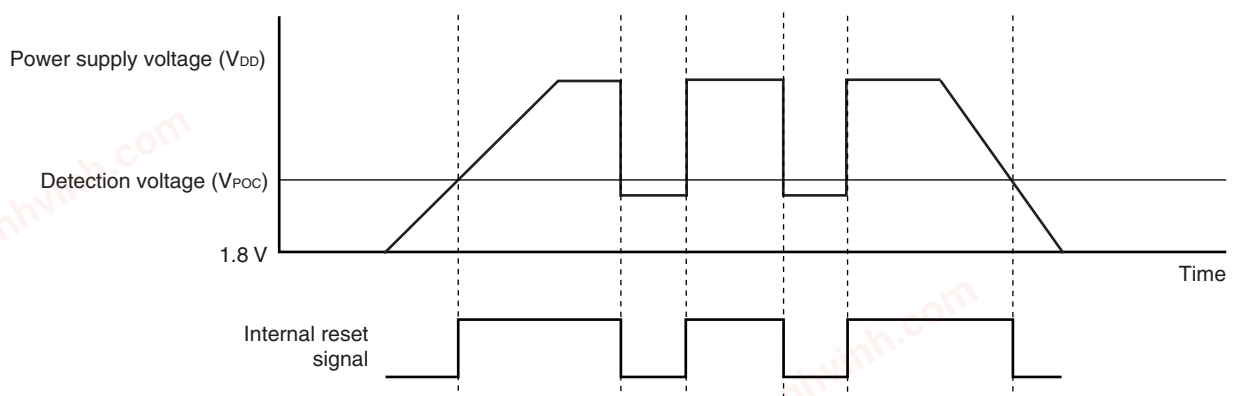
11.4 Power-on-Clear Circuit Operation

The POC circuit compares the detection voltage (V_{POC}) with the power supply voltage (V_{DD}) and generates an internal reset signal if $V_{DD} < V_{POC}$.

When a reset is generated via the power-on-clear circuit in bit 2 (POCOF1) on the power-on-clear register (POCF1) is set (1). This bit is then cleared (0) by an instruction written to POCF1. After a power-on-clear reset (i.e. after program execution has started from address 0000H), a power failure can be detected by detecting POCOF1.

Caution Use of the POC circuit can be selected by a mask option in the case of the mask ROM version. With the μPD78F9328, use of the POC circuit cannot be selected (always operating).

Figure 11-3. Timing of Internal Reset Signal Generation of POC Circuit



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CHAPTER 12 INTERRUPT FUNCTIONS

12.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Non-maskable interrupt

This interrupt is acknowledged unconditionally. It does not undergo interrupt priority control and is given top priority over all other interrupt requests.
A standby release signal is generated.
One interrupt source from the watchdog timer is incorporated as a non-maskable interrupt.

(2) Maskable interrupt

This interrupt undergoes mask control. If two or more interrupts with the same priority are simultaneously generated, each interrupt has a predetermined priority as shown in Table 12-1.
A standby release signal is generated.
2 external and 5 (6 for the μPD78F9328) internal interrupt sources are incorporated as maskable interrupts.

12.2 Interrupt Sources and Configuration

A total of 8 (9 for the μPD78F9328) non-maskable and maskable interrupts are incorporated as interrupt sources (see **Table 12-1**).

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Table 12-1. Interrupt Source List

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTCSI10	End of serial interface 10 3-wire SIO transfer reception[Note 3]	Internal	0008H[Note 3]	(B)
	3	INTWT	Watch timer interrupt		000AH	
	4	INTTM30	Generation of 8-bit timer 30 matching signal		000CH	
	5	INTTM40	Generation of 8-bit timer 40 matching signal		000EH	
	6	INTKR00	Key return signal detection	External	0010H	(C)
	7	INTWTI	Watch timer interval timer interrupt	Internal	0012H	(B)

Notes 1. Priority is the priority order when more than one maskable interrupt request is generated at the same time. 0 is the highest priority and 7 is the lowest.

2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in Figure 12-1.

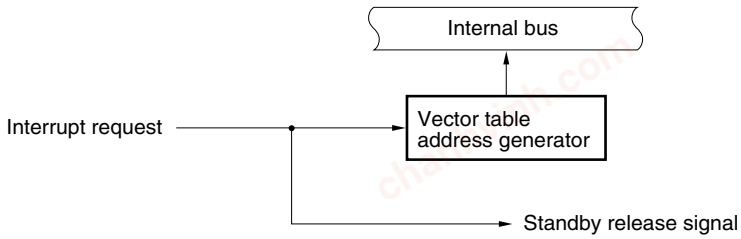
3. The μPD78F9328 only

Remark There are two interrupt sources for the watchdog timer (INTWDT): non-maskable and maskable interrupts (internal). Either one (but not both) should be selected for actual use.

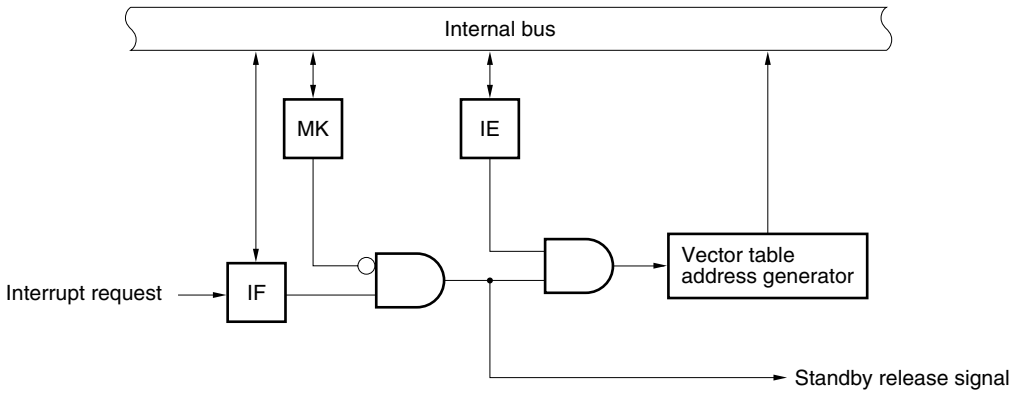
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Figure 12-1. Basic Configuration of Interrupt Function

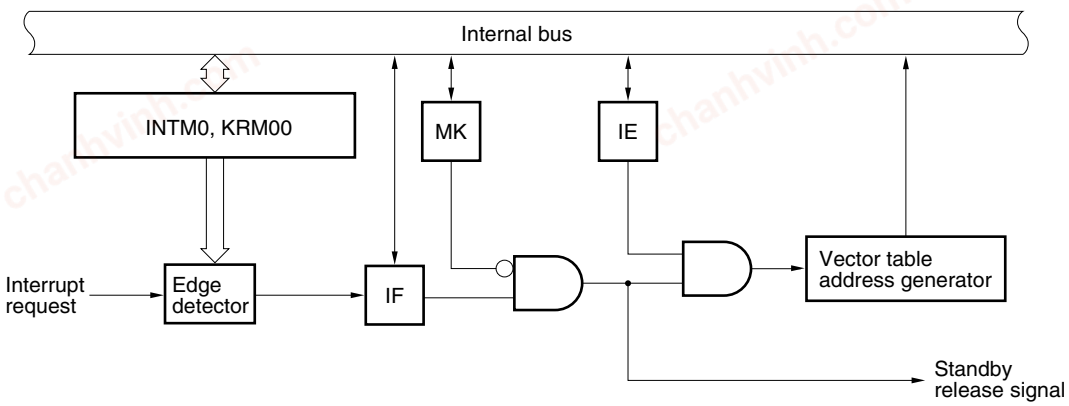
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



INTP0: External interrupt mode register 0
KRM00: Key return mode register 00
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

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12.3 Registers Controlling Interrupt Function

The following five types of registers are used to control the interrupt functions.

- Interrupt request flag register 0 (IF0)
- Interrupt mask flag register 0 (MK0)
- External interrupt mode register 0 (INTM0)
- Program status word (PSW)
- Key return mode register 00 (KRM00)

Table 12-2 gives a listing of interrupt request flag and interrupt mask flag names corresponding to interrupt requests.

Table 12-2. Flags Corresponding to Interrupt Request Signal Name

Interrupt Request Signal Name	Interrupt Request Flag	Interrupt Mask Flag
INTWDT	WDTIF	WDTMK
INTP0	PIF0	PMK0
INTCSI10 Note	CSIIF10 Note	CSIMK10 Note
INTWT	WTIF	WTMK
INTTM30	TMIF30	TMMK30
INTTM40	TMIF40	TMMK40
INTKR00	KRIF00	KRMK00
INTWTI	WTIIF	WTIMK

Note The μPD78F9328 only

(1) Interrupt request flag register 0 (IF0)

An interrupt request flag is set (1) when the corresponding interrupt request is generated, or when an instruction is executed. It is cleared (0) when the interrupt request is acknowledged, when the $\overline{\text{RESET}}$ signal is input, or when an instruction is executed.

IF0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears IF0 to 00H.

Figure 12-2. Format of Interrupt Request Flag Register 0

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
IF0	WTIIF	KRIF00	TMIF40	TMIF30	WTIF	CSIIF10 Note	PIF0	WDTIF	FFE0H	00H	R/W

××IF×	Interrupt request flag
0	No interrupt request signal generated
1	An interrupt request signal is generated and an interrupt request made

Note Provided in the μPD78F9328 only. Be sure to clear 0 for a mask ROM version.

Cautions 1. The WDTIF flag can be read/written only when the watchdog timer is being used as an interval timer. It must be cleared to 0 if the watchdog timer is used in watchdog timer mode 1 or 2.

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Cautions 2. Because P61 functions alternately as an external interrupt input, when the output level changes after the output mode of the port function is specified, the interrupt request flag will be inadvertently set. Therefore, be sure to preset the interrupt mask flag (PMK0) to 1 before using the port in output mode.

3. When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is started.

(2) Interrupt mask flag register 0 (MK0)

Interrupt mask flags are used to enable and disable the corresponding maskable interrupts.

MK0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets MK0 to FFH.

Figure 12-3. Format of Interrupt Mask Flag Register 0

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
MK0	WTIMK	KRMK00	TMMK40	TMMK30	WTMK	CSIMK10 Note	PMK0	WDTMK	FFE4H	FFH	R/W

××MK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Note Provided in the μPD78F9328 only. Be sure to set 1 for a mask ROM version.

Cautions 1. When the watchdog timer is being used in watchdog timer mode 1 or 2, any attempt to read the WDTMK flag results in an undefined value being detected.

2. Because P61 functions alternately as an external interrupt input, when the output level changes after the output mode of the port function is specified, the interrupt request flag will be inadvertently set. Therefore, be sure to preset the interrupt mask flag (PMK0) to 1 before using the port in output mode.

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(3) External interrupt mode register 0 (INTM0)

INTM0 is used to specify the valid edge for INTP0.

This register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears INTM0 to 00H.

Figure 12-4. Format of External Interrupt Mode Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
INTM0	0	0	0	0	ES01	ES00	0	0	FFECH	00H	R/W

ES01	ES00	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Cautions 1. Bits 0, 1, and 4 to 7 must be set to 0.

2. Before setting INTM0, set (1) the interrupt mask flag (PMK0) to disable interrupts. To enable interrupts, clear (0) the interrupt request flag (PIF0), then clear (0) the interrupt mask flag (PMK0).

(4) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for interrupt requests. The IE flag to set maskable interrupt enable/disable is mapped.

Besides 8-bit unit read/write, this register can carry out operations with a bit manipulation instruction and dedicated instructions (EI, DI). When a vectored interrupt is acknowledged, the PSW is automatically saved into a stack, and the IE flag is reset to 0.

$\overline{\text{RESET}}$ input sets PSW to 02H.

Figure 12-5. Configuration of Program Status Word

Symbol	7	6	5	4	3	2	1	0	After reset
PSW	IE	Z	0	AC	0	0	1	CY	02H

Used when normal instruction is executed

IE	Interrupt acknowledgement enabled/disabled
0	Disabled
1	Enabled

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(5) Key return mode register 00 (KRM00)

This register is used to specify whether the key return signal (falling edge of port 4) is to be detected.

This register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears KRM00 to 00H.

Figure 12-6. Format of Key Return Mode Register 00

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
KRM00	0	0	0	0	0	0	0	KRM00	FFF5H	00H	R/W

KRM00	Key return signal detection control
0	No detection
1	Detection (detecting falling edge of port 4)

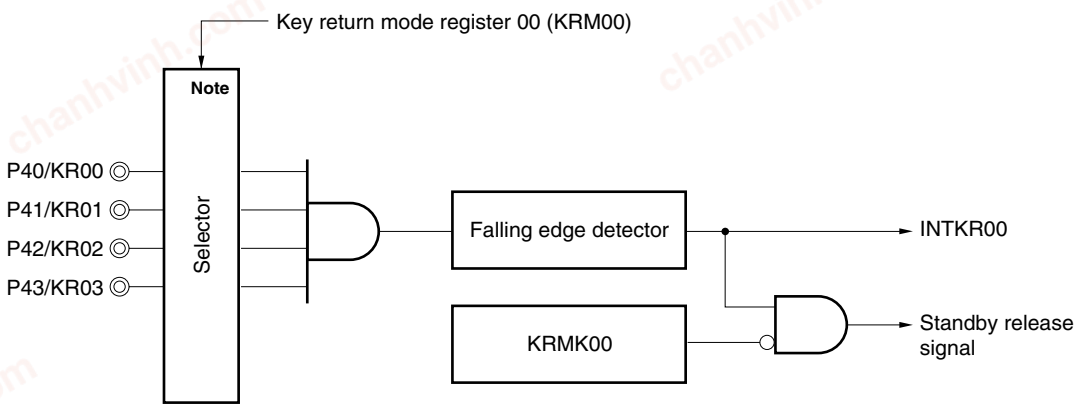
Cautions 1. Bits 1 to 7 must be set to 0.

2. Before setting KRM00, always set bit 6 of MK0 (KRMK00 = 1) to disable interrupts. After setting KRM00, clear KRMK00 after clearing bit 6 of IF1 (KRIF00 = 0) to enable interrupts.

3. On-chip pull-up resistors are automatically connected in input mode to the pins specified for key return signal detection (P40 to P43). Although these resistors are disconnected when the mode changes to output, key return signal detection continues unchanged.

4. The key return signal can be detected while all of P40 to P43 are high level. The key return signal cannot be detected while even one of P40 to P43 is low, even if any other key return pin goes low.

Figure 12-7. Block Diagram of Falling Edge Detector



Note Selector that selects the pin used for falling edge input

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12.4 Interrupt Servicing Operation

12.4.1 Non-maskable interrupt request acknowledgment operation

The non-maskable interrupt request is unconditionally acknowledged even when interrupts are disabled. It is not subject to interrupt priority control and takes precedence over all other interrupts.

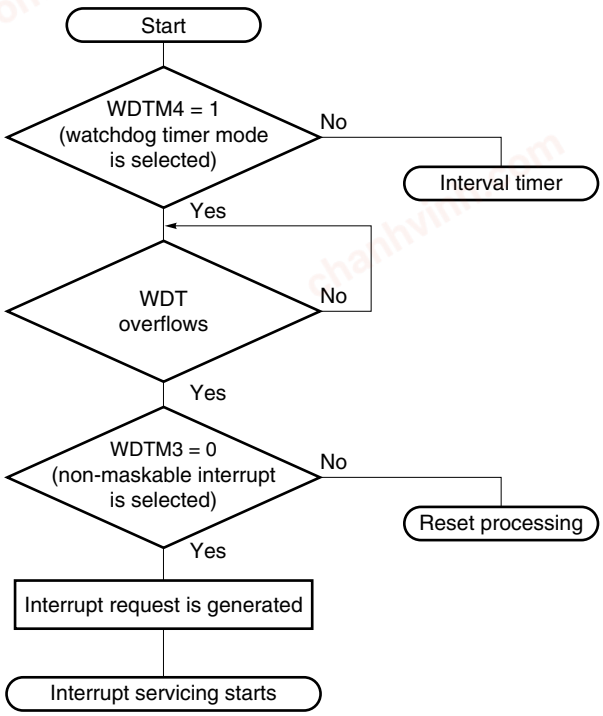
When the non-maskable interrupt request is acknowledged, PSW and PC are saved to the stack in that order, the IE flag is reset to 0, the contents of the vector table are loaded to the PC, and then program execution branches.

Figure 12-8 shows the flow from non-maskable interrupt request generation to acknowledgement, Figure 12-9 shows the timing of non-maskable interrupt acknowledgement, and Figure 12-10 shows the acknowledgement operation when a number of non-maskable interrupts are generated.

Caution During non-maskable interrupt service program execution, do not input another non-maskable interrupt request; if it is input, the service program will be interrupted and the new non-maskable interrupt request will be acknowledged.

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Figure 12-8. Flow from Generation of Non-Maskable Interrupt Request to Acknowledgment



WDTM: Watchdog timer mode register
WDT: Watchdog timer

Figure 12-9. Timing of Non-Maskable Interrupt Request Acknowledgment

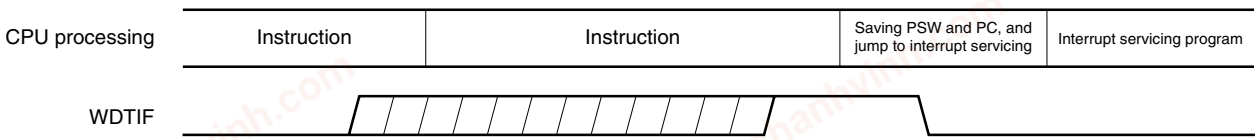
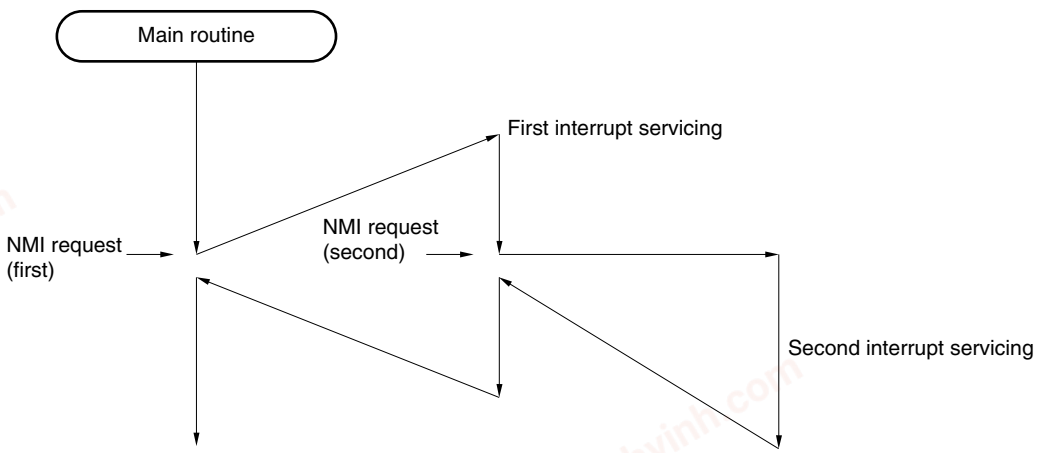


Figure 12-10. Non-Maskable Interrupt Request Acknowledgment



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12.4.2 Maskable interrupt request acknowledgment operation

A maskable interrupt request can be acknowledged when the interrupt request flag is set to 1 and the corresponding interrupt mask flag is cleared to 0. A vectored interrupt request is acknowledged in the interrupt enabled status (when the IE flag is set to 1).

The time required to start the interrupt servicing after a maskable interrupt request has been generated is shown in Table 12-3.

Refer to Figures 12-12 and 12-13 for the timing of interrupt request acknowledgement.

Table 12-3. Time from Generation of Maskable Interrupt Request to Servicing

Minimum Time	Maximum Time[Note]
9 clocks	19 clocks

Note The wait time is maximum when an interrupt request is generated immediately before BT or BF instruction.

Remark 1 clock: $\frac{1}{f_{CPU}}$ (f_{CPU}: CPU clock)

When two or more maskable interrupt requests are generated at the same time, they are acknowledged starting from the one assigned the highest priority by the priority specification flag.

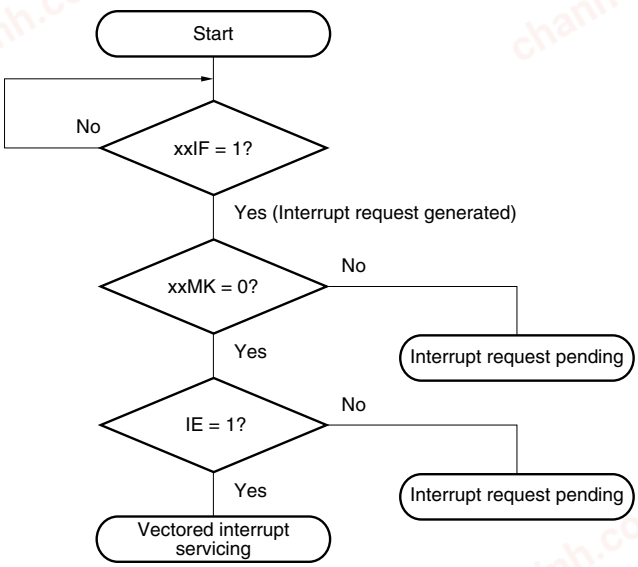
A pending interrupt is acknowledged when the status where it can be acknowledged is set.

Figure 12-11 shows the algorithm of interrupt request acknowledgement.

When a maskable interrupt request is acknowledged, the PSW and PC are saved to the stack in that order, the IE flag is reset to 0, and the data in the vector table determined for each interrupt request is loaded to the PC, and execution branches.

To return from interrupt servicing, use the RETI instruction.

Figure 12-11. Interrupt Request Acknowledgment Program Algorithm



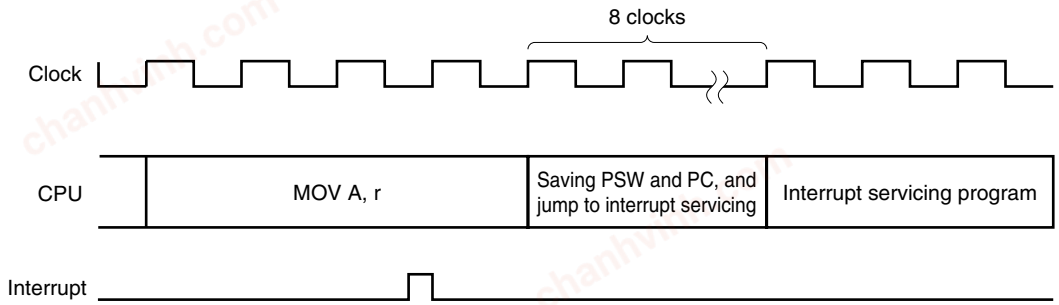
xxIF: Interrupt request flag

xxMK: Interrupt mask flag

IE: Flag to control maskable interrupt request acknowledgement (1 = enable, 0 = disable)

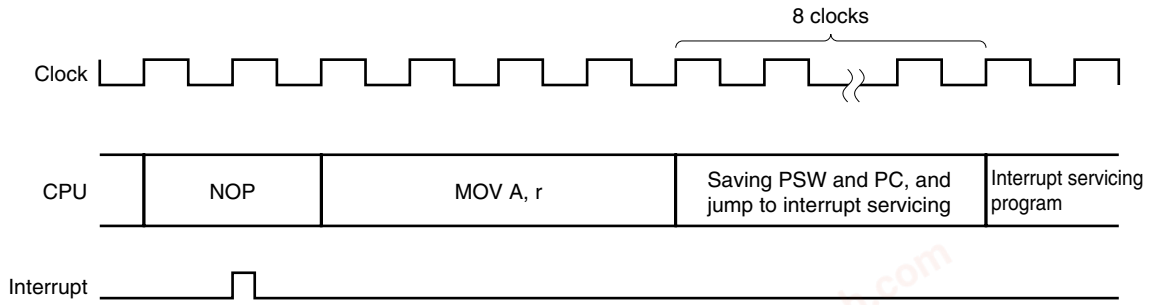
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Figure 12-12. Interrupt Request Acknowledgment Timing (Example: MOV A, r)



If the interrupt request has generated an interrupt request flag (xxIF) by the time the instruction clocks under execution, n clocks (n = 4 to 10), are n – 1, interrupt request acknowledgment processing will start following the completion of the instruction under execution. Figure 12-12 shows an example using the 8-bit data transfer instruction MOV A, r. Because this instruction is executed in 4 clocks, if an interrupt request is generated between the start of execution and the 3rd clock, interrupt request acknowledgment processing will take place following the completion of MOV A, r.

Figure 12-13. Interrupt Request Acknowledgment Timing
(When Interrupt Request Flag Is Generated in Final Clock Under Execution)



If the interrupt request flag (xxIF) is generated in the final clock of the instruction, interrupt request acknowledgment processing will begin after execution of the next instruction is complete.

Figure 12-13 shows an example whereby an interrupt request was generated in the 2nd clock of NOP (a 2-clock instruction). In this case, the interrupt request will be serviced after execution of MOV A, r, which follows NOP, is complete.

Caution When interrupt request flag register 0 (IF0), or interrupt mask flag register 0 (MK0) is being accessed, interrupt requests will be held pending.

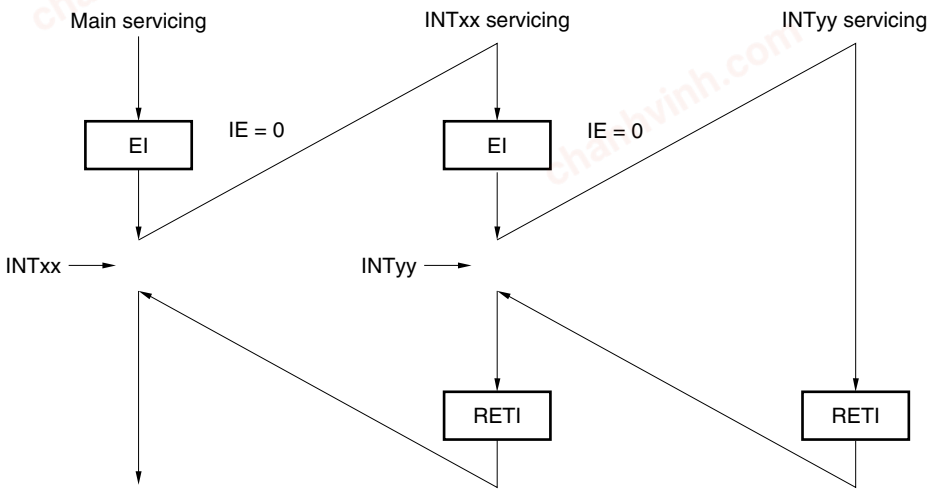
12.4.3 Multiple interrupt servicing

Multiple interrupts, in which another interrupt request is acknowledged while an interrupt request being serviced, can be serviced using the priority order. If multiple interrupts are generated at the same time, they are serviced in the order according to the priority assigned to each interrupt request in advance (refer to **Table 12-1**).

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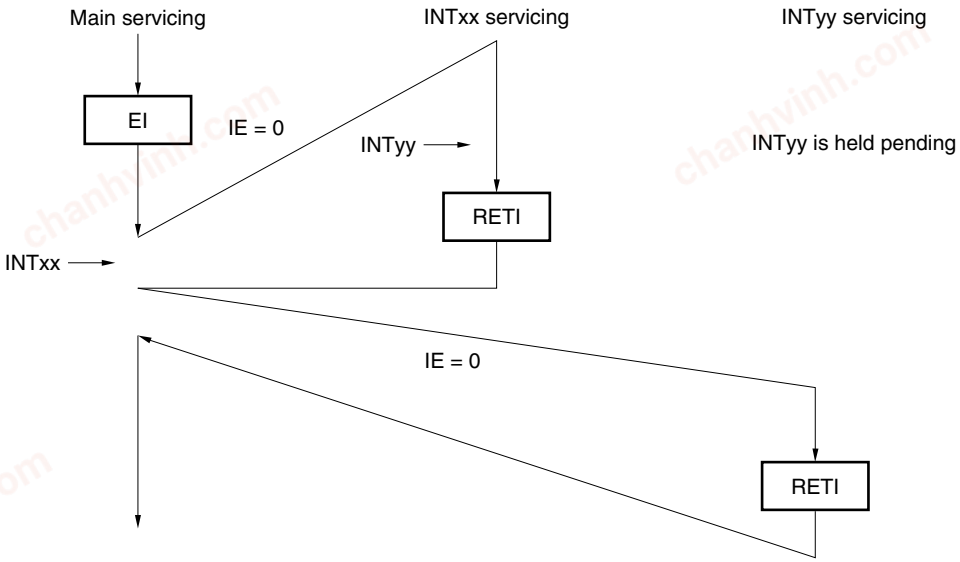
Figure 12-14. Example of Multiple Interrupts

Example 1. Acknowledging multiple interrupts



The interrupt request INTyy is acknowledged during the servicing of interrupt INTxx and multiple interrupts are performed. Before each interrupt request is acknowledged, the EI instruction is issued and the interrupt request is enabled.

Example 2. Multiple interrupts are not performed because interrupts are disabled



Because interrupt requests are disabled (the EI instruction has not been issued) in the interrupt INTxx servicing, the interrupt request INTyy is not acknowledged and multiple interrupts are not performed. INTyy is held pending and is acknowledged after INTxx servicing is completed.

IE = 0: Interrupt requests disabled

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12.4.4 Putting interrupt requests on hold

If an interrupt request (such as a maskable, non-maskable, or external interrupt) is generated when a certain type of instruction is being executed, the interrupt request will not be acknowledged until the instruction is completed. Such instructions (interrupt request pending instructions) are as follows.

- Instructions that manipulate interrupt request flag register 0 (IF0)
- Instructions that manipulate interrupt mask flag register 0 (MK0)

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CHAPTER 13 STANDBY FUNCTION

13.1 Standby Function and Configuration

The standby function is to reduce the power consumption of the system and can be effected in the following two modes:

(1) HALT mode

This mode is set when the HALT instruction is executed. The HALT mode stops the operation clock of the CPU. The system clock oscillator continues oscillating. This mode does not reduce the operating current as much as the STOP mode, but is useful for resuming processing immediately when an interrupt request is generated, or for intermittent operations.

(2) STOP mode

This mode is set when the STOP instruction is executed. The STOP mode stops the main system clock oscillator and stops the entire system. The power consumption of the CPU can be substantially reduced in this mode.

The data memory can be retained at the low voltage (V_{DD} = 1.8 V). Therefore, this mode is useful for retaining the contents of the data memory at an extremely low operating current.

The STOP mode can be released by an interrupt request, so that this mode can be used for intermittent operation. However, some time is required until the system clock oscillator stabilizes after the STOP mode has been released. If processing must be resumed immediately by using an interrupt request, therefore, use the HALT mode.

In both modes, the previous contents of the registers, flags, and data memory before setting the standby mode are all retained. In addition, the statuses of the output latch of the I/O ports and output buffer are also retained.

Caution To set the STOP mode, be sure to stop the operations of the peripheral hardware, and then execute the STOP instruction.

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13.2 Register Controlling Standby Function

The wait time after the STOP mode is released upon interrupt request until oscillation stabilizes is controlled with the oscillation stabilization time selection register (OSTS).

OSTS is set with a 1-bit or 8-bit memory manipulation instruction.

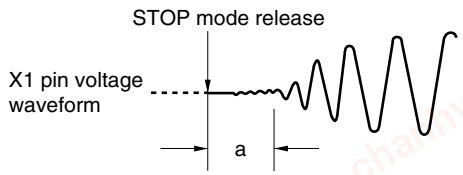
$\overline{\text{RESET}}$ input sets OSTS to 04H. Note that the time required for oscillation to stabilize after $\overline{\text{RESET}}$ input varies depending on the device (refer to **Table 13-1**), not depending on OSTS.

Figure 13-1. Format of Oscillation Stabilization Time Selection Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	
0	0	0	2^{12}/fx (819 μs)
0	1	0	2^{15}/fx (6.55 ms)
1	0	0	2^{17}/fx (26.2 ms)
Other than above			Setting prohibited

Caution The wait time after the STOP mode is released does not include the time from STOP mode release to clock oscillation start ("a" in the figure below), regardless of whether STOP mode is released by $\overline{\text{RESET}}$ input or by interrupt generation.



Remarks 1. fx: Main system clock oscillation frequency

2. The parenthesized values apply to operation at fx = 5.0 MHz.

Table 13-1. Oscillation Stabilization Time After $\overline{\text{RESET}}$ Input

Part Number	Oscillation Stabilization Time After $\overline{\text{RESET}}$ Input
μPD179322, 179322A, 179324, 179324A, 179326, 179327	2^{15}/fx or 2^{17}/fx (selectable using mask option)
μPD78F9328	2^{15}/fx

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13.3 Standby Function Operation

13.3.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction.

The operation status in the HALT mode is shown in the following table.

Table 13-2. Operation Statuses in HALT Mode

Item	HALT Mode Operation Status During Main System Clock Operation		HALT Mode Operation Status During Subsystem Clock Operation	
	Subsystem Clock Operating	Subsystem Clock Stopped	Main System Clock Operating	Main System Clock Stopped
Main system clock	Can be oscillated			Oscillation stopped
CPU	Operation stopped			
Ports (output latches)	Status before HALT mode setting retained			
8-bit timer 30, 40	Operable			Operation stopped
Watch timer	Operable	Operable[Note 1]	Operable	Operable[Note 2]
Watchdog timer	Operable		Operation stopped	
Power-on-clear circuit	Operable			
Key return circuit	Operable[Note 3]			
Serial interface 10 (provided in the μPD78F9328 only)	Operable			Operable[Note 4]
LCD controller/driver	Operable[Note 5]	Operable[Notes 1, 5]	Operable[Note 5]	Operable[Notes 2, 5]
External interrupts	Operable[Note 3]			

Notes 1. Operation is enabled when the main system clock is selected

2. Operation is enabled when the subsystem clock is selected

3. Operation is enabled only for a maskable interrupt that is not masked

4. Operation is enabled only when an external clock is selected

5. The HALT instruction can be set after display instruction execution

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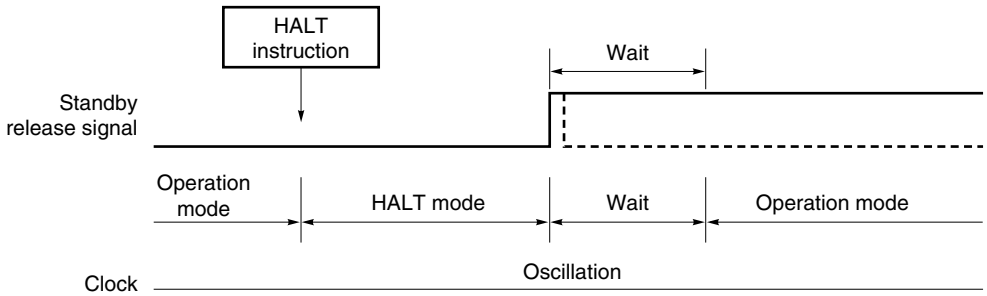
(2) Releasing HALT mode

The HALT mode can be released by the following three types of sources:

(a) Releasing by unmasked interrupt request

The HALT mode is released by an unmasked interrupt request. In this case, if the interrupt is enabled to be acknowledged, vectored interrupt processing is performed. If the interrupt is disabled, the instruction at the next address is executed.

Figure 13-2. Releasing HALT Mode by Interrupt



Remarks 1. The broken line indicates the case where the interrupt request that has released the standby mode is acknowledged.

2. The wait time is as follows:

- When vectored interrupt processing is performed: 9 to 10 clocks
- When vectored interrupt processing is not performed: 1 to 2 clocks

(b) Releasing by non-maskable interrupt request

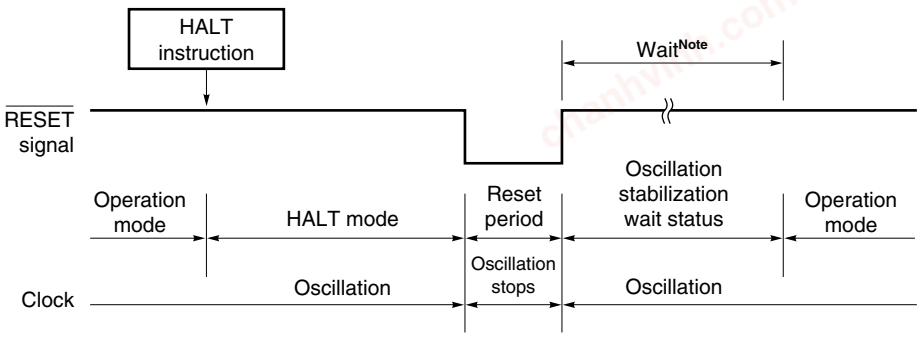
The HALT mode is released regardless of whether the interrupt is enabled or disabled, and vectored interrupt processing is performed.

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(c) Releasing by $\overline{\text{RESET}}$ input

When the HALT mode is released by the $\overline{\text{RESET}}$ signal, execution branches to the reset vector address in the same manner as the ordinary reset operation, and program execution is started.

Figure 13-3. Releasing HALT Mode by $\overline{\text{RESET}}$ Input



Note 2^{15}/fx: 6.55 ms (@ fx = 5.0 MHz operation)

Remark fx: Main system clock oscillation frequency

Table 13-3. Operation After Releasing HALT Mode

Releasing Source	MK××	IE	Operation
Maskable interrupt request	0	0	Executes next address instruction
	0	1	Executes interrupt servicing
	1	×	Retains HALT mode
Non-maskable interrupt request	–	×	Executes interrupt servicing
$\overline{\text{RESET}}$ input	–	–	Reset processing

×: don't care

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13.3.2 STOP mode

(1) Setting and operation status of STOP mode

The STOP mode is set by executing the STOP instruction.

Caution Because the standby mode can be released by an interrupt request signal, the standby mode is released as soon as it is set if there is an interrupt source whose interrupt request flag is set and interrupt mask flag is reset. When the STOP mode is set, therefore, the HALT mode is set immediately after the STOP instruction has been executed, the wait time set by the oscillation stabilization time selection register (OSTS) elapses, and then an operation mode is set.

The operation status in the STOP mode is shown in the following table.

Table 13-4. Operation Statuses in STOP Mode

Item	STOP Mode Operation Status During Main System Clock Operation	
	Subsystem Clock Operating	Subsystem Clock Stopped
Main system clock	Oscillation stopped	
CPU	Operation stopped	
Ports (output latches)	Status before STOP mode setting retained	
8-bit timer 30, 40	Operation stopped	
Watch timer	Operable Note 1	Operation stopped
Watchdog timer	Operation stopped	
Power-on-clear circuit	Operable	
Key return circuit	Operable Note 2	
Serial interface 10 (provided in the μPD78F9328 only)	Operable Note 3	
LCD controller/driver	Operable Note 1	Operation stopped Note 4
External interrupts	Operable Note 2	

Notes 1. Operation is enabled when the subsystem clock is selected.

2. Operation is enabled only for a maskable interrupt that is not masked.

3. Operation is enabled only when an external clock is selected.

4. Before selecting the STOP mode, disable display and select the static mode (refer to **10.3 (1) LCD display mode register 0 (LCDM0)**).

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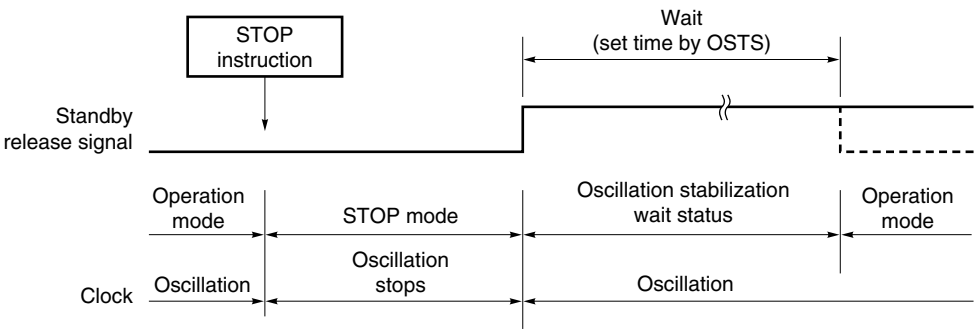
(2) Releasing STOP mode

The STOP mode can be released by the following two types of sources:

(a) Releasing by unmasked interrupt request

The STOP mode can be released by an unmasked interrupt request. In this case, if the interrupt is enabled to be acknowledged, vectored interrupt processing is performed, after the oscillation stabilization time has elapsed. If the interrupt is disabled, the instruction at the next address is executed.

Figure 13-4. Releasing STOP Mode by Interrupt



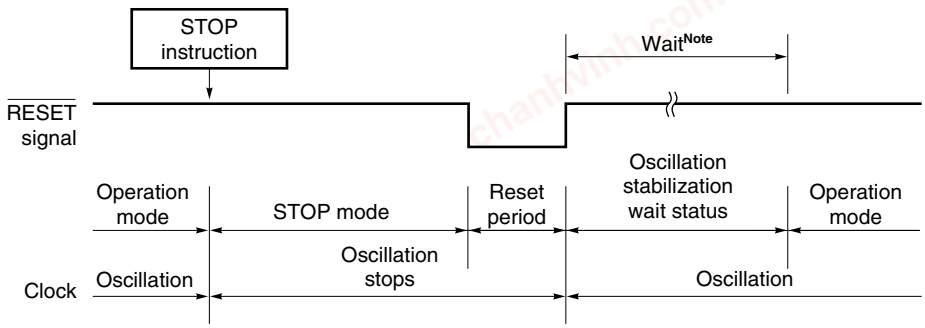
Remark The broken line indicates the case where the interrupt request that has released the standby mode is acknowledged.

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(b) Releasing by $\overline{\text{RESET}}$ input

When the STOP mode is released by the $\overline{\text{RESET}}$ signal, the reset operation is performed after the oscillation stabilization time has elapsed.

Figure 13-5. Releasing STOP Mode by $\overline{\text{RESET}}$ Input



Note 2^{15}/fx: 6.55 ms (@ fx = 5.0 MHz operation)

Remark fx: Main system clock oscillation frequency

Table 13-5. Operation After Releasing STOP Mode

Releasing Source	MK××	IE	Operation
Maskable interrupt request	0	0	Executes next address instruction
	0	1	Executes interrupt servicing
	1	×	Retains STOP mode
$\overline{\text{RESET}}$ input	–	–	Reset processing

×: don't care

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CHAPTER 14 RESET FUNCTION

The following three operations are available to generate reset signals.

(1) External reset signal input via $\overline{\text{RESET}}$ pin
(2) Internal reset by detection of watchdog timer inadvertent program loop time
(3) Internal reset using power-on-clear circuit (POC[Note])

The external and internal reset signals are functionally equivalent. When $\overline{\text{RESET}}$ is input, program execution begins from the addresses written at addresses 0000H and 0001H.

If a low-level signal is applied to the $\overline{\text{RESET}}$ pin, or if the watchdog timer overflows, a reset occurs, causing each item of the hardware to enter the states listed in Table 14-1. While a reset is being applied, or while the oscillation frequency is stabilizing immediately after the end of a reset sequence, each pin remains in the high-impedance state.

If a high-level signal is applied to the $\overline{\text{RESET}}$ pin, the reset sequence is terminated, and program execution is started after the oscillation stabilization time has elapsed. A reset sequence caused by a watchdog timer overflow is terminated automatically and program execution is started after the oscillation stabilization time has elapsed.

Reset by power-on-clear (POC[Note]) is cleared if the supply voltage rises beyond a specific level, and the program execution is started after the oscillation stabilization time has elapsed.

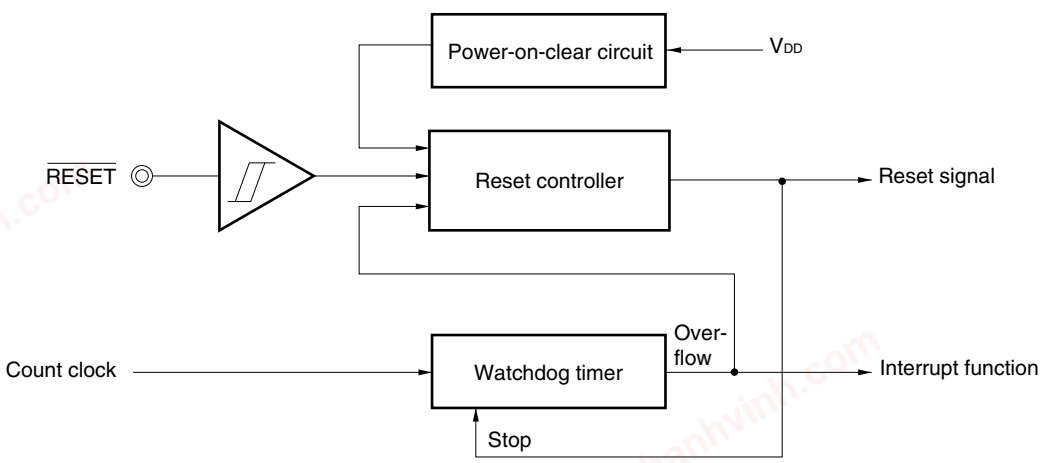
Note Enabled in mask ROM versions (μPD179322, 179322A, 179324, 179324A, 179326, and 179327) only when POC circuit usage is selected by a mask option.

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.

2. When the STOP mode is cleared by reset, the STOP mode contents are held during reset input. However, the port pins become high impedance.

3. In the case of mask ROM versions, the oscillation stabilization time after $\overline{\text{RESET}}$ input or the release of STOP mode by POC can be selected from $2^{15}/f_X$ or $2^{17}/f_X$ by mask option (refer to CHAPTER 16 MASK OPTIONS). In the case of the μPD78F9328, only $2^{15}/f_X$ can be set because the mask option is not available.

Figure 14-1. Block Diagram of Reset Function



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Figure 14-2. Reset Timing by $\overline{\text{RESET}}$ Input

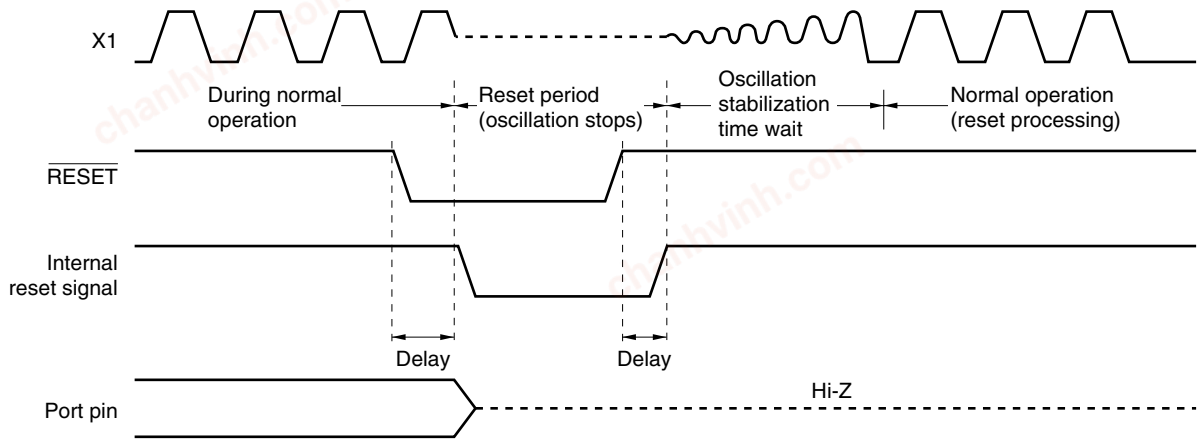


Figure 14-3. Reset Timing by Overflow in Watchdog Timer

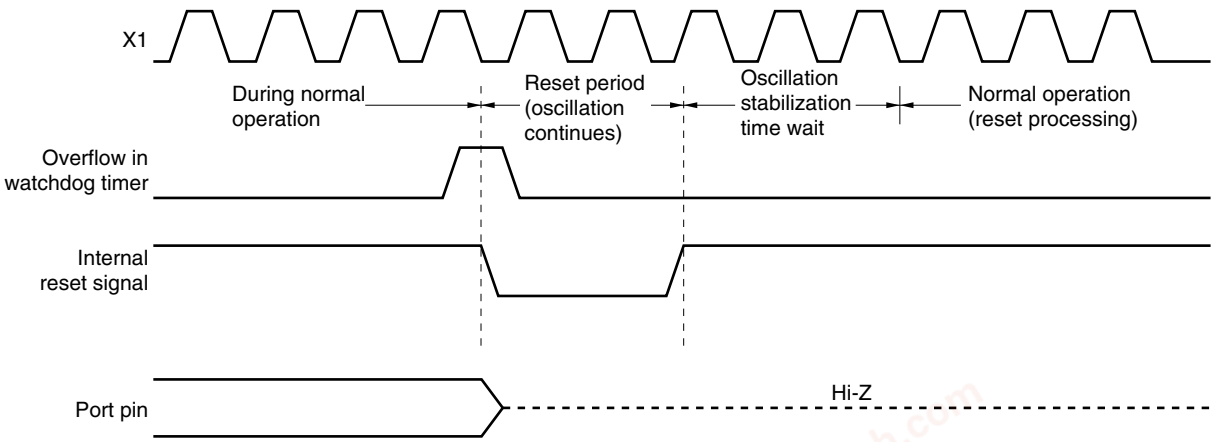
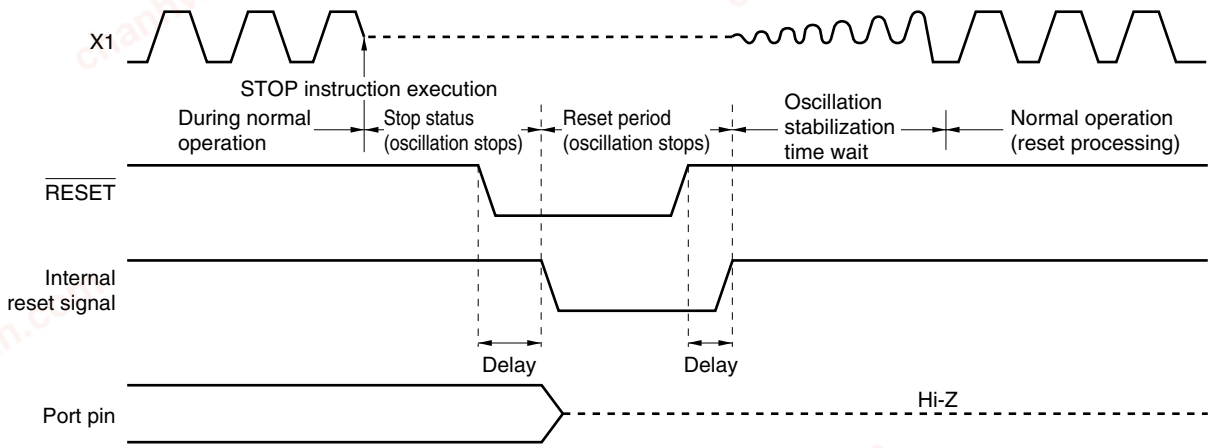


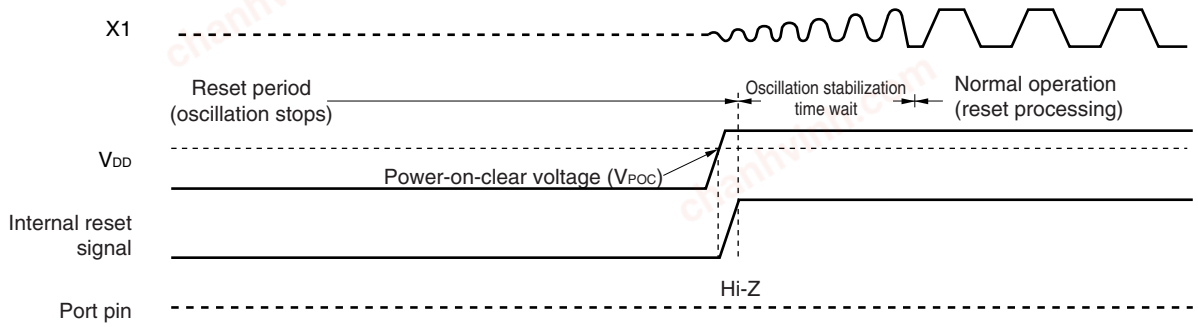
Figure 14-4. Reset Timing by $\overline{\text{RESET}}$ Input in STOP Mode



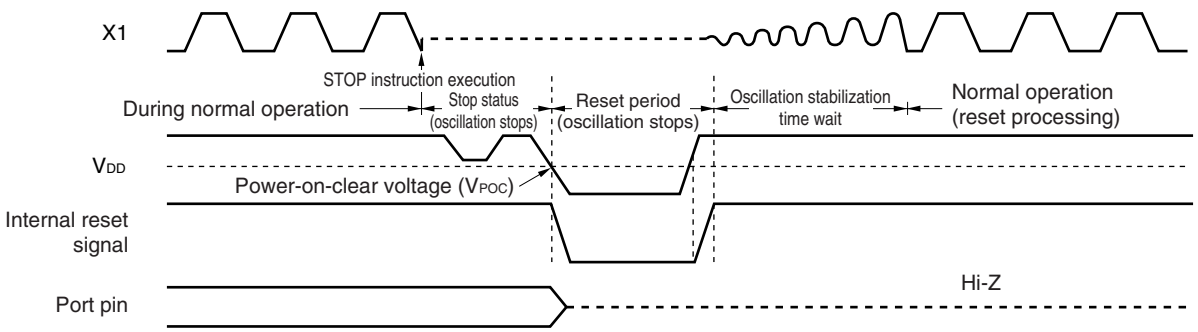
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Figure 14-5. Reset Timing by Power-on Clear

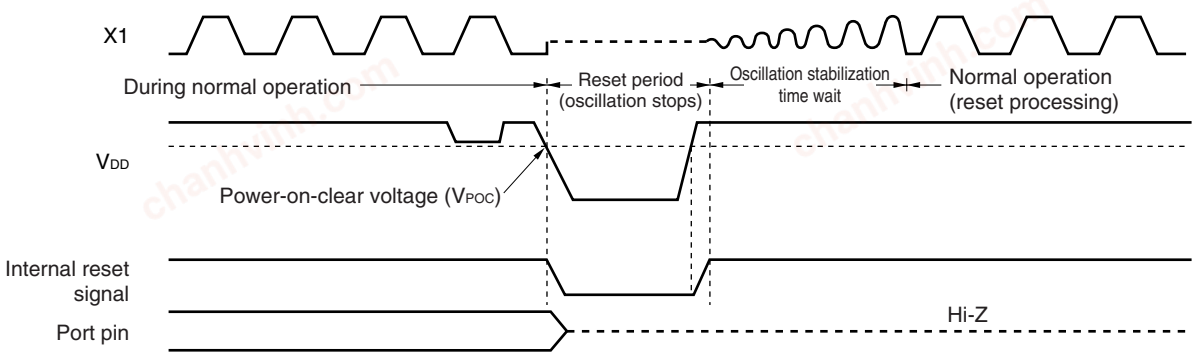
(a) At power application



(b) In STOP mode



(c) In normal operation mode (including HALT mode)



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Table 14-1. Hardware Status After Reset

Hardware		Status After Reset
Program counter (PC)[Note 1]		Contents of reset vector table (0000H, 0001H) set
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Ports (P0 to P2, P4, P6, P8) (output latches)		00H
Port mode registers (PM0 to PM2, PM4, PM6)		FFH
Port mode register 8 (PM8)		3FH
Port function register 8 (PF8)		00H
Pull-up resistor option registers (PU0, PUB2)		00H
Processor clock control register (PCC)		02H
Suboscillation mode register (SCKM)		00H
Subclock control register (CSS)		00H
Oscillation stabilization time selection register (OSTS)		04H
8-bit timer 30, 40	Timer counters (TM30, TM40)	00H
	Compare registers (CR30, CR40, CRH40)	Undefined
	Mode control registers (TMC30, TMC40)	00H
	Carrier generator output control register (TCA40)	00H
Watch timer	Mode control register (WTM)	00H
Watchdog timer	Mode register (WDTM)	00H
	Clock selection register (TCL2)	00H
Serial interface 10 (Provided in the μPD78F9328 only)	Serial operation mode register 10 (CSIM10)[Note 3]	00H
	Transmit/receive shift register 10 (SIO10)[Note 3]	Undefined
LCD controller/driver	Display mode register 0 (LCDM0)	00H
	Clock control register 0 (LCDC0)	00H
Power-on-clear circuit	Power-on-clear register 1 (POCF1)	00H[Note 4]
Interrupts	Request flag register 0 (IF0)	00H
	Mask flag register 0 (MK0)	FFH
	External interrupt mode register 0 (INTM0)	00H
	Key return mode register 00 (KRM00)	00H

Notes 1. While a reset signal is being input, and during the oscillation stabilization time wait, only the contents of the PC will be undefined; the remainder of the hardware will be the same state as after reset.

2. In standby mode, RAM enters the hold state after reset.

3. Provided in the μPD78F9328 only

4. The value is 04H only after a power-on-clear reset.

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CHAPTER 15 μPD78F9328

The μPD78F9328 is available as the flash memory version of the μPD179327 Subseries.

The μPD78F9328 is a version with the internal ROM of the μPD179322, 179322A, 179324, 179324A, 179326, 179327 replaced with flash memory. The differences between the μPD78F9328 and the mask ROM versions are shown in Table 15-1.

Table 15-1. Differences Between μPD78F9328 and Mask ROM Versions

Item \ Part Number		Flash Memory Version	Mask ROM Version			
		μPD78F9328	μPD179322 μPD179322A	μPD179324 μPD179324A	μPD179326	μPD179327
Internal memory	ROM	32 KB (flash memory)	4 KB	8 KB	16 KB	24 KB
	High-speed RAM	512 bytes	256 bytes		512 bytes	
	LCD display RAM	24 × 4 bits				
IC0 pin		Not provided	Provided			
V_{PP} pin		Provided	Not provided			
Serial interface 10		Provided	Not provided			
Power-on clear (POC) circuit		Always operates	Use is selected by mask option			
Oscillation stabilization wait time after STOP mode is released by RESET or POC		Fixed to $2^{15}/f_X$	$2^{15}/f_X$ or $2^{17}/f_X$ selected by mask option			
Power supply voltage		V_{DD} = 1.8 to 5.5 V	V_{DD} = 1.8 to 3.6 V			
Electrical specifications		Refer to **CHAPTER 18 ELECTRICAL SPECIFICATIONS (μPD179322, 179322A, 179324, 179324A, 179326, AND 179327) and CHAPTER 19 ELECTRICAL SPECIFICATIONS (μPD78F9328)**				

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

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15.1 Flash Memory Characteristics

Flash memory programming is performed by connecting a dedicated flash programmer (Flashpro IV (part no. FL-PR4, PG-FP4)) to the target system with the flash memory mounted on the target system (on-board). A flash memory writing adapter (program adapter), which is a target board used exclusively for programming, is also provided.

Remark FL-PR4, and the program adapter are the products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

Programming using flash memory has the following advantages.

- Software can be modified after the microcontroller is solder-mounted on the target system.
- Distinguishing software facilities low-quantity, varied model production
- Easy data adjustment when starting mass production

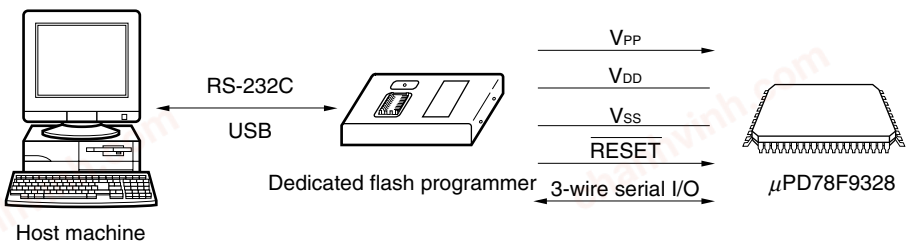
15.1.1 Programming environment

The following shows the environment required for μPD78F9328 flash memory programming.

When Flashpro III/Flashpro IV is used as a dedicated flash programmer, a host machine is required to control the dedicated flash programmer. Communication between the host machine and flash programmer is performed via RS-232C/USB (Rev.1.1).

For details, refer the manuals for Flashpro IV.

Figure 15-1. Environment for Writing Program to Flash Memory



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15.1.2 Communication mode

Use the communication mode shown in Table 15-2 to perform communication between the dedicated flash programmer and μPD78F9328.

Table 15-2. Communication Mode List

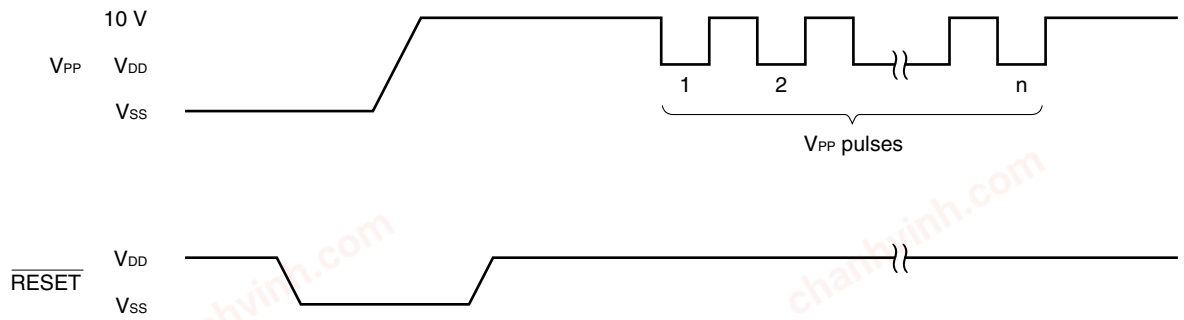
Communication Mode	TYPE Setting[Note 1]					Pins used	Number of V_{PP} pulses
	COMM PORT	SIO clock	CPU Clock		Multiple rate		
			In Flashpro	On Target Board			
3-wire serial I/O	SIO ch-0 (3-wired, sync)	100 Hz to 1.25 MHz[Note2]	1, 2, 4, 5 MHz[Notes 2, 3]	1 to 5 MHz[Note 2]	1.0	$\overline{SCK}$10/P20 SO10/P21 SI10/P22	0

Notes 1. Selection items for TYPE settings on the dedicated flash programmer (Flashpro IV (part no. FL-PR4, PG-FP4)).

2. The possible setting range differs depending on the voltage. For details, refer to **CHAPTER 19 ELECTRICAL SPECIFICATIONS (μPD78F9328).**

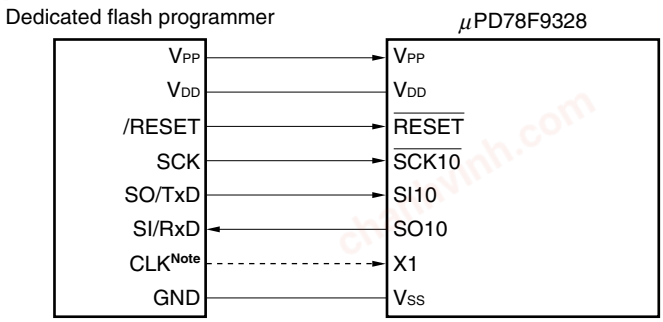
Caution Be sure to select a communication mode depending on the number of V_{PP} pulses shown in Table 15-2.

Figure 15-2. Communication Mode Selection Format



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Figure 15-3. Example of Connection with Dedicated Flash Programmer



Note Connect this pin when the system clock is supplied by dedicated flash programmer. If an oscillator is already connected to the X1 pin, do not connect to the CLK pin.

Caution The V_{DD} pin, if already connected to the power supply, must be connected to the VDD pin of the dedicated flash programmer. Before using the power supply connected to the V_{DD} pin, supply voltage before starting programming.

If Flashpro III/Flashpro IV is used as a dedicated flash programmer, the following signals are generated for the μPD78F9328. For details, refer to the manual of Flashpro III/Flashpro IV.

Table 15-3. Pin Connection List

Signal Name	I/O	Pin Function	Pin Name	3-Wire Serial I/O
VPP1	Output	Write voltage	V_{PP}	◎
VPP2	–	–		×
VDD	I/O	V_{DD} voltage generation	V_{DD}	◎ Note
GND	–	Ground	V_{SS}	◎
CLK	Output	Clock output	X1	○
RESET	Output	Reset signal	$\overline{\text{RESET}}$	◎
SI	Input	Reception signal	SO10	◎
SO	Output	Transmit signal	SI10	◎
SCK	Output	Transfer clock	$\overline{\text{SCK10}}$	◎
HS	–	–	–	×

Note V_{DD} voltage must be supplied before programming is started.

Remark ◎: Pin must be connected.
○: If the signal is supplied on the target board, pin need not be connected.
×: Pin need not be connected.

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15.1.3 On-board pin processing

When performing programming on the target system, provide a connector on the target system to connect the dedicated flash programmer.

An on-board function that allows switching between normal operation mode and flash memory programming mode may be required in some cases.

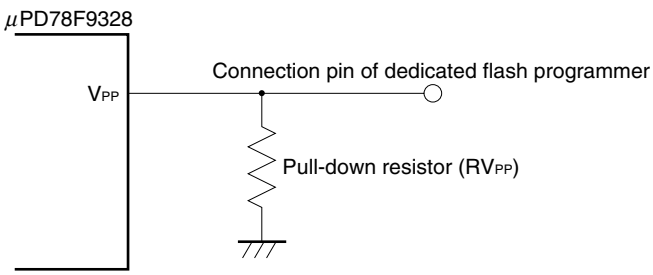
<V_{PP} pin>

In normal operation mode, input 0 V to the V_{PP} pin. In flash memory programming mode, a write voltage of 10.0 V (TYP.) is supplied to the V_{PP} pin, so perform the following.

(1) Connect a pull-down resistor (RV_{PP} = 10 kΩ) to the V_{PP} pin.
(2) Use the jumper on the board to switch the V_{PP} pin input to either the writer or directly to GND.

A V_{PP} pin connection example is shown below.

Figure 15-4. V_{PP} Pin Connection Example



<Serial interface pin>

The following shows the pins used by the serial interface.

Serial Interface	Pins Used
3-wire serial I/O	$\overline{SCK10}$, SO10, SI10

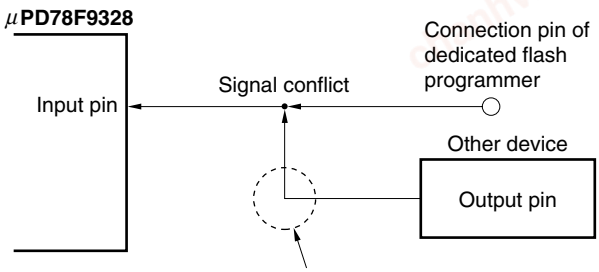
When connecting the dedicated flash programmer a serial interface pin that is connected to another device on-board, signal conflict or abnormal operation of the other devices may occur. Care must therefore be taken with such connections.

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(1) Signal conflict

If the dedicated flash programmer (output) is connected to a serial interface pin (input) that is connected to another device (output), a signal conflict occurs. To prevent this, isolate the connection with the other device or set the other device to the output high impedance status.

Figure 15-5. Signal Conflict (Input Pin of Serial Interface)

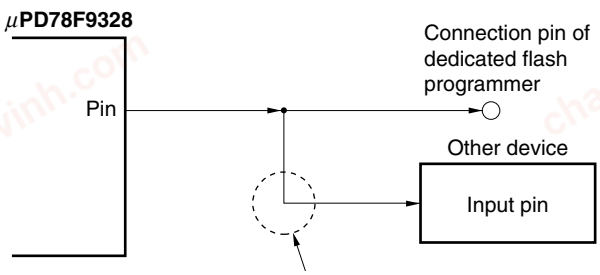


In the flash memory programming mode, the signal output by another device and the signal sent by the dedicated flash programmer conflict, therefore, isolate the signal of the other device.

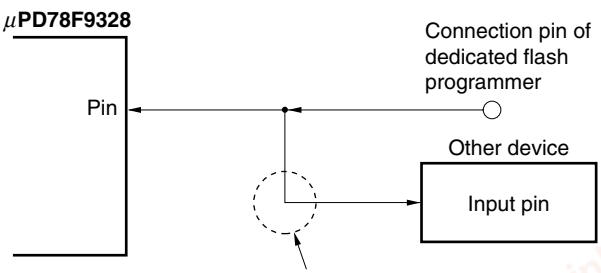
(2) Abnormal operation of other device

If the dedicated flash programmer (output or input) is connected to a serial interface pin (input or output) that is connected to another device (input), a signal is output to the device, and this may cause an abnormal operation. To prevent this abnormal operation, isolate the connection with the other device or set so that the input signals to the other device are ignored.

Figure 15-6. Abnormal Operation of Other Device



If the signal output by the μPD78F9328 affects another device in the flash memory programming mode, isolate the signals of the other device.



If the signal output by the dedicated flash programmer affects another device in the flash memory programming mode, isolate the signals of the other device.

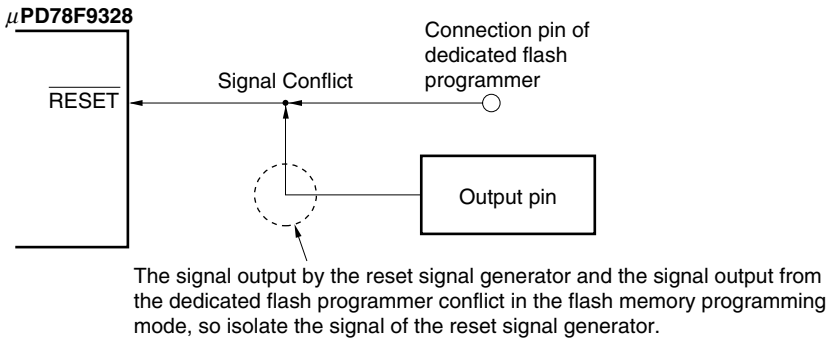
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<RESET pin>

If the reset signal of the dedicated flash programmer is connected to the RESET pin connected to the reset signal generator on-board, a signal conflict occurs. To prevent this, isolate the connection with the reset signal generator.

If the reset signal is input from the user system in the flash memory programming mode, a normal programming operation cannot be performed. Therefore, do not input reset signals from other than the dedicated flash programmer.

Figure 15-7. Signal Conflict (RESET Pin)



<Port pins>

When the μPD78F9328 enters the flash memory programming mode, all the pins other than those that communicate in flash memory programming are in the same status as immediately after reset.

If the external device does not recognize initial statuses such as the output high impedance status, therefore, connect the external device to V_{DD} or V_{SS} via a resistor.

<Oscillator>

When using the on-board clock, connect X1 and X2 as required in the normal operation mode.

When using the clock output of the flash programmer, connect it directly to X1, disconnecting the main oscillator on-board, and leave the X2 pin open.

<Power supply>

When using the power supply output of the flash programmer, connect the V_{DD} and V_{SS} pins to VDD and GND of the flash programmer, respectively.

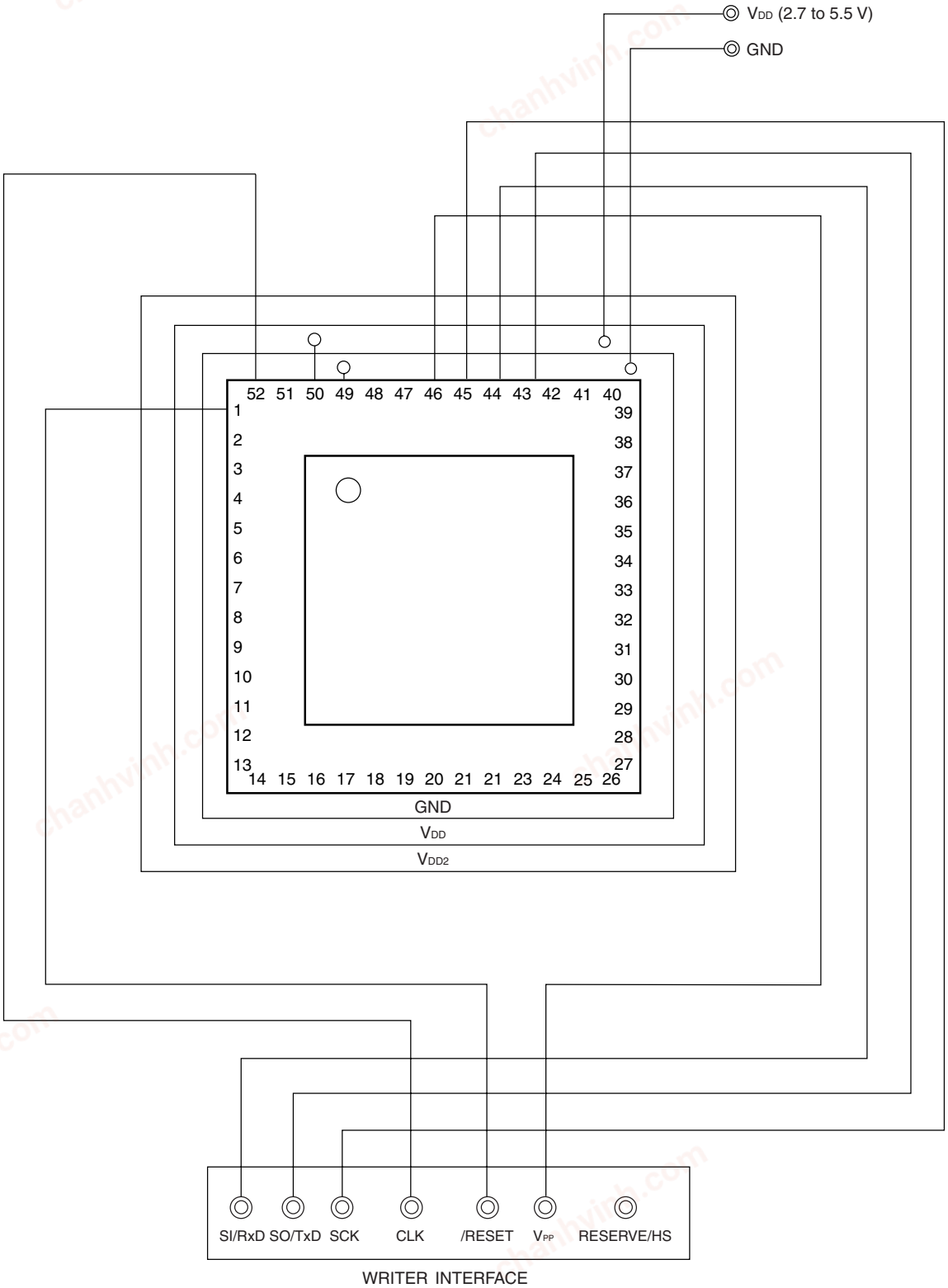
When using the on-board power supply, connect it as required in the normal operation mode. Because the flash programmer monitors the voltage, however, VDD of the flash programmer must be connected.

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15.1.4 Connection on flash memory writing adapter

The following shows an example of the recommended connection when using the flash memory writing adapter.

Figure 15-8. Wiring Example of Flash Memory Writing Adapter Using 3-Wire Serial I/O Mode



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CHAPTER 16 MASK OPTIONS

The mask ROM versions (μPD179322, 179322A, 179324, 179324A, 179326, and 179327) have the following mask option.

- Oscillation stabilization wait time
  The oscillation stabilization wait time after the release of STOP mode by $\overline{\text{RESET}}$ or POC can be selected.
  <1> 2^{15}/fx
  <2> 2^{17}/fx

Caution The oscillation stabilization wait time for the flash memory version (μPD78F9328) is fixed to 2^{15}/fx.

- Power-on-clear (POC) circuit
  Use/non use of the POC circuit can be selected.
  <1> POC circuit used
  <2> POC circuit not used

Caution The POC circuit of the flash memory version (μPD78F9328) is always used (always operating).

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CHAPTER 17 INSTRUCTION SET

This chapter lists the instruction set of the μPD179327 Subseries. For the details of the operation and machine language (instruction code) of each instruction, refer to **78K/0S Series Instructions User's Manual (U11047E)**.

17.1 Operation

17.1.1 Operand identifiers and description methods

Operands are described in "Operands" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and symbols, #, !, $, and [ ] are key words and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, $ and [ ] symbols.

For operand register identifiers, r and rp, either functional names (X, A, C, etc.) or absolute names (names in parenthesis in the table below, R0, R1, R2, etc.) can be used for description.

Table 17-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special-function register symbol
saddr saddrp	FE20H to FF1FH Immediate data or labels FE20H to FF1FH Immediate data or labels (even addresses only)
addr16 addr5	0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions) 0040H to 007FH Immediate data or labels (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

Remark See **Table 3-3 Special Function Registers** for symbols of special function registers.

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17.1.2 Description of “Operation” column

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Flag indicating non-maskable interrupt servicing in progress
( ):	Memory contents indicated by address or register contents in parenthesis
X_H, X_L:	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
$\veebar$:	Exclusive logical sum (exclusive OR)
$\overline{\ }$:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

17.1.3 Description of “Flag” column

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
x:	Set/cleared according to the result
R:	Previously saved value is restored

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17.2 Operation List

Mnemonic	Operands	Byte	Clock	Operation	Flag
					Z AC CY
MOV	r, #byte	3	6	r ← byte	
	saddr, #byte	3	6	(saddr) ← byte	
	sfr, #byte	3	6	sfr ← byte	
	A, r Note 1	2	4	A ← r	
	r, A Note 1	2	4	r ← A	
	A, saddr	2	4	A ← (saddr)	
	saddr, A	2	4	(saddr) ← A	
	A, sfr	2	4	A ← sfr	
	sfr, A	2	4	sfr ← A	
	A, !addr16	3	8	A ← (addr16)	
	!addr16, A	3	8	(addr16) ← A	
	PSW, #byte	3	6	PSW ← byte	x x x
	A, PSW	2	4	A ← PSW	
	PSW, A	2	4	PSW ← A	x x x
	A, [DE]	1	6	A ← (DE)	
	[DE], A	1	6	(DE) ← A	
	A, [HL]	1	6	A ← (HL)	
	[HL], A	1	6	(HL) ← A	
	A, [HL+byte]	2	6	A ← (HL + byte)	
	[HL+byte], A	2	6	(HL + byte) ← A	
XCH	A, X	1	4	A ↔ X	
	A, r Note 2	2	6	A ↔ r	
	A, saddr	2	6	A ↔ (saddr)	
	A, sfr	2	6	A ↔ sfr	
	A, [DE]	1	8	A ↔ (DE)	
	A, [HL]	1	8	A ↔ (HL)	
	A, [HL+byte]	2	8	A ↔ (HL + byte)	

Notes 1. Except r = A.

2. Except r = A, X.

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

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Mnemonic	Operands	Byte	Clock	Operation	Flag
					Z AC CY
MOVW	rp, #word	3	6	rp ← word	
	AX, saddrp	2	6	AX ← (saddrp)	
	saddrp, AX	2	8	(saddrp) ← AX	
	AX, rp Note	1	4	AX ← rp	
	rp, AX Note	1	4	rp ← AX	
XCHW	AX, rp Note	1	8	AX ↔ rp	
ADD	A, #byte	2	4	A, CY ← A + byte	x x x
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	x x x
	A, r	2	4	A, CY ← A + r	x x x
	A, saddr	2	4	A, CY ← A + (saddr)	x x x
	A, !addr16	3	8	A, CY ← A + (addr16)	x x x
	A, [HL]	1	6	A, CY ← A + (HL)	x x x
	A, [HL+byte]	2	6	A, CY ← A + (HL + byte)	x x x
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	x x x
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	x x x
	A, r	2	4	A, CY ← A + r + CY	x x x
	A, saddr	2	4	A, CY ← A + (saddr) + CY	x x x
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	x x x
	A, [HL]	1	6	A, CY ← A + (HL) + CY	x x x
	A, [HL+byte]	2	6	A, CY ← A + (HL + byte) + CY	x x x
SUB	A, #byte	2	4	A, CY ← A – byte	x x x
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	x x x
	A, r	2	4	A, CY ← A – r	x x x
	A, saddr	2	4	A, CY ← A – (saddr)	x x x
	A, !addr16	3	8	A, CY ← A – (addr16)	x x x
	A, [HL]	1	6	A, CY ← A – (HL)	x x x
	A, [HL+byte]	2	6	A, CY ← A – (HL + byte)	x x x

Note Only when rp = BC, DE, or HL.

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

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Mnemonic	Operands	Byte	Clock	Operation	Flag		
					Z	AC	CY
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	x	x	x
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	x	x	x
	A, r	2	4	A, CY ← A – r – CY	x	x	x
	A, saddr	2	4	A, CY ← A – (saddr) – CY	x	x	x
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	x	x	x
	A, [HL]	1	6	A, CY ← A – (HL) – CY	x	x	x
	A, [HL+byte]	2	6	A, CY ← A – (HL + byte) – CY	x	x	x
AND	A, #byte	2	4	A ← A ∧ byte	x		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	x		
	A, r	2	4	A ← A ∧ r	x		
	A, saddr	2	4	A ← A ∧ (saddr)	x		
	A, !addr16	3	8	A ← A ∧ (addr16)	x		
	A, [HL]	1	6	A ← A ∧ (HL)	x		
	A, [HL+byte]	2	6	A ← A ∧ (HL + byte)	x		
OR	A, #byte	2	4	A ← A ∨ byte	x		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	x		
	A, r	2	4	A ← A ∨ r	x		
	A, saddr	2	4	A ← A ∨ (saddr)	x		
	A, !addr16	3	8	A ← A ∨ (addr16)	x		
	A, [HL]	1	6	A ← A ∨ (HL)	x		
	A, [HL+byte]	2	6	A ← A ∨ (HL + byte)	x		
XOR	A, #byte	2	4	A ← A $\overline{\vee}$ byte	x		
	saddr, #byte	3	6	(saddr) ← (saddr) $\overline{\vee}$ byte	x		
	A, r	2	4	A ← A $\overline{\vee}$ r	x		
	A, saddr	2	4	A ← A $\overline{\vee}$ (saddr)	x		
	A, !addr16	3	8	A ← A $\overline{\vee}$ (addr16)	x		
	A, [HL]	1	6	A ← A $\overline{\vee}$ (HL)	x		
	A, [HL+byte]	2	6	A ← A $\overline{\vee}$ (HL + byte)	x		

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

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Mnemonic	Operands	Byte	Clock	Operation	Flag		
					Z	AC	CY
CMP	A, #byte	2	4	A – byte	x	x	x
	saddr, #byte	3	6	(saddr) – byte	x	x	x
	A, r	2	4	A – r	x	x	x
	A, saddr	2	4	A – (saddr)	x	x	x
	A, !addr16	3	8	A – (addr16)	x	x	x
	A, [HL]	1	6	A – (HL)	x	x	x
	A, [HL+byte]	2	6	A – (HL + byte)	x	x	x
ADDW	AX, #word	3	6	AX, CY ← AX + word	x	x	x
SUBW	AX, #word	3	6	AX, CY ← AX – word	x	x	x
CMPW	AX, #word	3	6	AX – word	x	x	x
INC	r	2	4	r ← r + 1	x	x	
	saddr	2	4	(saddr) ← (saddr) + 1	x	x	
DEC	r	2	4	r ← r – 1	x	x	
	saddr	2	4	(saddr) ← (saddr) – 1	x	x	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1			x
ROL	A, 1	1	2	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1			x
RORC	A, 1	1	2	(CY ← A_0, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1			x
ROLC	A, 1	1	2	(CY ← A_7, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1			x
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	x	x	x
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	x	x	x
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			x

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

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Mnemonic	Operands	Byte	Clock	Operation	Flag
					Z AC CY
CALL	!addr16	3	6	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, $PC \leftarrow$ addr16, $SP \leftarrow SP-2$	
CALLT	[addr5]	1	8	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_H \leftarrow$ (00000000, addr5 + 1), $PC_L \leftarrow$ (00000000, addr5), $SP \leftarrow SP-2$	
RET		1	6	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, $SP \leftarrow SP+2$	
RETI		1	8	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, $PSW \leftarrow (SP+2)$, $SP \leftarrow SP+3$, NMIS $\leftarrow 0$	R R R
PUSH	PSW	1	2	$(SP-1) \leftarrow PSW$, $SP \leftarrow SP-1$	
	rp	1	4	$(SP-1) \leftarrow rp_H$, $(SP-2) \leftarrow rp_L$, $SP \leftarrow SP-2$	
POP	PSW	1	4	$PSW \leftarrow (SP)$, $SP \leftarrow SP+1$	R R R
	rp	1	6	$rp_H \leftarrow (SP+1)$, $rp_L \leftarrow (SP)$, $SP \leftarrow SP+2$	
MOVW	SP, AX	2	8	$SP \leftarrow AX$	
	AX, SP	2	6	$AX \leftarrow SP$	
BR	!addr16	3	6	$PC \leftarrow$ addr16	
	$addr16	2	6	$PC \leftarrow PC+2+$ jdisp8	
	AX	1	6	$PC_H \leftarrow A$, $PC_L \leftarrow X$	
BC	$saddr16	2	6	$PC \leftarrow PC+2+$ jdisp8 if CY = 1	
BNC	$saddr16	2	6	$PC \leftarrow PC+2+$ jdisp8 if CY = 0	
BZ	$saddr16	2	6	$PC \leftarrow PC+2+$ jdisp8 if Z = 1	
BNZ	$saddr16	2	6	$PC \leftarrow PC+2+$ jdisp8 if Z = 0	
BT	saddr.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if (saddr.bit) = 1	
	sfr.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if sfr.bit = 1	
	A.bit, $addr16	3	8	$PC \leftarrow PC+3+$ jdisp8 if A.bit = 1	
	PSW.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if PSW.bit = 1	
BF	saddr.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if (saddr.bit) = 0	
	sfr.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if sfr.bit = 0	
	A.bit, $addr16	3	8	$PC \leftarrow PC+3+$ jdisp8 if A.bit = 0	
	PSW.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if PSW.bit = 0	
DBNZ	B, $addr16	2	6	$B \leftarrow B-1$, then $PC \leftarrow PC+2+$ jdisp8 if $B \neq 0$	
	C, $addr16	2	6	$C \leftarrow C-1$, then $PC \leftarrow PC+2+$ jdisp8 if $C \neq 0$	
	saddr, $addr16	3	8	(saddr) $\leftarrow$ (saddr) -1, then $PC \leftarrow PC+3+$ jdisp8 if (saddr) $\neq 0$	
NOP		1	2	No Operation	
EI		3	6	IE $\leftarrow$ 1 (Enable interrupt)	
DI		3	6	IE $\leftarrow$ 0 (Disable interrupt)	
HALT		1	2	Set HALT mode	
STOP		1	2	Set STOP mode	

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

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17.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, INC, DEC, ROR, ROL, RORC, ROLC, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV[Note] XCH[Note] ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											
[HL+byte]		MOV											

Note Except r = A.

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(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	saddrp	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	
rp	MOVW	MOVW[Note]				INCW DECW PUSH POP
saddrp		MOVW				
SP		MOVW				

Note Only when rp = BC, DE, or HL.

(3) Bit manipulation instructions

SET1, CLR1, NOT1, BT, BF

1st Operand \ 2nd Operand	$addr16	None
A.bit	BT BF	SET1 CLR1
sfr.bit	BT BF	SET1 CLR1
saddr.bit	BT BF	SET1 CLR1
PSW.bit	BT BF	SET1 CLR1
[HL].bit		SET1 CLR1
CY		SET1 CLR1 NOT1

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(4) Call instructions/branch instructions

CALL, CALLT, BR, BC, BNC, BZ, BNZ, DBNZ

2nd Operand / 1st Operand	AX	!addr16	[addr5]	$addr16
Basic Instructions	BR	CALL BR	CALLT	BR BC BNC BZ BNZ
Compound Instructions				DBNZ

(5) Other instructions

RET, RETI, NOP, EI, DI, HALT, STOP

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CHAPTER 18 ELECTRICAL SPECIFICATIONS (μPD179322, 179322A, 179324, 179324A, 179326, AND 179327)

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
	V_{LC0}		–0.3 to +6.5	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3 Note	V
Output voltage	V_{O1}	P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61	–0.3 to V_{DD} + 0.3 Note	V
	V_{O2}	COM0 to COM3, S0 to S16, P80/S22 to P85/S17, S23	–0.3 to V_{LC0} + 0.3 Note	V
Output current, high	I_{OH}	Pin P60/TO40	–30	mA
		Per pin (except P60/TO40)	–10	mA
		Total for all pins (except P60/TO40)	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	80	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

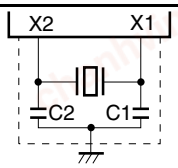
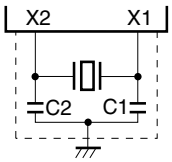
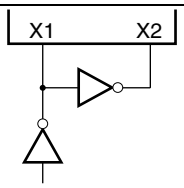
Note 6.5 V or less

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} has reached the oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2				30	ms
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use the resonator to stabilize oscillation within the oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

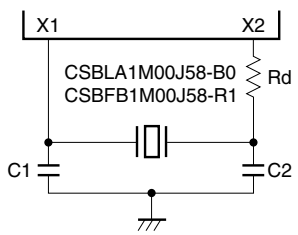
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Recommended Oscillation Circuit Constants

Ceramic oscillator (T_A = –40 to +85°C) (mask ROM version)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remark
			C1	C2	MIN.	MAX.	
Murata Mfg. (standard product)	CSBLA1M00J58-B0[Note]	1.0	100	100	1.9	3.6	Rd = 1.5 kΩ
	CSBFB1M00J58-R1[Note]						
	CSTCC2M00G56-R0	2.0	–	–			With internal capacitor
	CSTLS2M00G56-B0						
	CSTCR4M00G53-R0	4.0			1.8	3.6	
	CSTLS4M00G53-B0				1.9	3.6	
	CSTCR4M19G53-R0	4.194			1.8	3.6	
	CSTLS4M19G53-B0				1.9	3.6	
	CSTCR4M91G53-R0	4.915					
	CSTLS4M91G53-B0						
	CSTCR5M00G53-R0	5.0					
	CSTLS5M00G53-B0						
Murata Mfg. (low-voltage drive type)	CSTLS4M00G53093-B0	4.0	–	–	1.8	3.6	With internal capacitor
	CSTLS4M19G53093-B0	4.194					
	CSTCR4M91G53093-R0	4.915					
	CSTLS4M91G53093-B0						
	CSTCR5M00G53093-R0	5.0					
	CSTLS5M00G53093-B0						
TDK	FCR4.0MC5	4.0	–	–	2.2	3.6	With internal capacitor
	FCR5.0MC5	5.0					

Note When using the CSBLA1M00J58-B0 or CSBFB1M00J58-R1 (1.0 MHz) of Murata Mfg. as the ceramic oscillator, a limiting resistor (Rd = 1.5 kΩ) is necessary (refer to the figure below). The limiting resistor is not necessary when other recommended oscillators are used.

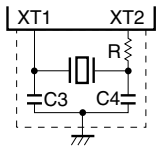
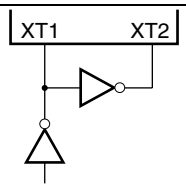


Caution The oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer.
If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.
The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the μPD179327 Subseries so that the internal operating conditions are within the specifications of the DC and AC characteristics.

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Remark For the resonator selection and oscillator constant of μPD179322A and 179324A, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2				10	s
External clock		XT1 input frequency (f_{XT}) Note 1		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. The time required for oscillation to stabilize after V_{DD} reaches the MIN. oscillation voltage range. Use a resonator to stabilize oscillation during the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Output current, high	I_{OH}	Per pin (except P60/TO40)				–1	mA
		P60/TO40	V_{DD} = 3.0 V, V_{OH} = 2.0 V	–7	–15	–24	mA
		Total for all pins (except P60/TO40)				–15	mA
Input voltage, high	V_{IH1}	P00 to P03, P10, P11, P60, P80 to P85	2.7 ≤ V_{DD} ≤ 3.6 V	0.7V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} ≤ 3.6 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P20 to P22, P40 to P43, P61	2.7 ≤ V_{DD} ≤ 3.6 V	0.8V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} ≤ 3.6 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.1		V_{DD}	V
	V_{IH4}	XT1, XT2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P03, P10, P11, P60, P80 to P85	2.7 ≤ V_{DD} ≤ 3.6 V	0		0.3V_{DD}	V
			1.8 ≤ V_{DD} ≤ 3.6 V	0		0.1V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$, P20 to P22, P40 to P43, P61	2.7 ≤ V_{DD} ≤ 3.6 V	0		0.2V_{DD}	V
			1.8 ≤ V_{DD} ≤ 3.6 V	0		0.1V_{DD}	V
	V_{IL3}	X1, X2		0		0.1	V
	V_{IL4}	XT1, XT2		0		0.1	V
Output voltage, high	V_{OH11}	P00 to P03, P10, P11, P20 to P22, P40 to P43, P61	1.8 ≤ V_{DD} ≤ 3.6 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
	V_{OH12}		1.8 ≤ V_{DD} ≤ 3.6 V, I_{OH} = –500 μA	V_{DD} – 0.7			V
	V_{OH21}	P60/TO40	1.8 ≤ V_{DD} ≤ 3.6 V, I_{OH} = –400 μA	V_{DD} – 0.5			V
	V_{OH22}		1.8 ≤ V_{DD} ≤ 3.6 V, I_{OH} = –2 mA	V_{DD} – 0.7			V
	V_{OH31}	P80/S22 to P85/S17	1.8 ≤ V_{DD} ≤ 3.6 V, I_{OH} = –100 μA	V_{LC0} – 0.5			V
	V_{OH32}		1.8 ≤ V_{DD} ≤ 3.6 V, I_{OH} = –500 μA	V_{LC0} – 0.7			V
Output voltage, low	V_{OL11}	P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61	1.8 ≤ V_{DD} ≤ 3.6 V, I_{OL} = 400 μA			0.5	V
	V_{OL12}		1.8 ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA			0.7	V
	V_{OL21}	P80/S22 to P85/S17	1.8 ≤ V_{LC0} ≤ 3.6 V, I_{OL} = 400 μA			0.5	V
	V_{OL22}		1.8 ≤ V_{LC0} ≤ 3.6 V, I_{OL} = 2 mA			0.7	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61, $\overline{\text{RESET}}$, P80 to P85			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61, $\overline{\text{RESET}}$, P80 to P85			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Software pull-up resistors	R_1	V_{IN} = 0 V	P00 to P03, P10, P11, P20 to P22, P40 to P43	50	100	200	kΩ
Supply current[Note 1]	I_{DD1}	5.0 MHz crystal oscillation operating mode	V_{DD} = 3.3 V[Note 2]		0.6	1.2	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode	V_{DD} = 3.3 V		0.4	0.8	mA
	I_{DD3}	32.768 kHz crystal oscillation HALT mode[Note 3]	V_{DD} = 3.3 V		7	25	μA
	I_{DD4}	32.768 kHz crystal oscillation stopped STOP mode (POC circuit used)	V_{DD} = 3.3 V		1	10	μA
	I_{DD5}	32.768 kHz crystal oscillation stopped STOP mode (POC circuit not used)	V_{DD} = 3.3 V		0.05	5	μA

Notes 1. Current flowing through ports (including current flowing through on-chip pull-up resistors and from V_{LC0} to V_{SS}) is not included.

2. Low-speed mode operation (when PCC is set to 02H)

3. When the main system clock operation is stopped.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

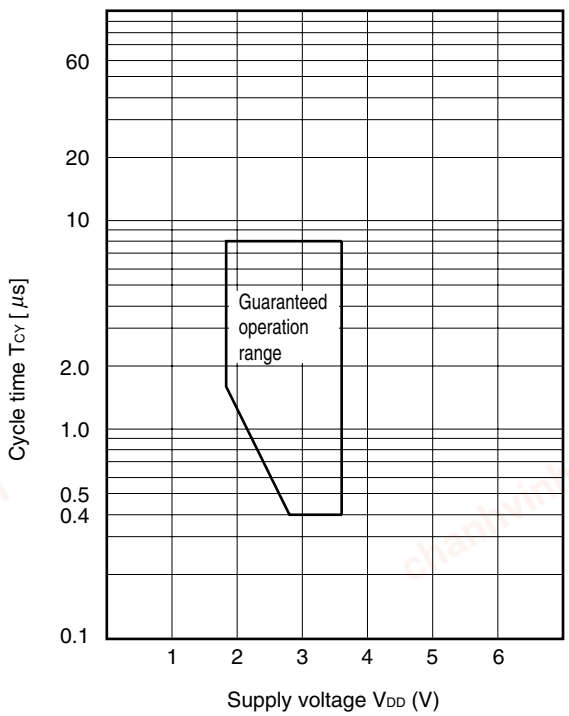
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AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

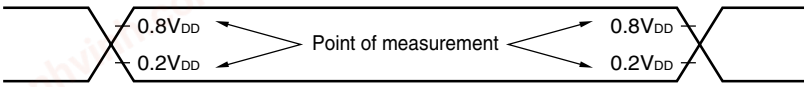
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	2.7 ≤ V_{DD} ≤ 3.6 V	0.4		8.0	μs
		1.8 ≤ V_{DD} ≤ 3.6 V	1.6		8.0	μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INT	10			μs
Key return pin low-level width	t_{KRIL}	KR00 to KR03	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD} (Main System Clock)

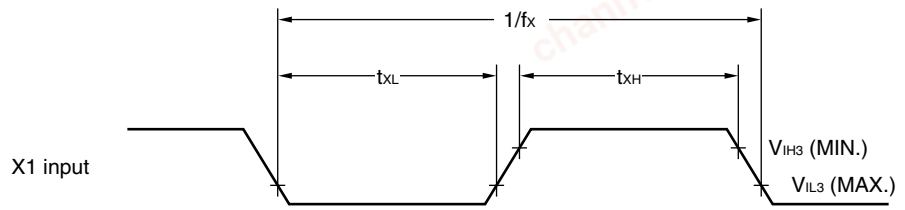


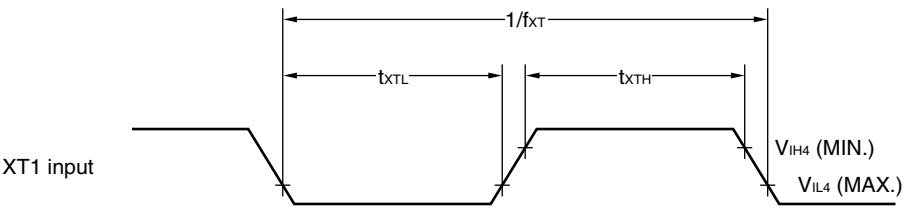
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AC Timing Measurement Points (Excluding X1, XT1 Input)

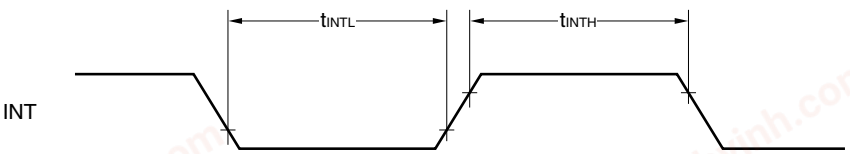


Clock Timing

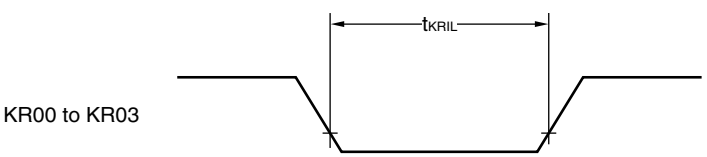




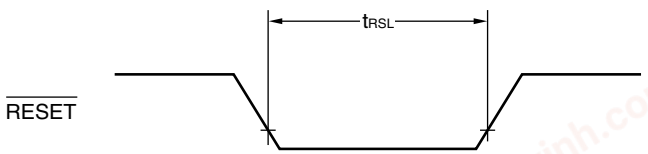
Interrupt Input Timing



Key Return Input Timing



$\overline{\text{RESET}}$ Input Timing



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LCD Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V, V_{LC0} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	VAON0[Note 1] = 1		1.8		V_{LC0}	V
		VAON0[Note 1] = 0		2.7		V_{LC0}	V
LCD division resistor	R_{LCD}			50	100	200	kΩ
LCD output voltage differential[Note 2] (common)	V_{ODC}	I_O = ±5 μA	1/3 bias	0		±0.2	V
LCD output voltage differential[Note 2] (segment)	V_{ODS}	I_O = ±1 μA	1/3 bias	0		±0.2	V

Notes 1. Bit 6 of LCD display mode register 0 (LCDM0).

2. The voltage differential is the difference between the output voltage and the ideal value of the segment and common signal outputs.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		3.6	V
Low voltage detection (POC) voltage	V_{POC}	Response time: 2 ms[Note 1]	1.8	1.9	2.0	V
Supply voltage rise time	t_{Pth}	V_{DD} : 0 V → 1.8 V	0.01		100	ms
Release signal set time	t_{SREL}	STOP released by $\overline{\text{RESET}}$	10			μs
Oscillation stabilization wait time[Note 2]	t_{WAIT}	Canceled by $\overline{\text{RESET}}$ pin or POC		**Note 3**		s
		Canceled by interrupt request		**Note 4**		s

Notes 1. The response time is the time until the output is inverted following detection of voltage by POC, or the time until operation stabilizes after the shift from the operation stopped state to the operating state.

2. The oscillation stabilization time is the amount of time the CPU operation is stopped in order to avoid unstable operation at the start of oscillation. Program operation does not start until both the oscillation stabilization time and the time until oscillation starts have elapsed.

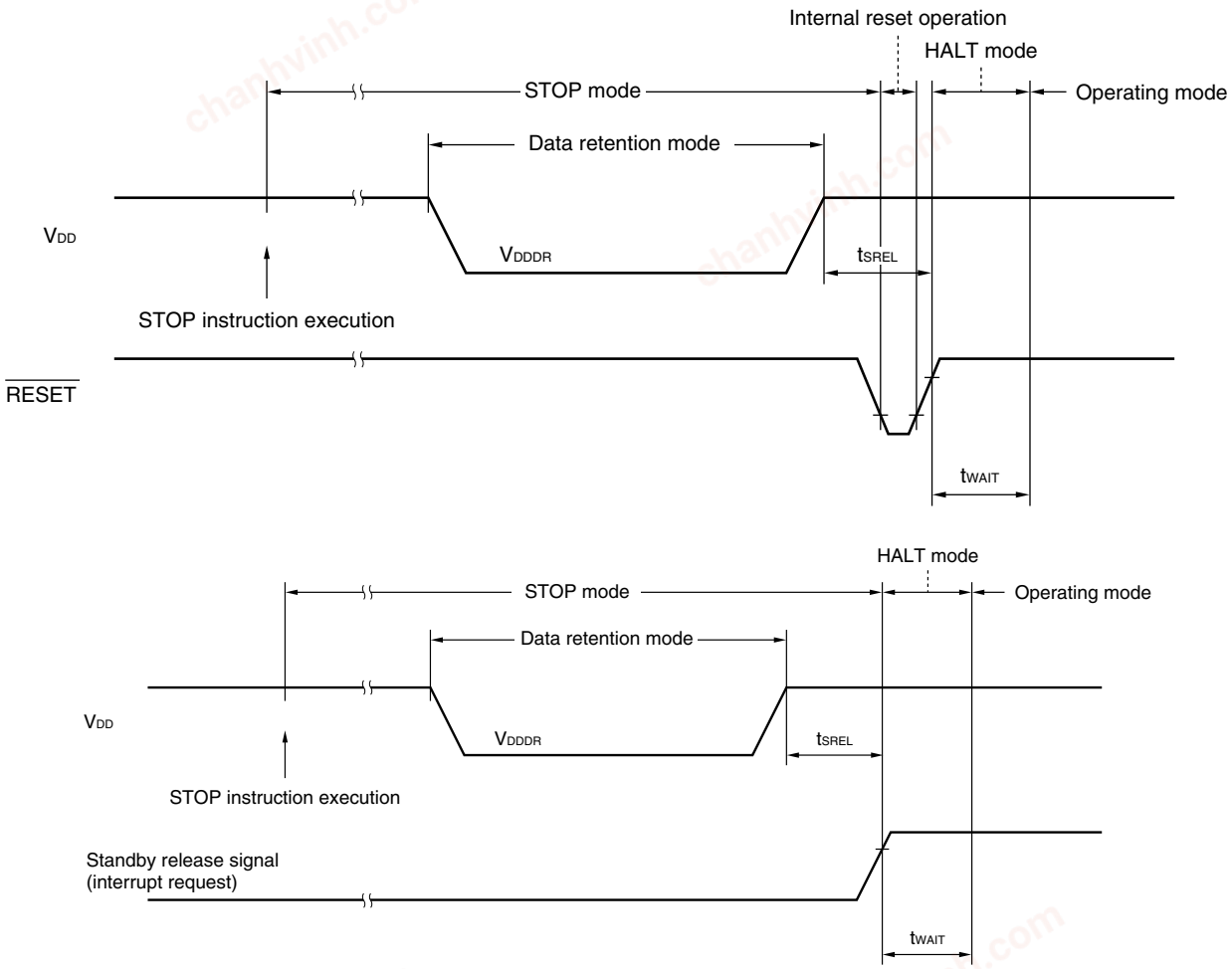
3. μPD78F9328 is fixed to 2^{15}/fx. In mask ROM versions, 2^{15}/fx or 2^{17}/fx is selected by a mask option (refer to **CHAPTER 16 MASK OPTIONS**).

4. Selection of 2^{12}/fx, 2^{15}/fx, and 2^{17}/fx is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS) (refer to **13.2 Register Controlling Standby Function**).

Remark fx: Main system clock oscillation frequency

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Data Retention Timing



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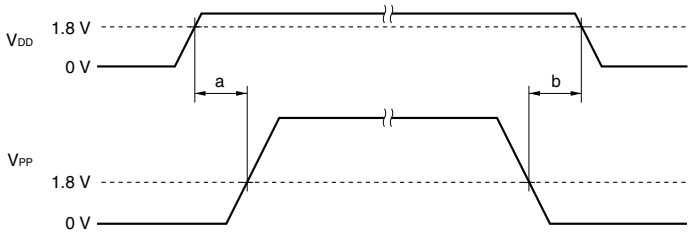
CHAPTER 19 ELECTRICAL SPECIFICATIONS (μPD78F9328)

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
	V_{LC0}		–0.3 to +6.5	V
	V_{PP}	**Note 1**	–0.3 to +10.5	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61	–0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	COM0 to COM3, S0 to S16, P80/S22 to P85/S17, S23	–0.3 to V_{LC0} + 0.3 Note 2	V
Output current, high	I_{OH}	Pin P60/TO40	–30	mA
		Per pin (except P60/TO40)	–10	mA
		Total for all pins (except P60/TO40)	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	80	mA
Operating ambient temperature	T_A	During normal operation	–40 to +85	°C
		During flash memory programming	10 to 40	°C
Storage temperature	T_{stg}	Flash memory version	–40 to +125	°C

Notes 1. Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- When supply voltage rises
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (a in the figure below).
- When supply voltage falls
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (1.8 V) of the range of V_{DD} (b in the figure below).



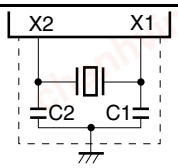
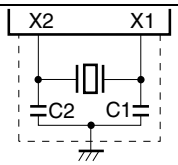
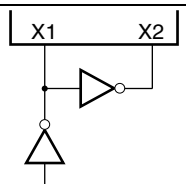
2. 6.5 V or less

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} has reached the oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequencyNote 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	4.5 ≤ V_{DD} ≤ 5.5 V			10	ms
			1.8 ≤ V_{DD} ≤ 5.5 V			30	ms
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use the resonator to stabilize oscillation within the oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

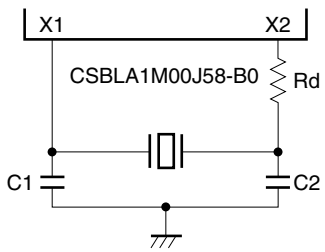
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Recommended Oscillation Circuit Constants

Ceramic oscillator (T_A = –40 to +85°C) (flash memory version)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remark
			C1	C2	MIN.	MAX.	
Murata Mfg. (standard product)	CSBLA1M00J58-B0[Note]	1.0	100	100	2.1	5.5	Rd = 3.3 kΩ
	CSTCC2M00G56-R0	2.0	–	–	1.8	5.5	With internal capacitor
	CSTCR4M00G53-R0	4.0					
	CSTLS4M00G53-B0						
	CSTCR4M19G53-R0	4.194					
	CSTLS4M19G53-B0						
	CSTCR4M91G53-R0	4.915					
	CSTLS4M91G53-B0						
	CSTCR5M00G53-R0	5.0					
	CSTLS5M00G53-B0						
TDK	FCR4.0MC5	4.0	–	–	2.2	5.5	With internal capacitor
	FCR5.0MC5	5.0					
Kyocera	PBRC4.00HR	4.0	–	–	1.8	5.5	With internal capacitor
	PBRC4.19HR	4.19					
	PBRC4.91HR	4.91					
	PBRC5.00HR	5.0					

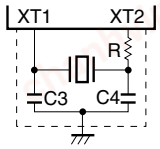
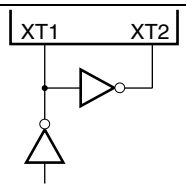
Note When using the CSBLA1M00J58-B0 of Murata Mfg. as the ceramic oscillator, a limiting resistor (Rd = 3.3 kΩ) is necessary (refer to the figure below). The limiting resistor is not necessary when other recommended oscillators are used.



Caution The oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer.
If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.
The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the μPD78F9328 so that the internal operating conditions are within the specifications of the DC and AC characteristics.

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Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	4.5 ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			1.8 ≤ V_{DD} ≤ 5.5 V			10	s
External clock		XT1 input frequency (f_{XT}) Note 1		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. The time required for oscillation to stabilize after V_{DD} reaches the MIN. oscillation voltage range. Use a resonator to stabilize oscillation during the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Output current, high	I_{OH}	Per pin (except P60/TO40)				–1	mA
		P60/TO40	V_{DD} = 3.0 V, V_{OH} = 2.0 V	–7	–15	–24	mA
		Total for all pins (except P60/TO40)				–15	mA
Input voltage, high	V_{IH1}	P00 to P03, P10, P11, P60, P80 to P85	2.7 ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} ≤ 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P20 to P22, P40 to P43, P61	2.7 ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} ≤ 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.1		V_{DD}	V
	V_{IH4}	XT1, XT2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P03, P10, P11, P60, P80 to P85	2.7 ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 ≤ V_{DD} ≤ 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$, P20 to P22, P40 to P43, P61	2.7 ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 ≤ V_{DD} ≤ 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	X1, X2		0		0.1	V
	V_{IL4}	XT1, XT2		0		0.1	V
Output voltage, high	V_{OH11}	P00 to P03, P10, P11, P20 to P22, P40 to P43, P61	1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
	V_{OH12}		1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –500 μA	V_{DD} – 0.7			V
	V_{OH21}	P60/TO40	1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –400 μA	V_{DD} – 0.5			V
	V_{OH22}		1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –2 mA	V_{DD} – 0.7			V
	V_{OH31}	P80/S22 to P85/S17	1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –100 μA	V_{LC0} – 0.5			V
	V_{OH32}		1.8 ≤ V_{DD} ≤ 5.5 V, I_{OH} = –500 μA	V_{LC0} – 0.7			V
Output voltage, low	V_{OL11}	P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61	1.8 ≤ V_{DD} ≤ 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL12}		1.8 ≤ V_{DD} ≤ 5.5 V, I_{OL} = 2 mA			0.7	V
	V_{OL21}	P80/S22 to P85/S17	1.8 ≤ V_{LC0} ≤ 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL22}		1.8 ≤ V_{LC0} ≤ 5.5 V, I_{OL} = 2 mA			0.7	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61, $\overline{\text{RESET}}$, P80 to P85			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10, P11, P20 to P22, P40 to P43, P60, P61, $\overline{\text{RESET}}$, P80 to P85			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Software pull-up resistors	R_1	V_{IN} = 0 V	P00 to P03, P10, P11, P20 to P22, P40 to P43	50	100	200	kΩ
Supply current[Note 1]	I_{DD1}	5.0 MHz crystal oscillation operating mode	V_{DD} = 5.5 V[Note 2]		5.0	15.0	mA
			V_{DD} = 3.3 V[Note 3]		2.0	5.0	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode	V_{DD} = 5.5 V		1.2	3.6	mA
			V_{DD} = 3.3 V		0.5	1.5	mA
	I_{DD3}	32.768 kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.5 V		25	70	μA
			V_{DD} = 3.3 V		10	35	μA
	I_{DD4}	32.768 kHz crystal oscillation stopped STOP mode	V_{DD} = 5.5 V		2	20	μA
			V_{DD} = 3.3 V		1	10	μA

Notes 1. Current flowing through ports (including current flowing through on-chip pull-up resistors and from V_{LC0} to V_{SS}) is not included.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

3. Low-speed mode operation (when PCC is set to 02H)

4. When the main system clock operation is stopped.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

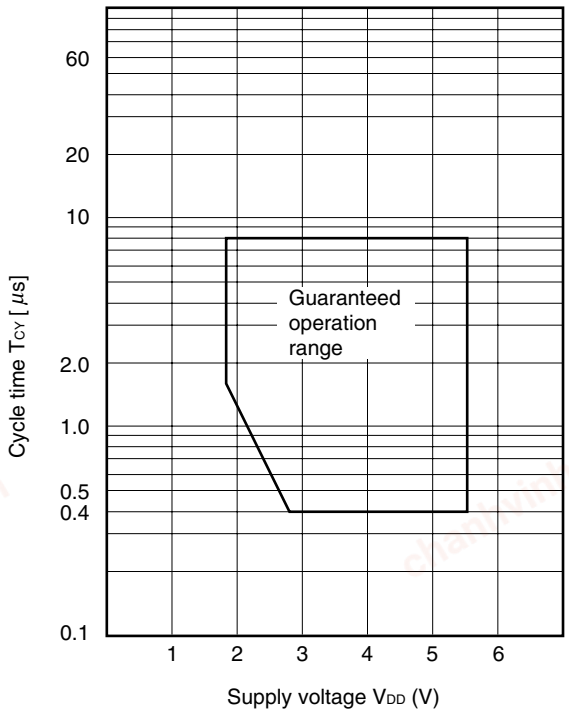
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AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	2.7 ≤ V_{DD} ≤ 5.5 V	0.4		8.0	μs
		1.8 ≤ V_{DD} ≤ 5.5 V	1.6		8.0	μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INT	10			μs
Key return pin low-level width	t_{KRIL}	KR00 to KR03	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

T_{CY} vs. V_{DD} (Main System Clock)



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(2) Serial Interface 10 (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode (internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK10}$ high/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2-50			ns
		V_{DD} = 1.8 to 5.5 V		t_{KCY1}/2-150			ns
SI10 setup time (to $\overline{SCK10}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI10 hold time (from $\overline{SCK10}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		800			ns
Delay time from $\overline{SCK10}$↓ to SO10 output	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	250		1000	ns

Note R and C are the load resistance and load capacitance of the SO10 output line.

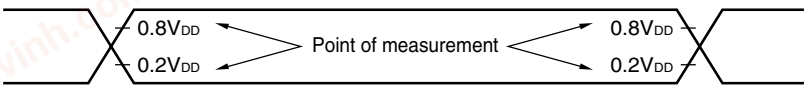
(a) 3-wire serial I/O mode (external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK10}$ high/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI10 setup time (to $\overline{SCK10}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI10 hold time (from $\overline{SCK10}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
Delay time from $\overline{SCK10}$↓ to SO10 output	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	250		1000	ns

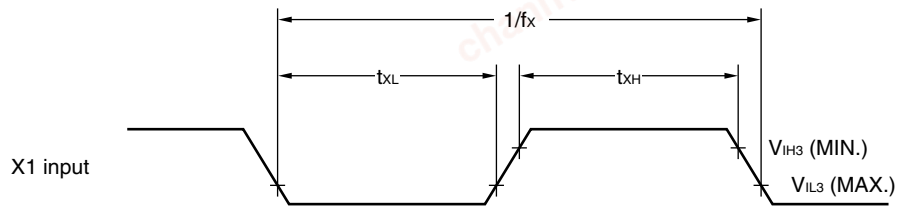
Note R and C are the load resistance and load capacitance of the SO10 output line.

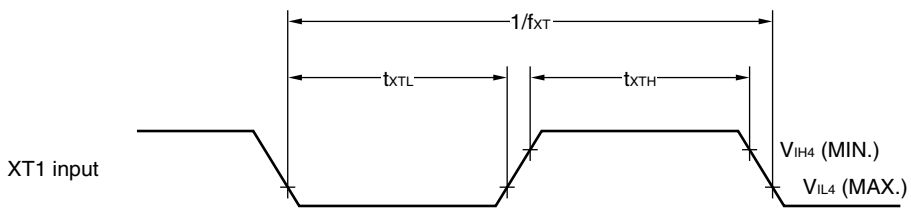
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AC Timing Measurement Points (Excluding X1, XT1 Input)

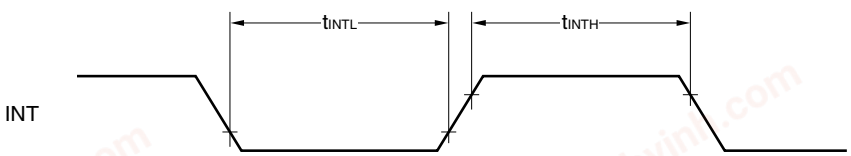


Clock Timing

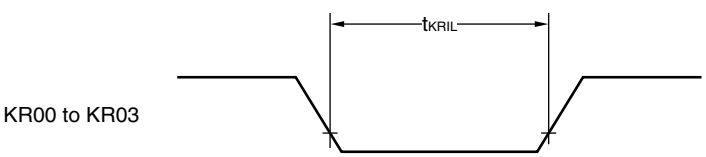




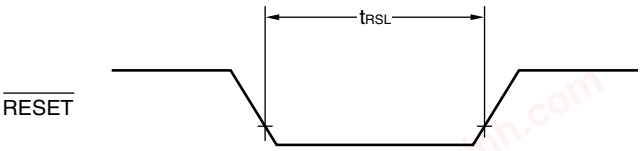
Interrupt Input Timing



Key Return Input Timing



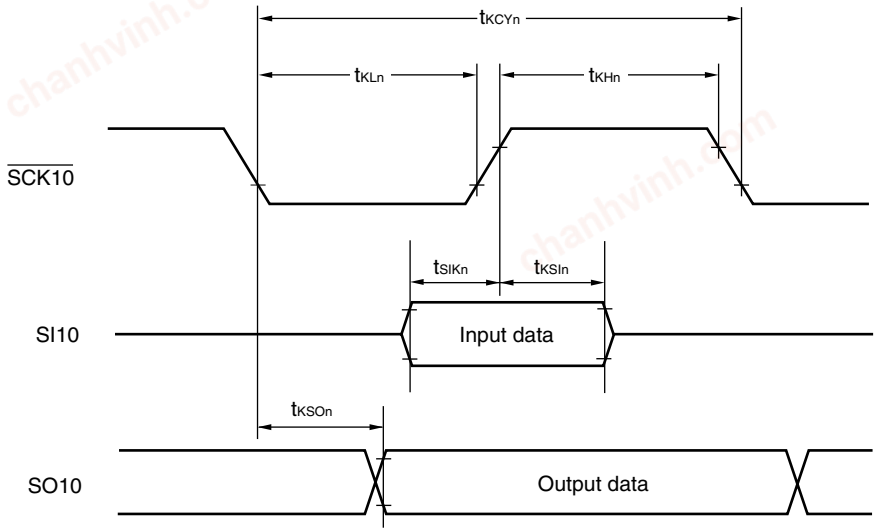
$\overline{\text{RESET}}$ Input Timing



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Serial Transfer Timing

3-wire serial I/O mode:



Remark n = 1, 2

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LCD Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V, V_{LC0} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	VAON0[Note 1] = 1		1.8		V_{LC0}	V
		VAON0[Note 1] = 0		2.7		V_{LC0}	V
LCD division resistor	R_{LCD}			50	100	200	kΩ
LCD output voltage differential[Note 2] (common)	V_{ODC}	I_O = ±5 μA	1/3 bias	0		±0.2	V
LCD output voltage differential[Note 2] (segment)	V_{ODS}	I_O = ±1 μA	1/3 bias	0		±0.2	V

Notes 1. Bit 6 of LCD display mode register 0 (LCDM0).

2. The voltage differential is the difference between the output voltage and the ideal value of the segment and common signal outputs.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Low voltage detection (POC) voltage	V_{POC}	Response time: 2 ms[Note 1]	1.8	1.9	2.0	V
Supply voltage rise time	t_{Pth}	V_{DD} : 0 V → 1.8 V	0.01		100	ms
Release signal set time	t_{SREL}	STOP released by $\overline{\text{RESET}}$	10			μs
Oscillation stabilization wait time[Note 2]	t_{WAIT}	Canceled by $\overline{\text{RESET}}$ pin or POC		2^{15}/fx		s
		Canceled by interrupt request		**Note 3**		s

Notes 1. The response time is the time until the output is inverted following detection of voltage by POC, or the time until operation stabilizes after the shift from the operation stopped state to the operating state.

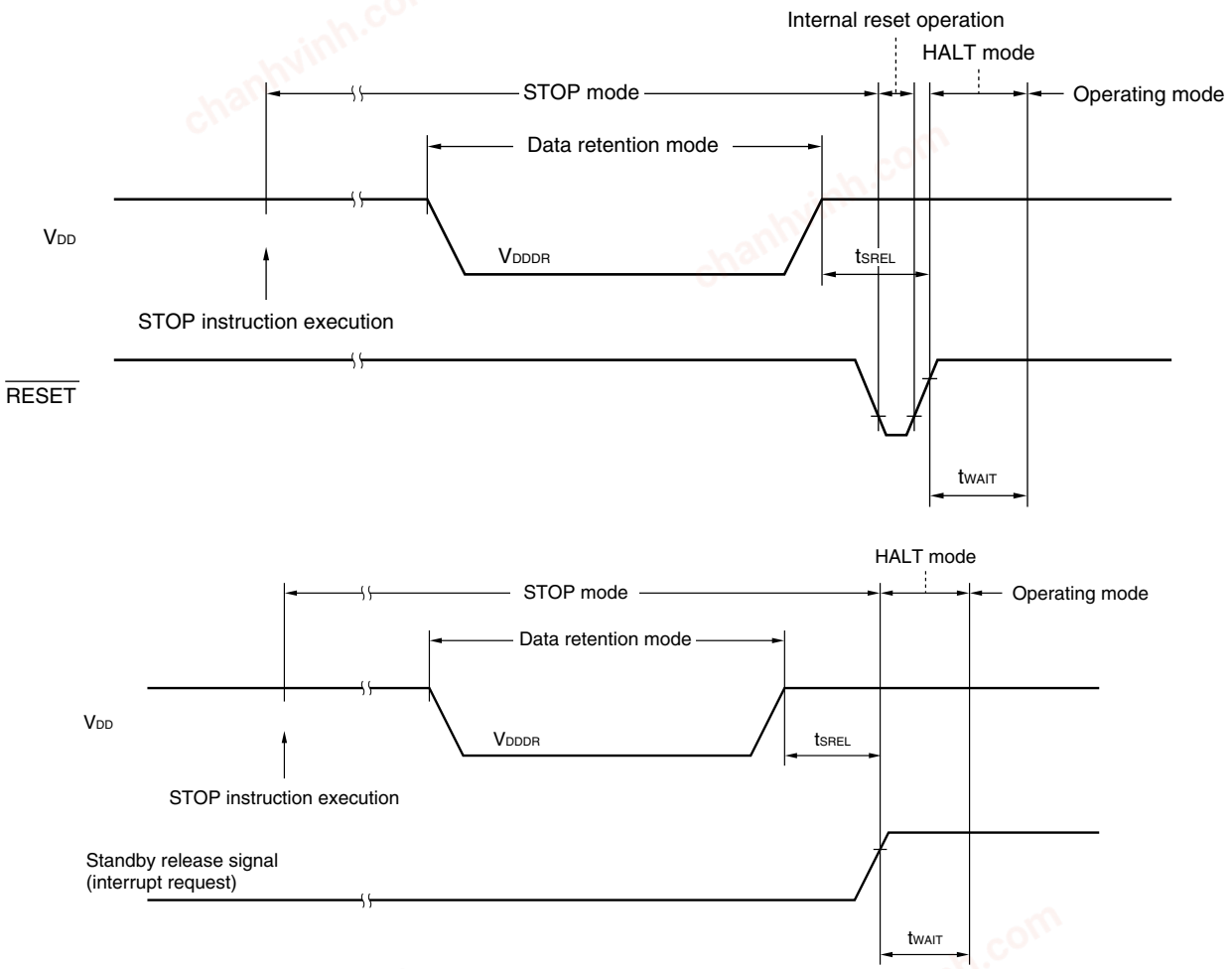
2. The oscillation stabilization time is the amount of time the CPU operation is stopped in order to avoid unstable operation at the start of oscillation. Program operation does not start until both the oscillation stabilization time and the time until oscillation starts have elapsed.

3. Selection of 2^{12}/fx, 2^{15}/fx, and 2^{17}/fx is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS) (refer to **13.2 Register Controlling Standby Function**).

Remark fx: Main system clock oscillation frequency

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Data Retention Timing



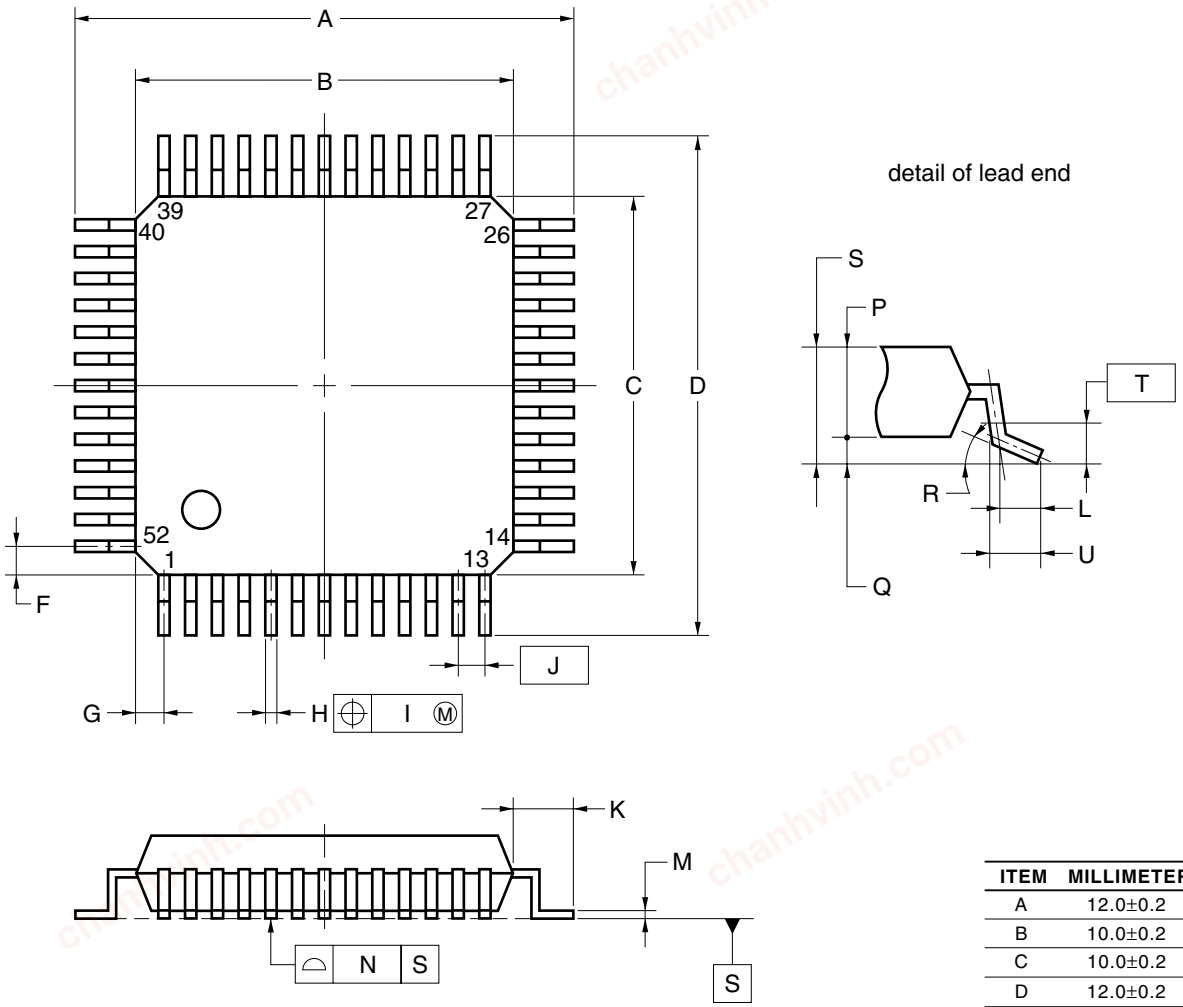
Writing and Erasing Characteristics (T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write operation frequency	f_X	V_{DD} = 2.7 to 5.5 V	1.0		5	MHz
		V_{DD} = 1.8 to 5.5 V	1.0		1.25	MHz
Write current (V_{DD} pin)[Note]	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (at 5.0 MHz operation)			7	mA
Write current (V_{PP} pin)[Note]	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			13	mA
Erase current (V_{DD} pin)[Note]	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (at 5.0 MHz operation)			7	mA
Erase current (V_{PP} pin)[Note]	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			100	mA
Unit erase time	t_{er}		0.5	1	1	s
Total erase time	t_{era}				20	s
Number of overwrites		Erase and write is considered as 1 cycle			20	Times
V_{PP} supply voltage	V_{PP0}	Normal operation	0		0.2V_{DD}	V
	V_{PP1}	Flash memory programming	9.7	10.0	10.3	V

Note Excludes current flowing through ports (including on-chip pull-up resistors)

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52-PIN PLASTIC LQFP (10x10)



ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.1
G	1.1
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.05}$
N	0.10
P	1.4
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1
T	0.25
U	0.6±0.15

S52GB-65-8ET-2

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CHAPTER 21 RECOMMENDED SOLDERING CONDITIONS

The μPD179322, 179322A, 179324, 179324A, 179326, 179327, and 78F9328 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 21-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD179322GB-×××-8ET, 179322AGB-×××-8ET

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 350°C max. Time: 3 seconds max. (per pin row)	—

(2) μPD179324GB-××× -8ET, 179324AGB-×××-8ET, 179326GB-××× -8ET, 179327GB-××× -8ET

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-103-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-103-1
Partial heating	Pin temperature: 350°C max. Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

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Table 21-1. Surface Mounting Type Soldering Conditions (2/2)

(3) μPD78F9328GB-8ET

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 350°C max. Time: 3 seconds max. (per pin row)	—

(4) μPD179322GB-8ET-A, 179322AGB-8ET-A, 179324GB-8ET-A, 179324AGB-8ET-A, 179326GB-8ET-A, 179327GB-8ET-A, 78F9328GB-8ET-A

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Wave soldering	For details, contact an NEC Electronics sales representative.	–
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remark Products that have the part numbers suffixed by "-A" are lead-free products.

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APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μPD179327 Subseries. Figure A-1 shows development tools.

- Support of PC98-NX series

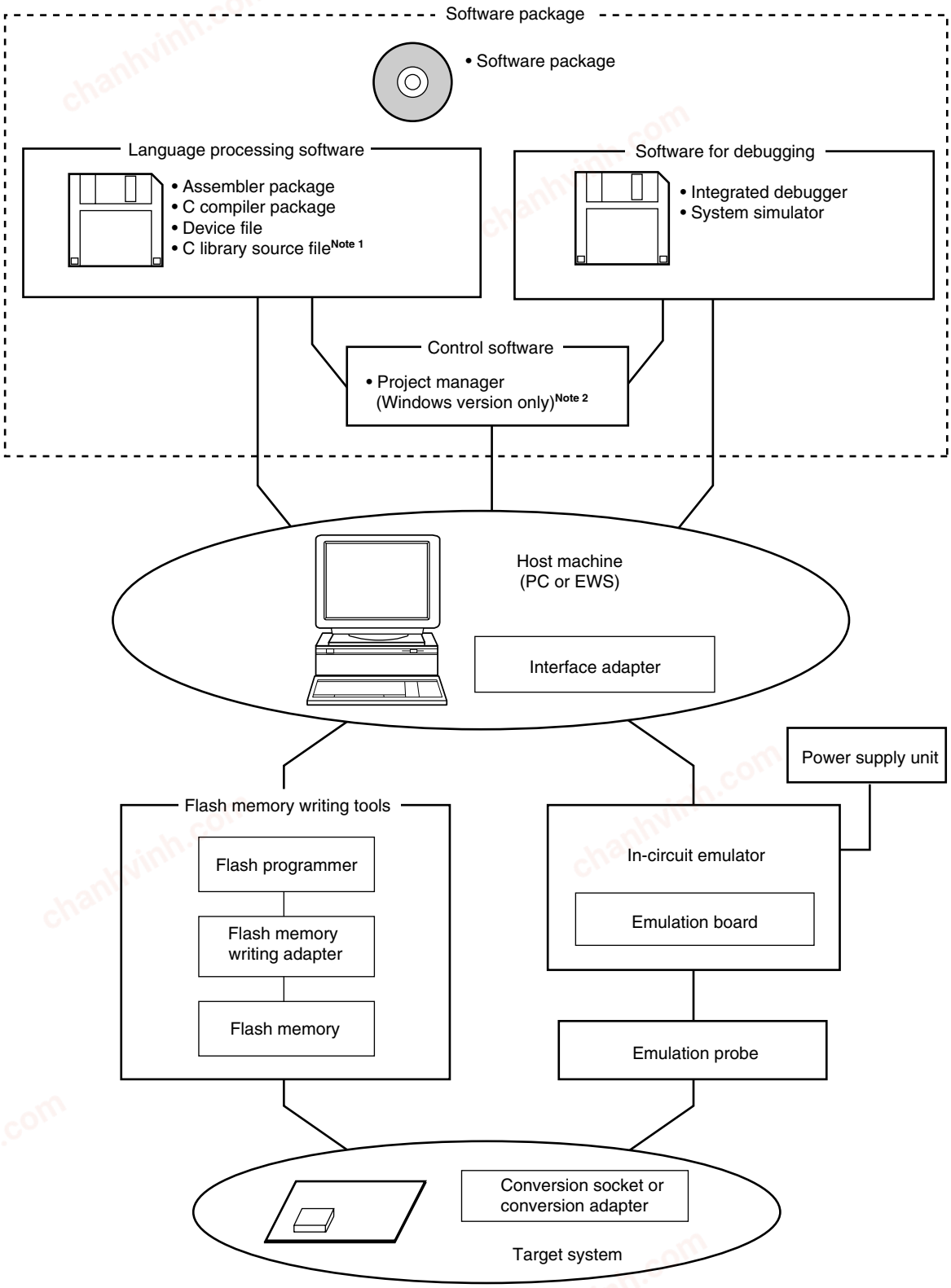
  Unless specified otherwise, the products supported by IBM PC/AT™ compatibles can be used in the PC98-NX series. When using the PC98-NX Series, refer to the explanation of IBM PC/AT compatibles.

- Windows™

  Unless specified otherwise, "Windows" indicates the following operating systems.
  - Windows 98
  - Windows 2000
  - Windows NT™ Ver.4.0
  - Windows XP

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Figure A-1. Development Tools



Notes 1. The C library source file is not included in the software package.

2. The project manager is included in the assembler package. The project manager is used only for Windows.

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A.1 Software Package

SP78K0S Software package	Various software tools for 78K/0S Series development are integrated into one package. The following tools are included. RA78K0S, CC78K0S, ID78K0S-NS, SM78K0S, various device files
	Part number: μS××××SP78K0S

Remark ×××× in the part number differs depending on the operating system to be used.

μS××××SP78K0S

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Japanese Windows	CD-ROM
BB17		English Windows	

A.2 Language Processing Software

RA78K0S Assembler package	Program that converts program written in mnemonic into object codes that can be executed by microcontroller. In addition, automatic functions to generate symbol tables and optimize branch instructions are also provided. Used in combination with a device file (DF179327) (sold separately). **<Caution when used in PC environment>** The assembler package is a DOS-based application but may be used in the Windows environment by using the Project Manager of Windows (included in the assembler package).
	Part number: μS××××RA78K0S
CC78K0S C compiler package	Program that converts program written in C language into object codes that can be executed by microcontroller. Used in combination with an assembler package (RA78K0S) and device file (DF179327) (both sold separately). **<Caution when used in PC environment>** The C compiler package is a DOS-based application but may be used in the Windows environment by using the Project Manager of Windows (included in the assembler package).
	Part number: μS××××CC78K0S
DF179327[Note1] Device file	File containing the information specific to the device. Used in combination with the RA78K0S, CC78K0S, and SM78K0S (sold separately).
	Part number: μS××××DF179327
CC78K0S-L[Note2] C library source file	Source file of functions for generating object library included in C compiler package. Necessary for changing object library included in C compiler package according to customer's specifications. Since this is a source file, its working environment does not depend on any particular operating system.
	Part number: μS××××CC78K0S-L

Notes 1. DF179327 is a common file that can be used with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S.

2. CC78K0S-L is not included in the software package (SP78K0S).

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Remark ××××in the part number differs depending on the host machine and operating system to be used.

μS××××RA78K0S
μS××××CC78K0S

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatibles	Japanese Windows	3.5” 2HD FD
BB13		English Windows	
AB17		Japanese Windows	CD-ROM
BB17		English Windows	
3P17	HP9000 series 700™	HP-UX™ (Rel.10.10)	
3K17	SPARCstation™	SunOS™ (Rel.4.1.4), Solaris™ (Rel.2.5.1)	

μS××××DF179327
μS××××CC78K0S-L

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatibles	Japanese Windows	3.5” 2HD FD
BB13		English Windows	
3P16	HP9000 series 700	HP-UX (Rel.10.10)	DAT
3K13	SPARCstation	SunOS (Rel.4.1.4), Solaris (Rel.2.5.1)	3.5” 2HD FD
3K15			1/4” CGMT

A.3 Control Software

Project manager	Control software designed so that the user program can be efficiently developed in the Windows environment. A series of jobs for user program development including starting the editor, building, and starting the debugger, can be executed on the project manager. <Caution> The project manager is included in the assembler package (RA78K0S). It cannot be used in an environment other than Windows.

A.4 Flash Memory Writing Tools

Flashpro IV (Part No. FL-PR4, PG-FP4) Flash programmer	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-52GB-8ET Flash memory writing adapter	Adapter for writing to flash memory and connected to Flashpro III or Flashpro IV. FA-52GB-8ET: for 52-pin plastic LQFP (GB-8ET type)

Remark The FL-PR4, and FA-52GB-8ET are products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

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A.5 Debugging Tools (Hardware)

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging hardware and software of application system using 78K/0S Series. Supports integrated debugger (ID78K0S-NS). Used in combination with AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-78K0S-NS-A In-circuit emulator	A coverage function has been added to the IE-78K0S-NS function and the debug function has been further enhanced, enhancing the tracer and timer functions.
IE-70000-MC-PS-B AC adapter	Adapter for supplying power from AC 100 to 240 V outlet.
IE-70000-98-IF-C Interface adapter	Adapter necessary when using PC-9800 series PC (except notebook type) as host machine (C bus supported)
IE-70000-CD-IF-A PC card interface	PC card and interface cable necessary when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter	Interface adapter necessary when using IBM PC/AT compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A Interface adapter	Adapter necessary when using personal computer incorporating PCI bus as host machine
IE-789468-NS-EM1 Emulation board	Board for emulating peripheral hardware specific to device. Used in combination with in-circuit emulator.
NP-H52GB-TQ Emulation probe	Probe for connecting in-circuit emulator and target system. Used in combination with TGB-052SBP.
TGB-052SBP Conversion adapter	Conversion adapter to connect NP-H52GB-TQ and target system board on which 52-pin plastic LQFP (GB-8ET type) can be mounted

Remarks 1. The NP-H52GB-TQ is a product made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

2. The TGB-052SBP is a product made by TOKYO ELETECH CORPORATION.
For further information, contact: Daimaru Kogyo, Ltd.
Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)

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A.6 Debugging Tools (Software)

ID78K0S-NS Integrated debugger	A debugger supporting in-circuit emulators for the 78K/0S Series: IE-78K0S-NS and IE-78K0S-NS-A. The ID78K0S-NS is Windows-based software. This program enhances the debugging functions for C language. Therefore, it can display the trace results corresponding to the source program by using the window integration function that links the source program, disassembled display, and memory display with the trace results. Use this program in combination with a device file (DF179327) (sold separately).
	Part number: μS××××ID78K0S-NS
SM78K0S System simulator	A system simulator for the 78K/0S Series. The SM78K0S is Windows-based software. C-source-level or assembler level debugging is possible while simulating the operation of the target system on the host machine. Using the SM78K0S enables logical and performance verification of an application independently of the hardware development. This enhances development efficiency and improves software quality. Use this program in combination with a device file (DF179327) (sold separately).
	Part number: μS××××SM78K0S
DF179327[Note] Device file	File containing information specific to the device. Use this file in combination with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S (sold separately).
	Part number: μS××××DF179327

Note DF179327 is a common file that can be used with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S.

Remark ×××× in the part number differs depending on the operating system to be used and the supply medium.

μS××××ID78K0S-NS
μS××××SM78K0S

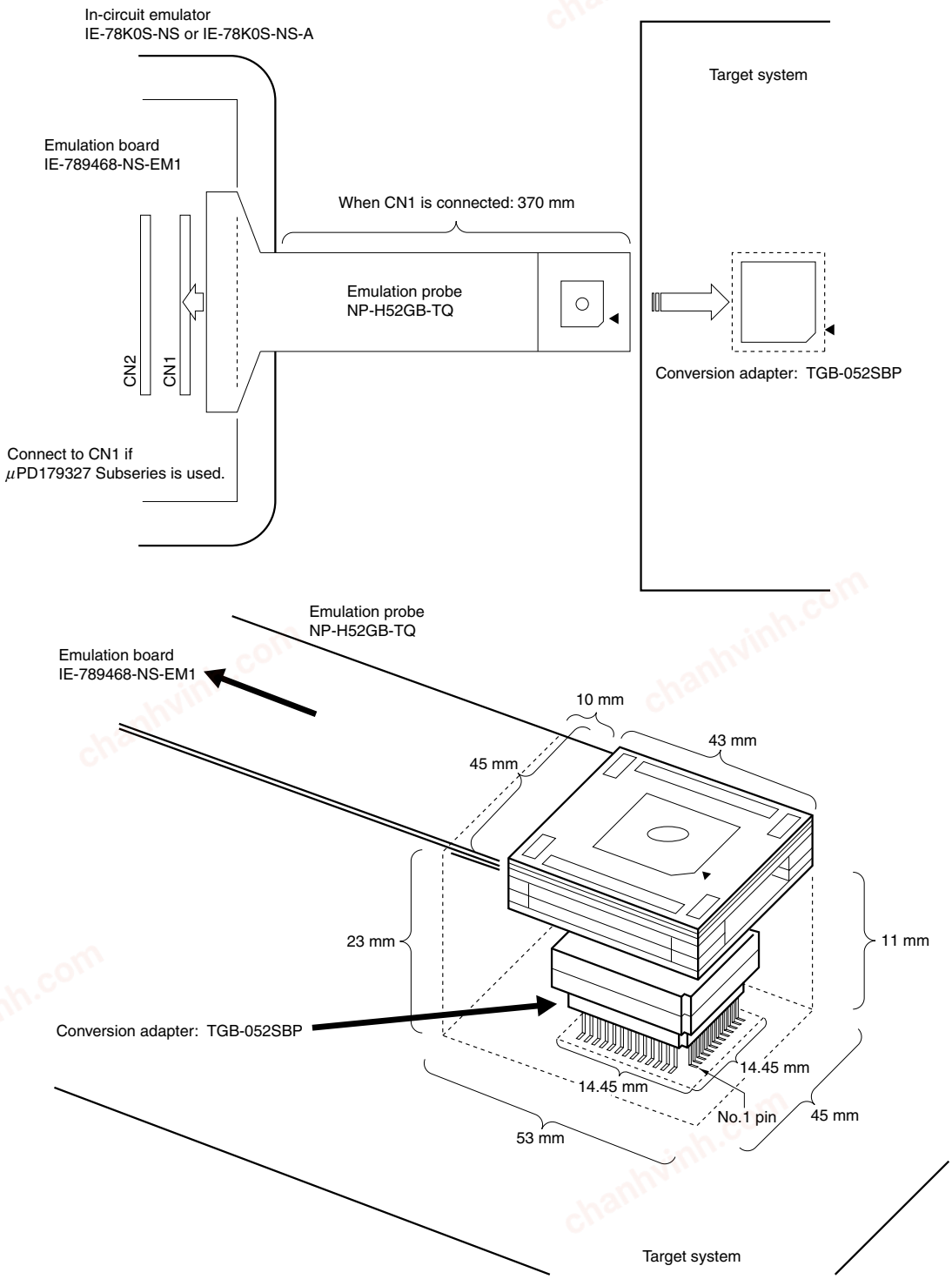
××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT compatibles	Japanese Windows	3.5” 2HD FD
BB13		English Windows	
AB17		Japanese Windows	CD-ROM
BB17		English Windows	

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A.7 Cautions when designing target system

The following shows the conditions when connecting the emulation probe to the conversion adapter. Design the system considering shapes and other conditions of the components to be mounted on the target system and be sure to follow the configuration below.

Figure A-2. Condition Diagram of Connection to Target System



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APPENDIX B REGISTER INDEX

B.1 Register Index (Alphabetic Order of Register Name)

[C]

Carrier generator output control register 40 (TCA40) 93

[E]

8-bit compare register 30 (CR30) 88
8-bit compare register 40 (CR40) 88
8-bit H width compare register 40 (CRH40) 88
8-bit timer counter 30 (TM30) 89
8-bit timer counter 40 (TM40) 89
8-bit timer mode control register 30 (TMC30) 91
8-bit timer mode control register 40 (TMC40) 92
External interrupt mode register 0 (INTM0) 156

[I]

Interrupt mask flag register 0 (MK0) 155
Interrupt request flag register 0 (IF0) 154

[K]

Key return mode register 00 (KRM00) 157

[L]

LCD clock control register 0 (LCDC0) 136
LCD display mode register 0 (LCDM0) 134

[O]

Oscillation stabilization time selection register (OSTS) 165

[P]

Port 0 (P0) 59
Port 1 (P1) 60
Port 2 (P2) 61
Port 4 (P4) 64
Port 6 (P6) 65
Port 8 (P8) 67
Port function register 8 (PF8) 70, 137
Port mode register 0 (PM0) 68
Port mode register 1 (PM1) 68
Port mode register 2 (PM2) 68, 128
Port mode register 4 (PM4) 68
Port mode register 6 (PM6) 68, 94
Port mode register 8 (PM8) 68

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Power-on-clear register 1 (POCF1) 150
Processor clock control register (PCC) 75
Pull-up resistor option register 0 (PU0) 69
Pull-up resistor option register B2 (PUB2) 70

[S]

Serial operation mode register 10 (CSIM10) 127
Subclock control register (CSS) 76
Suboscillation mode register (SCKM) 76

[T]

Transmit/receive shift register 10 (SIO10) 125

[W]

Watchdog timer clock selection register (TCL2) 120
Watchdog timer mode register (WDTM) 121
Watch timer mode control register (WTM) 115

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B.2 Register Index (Alphabetic Order of Register Symbol)

[C]

CR30: 8-bit compare register 30 88
CR40: 8-bit compare register 40 88
CRH40: 8-bit H width compare register 40 88
CSIM10: Serial operation mode register 10 127
CSS: Subclock control register 76

[I]

IF0: Interrupt request flag register 0 154
INTM0: External interrupt mode register 0 156

[K]

KRM00: Key return mode register 00 157

[L]

LCDC0: LCD clock control register 0 136
LCDM0: LCD display mode register 0 134

[M]

MK0: Interrupt mask flag register 0 155

[O]

OSTS: Oscillation stabilization time selection register 165

[P]

P0: Port 0 59
P1: Port 1 60
P2: Port 2 61
P4: Port 4 64
P6: Port 6 65
P8: Port 8 67
PCC: Processor clock control register 75
PF8: Port function register 8 ..... 70, 137
PM0: Port mode register 0 68
PM1: Port mode register 1 68
PM2: Port mode register 2 ..... 68, 128
PM4: Port mode register 4 68
PM6: Port mode register 6 ..... 68, 94
PM8: Port mode register 8 68
POCF1: Power-on-clear register 1 150
PU0: Pull-up resistor option register 0 69
PUB2: Pull-up resistor option register B2 70

[S]

SCKM: Suboscillation mode register 76
SIO10: Transmit/receive shift register 10 125

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[T]

TCA40: Carrier generator output control register 40 93
TCL2: Watchdog timer clock selection register 120
TM30: 8-bit timer counter 30 89
TM40: 8-bit timer counter 40 89
TMC30: 8-bit timer mode control register 30 91
TMC40: 8-bit timer mode control register 40 92

[W]

WDTM: Watchdog timer mode register 121
WTM: Watch timer mode control register 115

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APPENDIX C REVISION HISTORY

C.1 Major Revisions in This Edition

Page	Description
Throughout	Addition of μPD179322A and 179324A
p. 231	Addition of **C.2 Revision History of Preceding Editions**

<R>

C.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

Page	Description
p. 15	Addition of lead-free products to **1.3 Ordering Information**
p. 218	Addition of lead-free products to **CHAPTER 21 RECOMMENDED SOLDERING CONDITIONS**

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