chanhvinh.com

CEL

BIPOLAR ANALOG INTEGRATED CIRCUIT

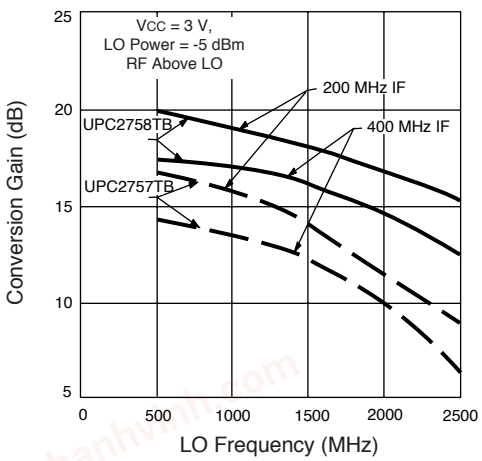
UPC2757TB / UPC2758TB

3 V, SUPER MINIMOLD SI MMIC DOWNCONVERTER

FEATURES

- **HIGH-DENSITY SURFACE MOUNTING:** 6 pin super minimold or SOT-363 package
- **WIDEBAND OPERATION:** RF = 0.1 GHz to 2.0 GHz, IF = 20 MHz to 300 MHz
- **BUILT-IN POWER SAVE FUNCTION**
- **SUPPLY VOLTAGE:** V_{CC} = 2.7 TO 3.3 V

CONVERSION GAIN vs. LO FREQUENCY



DESCRIPTION

The UPC2757TB and UPC2758TB are silicon RFICs manufactured using the NESAT™III process. The devices consist of a mixer, an IF amplifier and an LO buffer amplifier. These devices are suitable as 1st IF downconverters for the receiver stage of cellular and other wireless systems. The UPC2757TB is designed for low power consumption while the UPC2758TB is designed for low distortion. The UPC2757TB/58TB are pin compatible and have comparable performance to the larger UPC2757T/58T, so they are suitable for use as a replacement to help reduce system size. The IC is housed in a 6 pin super minimold or SOT-363 package.

Stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = V_{PS} = 3.0 V, P_{LO} = -10 dBm)

PART NUMBER / PACKAGE OUTLINE			UPC2757TB S06			UPC2758TB S06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX
I_{CC}	Circuit Current, V_{PS} = 3 V	mA	3.7	5.6	7.7	6.6	11	14.8
	V_{PS} = 0.5 V	μA		0.1			0.1	
f_{RF}	RF Operating Frequency Range (The conversion gain at f_{RF} is not more than 3 dB down from the gain at f_{RF} = 800 MHz, f_{IF} = 130 MHz)	GHz	0.1		2.0	0.1		2.0
f_{IF}	IF Operating Frequency Range (The conversion gain at f_{IF} is not more than 3 dB down from the gain at f_{RF} = 800 MHz, f_{IF} = 130 MHz)	MHz	20		300	20		300
CG	Conversion Gain[1], f_{RF} = 800 MHz, f_{IF} = 130 MHz	dB	12	15	18	16	19	22
	f_{RF} = 2.0 GHz, f_{IF} = 250 MHz	dB	10	13	16	14	17	20
NF	Noise Figure, SSB f_{RF} = 800 MHz, f_{IF} = 130 MHz	dB		10	13		9	12
	f_{RF} = 2.0 GHz, f_{IF} = 250 MHz	dB		13	16		13	15
P_{SAT}	Saturated Output Power[2], f_{RF} = 800 MHz, f_{IF} = 100 MHz	dBm	-11	-3		-7	+1	
	f_{RF} = 2.0 GHz, f_{IF} = 250 MHz	dBm	-11	-8		-7	-4	
P_{1dB}	Output Power at 1dB compression point f_{RF} = 800 MHz, f_{IF} = 100 MHz	dBm		-8			-3.5	
OIP_3	Output 3rd Order Intercept Point, (SSB) P_{LO} = -10 dBm, f_{RF} = 0.8~2.0 GHz, f_{IF} = 100 MHz	dBm		+5			+11	
ISOL	LO Leakage, f_{LO} = 0.8 ~2.0 GHz at RF pin	dBm		-35			-30	
	at IF pin	dBm		-23			-15	
$R_{TH\ (J-A)}$	Thermal Resistance (Junction to Ambient) Mounted on a 50 x 50 x 1.6 mm epoxy glass PWB	°C/W			325			325

Notes:
1. P_{RF} = -40 dBm. 2. P_{RF} = -10 dBm.

chanhvinh.com

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

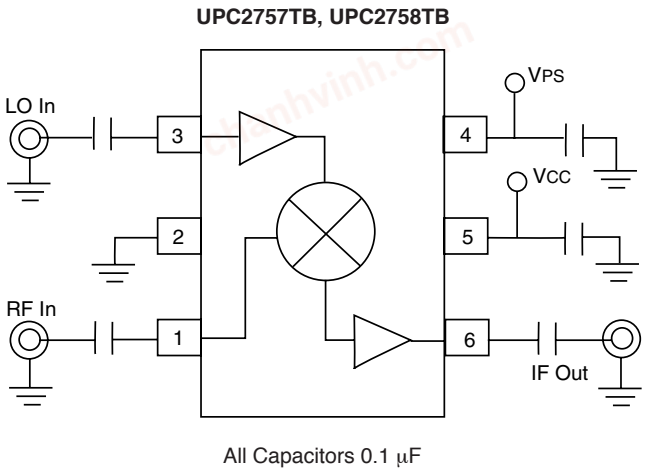
SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}, V_{PS}	Supply Voltage	V	5.5
P_T	Total Power Dissipation[2]	mW	200
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50 x 50 x 1.6 mm epoxy glass PWB (T_A = +85°C).

RECOMMENDED OPERATING CONDITIONS

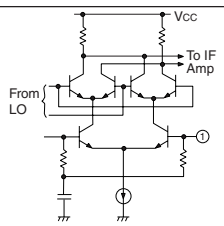
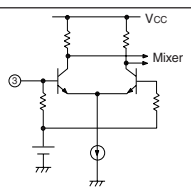
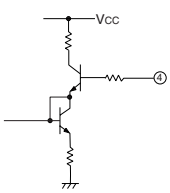
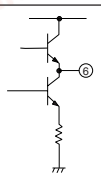
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	3.3
T_{OP}	Operating Temperature	°C	-40	+25	+85
P_{LO}	LO Input Level	dBm	-15	-10	0

TEST CIRCUIT/BLOCK DIAGRAM



All Capacitors 0.1 μF

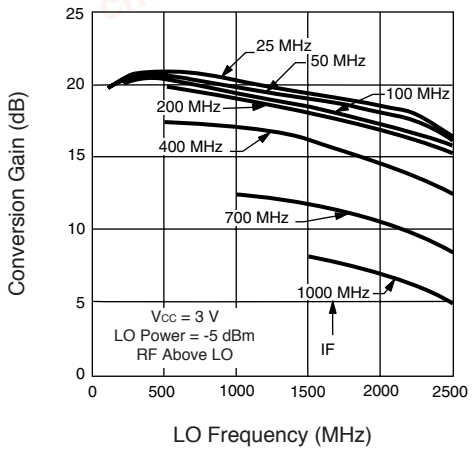
PIN DESCRIPTION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)	Description	Internal Equivalent Circuit
1	RF_{IN}	—	1.2	Signal input pin to double balanced mixer. This pin must be coupled to the signal source with a blocking capacitor.	
2	GND	0	—	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible.	
3	LO_{IN}	—	1.3	LO input pin. The LO buffer is designed as a differential amplifier. Recommended input level is -15 to 0 dBm.	
4	V_{PS}	VCC / GND	—	Power save control pin can control the On/Sleep state with bias as follows: V_{PS} (V) / STATE ≥2.5 / ON 0 to 0.5 / SLEEP Rise time/fall time using this pin is approximately 10 μs.	
5	V_{CC}	2.7 to 3.3	—	Power supply pin. This pin should be externally equipped with a bypass capacitor to minimize ground impedance.	
6	IF_{OUT}	—	1.7	Output of single-ended push-pull IF buffer amplifier. This is an emitter-follower output with low impedance. This pin must be coupled to the next stage with a blocking capacitor.	

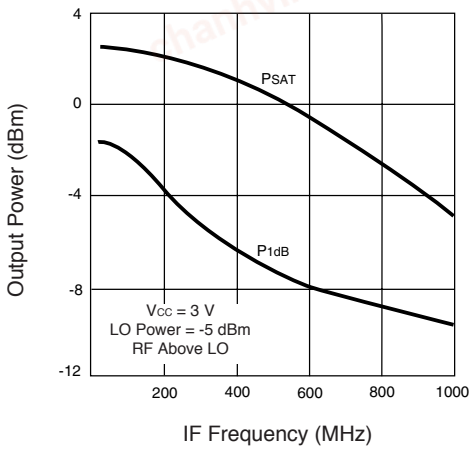
chanhvinh.com

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

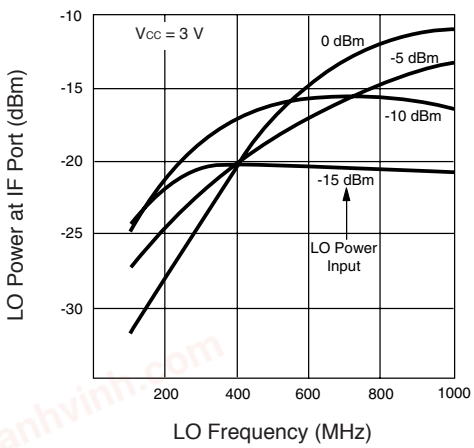
UPC2758TB
CONVERSION GAIN vs. LO FREQUENCY



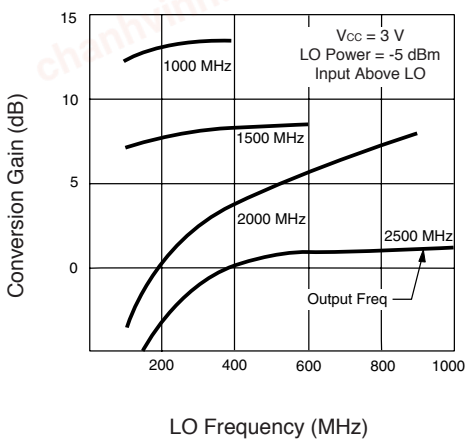
UPC2758TB
OUTPUT POWER vs. IF FREQUENCY



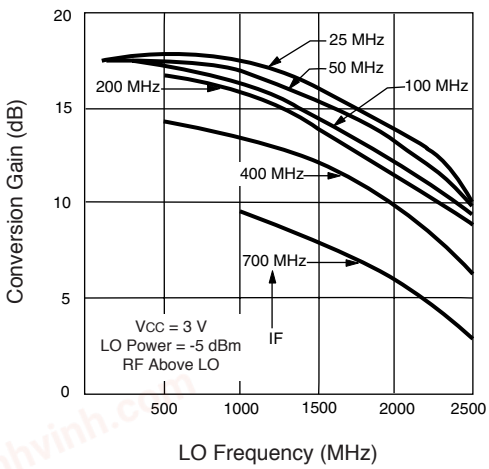
UPC2758TB
LO TO IF ISOLATION vs. LO FREQUENCY



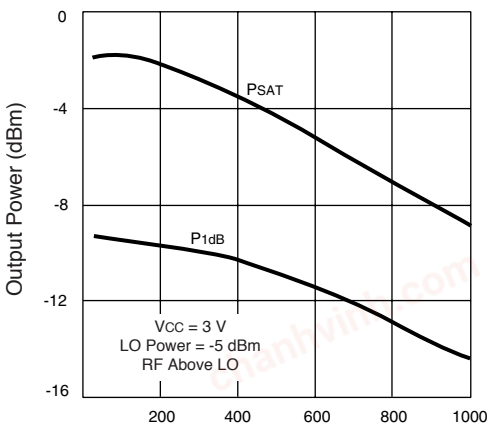
UPC2758TB
UP-CONVERSION GAIN vs. LO FREQUENCY



UPC2757TB
CONVERSION GAIN vs. LO FREQUENCY



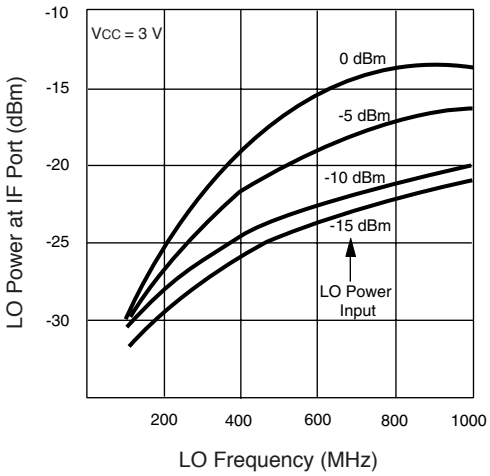
UPC2757TB
OUTPUT POWER vs. IF FREQUENCY



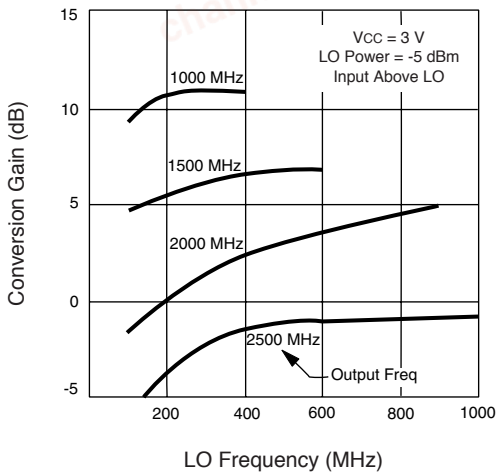
chanhvinh.com

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

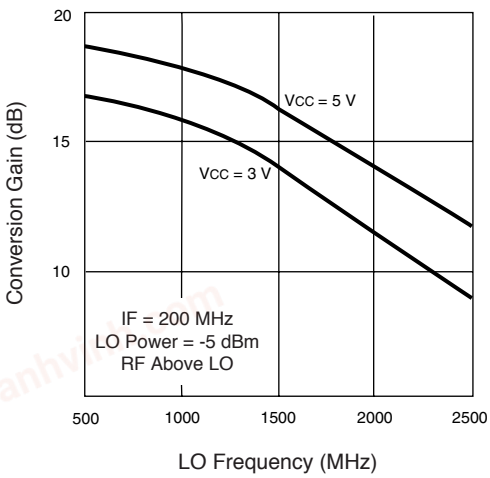
UPC2757TB
LO TO IF ISOLATION vs. LO FREQUENCY



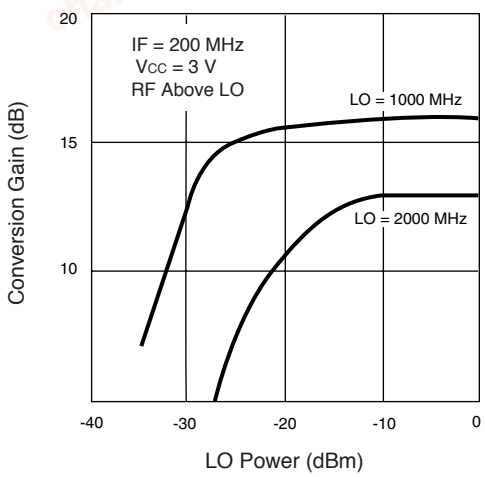
UPC2757TB
UP-CONVERSION GAIN vs. LO FREQUENCY



UPC2757TB
CONVERSION GAIN vs. LO FREQUENCY



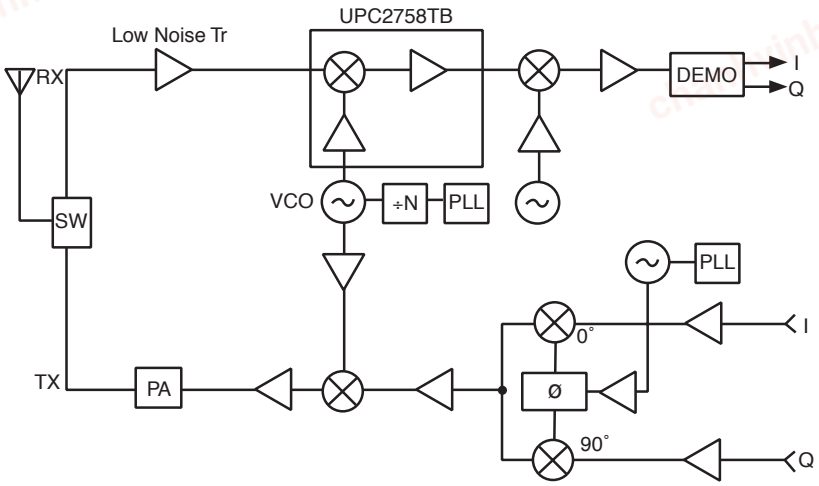
UPC2757TB
CONVERSION GAIN vs. LO POWER



chanhvinh.com

APPLICATION EXAMPLE

Digital Cellular Telephone



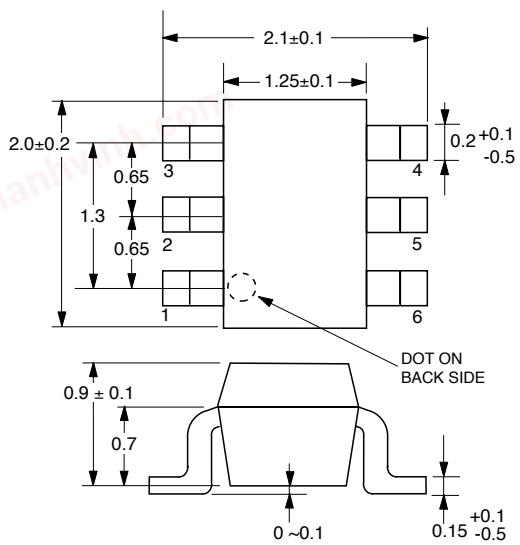
ORDERING INFORMATION

PART NUMBER	QTY
UPC2757TB-E3-A	3K/Reel
UPC2758TB-E3-A	3K/Reel

Note:
Embossed Tape, 8 mm wide,
Pins 1, 2, 3 are in tape pull-out direction.

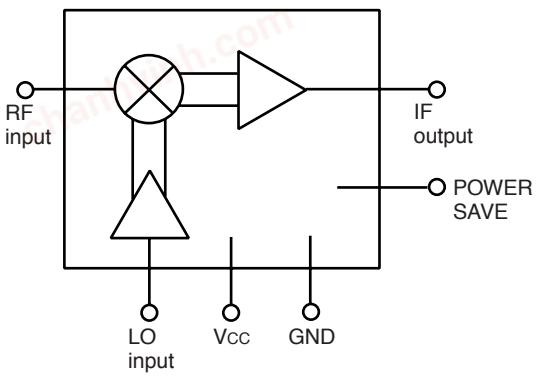
OUTLINE DIMENSIONS

PACKAGE OUTLINE S06

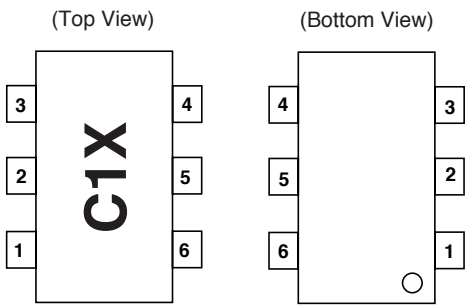


Note:
All dimensions are typical unless otherwise specified.

INTERNAL BLOCK DIAGRAM



LEAD CONNECTIONS



1. RF INPUT
2. GND
3. LO INPUT
4. PS
5. VCC
6. IF OUTPUT

Note:
Package Markings:
C1X: UPC2757TB
C1Y: UPC2758TB