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Datasheet

RX72M Group
Renesas MCUs

R01DS0332EJ0100
Rev.1.00
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240-MHz 32-bit RX MCU, on-chip double-precision FPU, 1396 CoreMark, Arithmetic unit for trigonometric functions, up to 4-MB flash memory (supportive of the dual bank function), 1-MB SRAM, EtherCAT Slave Controller, various communications interfaces including Ethernet MAC compliant with IEEE 1588, SD host interface, quad SPI, and CAN, 12-bit A/D converter, RTC, Encryption functions (optional), Serial sound interface, CMOS camera interface, Graphic-LCD controller, 2D drawing engine

Features

■ 32-bit RXv3 CPU core
- Maximum operating frequency: 240 MHz
  Capable of 1396 CoreMark in operation at 240 MHz
- Double-precision 64-bit IEEE-754 floating point
- A collective register bank save function is available.
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture
- Operation from a single 2.7- to 3.6-V supply
- RTC is capable of operation from a dedicated power supply.
- Four low-power modes

■ On-chip code flash memory
- Supports versions with up to 4 Mbytes of ROM
- No wait cycles at up to 120 MHz or when the ROM cache is hit, one-wait state at above 120 MHz
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

■ On-chip data flash memory
- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM
- 1 Mbyte of SRAM (no wait states; however, if ICLK is at a frequency above 120 MHz, access to locations in the 512 Kbytes of SRAM from 0080 0000h to 0087 FFFFh requires one cycle of waiting)
- 32 Kbytes of RAM with ECC (single error correction/double error detection)
- 8 Kbytes of standby RAM (backup on deep software standby)

■ Data transfer
- DMACAa: 8 channels
- DTCb: 1 channel
- EXDMAC: 2 channels
- DMAC for the Ethernet controller: 3 channels

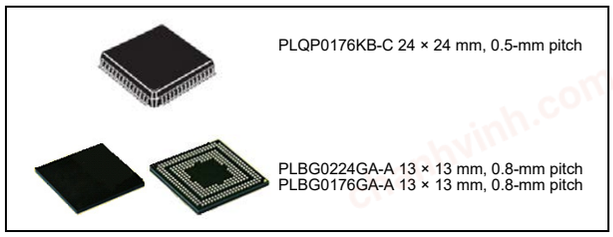
■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- PLL for specific purposes
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture function
  (for capturing times in response to event-signal input)

■ Independent watchdog timer
- 120-kHz clock operation

■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, frequency measurement, CRCA, IWDTa, self-diagnostic function for the A/D converter, etc.
- Register write protection function can protect values in important registers against overwriting.



■ Various communications interfaces
- EtherCAT slave controller (two ports)
- Ethernet MAC compliant with IEEE 1588 (2 channels)
- PHY layer (1 channel) for host/function or OTG controller (1 channel) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (3 channels)
- SCIj and SCIh with multiple functionalities (8 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- SCIi with 16-byte transmission and reception FIFOs (5 channels)
- I^2C bus interface for transfer at up to 1 Mbps (3 channels)
- Four-wire QSPI (1 channel) in addition to RSPIc (3 channels)
- Parallel data capture unit (PDC) for the CMOS camera interface
- Graphic-LCD controller (GLCDC)
- 2D drawing engine (DRW2D)
- SD host interface (1 channel) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- MMCIF with 1-, 4-, or 8-bit transfer bus width

■ External address space
- Buses for full-speed data transfer (max. operating frequency of 80 MHz)
- 8 CS areas
- 8-, 16-, or 32-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

■ Up to 29 extended-function timers
- 32-bit GPTW (4 channels)
- 16-bit TPUa (6 channels), MTU3a (9 channels)
- 8-bit TMRa (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

■ 12-bit A/D converter
- Two 12-bit units (8 channels for unit 0; 21 channels for unit 1)
- Self diagnosis, detection of analog input disconnection

■ 12-bit D/A converter: 2 channels

■ Temperature sensor for measuring temperature within the chip

■ Arithmetic unit for trigonometric functions

■ Delta-Sigma Modulator Interface
- Six external delta-sigma modulators are connectable

■ Encryption functions (optional)
- AES (key lengths: 128, 192, and 256 bits)
- Trusted Secure IP (TSIP)

■ Up to 182 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating temp. range
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C

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1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.
Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package and the capacity of the code flash memory. For details, refer to Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/11)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 240 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • 113 instructions Instructions installed as standard: 111 Basic instructions: 77 Single-precision floating-point operation instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single-precision floating-point numbers (32 bits) and double-precision floating-point numbers (64 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard
	Double-precision floating point coprocessor	• Double-precision floating-point register set Double-precision floating-point data registers: 16, each with 64-bit width Double-precision floating-point control registers: Four, each with 32-bit width • Double-precision floating-point processing instructions: 21 • Notifying the interrupt controller of double-precision floating-point exceptions
	Register bank save function	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

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Table 1.1 Outline of Specifications (2/11)

Classification	Module/Function	Description
Memory	Code flash memory	• Capacity: 2 Mbytes/4 Mbytes • ROM cache: 8 Kbytes • 120 MHz ≤ No-wait cycle access, 120 MHz > One-wait cycle access • Instructions hitting the ROM cache or operand = 240 MHz: No-wait access • On-board programming: Four types • Off-board programming (parallel programmer mode) • Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized. • A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data flash memory	• Capacity: 32 Kbytes • Programming/erasing: 100,000 times
	Unique ID	• 16-byte unique ID for each device
	RAM	• Capacity: 512 Kbytes • Up to 240 MHz, no-wait access
	Expansion RAM	• Capacity: 512 Kbytes • 120 MHz ≤ No-wait cycle access, 120 MHz > One-wait cycle access
	ECC RAM	• Capacity: 32 Kbytes • If the operating frequency is no greater than 120 MHz, one-wait cycle access, if greater than 120MHz, two-wait cycle access in the case of reading, and three-wait cycle access in the case of writing • SEC-DED (single-bit error correction and double-bit error detection)
	Standby RAM	• Capacity: 8 Kbytes • Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (for the SCI interface) Boot mode (for the USB interface) Boot mode (for the FINE interface) • Selection of operating mode by register setting Single-chip mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode • Endian selectable
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer (two circuits), and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 240 MHz Peripheral modules of MTU, RSPI, SCIi, ETHERC, EPTPC, PMGI, EDMAC, GPTW, GLCDC, DRW2D, and ESC run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the S12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz ADCLK in the S12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 80 MHz • The high-speed on-chip oscillator (HOCO) can be obtained through frequency-multiplication of the PLL or PPLL reference clock • External clock input frequency: 30 MHz (max) • Clock output function

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Table 1.1 Outline of Specifications (3/11)

Classification	Module/Function	Description
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		• If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, 2.80 V) • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, 2.85 V) Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking
Low power consumption	Low power consumption function	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Battery backup function	• When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating.
Interrupt	Interrupt controller (ICUD)	• Number of interrupt vectors: 256 • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: 2 sources • Non-maskable interrupts: 8 sources • Sixteen levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 128 vectors are selected from among the other 169 sources.)
External bus extension		• The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7) A chip-select signal (CS0# to CS7#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • SDRAM interface connectable • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility

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Table 1.1 Outline of Specifications (4/11)

Classification	Module/Function	Description
DMA	DMA controller (DMACAa)	• 8 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger and interrupt requests from peripheral functions
	EXDMA controller (EXDMACa)	• 2 channels Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer • Single-address transfer enabled with the EDACKn signal • Request sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions
	Data transfer controller (DTCb)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions • Sequence transfer
I/O ports	Programmable I/O ports	• I/O ports for the 224-pin LFBGA I/O pins: 182 Input pin: 1 Pull-up resistors: 182 Open-drain outputs: 182 5-V tolerance: 19 • I/O ports for the 176-pin LFBGA and 176-pin LFQFP I/O pins: 136 Input pin: 1 Pull-up resistors: 136 Open-drain outputs: 136 5-V tolerance: 19
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 137 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.

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Table 1.1 Outline of Specifications (5/11)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Digital filtering of signals from the input capture pins • Event linking by the ELC
	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLK/A32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 14 of the signals are available for channel 0, 11 are available for channels 1, 3, 4, 6 to 8, 12 are available for channel 2, and 10 are available for channel 5. • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 43 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • PPG output trigger can be generated • Event linking by the ELC
	Port output enable 3 (POE3a)	• Control of the high-impedance state of the MTU waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by oscillation-stoppage detection or software • Additional programming of output control target pins is enabled

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Table 1.1 Outline of Specifications (6/11)

Classification	Module/Function	Description
Timers	General PWM timer (GPTW)	• 32 bits × 4 channels (GPTW0 to GPTW3) • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Capable of synchronous start, stop, or clearing of counter for any channel • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting input level comparison • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 4 external triggers • Output pin disabling function by a dead time error or a short circuit detection among output pins • Capable of generating conversion start triggers for the A/D converters as well as monitoring external pins for a start timing of conversion. • Capable of outputting events, such as compare-match from A to F and overflow/ underflow, to ELC • Capable of using noise filter of input capture
	Port output enable for GPTW (POEG)	• Controlling the output disable for GPTW waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPTW • Initiation by detection of oscillation stop or by software
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMR)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512)
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)*1	• Clock sources: Main clock, sub-clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)

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Table 1.1 Outline of Specifications (7/11)

Classification	Module/Function	Description
Timers	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
Communication function	Ethernet controller (ETHERC)	• 2 channels • Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) and RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*2 or output of a “wake-on-LAN” signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards • Filtering of multicast frames is supported. • Frame data can be directly transferred between 2 channels by cut-through switching.
	PHY management interface (PMGI)	• 2 channels • This module is compliant with the MII (Media Independent Interface) as defined in the IEEE 802.3u standard. • Transmission and reception of management frames through PHY-LSI chips having an MII or RMII interface is supported. • Alleviates load on the CPU by shifting it to dedicated hardware • The timing of management data is adjustable. • Preambles can be deleted.
	PTP module for the ethernet controller (EPTPCb)	• In connection with the Ethernet controller (ETHERC), this module is compliant with the IEEE1588 standard. • Matching with time stamps can be used to trigger counting by the MTU and GPTW.
	DMA controller for ethernet controller (EDMACa)	• 3 channels (each EDMAC determines the order of priority by a round-robin algorithm) For ETHERC: 2 channels, for EPTPC: 1 channel • Alleviation of CPU load by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 4 Kbytes
	EtherCAT slave controller (ESC)*3	• One channel (two ports) • The Beckoff EtherCAT Slave Controller IP Core was adopted for this.
	USB 2.0 FS host/ function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-power mode and bus-power mode are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required

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Table 1.1 Outline of Specifications (8/11)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIj, SCIi, SCIh)	• 13 channels (SCIj: 7 channels + SCIi: 5 channels + SCIh: 1 channel) • SCIj, SCIi, SCIh Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Start-bit detection: Level or edge detection is selectable. Simple I2C Simple SPI 7- to 9-bit transfer mode Bit rate modulation Double-speed mode Detecting matches of data is supported (other than for SCI12) • SCIj, SCIh Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Event linking by the ELC (only on channel 5) • SCIh Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format • SCIi Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit
	I2C bus interface (RIICa)	• 3 channels (only channel 0 can be used in fast-mode plus) Communication formats I2C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) • Event linking by the ELC
	CAN module (CAN)	• 3 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interface (RSPIc)	• 3 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transit/receive data can be swapped in byte units • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC
	Quad serial peripheral interface (QSPI)	• 1 channel • Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation) • Programmable bit length and selectable active sense and phase of the clock signal • Sequential execution of transfer • LSB or MSB first is selectable

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Table 1.1 Outline of Specifications (9/11)

Classification	Module/Function	Description
Extended serial sound interface (SSIE)		• 2 channels • Full-duplex transmission (only for channel 0) • Various types of serial audio formatting are supported. • Master and slave operations are supported. • The bit-clock frequency is selectable from among 13 frequencies (1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128). • Data formats with 8, 16, 18, 20, 22, 24, and 32 bits are supported. • 32-stage FIFO buffers for transmission and reception • Stopping or not stopping the SSILRCK signal on stopping of data transmission is selectable.
SD host interface (SDHI)		• 1 channel • Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt, interrupt of SD buffer access • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection
MMC host interface (MMCIF)		• 1 channel • Transfer speed: Data transfer mode (30 MB/s), backward compatible mode (25 MB/s) • Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported) • Interface for Multimedia Cards (MMCs) • Data buses: Support for 1-, 4-, and 8-bit MMC buses • Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt, interrupt of MMCIF buffer access • DMA transfer requests: CE_DATA write and CE_DATA read • Support for card detection, boot operation, high priority interrupt (HPI)
The arithmetic unit for trigonometric functions (TFU)		• Sine, cosine, arctangent, $\sqrt{x^2+y^2}$ Simultaneous calculation of sine and cosine Simultaneous calculation of arctangent and $\sqrt{x^2+y^2}$
Delta-sigma modulator interface (DSMIF)		• 6 channels • Up to six external delta-sigma modulators are connectable. • The sinc filters are selectable as first-, second-, or third-order.
Parallel data capture unit (PDC)		• 1 channel • Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals • Setting of the image size when clipping of the output for a one-frame image is required
Graphic-LCD controller (GLCDC)		• 1 channel • Various data formats and LCD panels are supported • Superposition of 3 planes (single-color background, graphic 1, graphic 2) • 32- and 16-bpp graphics data and 8-, 4-, and 1-bit CLUT data formats are supported
2D drawing engine (DRW2D)		• 1 channel • Vector drawing (straight lines, triangles, and circles) • Bit blitting (with support for filling, copying, stretching, and rotation) • Bus master function for input and output of frame buffer data 32-, 16-, and 8-bit pixel graphics data are supported • Bus master function for input of texture data Input of texture data (32, 24, 16, 8, 4, 2, or 1 bit) are supported. Run length encoding is supported A CLUT is installed and index data can be converted into color data • Two rendering modes are supported (register mode and display list mode) • Performance counting • Interrupts in response to completion of rendering and processing of the display list

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Table 1.1 Outline of Specifications (10/11)

Classification	Module/Function	Description
12-bit A/D converter (S12ADFa)		• 12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels) • 12-bit resolution (switchable between 8, 10, and 12 bits) • Conversion time 0.48 µs per channel (for 12-bit conversion) 0.45 µs per channel (for 10-bit conversion) 0.42 µs per channel (for 8-bit conversion) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control (only for 3 group scan mode) • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (MTU, TMR, TPU) trigger, external trigger • Event linking by the ELC
12-bit D/A converter (R12DAa)		• 2 channels • 12-bit resolution • Output voltage: 0.2 V to AVCC1 – 0.2 V (buffered output), 0 V to AVCC1 (unbuffered output) • Buffered output or unbuffered output can be selected. • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ± 1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An access exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Programs in the TM target area in the code flash memory are protected against reading • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection	• Main clock oscillation stop detection: Available

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Table 1.1 Outline of Specifications (11/11)

Classification	Module/Function	Description
Safety	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, USB clock, Ethernet-PHY external clock, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	• The function to compare, add, or subtract 16-bit data
Encryption function	Trusted Secure IP (TSIP)*4	• Security algorithm Common key encryption: AES (compliant with NIST FIPS PUB 197), TDES, ARC4 Non-common key encryption: RSA • Other features TRNG (true-random number generator) Hash value generation: SHA1, SHA224, SHA256, MD5, GHASH Prevention of the illicit copying of keys
Operating frequency		Up to 240 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, V_{BATT} = 2.0 to 3.6 V
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C
Package		224-pin LFBGA (PLBG0224GA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LFQFP (PLQP0176KB-C)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces)

Note 1. When the realtime clock is not used, initialize the registers in the time clock according to description in section 33.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.
Note 2. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 3. EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.
Note 4. The product part number differs according to whether or not the MCU includes the encryption function.

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Table 1.2 Comparison of Functions for Different Packages (1/2)

Functions		RX72M	
Package		**224 Pins**	**176 Pins**
External bus	External bus width	32 bits/16 bits/8 bits	
	SDRAM area controller	Available	
DMA	DMA controller	Ch. 0 to 7	
	Data transfer controller	Available	
	EXDMA controller	Ch. 0 and 1	
Timers	16-bit timer pulse unit	Ch. 0 to 5	
	Multi-function timer pulse unit 3	Ch. 0 to 8	
	General PWM timer	Ch. 0 to 3	
	Port output enable 3	Available	
	Port output enable for GPTW	Available	
	Programmable pulse generator	Ch. 0 and 1	
	8-bit timers	Ch. 0 to 3	
	Compare match timer	Ch. 0 to 3	
	Compare match timer W	Ch. 0 and 1	
	Realtime clock	Available	
	Watchdog timer	Available	
	Independent watchdog timer	Available	
Communication function	Ethernet controller	Ch. 0 and 1	
	PHY management interface	Ch. 0 and 1	
	PTP controller for the ethernet controller	Available	
	DMA controller for the ethernet controller	Ch. 0 and 1 (ETHERC) Ch. 2 (EPTPC)	
	EtherCAT slave controller	Ch. 0 and 1	
	USB 2.0 FS host/function module	Ch. 0	
	Serial communications interfaces (SCIj)	Ch. 0 to 6	
	Serial communications interfaces (SCIi)	Ch. 7 to 11	
	Serial communications interfaces (SCIh)	Ch. 12	
	I^2C bus interfaces	Ch. 0 to 2	
	Serial peripheral interface	Ch. 0 to 2	
	CAN module	Ch. 0 to 2	
	Quad serial peripheral interface	Ch. 0	
	Expansion serial sound interface	Ch. 0 and 1	
	SD host interface	Ch. 0	
	Multimediacard interface	Ch. 0	
	Parallel data capture unit	Available	
Graphics	Graphic-LCD controller	Available	
	2D drawing engine	Available	
12-bit A/D converter	Unit 0	AN000 to 007 (8 channels)	
	Unit 1	AN100 to 120 (21 channels)	
12-bit D/A converter		Ch. 0 and 1	
Temperature sensor		Available	
Arithmetic unit for trigonometric functions		Available	

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Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions	RX72M	
Package	**224 Pins**	**176 Pins**
Delta-sigma modulator interface	Available	
CRC calculator	Available	
Data operation circuit	Available	
Clock frequency accuracy measurement circuit	Available	
Trusted Secure IP	Available/Not available	
Event link controller	Available	

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1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	Operating temperature (°C)
RX72M (D-version)	R5F572MNDDFC	PLQP0176KB-C	4 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Not available	–40 to +85
	R5F572MNHDFC	PLQP0176KB-C	4 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Available	–40 to +85
	R5F572MDDDFC	PLQP0176KB-C	2 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Not available	–40 to +85
	R5F572MDHDFC	PLQP0176KB-C	2 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Available	–40 to +85
	R5F572MNDDBD	PLBG0224GA-A	4 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Not available	–40 to +85
	R5F572MNHDBD	PLBG0224GA-A	4 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Available	–40 to +85
	R5F572MDDDBD	PLBG0224GA-A	2 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Not available	–40 to +85
	R5F572MDHDBD	PLBG0224GA-A	2 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Available	–40 to +85
	R5F572MNDDBG	PLBG0176GA-A	4 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Not available	–40 to +85
	R5F572MNHDBG	PLBG0176GA-A	4 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Available	–40 to +85
	R5F572MDDDBG	PLBG0176GA-A	2 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Not available	–40 to +85
	R5F572MDHDBG	PLBG0176GA-A	2 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Available	–40 to +85
RX72M (G-version)	R5F572MNDGFC	PLQP0176KB-C	4 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Not available	–40 to +105
	R5F572MNHGFC	PLQP0176KB-C	4 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Available	–40 to +105
	R5F572MDDGFC	PLQP0176KB-C	2 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Not available	–40 to +105
	R5F572MDHGFC	PLQP0176KB-C	2 Mbytes	1 Mbyte	32 Kbytes	240 MHz	Available	–40 to +105

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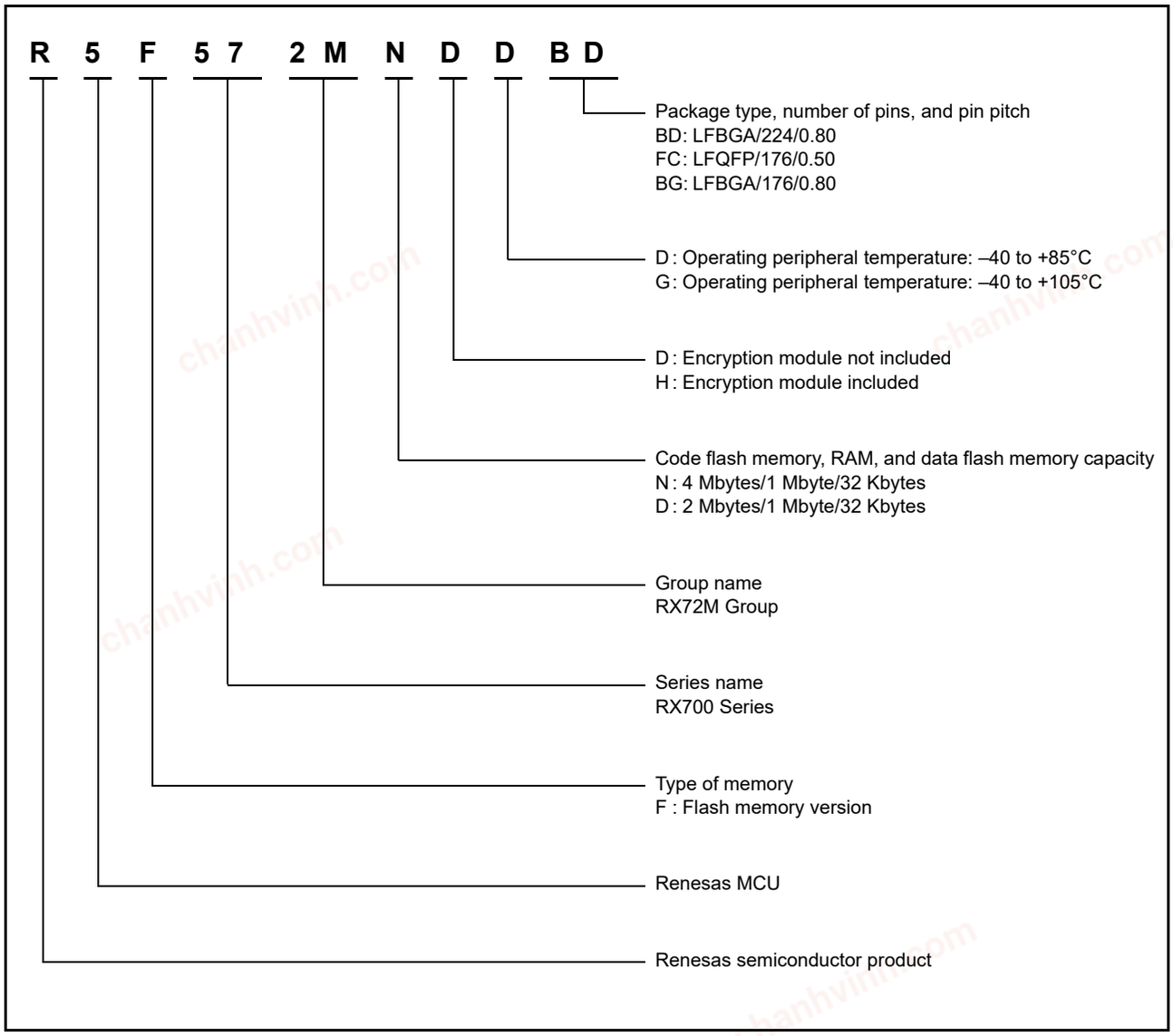
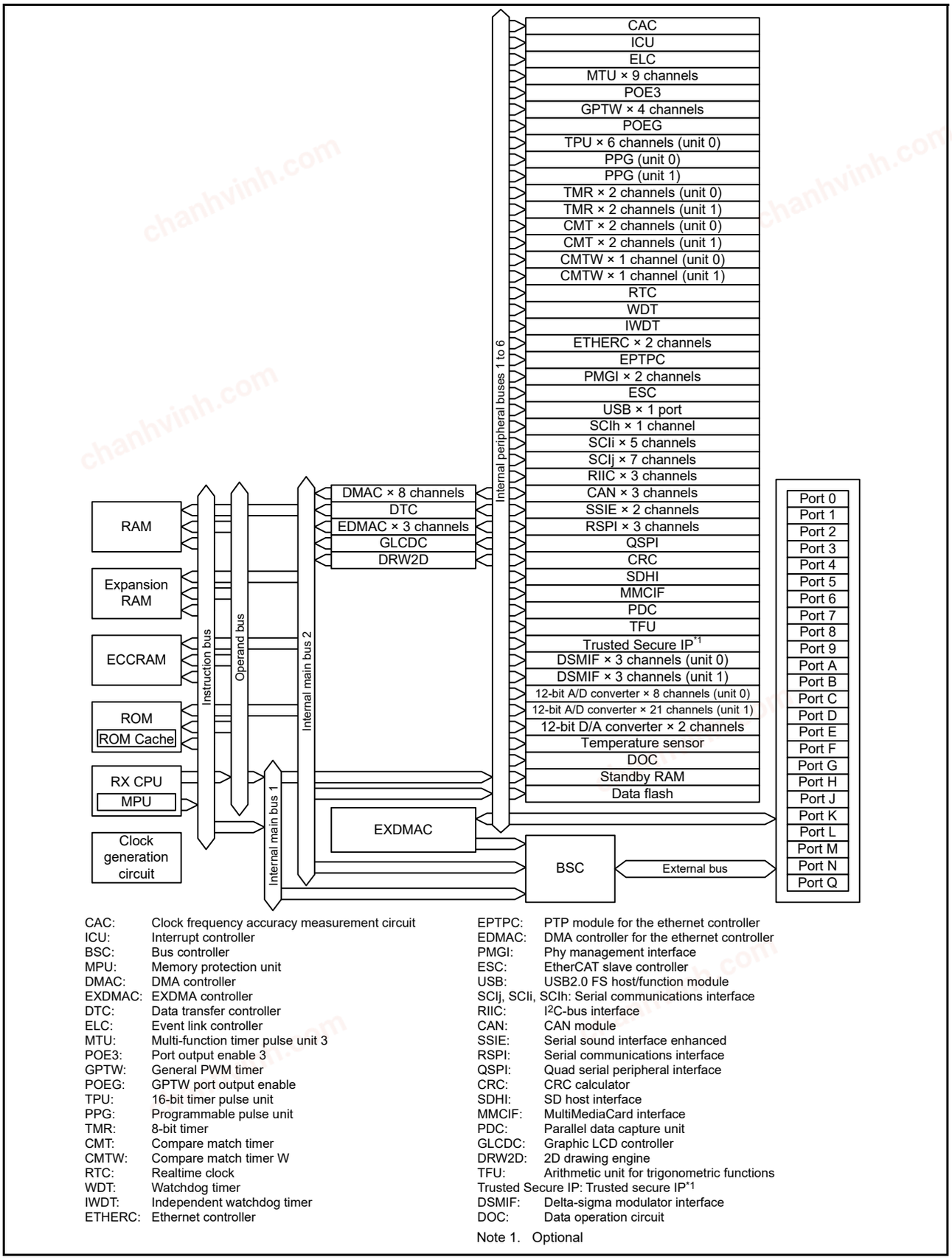


Figure 1.1 How to Read the Product Part Number

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1.3 Block Diagram

Figure 1.2 shows a block diagram.



CAC: Clock frequency accuracy measurement circuit
ICU: Interrupt controller
BSC: Bus controller
MPU: Memory protection unit
DMAC: DMA controller
EXDMAC: EXDMA controller
DTC: Data transfer controller
ELC: Event link controller
MTU: Multi-function timer pulse unit 3
POE3: Port output enable 3
GPTW: General PWM timer
POEG: GPTW port output enable
TPU: 16-bit timer pulse unit
PPG: Programmable pulse unit
TMR: 8-bit timer
CMT: Compare match timer
CMTW: Compare match timer W
RTC: Realtime clock
WDT: Watchdog timer
IWDT: Independent watchdog timer
ETHERC: Ethernet controller

EPTPC: PTP module for the ethernet controller
EDMAC: DMA controller for the ethernet controller
PMGI: Phy management interface
ESC: EtherCAT slave controller
USB: USB2.0 FS host/function module
SCIj, SCIi, SCIh: Serial communications interface
RIIC: I²C-bus interface
CAN: CAN module
SSIE: Serial sound interface enhanced
RSPI: Serial communications interface
QSPI: Quad serial peripheral interface
CRC: CRC calculator
SDHI: SD host interface
MMCIF: MultiMediaCard interface
PDC: Parallel data capture unit
GLCDC: Graphic LCD controller
DRW2D: 2D drawing engine
TFU: Arithmetic unit for trigonometric functions
Trusted Secure IP: Trusted secure IP*1
DSMIF: Delta-sigma modulator interface
DOC: Data operation circuit

Note 1. Optional

Figure 1.2 Block Diagram

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1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/9)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.22-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Input/output pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
	CLKOUT	Output	Clock output pin.
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Input pin for setting the operating mode. The signal level on this pin must not be changed during operation.
	UB	Input	USB boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-power mode and the high level selects bus power mode.
System control	RES#	Input	Reset signal input pin. This MCU enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	FINE interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC, TRSYNC1	Output	These pins indicate that output from the TRDATA0 to TRDATA7 pins is valid.
	TRDATA0 to TRDATA7	Output	These pins output the trace information.
Address bus	A0 to A26	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

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Table 1.4 Pin Functions (2/9)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
SDRAM interface	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strove signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15, IRQ0-DS to IRQ15-DS	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU in the high impedance state

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Table 1.4 Pin Functions (3/9)

Classifications	Pin Name	I/O	Description
General PWM timer W	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	Input pins for the external trigger signals
	GTIOC0A to GTIOC3A, GTIOC0B to GTIOC3B	I/O	Input capture input/output compare output/PWM output pins
	GTADSM0, GTADSM1	Output	Output pins for monitoring A/D conversion start requests.
16-bit timer pulse unit	TIOCA0, TIOCB0, TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins
	TCLKA, TCLKB, TCLKC, TCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC3	Output	Output pins for CMTW
Serial communications interface (SCIj)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK6	I/O	Input/output pins for the clock
	RXD0 to RXD6	Input	Input pins for received data
	TXD0 to TXD6	Output	Output pins for transmitted data
	CTS0# to CTS6#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS6#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL6	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA6	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK6	I/O	Input/output pins for the clock
	SMISO0 to SMISO6	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI6	I/O	Input/output pins for master transmission of data
	SS0# to SS6#	Input	Chip-select input pins

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Table 1.4 Pin Functions (4/9)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIi)	• Asynchronous mode/clock synchronous mode		
	SCK7 to SCK11	I/O	Input/output pins for the clock
	RXD7 to RXD11	Input	Input pins for received data
	TXD7 to TXD11	Output	Output pins for transmitted data
	CTS7# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS7# to RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL7 to SSCL11	I/O	Input/output pins for the I^2C clock
	SSDA7 to SSDA11	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK7 to SCK11	I/O	Input/output pins for the clock
	SMISO7 to SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI7 to SMOSI11	I/O	Input/output pins for master transmission of data
	SS7# to SS11#	Input	Chip-select input pins
I^2C bus interface	SCL0[FM+], SCL1, SCL2, SCL2-DS	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA1, SDA2, SDA2-DS	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

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Table 1.4 Pin Functions (5/9)

Classifications	Pin Name	I/O	Description
Ethernet controller	REF50CK0, REF50CK1	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode.
	RMII0_CRS_DV, RMII1_CRS_DV	Input	These pins indicate that there are carrier detection signals and valid receive data on RMIIn_RXD1 and RMIIn_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1, RMII1_TXD0, RMII1_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1, RMII1_RXD0, RMII1_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN, RMII1_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode
	RMII0_RX_ER, RMII1_RX_ER	Input	These pins indicate an error has occurred during reception of data in RMII mode.
	ET0_CRS, ET1_CRS	Input	Carrier detection/data reception enable pins
	ET0_RX_DV, ET1_RX_DV	Input	These pins indicate that there are valid receive data on ETn_ERXD3 to ETn_ERXD0.
	ET0_EXOUT, ET1_EXOUT	Output	General-purpose external output pins
	ET0_LINKSTA, ET1_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3, ET1_ETXD0 to ET1_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3, ET1_ERXD0 to ET1_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN, ET1_TX_EN	Output	Transmit enable pins. These pins function as signals indicating that transmit data are ready on ETn_ETXD3 to ETn_ETXD0.
	ET0_TX_ER, ET1_TX_ER	Output	Transmit error pins. These pins function as signals notifying the PHY-LSI of an error during transmission.
	ET0_RX_ER, ET1_RX_ER	Input	Receive error pins. These pins function as signals to recognize an error during reception.
	ET0_TX_CLK, ET1_RX_CLK	Input	Transmit clock pins. These pins input reference signals for output timings from ETn_TX_EN, ETn_ETXD3 to ETn_ETXD0, and ETn_TX_ER.
	ET0_RX_CLK, ET1_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timings to ETn_RX_DV, ETn_ERXD3 to ETn_ERXD0, and ETn_RX_ER.
	ET0_COL, ET1_COL	Input	Input collision detection signals.
	ET0_WOL, ET1_WOL	Output	Receive Magic packets.
	ET0_MDC, ET1_MDC	Output	Output reference clock signals for information transfer via ETn_MDIO.
	ET0_MDIO, ET1_MDIO	I/O	Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.
	CLKOUT25M	Output	25-MHz clock output pin for PHY clock input (used in common by the EtherCAT module)
	EPLSOUT0, EPLSOUT1	Output	Pulse output signals for time synchronization
PHY management interface	PMGI0_MDC, PMGI1_MDC	Output	Reference clock signals for information transfer by PMGIn_MDIO
	PMGI0_MDIO, PMGI1_MDIO	I/O	Bi-directional signals for the exchange of management information between the PHY LSI chip and this MCU

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Table 1.4 Pin Functions (6/9)

Classifications	Pin Name	I/O	Description
EtherCAT slave controller	• MII mode		
	CAT0_LINKSTA, CAT1_LINKSTA	Input	PHY link signal input pins
	CAT0_RX_CLK, CAT1_RX_CLK	Input	Receive clock input pins
	CAT0_RX_DV, CAT1_RX_DV	Input	Receive data enabling signal input pins
	CAT0_ERXD0 to CAT0_ERXD3, CAT1_ERXD0 to CAT1_ERXD3	Input	Receive data signal input pins
	CAT0_RX_ER, CAT1_RX_ER	Input	Receive data error signal input pins
	CAT0_TX_CLK, CAT1_TX_CLK	Input	Transmit clock input pins
	CAT0_TX_EN, CAT1_TX_EN	Output	Transmit enabling signal output pins
	CAT0_ETXD0 to CAT0_ETXD3, CAT1_ETXD0 to CAT1_ETXD3	Output	Transmit data signal output pins
	CAT0_MDC	Output	Management interface clock output pin
	CAT0_MDIO	I/O	Management data signal input/output pin
	CLKOUT25M	Output	25-MHz clock output pin for PHY clock input (used in common by the EtherC module)
	• Exclusively for EtherCAT		
	CATRESTOUT	Output	Output signal for resetting the PHY chip
	CATLEDRUN	Output	EtherCAT run LED signal output pin
	CATIRQ	Output	EtherCAT IRQ signal output pin
	CATLEDSTER	Output	EtherCAT dual-color state LED signal output pin
	CATLEDERR	Output	EtherCAT error LED signal output pin
	CATLINKACT0, CATLINKACT1	Output	EtherCAT link/activity LED signal output pins
	CATSYNC0, CATSYNC1	Output	EtherCAT sync signal output pins
	CATLATCH0, CATLATCH1	Input	EtherCAT latch signal output pins
	CATI2CCLK	Output	EtherCAT EEPROM I^2C clock signal output pin
	CATI2CDATA	I/O	EtherCAT EEPROM I^2C data signal input/output pin
USB 2.0 host/function module	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB0_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN	Output	USB VBUS power enable pin
	USB0_OVRCURA/ USB0_OVRCURB	Input	USB overcurrent pins
	USB0_VBUS	Input	USB cable connection/disconnection detection input pin
CAN module	CRX0, CRX1, CRX2, CRX1-DS	Input	Input pins
	CTX0, CTX1, CTX2	Output	Output pins

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Table 1.4 Pin Functions (7/9)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA-A/RSPCKA-B/ RSPCKB-A/RSPCKB-B/ RSPCKC-A/RSPCKC-B	I/O	Clock input/output pins
	MOSIA-A/MOSIA-B/ MOSIB-A/MOSIB-B/ MOSIC-A/MOSIC-B	I/O	Input or output data output from the master
	MISOA-A/MISOA-B/ MISOB-A/MISOB-B/ MISOC-A/MISOC-B	I/O	Input or output data output from the slave
	SSLA0-A/SSLA0-B/ SSLB0-A/SSLB0-B/ SSLC0-A/SSLC0-B	I/O	Input or output pins for slave selection
	SSLA1-A/SSLA1-B/ SSLB1-A/SSLB1-B/ SSLC1-A/SSLC1-B, SSLA2-A/SSLA2-B/ SSLB2-A/SSLB2-B/ SSLC2-A/SSLC2-B, SSLA3-A/SSLA3-B/ SSLB3-A/SSLB3-B/ SSLC3-A/SSLC3-B	Output	Output pins for slave selection
Quad serial peripheral interface	QSPCLK-A/QSPCLK-B	Output	QSPI clock output pins
	QSSL-A/QSSL-B	Output	QSPI slave output pins
	QMO-A/QMO-B, QIO0-A/QIO0-B	I/O	Master transmit data/data 0
	QMI-A/QMI-B, QIO1-A/QIO1-B	I/O	Master input data/data 1
	QIO2-A/QIO2-B, QIO3-A/QIO3-B	I/O	Data 2, data 3
Serial sound interface enhanced	SSIBCK0, SSIBCK1	I/O	SSIE serial bit-clock pins
	SSILRCK0, SSILRCK1	I/O	LR clock
	SSITXD0	Output	Serial data output pin
	SSIRXD0	Input	Serial data input pin
	SSIDATA1	I/O	Serial data input/output pin
	AUDIO_CLK	Input	External clock pin for audio (input for an oversampling clock)
MMC host interface	MMC_CLK-A/MMC_CLK-B	Output	MMC clock pins
	MMC_CMD-A/MMC_CMD-B	I/O	Command/response pins
	MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B	I/O	Transmit data/receive data
	MMC_CD-A/MMC_CD-B	Input	Card detection pins
	MMC_RES#-A/MMC_RES#-B	Output	MMC reset output pins
SD host interface	SDHI_CLK-A/SDHI_CLK-B/ SDHI_CLK-C	Output	SD clock output pins
	SDHI_CMD-A/SDHI_CMD-B/ SDHI_CMD-C	I/O	SD command output, response input signal pins
	SDHI_D3-A/SDHI_D3-B/ SDHI_D3-C to SDHI_D0-A/ SDHI_D0-B/SDHI_D0-C	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
Delta-sigma modulator interface	DSMCLK0 to DSMCLK5	I/O	Input/output pins for the clock
	DSMDAT0 to DSMDAT5	Input	Input pins for data

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Table 1.4 Pin Functions (8/9)

Classifications	Pin Name	I/O	Description
Parallel data capture unit	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock
Graphic-LCD controller	LCD_CLK-A, LCD_CLK-B	Output	Panel clock output pins
	LCD_TCON3-A/ LCD_TCON3-B to LCD_TCON0-A/ LCD_TCON0-B	Output	Control signal output pins
	LCD_DATA23-A/ LCD_DATA23-B to LCD_DATA0-A/ LCD_DATA0-B	Output	LCD signal output pins
	LCD_EXTCLK-A, LCD_EXTCLK-B	Input	Panel clock source input pins
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
12-bit A/D converter	AN000 to AN007, AN100 to AN120	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.

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Table 1.4 Pin Functions (9/9)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins
	P10 to P17	I/O	8-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins (P35: input pin)
	P40 to P47	I/O	8-bit input/output pins
	P50 to P57	I/O	8-bit input/output pins
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P87	I/O	8-bit input/output pins
	P90 to P97	I/O	8-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF0 to PF5	I/O	6-bit input/output pins
	PG0 to PG7	I/O	8-bit input/output pins
	PJ0 to PJ3, PJ5	I/O	5-bit input/output pins
	PH0 to PH7	I/O	8-bit input/output pins
	PK0 to PK7	I/O	8-bit input/output pins
	PL0 to PL7	I/O	8-bit input/output pins
	PM0 to PM7	I/O	8-bit input/output pins
	PN0 to PN5	I/O	6-bit input/output pins
	PQ0 to PQ7	I/O	8-bit input/output pins

Note: Note the following regarding pin names. For details, refer to section 1.5, Pin Assignments.
- We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups.
  For the RSPI, QSPI, SDHI, MMC, and GLCDC interfaces, the AC portion of the electrical characteristics is measured for each group.
- When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.
- RIIC pin functions that have [FM+] appended to their names support fast-mode plus.

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1.5 Pin Assignments

Figure 1.3 to Figure 1.5 show the pin assignments. Table 1.5 to Table 1.7 are the lists of pins and pin functions.

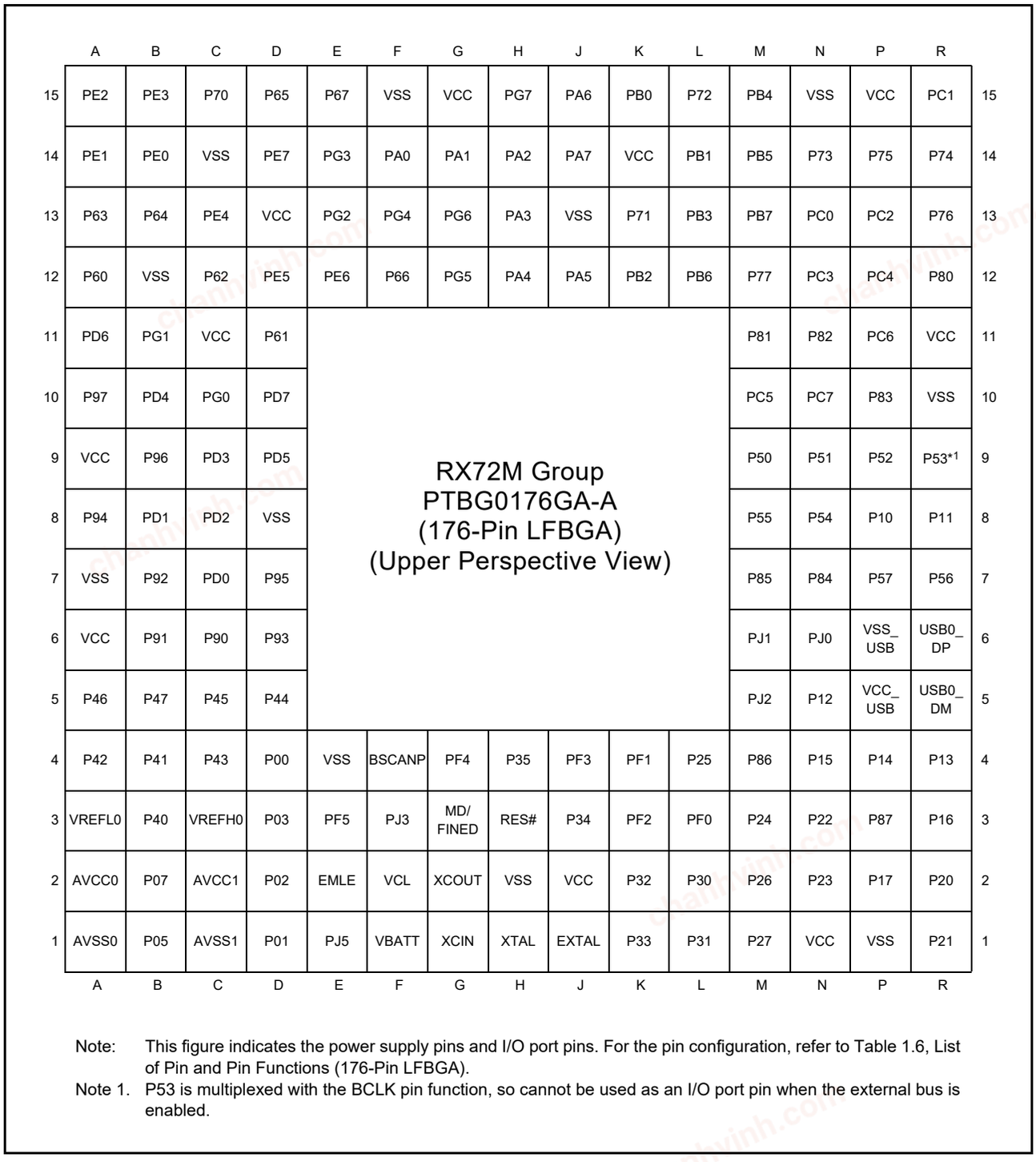
RX72M Group
PLBG0224GA-A (224-Pin LFBGA)
(Upper Perspective View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P70	PE7	P66	P67	PG4	PG7	PA4	PA5	PA7	P72	PB4	PB6	PB7	PM3	PM5	15
14	PE1	PE4	P65	PG2	PG5	PG6	PA3	PA6	PB0	PB3	PB2	PC0	PC1	PM4	P74	14
13	P62	PE2	PE5	VSS	PE6	PG3	PA2	VSS	P71	PB5	VCC	PM7	PM6	PC2	P75	13
12	P61	P63	VSS	PE3	VCC	PA0	PA1	VCC	PB1	VSS	PN4	PL6	P76	PL2	PL4	12
11	PD7	VCC	P64	PE0	PQ4	PM1	PM0	PL0	PN5	PM2	P77	PL5	PK2	PC4	PC3	11
10	PG0	PD6	P60	PG1	PQ5	VSS	VCC	P73	PL1	PL3	PL7	PK0	P80	P82	PC5	10
9	PD3	PD4	P97	PD5	PQ3	PQ6	PN2	PN3	PK3	PK1	P81	P83	PC7	VSS	PC6	9
8	P96	P95	VCC	VSS	PQ1	PN1	PQ2	PQ7	P53*1	P50	P52	P51	VCC	P11	P55	8
7	PD2	P94	PD1	P93	PQ0	PK6	RES#	PJ3	P15	P10	VCC	VSS	P56	P57	P54	7
6	PD0	VCC	P90	P02	PN0	EMLE	PF5	BSCANP	PH2	PH1	PJ2	P84	PJ1	VSS_USB	USB0_DP	6
5	P92	P91	VSS	P01	P07	PK5	PJ5	P32	P30	PF0	VCC	PJ0	P13	VCC_USB	USB0_DM	5
4	P41	P46	P44	P40	P43	PK4	MD/FINED	P33	P31	PH5	P24	VSS	P85	P14	P12	4
3	VREFL0	P42	P05	P03	P00	PF4	VCC	P35	PF3	PH4	PF1	P25	P86	P20	P16	3
2	VREFH0	AVCC0	AVCC1	P47	VSS	VBATT	VSS	P34	PF2	PH6	P27	P23	PH0	P17	P87	2
1	NC	AVSS0	AVSS1	P45	VCL	XCIN	XCOUT	XTAL	EXTAL	PH7	PH3	P26	P22	PK7	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.5, List of Pin and Pin Functions (224-Pin LFBGA).
Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Figure 1.3 Pin Assignment (224-Pin LFBGA)

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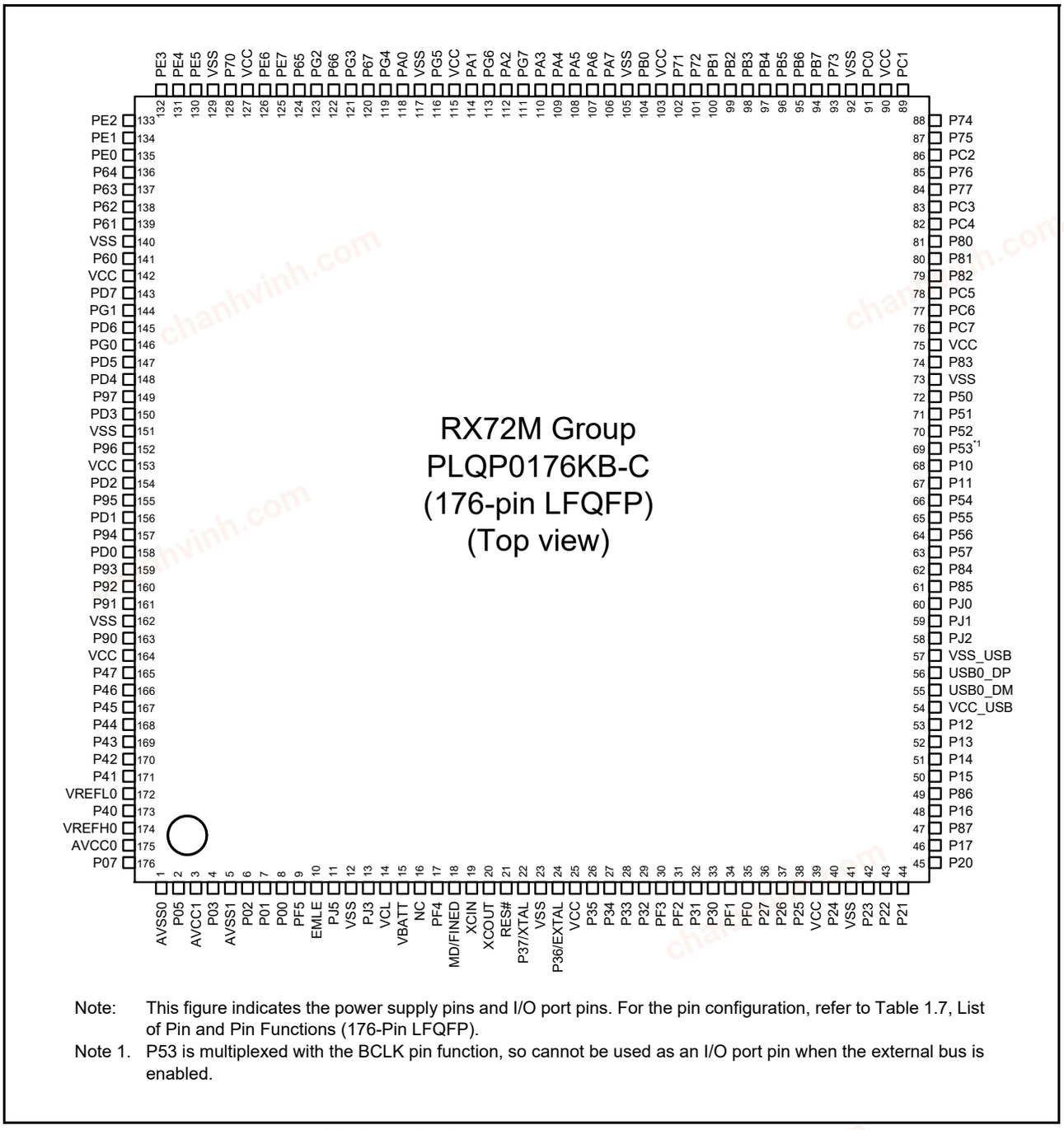
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53*1	9
8	P94	PD1	PD2	VSS								P55	P54	P10	P11	8
7	VSS	P92	PD0	P95								P85	P84	P57	P56	7
6	VCC	P91	P90	P93								PJ1	PJ0	VSS_ USB	USB0_ DP	6
5	P46	P47	P45	P44								PJ2	P12	VCC_ USB	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.6, List of Pin and Pin Functions (176-Pin LFBGA).

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Figure 1.4 Pin Assignment (176-Pin LFBGA)

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Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.7, List of Pin and Pin Functions (176-Pin LFQFP).

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

Figure 1.5 Pin Assignment (176-Pin LFQFP)

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (1/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
A1	NC											
A2	VREFH0											
A3	VREFL0											
A4		P41								IRQ9-DS	AN001	
A5		P92	D18/A18	POE4#		RXD7/ SMISO7/ SSCL7	ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV				AN116	DSMCLK4
A6		PD0	D0[A0/D0]	POE4#	GTIOC1B				LCD_EXTCLK-B	IRQ0	AN108	
A7		PD2	D2[A2/D2]	MTIOC4D/ TIC2	GTIOC0B	MISOC-A/ CRX0	ET1_EXOUT	QIO2-B/ SDHI_D2-B/ MMC_D2-B	LCD_DATA22-B	IRQ2	AN110	
A8	TRDATA5	P96	D22/A22				ET1_ERXD2/ CAT1_ERXD2					
A9		PD3	D3[A3/D3]	MTIOC8D/ TOC2/ POE8#	GTIOC0A	RSPCKC-A	ET1_WOL	QIO3-B/ SDHI_D3-B/ MMC_D3-B	LCD_DATA21-B	IRQ3	AN111	
A10	TRDATA6	PG0	D24				ET1_RX_CLK/ REF50CK1/ CAT1_RX_CLK					
A11		PD7	D7[A7/D7]	MTIC5U/ POE0#		SSLC3-A	ET1_RX_ER/ RMII1_RX_ER/ CAT1_RX_ER	QMI-B/ QIO1-B/ SDHI_D1-B/ MMC_D1-B	LCD_DATA17-B	IRQ7	AN107	
A12		P61	SDCS#/ D0[A0/D0]/ CS1#				ET1_ERXD1/ RMII1_RXD1/ CAT1_ERXD1					
A13		P62	RAS#/ D1[A1/D1]/ CS2#				ET1_ERXD0/ RMII1_RXD0/ CAT1_ERXD0					
A14		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	GTIOC1B	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B		MMC_D5-B	LCD_DATA15-B		ANEX1	
A15		P70	SDCLK				CATLINKACT0					
B1	AVSS0											
B2	AVCC0											
B3		P42								IRQ10-DS	AN002	
B4		P46								IRQ14-DS	AN006	
B5		P91	D17/A17			SCK7	ET1_COL				AN115	DSMDAT5
B6	VCC											

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (2/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
B7		P94	D20/A20				ET1_ERXD0/ RMII1_RXD0/ CAT1_ERXD0					
B8	TRDATA4	P95	D21/A21				ET1_ERXD1/ RMII1_RXD1/ CAT1_ERXD1					
B9		PD4	D4[A4/D4]	MTIOC8B/ POE11#		SSLC0-A	ET1_MDIO/ PMGI1_MDIO	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112	
B10		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#		SSLC2-A	ET1_RX_CLK/ REF50CK1/ CAT1_RX_CLK	QMO-B/ QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106	
B11	VCC											
B12		P63	CAS#/ D2[A2/D2]/ CS3#				ET1_ETXD1/ RMII1_TXD1/ CAT1_ETXD1					
B13		PE2	D10[A10/ D10]/ D2[A2/D2]	MTIOC4A/ PO23/TIC3	GTIOC0B	RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B		MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100	
B14		PE4	D12[A12/ D12]/ D4[A4/D4]	MTIOC4D/ MTIOC1A/ PO28	GTIOC1A	SSLB0-B	ET0_ERXD2/ CAT0_ERXD2		LCD_DATA12-B		AN102	
B15		PE7	D15[A15/ D15]/ D7[A7/D7]	MTIOC6A/ TOC1	GTIOC3A	MISOB-B		SDHI_WP/ MMC_RES#-B	LCD_DATA9-B	IRQ7	AN105	
C1	AVSS1											
C2	AVCC1											
C3		P05				SSILRCK1				IRQ13	DA1	
C4		P44								IRQ12-DS	AN004	
C5	VSS											
C6		P90	D16/A16			TXD7/ SMOSI7/ SSDA7	ET1_RX_DV/ CAT1_RX_DV				AN114	DSMCLK5
C7		PD1	D1[A1/D1]	MTIOC4B/ POE0#	GTIOC1A	MOSIC-A/ CTX0			LCD_DATA23-B	IRQ1	AN109	
C8	VCC											
C9	TRSYNC1	P97	D23/A23				ET1_ERXD3/ CAT1_ERXD3					
C10		P60	CS0#				ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN					

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (3/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
C11		P64	WE#/ D3[A3/D3]/ CS4#				ET1_ETXD0/ RMII1_TXD0/ CAT1_ETXD0					
C12	VSS											
C13		PE5	D13[A13/ D13]/ D5[A5/D5]	MTIOC4C/ MTIOC2B	GTIOC0A	RSPCKB-B	ET0_RX_CLK/ REF50CK0/ CAT0_RX_CLK		LCD_DATA11-B	IRQ5	AN103	
C14		P65	CKE/CS5#									
C15		P66	DQM0/ CS6#	MTIOC7D	GTIOC2B	CTX2						
D1		P45								IRQ13-DS	AN005	
D2		P47								IRQ15-DS	AN007	
D3		P03				SSIDATA1				IRQ11	DA0	
D4		P40								IRQ8-DS	AN000	
D5		P01		TMCI0		RXD6/ SMISO6/ SSCL6/ SSIBCK0	CATLEDERR	QIO3-C		IRQ9	AN119	
D6		P02		TMCI1		SCK6/ SSIBCK1	CATLEDSTER			IRQ10	AN120	
D7		P93	D19/A19	POE0#		CTS7#/ RTS7#/ SS7#	ET1_LINKSTA/ CAT1_LINKSTA				AN117	DSMDAT4
D8	VSS											
D9		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ MTCLKA/ POE10#		SSLC1-A	ET1_MDC/ PMGI1_MDC	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DATA19-B	IRQ5	AN113	
D10	TRDATA7	PG1	D25				ET1_RX_ER/ RMII1_RX_ER/ CAT1_RX_ER					
D11		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	GTIOC2B	SCK12/ SSLB1-B		MMC_D4-B	LCD_DATA16-B		ANEX0	
D12		PE3	D11[A11/ D11]/ D3[A3/D3]	MTIOC4B/ PO26/ TOC3/ POE8#	GTIOC2A	CTS12#/ RTS12#/ SS12#	ET0_ERXD3/ CAT0_ERXD3	MMC_D7-B	LCD_DATA13-B		AN101	
D13	VSS											
D14	TRDATA0	PG2	D26				ET1_TX_CLK/ CAT1_TX_CLK					
D15		P67	DQM1/ CS7#	MTIOC7C	GTIOC1B	CRX2	EPLSOUT1/ CATSYNC1			IRQ15		
E1	VCL											
E2	VSS											

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (4/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
E3		P00		TMRI0		TXD6/ SMOSI6/ SSDA6/ AUDIO_CLK	CATLATCH1	QIO2-C		IRQ8	AN118	
E4		P43								IRQ11-DS	AN003	
E5		P07								IRQ15	ADTRG0#	
E6		PN0					ET1_ETXD2/ CAT1_ETXD2					
E7		PQ0				SCK11	ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV					
E8		PQ1				SMISO11/ SSCL11/ RXD11	ET1_COL					
E9		PQ3				RTS11#/ CTS11#/ SS11#	ET1_TX_ER					
E10		PQ5					ET1_ETXD0/ RMII1_TXD0/ CAT1_ETXD0					
E11		PQ4					ET1_RX_CLK/ REF50CK1/ CAT1_RX_CLK					
E12	VCC											
E13		PE6	D14[A14/ D14]/ D6[A6/D6]	MTIOC6C/ TIC1	GTIOC3B	MOSIB-B		SDHI_CD/ MMC_CD-B	LCD_DATA10-B	IRQ6	AN104	
E14	TRCLK	PG5	D29				ET1_ETXD2/ CAT1_ETXD2					
E15	TRSYNC	PG4	D28				ET1_ETXD1/ RMII1_TXD1/ CAT1_ETXD1					
F1	XCIN											
F2	VBATT											
F3	TRST#	PF4										
F4		PK4			GTADSM0	SSLB1	ET0_ERXD2/ CAT0_ERXD2					
F5		PK5			GTADSM1	SSLB2	ET0_ERXD3/ CAT0_ERXD3					
F6	EMLE											
F7		PK6			GTIOC1A	SSLB3	CATLINKACT0					

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (5/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
F8		PN1					ET1_ETXD3/ CAT1_ETXD3					
F9		PQ6					ET1_ETXD1/ RMII1_TXD1/ CAT1_ETXD1					
F10	VSS											
F11		PM1		TOC3	GTETRGB	SMISO10/ SSCL10/ RXD10	ET1_ERXD1/ RMII1_RXD1/ CAT1_ERXD1	SDHI_CMD-D/QSSL-A				
F12		PA0	DQM2/ BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/ PO16/ CACREF	GTIOC0B	SSLA1-B	ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/ CATLEDRUN		LCD_DATA8-B			
F13	TRDATA1	PG3	D27				ET1_ETXD0/ RMII1_TXD0/ CAT1_ETXD0					
F14	TRDATA2	PG6	D30				ET1_ETXD3/ CAT1_ETXD3					
F15	TRDATA3	PG7	D31				ET1_TX_ER					
G1	XCOUT											
G2	VSS											
G3	VCC											
G4	MD/FINED											
G5		PJ5		POE8#		CTS2#/ RTS2#/ SS2#/ SSIRXD0	EPLSOUT0/ CATSYNC0	QMI-C/ QIO1-C				
G6		PF5	WAIT#			SSILRCK0	CATLATCH0			IRQ4		
G7	RES#											
G8		PQ2				SMOSI11/ SSDA11/ TXD11	ET1_RX_DV/ CAT1_RX_DV					
G9		PN2					ET1_TX_CLK/ CAT1_TX_CLK					
G10	VCC											
G11		PM0		TIC3	GTETRGA	SCK10	ET1_ERXD0/ RMII1_RXD0/ CAT1_ERXD0	SDHI_CLK-D/QSPCLK-A				

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (6/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
G12		PA1	DQM3/A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/ PO17	GTIOC2A	SCK5/ SSLA2-B	ET0_WOL		LCD_DATA7-B	IRQ11		
G13		PA2	A2	MTIOC7A/ PO18	GTIOC1A	RXD5/ SMISO5/ SSCL5/ SSLA3-B	CATLINKACT1		LCD_DATA6-B			
G14		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/ PO19		RXD5/ SMISO5/ SSCL5	ET0_MDIO/ CAT0_MDIO/ PMGI0_MDIO		LCD_DATA5-B	IRQ6-DS		
G15		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/ PO20		TXD5/ SMOSI5/ SSDA5/ SSLA0-B	ET0_MDC/ CAT0_MDC/ CATIRQ/ PMGI0_MDC		LCD_DATA4-B	IRQ5-DS		
H1	XTAL	P37										
H2		P34		MTIOC0A/ TMCI3/ PO12/ POE10#		SCK6/ SCK0	ET0_LINKSTA/ CAT0_LINKSTA			IRQ4		DSMDAT0
H3	UPSEL	P35								NMI		
H4		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/ PO11/ POE4#/ POE11#		RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0		PCKO		IRQ3-DS		DSMCLK0
H5		P32		MTIOC0C/ TIOCC0/ TMO3/ PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#		TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUSEN		VSYNC		IRQ2-DS		
H6	BSCANP											
H7		PJ3	EDACK1	MTIOC3C		CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#/ SSITXD0	ET0_EXOUT/ CATRESTOUT	QMO-C/ QIO0-C				
H8		PQ7					ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN					
H9		PN3					ET1_RX_ER/ RMII1_RX_ER/ CAT1_RX_ER					
H10		P73	CS3#	PO16			ET0_WOL		LCD_EXTCLK-A			

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (7/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
H11		PL0		TIC2	GTETRGA	SCK9/ RSPCKC	ET0_ERXD0/ RMII0_RXD0/ CAT0_ERXD0					
H12	VCC											
H13	VSS											
H14		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/ PO22/ POE10#	GTETRGB	CTS5#/ RTS5#/ SS5#/ MOSIA-B	ET0_EXOUT/ CATRESTOUT		LCD_DATA2-B			
H15		PA5	A5	MTIOC6B/ TIOCB1/ PO21	GTIOC0A	RSPCKA-B	ET0_LINKSTA/ CAT0_LINKSTA		LCD_DATA3-B			
J1	EXTAL	P36										
J2	TDI	PF2				RXD1/ SMISO1/ SSCL1	CATI2CCLK					
J3	TMS	PF3										
J4		P31		MTIOC4D/ TMCI2/ PO9/ RTCIC1		CTS1#/ RTS1#/ SS1#/ SSLB0-A	ET1_MDC/ PMGI1_MDC			IRQ1-DS		
J5		P30		MTIOC4B/ TMRI3/ PO8/ RTCIC0/ POE8#		RXD1/ SMISO1/ SSCL1/ MISOB-A	ET1_MDIO/ PMGI1_MDIO			IRQ0-DS		
J6		PH2			GTETRGC	SMOSI7/ SSDA7/ TXD7/ MISOA	CATI2CDATA					
J7		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/ PO13	GTETRGA	RXD1/ SMISO1/ SSCL1/ SCK3/ CRX1-DS/ SSILRCK1	CATLEDRUN	PIXD0		IRQ5		
J8		P53*1	BCLK									
J9		PK3			GTETRGD	RTS8#/ CTS8#/ SS8#/ SSLB0	ET0_TX_ER					
J10		PL1		TOC2	GTETRGB	SMISO9/ SSCL9/ RXD9/ MOSIC	ET0_ERXD1/ RMII0_RXD1/ CAT0_ERXD1					
J11		PN5					ET1_MDC/ PMGI1_MDC	QSSL-C				
J12		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/ PO25		TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6	ET0_ERXD0/ RMII0_RXD0/ CAT0_ERXD0		LCD_TCON3-B	IRQ4-DS		

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (8/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
J13		P71	A18/CS1#				ET0_MDIO/ CAT0_MDIO/ PMGI0_MDIO					DSMCLK3
J14		PB0	A8	MTIC5W/ TIOCA3/ PO24		RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6	ET0_ERXD1/ RMII0_RXD1/ CAT0_ERXD1		LCD_DATA0-B	IRQ12		
J15		PA7	A7	TIOCB2/ PO23		MISOA-B	ET0_WOL		LCD_DATA1-B			
K1	CLKOUT25M	PH7			GTIOC0B							
K2	CLKOUT	PH6			GTIOC0A	SSLA3	CATLATCH1					
K3		PH4			GTADSM0	SSLA1	CATLEDSTER					
K4		PH5			GTADSM1	SSLA2	CATLATCH0					
K5	TDO	PF0				TXD1/ SMOSI1/ SSDA1	CATI2CDATA					
K6		PH1		TOC0	GTETRGB	SMISO7/ SSCL7/ RXD7/ MOSIA	CATI2CCLK					
K7		P10	ALE	MTIC5W/ TMRI3						IRQ0		
K8		P50	WR0#/ WR#			TXD2/ SMOSI2/ SSDA2/ SSLB1-A	CATLEDERR					
K9		PK1		TOC1	GTETRGB	SMISO8/ SSCL8/ RXD8/ MOSIB	ET0_COL					
K10		PL3			GTETRGD	RTS9#/ CTS9#/ SS9#/ SSLC0	ET0_RX_CLK/ REF50CK0/ CAT0_RX_CLK					
K11		PM2			GTETRGC	SMOSI10/ SSDA10/ TXD10	ET1_ERXD2/ CAT1_ERXD2	SDHI_D0-D/QMO-A/ QIO0-A				
K12	VSS											
K13		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/ PO29/ POE4#		SCK9/ RTS9#/ SCK11	ET0_ETXD0/ RMII0_TXD0/ CAT0_ETXD0		LCD_CLK-B			
K14		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/ PO27/ POE11#		SCK4/ SCK6	ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER		LCD_TCON1-B			

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (9/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
K15		P72	A19/CS2#				ET0_MDC/ CAT0_MDC/ PMGI0_MDC		LCD_DATA23-A			DSMDAT3
L1		PH3			GTETRGD	RTS7#/ CTS7#/ SS7#/ SSLA0	CATLEDERR					
L2		P27	CS7#	MTIOC2B/ TMCI3/ PO7		SCK1/ RSPCKB-A	ET1_WOL /CATIRQ					
L3	TCK	PF1				SCK1						
L4		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/ PO4		SCK3/ USB0_VBUSEN/ SSIBCK1		SDHI_WP/ PIXCLK				
L5	VCC											
L6	CLKOUT25M	PJ2				TXD8/ SMOSI8/ SSDA8/ SSLC3-B			LCD_TCON2-A			
L7	VCC											
L8		P52	RD#			RXD2/ SMISO2/ SSCL2/ SSLB3-A	CATLEDSTER					
L9		P81	EDACK0	MTIOC3D/ PO27	GTIOC0B	SMISO10/ SSCL10/ RXD10	ET0_ETXD0/ RMII0_TXD0/ CAT0_ETXD0/ CATI2CCLK	QIO3-A/ SDHI_CD/ MMC_D3-A	LCD_DATA13-A			
L10		PL7			GTIOC2B		ET0_MDIO/ CAT0_MDIO/ PMGI0_MDIO					
L11		P77	CS7#	PO23		SMOSI11/ SSDA11/ TXD11	ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER	QSPCLK-A/ SDHI_CLK-A/ MMC_CLK-A	LCD_DATA17-A			
L12		PN4					ET1_MDIO/ PMGI1_MDIO	QSPCLK-C				
L13	VCC											
L14		PB2	A10	TIOCC3/ TCLKC/ PO26		CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/ SS6#	ET0_RX_CLK/ REF50CK0/ CAT0_RX_CLK		LCD_TCON2-B			
L15		PB4	A12	TIOCA4/ PO28		CTS9#/ SS9#/ SS11#/ CTS11#/ RTS11#	ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN		LCD_TCON0-B			

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (10/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
M1		P26	CS6#	MTIOC2A/ TMO1/PO6		TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A	ET1_EXOUT/ CATLINKACT1					
M2		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/ PO3	GTIOC0A	TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/ CTX1/ SSIBCK0		SDHI_D1-C/PIXD7				
M3	CLKOUT	P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/ PO5		RXD3/ SMISO3/ SSCL3/ SSIDATA1		SDHI_CD/ HSYNC			ADTRG0#	
M4	VSS											
M5		PJ0		MTIOC6B		SCK8/ SSLC1-B	EPLSOUT0/ CATSYNC0		LCD_DATA0-A			
M6		P84		MTIOC6D			ET1_LINKSTA/ CAT1_LINKSTA		LCD_DATA2-A			
M7	VSS											
M8		P51	WR1#/ BC1#/ WAIT#			SCK2/ SSLB2-A						
M9		P83	EDACK1	MTIOC4C	GTIOC0A	SCK10/ SS10#/ CTS10#	ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV		LCD_DATA8-A			DSMCLK1
M10		PK0		TIC1	GTETRGA	SCK8/ RSPCKB	ET0_MDC/ CAT0_MDC/ PMGI0_MDC					
M11		PL5			GTADSM1	SSLC2	ET0_ETXD1/ RMII0_TXD1/ CAT0_ETXD1					
M12		PL6			GTIOC2A	SSLC3	ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN					
M13		PM7			GTIOC3B		ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV	SDHI_WP				
M14		PC0	A16	MTIOC3C/ TCLKC/ PO17		CTS5#/ RTS5#/ SS5#/ SSLA1-A	ET0_ERXD3/ CAT0_ERXD3			IRQ14		

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (11/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
M15		PB6	A14	MTIOC3D/ TIOCA5/ PO30		RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11	ET0_ETXD1/ RMII0_TXD1/ CAT0_ETXD1					
N1		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	GTIOC1A	SCK0/ USB0_OVRCURB/ AUDIO_CLK		SDHI_D0-C/PIXD6				
N2		PH0		TIC0	GTETRGA	SCK7/ RSPCKA	CATLEDRUN					
N3		P86		MTIOC4D/ TIOCA0	GTIOC2B	SMISO10/ SSCL10/ RXD10	CATLINKACT0	PIXD1				
N4		P85		MTIOC6C/ TIOCC0					LCD_DATA1-A			
N5		P13	WR2#/ BC2#	MTIOC0B/ TIOCA5/ TMO3/ PO13	GTADSM1	TXD2/ SMOSI2/ SSDA2/ SDA0[FM+]			LCD_TCON0-A	IRQ3	ADTRG1#	
N6		PJ1		MTIOC6A		RXD8/ SMISO8/ SSCL8/ SSLC2-B	EPLSOUT1/ CATSYNC1		LCD_TCON3-A			
N7	CLKOUT25M	P56	EDACK1	MTIOC3C/ TIOCA1		SCK7/ RSPCKC-B			LCD_DATA4-A			DSMDAT1
N8	VCC											
N9	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/ PO31/ TOC0/ CACREF	GTIOC3A	TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A	ET0_COL	MMC_D7-A	LCD_DATA9-A	IRQ14		
N10		P80	EDREQ0	MTIOC3B/ PO26		SCK10/ RTS10#	ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/ CATLATCH0	QIO2-A/ SDHI_WP/ MMC_D2-A	LCD_DATA14-A			
N11		PK2			GTETRGC	SMOSI8/ SSDA8/ TXD8/ MISOB	ET0_RX_DV/ CAT0_RX_DV					
N12		P76	CS6#	PO22		SMISO11/ SSCL11/ RXD11	ET0_RX_CLK/ REF50CK0/ CAT0_RX_CLK	QSSL-A/ SDHI_CMD-A/ MMC_CMD-A	LCD_DATA18-A			
N13		PM6			GTIOC3A		ET0_TX_CLK/ CAT0_TX_CLK	SDHI_CD				
N14		PC1	A17	MTIOC3A/ TCLKD/ PO18		SCK5/ SSLA2-A	ET0_ERXD2/ CAT0_ERXD2		LCD_DATA22-A	IRQ12		

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (12/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
N15		PB7	A15	MTIOC3B/ TIOCB5/ PO31		TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11	ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV					
P1		PK7			GTIOC1B		CATLINKACT1					
P2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/ PO15/ POE8#	GTIOC0B	SCK1/ TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0	EPLSOUT0/ CATSYNC0	SDHI_D3-C/PIXD3		IRQ7	ADTRG1#	
P3		P20		MTIOC1A/ TIOCB3/ TMRI0/ PO0		TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SSIRXD0		SDHI_CMD-C/PIXD4		IRQ8		
P4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/ PO15	GTETRGD	CTS1#/ RTS1#/ SS1#/ CTX1/ USB0_OVRCURA			LCD_CLK-A	IRQ4		
P5	VCC_USB											
P6	VSS_USB											
P7		P57				RXD7/ SMISO7/ SSCL7/ SSLC0-B			LCD_DATA3-A			
P8		P11		MTIC5V/ TMCI3		SCK2	EPLSOUT1/ CATSYNC1		LCD_DATA7-A	IRQ1		
P9	VSS											
P10		P82	EDREQ1	MTIOC4A/ PO28	GTIOC2A	SMOSI10/ SSDA10/ TXD10	ET0_ETXD1/ RMII0_TXD1/ CAT0_ETXD1/ CATI2CDATA	MMC_D4-A	LCD_DATA12-A			
P11		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/ PO25/ POE0#	GTETRGC	SCK5/ CTS8#/ SS8#/ SS10#/ CTS10#/ RTS10#/ SSLA0-A	ET0_TX_CLK/ CAT0_TX_CLK/ CATSYNC0	QMI-A/ QIO1-A/ SDHI_D1-A/ MMC_D1-A	LCD_DATA15-A			
P12		PL2			GTETRGC	SMOSI9/ SSDA9/ TXD9/ MISOC	ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER					
P13		PC2	A18	MTIOC4B/ TCLKA/ PO21	GTIOC2B	RXD5/ SMISO5/ SSCL5/ SSLA3-A	ET0_RX_DV/ CAT0_RX_DV	SDHI_D3-A/ MMC_CD-A	LCD_DATA19-A			

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (13/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
P14		PM4			GTADSM0		ET0_ETXD2/ CAT0_ETXD2	SDHI_D2-D/QIO2-A				
P15		PM3			GTETRGD	RTS10#/ CTS10#/ SS10#	ET1_ERXD3/ CAT1_ERXD3	SDHI_D1-D/QMI-A/ QIO1-A				
R1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/ PO1	GTIOC2A	RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXICEN/ SSILRCK0		SDHI_CLK-C/PIXD5		IRQ9		
R2		P87		MTIOC4C/ TIOCA2	GTIOC1B	SMOSI10/ SSDA10/ TXD10	EPLSOUT1/ CATSYNC1	SDHI_D2-C/PIXD2				
R3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/ PO14/ RTCOUT		TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB				IRQ6	ADTRG0#	
R4		P12	WR3#/ BC3#	MTIC5U/ TMCI1	GTADSM0	RXD2/ SMISO2/ SSCL2/ SCL0[FM+]			LCD_TCON1-A	IRQ2		
R5						USB0_DM						
R6						USB0_DP						
R7		P54	D1[A1/D1]/ EDACK0/ ALE	MTIOC4B/ TMCI1		CTS2#/ RTS2#/ SS2#/ MOSIC-B/ CTX1	ET0_LINKSTA/ CAT0_LINKSTA		LCD_DATA6-A			
R8		P55	D0[A0/D0]/ EDREQ0/ WAIT#	MTIOC4D/ TMO3		TXD7/ SMOSI7/ SSDA7/ MISOC-B/ CRX1	ET0_EXOUT		LCD_DATA5-A	IRQ10		
R9		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/ PO30/TIC0	GTIOC3B	RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A	ET0_ETXD3/ CAT0_ETXD3/ CATLATCH1	MMC_D6-A	LCD_DATA10-A	IRQ13		
R10		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/ PO29	GTIOC1A	SCK8/ RTS8#/ SCK10/ RSPCKA-A	ET0_ETXD2/ CAT0_ETXD2	MMC_D5-A	LCD_DATA11-A			
R11		PC3	A19	MTIOC4D/ TCLKB/ PO24	GTIOC1B	TXD5/ SMOSI5/ SSDA5	ET0_TX_ER	QMO-A/ QIO0-A/ SDHI_D0-A/ MMC_D0-A	LCD_DATA16-A			

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Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (14/14)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
R12		PL4			GTADSM0	SSLC1	ET0_ETXD0/ RMII0_TXD0/ CAT0_ETXD0					
R13		P75	CS5#	PO20		SCK11/ RTS11#	ET0_ERXD0/ RMII0_RXD0/ CAT0_ERXD0	SDHI_D2-A/ MMC_RES#-A	LCD_DATA20-A			DSMDAT2
R14		P74	A20/CS4#	PO19		SS11#/ CTS11#	ET0_ERXD1/ RMII0_RXD1/ CAT0_ERXD1		LCD_DATA21-A			DSMCLK2
R15		PM5			GTADSM1		ET0_ETXD3/ CAT0_ETXD3	SDHI_D3-D/QIO3-A				

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (1/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
A1	AVSS0											
A2	AVCC0											
A3	VREFL0											
A4		P42								IRQ10-DS	AN002	
A5		P46								IRQ14-DS	AN006	
A6	VCC											
A7	VSS											
A8		P94	D20/A20				ET1_ERXD0/ RMII1_RXD0/ CAT1_ERXD0					
A9	VCC											
A10	TRSYNC1	P97	D23/A23				ET1_ERXD3/ CAT1_ERXD3					
A11		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#		SSLC2-A	ET1_RX_CLK/ REF50CK1/ CAT1_RX_CLK	QMO-B/ QIO0-B/ SDHI_D0-B/ MMC_D0-B	LCD_DATA18-B	IRQ6	AN106	
A12		P60	CS0#				ET1_TX_EN/ RMII1_TXD_EN/ CAT1_TX_EN					
A13		P63	CAS#/ D2[A2/D2]/ CS3#				ET1_ETXD1/ RMII1_TXD1/ CAT1_ETXD1					
A14		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	GTIOC1B	TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B		MMC_D5-B	LCD_DATA15-B		ANEX1	
A15		PE2	D10[A10/D10]/ D2[A2/D2]	MTIOC4A/ PO23/TIC3	GTIOC0B	RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B		MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100	
B1		P05				SSILRCK1				IRQ13	DA1	
B2		P07								IRQ15	ADTRG0#	
B3		P40								IRQ8-DS	AN000	
B4		P41								IRQ9-DS	AN001	
B5		P47								IRQ15-DS	AN007	
B6		P91	D17/A17			SCK7	ET1_COL				AN115	DSMDAT5
B7		P92	D18/A18	POE4#		RXD7/ SMISO7/ SSCL7	ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV				AN116	DSMCLK4

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (2/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
B8		PD1	D1[A1/D1]	MTIOC4B/ POE0#	GTIOC1A	MOSIC-A/ CTX0			LCD_DATA23-B	IRQ1	AN109	
B9	TRDATA5	P96	D22/A22				ET1_ERXD2/ CAT1_ERXD2					
B10		PD4	D4[A4/D4]	MTIOC8B/ POE11#		SSLC0-A	ET1_MDIO/ PMGI1_MDIO	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112	
B11	TRDATA7	PG1	D25				ET1_RX_ER/ RMII1_RX_ER/ CAT1_RX_ER					
B12	VSS											
B13		P64	WE#/ D3[A3/D3]/ CS4#				ET1_ETXD0/ RMII1_TXD0/ CAT1_ETXD0					
B14		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	GTIOC2B	SCK12/ SSLB1-B		MMC_D4-B	LCD_DATA16-B		ANEX0	
B15		PE3	D11[A11/ D11]/ D3[A3/D3]	MTIOC4B/ PO26/ TOC3/ POE8#	GTIOC2A	CTS12#/ RTS12#/ SS12#	ET0_ERXD3/ CAT0_ERXD3	MMC_D7-B	LCD_DATA13-B		AN101	
C1	AVSS1											
C2	AVCC1											
C3	VREFH0											
C4		P43								IRQ11-DS	AN003	
C5		P45								IRQ13-DS	AN005	
C6		P90	D16/A16			TXD7/ SMOSI7/ SSDA7	ET1_RX_DV/ CAT1_RX_DV				AN114	DSMCLK5
C7		PD0	D0[A0/D0]	POE4#	GTIOC1B				LCD_EXTCLK-B	IRQ0	AN108	
C8		PD2	D2[A2/D2]	MTIOC4D/ TIC2	GTIOC0B	MISOC-A/ CRX0	ET1_EXOUT	QIO2-B/ SDHI_D2-B/ MMC_D2-B	LCD_DATA22-B	IRQ2	AN110	
C9		PD3	D3[A3/D3]	MTIOC8D/ TOC2/ POE8#	GTIOC0A	RSPCKC-A	ET1_WOL	QIO3-B/ SDHI_D3-B/ MMC_D3-B	LCD_DATA21-B	IRQ3	AN111	
C10	TRDATA6	PG0	D24				ET1_RX_CLK/ REF50CK1/ CAT1_RX_CLK					
C11	VCC											
C12		P62	RAS#/ D1[A1/D1]/ CS2#				ET1_ERXD0/ RMII1_RXD0/ CAT1_ERXD0					

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (3/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
C13		PE4	D12[A12/D12]/D4[A4/D4]	MTIOC4D/MTIOC1A/PO28	GTIOC1A	SSLB0-B	ET0_ERXD2/CAT0_ERXD2		LCD_DATA12-B		AN102	
C14	VSS											
C15		P70	SDCLK				CATLINKACT0					
D1		P01		TMCI0		RXD6/SMISO6/SSCL6/SSIBCK0	CATLEDERR			IRQ9	AN119	
D2		P02		TMCI1		SCK6/SSIBCK1	CATLEDSTER			IRQ10	AN120	
D3		P03				SSIDATA1				IRQ11	DA0	
D4		P00		TMRI0		TXD6/SMOSI6/SSDA6/AUDIO_CLK	CATLATCH1			IRQ8	AN118	
D5		P44								IRQ12-DS	AN004	
D6		P93	D19/A19	POE0#		CTS7#/RTS7#/SS7#	ET1_LINKSTA/CAT1_LINKSTA				AN117	DSMDAT4
D7	TRDATA4	P95	D21/A21				ET1_ERXD1/RMII1_RXD1/CAT1_ERXD1					
D8	VSS											
D9		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/MTCLKA/POE10#		SSLC1-A	ET1_MDC/PMGI1_MDC	QSPCLK-B/SDHI_CLK-B/MMC_CLK-B	LCD_DATA19-B	IRQ5	AN113	
D10		PD7	D7[A7/D7]	MTIC5U/POE0#		SSLC3-A	ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER	QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B	LCD_DATA17-B	IRQ7	AN107	
D11		P61	SDCS#/D0[A0/D0]/CS1#				ET1_ERXD1/RMII1_RXD1/CAT1_ERXD1					
D12		PE5	D13[A13/D13]/D5[A5/D5]	MTIOC4C/MTIOC2B	GTIOC0A	RSPCKB-B	ET0_RX_CLK/REF50CK0/CAT0_RX_CLK		LCD_DATA11-B	IRQ5	AN103	
D13	VCC											
D14		PE7	D15[A15/D15]/D7[A7/D7]	MTIOC6A/TOC1	GTIOC3A	MISOB-B		SDHI_WP/MMC_RES#-B	LCD_DATA9-B	IRQ7	AN105	
D15		P65	CKE/CS5#									
E1		PJ5		POE8#		CTS2#/RTS2#/SS2#/SSIRXD0	EPLSOUT0/CATSYNC0					

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (4/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
E2	EMLE											
E3		PF5	WAIT#			SSILRCK0	CATLATCH0			IRQ4		
E4	VSS											
E12		PE6	D14[A14/D14]/D6[A6/D6]	MTIOC6C/TIC1	GTIOC3B	MOSIB-B		SDHI_CD/MMC_CD-B	LCD_DATA10-B	IRQ6	AN104	
E13	TRDATA0	PG2	D26				ET1_TX_CLK/CAT1_TX_CLK					
E14	TRDATA1	PG3	D27				ET1_ETXD0/RMII1_TXD0/CAT1_ETXD0					
E15		P67	DQM1/CS7#	MTIOC7C	GTIOC1B	CRX2	EPLSOUT1/CATSYNC1			IRQ15		
F1	VBATT											
F2	VCL											
F3		PJ3	EDACK1	MTIOC3C		CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#/SSITXD0	ET0_EXOUT/CATRESTOUT					
F4	BSCANP											
F12		P66	DQM0/CS6#	MTIOC7D	GTIOC2B	CTX2						
F13	TRSYNC	PG4	D28				ET1_ETXD1/RMII1_TXD1/CAT1_ETXD1					
F14		PA0	DQM2/BC0#/A0	MTIOC4A/MTIOC6D/TIOCA0/PO16/CACREF	GTIOC0B	SSLA1-B	ET0_TX_EN/RMII0_TXD_EN/CAT0_TX_EN/CATLEDRUN		LCD_DATA8-B			
F15	VSS											
G1	XCIN											
G2	XCOUT											
G3	MD/FINED											
G4	TRST#	PF4										
G12	TRCLK	PG5	D29				ET1_ETXD2/CAT1_ETXD2					
G13	TRDATA2	PG6	D30				ET1_ETXD3/CAT1_ETXD3					

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (5/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
G14		PA1	DQM3/A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/ PO17	GTIOC2A	SCK5/ SSLA2-B	ET0_WOL		LCD_DATA7-B	IRQ11		
G15	VCC											
H1	XTAL	P37										
H2	VSS											
H3	RES#											
H4	UPSEL	P35								NMI		
H12		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/ PO20		TXD5/ SMOSI5/ SSDA5/ SSLA0-B	ET0_MDC/ CAT0_MDC/ CATIRQ/ PMGI0_MDC		LCD_DATA4-B	IRQ5-DS		
H13		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/ PO19		RXD5/ SMISO5/ SSCL5	ET0_MDIO/ CAT0_MDIO/ PMGI0_MDIO		LCD_DATA5-B	IRQ6-DS		
H14		PA2	A2	MTIOC7A/ PO18	GTIOC1A	RXD5/ SMISO5/ SSCL5/ SSLA3-B	CATLINKACT1		LCD_DATA6-B			
H15	TRDATA3	PG7	D31				ET1_TX_ER					
J1	EXTAL	P36										
J2	VCC											
J3		P34		MTIOC0A/ TMCI3/ PO12/ POE10#		SCK6/ SCK0	ET0_LINKSTA/ CAT0_LINKSTA			IRQ4		DSMDAT0
J4	TMS	PF3										
J12		PA5	A5	MTIOC6B/ TIOCB1/ PO21	GTIOC0A	RSPCKA-B	ET0_LINKSTA/ CAT0_LINKSTA		LCD_DATA3-B			
J13	VSS											
J14		PA7	A7	TIOCB2/ PO23		MISOA-B	ET0_WOL		LCD_DATA1-B			
J15		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/ PO22/ POE10#	GTETRGB	CTS5#/ RTS5#/ SS5#/ MOSIA-B	ET0_EXOUT/ CATRESTOUT		LCD_DATA2-B			
K1		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/ PO11/ POE4#/ POE11#		RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0		PCKO		IRQ3-DS		DSMCLK0

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (6/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F					
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
K2		P32		MTIOC0C/ TIOCC0/ TMO3/ PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#		TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VB USEN		VSYNC		IRQ2-DS		
K3	TDI	PF2				RXD1/ SMISO1/ SSCL1	CATI2CCL K					
K4	TCK	PF1				SCK1						
K12		PB2	A10	TIOCC3/ TCLKC/ PO26		CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/ SS6#	ET0_RX_ CLK/ REF50CK 0/ CAT0_RX _CLK		LCD_TCO N2-B			
K13		P71	A18/CS1#				ET0_MDI O/ CAT0_MDI O/ PMGI0_M DIO					DSMCLK3
K14	VCC											
K15		PB0	A8	MTIC5W/ TIOCA3/ PO24		RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6	ET0_ERX D1/ RMII0_RX D1/ CAT0_ER XD1		LCD_DAT A0-B	IRQ12		
L1		P31		MTIOC4D/ TMCI2/ PO9/ RTCIC1		CTS1#/ RTS1#/ SS1#/ SSLB0-A	ET1_MDC/ PMGI1_M DC			IRQ1-DS		
L2		P30		MTIOC4B/ TMRI3/ PO8/ RTCIC0/ POE8#		RXD1/ SMISO1/ SSCL1/ MISOB-A	ET1_MDI O/ PMGI1_M DIO			IRQ0-DS		
L3	TDO	PF0				TXD1/ SMOSI1/ SSDA1	CATI2CDA TA					
L4	CLKOUT	P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/ PO5		RXD3/ SMISO3/ SSCL3/ SSIDATA1		SDHI_CD/ HSYNC			ADTRG0#	
L12		PB6	A14	MTIOC3D/ TIOCA5/ PO30		RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11	ET0_ETX D1/ RMII0_TX D1/ CAT0_ET XD1					
L13		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/ PO27/ POE11#		SCK4/ SCK6	ET0_RX_ ER/ RMII0_RX _ER/ CAT0_RX _ER		LCD_TCO N1-B			
L14		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/ PO25		TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6	ET0_ERX D0/ RMII0_RX D0/ CAT0_ER XD0		LCD_TCO N3-B	IRQ4-DS		

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (7/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
L15		P72	A19/CS2#				ET0_MDC/ CAT0_MDC/ PMGI0_MDC		LCD_DATA23-A			DSMDAT3
M1		P27	CS7#	MTIOC2B/ TMCI3/ PO7		SCK1/ RSPCKB-A	ET1_WOL /CATIRQ					
M2		P26	CS6#	MTIOC2A/ TMO1/PO6		TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A	ET1_EXOUT/ CATLINKACT1					
M3		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/ PO4		SCK3/ USB0_VBUSEN/ SSIBCK1		SDHI_WP/ PIXCLK				
M4		P86		MTIOC4D/ TIOCA0	GTIOC2B	SMISO10/ SSCL10/ RXD10	CATLINKACT0	PIXD1				
M5	CLKOUT25M	PJ2				TXD8/ SMOSI8/ SSDA8/ SSLC3-B			LCD_TCON2-A			
M6		PJ1		MTIOC6A		RXD8/ SMISO8/ SSCL8/ SSLC2-B	EPLSOUT1/ CATSYNC1		LCD_TCON3-A			
M7		P85		MTIOC6C/ TIOCC0					LCD_DATA1-A			
M8		P55	D0[A0/D0]/ EDREQ0/ WAIT#	MTIOC4D/ TMO3		TXD7/ SMOSI7/ SSDA7/ MISOC-B/ CRX1	ET0_EXOUT		LCD_DATA5-A	IRQ10		
M9		P50	WR0#/ WR#			TXD2/ SMOSI2/ SSDA2/ SSLB1-A	CATLEDERR					
M10		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/ PO29	GTIOC1A	SCK8/ RTS8#/ SCK10/ RSPCKA-A	ET0_ETXD2/ CAT0_ETXD2	MMC_D5-A	LCD_DATA11-A			
M11		P81	EDACK0	MTIOC3D/ PO27	GTIOC0B	SMISO10/ SSCL10/ RXD10	ET0_ETXD0/ RMII0_TXD0/ CAT0_ETXD0/ CATI2CCLK	QIO3-A/ SDHI_CD/ MMC_D3-A	LCD_DATA13-A			
M12		P77	CS7#	PO23		SMOSI11/ SSDA11/ TXD11	ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER	QSPCLK-A/ SDHI_CLK-A/ MMC_CLK-A	LCD_DATA17-A			
M13		PB7	A15	MTIOC3B/ TIOCB5/ PO31		TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11	ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV					

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (8/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
M14		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/ PO29/ POE4#		SCK9/ RTS9#/ SCK11	ET0_ETXD0/ RMII0_TXD0/ CAT0_ETXD0		LCD_CLK-B			
M15		PB4	A12	TIOCA4/ PO28		CTS9#/ SS9#/ SS11#/ CTS11#/ RTS11#	ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN		LCD_TCON0-B			
N1	VCC											
N2		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/ PO3	GTIOC0A	TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/ CTX1/ SSIBCK0		SDHI_D1-C/PIXD7				
N3		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	GTIOC1A	SCK0/ USB0_OVRCURB/ AUDIO_CLK		SDHI_D0-C/PIXD6				
N4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/ PO13	GTETRGA	RXD1/ SMISO1/ SSCL1/ SCK3/ CRX1-DS/ SSILRCK1	CATLEDRUN	PIXD0		IRQ5		
N5		P12	WR3#/ BC3#	MTIC5U/ TMCI1	GTADSM0	RXD2/ SMISO2/ SSCL2/ SCL0[FM+]			LCD_TCON1-A	IRQ2		
N6		PJ0		MTIOC6B		SCK8/ SSLC1-B	EPLSOUT0/ CATSYNC0		LCD_DATA0-A			
N7		P84		MTIOC6D			ET1_LINKSTA/ CAT1_LINKSTA		LCD_DATA2-A			
N8		P54	D1[A1/D1]/ EDACK0/ ALE	MTIOC4B/ TMCI1		CTS2#/ RTS2#/ SS2#/ MOSIC-B/ CTX1	ET0_LINKSTA/ CAT0_LINKSTA		LCD_DATA6-A			
N9		P51	WR1#/ BC1#/ WAIT#			SCK2/ SSLB2-A						
N10	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/ PO31/ TOC0/ CACREF	GTIOC3A	TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A	ET0_COL	MMC_D7-A	LCD_DATA9-A	IRQ14		
N11		P82	EDREQ1	MTIOC4A/ PO28	GTIOC2A	SMOSI10/ SSDA10/ TXD10	ET0_ETXD1/ RMII0_TXD1/ CAT0_ETXD1/ CATI2CDATA	MMC_D4-A	LCD_DATA12-A			

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (9/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
N12		PC3	A19	MTIOC4D/ TCLKB/ PO24	GTIOC1B	TXD5/ SMOSI5/ SSDA5	ET0_TX_ER	QMO-A/ QIO0-A/ SDHI_D0-A/ MMC_D0-A	LCD_DATA16-A			
N13		PC0	A16	MTIOC3C/ TCLKC/ PO17		CTS5#/ RTS5#/ SS5#/ SSLA1-A	ET0_ERXD3/ CAT0_ERXD3			IRQ14		
N14		P73	CS3#	PO16			ET0_WOL		LCD_EXTCLK-A			
N15	VSS											
P1	VSS											
P2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/ PO15/ POE8#	GTIOC0B	SCK1/ TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0	EPLSOUT0/ CATSYNC0	SDHI_D3-C/PIXD3		IRQ7	ADTRG1#	
P3		P87		MTIOC4C/ TIOCA2	GTIOC1B	SMOSI10/ SSDA10/ TXD10	EPLSOUT1/ CATSYNC1	SDHI_D2-C/PIXD2				
P4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/ PO15	GTETRGD	CTS1#/ RTS1#/ SS1#/ CTX1/ USB0_OVRCURA			LCD_CLK-A	IRQ4		
P5	VCC_USB											
P6	VSS_USB											
P7		P57				RXD7/ SMISO7/ SSCL7/ SSLC0-B			LCD_DATA3-A			
P8		P10	ALE	MTIC5W/ TMRI3						IRQ0		
P9		P52	RD#			RXD2/ SMISO2/ SSCL2/ SSLB3-A	CATLEDSTER					
P10		P83	EDACK1	MTIOC4C	GTIOC0A	SCK10/ SS10#/ CTS10#	ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV		LCD_DATA8-A			DSMCLK1
P11		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/ PO30/TIC0	GTIOC3B	RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A	ET0_ETXD3/ CAT0_ETXD3/ CATLATCH1	MMC_D6-A	LCD_DATA10-A	IRQ13		
P12		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/ PO25/ POE0#	GTETRGC	SCK5/ CTS8#/ SS8#/ SS10#/ CTS10#/ RTS10#/ SSLA0-A	ET0_TX_CLK/ CAT0_TX_CLK/ CATSYNC0	QMI-A/ QIO1-A/ SDHI_D1-A/ MMC_D1-A	LCD_DATA15-A			

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (10/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
P13		PC2	A18	MTIOC4B/ TCLKA/ PO21	GTIOC2B	RXD5/ SMISO5/ SSCL5/ SSLA3-A	ET0_RX_ DV/ CAT0_RX _DV	SDHI_D3- A/ MMC_CD-A	LCD_DAT A19-A			
P14		P75	CS5#	PO20		SCK11/ RTS11#	ET0_ERX D0/ RMII0_RX D0/ CAT0_ER XD0	SDHI_D2- A/ MMC_RES #-A	LCD_DAT A20-A			DSMDAT2
P15	VCC											
R1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/ PO1	GTIOC2A	RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXI CEN/ SSILRCK0		SDHI_CLK- C/PIXD5		IRQ9		
R2		P20		MTIOC1A/ TIOCB3/ TMRI0/ PO0		TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SSIRXD0		SDHI_CMD -C/PIXD4		IRQ8		
R3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/ PO14/ RTCOUT		TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VB USEN/ USB0_VB US/ USB0_OV RCURB				IRQ6	ADTRG0#	
R4		P13	WR2#/ BC2#	MTIOC0B/ TIOCA5/ TMO3/ PO13	GTADSM1	TXD2/ SMOSI2/ SSDA2/ SDA0[FM+]			LCD_TCO N0-A	IRQ3	ADTRG1#	
R5						USB0_DM						
R6						USB0_DP						
R7	CLKOUT2 5M	P56	EDACK1	MTIOC3C/ TIOCA1		SCK7/ RSPCKC- B			LCD_DAT A4-A			DSMDAT1
R8		P11		MTIC5V/ TMCI3		SCK2	EPLSOUT 1/ CATSYNC 1		LCD_DAT A7-A	IRQ1		
R9		P53*1	BCLK									
R10	VSS											
R11	VCC											
R12		P80	EDREQ0	MTIOC3B/ PO26		SCK10/ RTS10#	ET0_TX_E N/ RMII0_TX D_EN/ CAT0_TX_ EN/ CATLATC H0	QIO2-A/ SDHI_WP/ MMC_D2-A	LCD_DAT A14-A			

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Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (11/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
R13		P76	CS6#	PO22		SMISO11/ SSCL11/ RXD11	ET0_RX_ CLK/ REF50CK 0/ CAT0_RX _CLK	QSSL-A/ SDHI_CMD -A/ MMC_CMD -A	LCD_DAT A18-A			
R14		P74	A20/CS4#	PO19		SS11#/ CTS11#	ET0_ERX D1/ RMII0_RX D1/ CAT0_ER XD1		LCD_DAT A21-A			DSMCLK2
R15		PC1	A17	MTIOC3A/ TCLKD/ PO18		SCK5/ SSLA2-A	ET0_ERX D2/ CAT0_ER XD2		LCD_DAT A22-A	IRQ12		

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (1/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
1	AVSS0											
2		P05				SSILRCK1				IRQ13	DA1	
3	AVCC1											
4		P03				SSIDATA1				IRQ11	DA0	
5	AVSS1											
6		P02		TMCI1		SCK6/ SSIBCK1	CATLEDS TER			IRQ10	AN120	
7		P01		TMCI0		RXD6/ SMISO6/ SSCL6/ SSIBCK0	CATLEDE RR			IRQ9	AN119	
8		P00		TMRI0		TXD6/ SMOSI6/ SSDA6/ AUDIO_CL K	CATLATC H1			IRQ8	AN118	
9		PF5	WAIT#			SSILRCK0	CATLATC H0			IRQ4		
10	EMLE											
11		PJ5		POE8#		CTS2#/ RTS2#/ SS2#/ SSIRXD0	EPLSOUT 0/ CATSYNC 0					
12	VSS											
13		PJ3	EDACK1	MTIOC3C		CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#/ SSITXD0	ET0_EXO UT/ CATREST OUT					
14	VCL											
15	VBATT											
16	NC											
17	TRST#	PF4										
18	MD/FINED											
19	XCIN											
20	XCOUT											
21	RES#											
22	XTAL	P37										
23	VSS											
24	EXTAL	P36										
25	VCC											
26	UPSEL	P35								NMI		
27		P34		MTIOC0A/ TMCI3/ PO12/ POE10#		SCK6/ SCK0	ET0_LINK STA/ CAT0_LIN KSTA			IRQ4		DSMDAT0

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (2/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
28		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/ PO11/ POE4#/ POE11#		RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0		PCKO		IRQ3-DS		DSMCLK0
29		P32		MTIOC0C/ TIOCC0/ TMO3/ PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#		TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUSEN		VSYNC		IRQ2-DS		
30	TMS	PF3										
31	TDI	PF2				RXD1/ SMISO1/ SSCL1	CATI2CCLK					
32		P31		MTIOC4D/ TMCI2/ PO9/ RTCIC1		CTS1#/ RTS1#/ SS1#/ SSLB0-A	ET1_MDC/ PMGI1_MDC			IRQ1-DS		
33		P30		MTIOC4B/ TMRI3/ PO8/ RTCIC0/ POE8#		RXD1/ SMISO1/ SSCL1/ MISOB-A	ET1_MDIO/ PMGI1_MDIO			IRQ0-DS		
34	TCK	PF1				SCK1						
35	TDO	PF0				TXD1/ SMOSI1/ SSDA1	CATI2CDATA					
36		P27	CS7#	MTIOC2B/ TMCI3/ PO7		SCK1/ RSPCKB-A	ET1_WOL/ CATIRQ					
37		P26	CS6#	MTIOC2A/ TMO1/PO6		TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A	ET1_EXOUT/ CATLINKACT1					
38	CLKOUT	P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/ PO5		RXD3/ SMISO3/ SSCL3/ SSIDATA1		SDHI_CD/ HSYNC			ADTRG0#	
39	VCC											
40		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/ PO4		SCK3/ USB0_VBUSEN/ SSIBCK1		SDHI_WP/ PIXCLK				
41	VSS											
42		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/ PO3	GTIOC0A	TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/ CTX1/ SSIBCK0		SDHI_D1-C/PIXD7				

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (3/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
43		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	GTIOC1A	SCK0/ USB0_OVRCURB/ AUDIO_CLK		SDHI_D0-C/PIXD6				
44		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/ PO1	GTIOC2A	RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXICEN/ SSILRCK0		SDHI_CLK-C/PIXD5		IRQ9		
45		P20		MTIOC1A/ TIOCB3/ TMRI0/ PO0		TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SSIRXD0		SDHI_CMD-C/PIXD4		IRQ8		
46		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/ PO15/ POE8#	GTIOC0B	SCK1/ TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0	EPLSOUT0/ CATSYNC0	SDHI_D3-C/PIXD3		IRQ7	ADTRG1#	
47		P87		MTIOC4C/ TIOCA2	GTIOC1B	SMOSI10/ SSDA10/ TXD10	EPLSOUT1/ CATSYNC1	SDHI_D2-C/PIXD2				
48		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/ PO14/ RTCOUT		TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB				IRQ6	ADTRG0#	
49		P86		MTIOC4D/ TIOCA0	GTIOC2B	SMISO10/ SSCL10/ RXD10	CATLINKACT0	PIXD1				
50		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/ PO13	GTETRGA	RXD1/ SMISO1/ SSCL1/ SCK3/ CRX1-DS/ SSILRCK1	CATLEDRUN	PIXD0		IRQ5		
51		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/ PO15	GTETRGD	CTS1#/ RTS1#/ SS1#/ CTX1/ USB0_OVRCURA			LCD_CLK-A	IRQ4		
52		P13	WR2#/ BC2#	MTIOC0B/ TIOCA5/ TMO3/ PO13	GTADSM1	TXD2/ SMOSI2/ SSDA2/ SDA0[FM+]			LCD_TCON0-A	IRQ3	ADTRG1#	
53		P12	WR3#/ BC3#	MTIC5U/ TMCI1	GTADSM0	RXD2/ SMISO2/ SSCL2/ SCL0[FM+]			LCD_TCON1-A	IRQ2		
54	VCC_USB											

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (4/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
55						USB0_DM						
56						USB0_DP						
57	VSS_USB											
58	CLKOUT25M	PJ2				TXD8/ SMOSI8/ SSDA8/ SSLC3-B			LCD_TCON2-A			
59		PJ1		MTIOC6A		RXD8/ SMISO8/ SSCL8/ SSLC2-B	EPLSOUT1/ CATSYNC1		LCD_TCON3-A			
60		PJ0		MTIOC6B		SCK8/ SSLC1-B	EPLSOUT0/ CATSYNC0		LCD_DATA0-A			
61		P85		MTIOC6C/ TIOCC0					LCD_DATA1-A			
62		P84		MTIOC6D			ET1_LINKSTA/ CAT1_LINKSTA		LCD_DATA2-A			
63		P57				RXD7/ SMISO7/ SSCL7/ SSLC0-B			LCD_DATA3-A			
64	CLKOUT25M	P56	EDACK1	MTIOC3C/ TIOCA1		SCK7/ RSPCKC-B			LCD_DATA4-A			DSMDAT1
65		P55	D0[A0/D0]/ EDREQ0/ WAIT#	MTIOC4D/ TMO3		TXD7/ SMOSI7/ SSDA7/ MISOC-B/ CRX1	ET0_EXOUT		LCD_DATA5-A	IRQ10		
66		P54	D1[A1/D1]/ EDACK0/ ALE	MTIOC4B/ TMCI1		CTS2#/ RTS2#/ SS2#/ MOSIC-B/ CTX1	ET0_LINKSTA/ CAT0_LINKSTA		LCD_DATA6-A			
67		P11		MTIC5V/ TMCI3		SCK2	EPLSOUT1/ CATSYNC1		LCD_DATA7-A	IRQ1		
68		P10	ALE	MTIC5W/ TMRI3						IRQ0		
69		P53*1	BCLK									
70		P52	RD#			RXD2/ SMISO2/ SSCL2/ SSLB3-A	CATLEDSTER					
71		P51	WR1#/ BC1#/ WAIT#			SCK2/ SSLB2-A						
72		P50	WR0#/ WR#			TXD2/ SMOSI2/ SSDA2/ SSLB1-A	CATLEDERR					
73	VSS											
74		P83	EDACK1	MTIOC4C	GTIOC0A	SCK10/ SS10#/ CTS10#	ET0_CRS/ RMII0_CRS_DV/ CAT0_RX_DV		LCD_DATA8-A			DSMCLK1

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (5/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
75	VCC											
76	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/ PO31/ TOC0/ CACREF	GTIOC3A	TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A	ET0_COL	MMC_D7-A	LCD_DATA9-A	IRQ14		
77		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/ PO30/TIC0	GTIOC3B	RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A	ET0_ETXD3/ CAT0_ETXD3/ CATLATCH1	MMC_D6-A	LCD_DATA10-A	IRQ13		
78		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/ PO29	GTIOC1A	SCK8/ RTS8#/ SCK10/ RSPCKA-A	ET0_ETXD2/ CAT0_ETXD2	MMC_D5-A	LCD_DATA11-A			
79		P82	EDREQ1	MTIOC4A/ PO28	GTIOC2A	SMOSI10/ SSDA10/ TXD10	ET0_ETXD1/ RMII0_TXD1/ CAT0_ETXD1/ CATI2CDATA	MMC_D4-A	LCD_DATA12-A			
80		P81	EDACK0	MTIOC3D/ PO27	GTIOC0B	SMISO10/ SSCL10/ RXD10	ET0_ETXD0/ RMII0_TXD0/ CAT0_ETXD0/ CATI2CCLK	QIO3-A/ SDHI_CD/ MMC_D3-A	LCD_DATA13-A			
81		P80	EDREQ0	MTIOC3B/ PO26		SCK10/ RTS10#	ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/ CATLATCH0	QIO2-A/ SDHI_WP/ MMC_D2-A	LCD_DATA14-A			
82		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/ PO25/ POE0#	GTETRGC	SCK5/ CTS8#/ SS8#/ SS10#/ CTS10#/ RTS10#/ SSLA0-A	ET0_TX_CLK/ CAT0_TX_CLK/ CATSYNC0	QMI-A/ QIO1-A/ SDHI_D1-A/ MMC_D1-A	LCD_DATA15-A			
83		PC3	A19	MTIOC4D/ TCLKB/ PO24	GTIOC1B	TXD5/ SMOSI5/ SSDA5	ET0_TX_ER	QMO-A/ QIO0-A/ SDHI_D0-A/ MMC_D0-A	LCD_DATA16-A			
84		P77	CS7#	PO23		SMOSI11/ SSDA11/ TXD11	ET0_RX_ER/ RMII0_RX_ER/ CAT0_RX_ER	QSPCLK-A/ SDHI_CLK-A/ MMC_CLK-A	LCD_DATA17-A			
85		P76	CS6#	PO22		SMISO11/ SSCL11/ RXD11	ET0_RX_CLK/ REF50CK0/ CAT0_RX_CLK	QSSL-A/ SDHI_CMD-A/ MMC_CMD-A	LCD_DATA18-A			

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (6/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
86		PC2	A18	MTIOC4B/ TCLKA/ PO21	GTIOC2B	RXD5/ SMISO5/ SSCL5/ SSLA3-A	ET0_RX_ DV/ CAT0_RX _DV	SDHI_D3- A/ MMC_CD-A	LCD_DAT A19-A			
87		P75	CS5#	PO20		SCK11/ RTS11#	ET0_ERX D0/ RMII0_RX D0/ CAT0_ER XD0	SDHI_D2- A/ MMC_RES #-A	LCD_DAT A20-A			DSMDAT2
88		P74	A20/CS4#	PO19		SS11#/ CTS11#	ET0_ERX D1/ RMII0_RX D1/ CAT0_ER XD1		LCD_DAT A21-A			DSMCLK2
89		PC1	A17	MTIOC3A/ TCLKD/ PO18		SCK5/ SSLA2-A	ET0_ERX D2/ CAT0_ER XD2		LCD_DAT A22-A	IRQ12		
90	VCC											
91		PC0	A16	MTIOC3C/ TCLKC/ PO17		CTS5#/ RTS5#/ SS5#/ SSLA1-A	ET0_ERX D3/ CAT0_ER XD3			IRQ14		
92	VSS											
93		P73	CS3#	PO16			ET0_WOL		LCD_EXT CLK-A			
94		PB7	A15	MTIOC3B/ TIOCB5/ PO31		TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11	ET0_CRS/ RMII0_CR S_DV/ CAT0_RX _DV					
95		PB6	A14	MTIOC3D/ TIOCA5/ PO30		RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11	ET0_ETX D1/ RMII0_TX D1/ CAT0_ET XD1					
96		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/ PO29/ POE4#		SCK9/ RTS9#/ SCK11	ET0_ETX D0/ RMII0_TX D0/ CAT0_ET XD0		LCD_CLK-B			
97		PB4	A12	TIOCA4/ PO28		CTS9#/ SS9#/ SS11#/ CTS11#/ RTS11#	ET0_TX_E N/ RMII0_TX D_EN/ CAT0_TX_ EN		LCD_TCO N0-B			
98		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/ PO27/ POE11#		SCK4/ SCK6	ET0_RX_ ER/ RMII0_RX _ER/ CAT0_RX _ER		LCD_TCO N1-B			
99		PB2	A10	TIOCC3/ TCLKC/ PO26		CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/ SS6#	ET0_RX_ CLK/ REF50CK 0/ CAT0_RX _CLK		LCD_TCO N2-B			

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (7/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
100		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/ PO25		TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6	ET0_ERXD0/ RMII0_RXD0/ CAT0_ERXD0		LCD_TCON3-B	IRQ4-DS		
101		P72	A19/CS2#				ET0_MDC/ CAT0_MDC/ PMGI0_MDC		LCD_DATA23-A			DSMDAT3
102		P71	A18/CS1#				ET0_MDIO/ CAT0_MDIO/ PMGI0_MDIO					DSMCLK3
103	VCC											
104		PB0	A8	MTIC5W/ TIOCA3/ PO24		RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6	ET0_ERXD1/ RMII0_RXD1/ CAT0_ERXD1		LCD_DATA0-B	IRQ12		
105	VSS											
106		PA7	A7	TIOCB2/ PO23		MISOA-B	ET0_WOL		LCD_DATA1-B			
107		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/ PO22/ POE10#	GTETRGB	CTS5#/ RTS5#/ SS5#/ MOSIA-B	ET0_EXOUT/ CATRESTOUT		LCD_DATA2-B			
108		PA5	A5	MTIOC6B/ TIOCB1/ PO21	GTIOC0A	RSPCKA-B	ET0_LINKSTA/ CAT0_LINKSTA		LCD_DATA3-B			
109		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/ PO20		TXD5/ SMOSI5/ SSDA5/ SSLA0-B	ET0_MDC/ CAT0_MDC/ CATIRQ/ PMGI0_MDC		LCD_DATA4-B	IRQ5-DS		
110		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/ PO19		RXD5/ SMISO5/ SSCL5	ET0_MDIO/ CAT0_MDIO/ PMGI0_MDIO		LCD_DATA5-B	IRQ6-DS		
111	TRDATA3	PG7	D31				ET1_TX_ER					
112		PA2	A2	MTIOC7A/ PO18	GTIOC1A	RXD5/ SMISO5/ SSCL5/ SSLA3-B	CATLINKACT1		LCD_DATA6-B			
113	TRDATA2	PG6	D30				ET1_ETXD3/ CAT1_ETXD3					
114		PA1	DQM3/A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/ PO17	GTIOC2A	SCK5/ SSLA2-B	ET0_WOL		LCD_DATA7-B	IRQ11		
115	VCC											

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (8/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
116	TRCLK	PG5	D29				ET1_ETXD2/ CAT1_ETXD2					
117	VSS											
118		PA0	DQM2/ BC0#/A0	MTIOC4A/ MTIOC6D/ TIOCA0/ PO16/ CACREF	GTIOC0B	SSLA1-B	ET0_TX_EN/ RMII0_TXD_EN/ CAT0_TX_EN/ CATLEDRUN		LCD_DATA8-B			
119	TRSYNC	PG4	D28				ET1_ETXD1/ RMII1_TXD1/ CAT1_ETXD1					
120		P67	DQM1/ CS7#	MTIOC7C	GTIOC1B	CRX2	EPLSOUT1/ CATSYNC1			IRQ15		
121	TRDATA1	PG3	D27				ET1_ETXD0/ RMII1_TXD0/ CAT1_ETXD0					
122		P66	DQM0/ CS6#	MTIOC7D	GTIOC2B	CTX2						
123	TRDATA0	PG2	D26				ET1_TX_CLK/ CAT1_TX_CLK					
124		P65	CKE/CS5#									
125		PE7	D15[A15/ D15]/ D7[A7/D7]	MTIOC6A/ TOC1	GTIOC3A	MISOB-B		SDHI_WP/ MMC_RES#-B	LCD_DATA9-B	IRQ7	AN105	
126		PE6	D14[A14/ D14]/ D6[A6/D6]	MTIOC6C/ TIC1	GTIOC3B	MOSIB-B		SDHI_CD/ MMC_CD-B	LCD_DATA10-B	IRQ6	AN104	
127	VCC											
128		P70	SDCLK				CATLINKACT0					
129	VSS											
130		PE5	D13[A13/ D13]/ D5[A5/D5]	MTIOC4C/ MTIOC2B	GTIOC0A	RSPCKB-B	ET0_RX_CLK/ REF50CK0/ CAT0_RX_CLK		LCD_DATA11-B	IRQ5	AN103	
131		PE4	D12[A12/ D12]/ D4[A4/D4]	MTIOC4D/ MTIOC1A/ PO28	GTIOC1A	SSLB0-B	ET0_ERXD2/ CAT0_ERXD2		LCD_DATA12-B		AN102	
132		PE3	D11[A11/ D11]/ D3[A3/D3]	MTIOC4B/ PO26/ TOC3/ POE8#	GTIOC2A	CTS12#/ RTS12#/ SS12#	ET0_ERXD3/ CAT0_ERXD3	MMC_D7-B	LCD_DATA13-B		AN101	

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (9/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
133		PE2	D10[A10/D10]/D2[A2/D2]	MTIOC4A/PO23/TIC3	GTIOC0B	RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B		MMC_D6-B	LCD_DATA14-B	IRQ7-DS	AN100	
134		PE1	D9[A9/D9]/D1[A1/D1]	MTIOC4C/MTIOC3B/PO18	GTIOC1B	TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B		MMC_D5-B	LCD_DATA15-B		ANEX1	
135		PE0	D8[A8/D8]/D0[A0/D0]	MTIOC3D	GTIOC2B	SCK12/SSLB1-B		MMC_D4-B	LCD_DATA16-B		ANEX0	
136		P64	WE#/D3[A3/D3]/CS4#				ET1_ETXD0/RMII1_TXD0/CAT1_ETXD0					
137		P63	CAS#/D2[A2/D2]/CS3#				ET1_ETXD1/RMII1_TXD1/CAT1_ETXD1					
138		P62	RAS#/D1[A1/D1]/CS2#				ET1_ERXD0/RMII1_RXD0/CAT1_ERXD0					
139		P61	SDCS#/D0[A0/D0]/CS1#				ET1_ERXD1/RMII1_RXD1/CAT1_ERXD1					
140	VSS											
141		P60	CS0#				ET1_TX_EN/RMII1_TXD_EN/CAT1_TX_EN					
142	VCC											
143		PD7	D7[A7/D7]	MTIC5U/POE0#		SSLC3-A	ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER	QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B	LCD_DATA17-B	IRQ7	AN107	
144	TRDATA7	PG1	D25				ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER					
145		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/POE4#		SSLC2-A	ET1_RX_CLK/REF50CK1/CAT1_RX_CLK	QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B	LCD_DATA18-B	IRQ6	AN106	

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (10/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
146	TRDATA6	PG0	D24				ET1_RX_CLK/ REF50CK1/ CAT1_RX_CLK					
147		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ MTCLKA/ POE10#		SSLC1-A	ET1_MDC/ PMGI1_MDC	QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B	LCD_DATA19-B	IRQ5	AN113	
148		PD4	D4[A4/D4]	MTIOC8B/ POE11#		SSLC0-A	ET1_MDIO/ PMGI1_MDIO	QSSL-B/ SDHI_CMD-B/ MMC_CMD-B	LCD_DATA20-B	IRQ4	AN112	
149	TRSYNC1	P97	D23/A23				ET1_ERXD3/ CAT1_ERXD3					
150		PD3	D3[A3/D3]	MTIOC8D/ TOC2/ POE8#	GTIOC0A	RSPCKC-A	ET1_WOL	QIO3-B/ SDHI_D3-B/ MMC_D3-B	LCD_DATA21-B	IRQ3	AN111	
151	VSS											
152	TRDATA5	P96	D22/A22				ET1_ERXD2/ CAT1_ERXD2					
153	VCC											
154		PD2	D2[A2/D2]	MTIOC4D/ TIC2	GTIOC0B	MISOC-A/ CRX0	ET1_EXOUT	QIO2-B/ SDHI_D2-B/ MMC_D2-B	LCD_DATA22-B	IRQ2	AN110	
155	TRDATA4	P95	D21/A21				ET1_ERXD1/ RMII1_RXD1/ CAT1_ERXD1					
156		PD1	D1[A1/D1]	MTIOC4B/ POE0#	GTIOC1A	MOSIC-A/ CTX0			LCD_DATA23-B	IRQ1	AN109	
157		P94	D20/A20				ET1_ERXD0/ RMII1_RXD0/ CAT1_ERXD0					
158		PD0	D0[A0/D0]	POE4#	GTIOC1B				LCD_EXTCLK-B	IRQ0	AN108	
159		P93	D19/A19	POE0#		CTS7#/ RTS7#/ SS7#	ET1_LINKSTA/ CAT1_LINKSTA				AN117	DSMDAT4
160		P92	D18/A18	POE4#		RXD7/ SMISO7/ SSCL7	ET1_CRS/ RMII1_CRS_DV/ CAT1_RX_DV				AN116	DSMCLK4
161		P91	D17/A17			SCK7	ET1_COL				AN115	DSMDAT5
162	VSS											

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Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (11/11)

Pin Number				Timer		Communication		Memory I/F Camera I/F				
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(GPTW, POEG)	(SCI, RSPI, RIIC, CAN, USB, SSIE)	(ETHERC, ESC, PGMI)	(QSPI, SDHI, MMCIF, PDC)	GLCDC	Interrupt	A/D D/A	DSMIF
163		P90	D16/A16			TXD7/ SMOSI7/ SSDA7	ET1_RX_ DV/ CAT1_RX _DV				AN114	DSMCLK5
164	VCC											
165		P47								IRQ15-DS	AN007	
166		P46								IRQ14-DS	AN006	
167		P45								IRQ13-DS	AN005	
168		P44								IRQ12-DS	AN004	
169		P43								IRQ11-DS	AN003	
170		P42								IRQ10-DS	AN002	
171		P41								IRQ9-DS	AN001	
172	VREFL0											
173		P40								IRQ8-DS	AN000	
174	VREFH0											
175	AVCC0											
176		P07								IRQ15	ADTRG0#	

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

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2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +4.0	V
V_{BATT} power supply voltage		V_{BATT}	–0.3 to +4.0	V
Input voltage (except for ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 0.3 (up to 4.0)	V
Input voltage (ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 4.0 (up to 5.8)	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3 (up to 4.0)	V
Analog power supply voltage		AVCC0, AVCC1*2	–0.3 to +4.0	V
Analog input voltage		V_{AN}	–0.3 to AVCC + 0.3 (up to 4.0)	V
Junction temperature	D version	T_j	–40 to +105	°C
	G version	T_j	–40 to +125	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS. When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

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2.2 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage*1	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
V_{BATT} power supply voltage	V_{BATT}	2.0	—	3.6	V
USB power supply voltage	VCC_USB	—	VCC	—	V
	VSS_USB	—	0	—	V
Analog power supply voltage*1, *2	AVCC0	—	VCC	—	V
	AVSS0	—	0	—	V
	AVCC1	—	VCC	—	V
	AVSS1	—	0	—	V
	VREFH0	2.7	—	AVCC0	V
	VREFL0	—	0	—	V
Input voltage (except for 5 V tolerant ports, except for ports 03, 05 and 40 to 47)*3	V_{in}	–0.3	—	VCC + 0.3	V
Input voltage (ports 03, 05 and 40 to 47)	V_{in}	–0.3	—	AVCC + 0.3	V
Input voltage (5V tolerant ports 11 to 17, ports 20 and 21, ports 30 to 33, port 67, and ports C0 to C3)*4	V_{in}	–0.3	—	VCC + 3.6 (up to 5.5)	V
Input voltage (5V tolerant port 07)	V_{in}	–0.3	—	AVCC + 3.6 (up to 5.5)	V
Operating temperature (D version)	T_{opr}	–40	—	85	°C
Operating temperature (G version)	T_{opr}	–40	—	105	°C

Note 1. Comply with the following potential condition: VCC = AVCC0 = AVCC1 = VCC_USB
Note 2. For details, refer to section 58.6.11, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.
Note 3. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.
Note 4. For P32, P31, and P30, input as follows when the V_{BATT} power supply is selected.
V_{in} Min. = –0.3, Max. = V_{BATT} + 0.3 (V_{BATT} = 2.0 to 3.6 V)

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance to stabilize the internal voltage	C_{VCL}	0.22 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor whose nominal capacitance is 0.22 µF and a capacitance tolerance is ±30% or better.

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2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1, MTU input pin*1, POE input pin*1, TPU input pin*1, TMR input pin*1, CMTW input pin*1, SCI input pin*1, CAN input pin*1, CAC input pin*1, ADTRG# input pin*1, QSPI input pin*1, SSIE input pin*1, DSMIF input pin*1, GPTW input pin*1, POEG input pin*1, ESC input pin (except for MII pin)*1, RES#, NMI, TCK	V_{IH}	VCC × 0.8	—	—	V	
		V_{IL}	—	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	—		
		V_{IL}	—	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Ports for 5 V tolerant*2	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		
	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	—	V	
	EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SDHI input pin, MMC input pin, PDC input pin, PMGI input pin		VCC × 0.8	—	—		
	ETHERC input pin, ESC input pin (MII pin)		2.3	—	—		
	D0 to D31		VCC × 0.7	—	—		
	RIIC (SMBus)		2.1	—	—		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	—	—	VCC × 0.1	V	
	EXTAL, RSPI input pin, ETHERC input pin, EXDMAC input pin, WAIT#, SDHI input pin, MMC input pin, PDC input pin, PMGI input pin, ESC input pin (MII pin)		—	—	VCC × 0.2		
	D0 to D31		—	—	VCC × 0.3		
	RIIC (SMBus)		—	—	0.8		

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. Ports 07, 11 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.
Note 3. For P32, P31, and P30, input as follows when the V_{BATT} power supply is selected.
V_{IH} Min. = V_{BATT} × 0.8, V_{IL} Max. = V_{BATT} × 0.2 (V_{BATT} = 2.0 to 3.6 V)

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Table 2.5 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins and ETHERC output pin)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC output pin		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC output pin (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC output pin	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V_{in} = 0 V V_{in} = 5.5 V
Input pull-up resistor current	Other than P35	I_p	–300	—	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input pull-down resistor current	EMLE, BSCANP	I_p	10	—	300	µA	V_{in} = VCC
Input capacitance	All input pins (except for ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM)	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	Ports 03, 05, 12, 13, 16, 17, 20, 21, EMLE, BSCANP, USB0_DP, and USB0_DM		—	—	16		
Output voltage of the VCL pin		V_{CL}	—	1.18	—	V	

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when V_{in} = 0 V.

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Table 2.6 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item				Symbol	D version		G version		Unit	Test Conditions
					Typ.	Max.	Typ.	Max.		
Supply current *1	High-speed operating mode	Full operation*2		I_{CC}*3	—	261	—	319	mA	ICLK = 240 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 60 MHz, FCLK = 60 MHz, BCLK = 120 MHz, BCLK pin = 60 MHz
		Normal operation	Peripheral module clocks are supplied *4		61	—	61	—		
			Peripheral module clocks are stopped *4, *5		30	—	30	—		
		Core Mark	Peripheral module clocks are stopped *4, *5		37	—	37	—		
		Sleep mode: Peripheral module clocks are supplied*4			42	144	42	196		
		All module clock stop mode (reference value)			14	115	14	167		
		Increased by BGO operation*8	Reading from the code flash memory while the data flash memory is being programmed		6	—	6	—		
			Reading from the code flash memory while the code flash memory is being programmed		7	—	7	—		
		Increased by Trusted Secure IP operation			—	15	—	15		
	Low-speed operating mode 1: Peripheral module clocks are stopped*4				4.2	—	4.2	—		All clocks 1 MHz
	Low-speed operating mode 2: Peripheral module clocks are stopped*4				4.2	—	4.2	—		All clocks 32.768 kHz
	Software standby mode				3.95	107	3.95	155		
	Deep software standby mode	Power is supplied to the standby RAM and USB resume detecting unit (USB0 only)			15.5	70	15.5	98	μA	
		Power is not supplied to the standby RAM and USB resume detecting unit (USB0 only)	Low power consumption function of the power-on reset circuit is disabled*6		11.5	42	11.5	58		
			Low power consumption function of the power-on reset circuit is enabled*7		4.9	32	4.9	47		
		Increase current by operating RTC	When a low C_L crystal is in use		1	—	1	—		
			When a standard C_L crystal is in use		2	—	2	—		
	When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function)		When a low C_L crystal is in use		0.9	—	0.9	—		V_{BATT} = 2.0 V, VCC = 0 V
					1.6	—	1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
			When a standard C_L crystal is in use		1.7	—	1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
					3.3	—	3.3	—		V_{BATT} = 3.3 V, VCC = 0 V
	Inrush current on returning from deep software standby mode		Inrush current*9	I_{RUSH}	—	211	—	211	mA	

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied.
Note 3. I_{CC} depends on the f (ICLK) as follows.
(when ICLK : PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 2 : 1 and EXTAL = 12 MHz)

- D version
  I_{CC} max. = 0.77 × f + 74 (full operation in high-speed operating mode)
  I_{CC} typ. = 0.22 × f + 7 (normal operation in high-speed operating mode)
  I_{CC} typ. = 0.50 × f + 3.7 (ICLK 1 MHz max) (low-speed operating mode 1)
  I_{CC} max. = 0.29 × f + 74 (sleep mode)

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- G version
  I_{CC} max. = 0.89 × f + 105 (full operation in high-speed operating mode)
  I_{CC} typ. = 0.22 × f + 7 (normal operation in high-speed operating mode)
  I_{CC} typ. = 0.50 × f + 3.7 (ICLK 1 MHz max) (low-speed operating mode 1)
  I_{CC} max. = 0.37 × f + 105 (sleep mode)

Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:
ICLK = 240 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = BCLK pin = 3.75 MHz (divided by 64).
Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.
Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.
Note 8. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.
Note 9. Reference value

Table 2.7 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	D version			G version			Unit	Test Conditions
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Analog power supply current*1, *3	During 12-bit A/D conversion (unit 0)		AI_{CC}	—	0.8	1	—	0.8	1	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with channel-dedicated sample-and-hold circuits (3 channels)			—	1.7	2.5	—	1.7	2.5	mA	IAVCC0_AD + SH
	During 12-bit A/D conversion (unit 1)			—	0.6	1	—	0.6	1	mA	IAVCC1_AD
	During 12-bit A/D conversion (unit 1) + temperature sensor			—	0.7	1.1	—	0.7	1.1	mA	IAVCC1_AD + TEMP
	During D/A conversion (2 channels)	Unbuffered output		—	0.25	0.4	—	0.25	0.4	mA	IAVCC1_DA
		Buffered output		—	0.75	1.1	—	0.75	1.1	mA	
	Waiting for A/D, D/A, and temperature sensor conversion (all units)			—	0.9	1.4	—	0.9	1.4	mA	IAVCC0 + IAVCC1
	A/D, D/A, and temperature sensor are in standby mode (all units)			—	1.4	6.7	—	1.4	9.0	µA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)		AI_{REFH}	—	38	60	—	38	60	µA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.5	—	0.07	0.6	µA	IVREFH0
	12-bit A/D converter in module stop mode (unit 0)			—	0.07	0.4	—	0.07	0.5	µA	IVREFH0
USB operating current	Low speed	USB0	$I_{CCUSBLS}$	—	3.7	6.5	—	3.7	6.5	mA	VCC_USB
	Full speed	USB0	$I_{CCUSBFS}$	—	4.2	10	—	4.2	10	mA	VCC_USB
RAM retension voltage			V_{RAM}	2.7	—	—	2.7	—	—	V	
VCC rising gradient			SrVCC	8.4	—	20000	8.4	—	20000	µs/V	
VCC falling gradient*2			SfVCC	8.4	—	—	8.4	—	—	µs/V	

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D converter (unit 1) and D/A converter.
Note 2. This applies when V_{BATT} is used.
Note 3. Supply current values are measured when all output pins are unloaded.

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Table 2.8 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}	—	—	3.8	mA
	All output pins*3	High-speed interface high-drive	I_{OL}	—	—	7.5	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}	—	—	7.6	mA
	All output pins*3	High-speed interface high-drive	I_{OL}	—	—	15	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–3.8	mA
	All output pins*3	High-speed interface high-drive	I_{OH}	—	—	–7.5	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–7.6	mA
	All output pins*3	High-speed interface high-drive	I_{OH}	—	—	–15	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the MCU's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

Table 2.9 Thermal Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Thermal resistance	176-pin LFQFP (PLQP0176KB-C)	θ_{ja}	31.5	°C/W	JESD51-2 and JESD51-7 compliant
	224-pin LFBGA (PLBG0224GA-A)		23.1		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		30.5		
	176-pin LFQFP (PLQP0176KB-C)	Ψ_{jt}	0.4	°C/W	JESD51-2 and JESD51-7 compliant
	224-pin LFBGA (PLBG0224GA-A)		0.2		JESD51-2 and JESD51-9 compliant
	176-pin LFBGA (PLBG0176GA-A)		0.3		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

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2.4 AC Characteristics

Table 2.10 Operating Frequency (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	—	—	240	MHz
	Peripheral module clock (PCLKA)		—	—	120	
	Peripheral module clock (PCLKB)		—	—	60	
	Peripheral module clock (PCLKC)		—	—	60	
	Peripheral module clock (PCLKD)		—	—	60	
	Flash-IF clock (FCLK)		—*1	—	60	
	External bus clock (BCLK)		—	—	120	
	BCLK pin output		—	—	80	
	SDRAM clock (SDCLK)		—	—	80	
	SDCLK pin output		—	—	80	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

Table 2.11 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKA)		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKC)*1		—	—	1	
	Peripheral module clock (PCLKD)*1		—	—	1	
	Flash-IF clock (FCLK)		—	—	1	
	External bus clock (BCLK)		—	—	1	
	BCLK pin output		—	—	1	
	SDRAM clock (SDCLK)		—	—	1	
	SDCLK pin output		—	—	1	

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

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Table 2.12 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	32	—	264	kHz
	Peripheral module clock (PCLKA)		—	—	264	
	Peripheral module clock (PCLKB)		—	—	264	
	Peripheral module clock (PCLKC)*1		—	—	264	
	Peripheral module clock (PCLKD)*1		—	—	264	
	Flash-IF clock (FCLK)		32	—	264	
	External bus clock (BCLK)		—	—	264	
	BCLK pin output		—	—	264	
	SDRAM clock (SDCLK)		—	—	264	
	SDCLK pin output		—	—	264	

Note 1. The 12-bit A/D converter cannot be used.

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2.4.1 Reset Timing

Table 2.13 Reset Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	1	—	—	ms	Figure 2.1
	Deep software standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.2
	Software standby mode, low-speed operating mode 2	t_{RESWS}	0.3	—	—	ms	
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Waiting time after release from the RES# pin reset		t_{RESWT}	54	—	55	t_{Lcyc}	Figure 2.1
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	100	—	108	t_{Lcyc}	

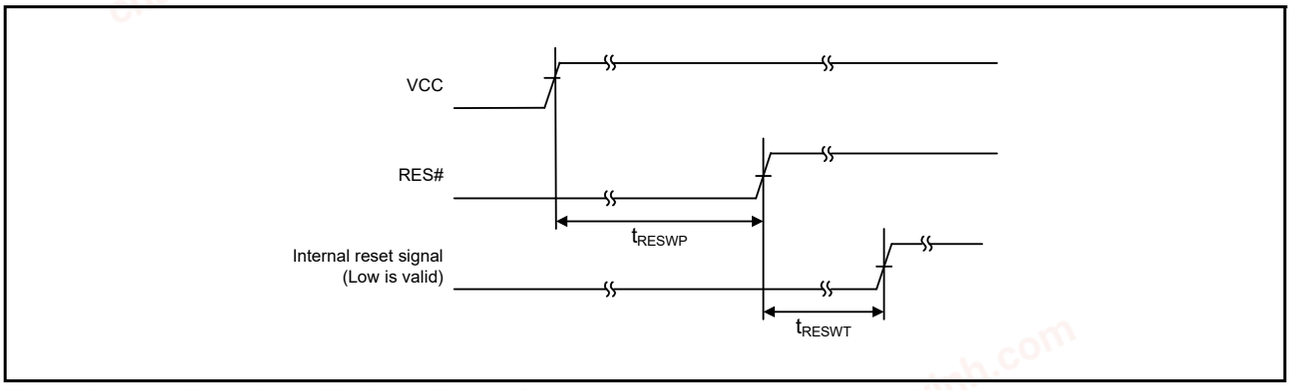


Figure 2.1 Reset Input Timing at Power-On

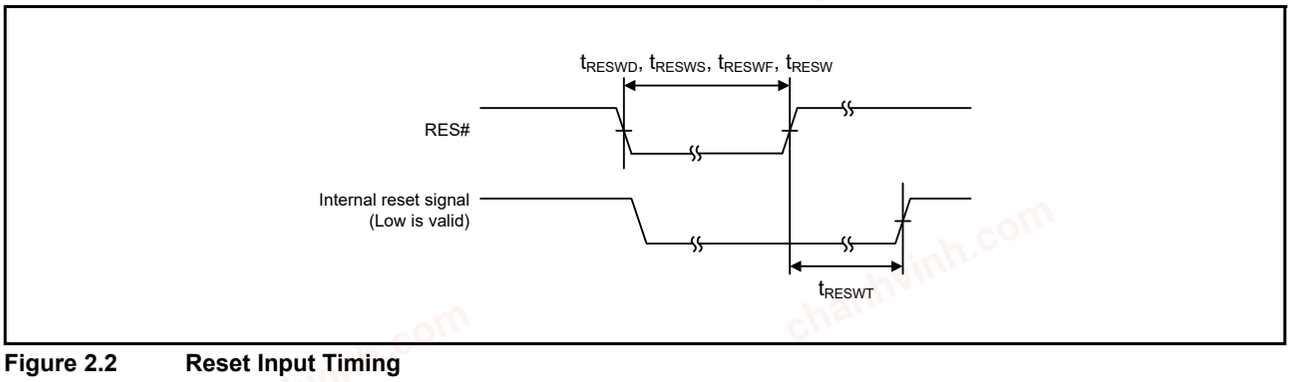


Figure 2.2 Reset Input Timing

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2.4.2 Clock Timing

Table 2.14 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	t_{Bcyc}	12.5	—	—	ns	Figure 2.3
BCLK pin output high pulse width	t_{CH}	3.25	—	—	ns	
BCLK pin output low pulse width	t_{CL}	3.25	—	—	ns	
BCLK pin output rising time	t_{Cr}	—	—	3	ns	
BCLK pin output falling time	t_{Cf}	—	—	3	ns	
SDCLK pin output cycle time	t_{Bcyc}	12.5	—	—	ns	
SDCLK pin output high pulse width	t_{CH}	3.25	—	—	ns	
SDCLK pin output low pulse width	t_{CL}	3.25	—	—	ns	
SDCLK pin output rising time	t_{Cr}	—	—	3	ns	
SDCLK pin output falling time	t_{Cf}	—	—	3	ns	

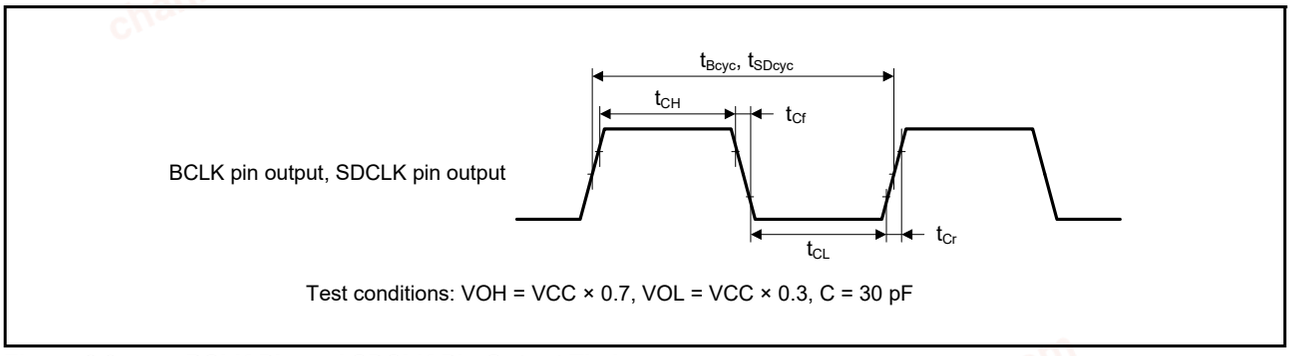


Figure 2.3 BCLK Pin and SDCLK Pin Output Timing

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Table 2.15 EXTAL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	f_{EXMAIN} ≤ 24 MHz			f_{EXMAIN} > 24 MHz			Unit	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	33.33	—	—	ns	Figure 2.4
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	—	—	30	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	13.33	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	13.33	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	—	—	5	ns	

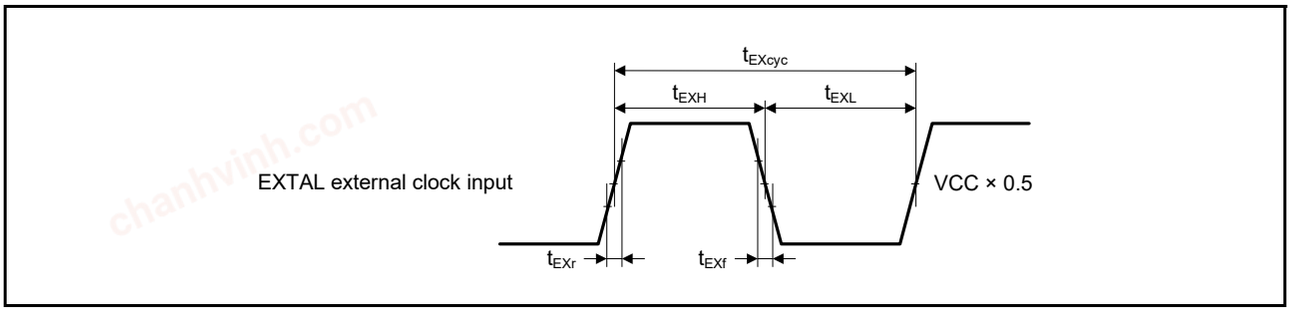


Figure 2.4 EXTAL External Clock Input Timing

Table 2.16 Main Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 2.5
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / f_{LOCO}

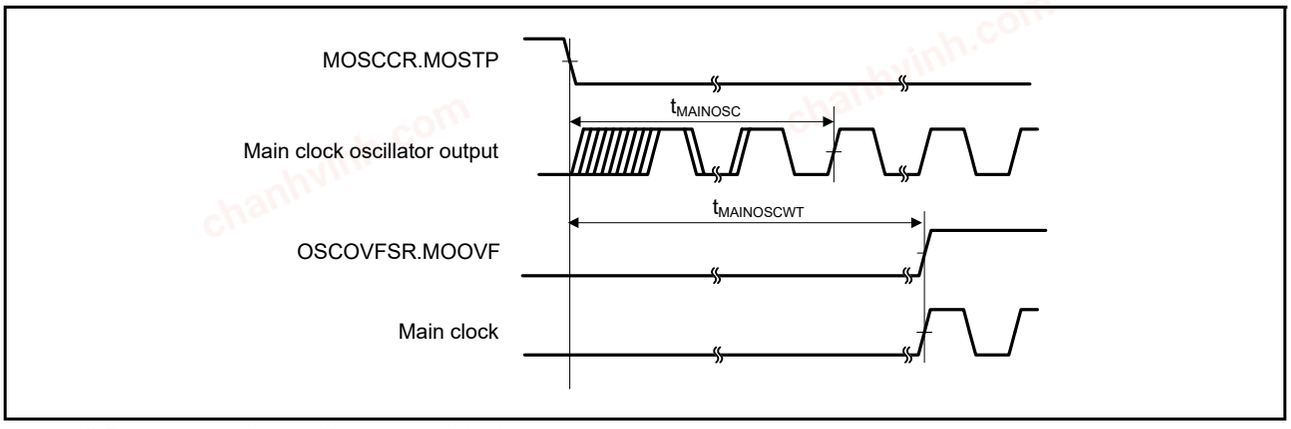


Figure 2.5 Main Clock Oscillation Start Timing

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Table 2.17 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.63	4.16	3.78	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	44	µs	Figure 2.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	9.26	8.33	7.57	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 2.7

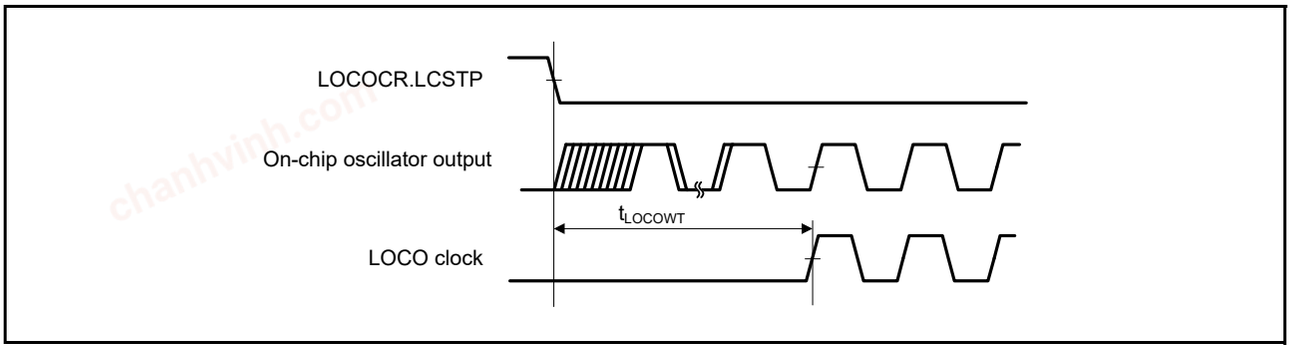


Figure 2.6 LOCO Clock Oscillation Start Timing

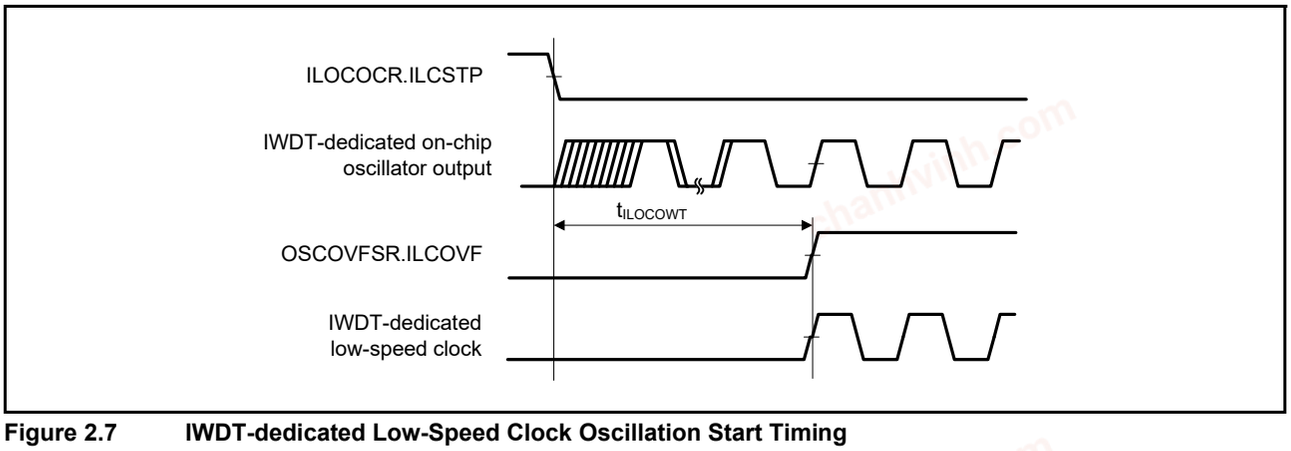


Figure 2.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

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Table 2.18 HOCO Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	–20°C ≤ T_a ≤ 105°C
		17.56	18	18.44	MHz	
		19.52	20	20.48	MHz	
		15.52	16	16.48	MHz	–40°C ≤ T_a < –20°C
		17.46	18	18.54	MHz	
		19.4	20	20.6	MHz	
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	µs	Figure 2.8
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	µs	Figure 2.9

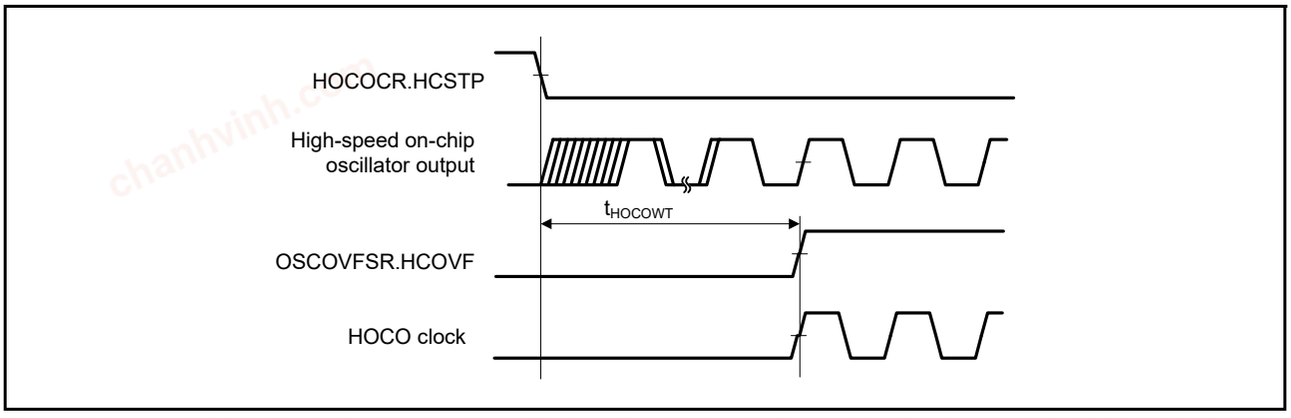


Figure 2.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

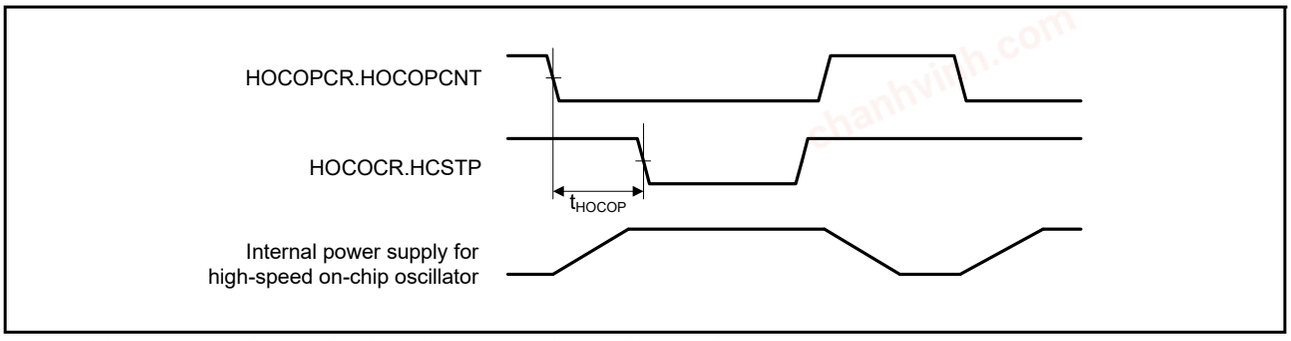


Figure 2.9 High-Speed On-Chip Oscillator Power Supply Control Timing

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Table 2.19 PLL/PPLL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL/PPLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL/PPLL clock oscillation stabilization wait time	t_{PLLWT}	—	259	320	µs	Figure 2.10

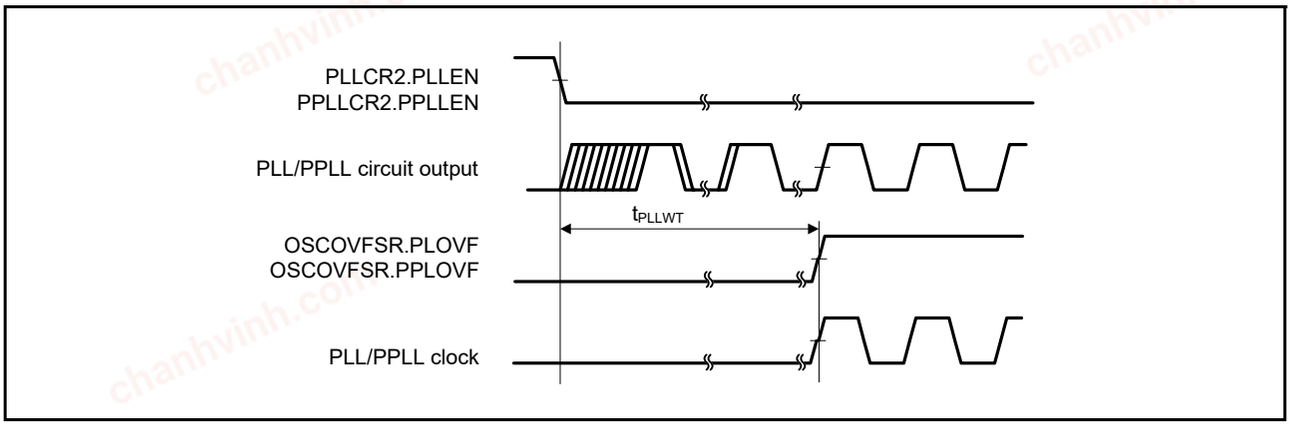


Figure 2.10 PLL/PPLL Clock Oscillation Start Timing

Table 2.20 Sub-Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time	t_{SUBOSC}	—	—	*1	s	Figure 2.11
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	*2	s	

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the SOSCWTCR.SSTS[7:0] bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.
$t_{SUBOSCWT}$ = [(SSTS[7:0] bits × 16384) + 10] / f_{LOCO}

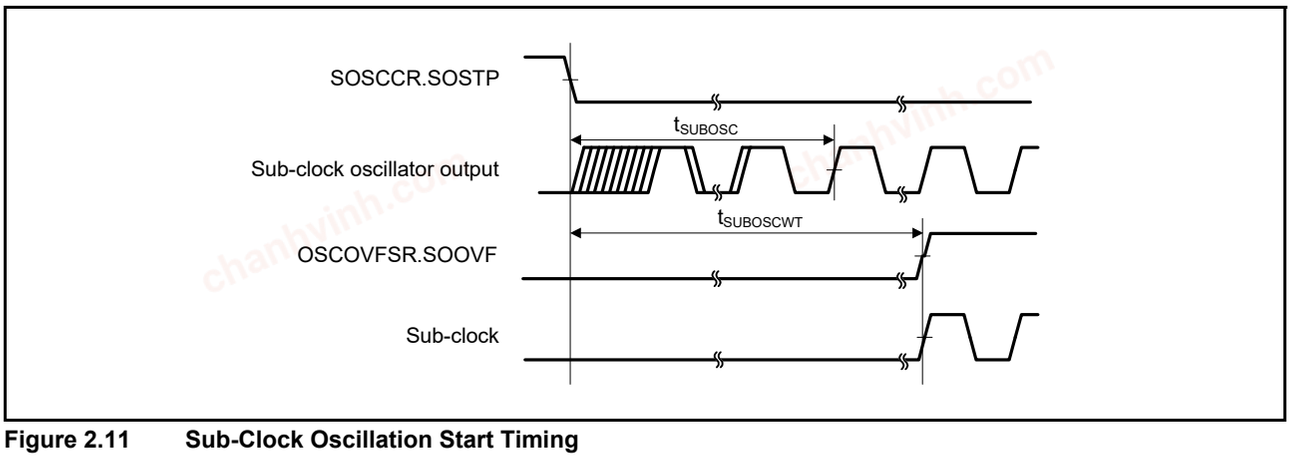


Figure 2.11 Sub-Clock Oscillation Start Timing

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Table 2.21 CLKOUT Pin Output Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CLKOUT pin output cycle time	t_{Ccyc}	25	—	—	ns	Figure 2.12 t_{Ccyc} = 25 ns
CLKOUT pin output high pulse width*1	t_{CH}	5	—	—	ns	
CLKOUT pin output low pulse width*1	t_{CL}	5	—	—	ns	
CLKOUT pin output rising time	t_{Cr}	—	—	5	ns	
CLKOUT pin output falling time	t_{Cf}	—	—	5	ns	

Note 1. If the main clock oscillator is selected by the CLKOUT output source select bit (CKOCR.CKOSEL[2:0]) and the external clock input is selected by the main clock oscillator switching bit (MOFCR.MOSEL), the pulse width depends on the input clock wave form.

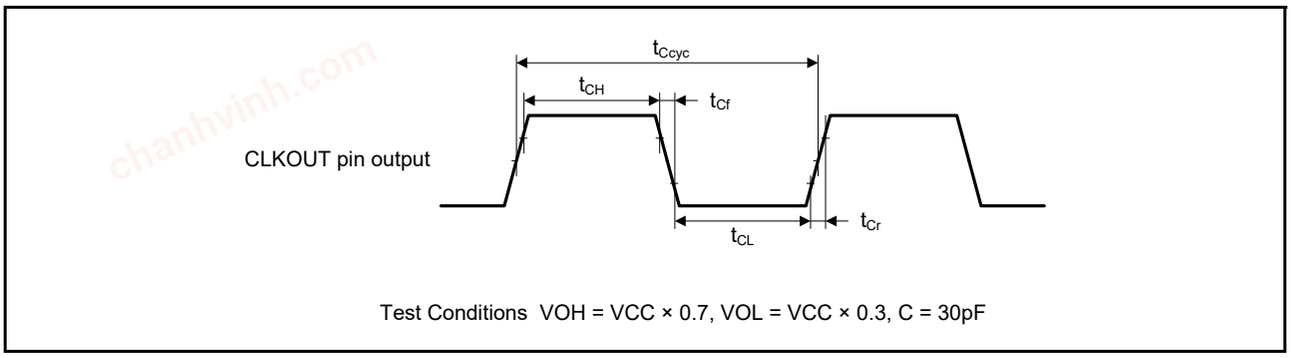


Figure 2.12 CLKOUT Pin Output Timing

Table 2.22 CLKOUT25M Pin Output Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$,
High-speed interface high-drive is selected by the driving ability control register

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CLKOUT25M pin output cycle time	t_{Ccyc}	—	40	—	ns	Figure 2.13
CLKOUT25M pin output high pulse width	t_{CH}	13	—	—	ns	
CLKOUT25M pin output low pulse width	t_{CL}	13	—	—	ns	
CLKOUT25M pin output rising time	t_{Cr}	—	—	3	ns	
CLKOUT25M pin output falling time	t_{Cf}	—	—	3	ns	

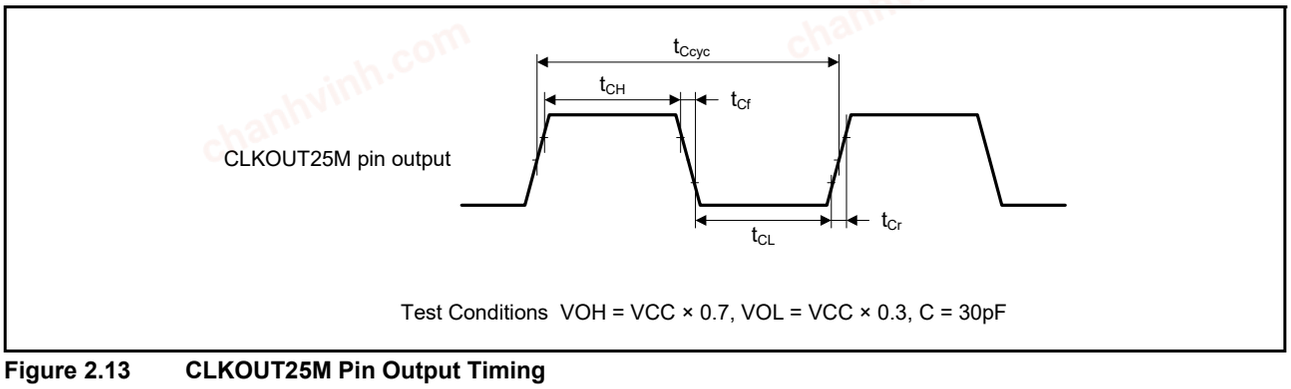


Figure 2.13 CLKOUT25M Pin Output Timing

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2.4.3 Timing of Recovery from Low Power Consumption Modes

Table 2.23 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time from software standby mode *1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	{(MSTS[7:0] bit × 32) + 76} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{MAIN}	µs	Figure 2.14
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			{(MSTS[7:0] bit × 32) + 138} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Sub-clock oscillator operating		t_{SBYSC}			{(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10 / f_{FCLK}	100 + 4 / f_{ICLK} + 2n / f_{SUE}		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	100 + 7 / f_{ICLK} + 2n / f_{HOCO}		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	100 + 7 / f_{ICLK} + 2n / f_{LOCO}		

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when f_{ICLK}:f_{FCLK} = 1:1, 2:1, or 4:1.

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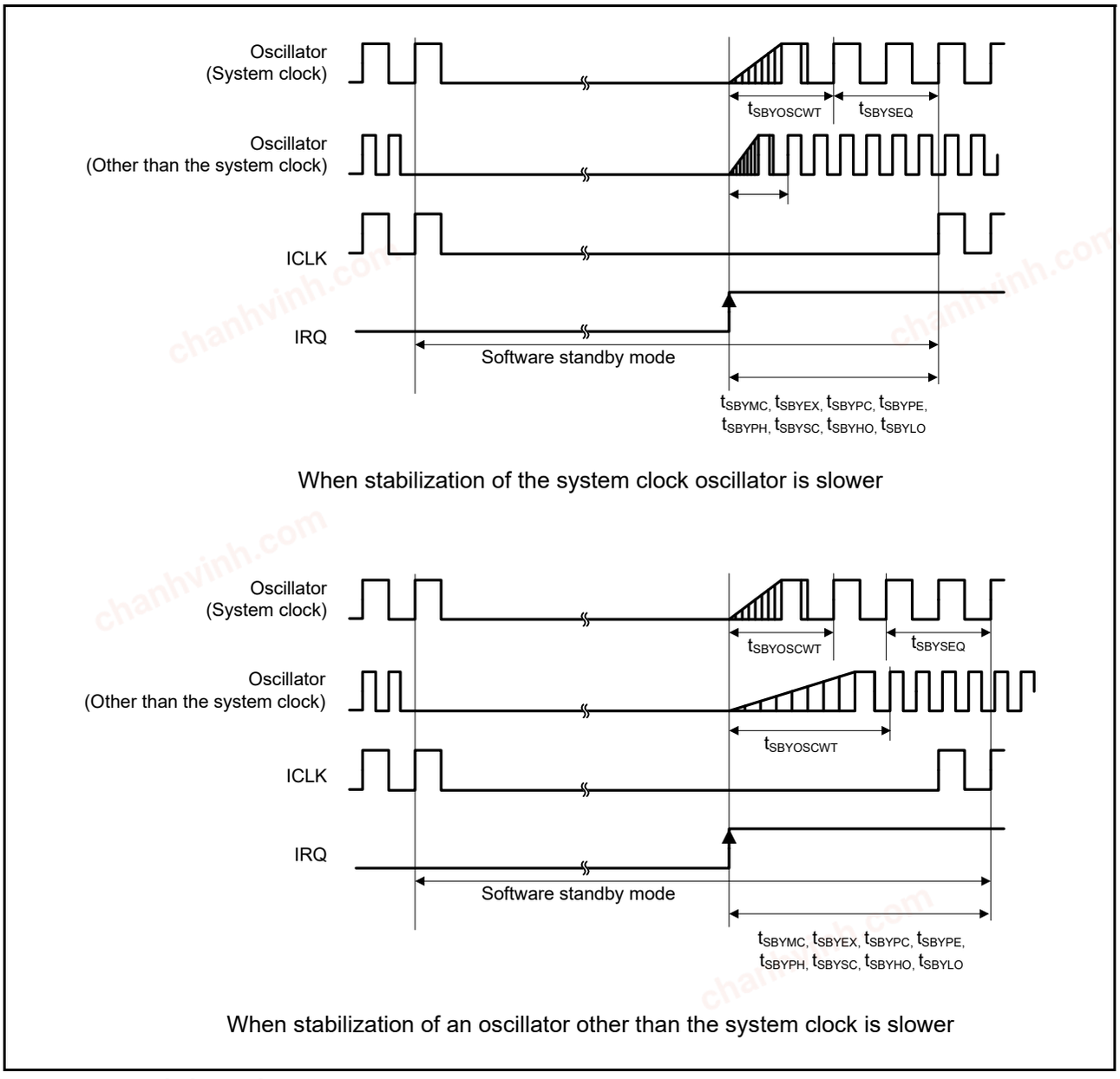


Figure 2.14 Software Standby Mode Recovery Timing

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Table 2.24 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 2.15
Wait time after recovery from deep software standby mode	t_{DSBYWT}	23	—	24	t_{Lcyc}	

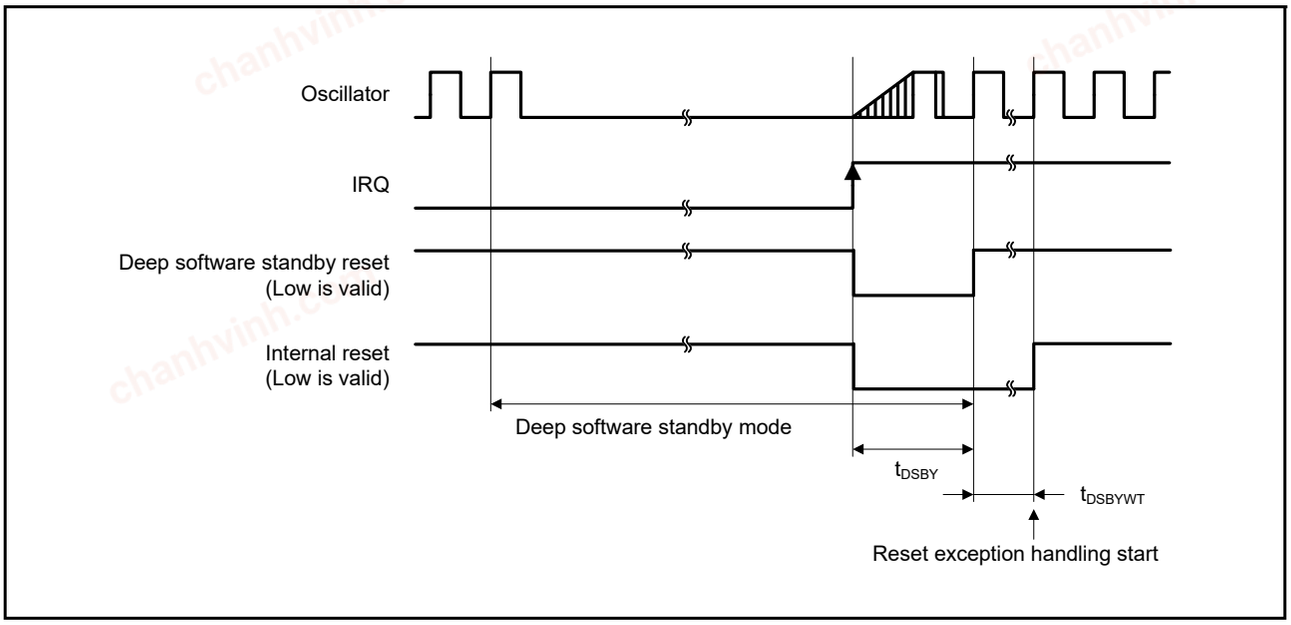


Figure 2.15 Deep Software Standby Mode Recovery Timing

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2.4.4 Control Signal Timing

Table 2.25 Control Signal Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 2.16
		t_{PBcyc} × 2	—	—	ns	t_{PBcyc} × 2 > 200 ns, Figure 2.16
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 2.17
		t_{PBcyc} × 2	—	—	ns	t_{PBcyc} × 2 > 200 ns, Figure 2.17

Note 1. t_{PBcyc}: PCLKB cycle

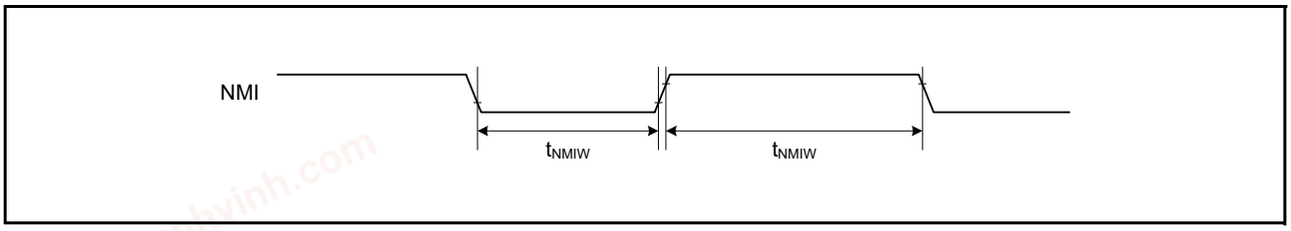


Figure 2.16 NMI Interrupt Input Timing

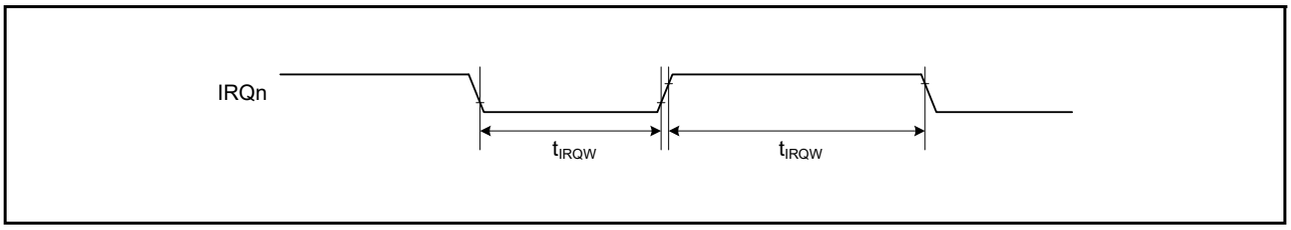


Figure 2.17 IRQ Interrupt Input Timing

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2.4.5 Bus Timing

Table 2.26 Bus Timing

Conditions 1: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Conditions 2: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, 60 MHz < BCLK = SDCLK ≤ 80 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5,
C = 15 pF for the SDCLK pin, C = 30 pF for other pins.

To control the drive capacity when using the SDRAM: set the PFBCR3.SDCLKDRV bit in external bus control register 1 to 1 to select the drive capacity of the SDCLK pin, and set the SDRAM pins other than the SDCLK pin as high-speed-interface driving outputs.

Item	Symbol	Conditions 1		Conditions 2		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
Address delay time	t_{AD}	—	12.5	—	12.5	ns	Figure 2.18 to Figure 2.23
Byte control delay time	t_{BCD}	—	12.5	—	12.5	ns	
CS# delay time	t_{CSD}	—	12.5	—	12.5	ns	
ALE delay time	t_{ALED}	—	12.5	—	12.5	ns	
RD# delay time	t_{RSD}	—	12.5	—	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
WR# delay time	t_{WRD}	—	12.5	—	12.5	ns	
Write data delay time	t_{WDD}	—	12.5	—	12.5	ns	
Write data hold time	t_{WDH}	0	—	0	—	ns	
WAIT# setup time	t_{WTS}	12.5	—	12.5	—	ns	Figure 2.24
WAIT# hold time	t_{WTH}	0	—	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	12.5	1	10.0	ns	Figure 2.25
CS# delay time 2 (SDRAM)	t_{CSD2}	1	12.5	1	10.0	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	12.5	1	10.0	ns	
CKE delay time (SDRAM)	t_{CKED}	1	12.5	1	10.0	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	10	—	6.0	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	12.5	—	10.0	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	12.5	1	10.0	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	12.5	1	10.0	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	12.5	1	10.0	ns	

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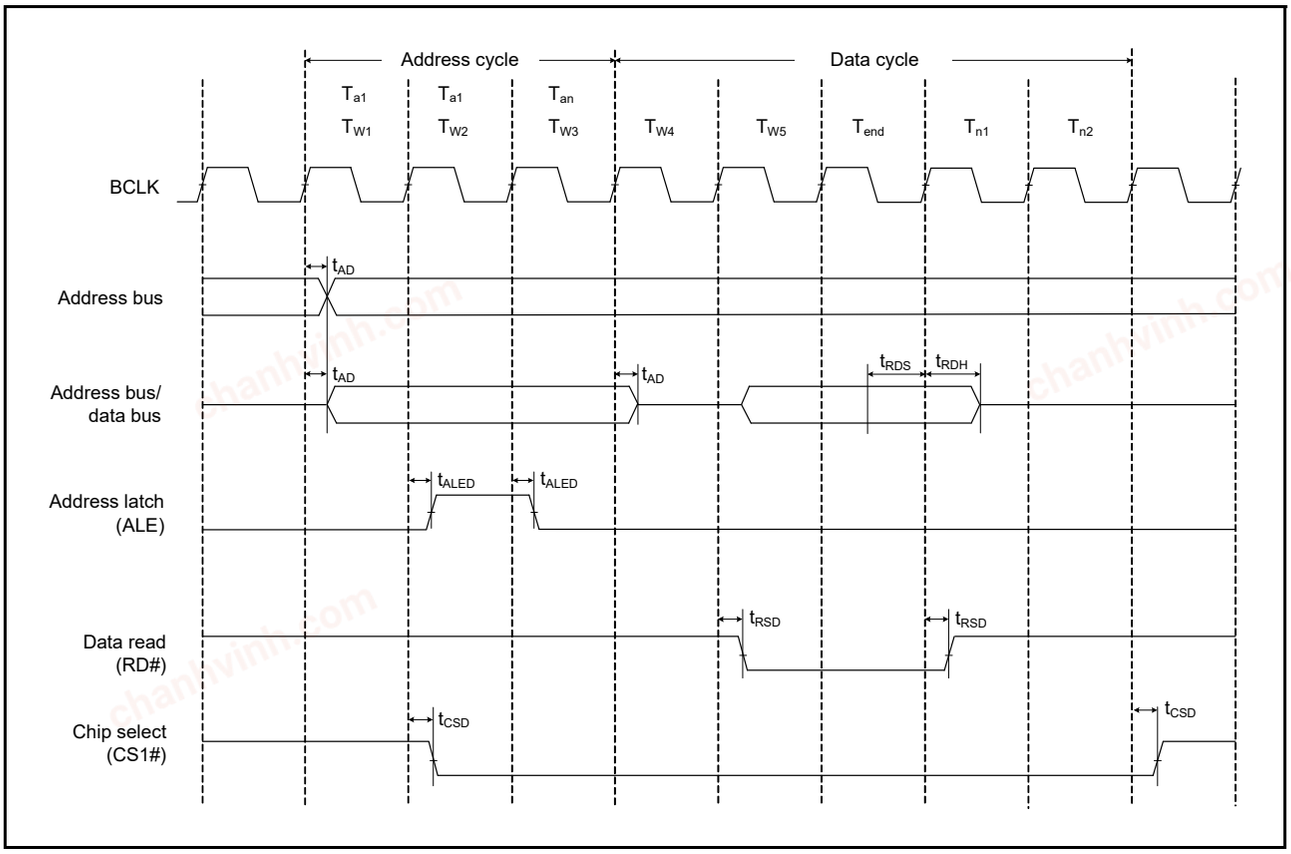


Figure 2.18 Address/Data Multiplexed Bus Read Access Timing

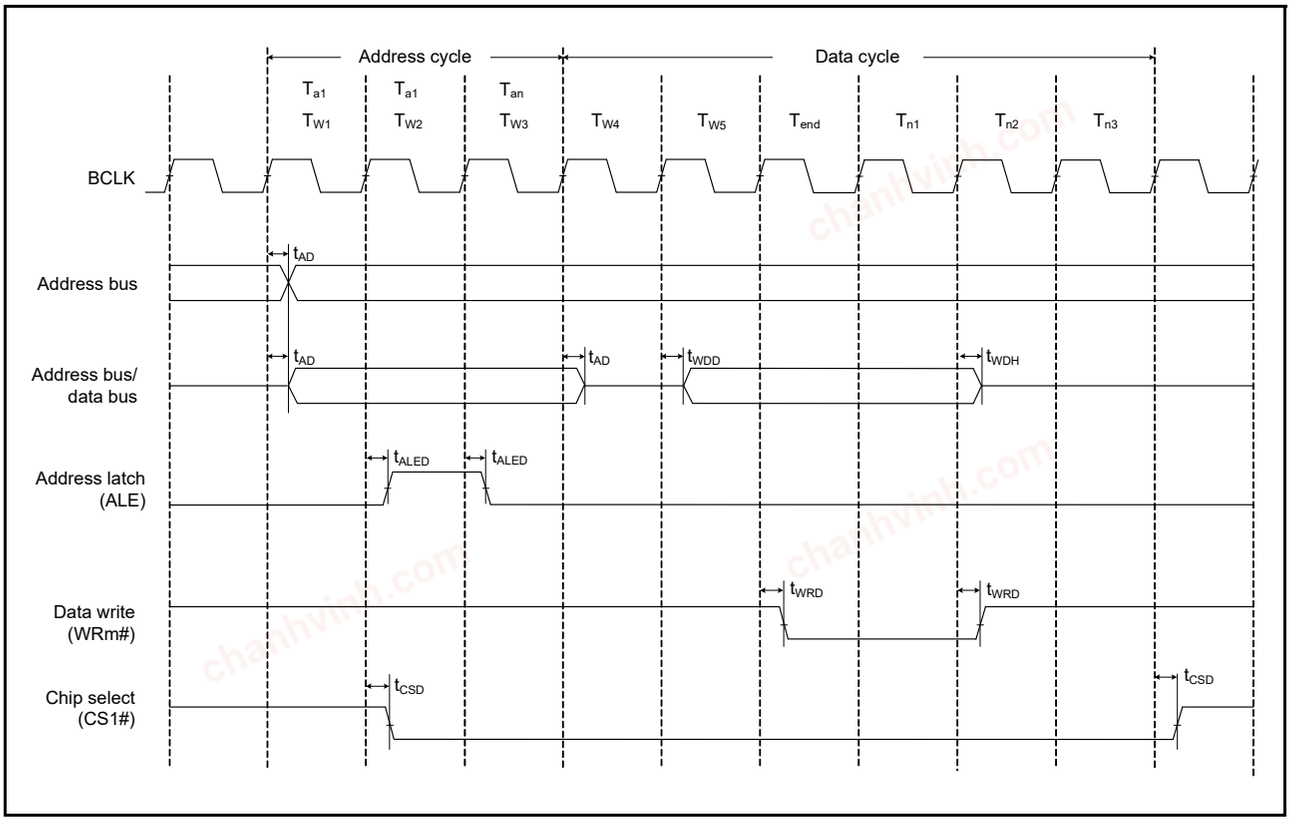


Figure 2.19 Address/Data Multiplexed Bus Write Access Timing

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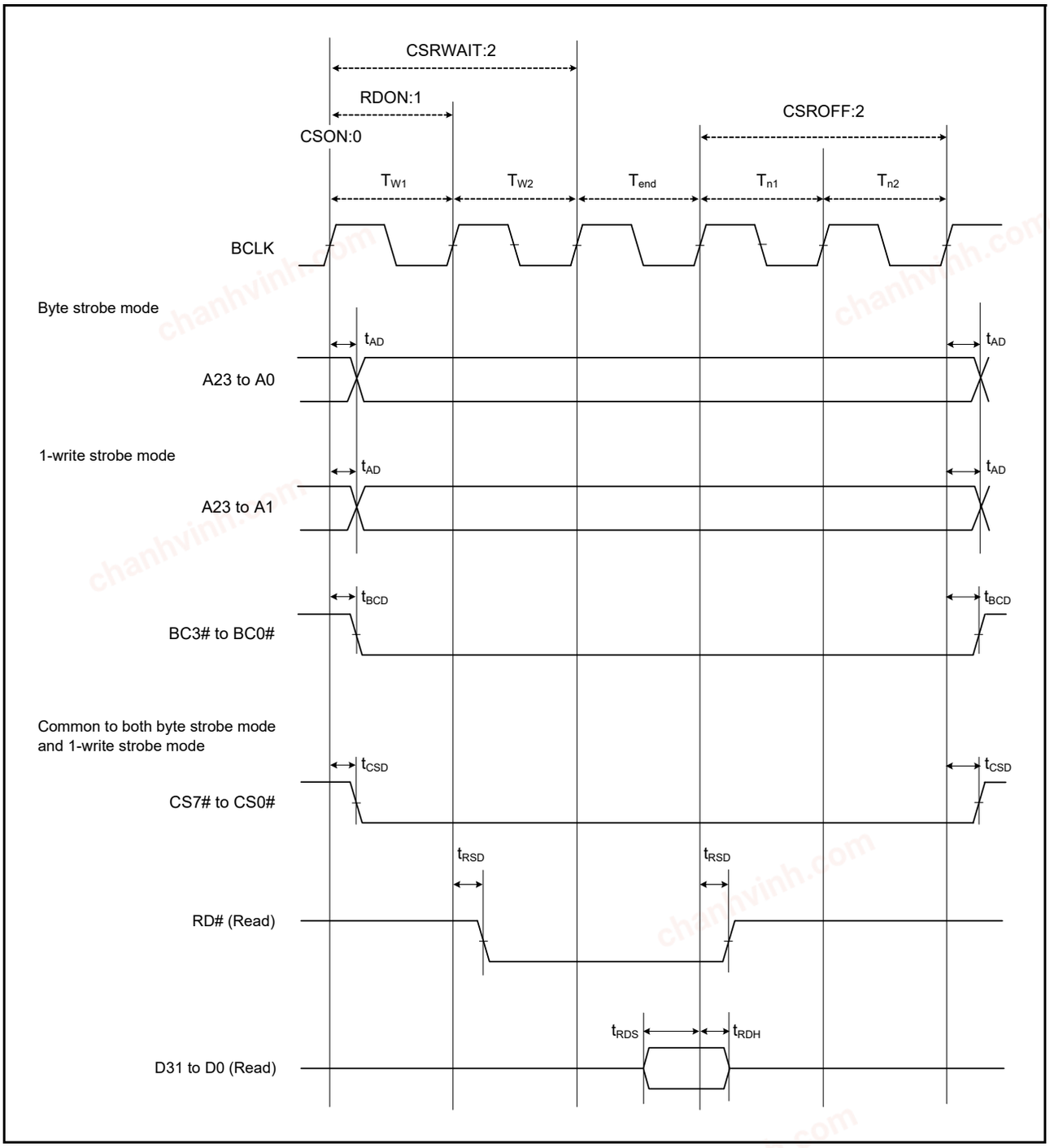
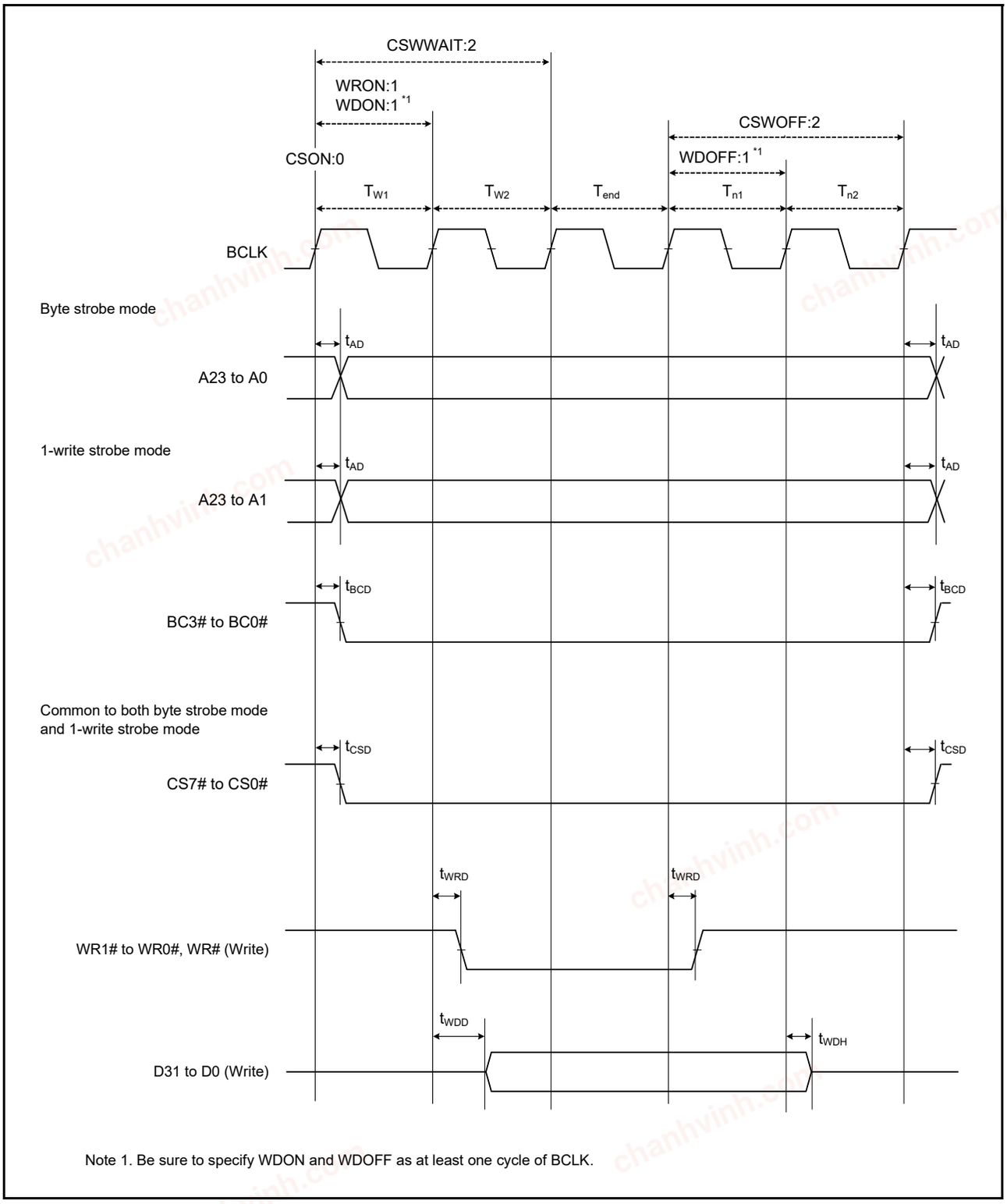


Figure 2.20 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

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Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.21 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

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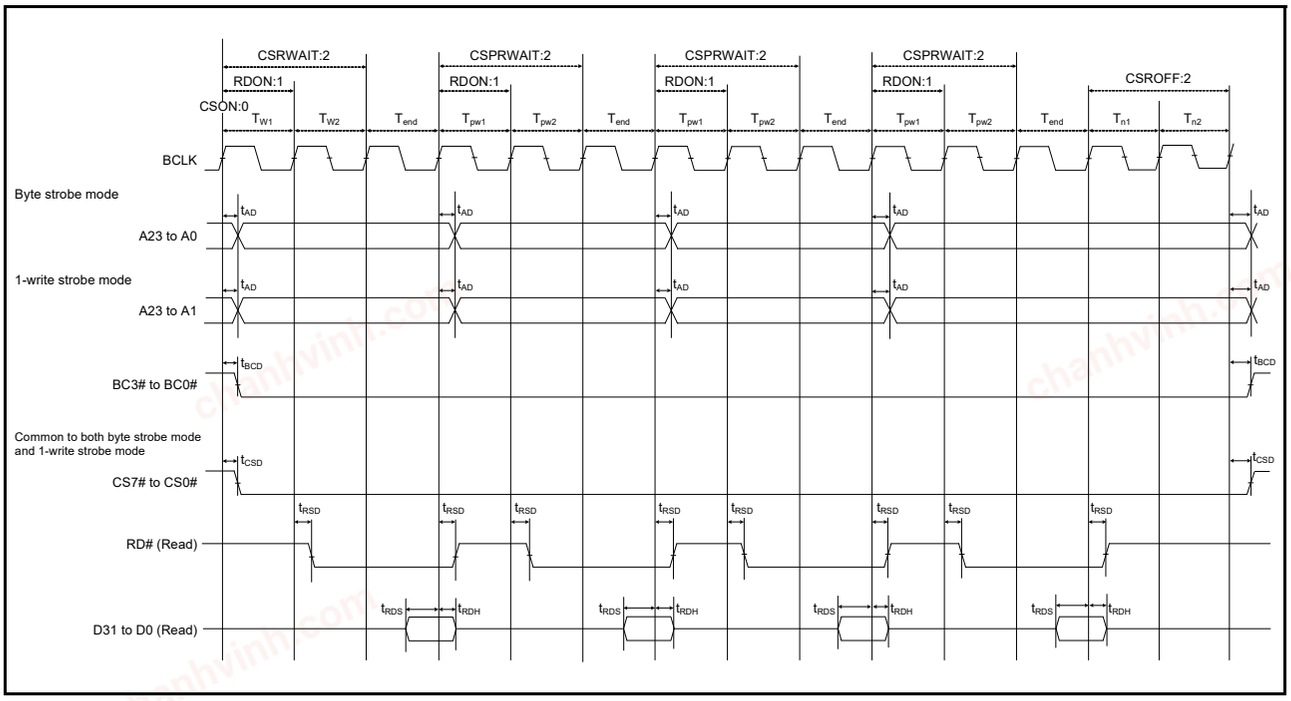
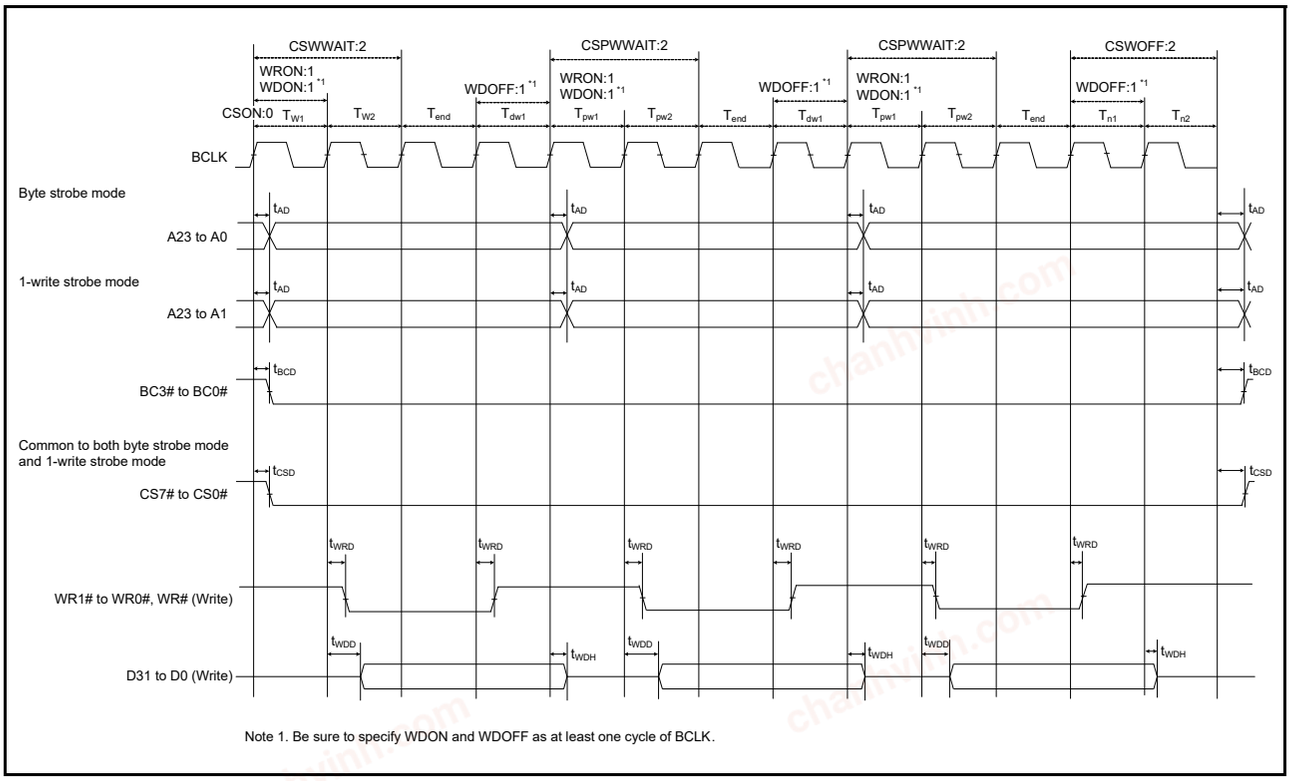


Figure 2.22 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.23 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

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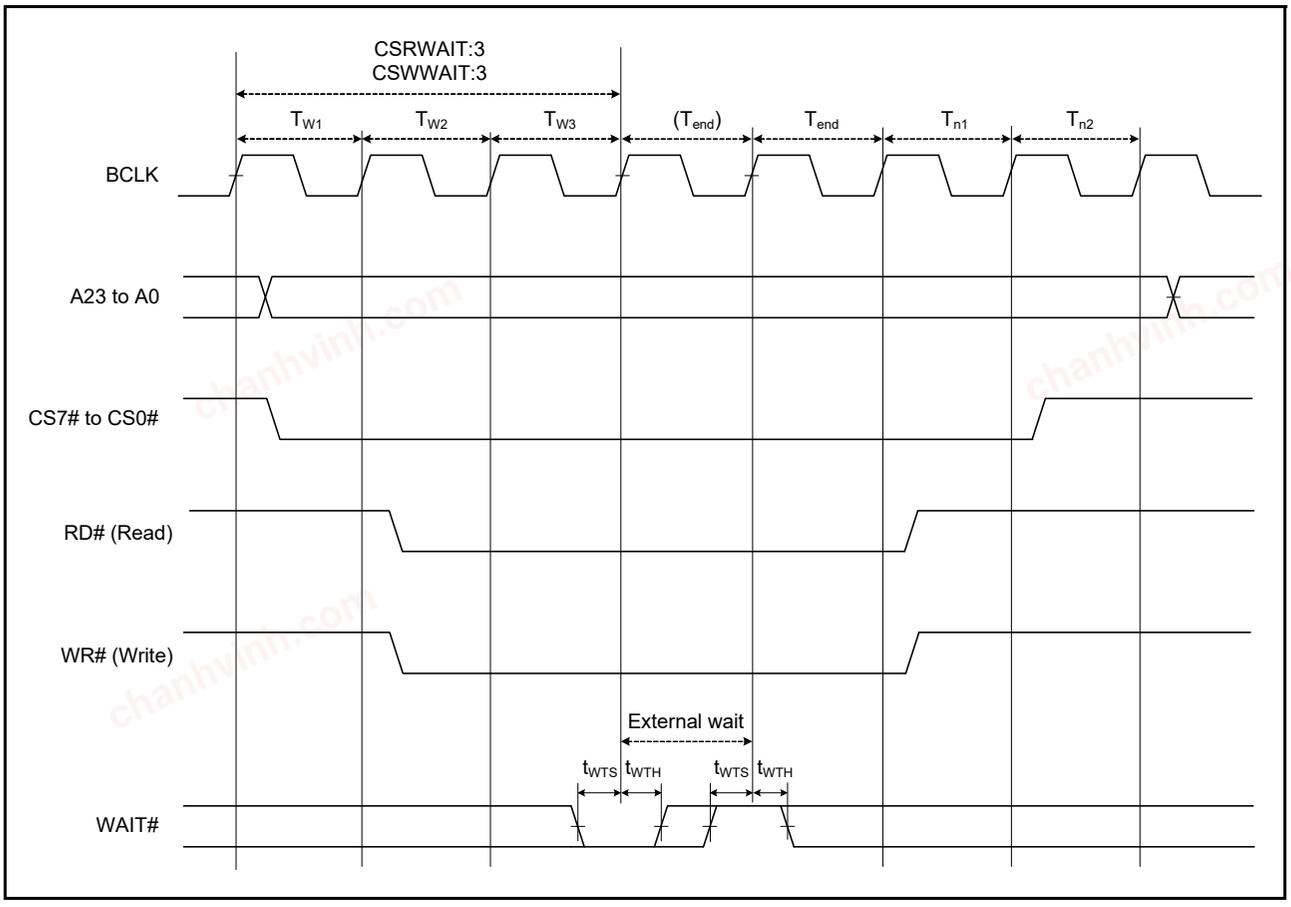
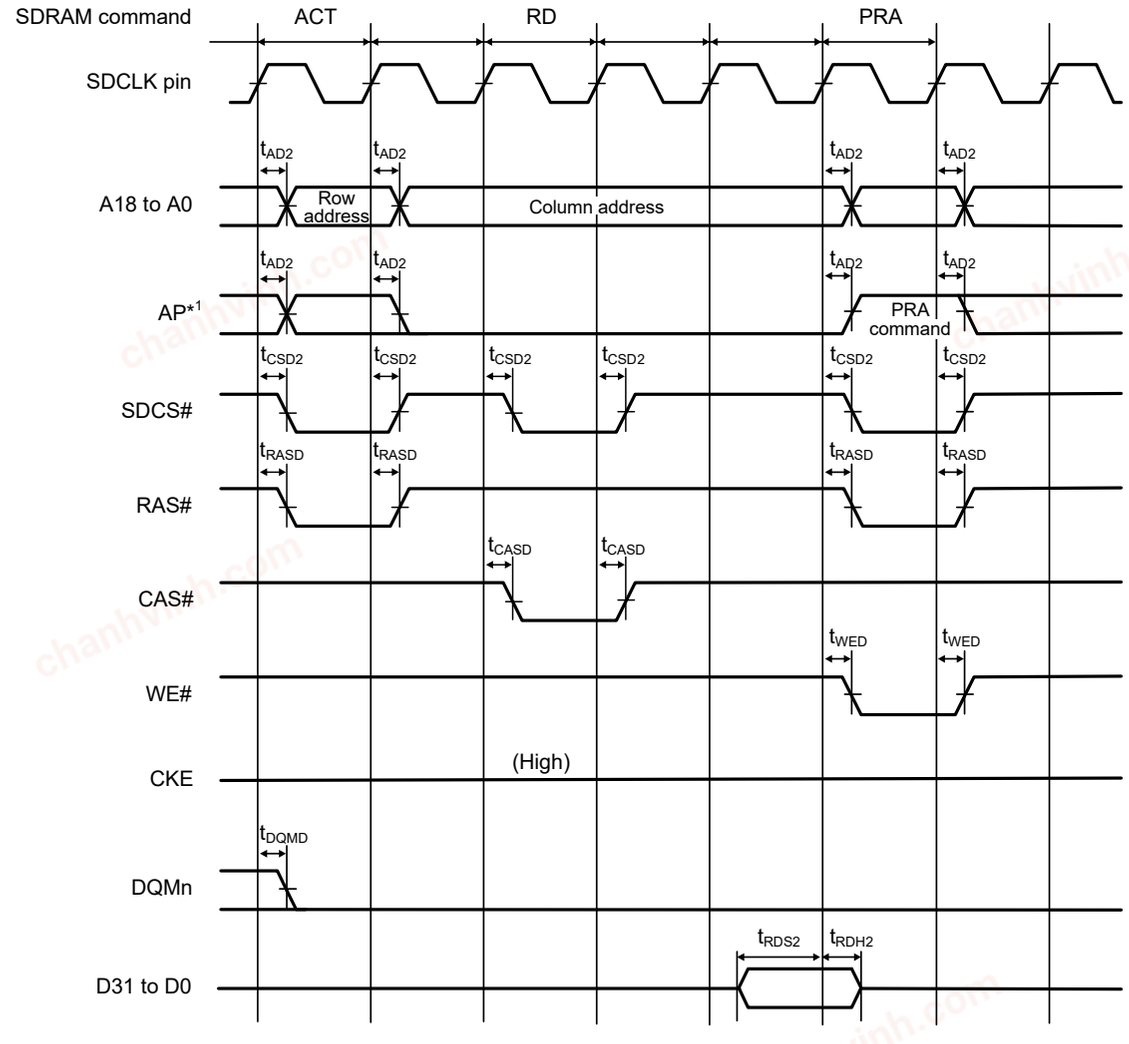


Figure 2.24 External Bus Timing/External Wait Control

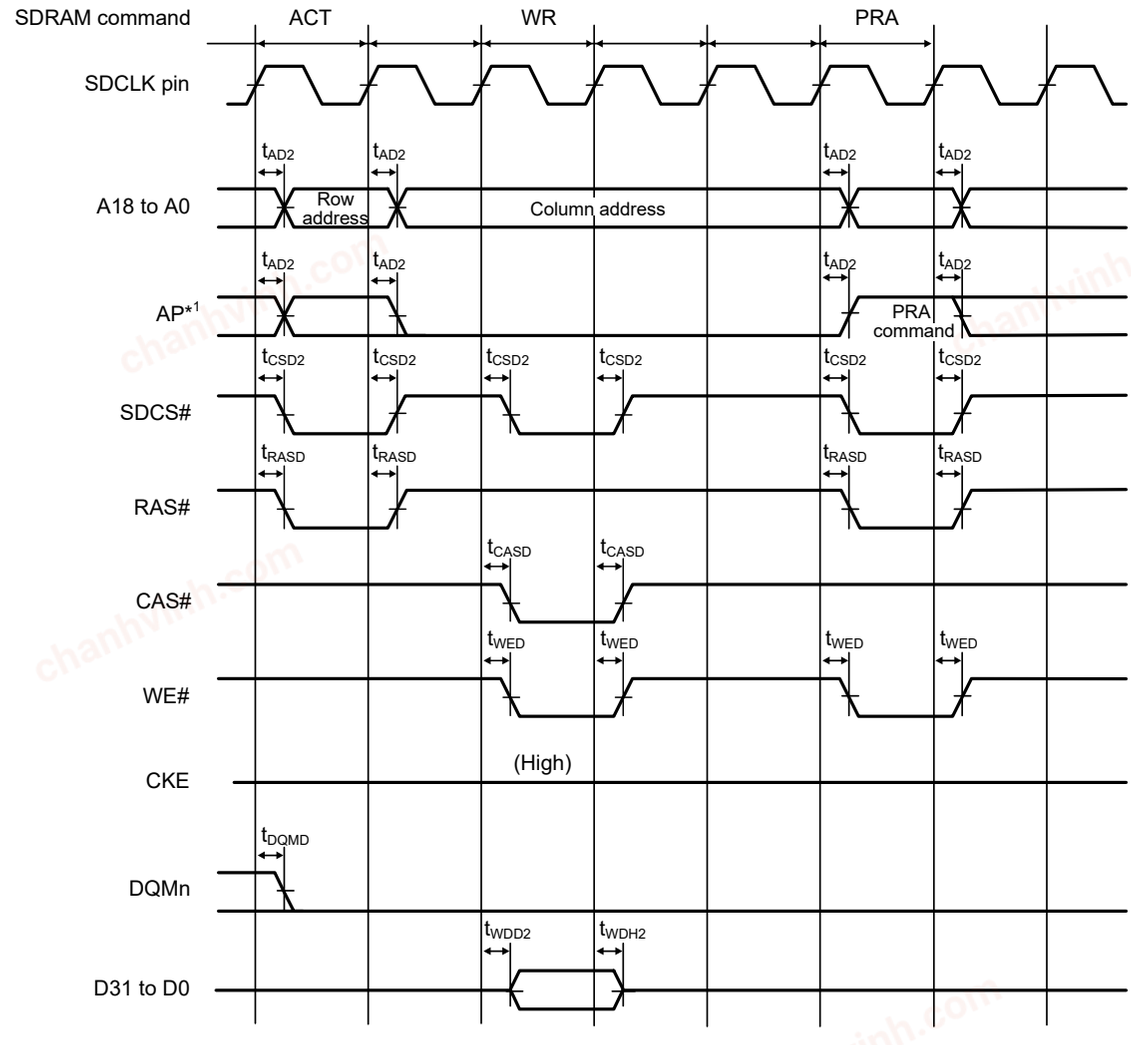
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Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.25 SDRAM Space Single Read Bus Timing

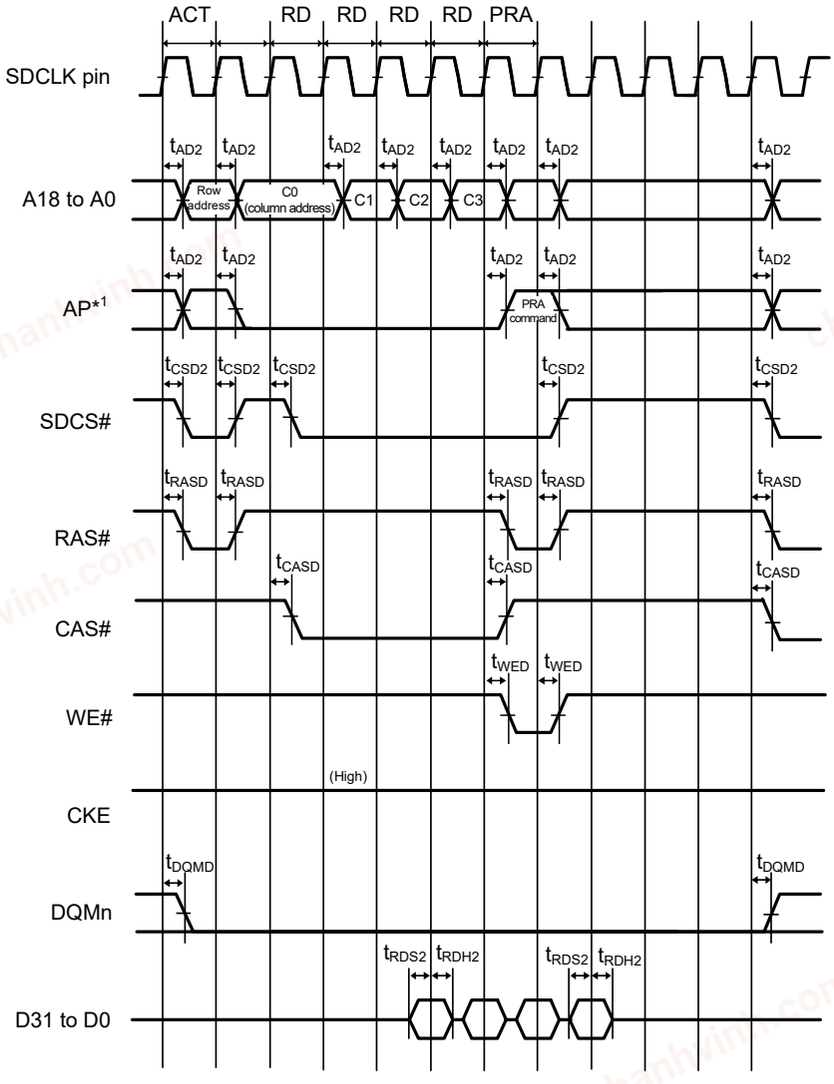
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Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.26 SDRAM Space Single Write Bus Timing

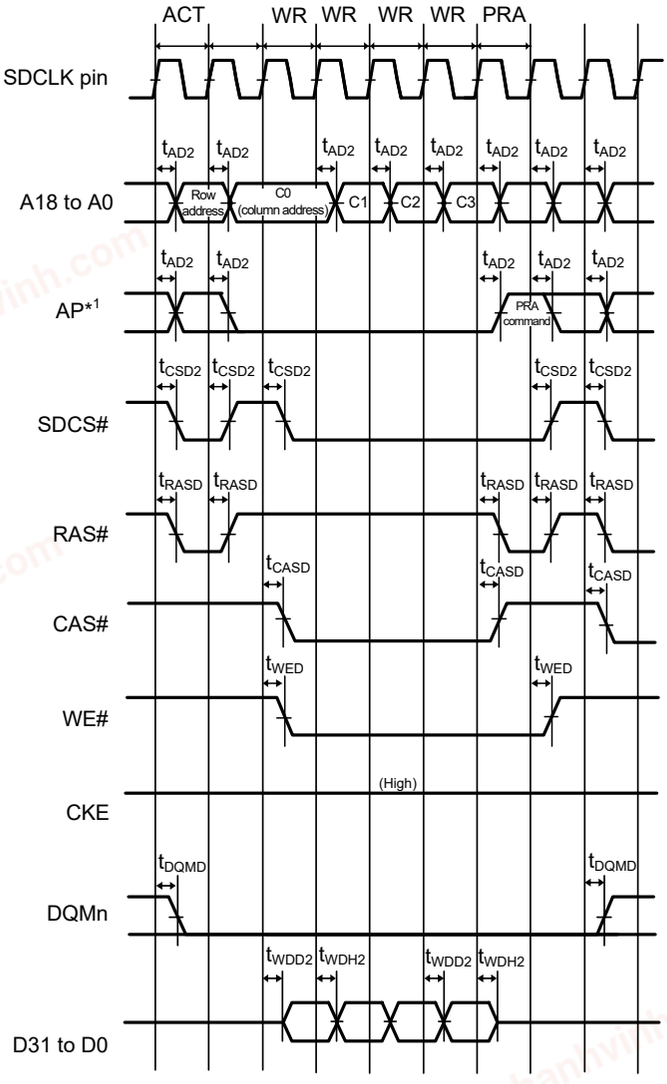
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Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.27 SDRAM Space Multiple Read Bus Timing

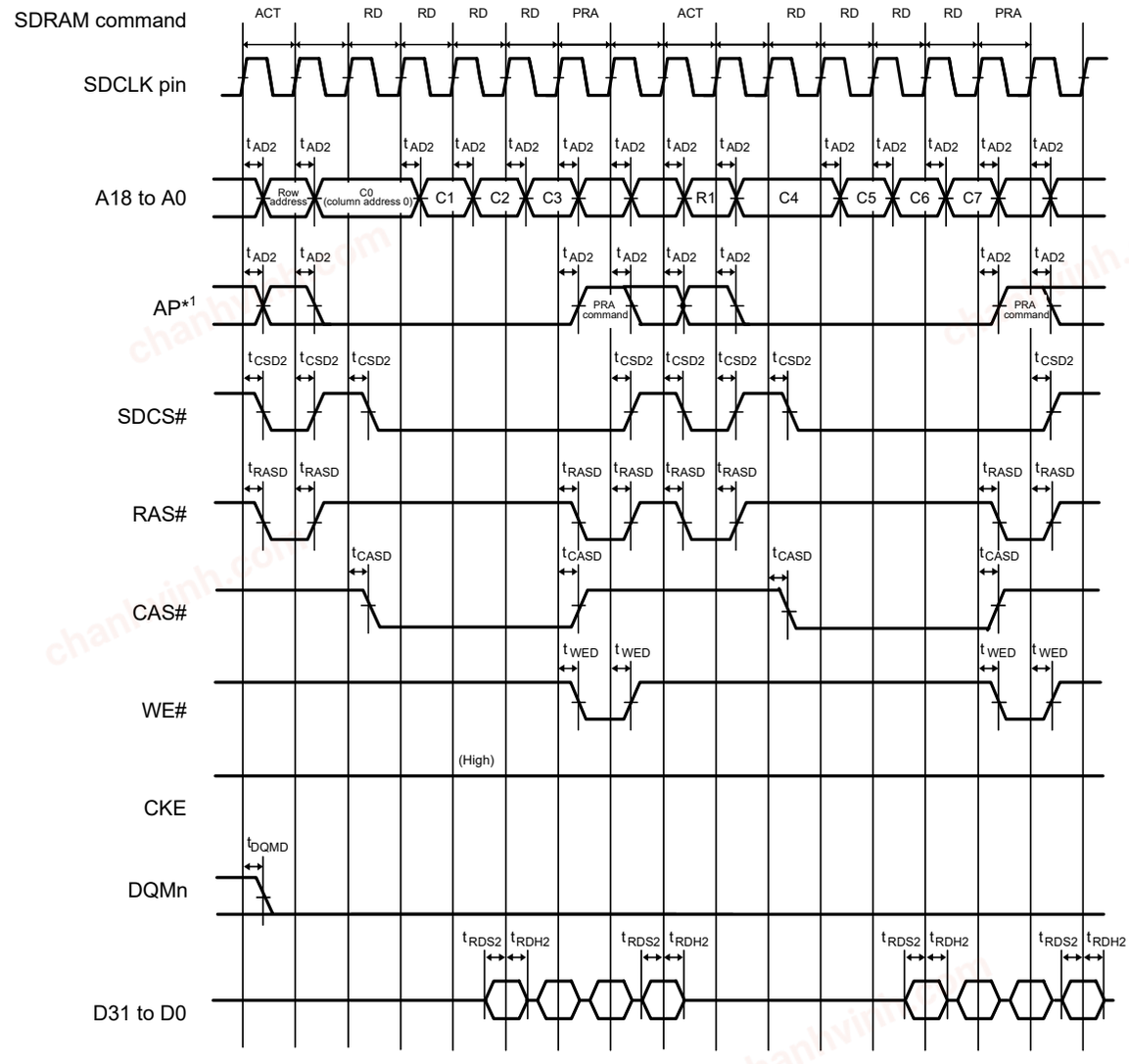
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Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.28 SDRAM Space Multiple Write Bus Timing

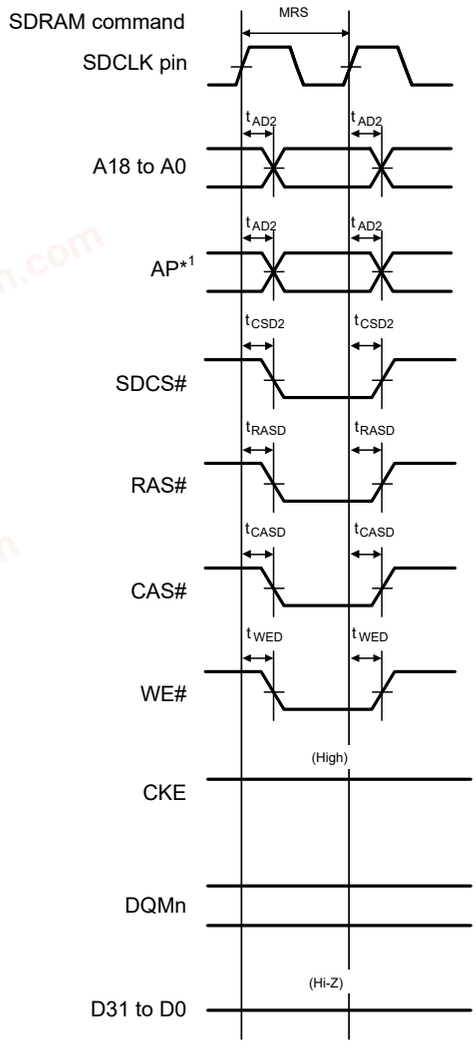
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Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.29 SDRAM Space Multiple Read Line Stride Bus Timing

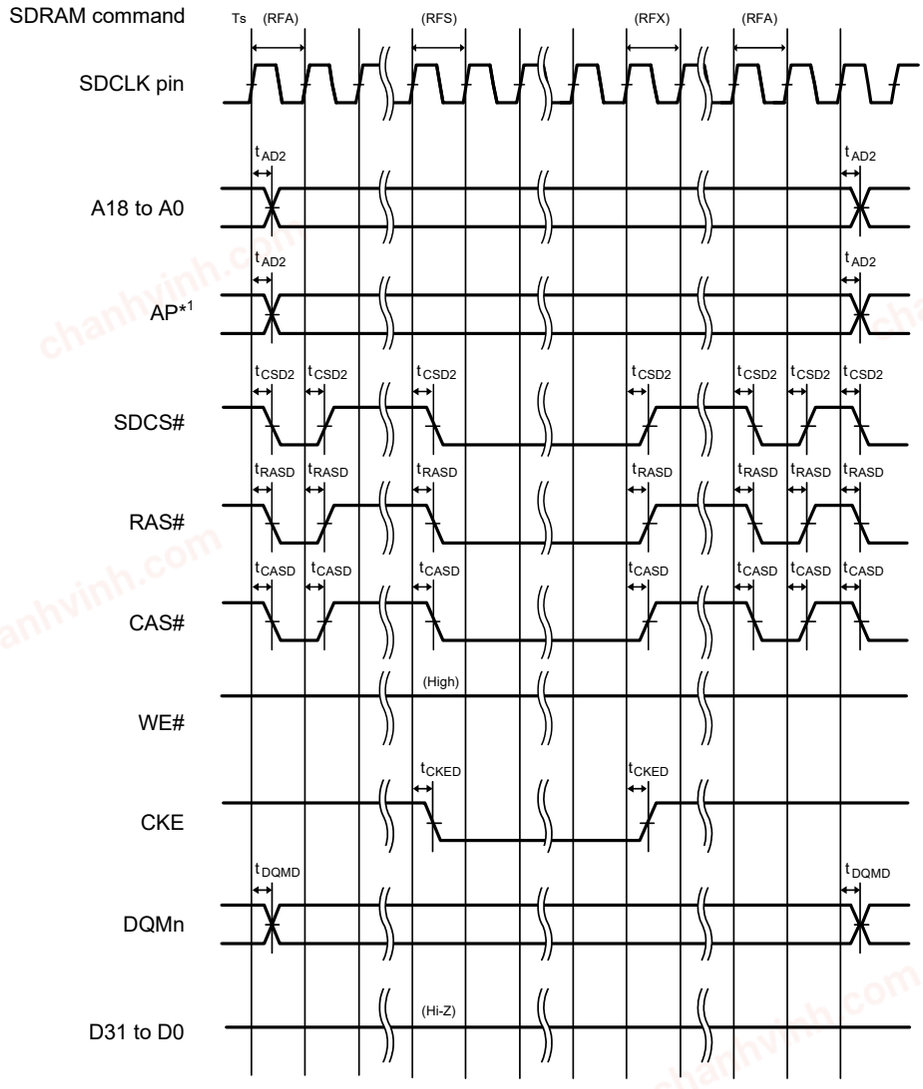
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Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.30 SDRAM Space Mode Register Set Bus Timing

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Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.31 SDRAM Space Self-Refresh Bus Timing

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2.4.6 EXDMAC Timing

Table 2.27 EXDMAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, BCLK = SDCLK = 8 to 80 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	13	—	ns	Figure 2.32
	EDREQ hold time	t_{EDRQH}	2	—	ns	
	EDACK delay time	t_{EDACD}	—	13	ns	Figure 2.33, Figure 2.34

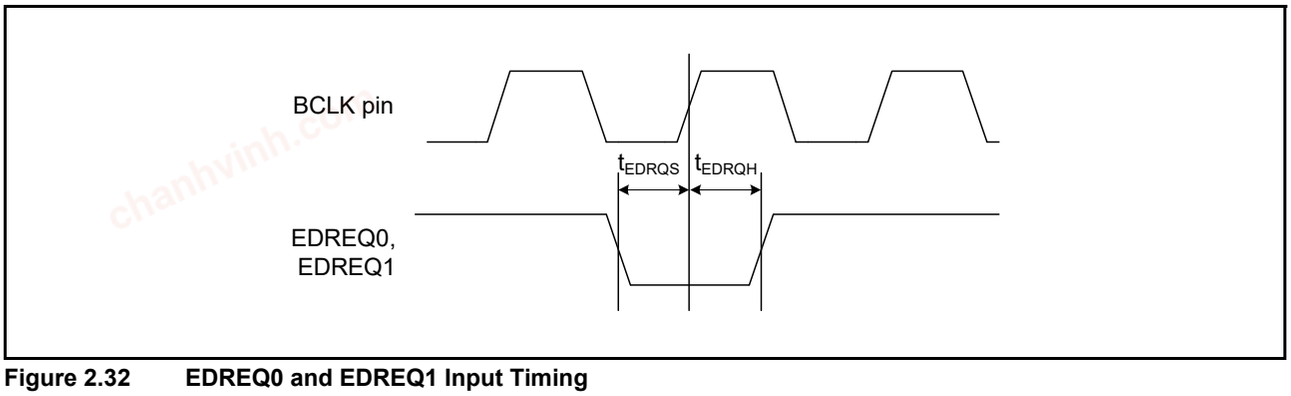


Figure 2.32 EDREQ0 and EDREQ1 Input Timing

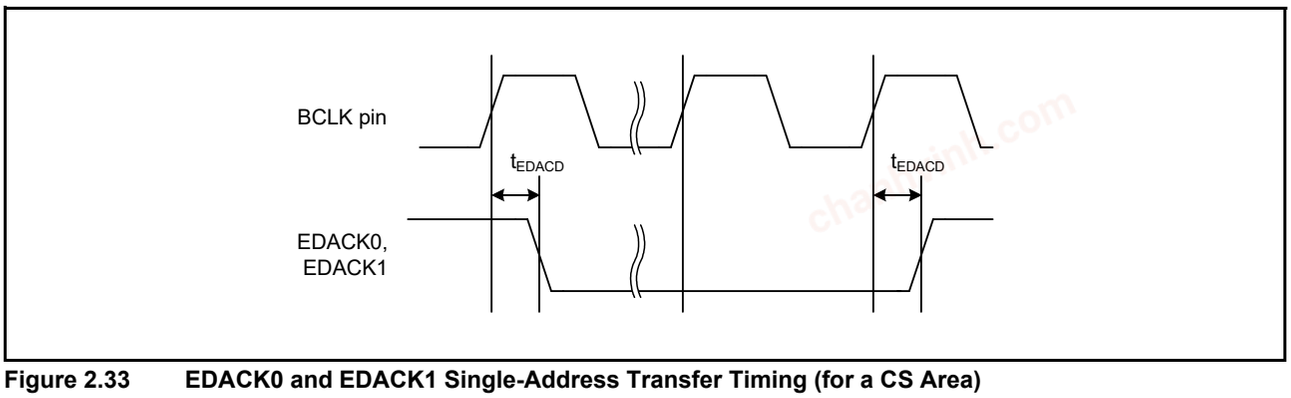


Figure 2.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)

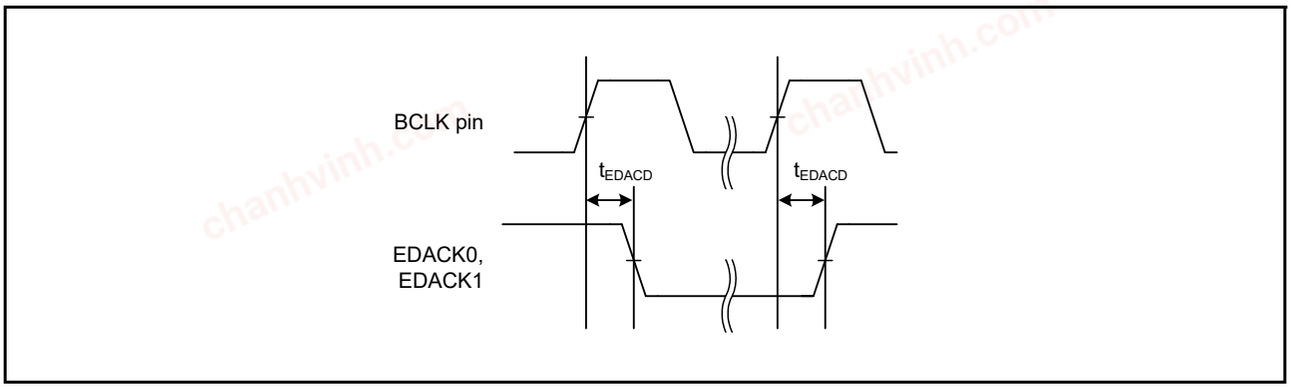


Figure 2.34 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)

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2.4.7 Timing of On-Chip Peripheral Modules

Table 2.28 I/O Port Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.35

Note 1. t_{PBcyc}: PCLKB cycle

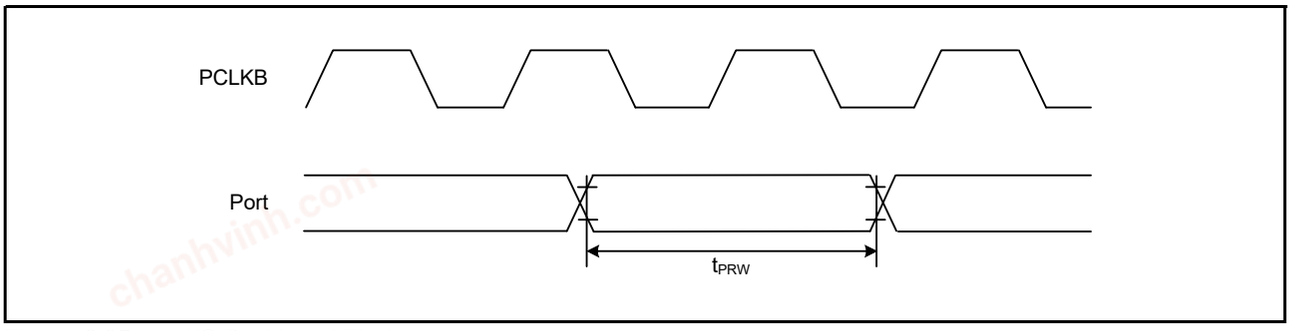


Figure 2.35 I/O Port Input Timing

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Table 2.29 TPU Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PBcyc}	Figure 2.36
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PBcyc}	Figure 2.37
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

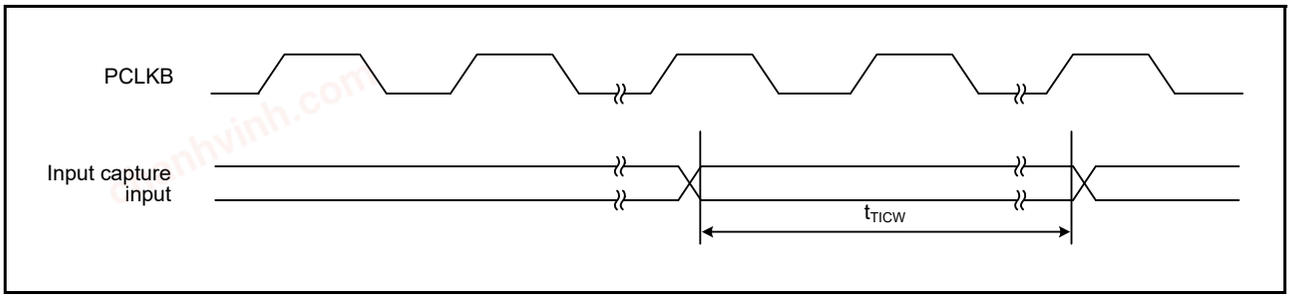


Figure 2.36 TPU Input Capture Input Timing

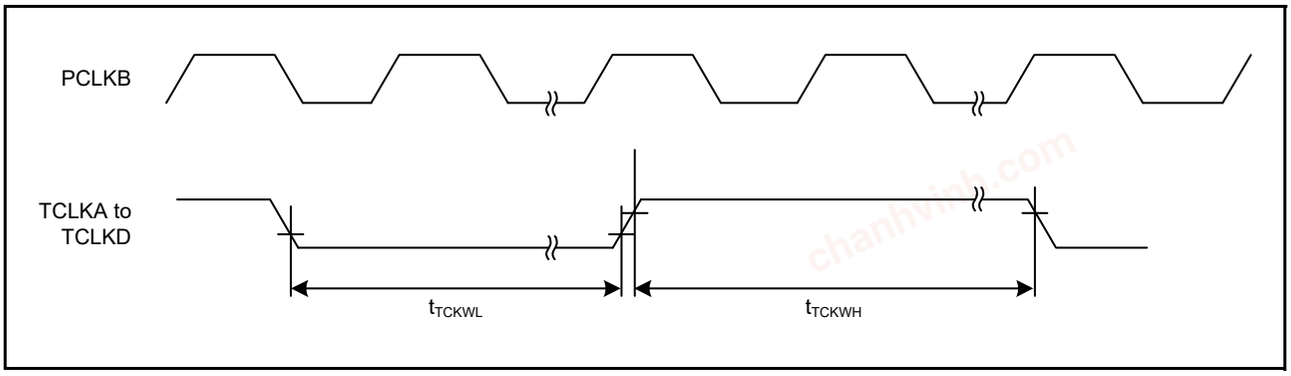


Figure 2.37 TPU Clock Input Timing

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Table 2.30 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.38
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

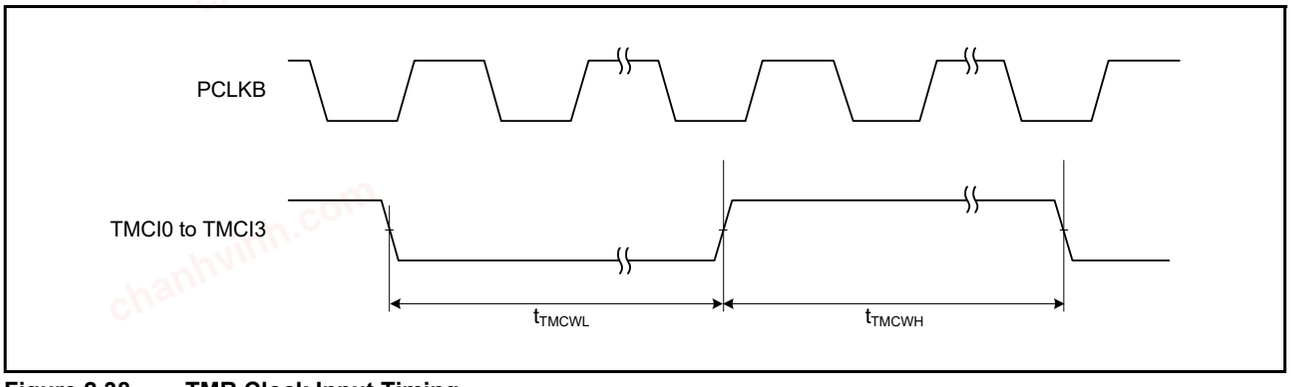


Figure 2.38 TMR Clock Input Timing

Table 2.31 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWTICW}$	1.5	—	t_{PBcyc}	Figure 2.39
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

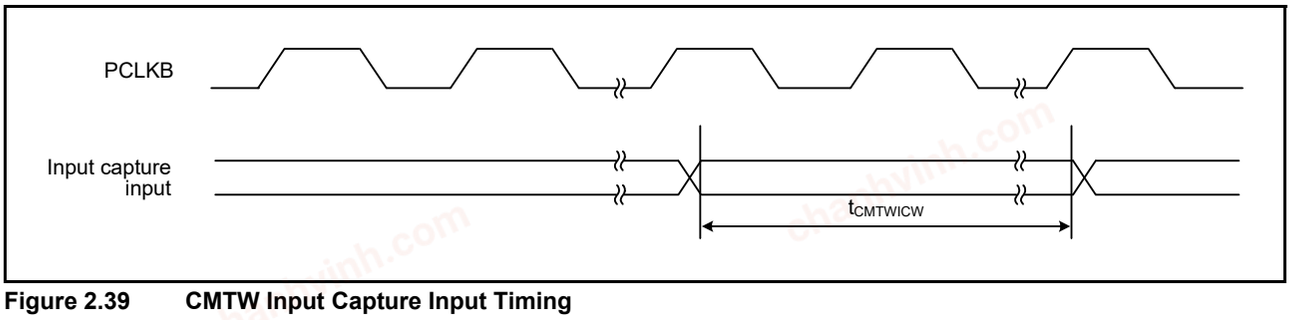


Figure 2.39 CMTW Input Capture Input Timing

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Table 2.32 MTU Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 2.40
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 2.41
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc}: PCLKA cycle

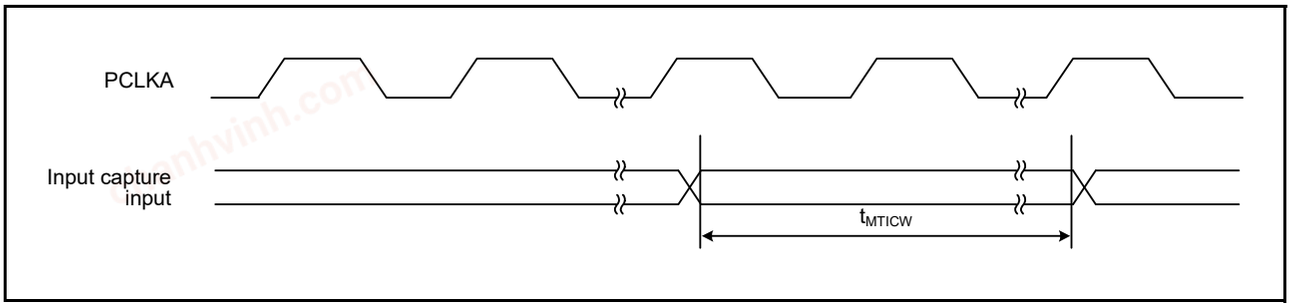


Figure 2.40 MTU Input Capture Input Timing

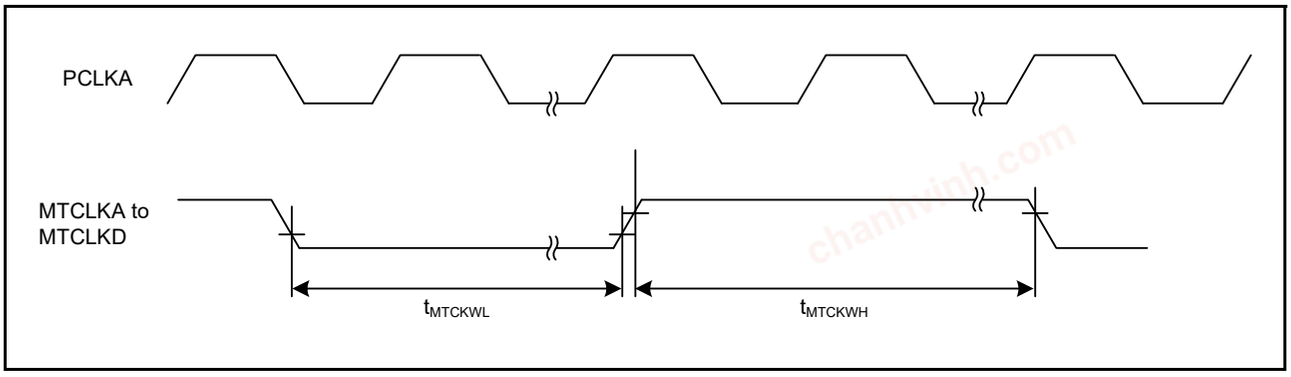


Figure 2.41 MTU Clock Input Timing

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Table 2.33 POE and POEG Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POEn# input pulse width (n = 0, 4, 8, 10, 11)		t_{POEW}	1.5	—	—	t_{PBcyc}	Figure 2.42
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	—	5 PCLKB + 0.24	µs	Figure 2.43 When detecting falling edges (ICSRm.POEnM[3:0] = 0000 (m = 1 to 5; n = 0, 4, 8, 10, 11))
		Simultaneous conduction of output pins	t_{POEDO}	—	—	3 PCLKB + 0.2	µs	Figure 2.44
		Register setting	t_{POEDS}	—	—	1 PCLKB + 0.2	µs	Figure 2.45 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	—	21	µs	Figure 2.46
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}	1.5	—	—	t_{PBcyc}	Figure 2.47
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	—	3 PCLKB + 0.34	µs	Figure 2.48 When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D))
		Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}	—	—	0.5	µs	Figure 2.49
		Register setting	t_{POEGDS}	—	—	1 PCLKB + 0.3	µs	Figure 2.50 Time for access to the register is not included.
		Oscillation stop detection	$t_{POEGDOS}$	—	—	21	µs	Figure 2.51

Note 1. t_{PBcyc}: PCLKB cycle

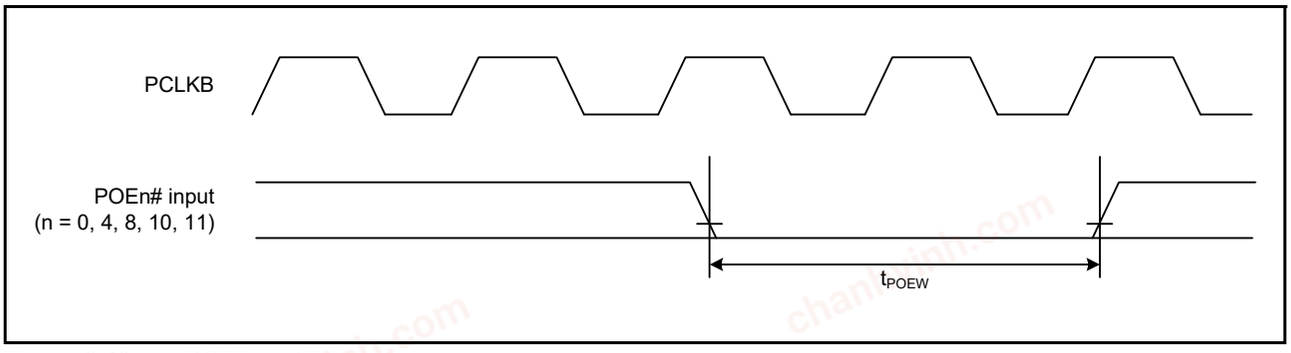


Figure 2.42 POE Input Timing

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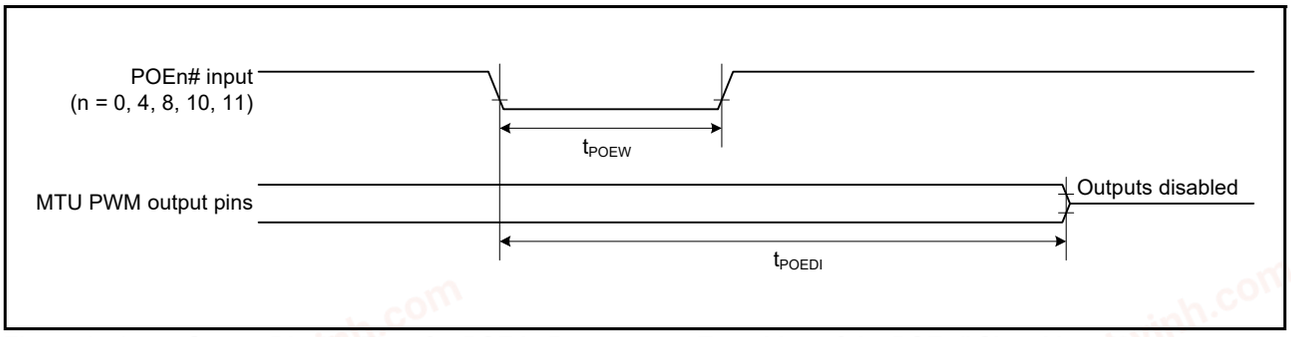
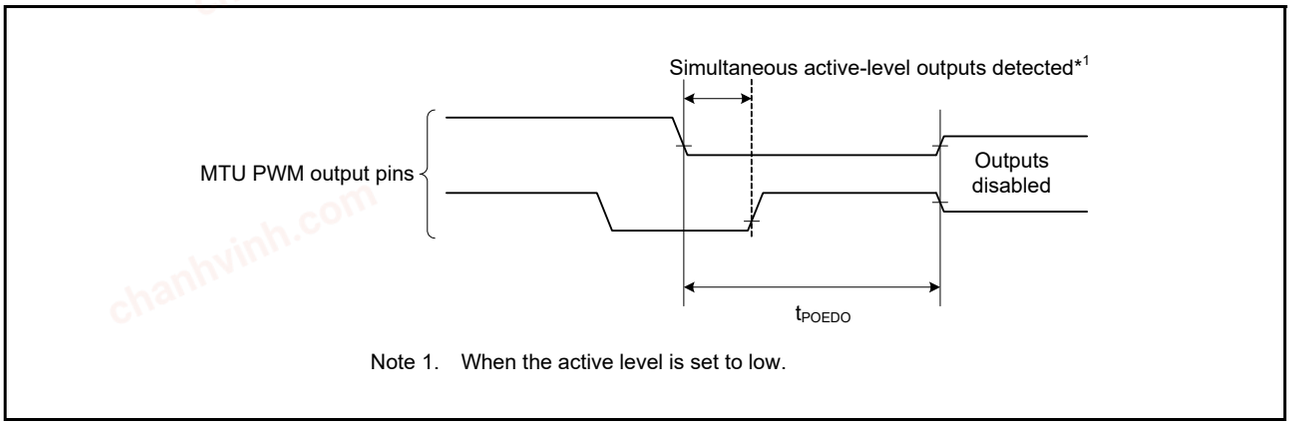


Figure 2.43 Output Disable Time for POE in Response to Transition of the POEn# Signal Level



Note 1. When the active level is set to low.

Figure 2.44 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

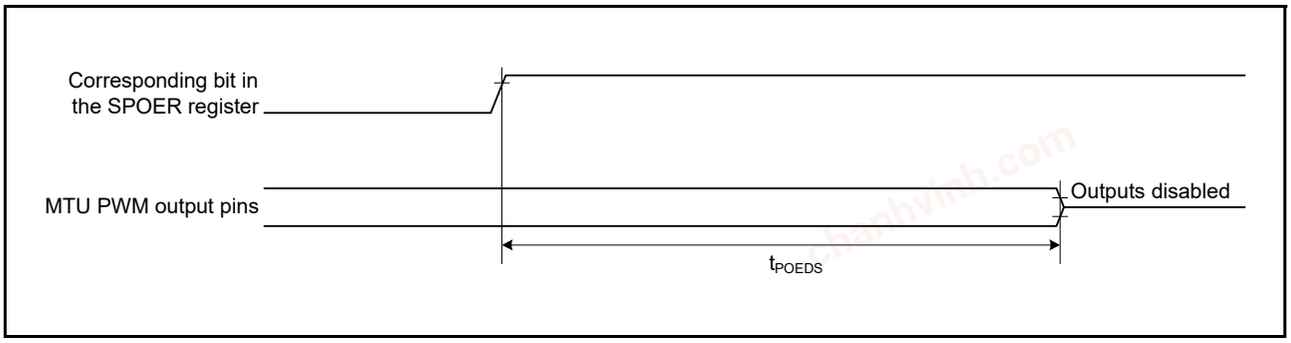


Figure 2.45 Output Disable Time for POE in Response to the Register Setting

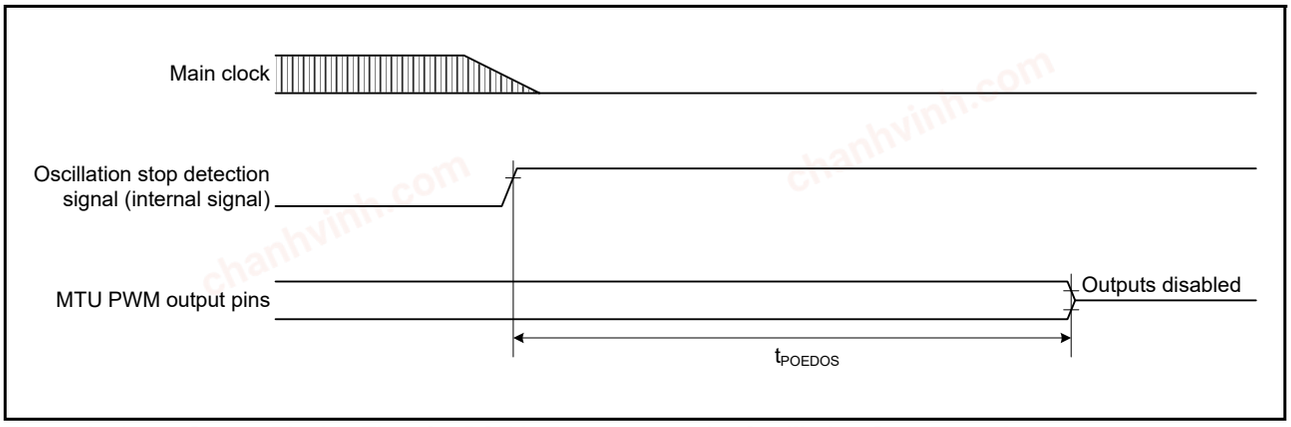


Figure 2.46 Output Disable Time for POE in Response to the Oscillation Stop Detection

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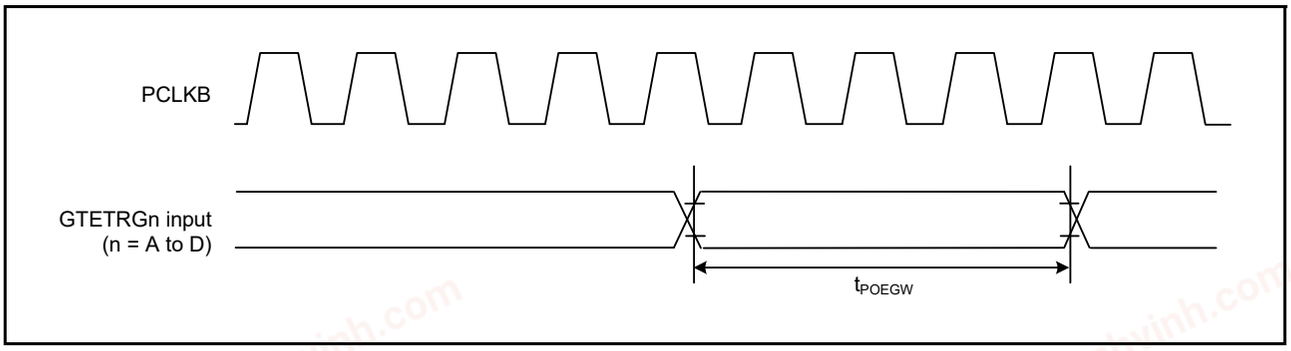


Figure 2.47 POEG Input Timing

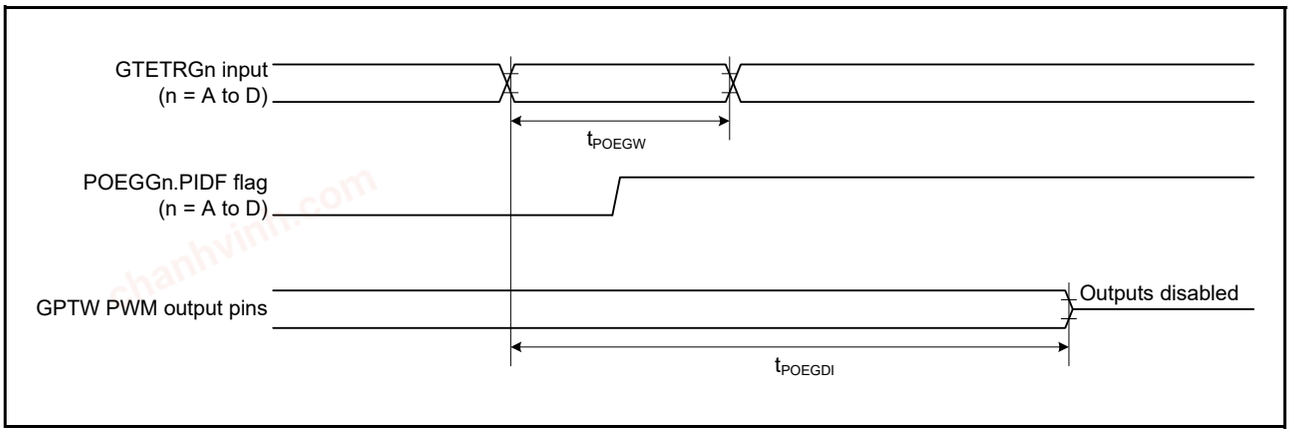
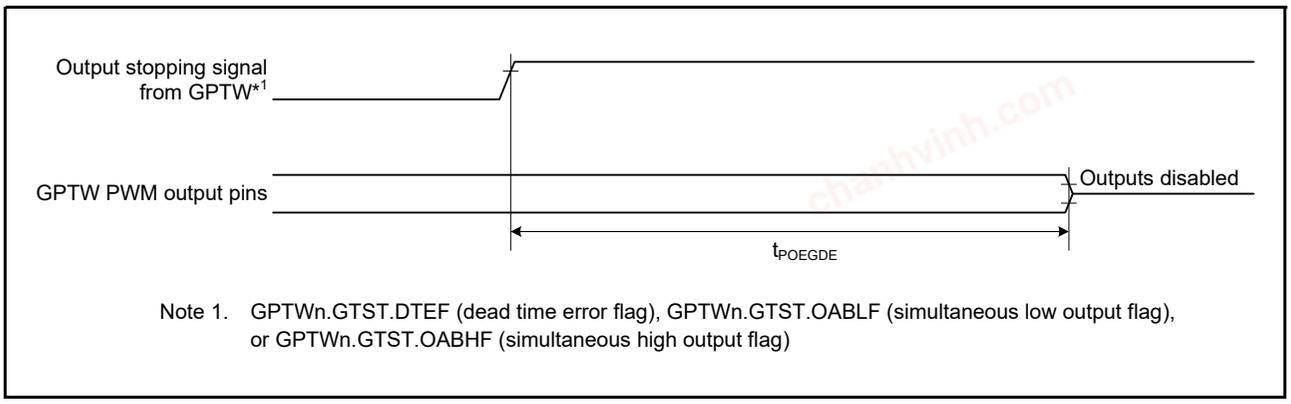


Figure 2.48 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin



Note 1. GPTWn.GTST.DTEF (dead time error flag), GPTWn.GTST.OABLF (simultaneous low output flag), or GPTWn.GTST.OABHF (simultaneous high output flag)

Figure 2.49 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW

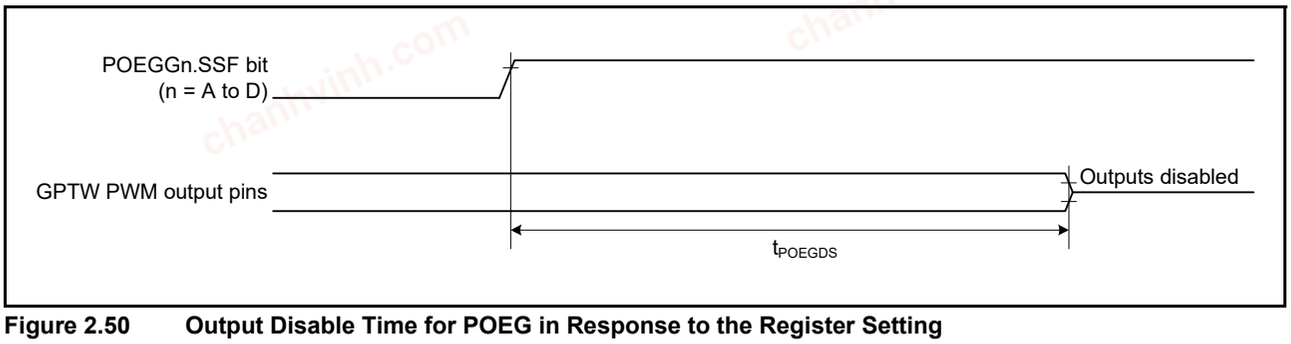


Figure 2.50 Output Disable Time for POEG in Response to the Register Setting

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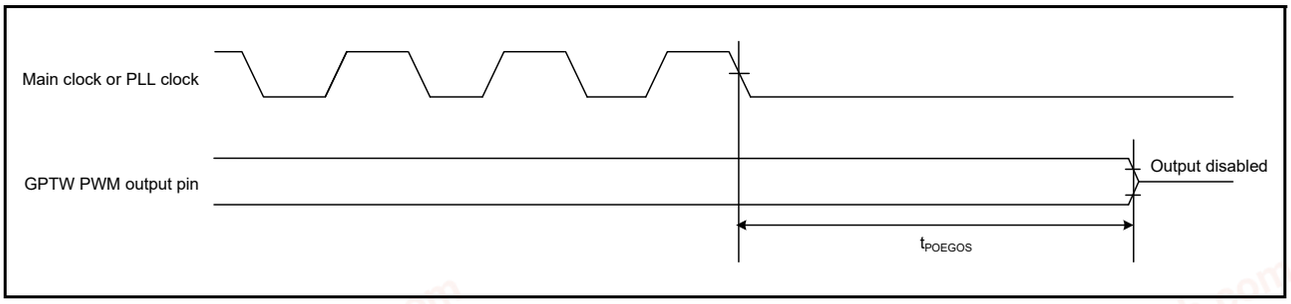


Figure 2.51 Output Disable Time of POEG in Response to the Oscillation Stop Detection

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Table 2.34 GPTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1, *2	Test Conditions
GPTW	Input capture input pulse width	Single-edge setting	t_{GTICW}	1.5	—	t_{PAcyc}	Figure 2.52
		Both-edge setting		2.5	—		
	External trigger input pulse width	Single-edge setting	t_{GTEW}	1.5	—	t_{PBcyc}	Figure 2.53
		Both-edge setting		2.5	—		

Note 1. t_{PAcyc}: PCLKA cycle
Note 2. t_{PBcyc}: PCLKB cycle

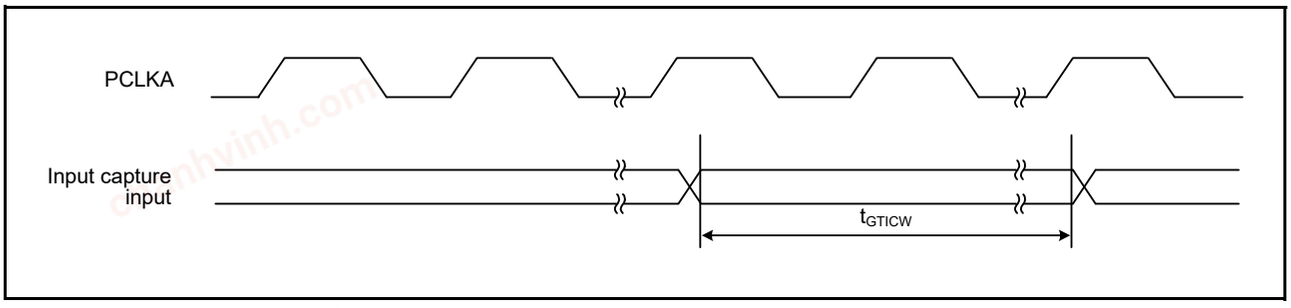


Figure 2.52 GPTW Input Capture Input Timing

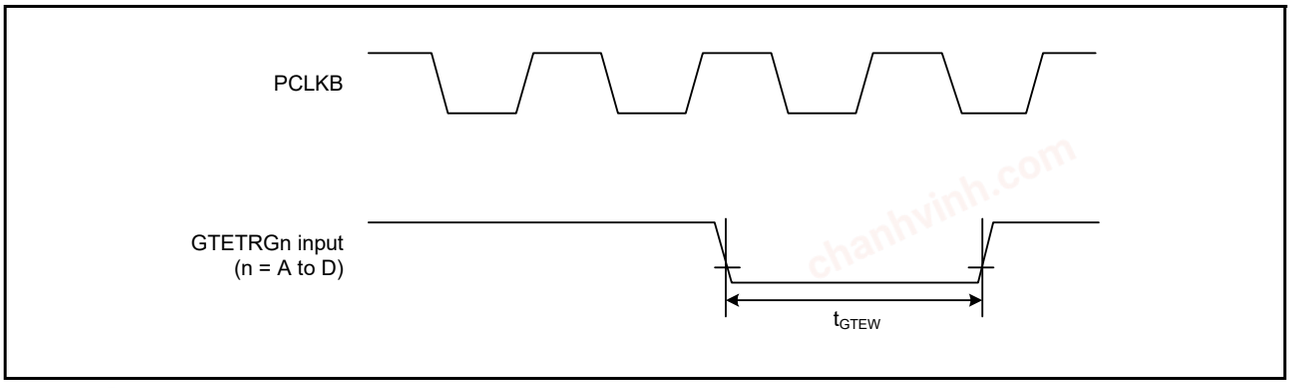


Figure 2.53 GPTW External Trigger Input Timing

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Table 2.35 A/D Converter Trigger Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 2.54

Note 1. t_{PBcyc}: PCLKB cycle

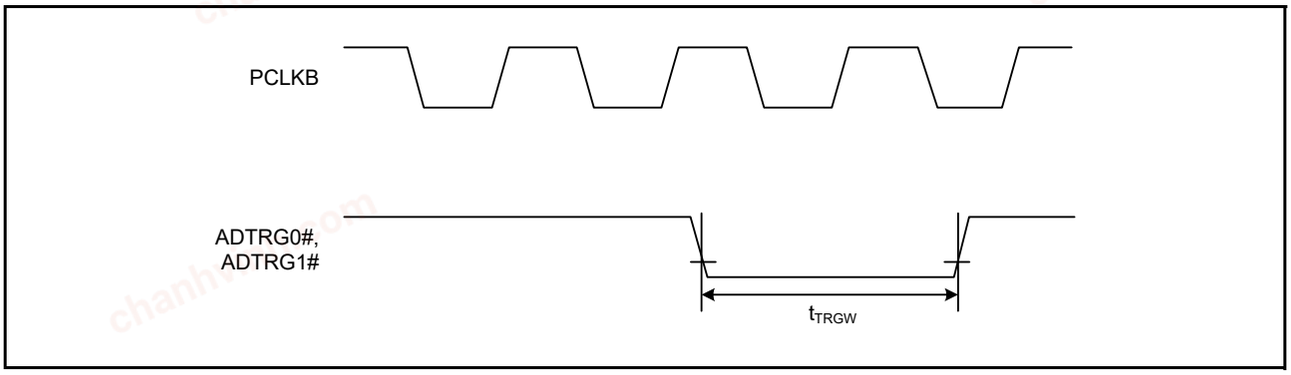


Figure 2.54 A/D Converter Trigger Input Timing

Table 2.36 CAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item*1, *2			Symbol	Min.*1, *2	Max.	Unit	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$	t_{CACREF}	4.5 t_{cac} + 3 t_{PBcyc}	—	ns	
		$t_{PBcyc} > t_{cac}$		5 t_{cac} + 6.5 t_{PBcyc}	—		

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{cac}: CAC count clock source cycle

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Table 2.37 SCI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCIh, SCIj	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 2.55
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{PBcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	28	ns	Figure 2.56
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	
SCIi	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 2.55
		Clock synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{PAcyc}	
		Clock synchronous		8	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Master	t_{TXD}	—	15	ns	Figure 2.56
		Slave		—	28		
	Receive data setup time	Clock synchronous	t_{RXS}	20	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—		

Note 1. t_{PBcyc}: PCLKB cycle; t_{PAcyc}: PCLKA cycle
Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1

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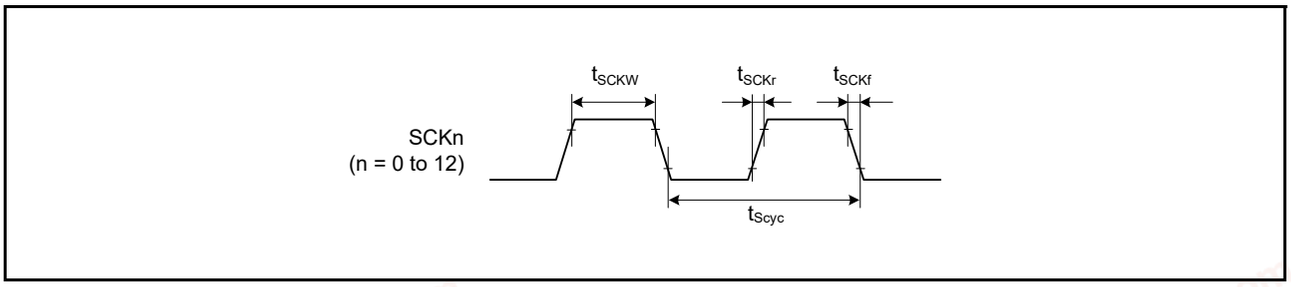


Figure 2.55 SCK Clock Input Timing

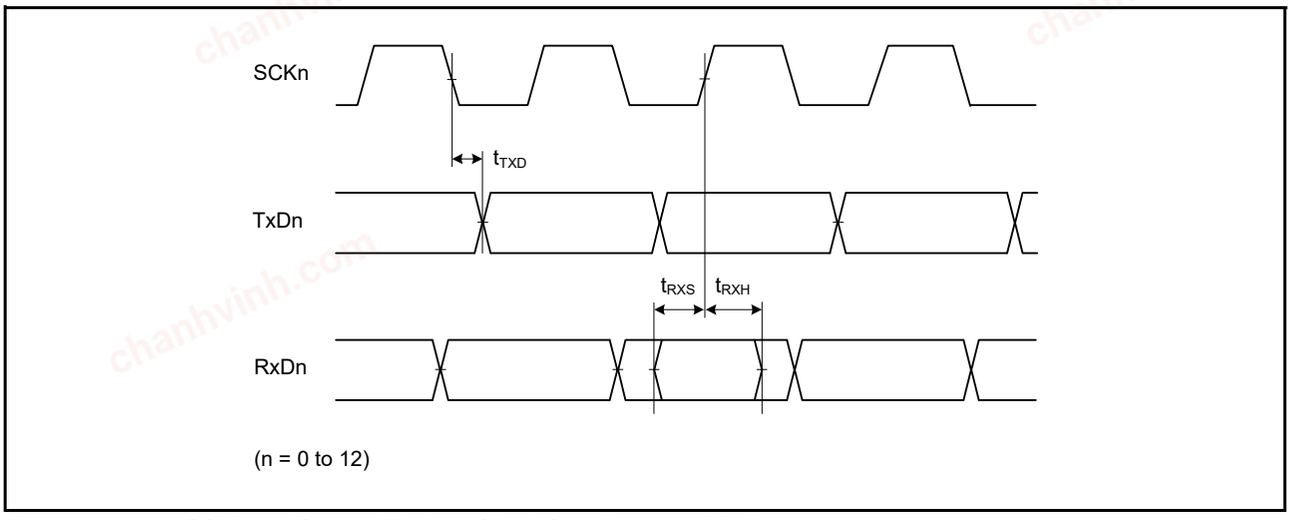


Figure 2.56 SCI Input/Output Timing: Clock Synchronous Mode

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Table 2.38 Expansion Serial Sound Interface Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit	Test Conditions
AUDIO_CLK	Cycle		t_{EXcyc}	20	—	ns	Figure 2.57
	High/low level		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	
SSIBCKn	Cycle	Master	t_O	80	—	ns	Figure 2.58
		Slave	t_I	80	—	ns	
	Output clock high level	Master	t_{HC}	0.35	—	t_O	
	Output clock low level		t_{LC}	0.35	—	t_O	
	Input clock high level	Slave	t_{HC}	0.35	—	t_I	
	Input clock low level		t_{LC}	0.35	—	t_I	
	Output clock rise time	Master	t_{RC}	—	0.15	t_O	
	Output clock fall time		t_{FC}	—	0.15	t_O	
	Input clock rise time	Slave	t_{RC}	—	0.15	t_I	
	Input clock fall time		t_{FC}	—	0.15	t_I	
SSILRCKn,SSITXD0, SSIRXD0, SSIDATA1	Input setup time	Master	t_{SR}	12	—	ns	Figure 2.59, Figure 2.60
		Slave		12	—	ns	
	Input hold time	Master	t_{HR}	8	—	ns	
		Slave		15	—	ns	
	Output delay time	Master	t_{DTR}	–10	5	ns	
		Slave		0	20	ns	
	Output delay time from when an SSILRCK0 signal is changed*1	Slave	t_{DTRW}	—	20	ns	Figure 2.61

n = 0, 1

Note 1. The SSIE has a single path for transmission in slave mode. To generate the data for transmission, the signals input through the SSILRCKn pin through the abovementioned path are used. After that, the data for transmission proceed to be used as the logical outputs to the SSITXD0 or SSIDATA1 pin.

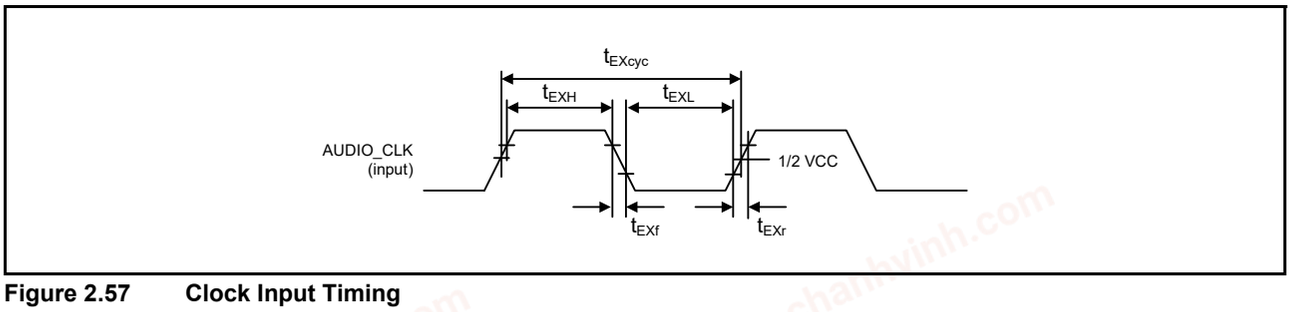


Figure 2.57 Clock Input Timing

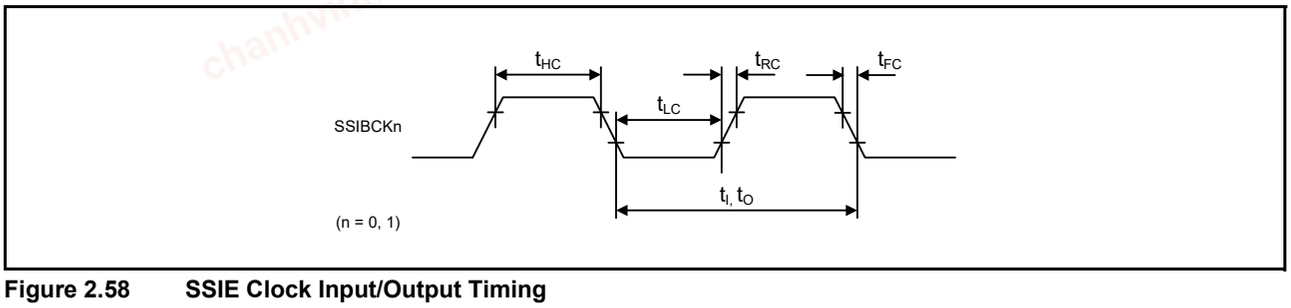


Figure 2.58 SSIE Clock Input/Output Timing

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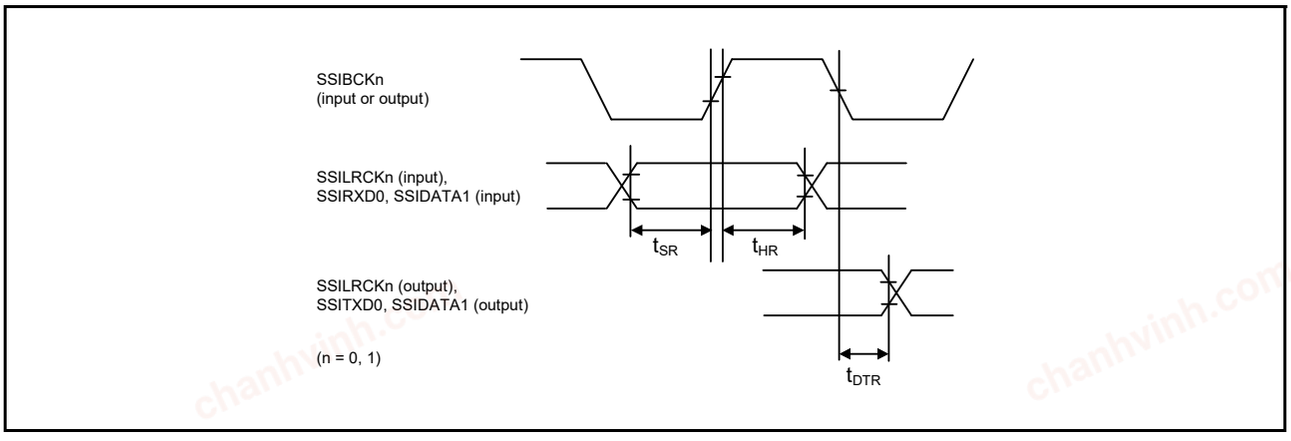


Figure 2.59 Transmission and Reception Timing for the SSIE Data When the SSICR.BCKP Bit is 0

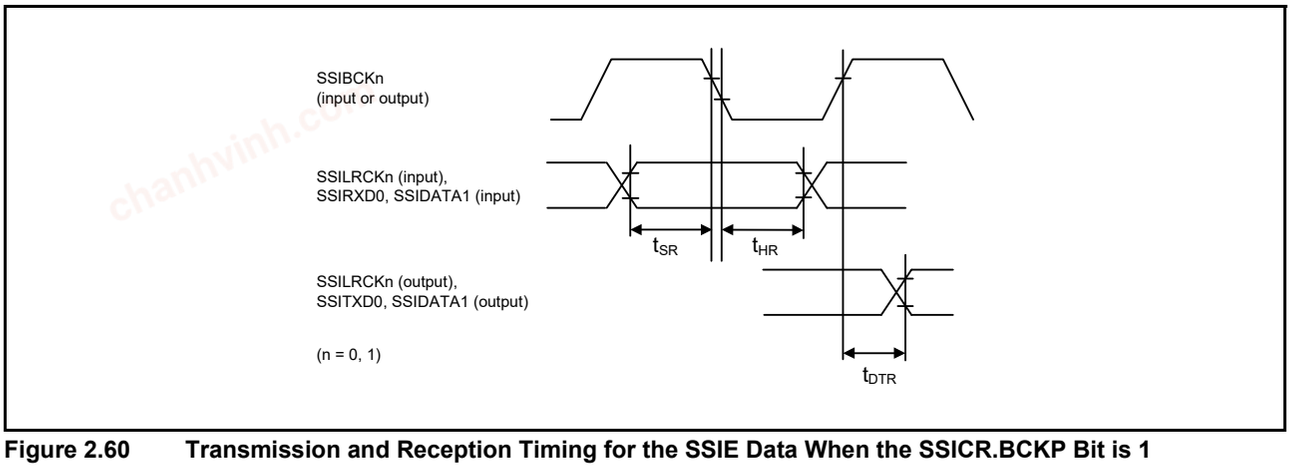


Figure 2.60 Transmission and Reception Timing for the SSIE Data When the SSICR.BCKP Bit is 1

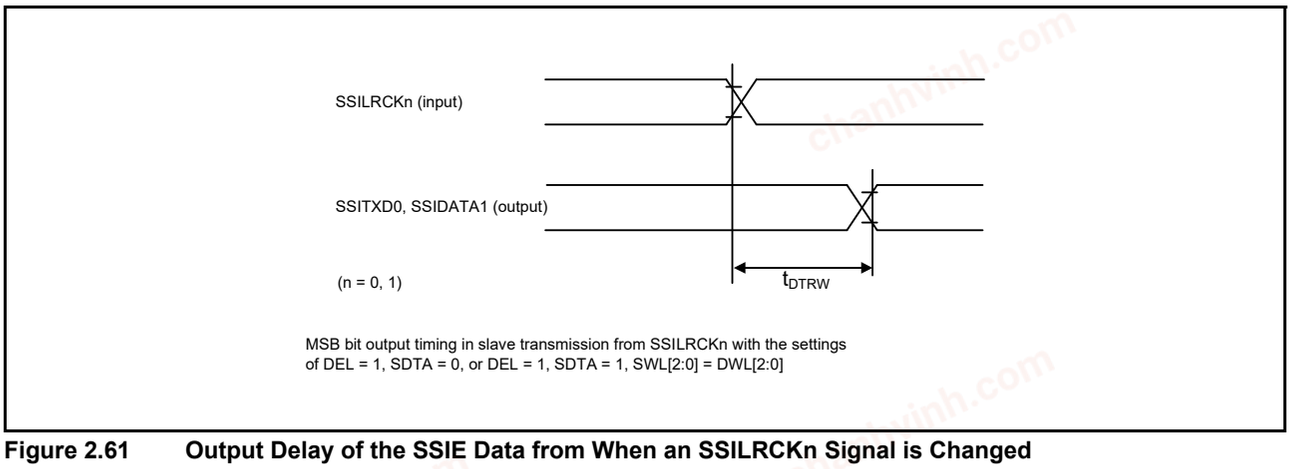


Figure 2.61 Output Delay of the SSIE Data from When an SSILRCKn Signal is Changed

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Table 2.39 RSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item				Symbol	Min.*1	Max.*1	Unit*1	Test Conditions*2
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	—	t_{PAcyc}	Figure 2.62
		Slave			4	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input			—	1	µs	
	Data input setup time	Master		t_{SU}	6	—	ns	Figure 2.63 to Figure 2.68
		Slave			8.3	—		
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—	ns	
			PCLKA division ratio set to a value other than 1/2	t_H	t_{PAcyc}	—		
		Slave			8.3	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			6	—	t_{PAcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			6	—	t_{PAcyc}	
	Data output delay time	Master		t_{OD}	—	6.3	ns	
		Slave			—	28		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns	
		Slave			$6 \times t_{PAcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, tSSLf	—	5	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	$2 \times t_{PAcyc} + 28$	ns	Figure 2.67, Figure 2.68
	Slave output release time			t_{REL}	—	$2 \times t_{PAcyc} + 28$	ns	

Note 1. t_{PAcyc}: PCLKA cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the RSPI interface, the AC portion of the electrical characteristics is measured for each group.

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Table 2.40 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{PAcyc}	Figure 2.62
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 2.63 to Figure 2.68
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{PBcyc}	Figure 2.67, Figure 2.68
	Slave output release time	t_{REL}	—	5	t_{PBcyc}	

Note 1. t_{PAcyc}: PCLKA cycle, t_{PBcyc}: PCLKB cycle

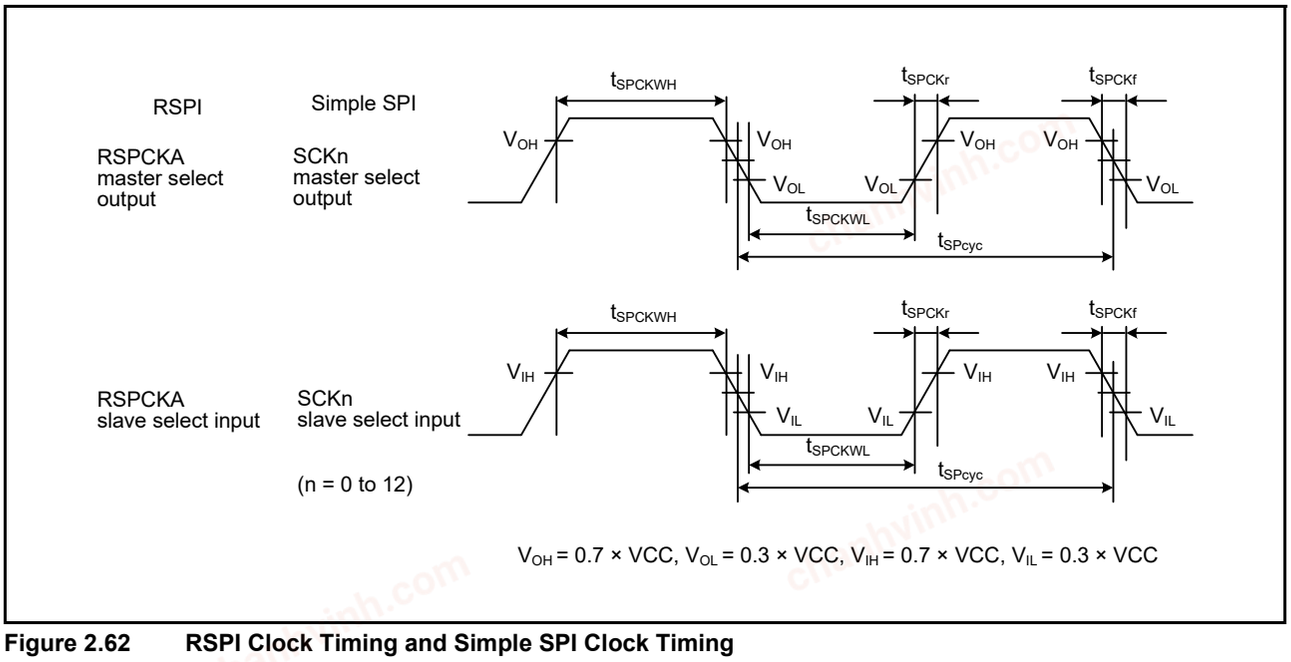


Figure 2.62 RSPI Clock Timing and Simple SPI Clock Timing

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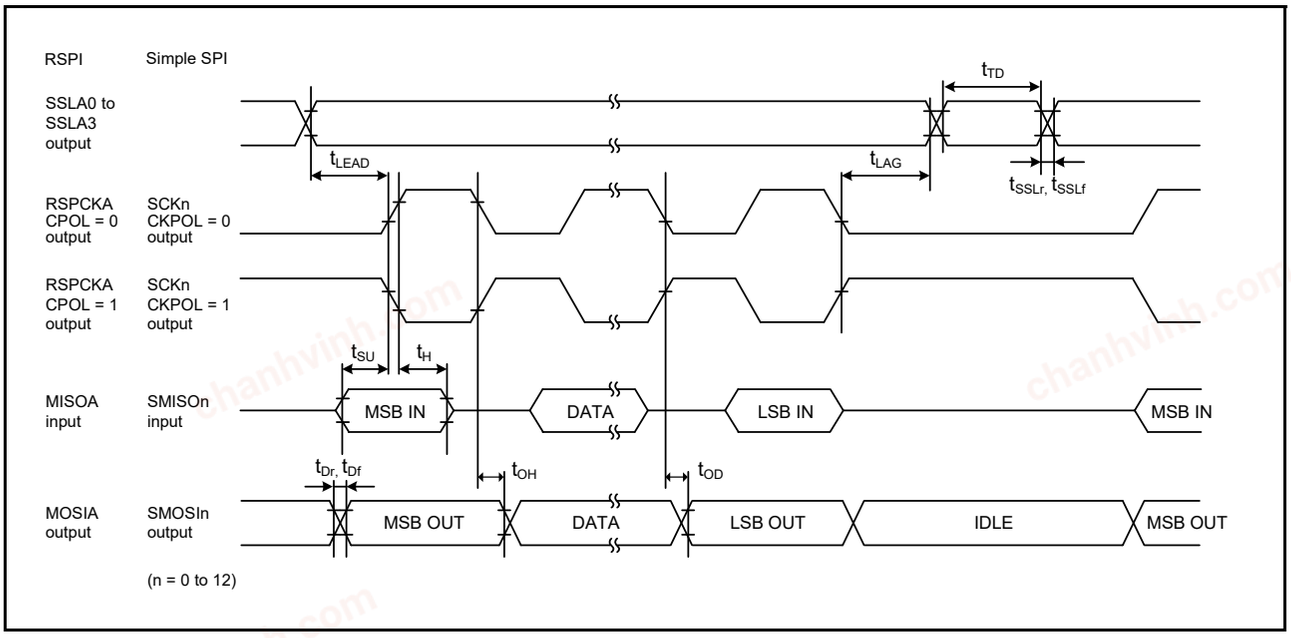


Figure 2.63 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1)

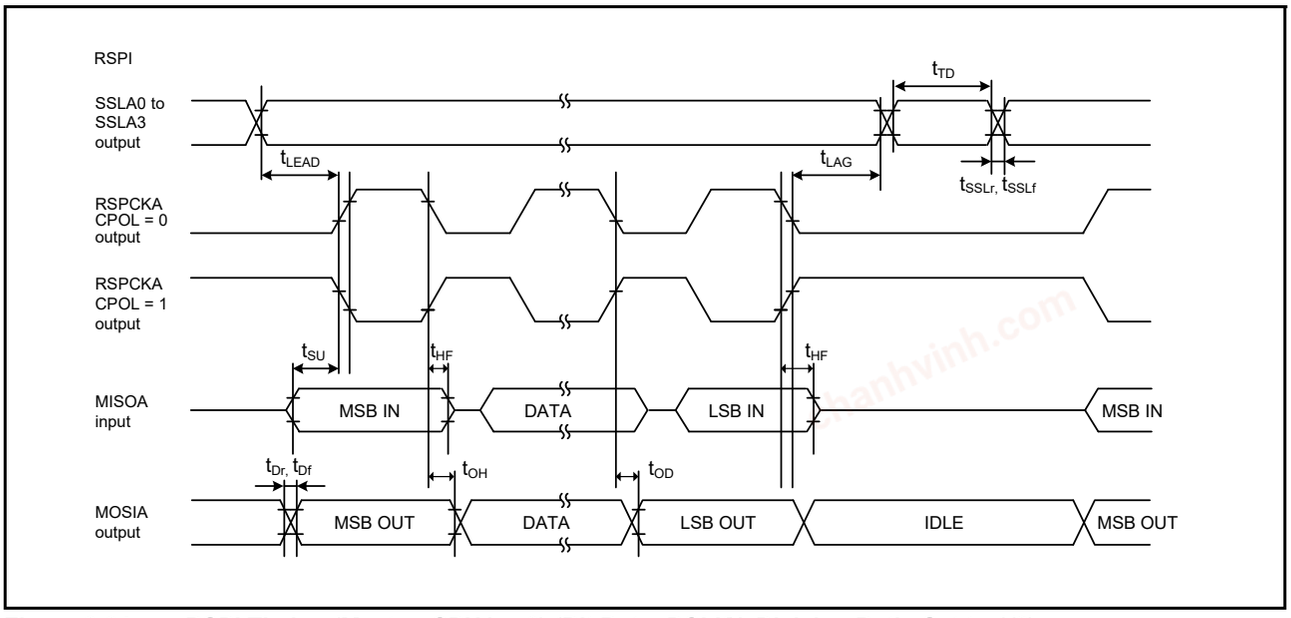


Figure 2.64 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

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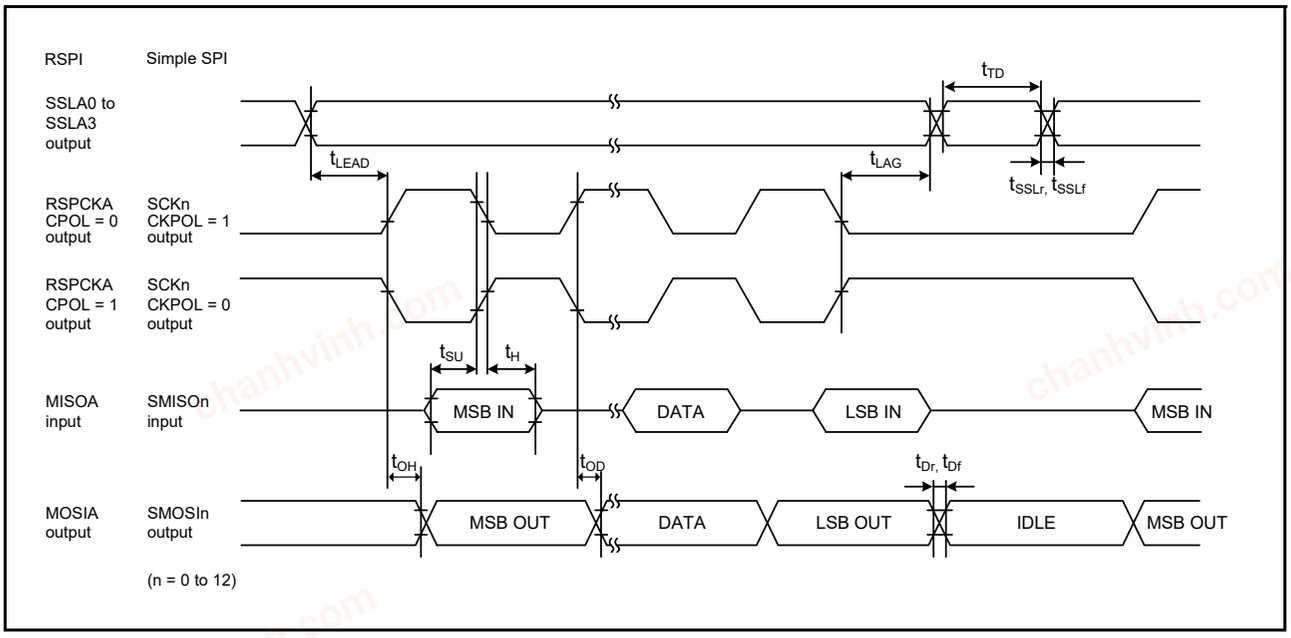


Figure 2.65 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

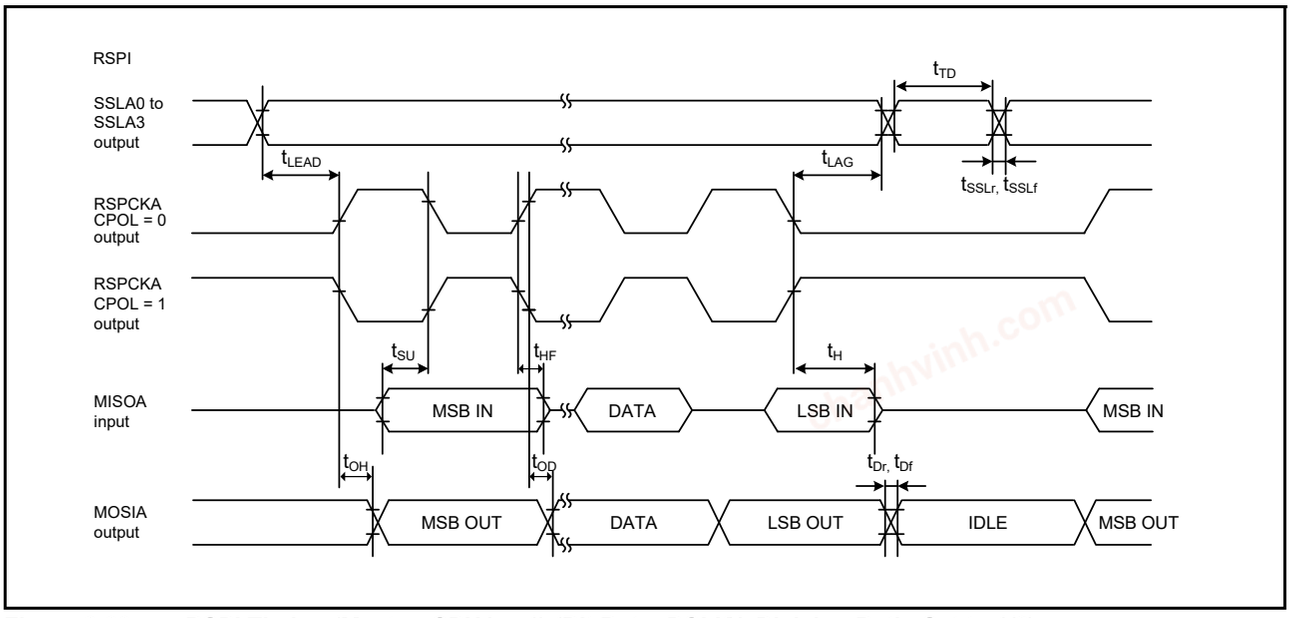


Figure 2.66 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

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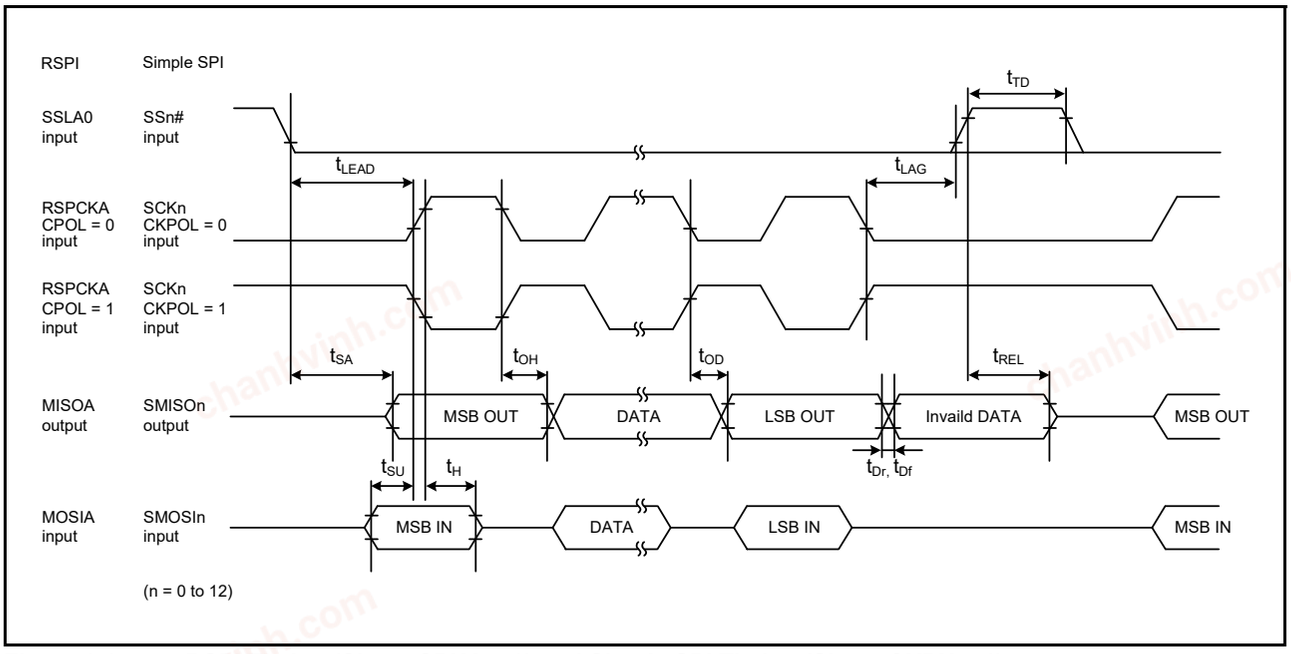


Figure 2.67 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

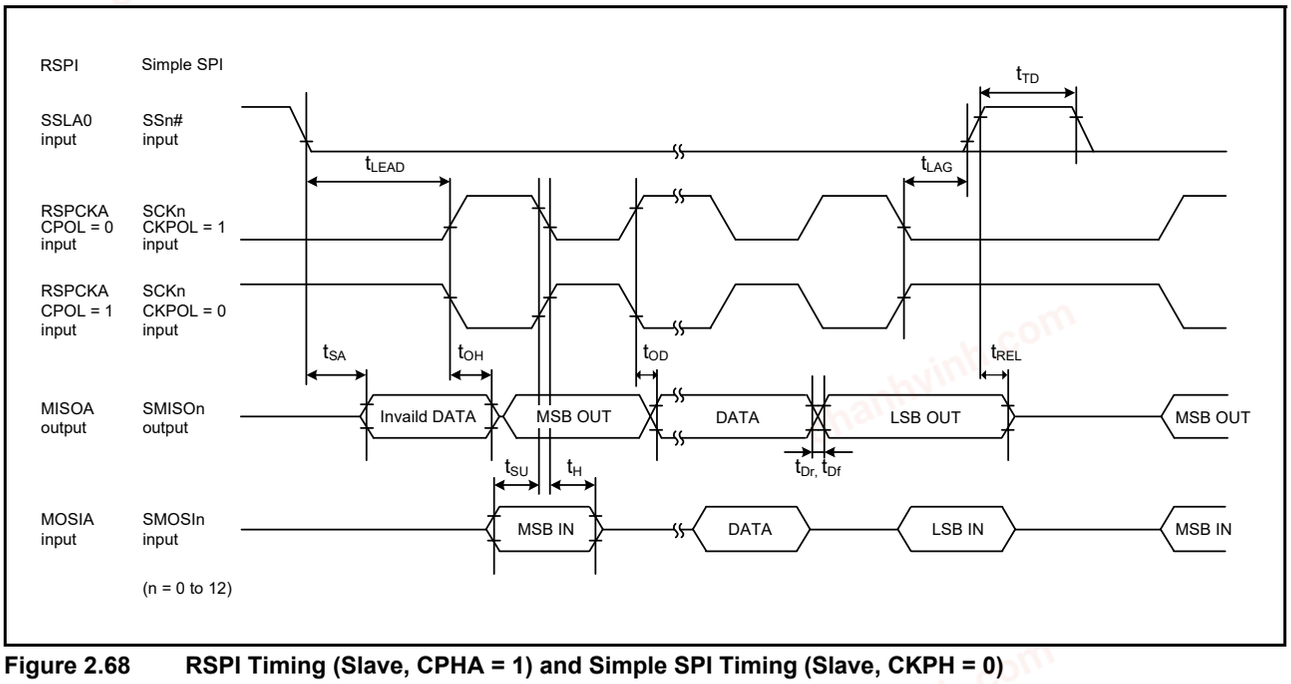


Figure 2.68 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

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Table 2.41 QSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions*2
QSPI	QSPCLK clock cycle	t_{QScyc}	2	4080	t_{PBcyc}	Figure 2.69
	Data input setup time	t_{Su}	6.5	—	ns	Figure 2.70, Figure 2.71
	Data input hold time	t_{IH}	5	—	ns	
	SS setup time	t_{LEAD}	1.5	8.5	t_{QScyc}	
	SS hold time	t_{LAG}	1	8	t_{QScyc}	
	Data output delay time	t_{OD}	—	10.0	ns	
	Data output hold time	t_{OH}	–5	—	ns	
	Successive transmission delay time	t_{TD}	1	8	t_{QScyc}	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the QSPI interface, the AC portion of the electrical characteristics is measured for each group.

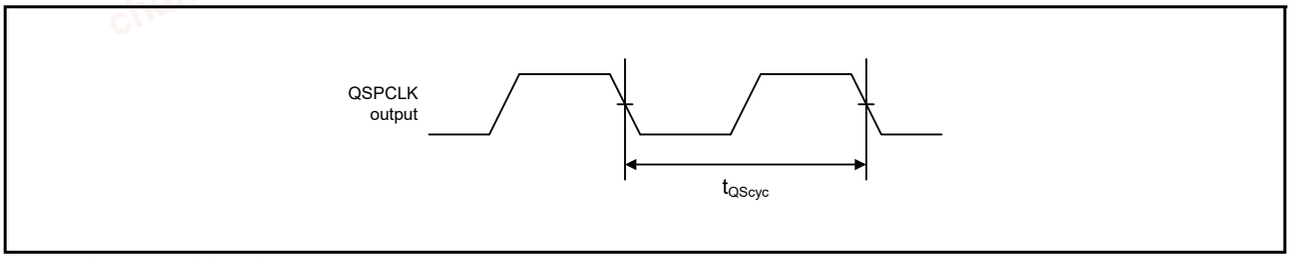


Figure 2.69 QSPI Clock Timing

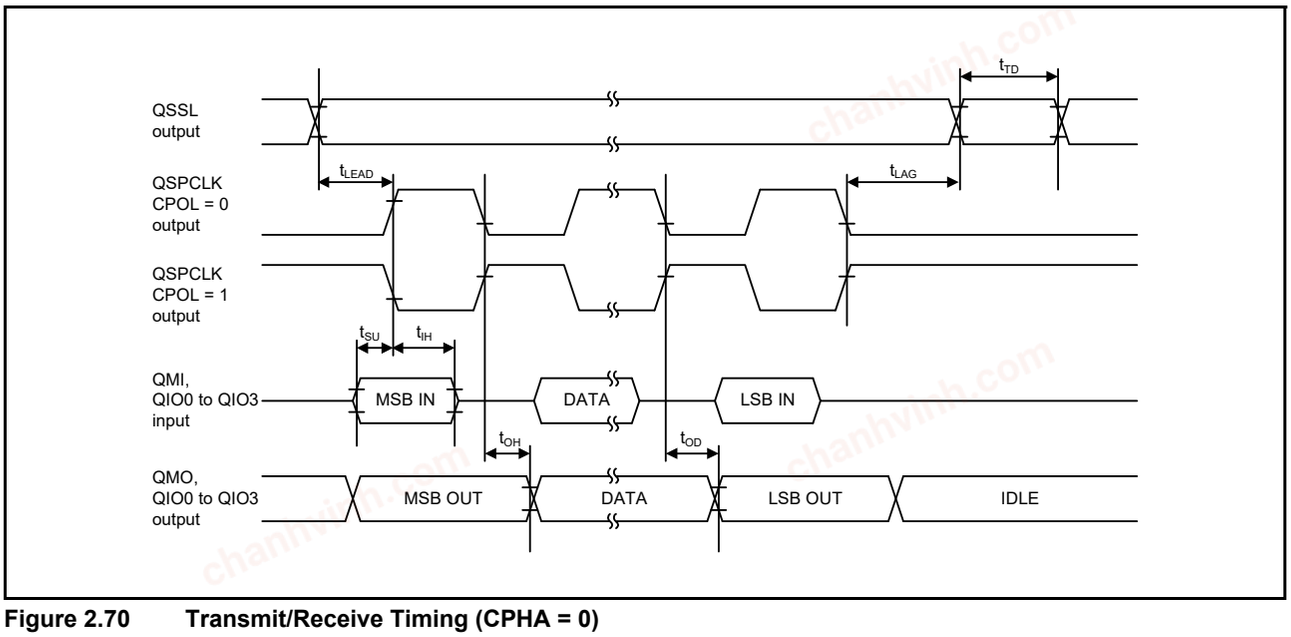


Figure 2.70 Transmit/Receive Timing (CPHA = 0)

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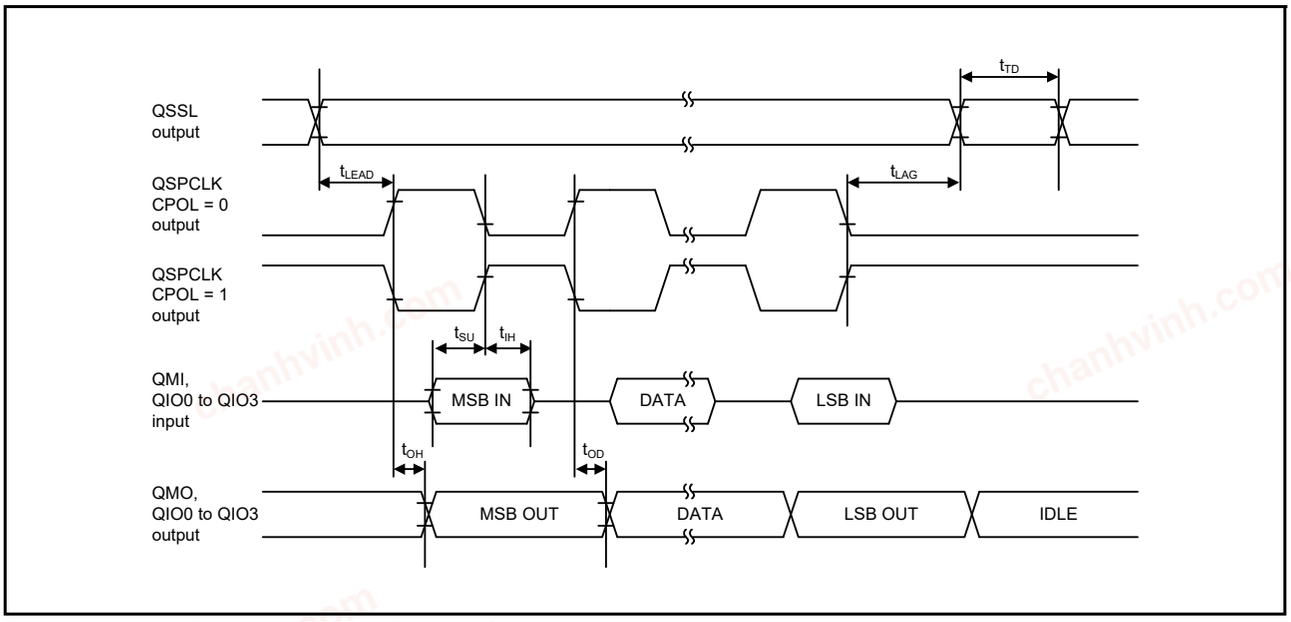


Figure 2.71 Transmit/Receive Timing (CPHA = 1)

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Table 2.42 RIIC Timing (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.72
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

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Table 2.43 RIIC Timing (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 240	—	ns	Figure 2.72
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 120	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 20	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{PBcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{PBcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle, t_{PBcyc}: PCLKB cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

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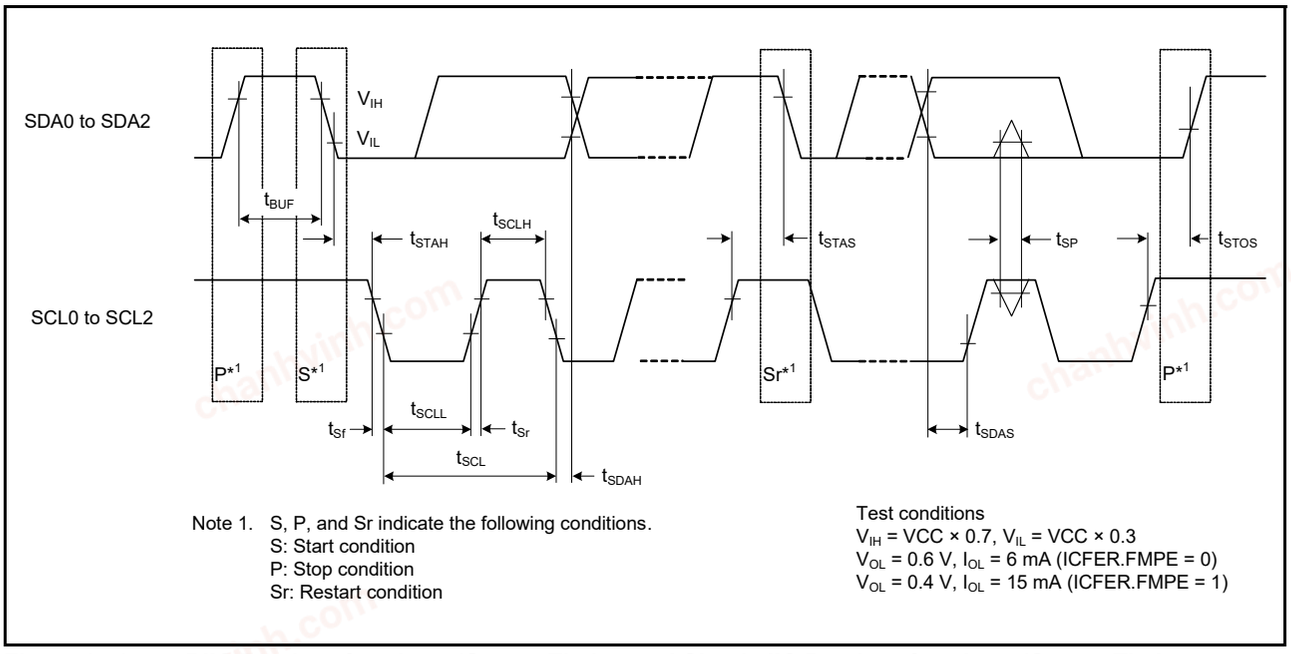


Figure 2.72 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

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Table 2.44 PMGI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
PMGI	PMGIn_MDC output cycle	t_{MDC}	80	—	ns	Figure 2.73
	PMGIn_MDIO setup time (relative to PMGIn_MDC↑)	t_{SMDIO}	20	—	ns	
	PMGIn_MDIO hold time (relative to PMGIn_MDC↑)	t_{HMDIO}	0	—	ns	
	PMGIn_MDIO output delay time (relative to PMGIn_MDC↑)	t_{DMDIO}	0	20	ns	

n = 0, 1

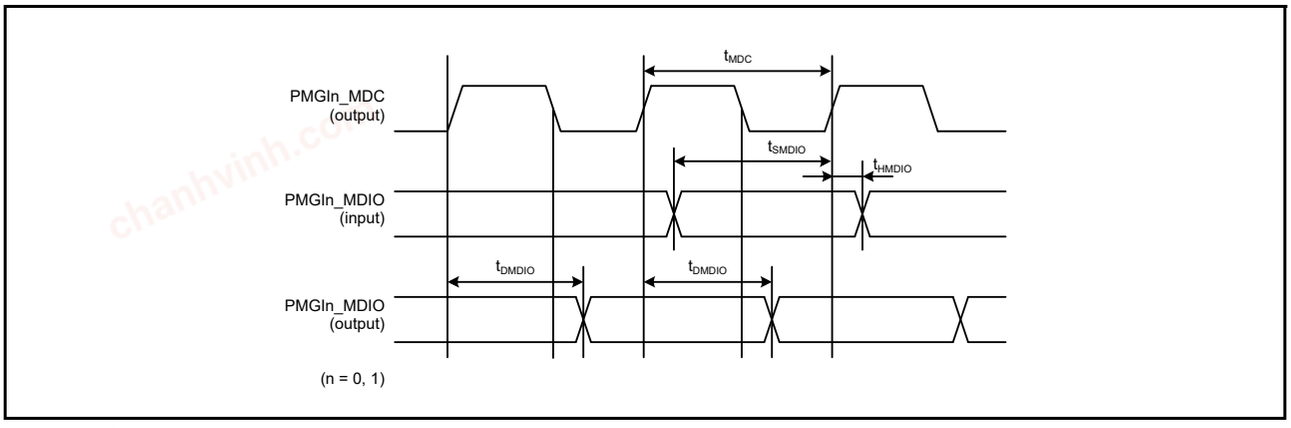


Figure 2.73 Timing of Serial Management Access

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Table 2.45 ESC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
MII: High-drive output for the high-speed interface is selected in the drive capacity selection control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ESC (MII)	CATn_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	CATn_TX_EN output delay time	t_{TENd}	1	25	ns	Figure 2.74
	CATn_ETXD0 to CATn_ETXD3 output delay time	t_{MTDd}	1	25	ns	
	CATn_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	CATn_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 2.75
	CATn_RX_DV hold time	t_{RDVh}	10	—	ns	
	CATn_ERXD0 to CATn_ERXD3 setup time	t_{MRDs}	10	—	ns	
	CATn_ERXD0 to CATn_ERXD3 hold time	t_{MRDh}	10	—	ns	
	CATn_RX_ER setup time	t_{RERs}	10	—	ns	Figure 2.76
	CATn_RX_ER hold time	t_{RERh}	10	—	ns	
ESC (MDIO)	CAT0_MDIO setup time (CAT0_MDC↑)	t_{SMDIO}	60	—	ns	Figure 2.77
	CAT0_MDIO hold time (CAT0_MDC↑)	t_{HMDIO}	0	—	ns	
	CAT0_MDIO output delay time (CAT0_MDC↓)	t_{DMDIO}	0	30	ns	

n = 0, 1

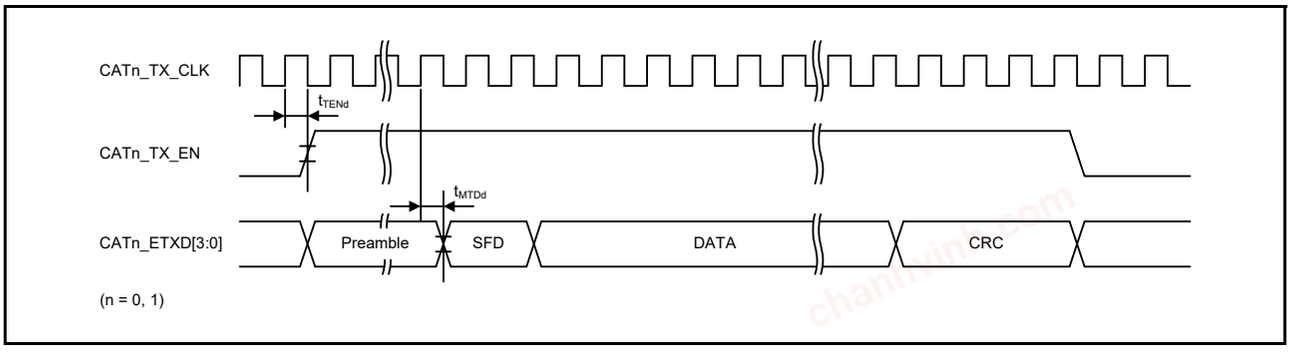


Figure 2.74 MII Transmission Timing (Normal Operation)

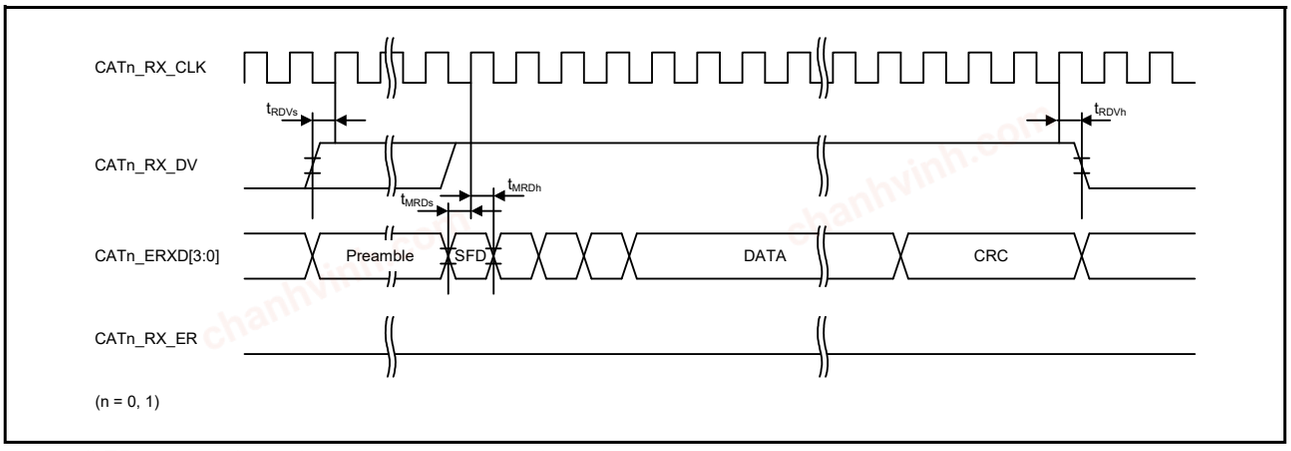


Figure 2.75 MII Reception Timing (Normal Operation)

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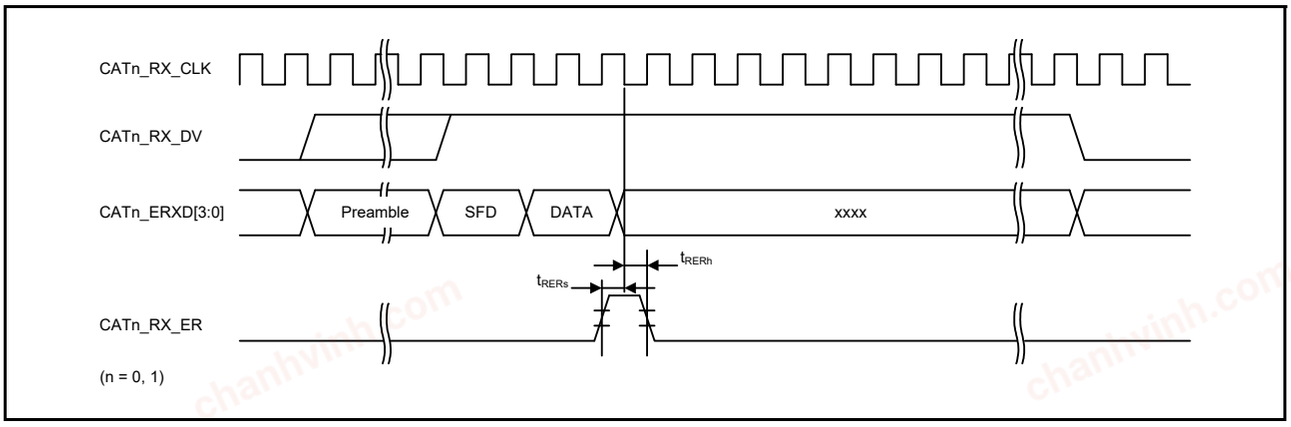


Figure 2.76 MII Reception Timing (Error Occurrence)

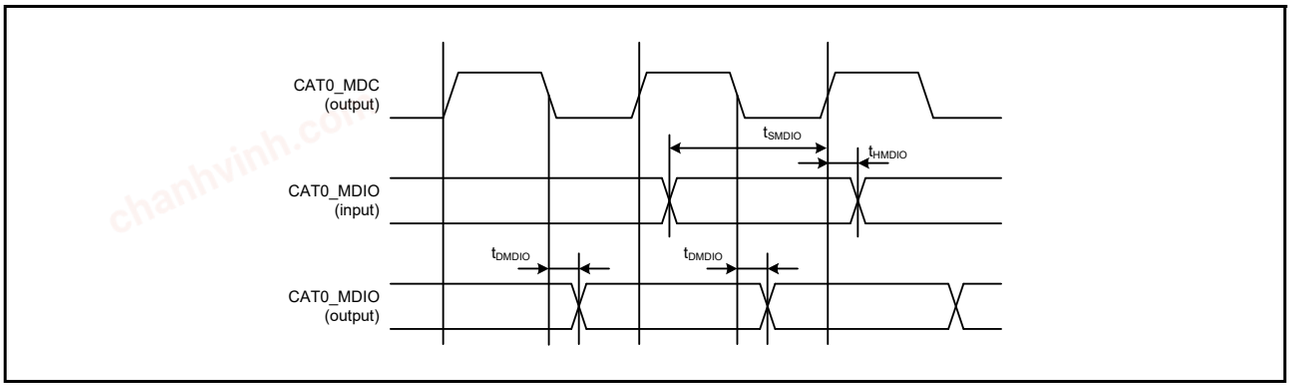


Figure 2.77 Timing of Serial Management Access

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Table 2.46 MMC Host Interface Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions*2
MMCIF	MMC_CLK clock cycle	t_{MMCPP}	2 × t_{PBcyc}	—	ns	Figure 2.78
	MMC_CLK clock high level width	t_{MMCWH}	6.5	—	ns	
	MMC_CLK clock low level width	t_{MMCWL}	6.5	—	ns	
	MMC_CLK clock rising time	t_{MMCLH}	—	3	ns	
	MMC_CLK clock falling time	t_{MMCHL}	—	3	ns	
	MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode)	$t_{MMCODLY}$	–6.6	6.6	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data setup	t_{MMCISU}	8	—	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data hold	t_{MMCIH}	2.5	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the MMC interface, the AC portion of the electrical characteristics is measured for each group.

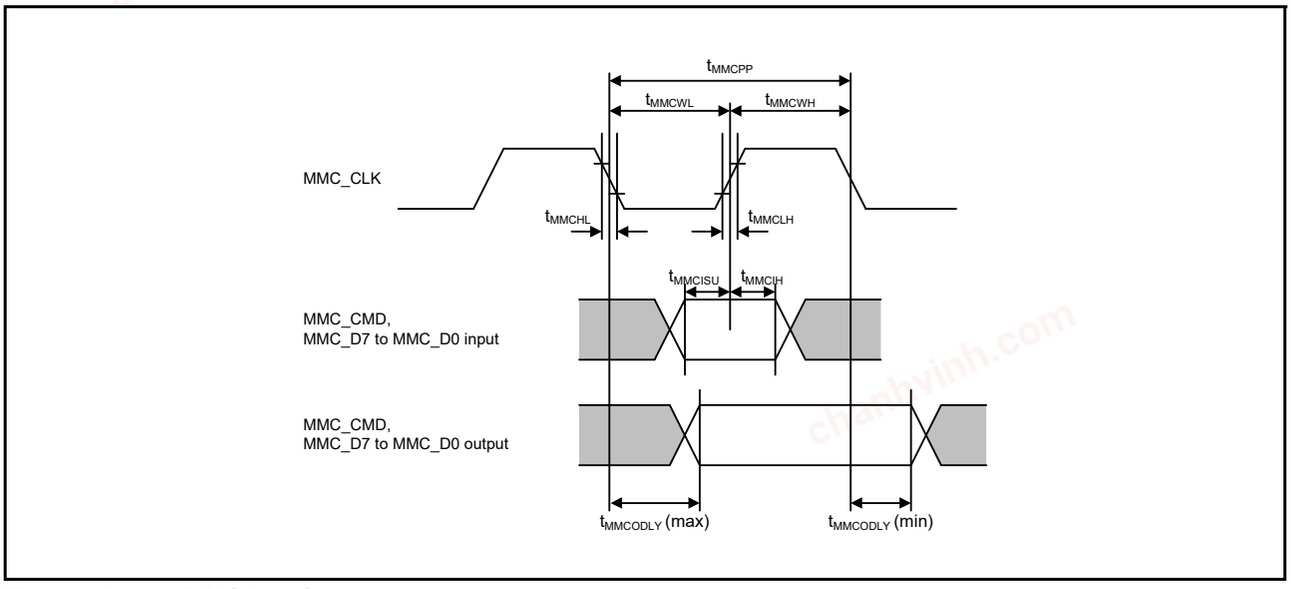


Figure 2.78 MMC Interface

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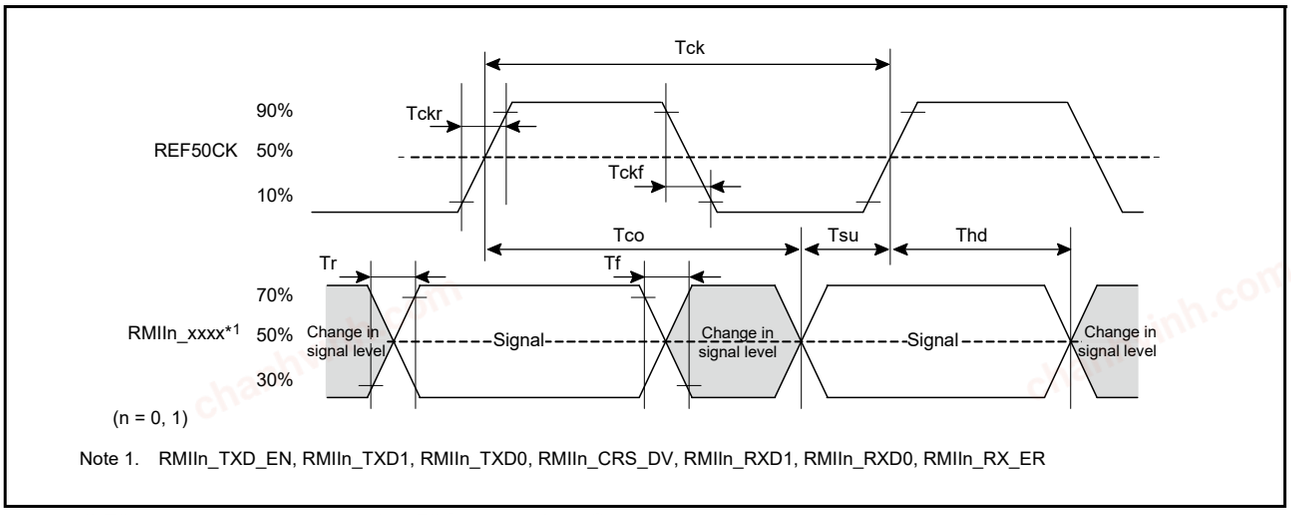
Table 2.47 ETHERC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
RMII: High-drive output for the high-speed interface is selected in the drive capacity selection control register.
MII: High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 2.79 to Figure 2.81
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMIIn_xxxx*1 output delay time	T_{co}	2.5	15.0	ns	
	RMIIn_xxxx*2 setup time	T_{su}	3	—	ns	
	RMIIn_xxxx*2 hold time	T_{hd}	1	—	ns	
	RMIIn_xxxx*1, *2 rise/fall time	T_r/T_f	—	5	ns	
	ETn_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 2.83
ETHERC (MII)	ETn_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ETn_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 2.84
	ETn_ETXD0 to ETn_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ETn_CRS setup time	t_{CRSs}	10	—	ns	
	ETn_CRS hold time	t_{CRSh}	10	—	ns	
	ETn_COL setup time	t_{COLs}	10	—	ns	Figure 2.85
	ETn_COL hold time	t_{COLh}	10	—	ns	
	ETn_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ETn_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 2.86
	ETn_RX_DV hold time	t_{RDVh}	10	—	ns	
	ETn_ERXD0 to ETn_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ETn_ERXD0 to ETn_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ETn_RX_ER setup time	t_{RERs}	10	—	ns	Figure 2.87
	ETn_RX_ER hold time	t_{RERh}	10	—	ns	
	ETn_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 2.88

n = 0, 1
Note 1. RMIIn_TXD_EN, RMIIn_TXD1, RMIIn_TXD0
Note 2. RMIIn_CRS_DV, RMIIn_RXD1, RMIIn_RXD0, RMIIn_RX_ER

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Note 1. RMIIn_TXD_EN, RMIIn_TXD1, RMIIn_TXD0, RMIIn_CRS_DV, RMIIn_RXD1, RMIIn_RXD0, RMIIn_RX_ER

Figure 2.79 Timing with the REF50CK and RMII Signals

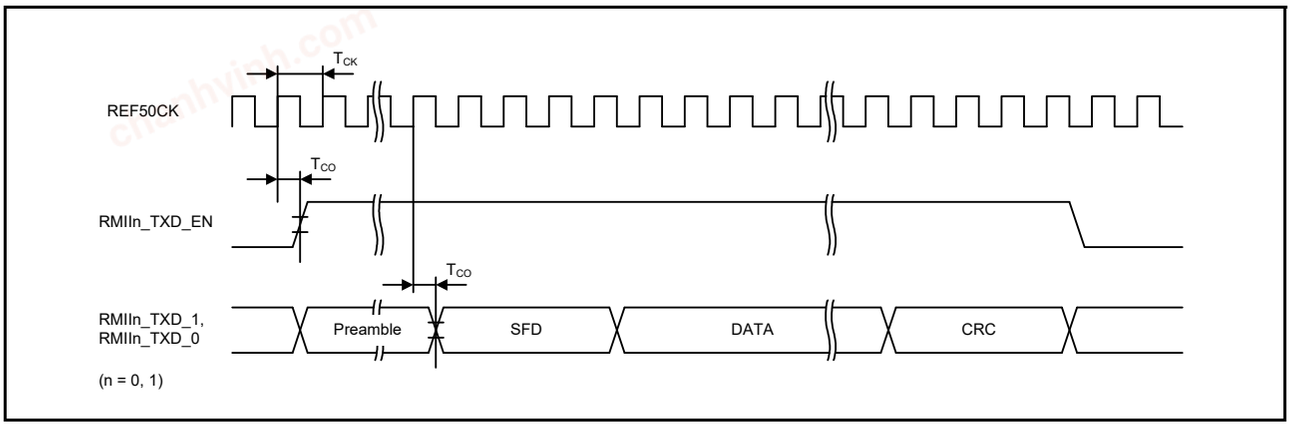


Figure 2.80 RMII Transmission Timing

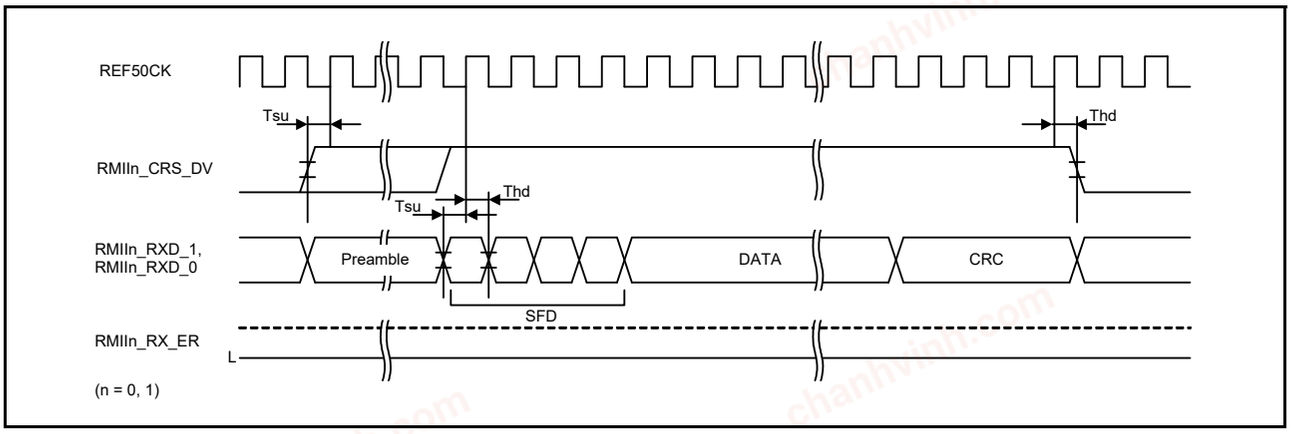


Figure 2.81 RMII Reception Timing (Normal Operation)

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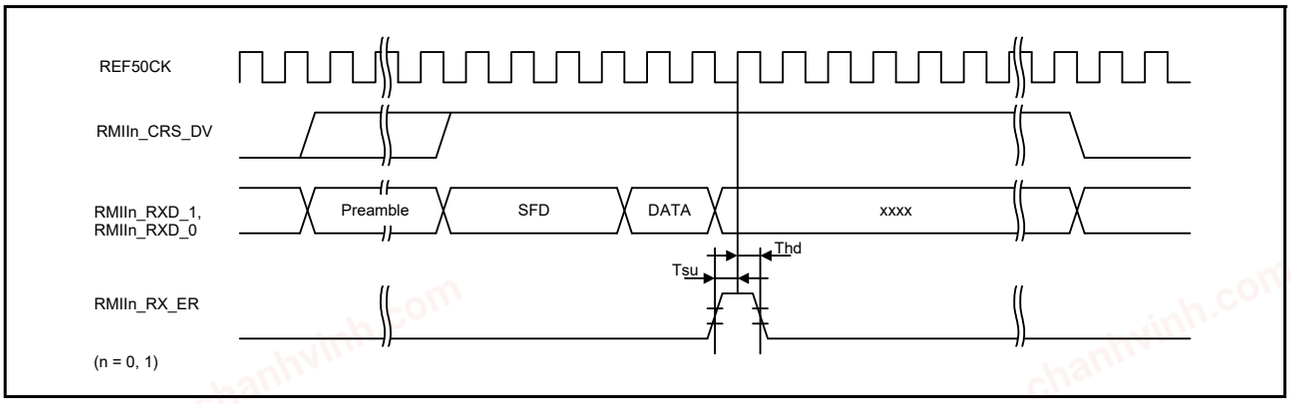


Figure 2.82 RMII Reception Timing (Error Occurrence)

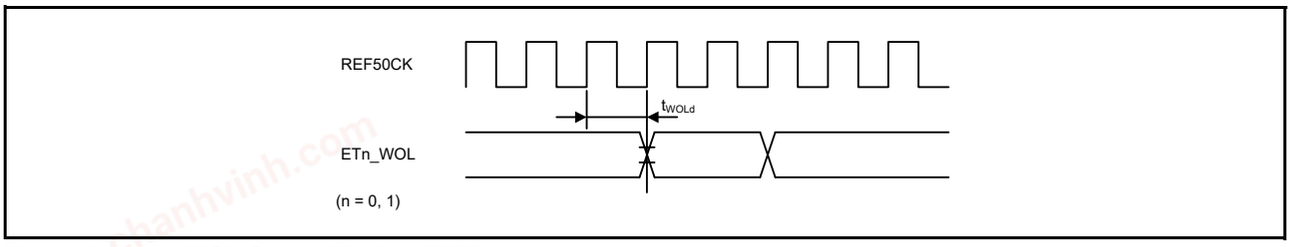


Figure 2.83 WOL Output Timing (RMII)

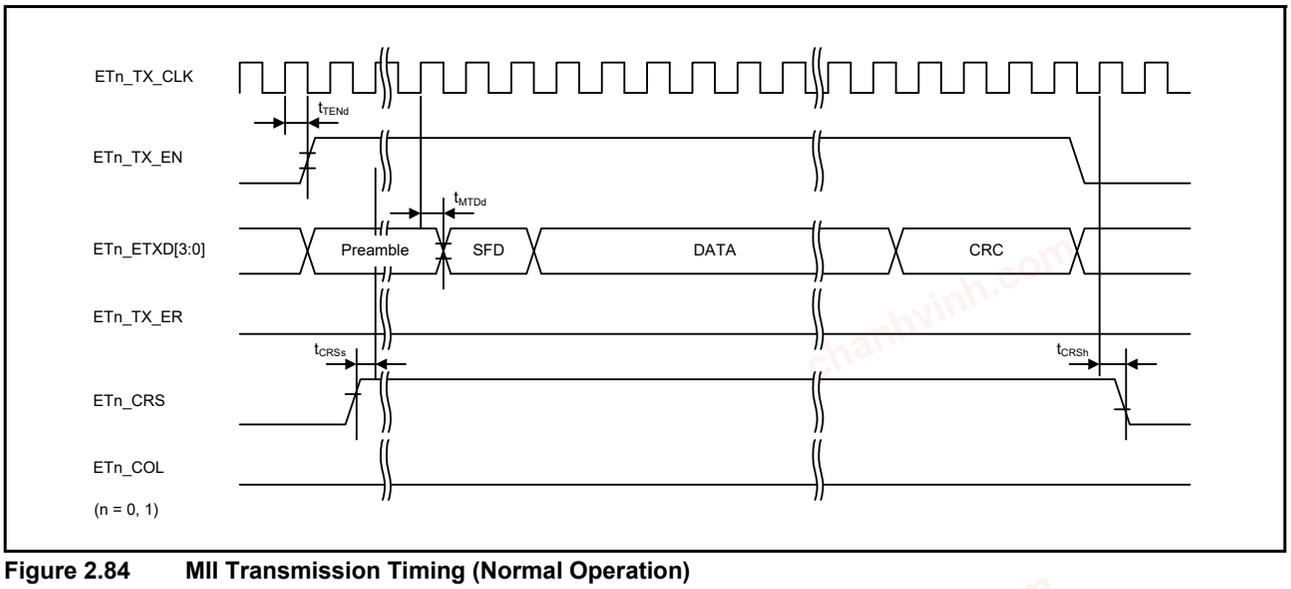


Figure 2.84 MII Transmission Timing (Normal Operation)

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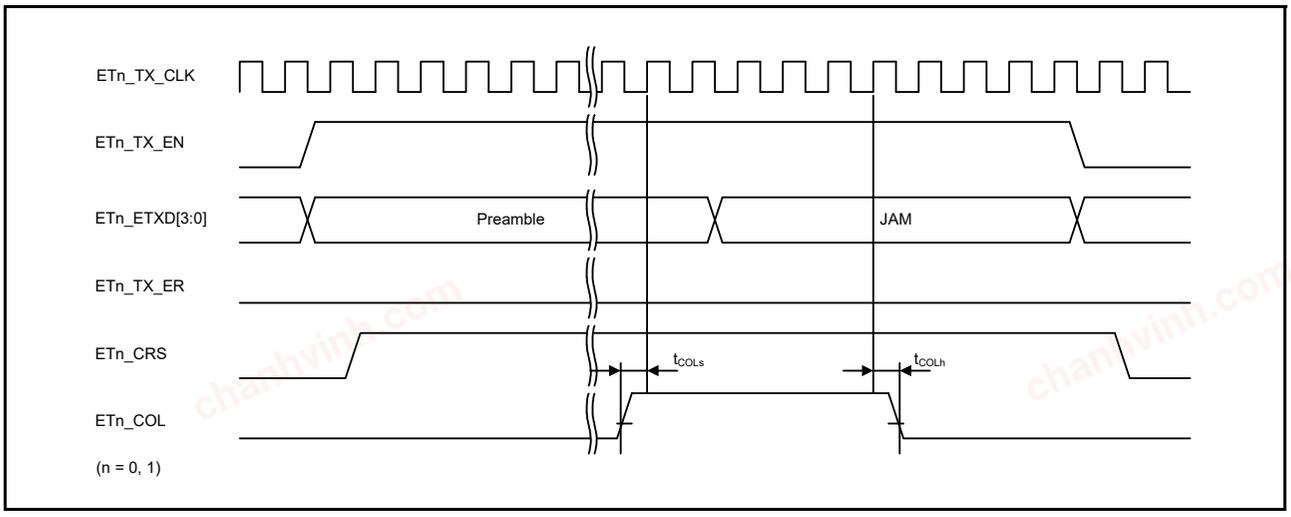


Figure 2.85 MII Transmission Timing (Conflict Occurrence)

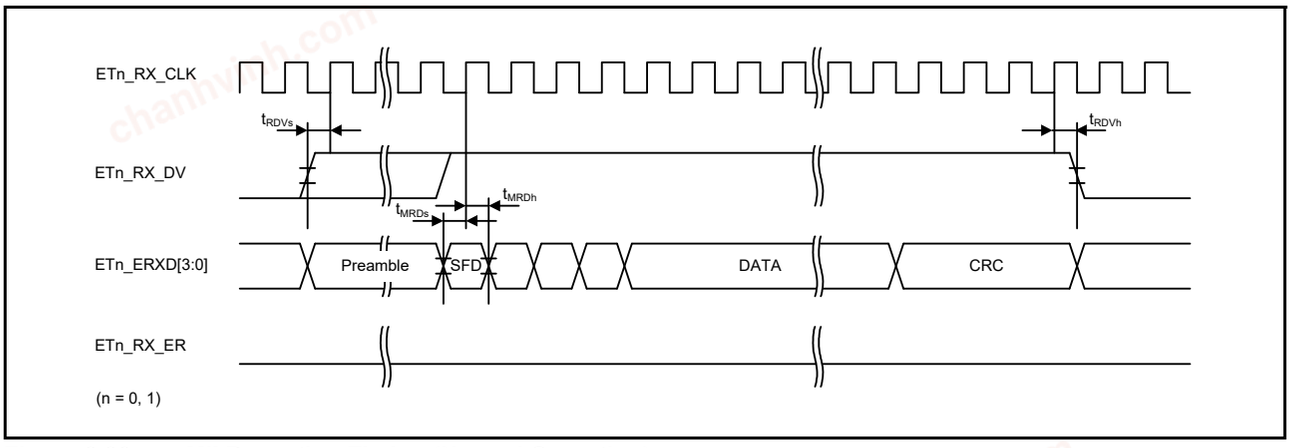


Figure 2.86 MII Reception Timing (Normal Operation)

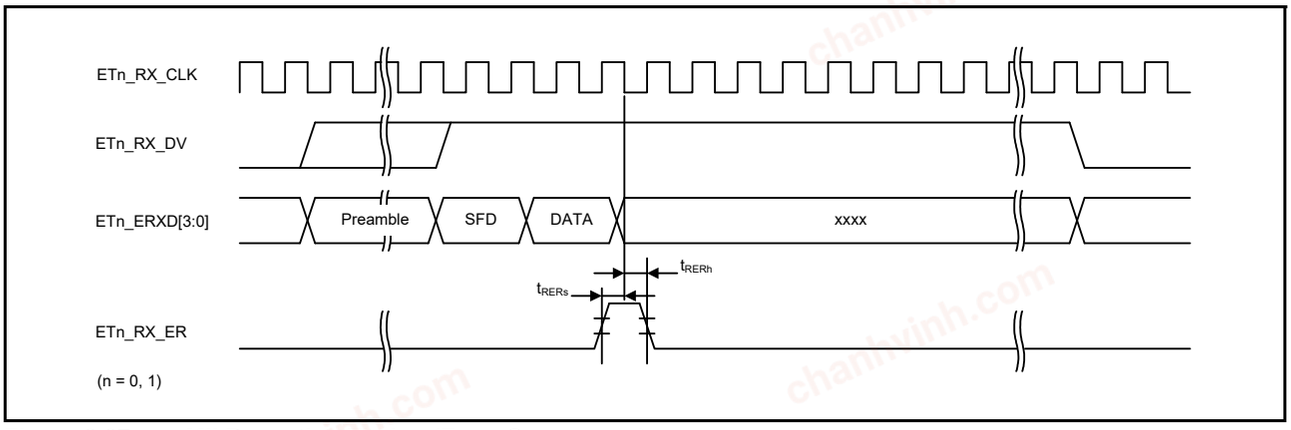


Figure 2.87 MII Reception Timing (Error Occurrence)

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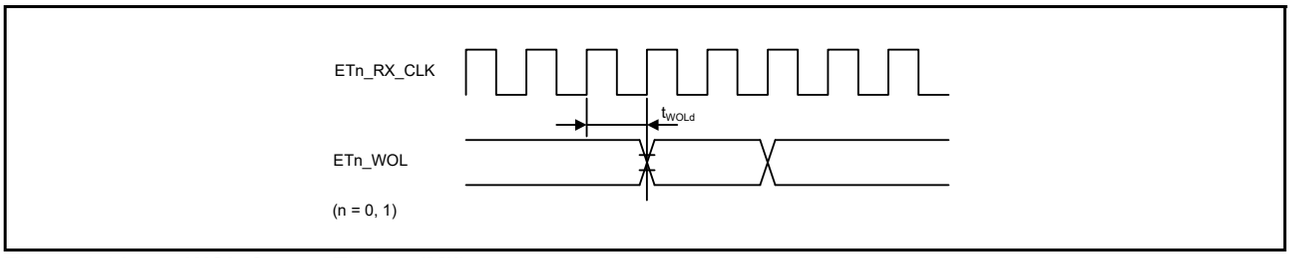


Figure 2.88 WOL Output Timing (MII)

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Table 2.48 PDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	—	ns	Figure 2.89
	PIXCLK input high pulse width	t_{PIXH}	10	—	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	—	ns	
	PIXCLK rising time	t_{PIXr}	—	5	ns	
	PIXCLK falling time	t_{PIXf}	—	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	—	ns	Figure 2.90
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	—	ns	
	PCKO rising time	t_{PCKr}	—	5	ns	
	PCKO falling time	t_{PCKf}	—	5	ns	
	VSYNC/HSYNC input setup time	t_{SYNCS}	10	—	ns	Figure 2.91
	VSYNC/HSYNC input hold time	t_{SYNCH}	5	—	ns	
	PIXD input setup time	t_{PIXDS}	10	—	ns	
	PIXD input hold time	t_{PIXDH}	5	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle

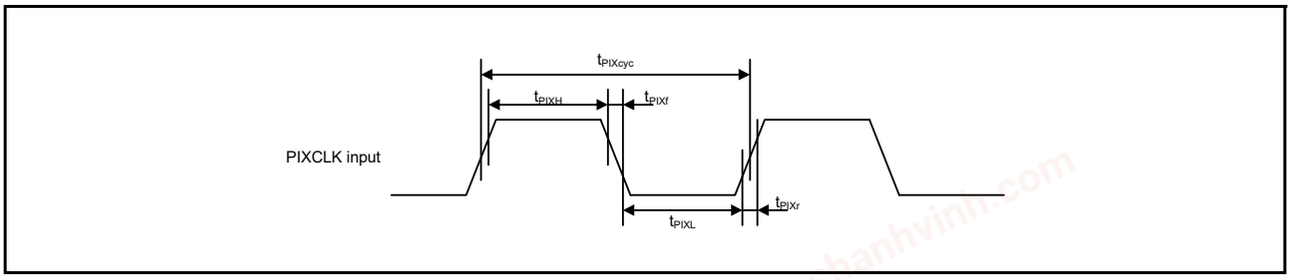


Figure 2.89 PDC Input Clock Timing

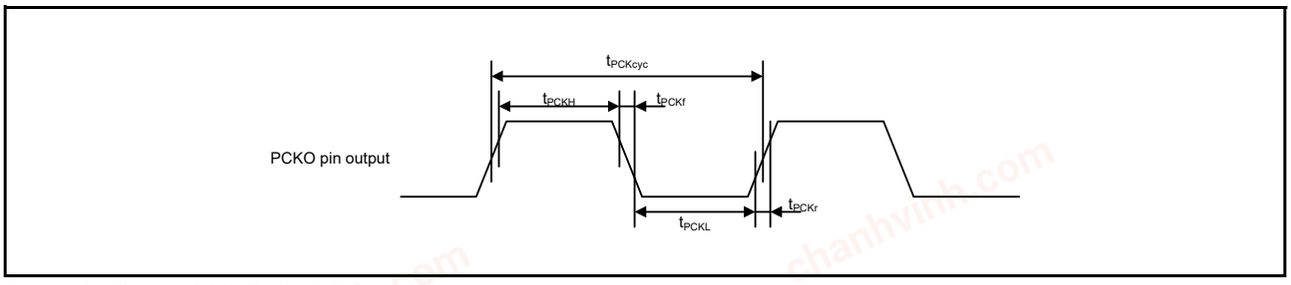


Figure 2.90 PDC Output Clock Timing

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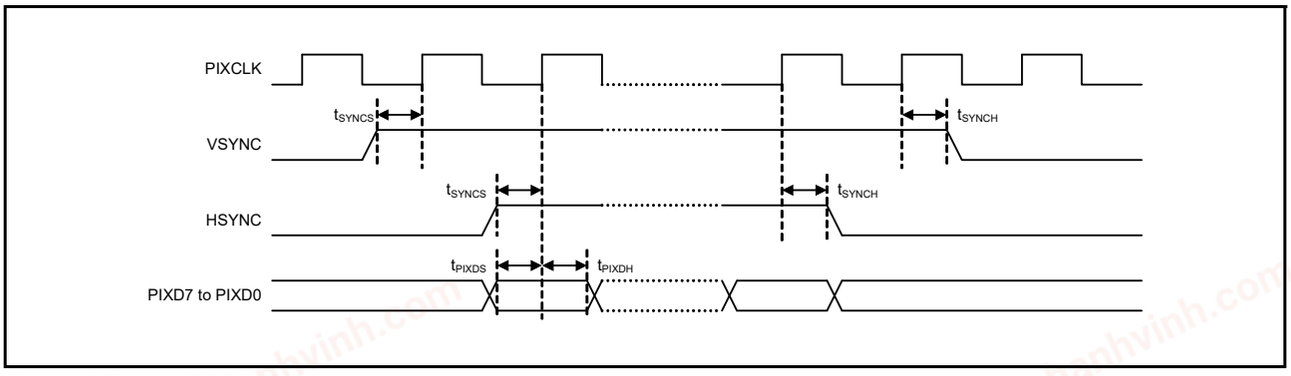


Figure 2.91 PDC AC Timing

Table 2.49 GLCDC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD_EXTCLK Input clock frequency	t_{Ecyc}	—	—	30*1	MHz	Figure 2.92
LCD_EXTCLK Input clock Low pulse width	t_{WL}	0.45	—	0.55	t_{Ecyc}	
LCD_EXTCLK Input clock High pulse width	t_{WH}	0.45	—	0.55		
LCD_CLK Output clock frequency	t_{Lcyc}	—	—	30*1	MHz	Figure 2.93
LCD_CLK Output clock Low pulse width	t_{LOL}	0.4	—	0.6	t_{Lcyc}	
LCD_CLK Output clock High pulse width	t_{LOH}	0.4	—	0.6	t_{Lcyc}	
LCD data output Delay timing	t_{DD}	–3.5*2	—	4*2	ns	Figure 2.94

Note 1. Parallel RGB888,666,565: Max. 27 MHz
Serial RGB888: Max. 30 MHz (4x speed)
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc) to indicate group membership appended to their names as groups.
For the GLCDC interface, the AC portion of the electrical characteristics is measured for each group.
If we use group “-A” and “-B” combination, “LCD data output Delay timing (t_{DD})” is Min = –5.0 ns, Max = 5.5 ns.

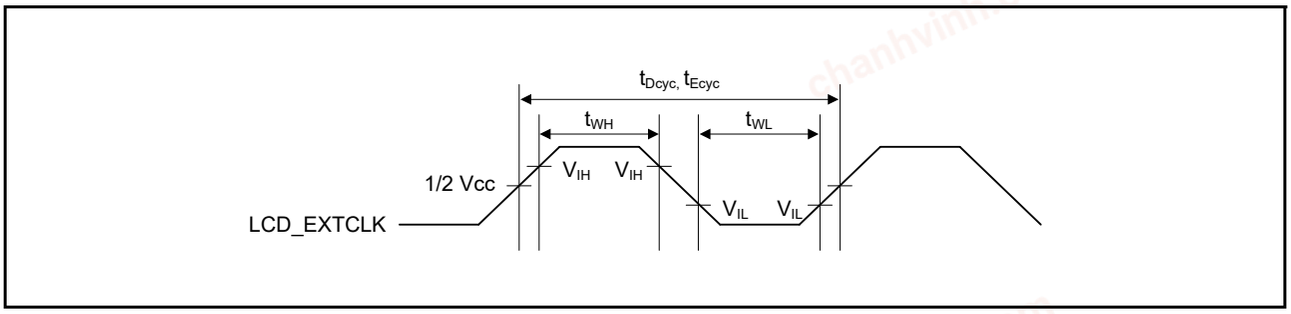


Figure 2.92 LCD_EXTCLK Clock Input Timing

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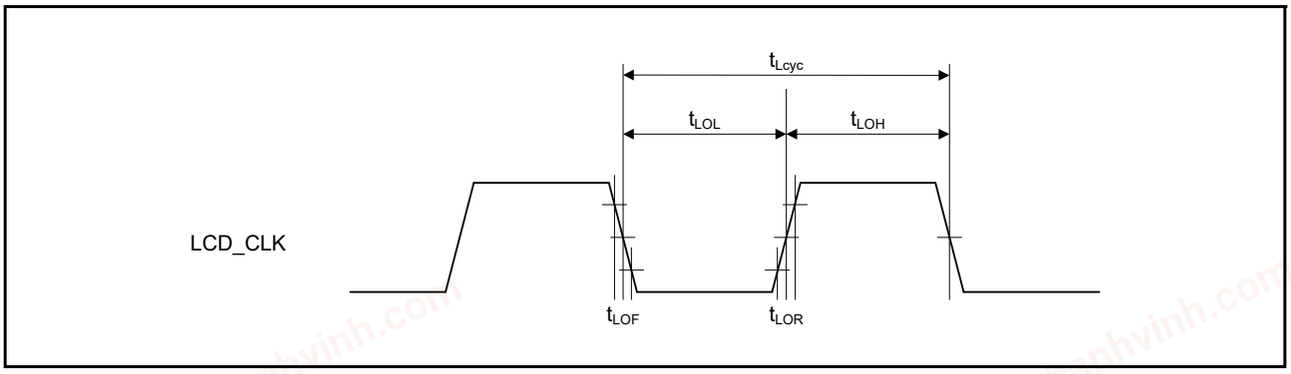


Figure 2.93 LCD_CLK Clock Output Timing

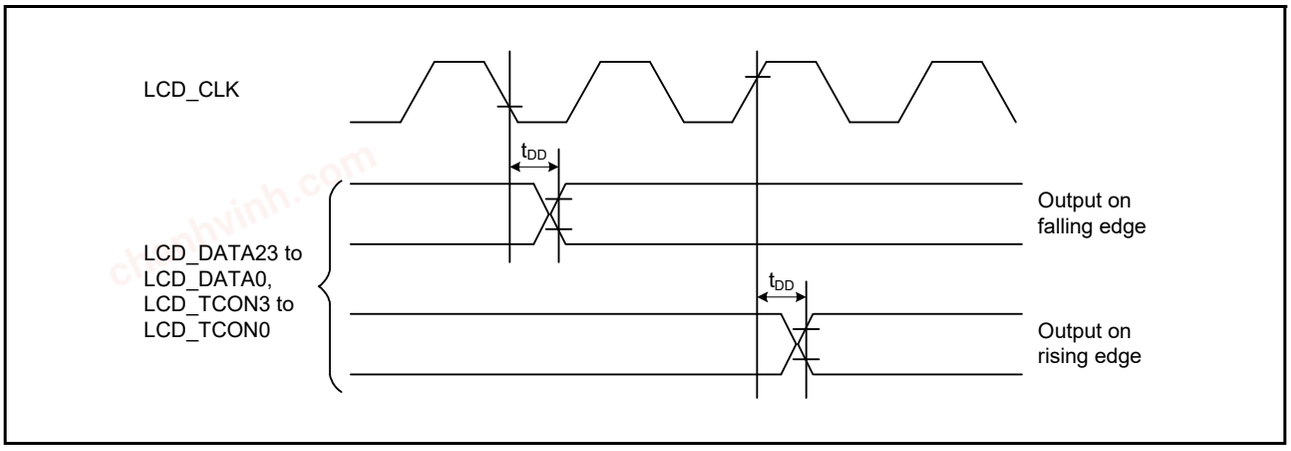


Figure 2.94 LCD Output Data Timing

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Table 2.50 Δ-Σ Interface Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
DSMIF	Clock cycle	Master	t_{DScyc}	2	32	t_{PBcyc}	Figure 2.95
		Slave		40	200	ns	
	Clock high level	Master	t_{DSCKWH}	16	—	ns	
		Slave		16	—	ns	
	Clock low level	Master	t_{DSCKWL}	16	—	ns	
		Slave		16	—	ns	
	Setup time	Master	t_{SU}	15	—	ns	Figure 2.96, Figure 2.97
		Slave		10	—	ns	
	Hold time	Master	t_H	0	—	ns	
		Slave		10	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle

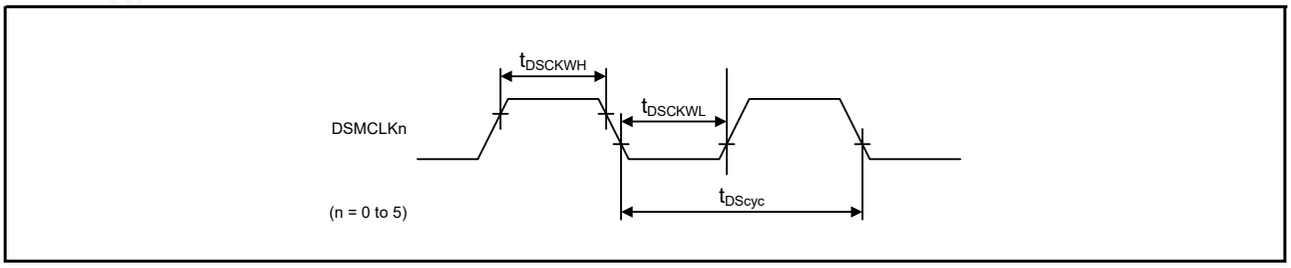


Figure 2.95 Clock Input/Output Timing

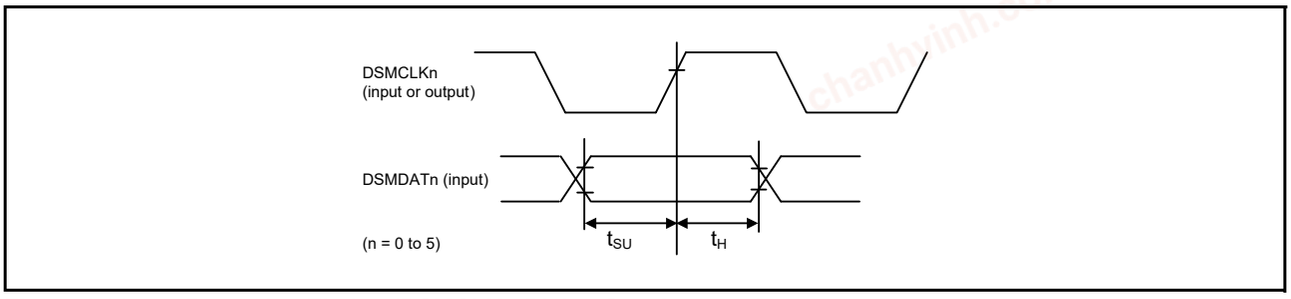


Figure 2.96 Reception Timing (DSMCLKn Rising Synchronous)

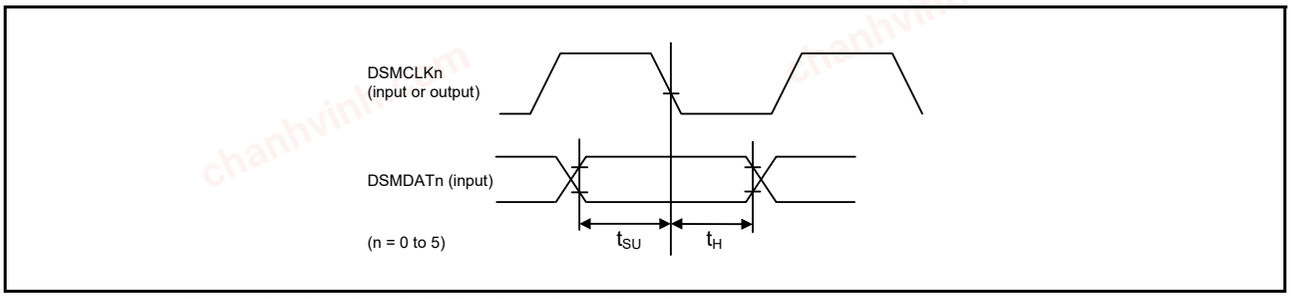


Figure 2.97 Reception Timing (DSMCLKn Falling Synchronous)

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Table 2.51 SDHI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6V, 2.7V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, Ta = T_{opr},
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions*1
SDHI	SDHI_CLK output cycle time	$t_{PP(SD)}$	20	—	ns	Figure 2.98
	SDHI_CLK output width at high level	$t_{WH(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK output width at low level	$t_{WL(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK output rising time	$t_{TLH(SD)}$	—	3	ns	
	SDHI_CLK output falling time	$t_{THL(SD)}$	—	3	ns	
	SDHI_CMD, SDHI_D3 to SDHI_D0 output data delay (data transfer mode)	$t_{ODLY(SD)}$	–6.5	4	ns	
	SDHI_CMD, SDHI_D3 to SDHI_D0 input data setup time	$t_{ISU(SD)}$	6	—	ns	
	SDHI_CMD, SDHI_D3 to SDHI_D0 input data hold time	$t_{IH(SD)}$	2	—	ns	

Note 1. We recommend using pin names that have a letter (“-A”, “-B”, etc.) to indicate group membership per group in the test. For the SDHI, the AC portion of the electrical characteristics is measured per group.

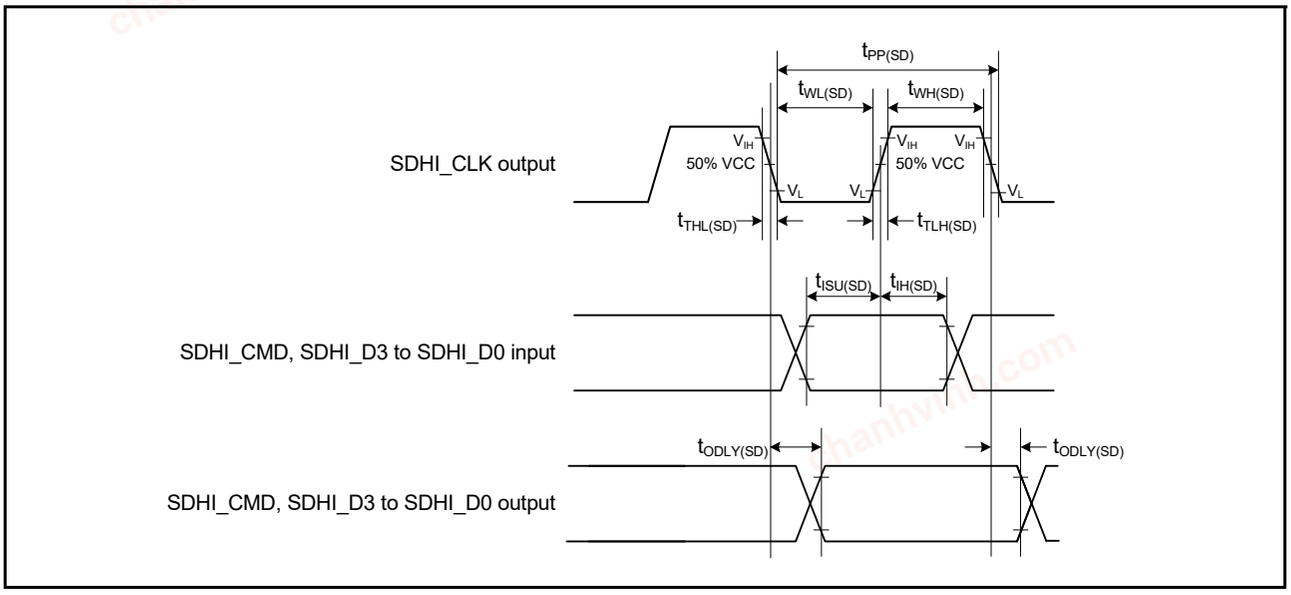


Figure 2.98 SD Host Interface Input/Output Signal Timing

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2.5 USB Characteristics

Table 2.52 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz, PCLKA = 8 to 120 MHz,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.99
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
Pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

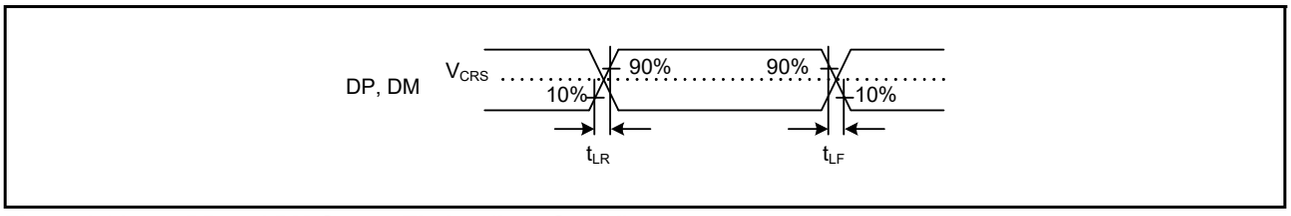


Figure 2.99 DP and DM Output Timing (Low Speed)

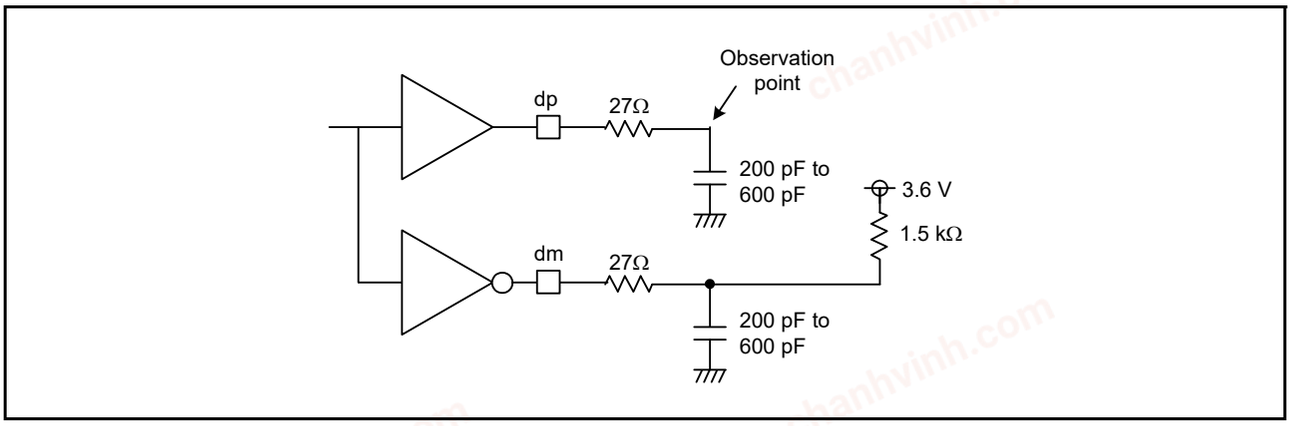


Figure 2.100 Test Circuit (Low Speed)

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Table 2.53 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz, PCLKA = 8 to 120 MHz,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.101
	Rise time	t_{FR}	4	—	20	ns	
	Fall time	t_{FF}	4	—	20	ns	
	Rise/fall time ratio	t_{FR} / t_{FF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	Rs = 27 Ω included
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	kΩ	Idle state
			1.425	—	3.090	kΩ	At transmission and reception
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

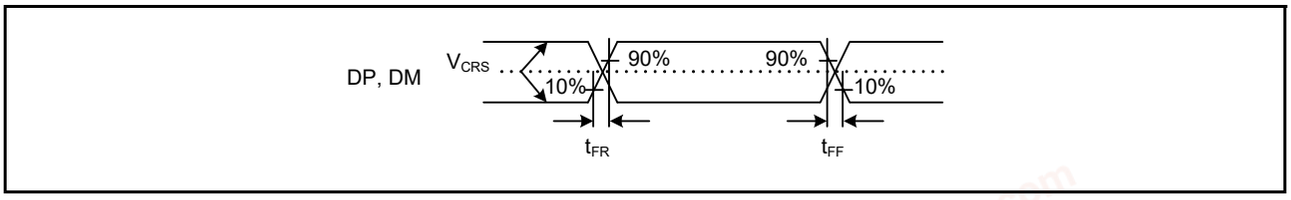


Figure 2.101 DP and DM Output Timing (Full-Speed)

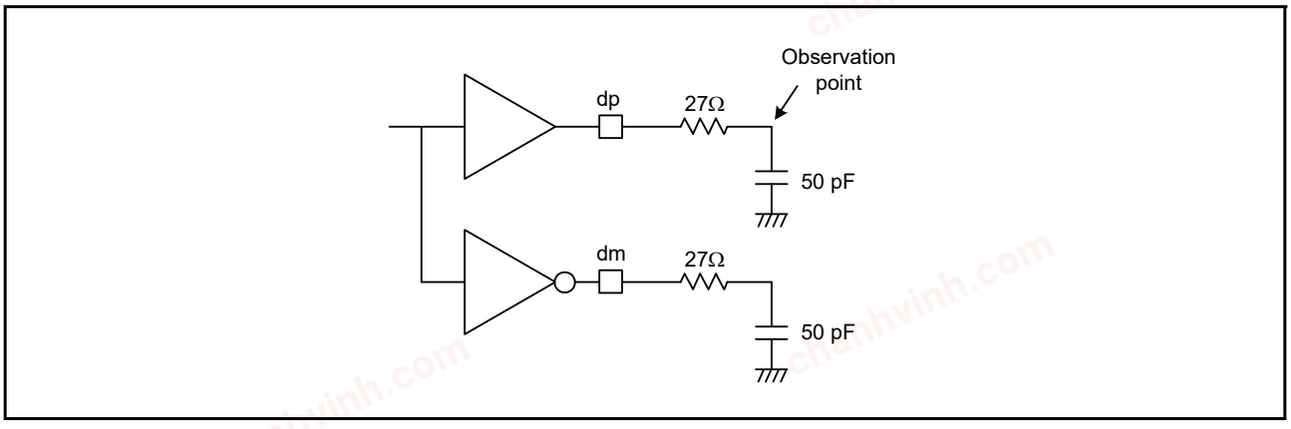


Figure 2.102 Test Circuit (Full-Speed)

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2.6 A/D Conversion Characteristics

Table 2.54 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, $T_a = T_{opr}$, Source impedance = 1.0 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLKC = 60 MHz)	1.06 (0.4 + 0.25) *2	—	—	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error	—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error	—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 – 0.25 V
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±3.0	±5.5	LSB	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±1.5	±3.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	20	µs	
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLKC = 60 MHz)	0.48 (0.267)*2	—	—	µs	Sampling in 16 states
	Offset error	—	±1.0	±2.5	LSB	
	Full-scale error	—	±1.0	±2.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.5	±4.5	LSB	
	DNL differential nonlinearity error	—	±0.5	±1.5	LSB	
	INL integral nonlinearity error	—	±1.0	±2.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

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Table 2.55 12-Bit A/D (Unit 1) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 1 MHz to 60 MHz, $T_a = T_{opr}$, Source impedance = 1.0 kΩ

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	8	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 60 MHz)	0.88 (0.633)*2	—	—	µs	Sampling in 38 states (ADSAM.SAM = 1)
Conversion time*1 (Operation at PCLKD = 30 MHz)	1 (0.500)*2	—	—	µs	Sampling in 15 states (ADSAM.SAM = 1)
Analog input capacitance	—	—	30	pF	
Offset error	—	±2.0	±3.5	LSB	
Full-scale error	—	±2.0	±3.5	LSB	
Quantization error	—	±0.5	—	LSB	
Absolute accuracy	—	±4.0	±6.0	LSB	
DNL differential nonlinearity error (Operation at PCLKD = 60 MHz)	—	±1.5	±4.0	LSB	
DNL differential nonlinearity error (Operation at PCLKD = 30 MHz)	—	±1.5	±2.5	LSB	
INL integral nonlinearity error (Operation at PCLKD = 60 MHz)	—	±2.0	±4.0	LSB	
INL integral nonlinearity error (Operation at PCLKD = 30 MHz)	—	±2.0	±3.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 2.56 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 60 MHz, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.13	1.18	1.23	V	

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2.7 D/A Conversion Characteristics

Table 2.57 D/A Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	12	12	12	Bit	
Unbuffered output	Absolute accuracy	—	—	—	±6.0	LSB	2-MΩ resistive load 10-bit conversion
	Differential nonlinearity error	DNL	—	±1.0	±2.0	LSB	2-MΩ resistive load
	Output resistance	R_O	—	8.6	—	kΩ	
	Setting time	t_S	—	—	3	μs	20-pF capacitive load
Buffered output	Load resistance	R_L	5	—	—	kΩ	
	Load capacitance	C_L	—	—	50	pF	
	Output voltage	V_O	0.2	—	AVCC1 – 0.2	V	
	Differential nonlinearity error	DNL	—	±1.0	±2.0	LSB	
	Integral nonlinearity error	INL	—	±2.0	±4.0	LSB	
	Setting time	t_S	—	—	4	μs	

2.8 Temperature Sensor Characteristics

Table 2.58 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4	—	mV/°C	
Output voltage (at 25°C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	μs	
Sampling time*1	4.15	—	—	μs	

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

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2.9 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.59 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V_{POR}	2.5	2.6	2.7	V	Figure 2.103
		Low power consumption function enabled*2		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.104
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.105
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.106
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.6	—	ms	Figure 2.103
	LVD0 reset time		t_{LVD0}	—	0.70	—		Figure 2.104
	LVD1 reset time		t_{LVD1}	—	0.57	—		Figure 2.105
	LVD2 reset time		t_{LVD2}	—	0.57	—		Figure 2.106
Minimum VCC down time			t_{VOFF}	200	—	—	µs	Figure 2.103, Figure 2.104
Response delay time			t_{det}	—	—	200	µs	Figure 2.103 to Figure 2.106
LVD operation stabilization time (after LVD is enabled)			$T_{d(E-A)}$	—	—	10	µs	Figure 2.105, Figure 2.106
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.
Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.
Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

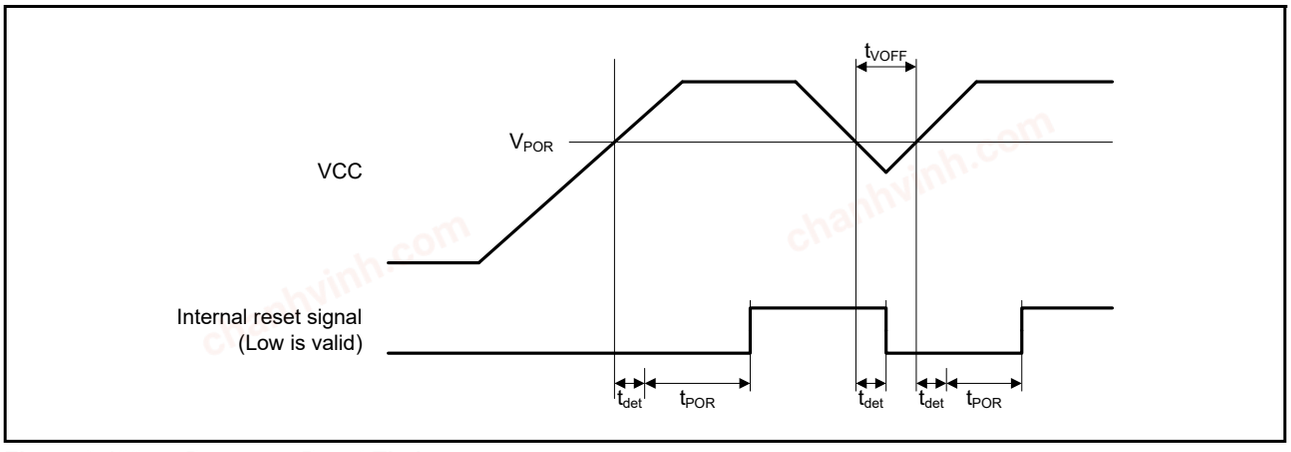


Figure 2.103 Power-on Reset Timing

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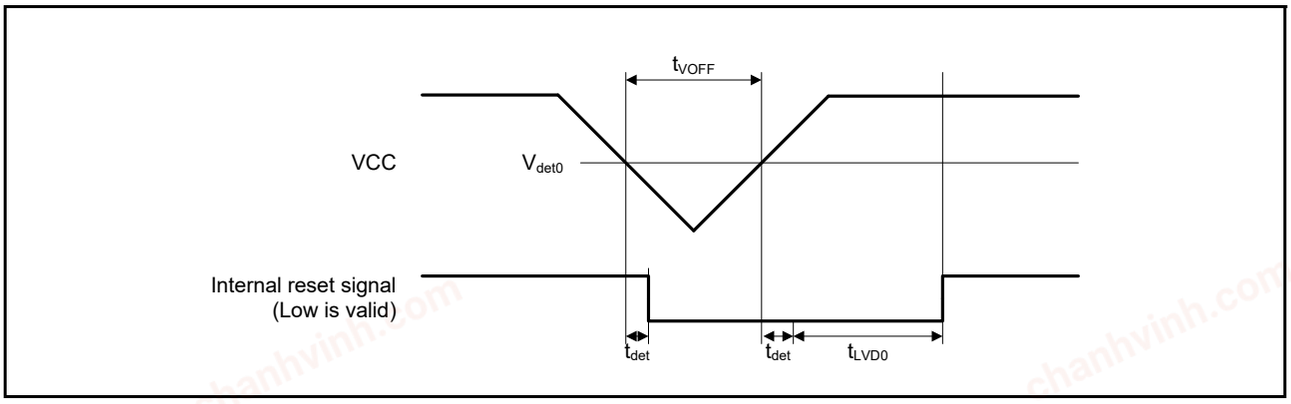


Figure 2.104 Voltage Detection Circuit Timing (V_{det0})

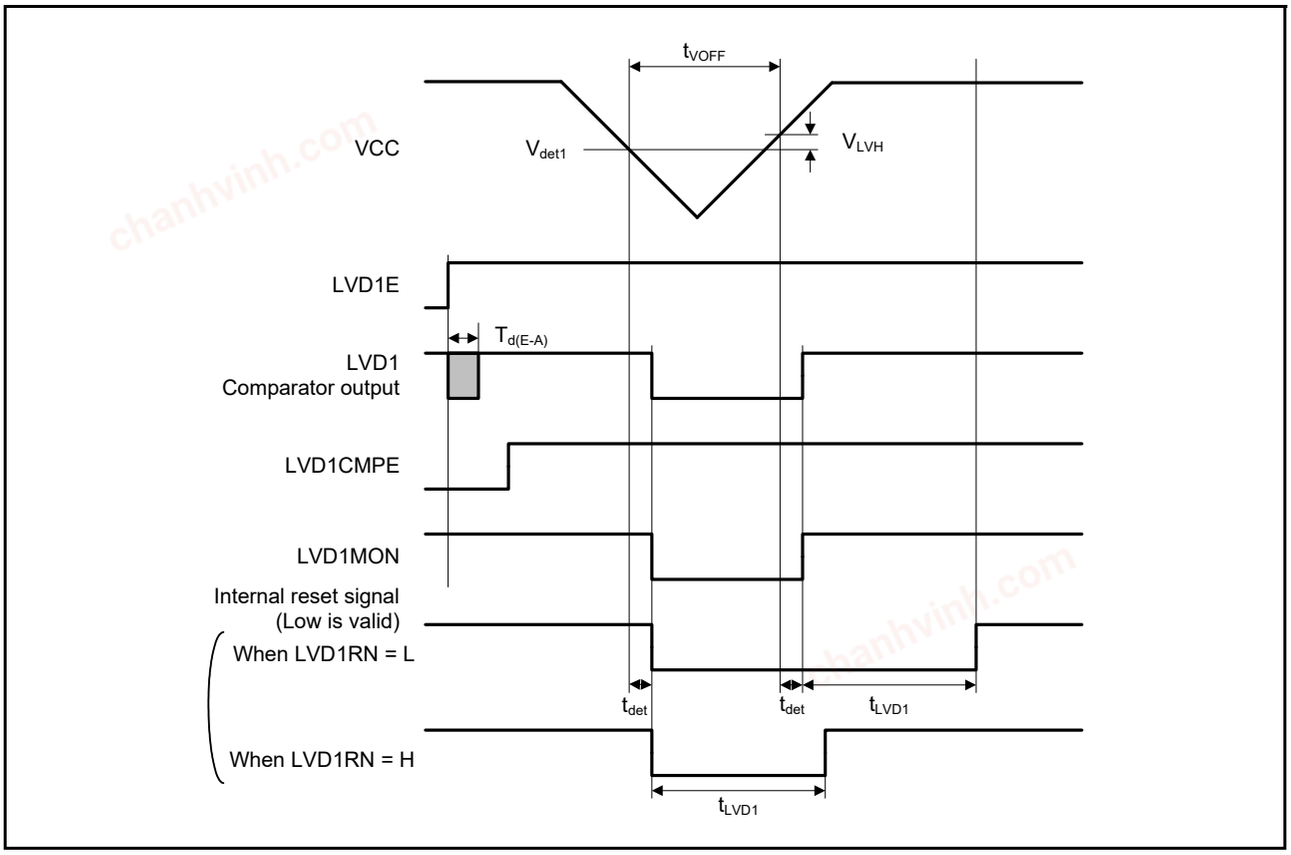


Figure 2.105 Voltage Detection Circuit Timing (V_{det1})

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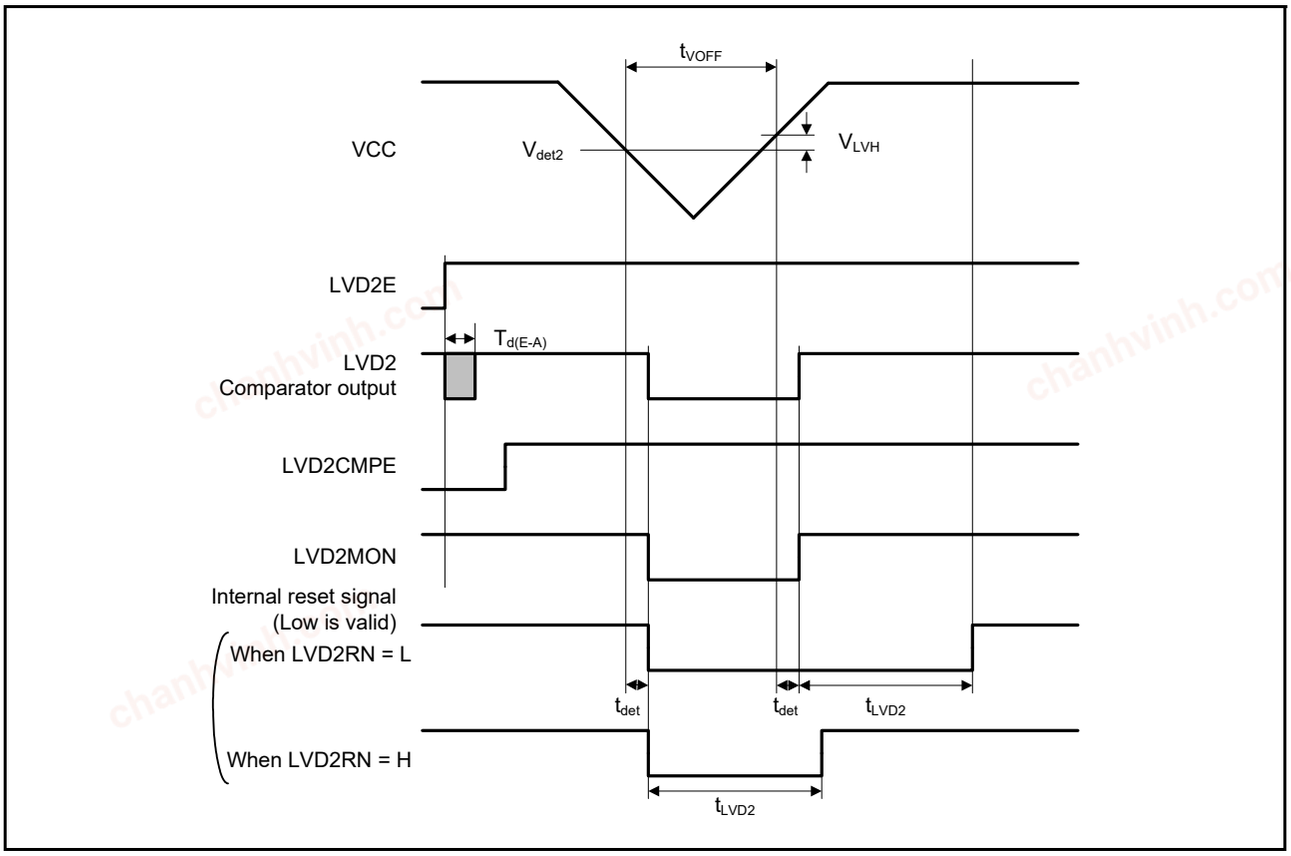


Figure 2.106 Voltage Detection Circuit Timing (V_{det2})

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2.10 Oscillation Stop Detection Timing

Table 2.60 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.107

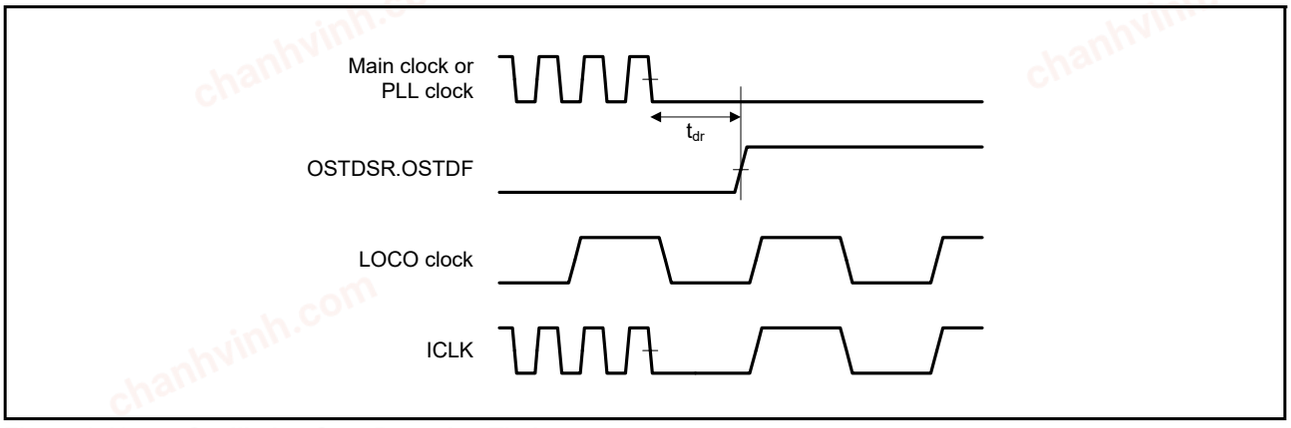


Figure 2.107 Oscillation Stop Detection Timing

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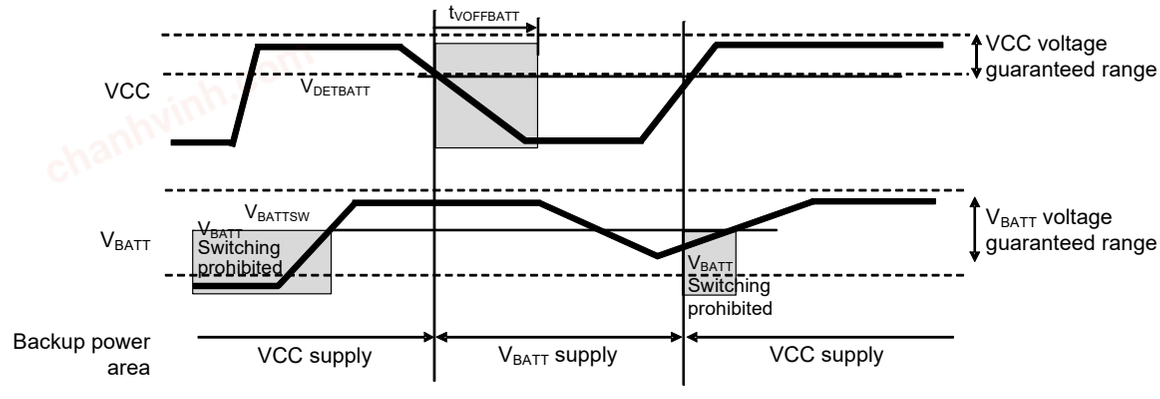
2.11 Battery Backup Function Characteristics

Table 2.61 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.108
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).



Note. The V_{BATT} voltage when the supplied power source switches from VCC to V_{BATT} should not be lower than V_{BATTSW}, the lower-limit V_{BATT} voltage for switching between power supplies due to a drop in the VCC voltage.

Figure 2.108 Battery Backup Function Characteristics

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2.12 Flash Memory Characteristics

Table 2.62 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N_{PEC} ≤ 100 times	128 bytes	t_{P128}	—	0.75	13.2	—	0.38	6.6	—	0.34	6	ms
	8 Kbytes	t_{P8K}	—	49	176	—	25	88	—	22	80	ms
	32 Kbytes	t_{P32K}	—	194	704	—	97	352	—	88	320	ms
Programming time N_{PEC} > 100 times	128 bytes	t_{P128}	—	0.91	15.8	—	0.46	8	—	0.41	7.2	ms
	8 Kbytes	t_{P8K}	—	60	212	—	30	106	—	27	96	ms
	32 Kbytes	t_{P32K}	—	234	848	—	117	424	—	106	384	ms
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	78	216	—	48	132	—	43	120	ms
	32 Kbytes	t_{E32K}	—	283	864	—	173	528	—	157	480	ms
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	94	260	—	58	158	—	52	144	ms
	32 Kbytes	t_{E32K}	—	341	1040	—	208	632	—	189	576	ms
Reprogramming/erasure cycle*1		N_{PEC}	10000 *2	—	—	10000 *2	—	—	10000 *2	—	—	Times
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	132	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	132	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	—	—	1.7	ms
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs
Data hold time*3		t_{DRP}	10	—	—	10	—	—	10	—	—	Year

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

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Table 2.63 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.18	1.9	—	0.16	1.7	ms
Erasure time	64 bytes	t_{DP64}	—	3.1	18	—	1.9	11	—	1.7	10	ms
	128 bytes	t_{DP128}	—	4.7	27	—	2.9	16	—	2.6	15	ms
	256 bytes	t_{DP256}	—	8.9	50	—	5.4	31	—	4.9	28	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	33	—	—	30	µs
	64 bytes	t_{DBC64}	—	—	280	—	—	110	—	—	100	µs
	2 Kbytes	t_{DBC2K}	—	—	6160	—	—	2420	—	—	2200	µs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	100000 *2	—	—	Times
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	132	—	—	120	µs
First suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	216	—	—	132	—	—	120	µs
	128 bytes	—	—	—	216	—	—	132	—	—	120	µs
	256 bytes	—	—	—	216	—	—	132	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Suspend delay time during erasing (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	10	—	—	Year

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

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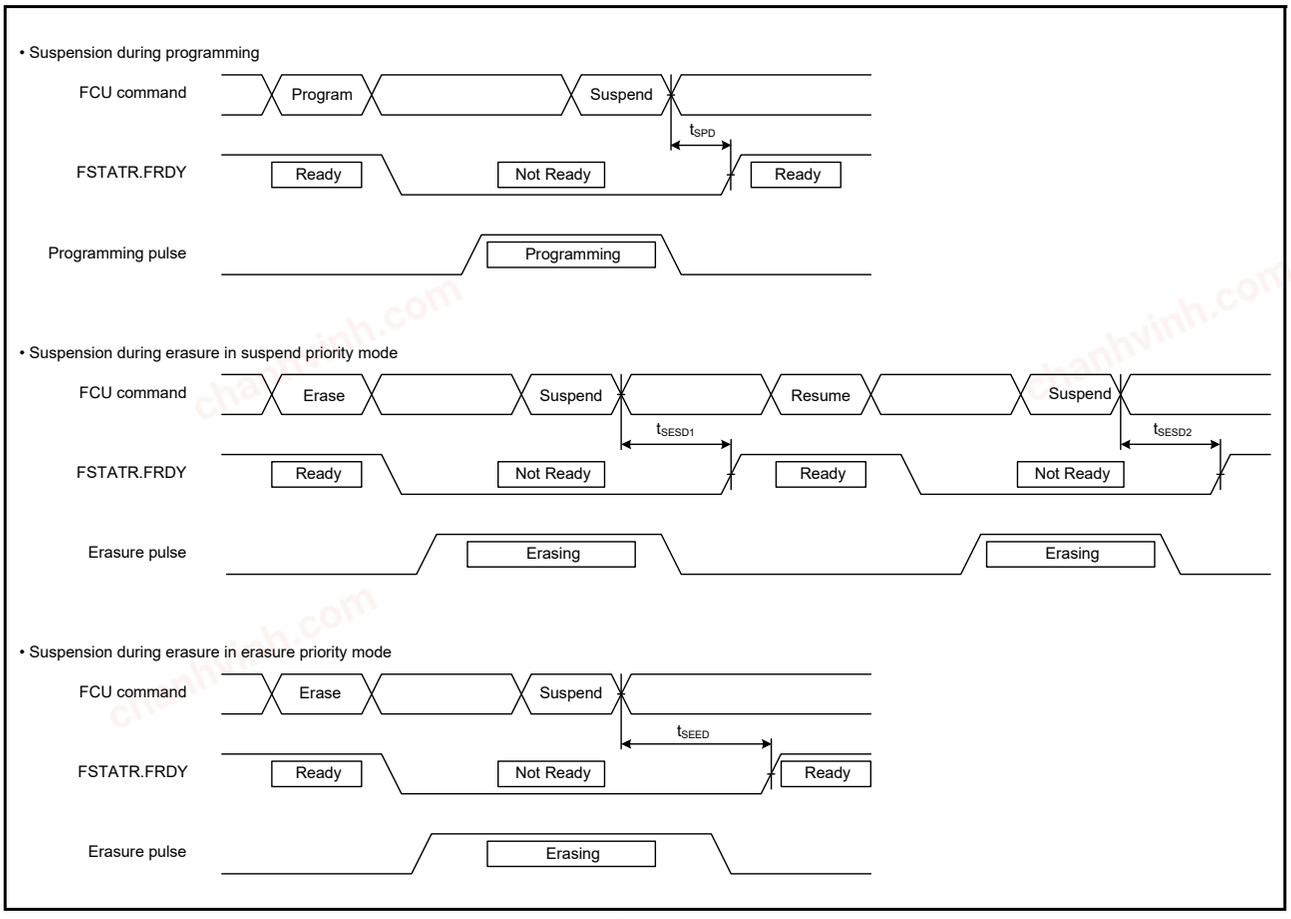


Figure 2.109 Flash Memory Programming/Erasure Suspension Timing

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2.13 Boundary Scan

Table 2.64 Boundary Scan Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 2.110
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 2.111
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 2.112
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

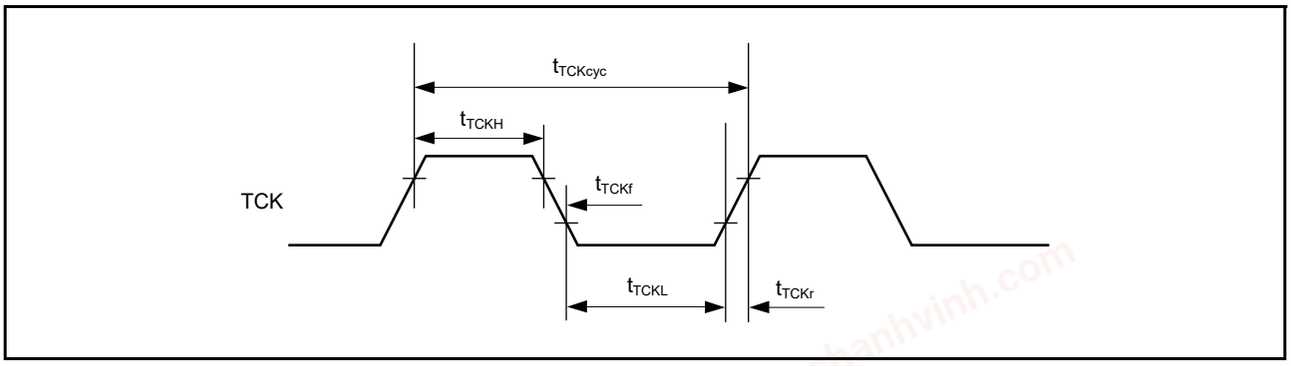


Figure 2.110 Boundary Scan TCK Timing

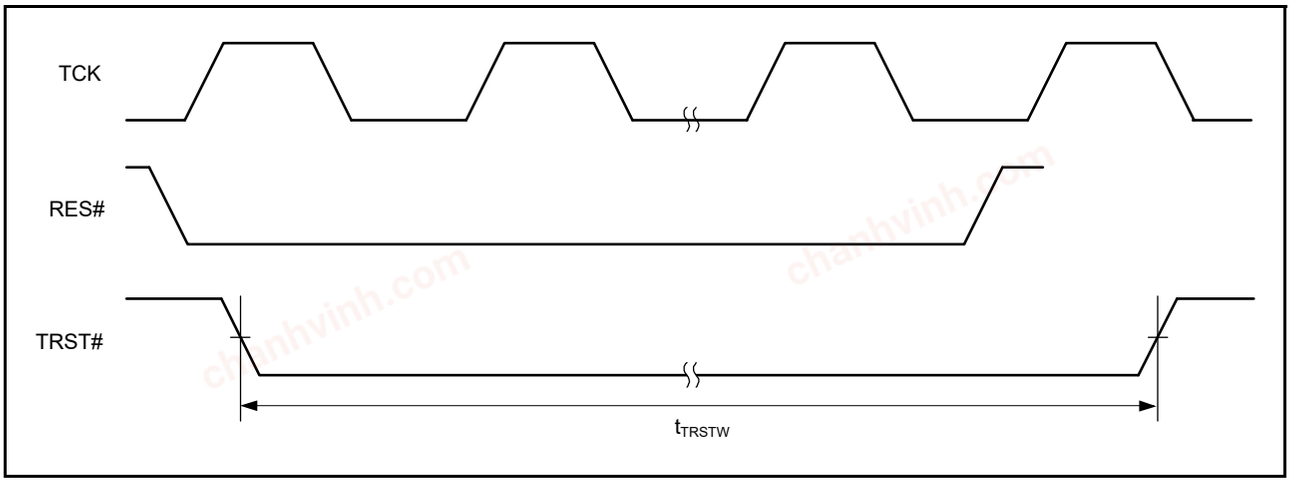


Figure 2.111 Boundary Scan TRST# Timing

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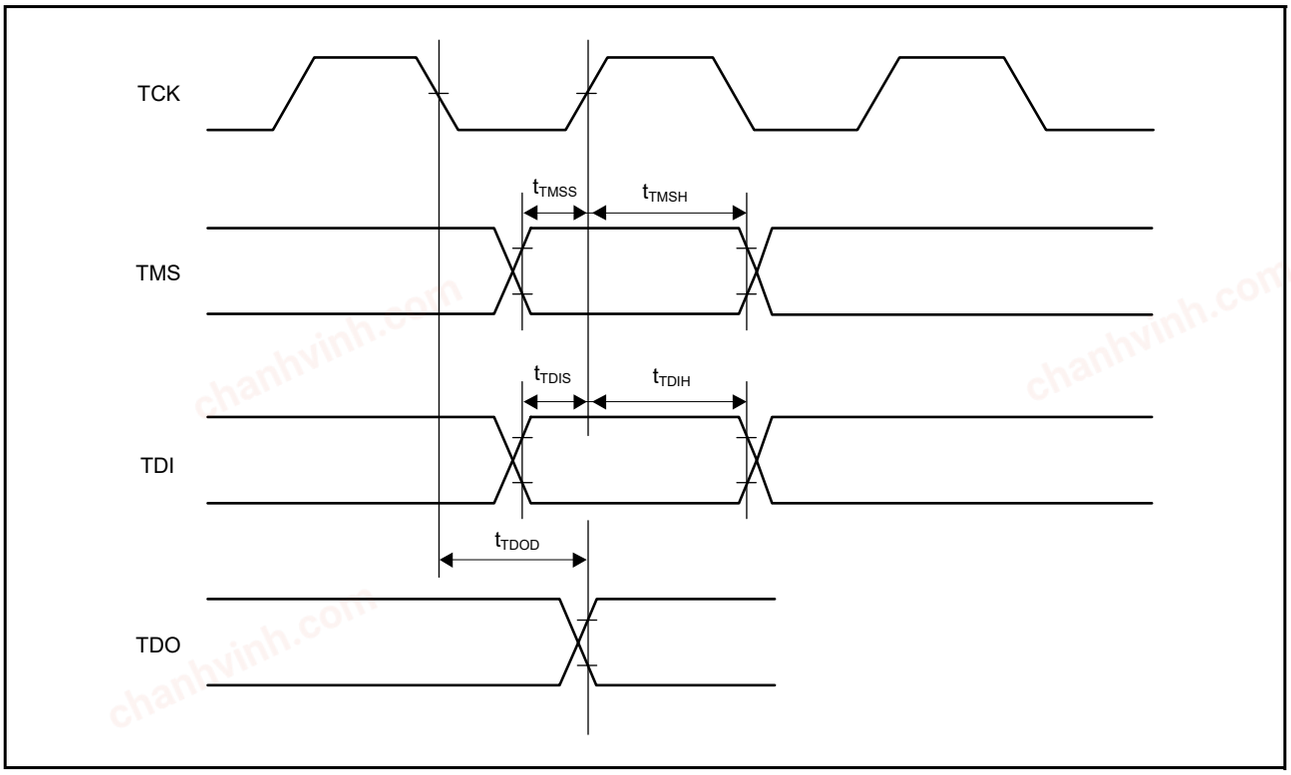


Figure 2.112 Boundary Scan Input/Output Timing

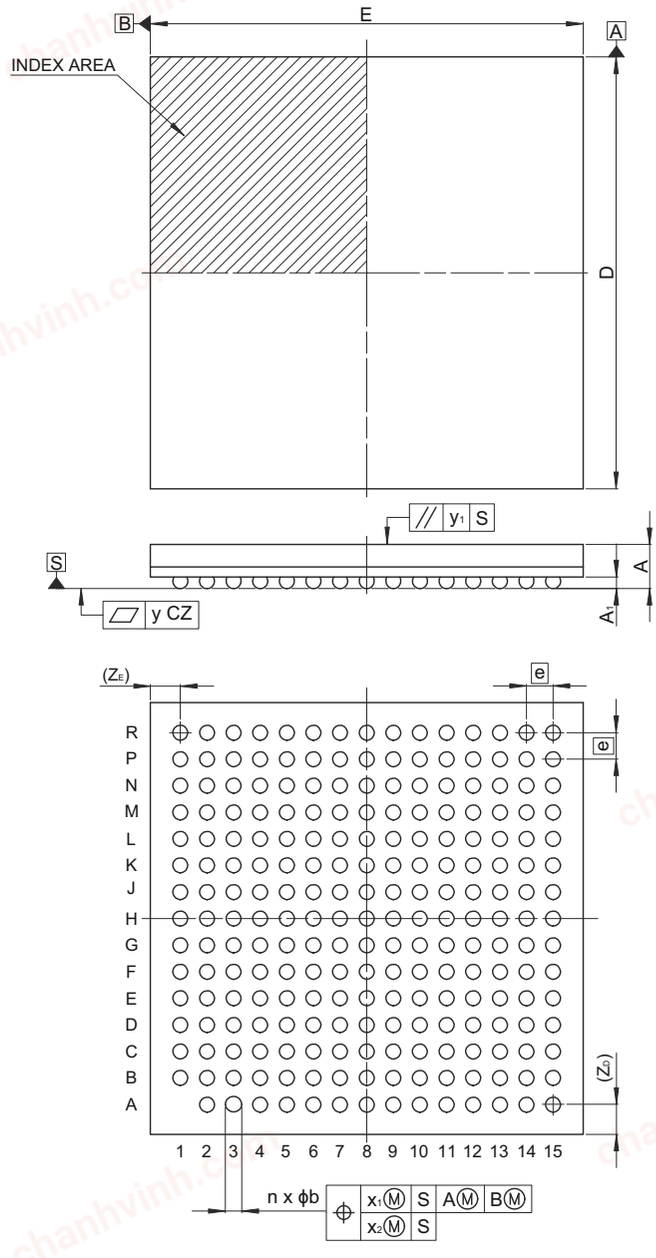
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Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFBGA224-13x13-0.80	PLBG0224GA-A	224FHE	0.4

Unit: mm

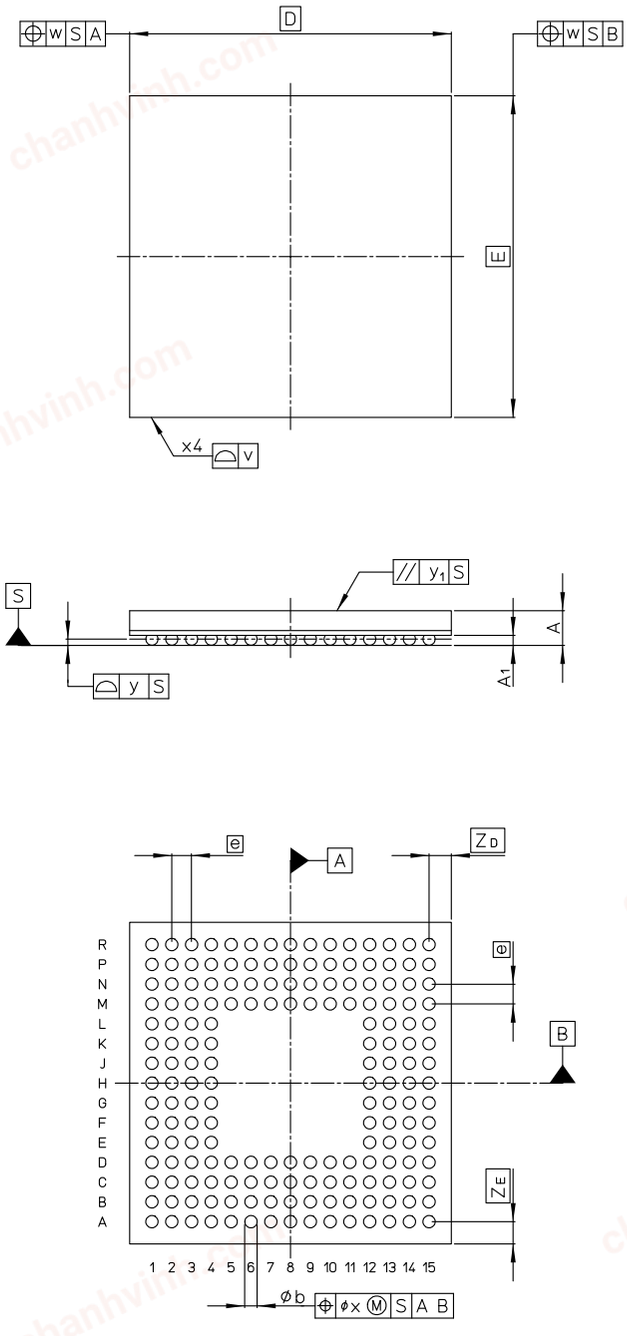


Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	12.9	13.0	13.1
E	12.9	13.0	13.1
A	—	—	1.40
A_1	0.30	0.35	0.40
e	—	0.80	—
b	0.40	0.45	0.50
x_1	—	—	0.15
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
n	—	224	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure A 224-Pin LFBGA (PLBG0224GA-A)

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JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g

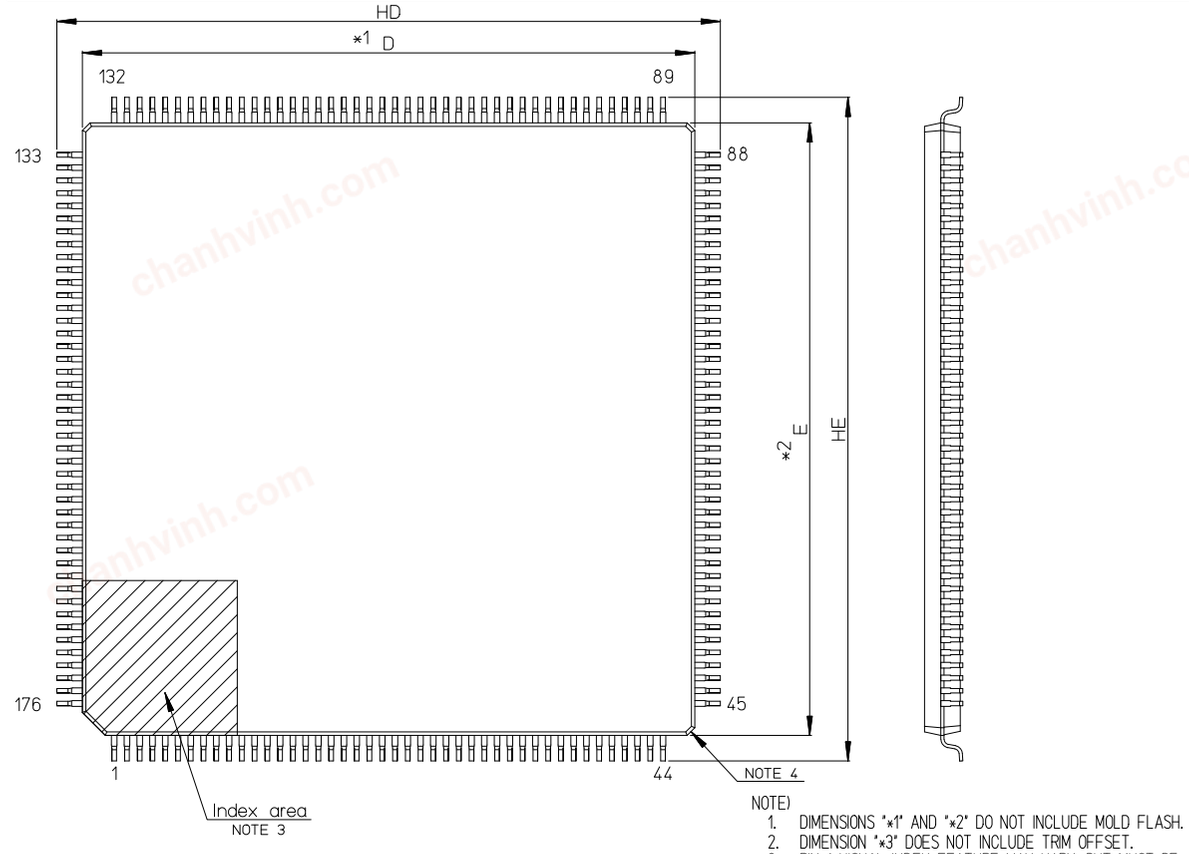


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

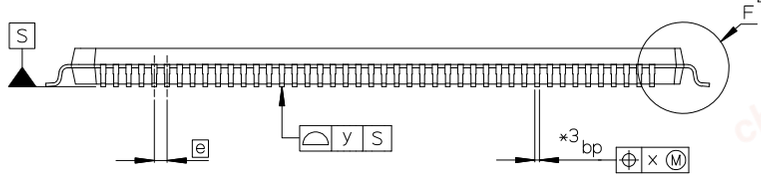
Figure B 176-Pin LFBGA (PLBG0176GA-A)

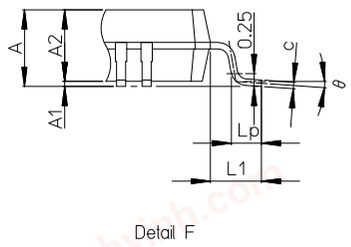
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JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-C	——	1.8g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.





Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.8	24.0	24.2
E	23.8	24.0	24.2
A2	——	1.4	——
HD	25.8	26.0	26.2
HE	25.8	26.0	26.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure C 176-Pin LFQFP (PLQP0176KB-C)

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REVISION HISTORY	RX72M Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	May 31, 2019	—	First edition, issued	

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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